

ISL54103

DDC Accelerator (DDCA)

**EOL PRODUCT  
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FN6303  
Rev 2.00  
October 14, 2011

The ISL54103 DDC Accelerator (DDCA) is a dual active pull-up bus terminator designed to improve data transmission speed on the DDC 2-wire serial bus interfaces.

The DDCA detects rising input transitions with two internal voltage references and two comparators per channel. After the voltage on a data line crosses the first threshold ( $V_{TRIPL}$ ), the boost pull-up current source is activated to speed transition. After the voltage crosses the second threshold ( $V_{TRIPH}$ ), the boost pull-up current source is de-activated, leaving an active pull-up current of 275 $\mu$ A on the line. When both channels are HIGH, the pull-up current for both lines is reduced to 100 $\mu$ A to save power. Internal logic ensures that the active and boost pull-up current sources are not activated during downward transitions.

The level for  $V_{TRIPH}$  is controlled by a bandgap voltage referred to  $V_{DD}$ . This feature makes the switching behavior invariant for all power supply voltages between 2.7V and 5.5V.

A noise filter on each channel prevents the circuit from responding to input transitions that do not exceed a voltage-time threshold. To activate the boost circuit, the input must exceed  $V_{TRIPL}$  by 100Vns (typical) (See Figure 10).

The DDCA permits operation of the bus at frequencies up to 100kHz, despite the capacitive loads of multiple devices and/or long PC board traces. Enhanced ESD protection on the accelerator pins are guaranteed to withstand 8kV ESD (HBM) events.

The DDC Accelerator provides an essential function in DDC applications because of distributed capacitance of the DDC wires in long video cables. By incorporating DDCA, systems using DDC can reliably increase their bus load, allowing longer cables, without the risk of data corruption.

**Features**

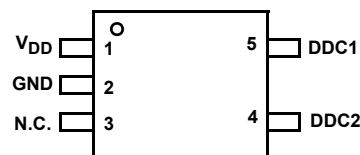
- Active Termination for DDC Lines
- Enhances System Bus Signal Rise Time
- More Reliable HDCP Performance In Video Multiplexers and Cable Extenders
- Increases Maximum Cable Length While Guaranteeing Data Integrity
- 2.2mA Current Boost on Low to High Transitions
- 8kV ESD Protection on SDA and SCL Pins
- Wide Operating Voltage Range: 2.7V to 5.5V
- Small Package - 5 Ld SOT-23
- Pb-free (RoHS Compliant)

**Target Applications**

- Video Multiplexers
- Video Cable Extenders
- Video Distribution Amplifiers
- Televisions
- Computer Monitors
- Projectors

**Pinout**

ISL54103  
(5 LD SOT-23)  
TOP VIEW



## Pin Descriptions

| SOT-23 | SYMBOL          | DESCRIPTION                   |
|--------|-----------------|-------------------------------|
| 1      | V <sub>DD</sub> | Supply Voltage                |
| 2      | GND             | Ground                        |
| 3      | N.C.            | No Connect                    |
| 4      | DDC1            | Active Pull-Up for DDC Signal |
| 5      | DDC2            | Active Pull-Up for DDC Signal |

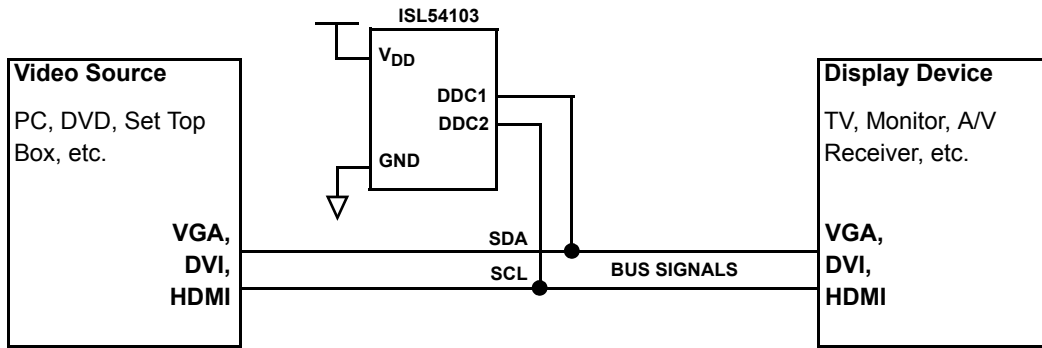
## Ordering Information

| PART NUMBER<br>(Notes 1, 2, 3) | PART MARKING<br>(Note 4) | TEMP<br>RANGE (°C) | PACKAGE<br>(Pb-free) | PKG.<br>DWG. # |
|--------------------------------|--------------------------|--------------------|----------------------|----------------|
| ISL54103IHZ-T7                 | 103Z                     | -40 to +85         | 5 Ld SOT-23          | P5.064         |
| ISL54103IHZ-T7A                | 103Z                     | -40 to +85         | 5 Ld SOT-23          | P5.064         |

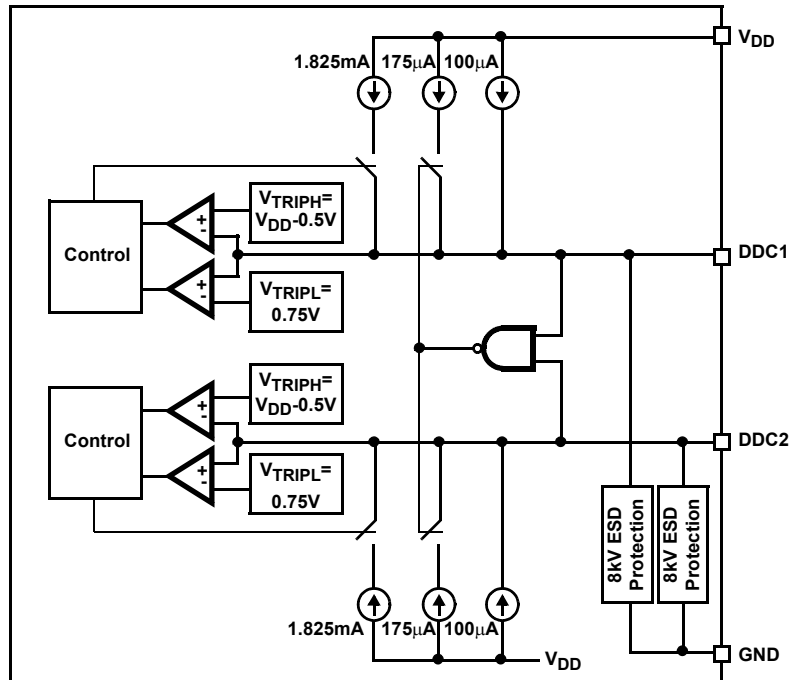
### NOTES:

1. Please refer to [TB347](#) for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for [ISL54103](#). For more information on MSL please see techbrief [TB363](#).
4. The part marking is located on the bottom of the part.

**System Diagram**



**IC Block Diagram**



**Absolute Maximum Ratings**

|                                |                        |
|--------------------------------|------------------------|
| Supply Voltage Range           | -1V to 6.5V            |
| Operating Junction Temperature | +135°C                 |
| Storage Temperature Range      | -65°C to +150°C        |
| Voltage on Pins                | -0.3V to $V_{DD}+0.3V$ |
| ESD Min Other Pins (HBM)       | >2kV                   |
| ESD DDC1 and DDC2 Pins (HBM)   | >8kV                   |

**Thermal Information**

Pb-Free Reflow Profile. . . . . see link below  
<http://www.intersil.com/pbfree/Pb-FreeReflow.asp>

**Recommended Operating Conditions**

Temperature . . . . . -40°C to +85°C  
 Supply Voltage. . . . . 2.7V to 5.5V

**CAUTION:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

**Electrical Specifications** Over all operating conditions unless otherwise specified, Typical values are measured at  $V_{DD} = 3.3V$  and  $T_A = +25^\circ C$

| SYMBOL                   | PARAMETER                                    | CONDITIONS                                   | MIN<br>(Note 6) | TYP             | MAX<br>(Note 6) | UNIT    |
|--------------------------|--|--|-----------------|-----------------|-----------------|---------|
| <b>ANALOG PARAMETERS</b> |  |  |                 |                 |                 |         |
| $V_{DD}$                 | Supply Voltage Range                         |  | 2.7             |                 | 5.5             | V       |
| $V_{DD\ RAMP}$           | $V_{DD}$ Ramp Rate                           |  | 0.05            |                 | 50              | V/ms    |
| $I_{DD}$                 | Supply Current                               | DDC1 = DDC2 = Open                           |                 | 80              | 100             | $\mu A$ |
| $I_{OUT\_SB}$            | Standby Pull-Up Current                      | DDC1 = DDC2 = $V_{DD} - 1.0V$                |                 | 80              | 125             | $\mu A$ |
| $I_{OUT\_A1}$            | Active Pull-Up Current                       | DDC1 = GND; DDC2 = Open                      | 125             | 275             | 350             | $\mu A$ |
| $I_{OUT\_A2}$            |  | DDC1 = Open; DDC2 = GND                      | 125             | 275             | 350             | $\mu A$ |
| $I_{OUT\_B1}$            | Boost Pull-Up Current (Figure 2)             | $V_{TRIPL} < DDC1 < V_{TRIPH}$ , DDC2 = Open | 1.6             | 2.2             |                 | mA      |
| $I_{OUT\_B2}$            |  | $V_{TRIPL} < DDC2 < V_{TRIPH}$ , DDC1 = Open | 1.6             | 2.2             |                 | mA      |
| $V_{TRIPL}$              | Input Voltage Threshold Low                  |  | 0.65            | 0.75            | 0.85            | V       |
| $V_{TRIPH}$              | Input Voltage Threshold High                 |  | $V_{DD} - 0.60$ | $V_{DD} - 0.50$ | $V_{DD} - 0.40$ | V       |
| $f_{MAX}$                | DDC Max Frequency                            |  |                 |                 | 100             | kHz     |
| NSS                      | Noise Spike Suppression (Note 5) (Figure 10) |  |                 | 20              |                 | V-ns    |

**NOTES:**

5. Measured as area under triangular waveform above  $V_{TRIPL}$ , with time as base and  $V_{IN}$  as height (See Figure 10).
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.

**Typical Performance Curves**

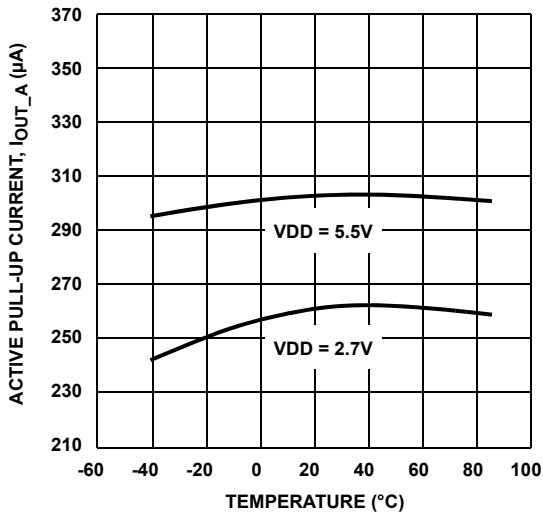


FIGURE 1. ACTIVE PULL-UP CURRENT, DDC PIN = 0V

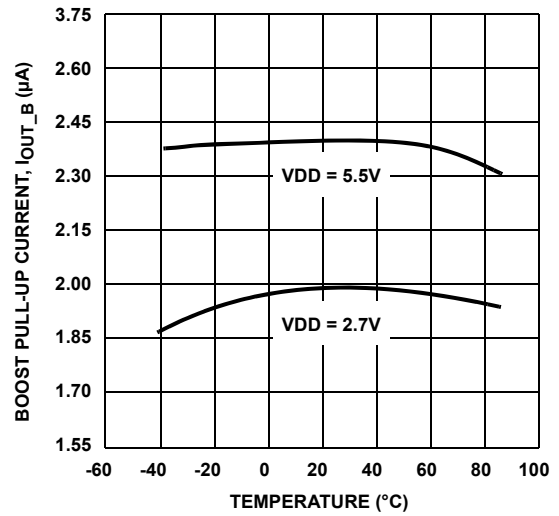


FIGURE 2. BOOST PULL-UP CURRENT, DDC PIN = V<sub>DD</sub>/2

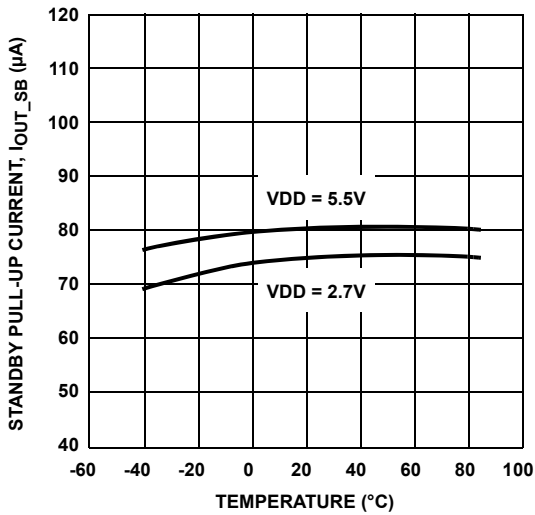


FIGURE 3. STANDBY PULL-UP CURRENT, DDC1, 2 = V<sub>DD</sub> - 0.5V

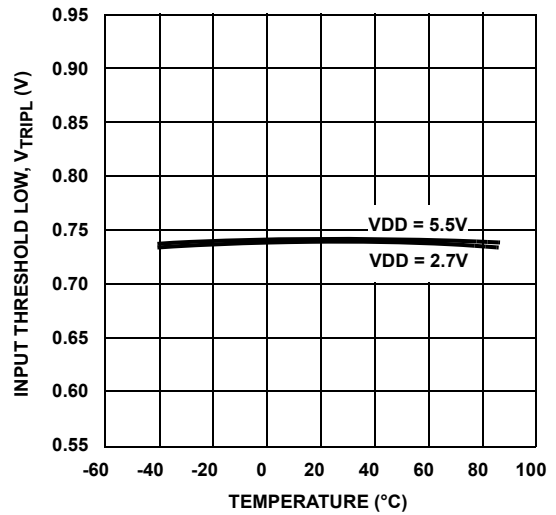


FIGURE 4. V<sub>TRIPL</sub> VOLTAGE

## Typical Performance Curves (Continued)

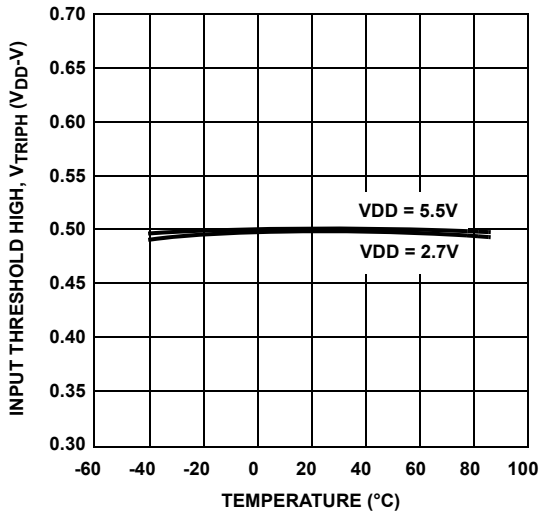
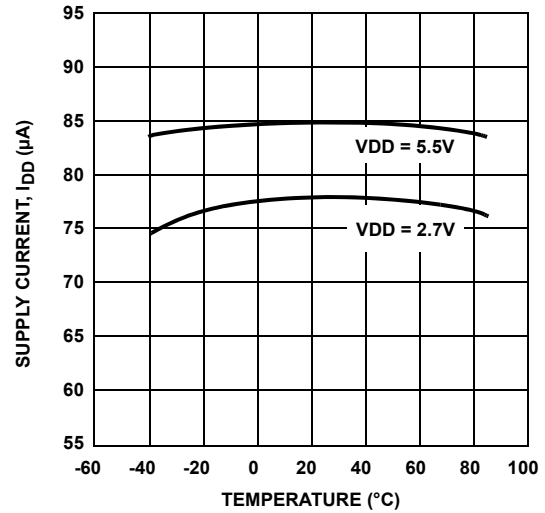
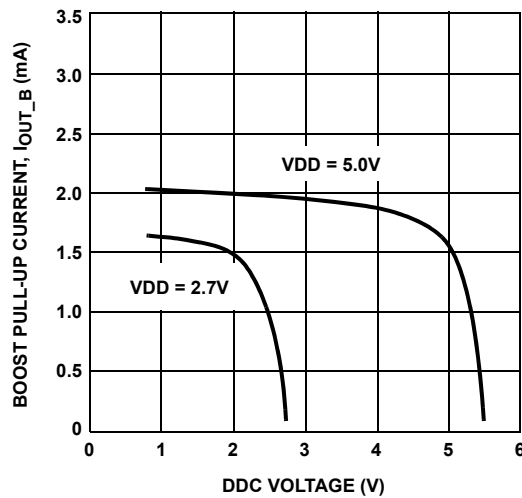
FIGURE 5. V<sub>TRIP\_H</sub> VOLTAGEFIGURE 6. I<sub>DD</sub> CURRENT, DDC1 = DDC2 = OPEN

FIGURE 7. BOOST PULL-UP CURRENT vs DDC VOLTAGE

## Functional Description

### DDC Overview

DDC is a 2-wire serial communication standard based on the I<sup>2</sup>C standard. Devices communicate to each other using one clock (SCL) and one data (SDA) line. These are both bidirectional.

Each signal is connected to a positive supply voltage via a current-source or pull-up resistor (see “System Diagram” on page 3). When the bus is free, both lines are HIGH. The output stages of all devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

Simple pull-up resistors on the clock and data lines work well unless there are long signal lines. The combined capacitance of long cables increases the rise time on the signal to such an

extent that the communication becomes unreliable or fails to meet the bus timing specifications. Smaller value resistors can sometimes compensate for the extra capacitance, but this increases the current consumption when the signal lines are pulled LOW.

### ISL54103 Operation

To improve the operation of the DDC where larger bus capacitance exists, the ISL54103 provides active pull-up using switched current sources. When the bus is idle and both lines are HIGH, a standby pull-up current of 100µA is used to maintain the signal level while minimizing power consumption. When either of the two signals is pulled LOW, an active pull-up current of 275µA maintains a good V<sub>OL</sub> noise margin.

When the bus line is released, it is pulled high by the ISL54103 active current until the voltage exceeds the V<sub>TRIP\_L</sub> level for a

period of time. This voltage-time combination filters out noise on the signal line. Once the ISL54103 detects a valid rising edge, a 2.2mA boost current pulls the bus line high very quickly (see Figure 8). This boost current turns off when the input level reaches the  $V_{TRIPH}$  threshold and the pull-up current returns to the active level. If both inputs are HIGH, the pull-up current drops to the standby level of  $100\mu A$ .

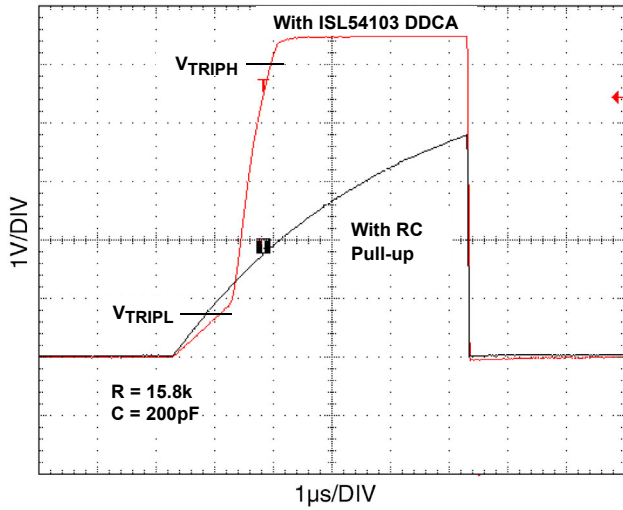


FIGURE 8. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ( $V_{DD} = 5.5V$ )

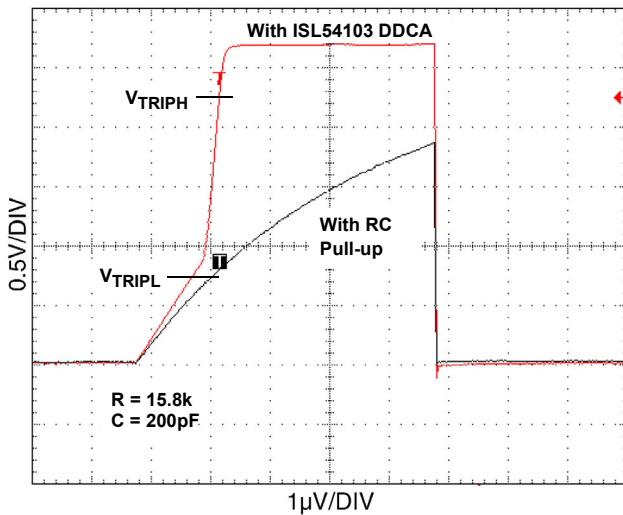


FIGURE 9. ISL54103 DDC SYSTEM BOOST PULL-UP COMPARED TO RESISTOR PULL-UP ( $V_{DD} = 2.7V$ )

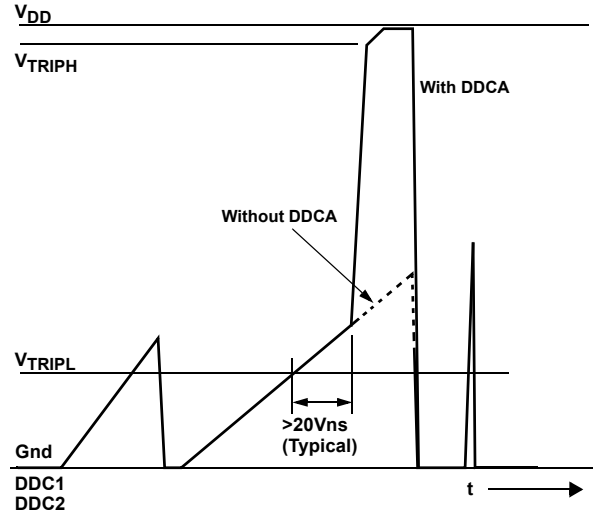


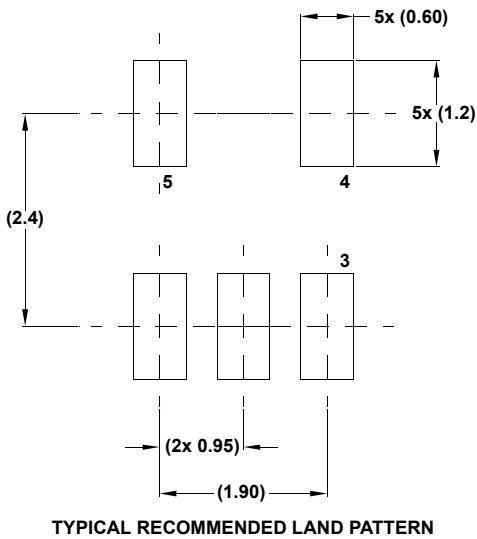
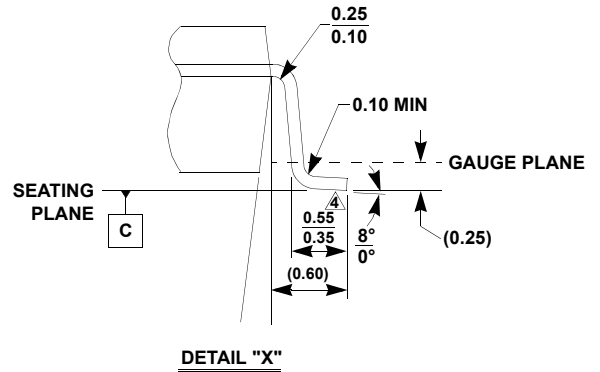
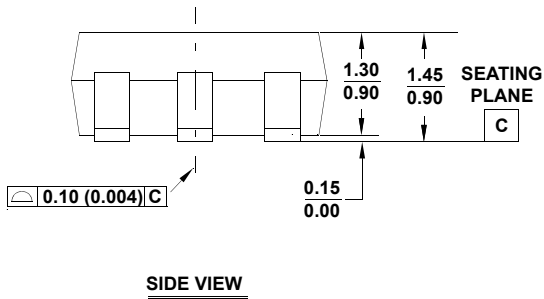
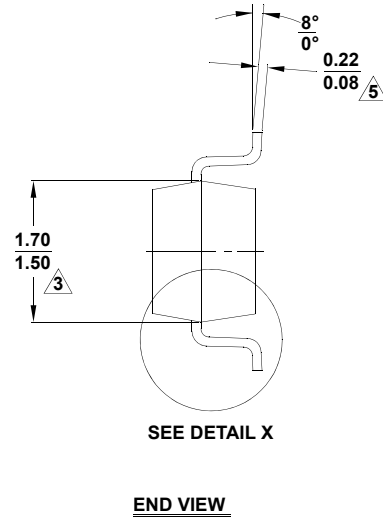
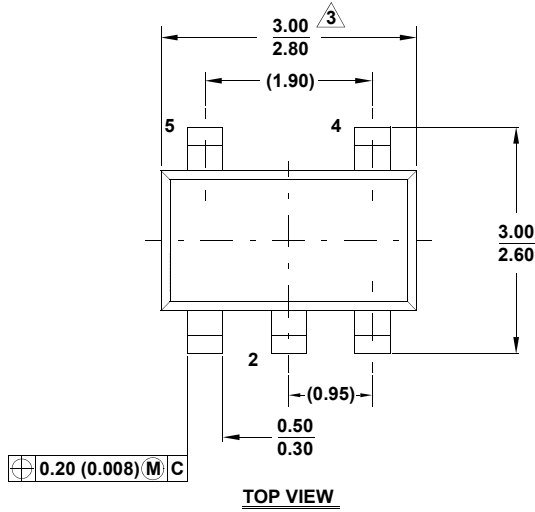
FIGURE 10. NOISE SUPPRESSION. BOOST CURRENT APPLIED WHEN INPUT SIGNAL EXCEEDS 20Vns (TYPICAL)

# Package Outline Drawing

## P5.064

### 5 LEAD SMALL OUTLINE TRANSISTOR PLASTIC PACKAGE

Rev 3, 4/11



**NOTES:**

1. Dimensioning and tolerance per ASME Y14.5M-1994.
2. Package conforms to EIAJ SC-74 and JEDEC MO178AA.
3. Package length and width are exclusive of mold flash, protrusions, or gate burrs.
4. Footlength measured at reference to gauge plane.
5. Lead thickness applies to the flat section of the lead between 0.08mm and 0.15mm from the lead tip.
6. Controlling dimension: MILLIMETER.  
Dimensions in ( ) for reference only.



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#### Renesas Electronics Corporation

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

#### Renesas Electronics America Inc.

1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.  
Tel: +1-408-432-8888, Fax: +1-408-434-5351

#### Renesas Electronics Canada Limited

9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3  
Tel: +1-905-237-2004

#### Renesas Electronics Europe Limited

Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K  
Tel: +44-1628-651-700

#### Renesas Electronics Europe GmbH

Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

#### Renesas Electronics (China) Co., Ltd.

Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

#### Renesas Electronics (Shanghai) Co., Ltd.

Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China  
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

#### Renesas Electronics Hong Kong Limited

Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2265-6688, Fax: +852 2886-9022

#### Renesas Electronics Taiwan Co., Ltd.

13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

#### Renesas Electronics Singapore Pte. Ltd.

80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949  
Tel: +65-6213-0200, Fax: +65-6213-0300

#### Renesas Electronics Malaysia Sdn.Bhd.

Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

#### Renesas Electronics India Pvt. Ltd.

No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India  
Tel: +91-80-67208700, Fax: +91-80-67208777

#### Renesas Electronics Korea Co., Ltd.

17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5338