# ISL6596

Synchronous Rectified MOSFET Driver

FN9240
Rev.3.00
May 30, 2018

The ISL6596 is a high frequency, MOSFET driver optimized to drive two N-Channel power MOSFETs in a synchronous buck converter topology. Combine this driver with the Renesas Multi-Phase Buck PWM controllers to form a complete single-stage core-voltage regulator solution with high efficiency performance at high switching frequency for advanced microprocessors.

The IC is biased by a single low voltage supply (5V), minimizing driver switching losses in high MOSFET gate capacitance and high switching frequency applications. Each driver can drive a 3nF load with less than 10ns rise/fall time. Bootstrapping of the upper gate driver is implemented with an internal low forward drop diode, reducing implementation cost, complexity, and allowing the use of higher performance, cost effective N-Channel MOSFETs. Adaptive shoot-through protection is integrated to prevent both MOSFETs from conducting simultaneously.

The ISL6596 features 4A typical sink current for the lower gate driver, enhancing the lower MOSFET gate hold-down capability during the PHASE node rising edge and preventing power loss caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

The ISL6596 also features an input that recognizes a high-impedance state, working with Renesas multi-phase 3.3V or 5V PWM controllers to prevent negative transients on the controlled output voltage when operation is suspended. This feature eliminates the need for the Schottky diode that may be used in a power system to protect the load from negative output voltage damage.

## Applications

- Core voltage supplies for Intel® and AMD® microprocessors
- High frequency low profile high efficiency DC/DC converters
- High current low voltage DC/DC converters
- Synchronous rectification for isolated power supplies

## Related Literature

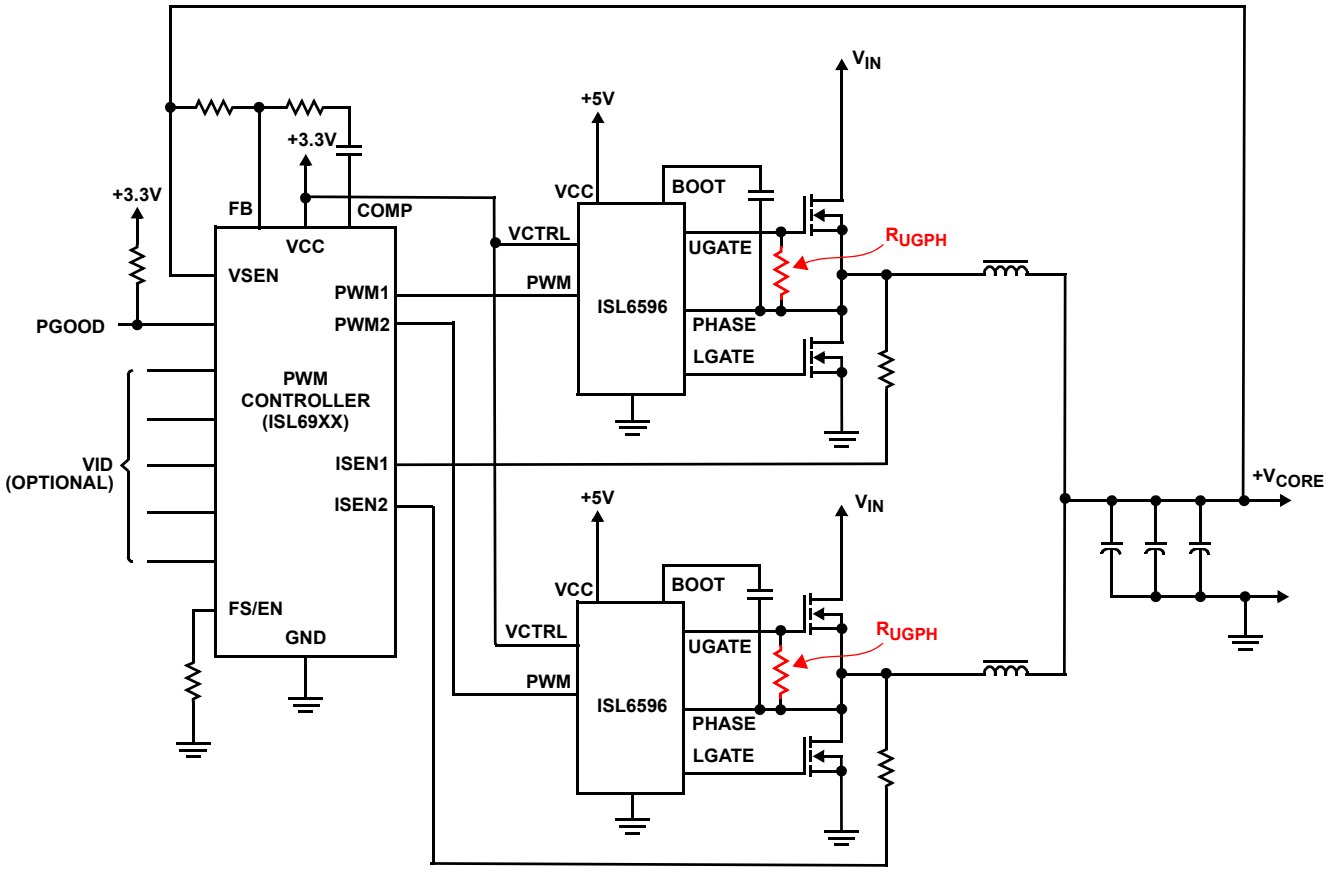
For a full list of related documents, visit our website

- ISL6596 product page

## Features

- Drives two N-Channel MOSFETs
- Adaptive shoot-through protection
- 0.4Ω on-resistance and 4A sink current capability
- Supports high switching frequency
- Fast output rise and fall time
- Low tri-state hold-off time (20ns)
- Supports 3.3V and 5V PWM inputs
- Low quiescent supply current
- Power-On reset
- Expandable bottom copper pad for heat spreading
- Dual Flat No-Lead (DFN) package
  - Compliant to JEDEC PUB95 MO-220 QFN-Quad Flat No Leads - product outline
  - Near chip-scale package footprint improves PCB efficiency and is thinner in profile
- Pb-Free (RoHS compliant)

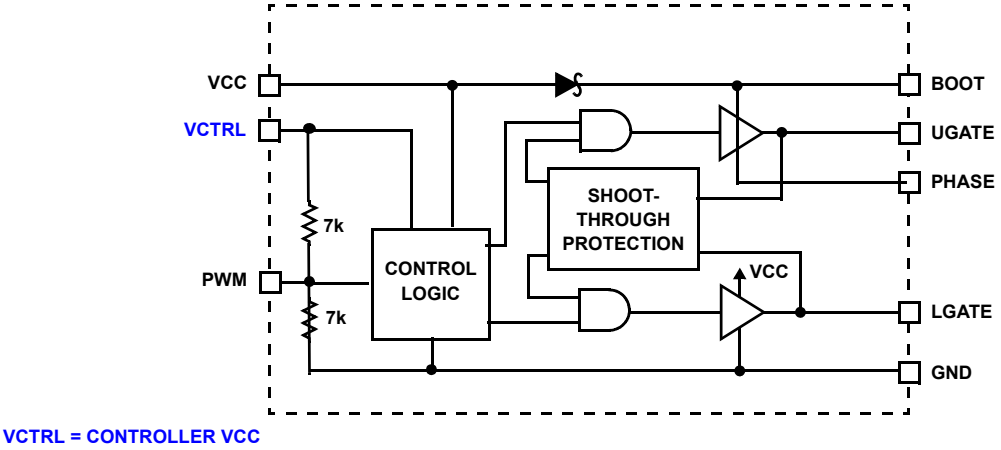
## Typical Application




RUGPH IS REQUIRED FOR SPECIAL POWER SEQUENCING APPLICATIONS

FIGURE 1. MULTI-PHASE CONVERTER USING ISL6596 GATE DRIVERS (SEE "APPLICATION INFORMATION" ON PAGE 9)

## Block Diagram




VCTRL = CONTROLLER VCC

FIGURE 2. BLOCK DIAGRAM

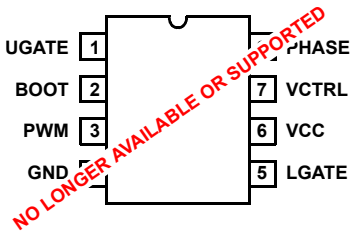
# Ordering Information

| PART NUMBER (Notes 2, 3) | PART MARKING | TEMP RANGE (°C) | TAPE AND REEL (UNITS) (Note 1) | PACKAGE (RoHS COMPLIANT) | PKG. DWG. # |
|---|---|---|---|---|---|
| ISL6596CBZ (No longer available, recommended replacement: ISL6596CRZ) | 6596 CBZ | 0 to +70 | - | 8 Ld SOIC | M8.15 |
| ISL6596CRZ | 596Z | 0 to +70 | - | 10 Ld 3x3 DFN | L10.3x3C |
| ISL6596CRZ-T | 596Z | 0 to +70 | 6k | 10 Ld 3x3 DFN | L10.3x3C |
| ISL6596IBZ (No longer available, recommended replacement: ISL6596IRZ) | 6596 IBZ | -40 to +85 | - | 8 Ld SOIC | M8.15 |
| ISL6596IRZ | 96IZ | -40 to +85 | - | 10 Ld 3x3 DFN | L10.3x3C |
| ISL6596IRZ-T | 96IZ | -40 to +85 | 6k | 10 Ld 3x3 DFN | L10.3x3C |

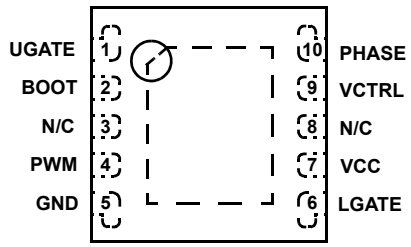
1. Refer to TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), refer to the ISL6596 product information page. For more information about MSL, see TB363.

# Pinouts

8 LD SOIC
TOP VIEW




10 LD DFN
TOP VIEW




# Functional Pin Descriptions

| PIN NUMBER (Note 4) | PIN NAME | DESCRIPTION |
|---|---|---|
| 1 | UGATE | Upper gate drive output. Connect to the gate of the high-side N-Channel power MOSFET. A gate resistor is never recommended on this pin because it interferes with the operation shoot-through protection circuitry. |
| 2 | BOOT | Floating bootstrap supply pin for the upper gate drive. Connect a bootstrap capacitor between this pin and the PHASE pin. The bootstrap capacitor provides the charge used to turn on the upper MOSFET. See "Bootstrap Considerations" on page 7 for information about choosing the appropriate capacitor value. |
| 3, 8 | N/C | Do not connect. |
| 4 | PWM | Driver control input. The PWM signal can enter three distinct states during operation. See "PWM Input and Threshold Control" on page 7 for more information. Connect this pin to the controller PWM output. |
| 5 | GND | Ground pin. All signals are referenced to this node. |
| 6 | LGATE | Lower gate drive output. Connect to the gate of the low side N-Channel power MOSFET. A gate resistor is never recommended on this pin because it interferes with the operation shoot-through protection circuitry. |
| 7 | VCC | Connect this pin to a +5V bias supply. Bypass locally to ground with a high quality ceramic capacitor. |

# Functional Pin Descriptions

| PIN NUMBER (Note 4) | PIN NAME | DESCRIPTION |
|---|---|---|
| 9 | VCTRL | Sets the PWM logic threshold. Connect this pin to a 3.3V source for 3.3V PWM input and pull it to a 5V source for 5V PWM input. |
| 10 | PHASE | Provides the return path for the upper gate driver current. Connect this pin to the upper MOSFET source. |
| - | Thermal Pad (DFN package only) | The metal pad underneath the center of the IC is a thermal substrate. The PCB “thermal land” design for this exposed die pad should include vias that drop down and connect to one or more buried copper plane(s). This combination of vias for vertical heat escape and buried planes for heat spreading allows the DFN to achieve its full thermal potential. This pad should be either grounded or floating, and it should not be connected to other nodes. Refer to TB389 for design guidelines. |

NOTES:

4. Pin numbers refer to the DFN package. Refer to “Pinouts” on page 3 for the corresponding SOIC pinout.

## Absolute Maximum Ratings

Supply Voltage (VCC, VCTRL) . . . . . -0.3V to 7V
Input Voltage ($V_{EN}$, $V_{PWM}$) . . . . . -0.3V to $V_{CC}$ + 0.3V
BOOT Voltage ($V_{BOOT-GND}$) . . . . . -0.3V to 33V (DC) or 36V (<200ns)
BOOT To PHASE Voltage ($V_{BOOT-PHASE}$) . . . . . -0.3V to 7V (DC)
. . . . . -0.3V to 9V (<10ns)
PHASE Voltage . . . . . (GND - 0.3V) to 30V (DC)
. . . . . GND - 8V (<20ns Pulse-Width, 10µJ) to 30V (<100ns)
UGATE Voltage . . . . . $V_{PHASE}$ - 0.3V (DC) to $V_{BOOT}$
. . . . . $V_{PHASE}$ - 5V (<20ns Pulse-Width, 10µJ) to $V_{BOOT}$
LGATE Voltage . . . . . GND - 0.3V (DC) to $V_{CC}$ + 0.3V
. . . . . GND - 2.5V (<20ns Pulse-Width, 5µJ) to $V_{CC}$ + 0.3V
Ambient Temperature Range . . . . . -40°C to +125°C
HBM ESD Rating . . . . . 2kV

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| SOIC Package (Note 5) | 110 | N/A |
| DFN Package (Notes 6, 7) | 48 | 7 |

Maximum Junction Temperature . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see TB493

## Recommended Operating Conditions

Ambient Temperature Range . . . . . -40°C to +100°C
Maximum Operating Junction Temperature . . . . . +125°C
Supply Voltage, VCC . . . . . 5V ±10%

*CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.*

NOTES:

5. $\theta_{JA}$ is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
6. $\theta_{JA}$ is measured in free air with the component mounted on a high-effective thermal conductivity test board with "direct attach" features. See TB379 for details.
7. For $\theta_{JC}$, the "case temp" location is at the center of the package underside exposed pad.

## Electrical Specifications

These specifications apply to the limits in "Absolute Maximum Ratings", unless otherwise noted.

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 9) | TYP | MAX (Note 9) | UNIT |
|---|---|---|---|---|---|---|
| **VCC SUPPLY CURRENT** | | | | | | |
| Bias Supply Current | $I_{VCC}$ | PWM pin floating, $V_{VCC}$ = 5V | - | 190 | - | µA |
| POR Rising | | | - | 3.4 | 4.2 | V |
| POR Falling | | | 2.2 | 3.0 | - | V |
| Hysteresis | | | - | 400 | - | mV |
| **VCTRL INPUT** | | | | | | |
| Rising Threshold | | | - | 2.75 | 2.90 | V |
| Falling Threshold | | | 2.4 | 2.65 | - | V |
| **PWM INPUT** | | | | | | |
| Sinking Impedance | $R_{PWM\_SNK}$ | | - | 3.5 | - | kΩ |
| Source Impedance | $R_{PWM\_SRC}$ | | - | 3.5 | - | kΩ |
| Tri-State LowerThreshold | | $V_{VCTRL}$ = 3.3V (-110mV Hysteresis) | - | 1.1 | - | V |
| | | $V_{VCTRL}$ = 5V (-250mV Hysteresis) | - | 1.5 | - | V |
| Tri-State Upper Threshold | | $V_{VCTRL}$ = 3.3V (+110mV Hysteresis) | - | 1.9 | - | V |
| | | $V_{VCTRL}$ = 5V (+250mV Hysteresis) | - | 3.25 | - | V |
| Tri-State Shutdown Holdoff Time | $t_{TSSHD}$ | $t_{PDLU}$ or $t_{PDLL}$ + Gate Falling Time | - | 20 | - | ns |
| **SWITCHING TIME** (See Figure 3 on page 6 ) | | | | | | |
| UGATE Rise Time (Note 8) | $t_{RU}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8.0 | - | ns |
| LGATE Rise Time (Note 8) | $t_{RL}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8.0 | - | ns |
| UGATE Fall Time (Note 8) | $t_{FU}$ | $V_{VCC}$ = 5V, 3nF Load | - | 8.0 | - | ns |
| LGATE Fall Time (Note 8) | $t_{FL}$ | $V_{VCC}$ = 5V, 3nF Load | - | 4.0 | - | ns |
| UGATE Turn-Off Propagation Delay | $t_{PDLU}$ | $V_{VCC}$ = 5V, Outputs Unloaded | - | 20 | - | ns |
| LGATE Turn-Off Propagation Delay | $t_{PDLL}$ | $V_{VCC}$ = 5V, Outputs Unloaded | - | 15 | - | ns |
| UGATE Turn-On Propagation Delay | $t_{PDHU}$ | $V_{VCC}$ = 5V, Outputs Unloaded | - | 19 | - | ns |

## Electrical Specifications These specifications apply to the limits in "Absolute Maximum Ratings", unless otherwise noted. (Continued)

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN (Note 9) | TYP | MAX (Note 9) | UNIT |
|---|---|---|---|---|---|---|
| LGATE Turn-On Propagation Delay | $t_{PDHL}$ | $V_{VCC}$ = 5V, Outputs Unloaded | - | 18 | - | ns |
| Tri-state to UG/LG Rising Propagation Delay | $t_{PTS}$ | $V_{VCC}$ = 5V, Outputs Unloaded | - | 30 | - | ns |
| **OUTPUT** (Note 8) | | | | | | |
| Upper Drive Source Resistance | $R_{UG\_SRC}$ | 250mA Source Current | - | 1.0 | 2.5 | Ω |
| Upper Drive Sink Resistance | $R_{UG\_SNK}$ | 250mA Sink Current | - | 1.0 | 2.5 | Ω |
| Lower Drive Source Resistance | $R_{LG\_SRC}$ | 250mA Source Current | - | 1.0 | 2.5 | Ω |
| Lower Drive Sink Resistance | $R_{LG\_SNK}$ | 250mA Sink Current | - | 0.4 | 1.0 | Ω |

NOTES:

8. Limits established by characterization and are not production tested.
9. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

# Timing Diagram

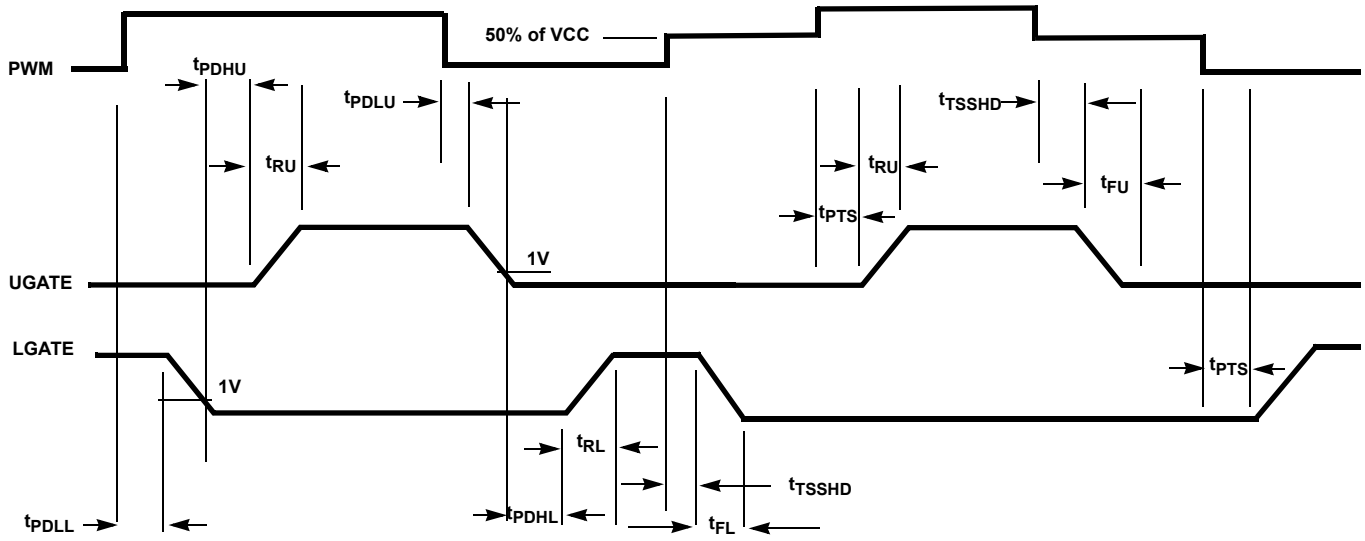



FIGURE 3. TIMING DIAGRAM

## Operation and Adaptive Shoot-Through Protection

The ISL6596 MOSFET driver is designed for high speed switching and controls both high-side and low-side N-Channel FETs from one externally provided PWM signal.

A rising transition on PWM initiates the turn-off of the lower MOSFET (see "Timing Diagram" on page 6). After a short propagation delay ($t_{PDLL}$), the lower gate begins to fall. Typical fall times ($t_{FL}$) are provided in the "Electrical Specifications" table on page 5. Adaptive shoot-through circuitry monitors the LGATE voltage and turns on the upper gate following a short delay ($t_{PDHU}$) after the LGATE voltage drops below ~1V. The upper gate drive then begins to rise ($t_{RU}$) and the upper MOSFET turns on.

A falling transition on PWM indicates the turn-off of the upper MOSFET and the turn-on of the lower MOSFET. A short propagation delay ($t_{PDLU}$) occurs before the upper gate begins to fall ($t_{FU}$). The adaptive shoot-through circuitry monitors the UGATE-PHASE voltage and turns on the lower MOSFET following a short delay time ($t_{PDHL}$) after the upper MOSFET's gate voltage drops below 1V. The lower gate then rises ($t_{RL}$), turning on the lower MOSFET. These methods prevent both the lower and upper MOSFETs from conducting simultaneously (shoot-through), while adapting the dead time to the gate charge characteristics of the MOSFETs being used.

This driver is optimized for voltage regulators with a large step down ratio. The lower MOSFET is usually larger than the upper MOSFET because the lower MOSFET conducts for a longer time during a switching period. The lower gate driver is therefore much larger to meet this application requirement. The 0.4Ω on-resistance and 4A sink current capability enable the lower gate driver to absorb the current injected into the lower gate through the drain-to-gate capacitor of the lower MOSFET and help prevent shoot-through caused by the self turn-on of the lower MOSFET due to the high dV/dt of the switching node.

## PWM Input and Threshold Control

The ISL6596 has a programmable PWM logic threshold set by the control pin (VCTRL) voltage. The VCTRL pin should connect to the VCC of the controller; thus the PWM logic threshold follows the controller voltage level. For 5V applications, this pin can tie to the driver VCC and simplify the routing.

The ISL6596 also features an adaptable tri-state PWM input. When the PWM signal enters the shutdown window, either MOSFET previously conducting is turned off. If the PWM signal remains within the shutdown window for longer than the gate turn-off propagation delay of the previously conducting MOSFET, the output drivers are disabled and both MOSFET gates are pulled and held low. The shutdown state is removed when the PWM signal moves outside the shutdown window. The PWM rising and falling thresholds in the "Electrical Specifications" beginning on page 5 determine when the lower and upper gates are enabled. During normal operation in a typical application, the PWM rise and fall times through the shutdown window should not exceed either output's turn-off propagation delay plus the MOSFET gate discharge time to ~1V. Abnormally long PWM signal transition times through the shutdown window will simply introduce additional dead time between turn-off and turn-on of the synchronous bridge's MOSFETs. For optimal performance, no more than 50pF parasitic capacitive load should be present on the PWM line of ISL6596 (assuming a Renesas PWM controller is used).

## Bootstrap Considerations

This driver features an internal bootstrap diode. Add an external capacitor across the BOOT and PHASE pins to complete the bootstrap circuit.

Use Equation 1 to select a proper bootstrap capacitor size:

$$C_{BOOT\_CAP} \geq \frac{Q_{GATE}}{\Delta V_{BOOT\_CAP}} \quad \text{(EQ. 1)}$$

$$Q_{GATE} = \frac{Q_{G1} \bullet VCC}{V_{GS1}} \bullet N_{Q1}$$

where $Q_{G1}$ is the amount of gate charge per upper MOSFET at $V_{GS1}$ gate-source voltage and $N_{Q1}$ is the number of control MOSFETs. $\Delta V_{BOOT\_CAP}$ is the allowable droop in the rail of the upper gate drive.

As an example, suppose two IRLR7821 FETs are chosen as the upper MOSFETs. The gate charge, $Q_G$, from the data sheet is 10nC at 4.5V ($V_{GS}$) gate-source voltage. The $Q_{GATE}$ is calculated to be 22nC at $V_{CC}$ level. Assume a 200mV droop in drive voltage over the PWM cycle. A bootstrap capacitance of at least 0.110µF is required. The next larger standard value capacitance is 0.22µF. A good quality ceramic capacitor is recommended.

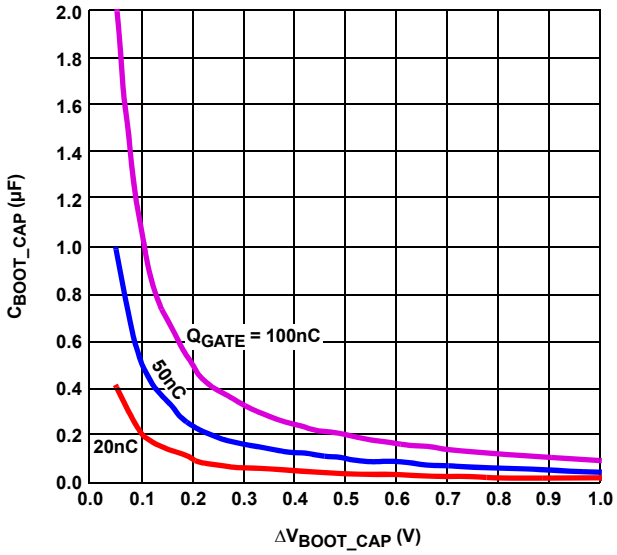



FIGURE 4. BOOTSTRAP CAPACITANCE vs BOOT RIPPLE VOLTAGE

## Power Dissipation

Package power dissipation is mainly a function of the switching frequency ($f_{SW}$), the output drive impedance, the external gate resistance, and the selected MOSFET's internal gate resistance and total gate charge. Calculating the power dissipation in the driver for a desired application is critical to ensure safe operation. Exceeding the maximum allowable power dissipation level pushes the IC beyond the maximum recommended operating junction temperature of +125°C. The maximum allowable IC power dissipation for the SO8 package is

approximately 800mW at room temperature, while the power dissipation capacity in the DFN package, with an exposed heat escape pad, is much higher. See "Layout Considerations" on page 9 for thermal transfer improvement suggestions. When designing the driver into an application, it is recommended that the following calculation is used to ensure safe operation at the desired frequency for the selected MOSFETs. The total gate drive power losses due to the gate charge of MOSFETs and the driver's internal circuitry and their corresponding average driver current can be estimated with Equations 2 and 3, respectively:

$$P_{Qg\_TOT} = P_{Qg\_Q1} + P_{Qg\_Q2} + I_Q \bullet VCC$$

$$P_{Qg\_Q1} = \frac{Q_{G1} \bullet VCC^2}{V_{GS1}} \bullet f_{SW} \bullet N_{Q1} \quad \text{(EQ. 2)}$$

$$P_{Qg\_Q2} = \frac{Q_{G2} \bullet VCC^2}{V_{GS2}} \bullet f_{SW} \bullet N_{Q2}$$

$$I_{VCC} = \left(\frac{Q_{G1} \bullet N_{Q1}}{V_{GS1}} + \frac{Q_{G2} \bullet N_{Q2}}{V_{GS2}}\right) \bullet VCC \bullet f_{SW} + I_Q \quad \text{(EQ. 3)}$$

where the gate charge ($Q_{G1}$ and $Q_{G2}$) is defined at a particular gate to source voltage ($V_{GS1}$and $V_{GS2}$) in the corresponding MOSFET datasheet, $I_Q$ is the driver's total quiescent current with no load at both drive outputs, $N_{Q1}$ and $N_{Q2}$ are the number of upper and lower MOSFETs, respectively. The $I_Q$ $V_{CC}$ product is the quiescent power of the driver without capacitive load and is typically negligible.

The total gate drive power losses are dissipated among the resistive components along the transition path. The drive resistance dissipates a portion of the total gate drive power losses and the rest is dissipated by the external gate resistors ($R_{G1}$ and $R_{G2}$) and the internal gate resistors ($R_{GI1}$ and $R_{GI2}$) of the MOSFETs. $R_{G1}$ and $R_{G2}$ should be a short to avoid interfering with the operation shoot-through protection circuitry. Figures 5 and 6 show the typical upper and lower gate drives turn-on transition path. The power dissipation on the driver can be roughly estimated as:

$$P_{DR} = P_{DR\_UP} + P_{DR\_LOW} + I_Q \bullet VCC$$

$$P_{DR\_UP} = \left(\frac{R_{HI1}}{R_{HI1} + R_{EXT1}} + \frac{R_{LO1}}{R_{LO1} + R_{EXT1}}\right) \bullet \frac{P_{Qg\_Q1}}{2} \quad \text{(EQ. 4)}$$

$$P_{DR\_LOW} = \left(\frac{R_{HI2}}{R_{HI2} + R_{EXT2}} + \frac{R_{LO2}}{R_{LO2} + R_{EXT2}}\right) \bullet \frac{P_{Qg\_Q2}}{2}$$

$$R_{EXT2} = R_{G1} + \frac{R_{GI1}}{N_{Q1}} \qquad R_{EXT2} = R_{G2} + \frac{R_{GI2}}{N_{Q2}}$$

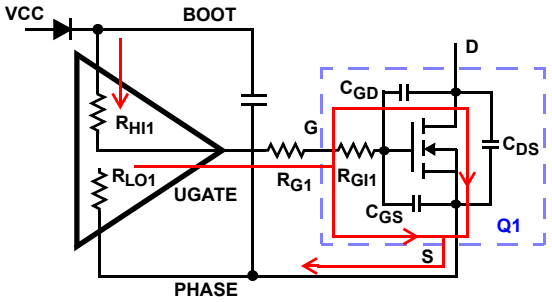



FIGURE 5. TYPICAL UPPER-GATE DRIVE TURN-ON PATH

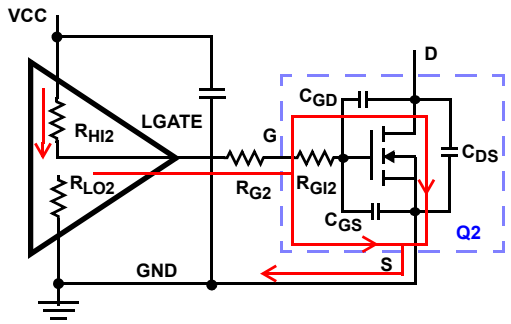



FIGURE 6. TYPICAL LOWER-GATE DRIVE TURN-ON PATH

# Application Information

## MOSFET Selection

The parasitic inductances of the PCB and of the power devices' packaging (both upper and lower MOSFETs) can cause serious ringing that exceeds the absolute maximum rating of the devices. The negative ringing at the edges of the PHASE node can increase the bootstrap capacitor voltage through the internal bootstrap diode, and in some cases, it can overstress the upper MOSFET driver. Careful layout and proper selection of MOSFETs and packaging can minimize this stress.

The $D^2$-PAK, or D-PAK packaged MOSFETs, have large parasitic lead inductances and are not recommended unless additional circuits are implemented to prevent the BOOT and PHASE pins from exceeding the device rating. Low-profile MOSFETs, such as Direct FETs and multi-SOURCE leads devices (SO-8, LFPAK, PowerPAK), have low parasitic lead inductances and are preferred.

## Layout Considerations

A good layout helps reduce the ringing on the switching node (PHASE) and significantly lowers the stress applied to the output drives. Optimize the layout using the following guidelines:

- Keep decoupling loops (VCC-GND and BOOT-PHASE) as short as possible
- Minimize trace inductance, especially on low-impedance lines. All power traces (UGATE, PHASE, LGATE, GND, VCC) should be as short and wide as possible
- Minimize the PHASE node inductance. Ideally, the source of the upper and the drain of the lower MOSFET should be as close as thermally allowable
- Minimize the current loop of the output and input power trains. Short the source connection of the lower MOSFET to ground as close to the transistor pin as possible. Place input capacitors (especially ceramic decoupling) as close to the drain of upper and source of the lower MOSFETs as possible

For proper heat spreading, place copper underneath the IC whether it has an exposed pad or not. The copper area can be extended beyond the bottom area of the IC and/or connected to buried power ground plane(s) with thermal vias. This combination of vias for vertical heat escape, extended copper plane, and buried planes improves heat dissipation and allows the part to achieve its full thermal potential.

## Upper MOSFET Self Turn-On Effects At Startup

If insufficient bias voltage is applied to the driver, its outputs are floating. If the input bus is energized at a high dV/dt rate while the driver outputs are floating because of self-coupling from the internal $C_{GD}$ of the MOSFET, the UGATE can momentarily rise up to a level greater than the threshold voltage of the MOSFET. This can potentially turn on the upper switch and result in cause inrush energy. Therefore, if such a situation (when input bus powered up before the bias of the controller and driver is ready) could occur, place a resistor ($R_{UGPH}$) across the gate and source of the upper MOSFET to suppress the Miller coupling effect. The value of the resistor depends mainly on the input voltage's rate of rise, the $C_{GD}/C_{GS}$ ratio, and the gate-source threshold of the upper MOSFET. A higher dV/dt, a lower $C_{DS}/C_{GS}$ ratio, and a lower gate-source threshold upper FET requires a smaller resistor to diminish the effect of the internal capacitive coupling. For most applications, a 5kΩ to 10kΩ resistor is typically sufficient and does not affect normal performance and efficiency.

The coupling effect can be roughly estimated with Equation 5, which assumes a fixed linear input ramp and neglect the clamping effect of the body diode of the upper drive and the bootstrap capacitor. Other parasitic components, such as lead inductances and PCB capacitances, are also not taken into account. These equations are provided for guidance purpose only. Therefore, examine the actual coupling effect using a very high impedance (10MΩ or greater) probe to ensure a safe design margin.

$$V_{GS\_MILLER} = \frac{dV}{dt} \cdot R \cdot C_{rss}\left(1 - e^{\frac{-V_{DS}}{\frac{dV}{dt} \cdot R \cdot C_{iss}}}\right) \quad \text{(EQ. 5)}$$

$$R = R_{UGPH} + R_{GI} \qquad C_{rss} = C_{GD} \qquad C_{iss} = C_{GD} + C_{GS}$$

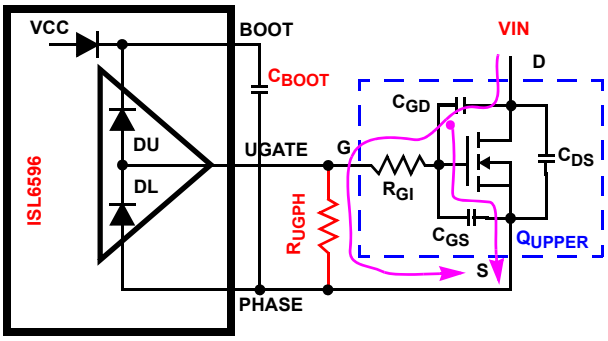



FIGURE 7. GATE TO SOURCE RESISTOR TO REDUCE UPPER MOSFET MILLER COUPLING

## Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please visit our website to make sure you have the latest revision.

| DATE | REVISION | CHANGE |
|---|---|---|
| May 30, 2018 | FN9240.3 | Added link to product information page in Related Literature section on page 1.<br>Updated Functional Pin Descriptions to match DFN package and moved descriptions to page 3.<br>Added Notes 1, 2, and 3 to Ordering Information table on page 3.<br>In Absolute Maximum Ratings section on page 5, changed the following:<br>-BOOT Voltage ($V_{BOOT}$ - GND): 25V to 33V<br>-PHASE Voltage: 15V to 30V<br>Updated Package Outline Drawing M8.15 to the latest revision.<br>-Revision 1 to Revision 2: Updated to new POD format by removing table, moving dimensions onto drawing, and adding land pattern<br>-Revision 2 to Revision 3: Changed values in Typical Recommended Land Pattern from:<br>2.41 (0.095) to 2.20 (0.087)<br>0.76 (0.030) to 0.60 (0.023)<br>0.200 to 5.20 (0.205)<br>-Revision 3 to Revision 4: changed Note 1 “1982” to “1994”<br>Updated template and added Renesas disclaimer.<br>Removed About Intersil section. |
| November 10, 2015 | FN9240.2 | Updated the Ordering Information table on page 1.<br>Added Revision History and About Intersil sections.<br>Updated Package Outline Drawing L10.3X3C to the latest revision.<br>-Revision 2 to Revision 3 changes - Removed package outline and included center to center distance between lands on recommended land pattern. Removed Note 4 "Dimension b applies to the metallized terminal and is measured between 0.18mm and 0.30mm from the terminal tip." since it is not applicable to this package. Renumbered notes accordingly.<br>-Revision 3 to Revision 3 changes - Tiebar Note 4 updated From: Tiebar shown (if present) is a non-functional feature. To: Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends). |

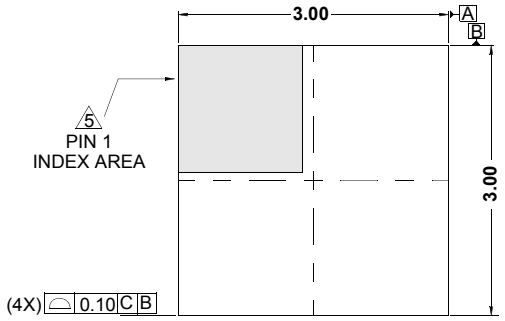
# Package Outline Drawings

For the most recent package outline drawing, see L10.3x3C.

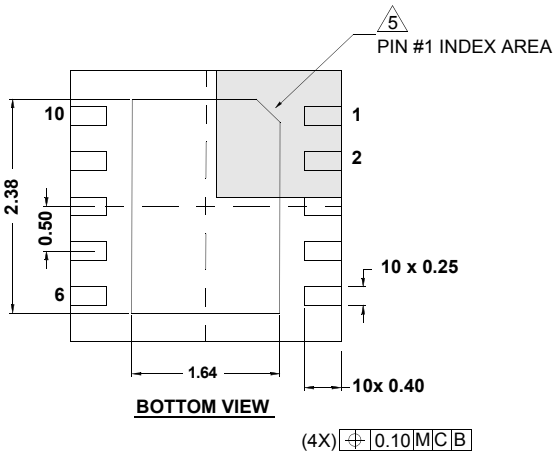
## L10.3x3C

**10 LEAD DUAL FLAT PACKAGE (DFN)**

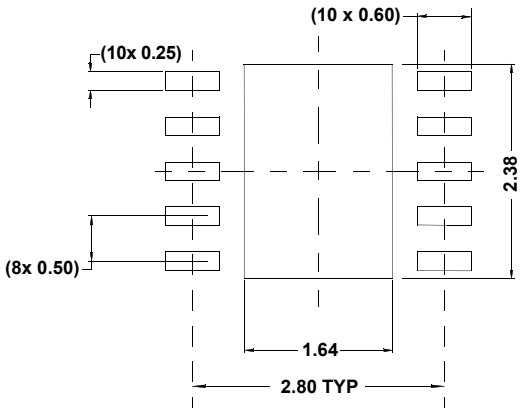
**Rev 4, 3/15**



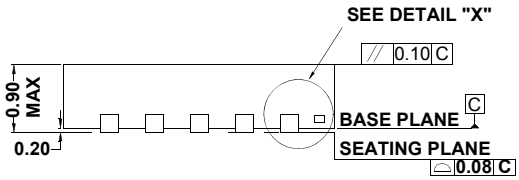

TOP VIEW



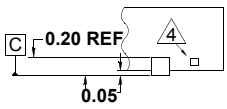

BOTTOM VIEW




TYPICAL RECOMMENDED LAND PATTERN




SIDE VIEW




DETAIL "X"

**NOTES:**

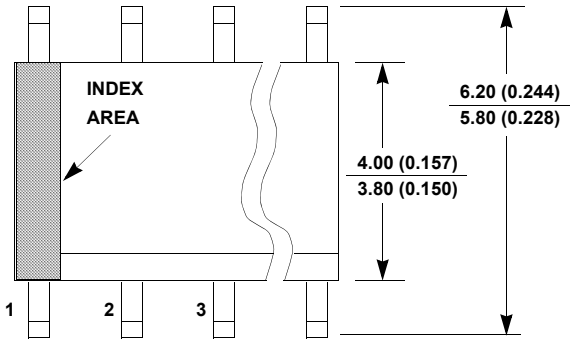
1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Tiebar shown (if present) is a non-functional feature and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
6. Compliant to JEDEC MO-229-WEED-3 except for E-PAD dimensions.

## M8.15

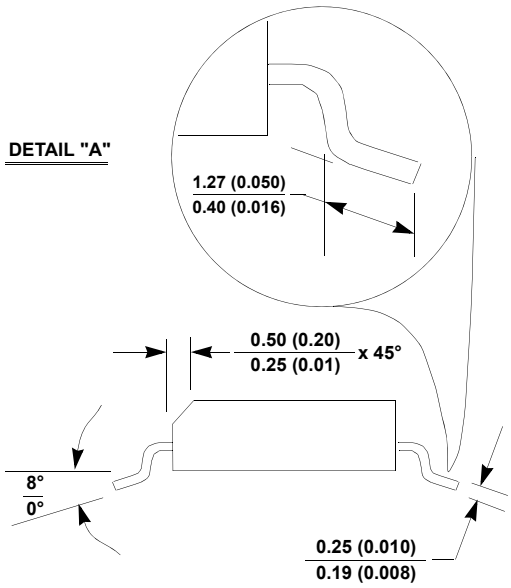
For the most recent package outline drawing, see M8.15.

**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

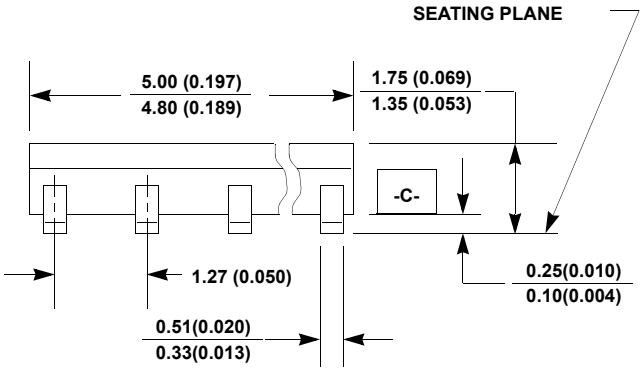
**Rev 4, 1/12**



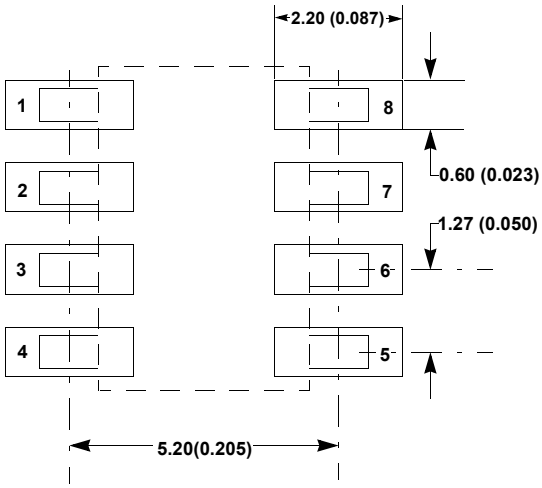

TOP VIEW




SIDE VIEW "B"




SIDE VIEW "A"




TYPICAL RECOMMENDED LAND PATTERN

**NOTES:**

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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