ISL70005SEH, ISL73005SEH

Radiation Hardened Dual Output 3A Synchronous Buck and ±1A LDO Regulator for DDR VDDQ and VTT

The ISL70005SEH and ISL73005SEH are radiation hardened dual output Point-of-Load (POL) regulators combining the high efficiency of a synchronous buck regulator with the low noise of a Low Dropout (LDO) regulator. They are suited for systems with 3.3V or 5V power buses and can support continuous output load currents of 3A for the buck regulator and ±1A for the LDO.

The buck regulator uses a voltage mode control architecture and switches at a resistor adjustable frequency of 100kHz to 1MHz. Externally adjustable loop compensation allows for an optimum balance between stability and output dynamic performance. The internal synchronous power switches are optimized for high efficiency and excellent thermal performance.

The LDO is completely configurable independent of the switching regulator. It uses NMOS pass devices and separate chip bias voltage (L_VCC) to drive its gate, enabling the LDO to operate with a very low voltage at the L_VIN input. The LDO can sink and source up to 1A continuously, making it an ideal choice to power DDR memory.

The ISL70005SEH and ISL73005SEH are available in a space saving 28 Ld ceramic dual flat-pack package or in die form. They are specified to operate across a temperature range of T_A = -55°C to +125°C.

Features

- Electrically screened to DLA SMD 5962-19209
- Dual Output Regulator: 3A Synchronous Buck and ±1A LDO
- DDR, DDR2, DDR3, and DDR4 VDDQ/VTT Regulator
- Independent EN, SS, and PG indicators
- ±1% reference voltage
- External clock synchronization: 100kHz to 1MHz
- Full military temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C
- TID Rad Hard Assurance (RHA) testing - ISL70005SEH
  - HDR (50-300rad(Si)/s): 100krad(Si)
  - LDR (0.01rad(Si)/s): 75krad(Si)
- TID Rad Hard Assurance (RHA) testing - ISL73005SEH
  - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE Characterization (see test report)
  - No DSEE with V_{DD} = 6.0V at 86.4MeV•cm^2/mg
  - No SEFI at LET 43MeV•cm^2/mg

Applications

- Point-of-load for low power FPGA core, auxiliary and I/O supply voltages
- DDR memory power for VDDQ and VTT rails
- Distributed power system of satellite payloads

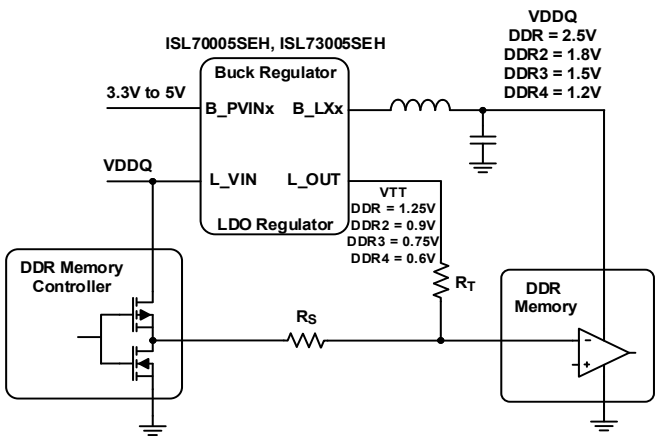


Figure 1. Power Solution for DDR - DDR4 Memory

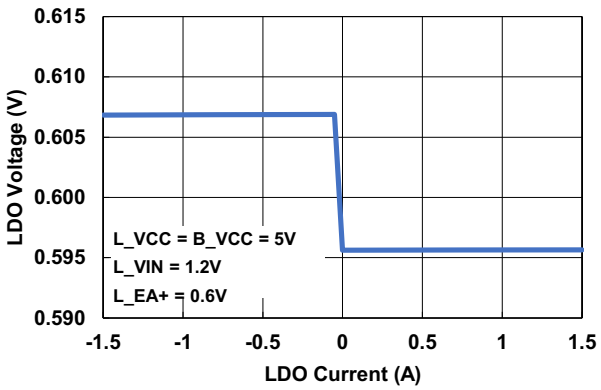


Figure 2. LDO Load Regulation; DDR4 Configuration

Contents

1. Overview

1.1 Typical Application Schematics

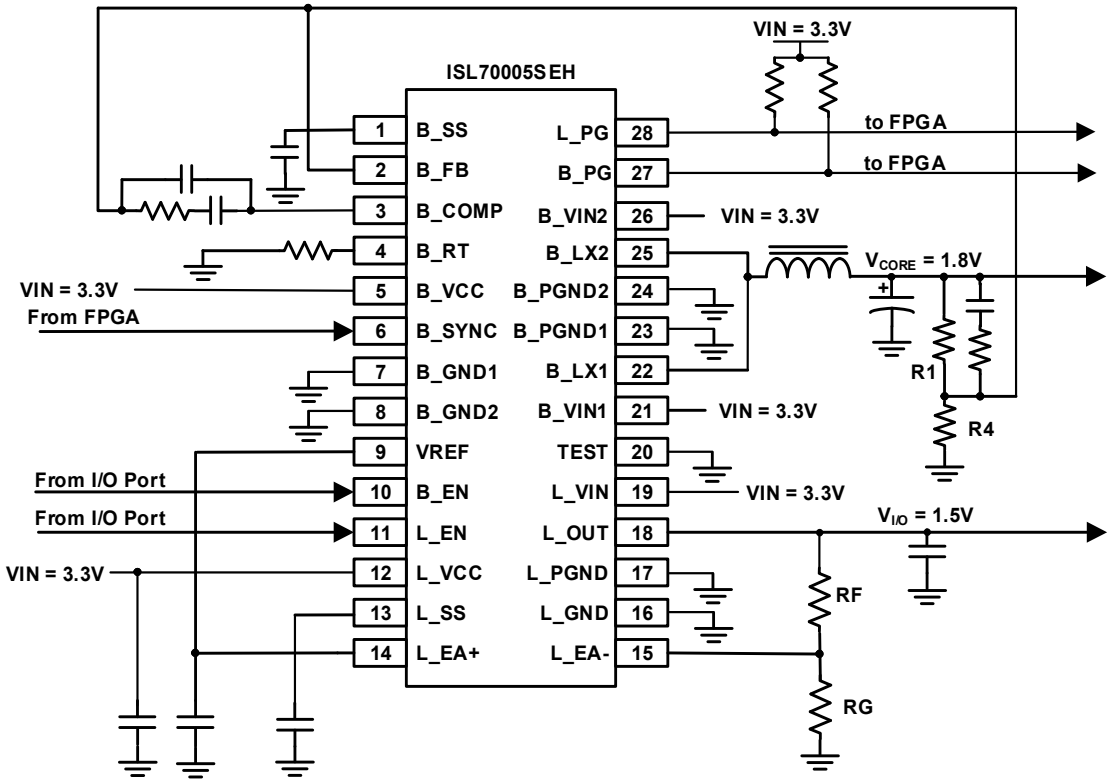


Figure 3. ISL70005SEH Application for Low Power FPGA Core and I/O Supply

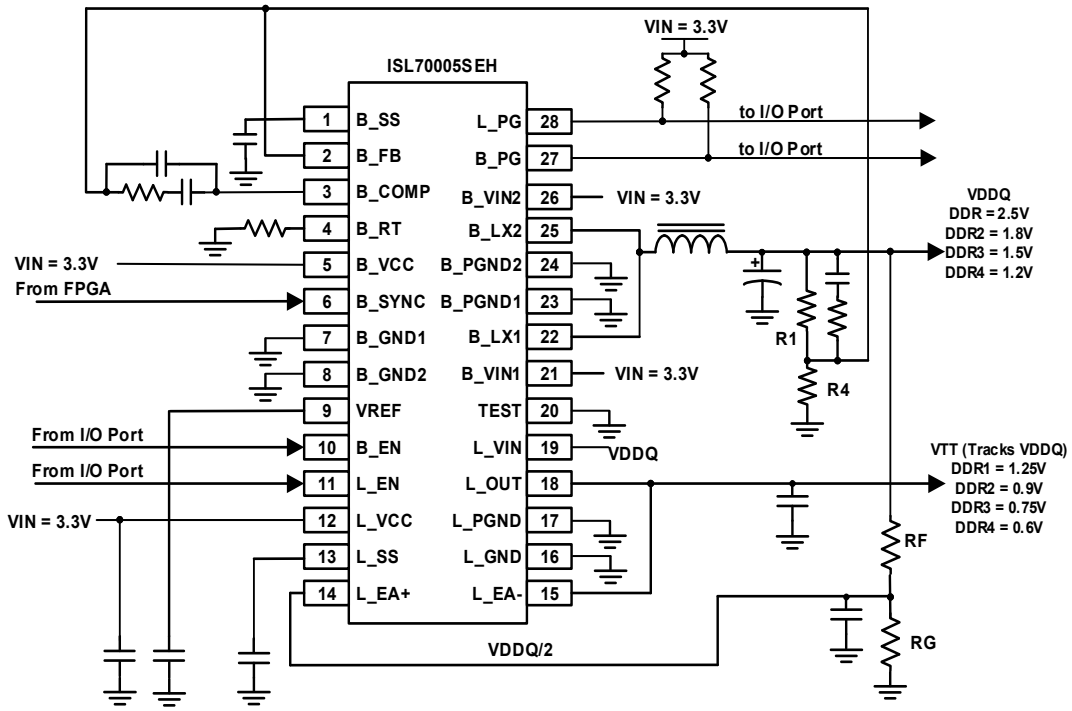


Figure 4. ISL70005SEH Application for DDR Memory Power Solution

1.2 Functional Block Diagram

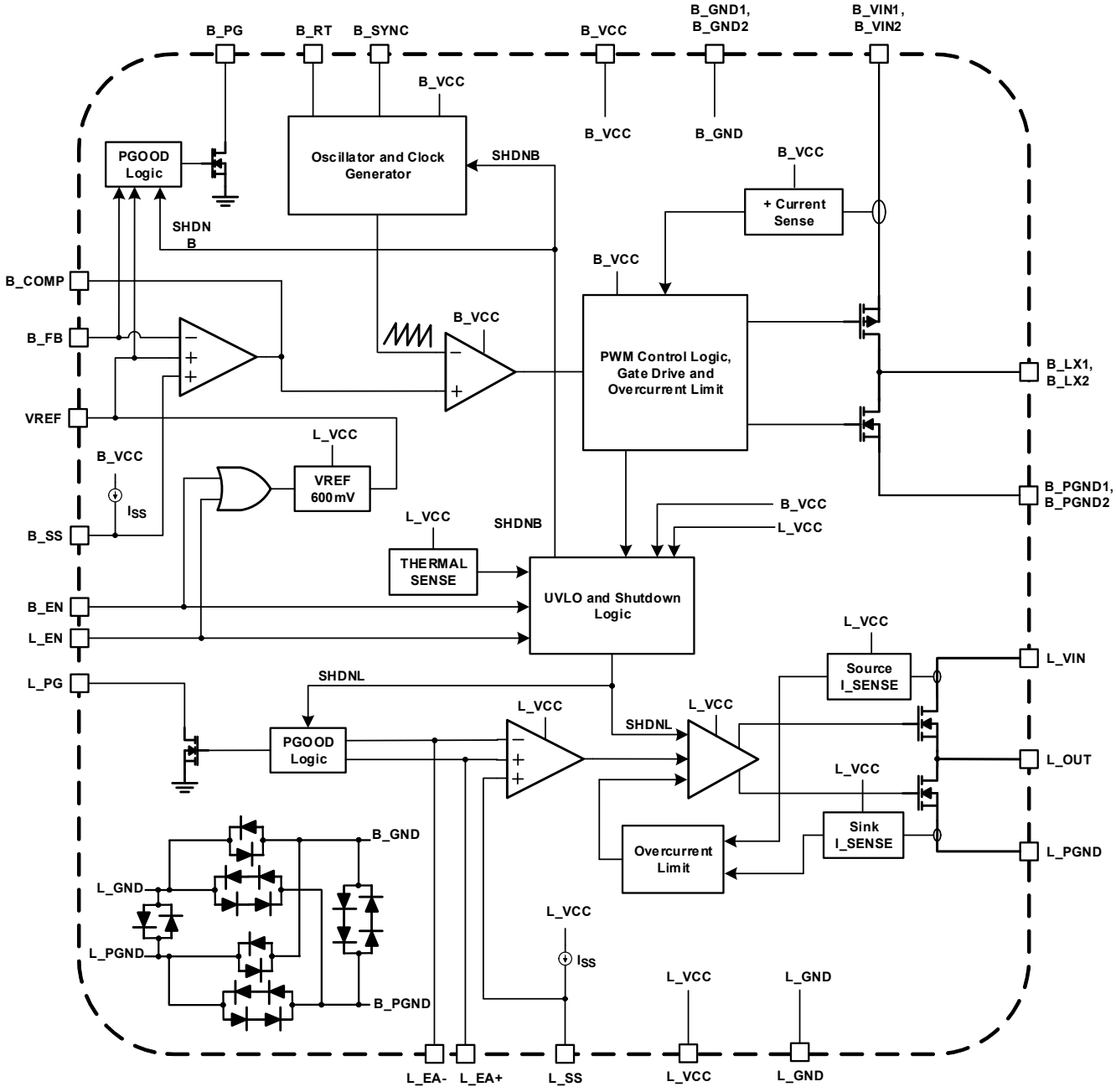


Figure 5. Block Diagram

1.3 Ordering Information

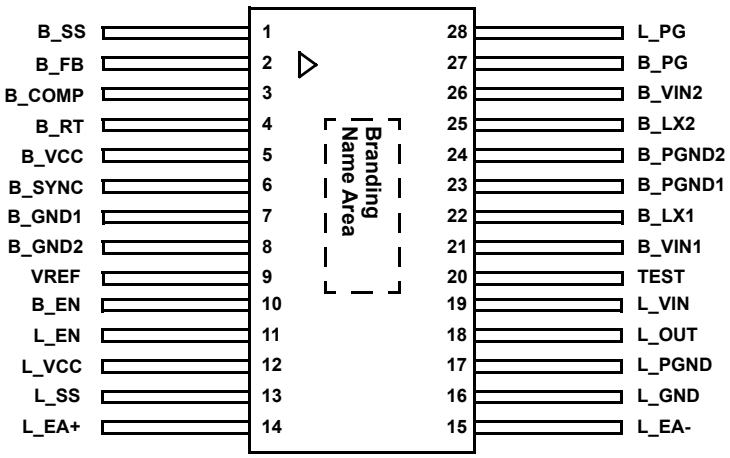
Ordering SMD Number (Note 1)	Part Number (Note 2)	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Temperature Range
5962R1920901VXC	ISL70005SEHVF	HDR to 100krad(Si) LDR to 75krad(Si)	28 Ld CDFP	K28.A	-55 to +125°C
5962R1920901V9A	ISL70005SEHVX (Note 5)		Die	-	
5962L1920902VXC	ISL73005SEHVF	LDR to 75krad(Si)	28 Ld CDFP	K28.A	
5962L1920902V9A	ISL73005SEHVX (Note 5)		Die	-	
N/A	ISL70005SEHF/PROTO (Note 3)	N/A	28 Ld CDFP	K28.A	
N/A	ISL70005SEHX/SAMPLE (Notes 3, 5)	N/A	Die	-	
N/A	ISL70005SEHDEMO1Z (Note 4)	Evaluation Board			
N/A	ISL70005SEHEV2Z (Note 4)	Evaluation Board			

Notes:

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Evaluation boards use the /PROTO parts and /PROTO parts are not rated or certified for total ionizing dose (TID) or Single Event Effect (SEE) immunity.
5. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in "Electrical Specifications" on page 10.

1.4 Pin Configuration

28 Ld CDFP
Top View

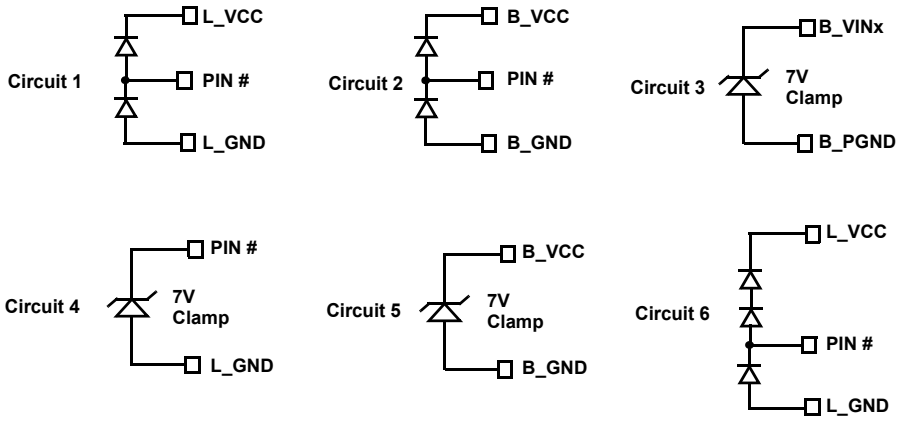


Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.5 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	B_SS	2	Soft-start input to the buck regulator. When B_EN is driven above 2V, a 24µA pull-up current charges a ceramic capacitor connected from B_SS to B_GNDx to set the soft-start ramp time.
2	B_FB	2	Inverting input to the buck error amplifier. Connect a type III compensation network between this pin and the B_COMP pin.
3	B_COMP	2	Output for the error amplifier of the buck regulator. Connect an external compensation network between this pin and the B_FB pin.
4	B_RT	2	Oscillator frequency select input. Connect a resistor from this pin to B_GNDx to program the switching frequency from 100kHz to 1MHz.
5	B_VCC	5	Supply input to the internal buck control circuitry. Bypass B_VCC to B_GNDx using a ceramic capacitor as close as possible to the IC. **Note:** B_VCC must be connected to the same DC voltage as B_VINx and L_VCC.
6	B_SYNC	2	Clock frequency synchronization input to the buck regulator. During soft-start, the ISL7x005SEH uses its internal oscillator until B_SS >600mV, and then synchronizes to B_SYNC if a clock is present. The rising edge of B_SYNC starts a new PWM cycle (begins minimum off-time). Connect to GND if synchronization is not used.
7	B_GND1	N/A	Buck analog ground pin and package lid connection.
8	B_GND2	N/A	
9	VREF	1	Output of the 600mV reference voltage. Bypass this pin to L_GND with a minimum 100nF ceramic capacitor located as close as possible to the IC. This pin may be used as the LDO reference voltage by connecting VREF to L_EA+. Additional loading is not recommended.
10	B_EN	6	Enable input to the buck regulator. Driving this pin above 2V enables the buck.
11	L_EN	6	Enable input to the LDO. Driving this pin above 2V enables the LDO.
12	L_VCC	4	Bias supply pin to the LDO analog circuitry and common functions circuitry. Bypass L_VCC to L_GND using a ceramic capacitor as close as possible to the IC. **Note:** L_VCC must be connected to the same DC voltage as B_VCC and B_VINx.
13	L_SS	1	Soft-start input to the LDO. When L_EN is driven above 2V, a 24µA pull-up current charges the ceramic capacitor connected from L_SS to L_GND to set the soft-start output ramp time.
14	L_EA+	1	Non-inverting input to the LDO error amplifier. Connect this pin to the VREF pin for independent LDO application or a resistor divider from the buck output for tracking DDR memory power applications.

Pin Number	Pin Name	ESD Circuit	Description
15	L_EA-	1	Inverting input to the LDO error amplifier. Connect a resistor divider network from L_OUT to this pin to set the output voltage. Connect L_EA- to L_OUT for setting L_OUT equal to L_EA+.
16	L_GND	NA	LDO analog ground pin.
17	L_PGND	NA	LDO power-stage ground pin.
18	L_OUT	1	LDO output pin.
19	L_VIN	4	Input supply for the LDO power-stage MOSFET. L_VIN voltage must not exceed L_VCC.
20	TEST	6	Factory use only. Must be connected to L_GND in application.
21	B_VIN1	3	Input supply for the buck power-stage MOSFETs. Bypass B_VINx pins directly to B_PGNDx with ceramic capacitors located as close as possible to the IC. **Note:** B_VIN1 must be connected to the same DC voltage as B_VCC and L_VCC.
22	B_LX1	NA	Buck regulator switch node connection. Output of the internal buck power MOSFETs. Connect to the power inductor.
23	B_PGND1	NA	Buck power-stage ground pin.
24	B_PGND2	NA	
25	B_LX2	NA	Buck regulator switch node connection. Output of the internal buck power MOSFETs. Connect to the power inductor.
26	B_VIN2	3	Input supply for the buck power-stage MOSFETs. Bypass B_VINx pins directly to B_PGNDx with ceramic capacitors located as close as possible to the IC. **Note:** B_VIN2 must be connected to the same DC voltage as B_VCC and L_VCC.
27	B_PG	2	Power-good output for the buck regulator. This output is open-drain logic. Connect a 10kΩ to 100kΩ pull-up resistor to B_VCC. Can be wired-OR with L_PG to have a single power-good signal. Bypass B_PG to B_GND with a 1nF ceramic capacitor to mitigate SEE.
28	L_PG	2	Power-good output for the LDO. This output is open-drain logic, connect a 10kΩ to 100kΩ pull-up resistor to L_VCC. Can be wired-OR with B_PG to have a single power-good signal. Bypass L_PG to L_GND with a 1nF ceramic capacitor to mitigate SEE.
LID	N/A	N/A	The top lid of the package is electrically connected to pins 7 (B_GND1) and 8 (B_GND2).



2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
B_VCC	B_GND - 0.3	B_GND + 6.5	V
B_VCC (Notes 6, 7)	B_GND - 0.3	B_GND + 6.0	V
B_VINx	B_PGND - 0.3	B_PGND + 6.5	V
B_VINx (Notes 6, 7)	B_PGND - 0.3	B_PGND + 6.0	V
L_VCC	L_GND - 0.3	L_GND + 6.5	V
L_VCC (Notes 6, 7)	L_GND - 0.3	L_GND + 6.0	V
L_VIN	L_GND - 0.3	L_GND + 6.5	V
L_VIN (Notes 6, 7)	L_GND - 0.3	L_GND + 6.0	V
B_LXx	B_PGND - 0.3; limit 6.5 from B_VIN	B_VINx + 0.3; limit 6.5 to B_PGND	V
B_LXx (Notes 6, 7)	B_PGND - 0.3; limit 6.0 from B_VIN	B_VINx + 0.3; limit 6.0 to B_PGND	V
B_LXx (<50ns pulse width up to 1MHz switching frequency)	B_PGND - 2.0; limit 6.5 from B_VIN	B_VINx + 1.5; limit 6.5 to B_PGND	V
L_OUT	L_PGND - 0.3	L_VIN + 0.3; limit 6.5	V
L_OUT (Notes 6, 7)	L_PGND - 0.3	L_VIN + 0.3; limit 6.0	V
L_PG, B_PG, B_RT, B_SYNC, B_COMP, B_FB	B_GND - 0.3	B_VCC + 0.3	V
B_EN, L_EN, L_EA-, L_EA+, VREF, TEST	L_GND - 0.3	L_VCC + 0.3	V
B_SS	B_GND - 0.3	B_VCC + 0.3, limit B_GND + 3.5	V
L_SS	L_GND - 0.3	L_VCC + 0.3, limit L_GND + 3.5	V
B_GND to L_PGND, B_GND to L_GND, L_GND to L_PGND	-0.3	0.3	V
B_GND to B_PGND, L_GND to B_PGND, L_PGND to B_PGND	-0.6	0.6	V
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015.7)	2		kV
Charged Device Model (Tested per JS-002-2014)	750		V

Notes:

6. For operation in a heavy ion environment at LET = 86.4MeV•cm^2/mg at 125°C (T_C) and with buck converter sourcing 0A and 3.5A load current.
7. For operation in a heavy ion environment at LET = 86.4MeV•cm^2/mg at 125°C (T_C) with LDO sourcing and sinking 1.2A load current.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
CDFP Package K28.A (Notes 8, 9)	19.5	1.2

Notes:

8. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with direct attach features. See TB379.
9. For θ_{JC}, the case temperature location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
B_VIN1, B_VIN2, B_VCC, L_VCC (These four pins must be at the same DC voltage)	3.3 ±10%	5.0 ±10%	V
L_VIN	1.0	L_VCC	V
L_EA+, L_EA-	0.6	1.27	V

2.4 Electrical Specifications

2.4.1 Buck Regulator Electrical Specifications

Unless otherwise noted, B_VINx = B_VCC = 3V to 5.5V; B_GND = B_PGNDx = 0V; B_EN = 2.0V; B_SYNC = B_LXx = Open Circuit; B_PG is pulled up to B_VCC with a 3kΩ resistor; VREF is bypassed to L_GND with a 22nF capacitor; B_SS is bypassed to B_GNDx with a 220nF capacitor; I_{OUT} = 0A; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C, without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply					
Operating Supply Current - Switching	B_EN = 2V, 100kHz switching, B_LXx floating		10	**15**	mA
Shutdown Supply Current - Idle	B_EN = GND		0.6	**3.0**	mA
Enable Pin Characteristics					
B_EN Rising Threshold		**1.6**		**2.0**	V
B_EN Falling Threshold		**1.4**		**1.9**	V
B_EN Input Hysteresis		**100**	200		mV
B_EN Pull-Down Resistance	B_EN = 5.5V	**80**		**160**	kΩ
B_EN Pull-Down Resistance	B_EN = 1.4V	**60**		**130**	kΩ
PWM Control Logic					
Switching Frequency	B_RT resistor = 544kΩ	**85**	100	**115**	kHz
	B_RT resistor = 44kΩ	**875**	1000	**1175**	kHz
B_LXx Minimum On-Time	B_VIN = B_VCC = 5.5V, B_COMP = 180mV, 1kΩ from B_LXx to 2.75V	**100**	175	**240**	ns
B_LXx Minimum On-Time	B_VIN = B_VCC = 3V, B_COMP = 180mV, 1kΩ from B_LXx to 1.5V	**115**	215	**325**	ns
B_LXx Minimum Off-Time	B_COMP = 180mV, 1kΩ from B_LXx to [B_VIN / 2]	**50**	105	**165**	ns

Unless otherwise noted, B_VINx = B_VCC = 3V to 5.5V; B_GND = B_PGNDx = 0V; B_EN = 2.0V; B_SYNC = B_LXx = Open Circuit; B_PG is pulled up to B_VCC with a 3kΩ resistor; VREF is bypassed to L_GND with a 22nF capacitor; B_SS is bypassed to B_GNDx with a 220nF capacitor; I_{OUT} = 0A; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C, without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

Parameter	Test Conditions	Min	Typ	Max	Unit
Modulator Gain (Note 10)			2.35		V/V
External Synchronization Range	B_RT clock set to 90% of B_SYNC clock, 50% duty cycle clock input	**100**		**1000**	kHz
B_SYNC Input Voltage	B_SYNC VIH voltage	**2**			V
	B_SYNC VIL voltage			**0.8**	V
B_SYNC Input Leakage Current		**-1**		**1**	µA
Soft-Start					
Soft-Start Source Current	SS = GND	**17**	23	**30**	µA
Soft-Start Discharge ON-Resistance			3.0	**6.0**	Ω
Soft-Start Discharge Time			256		Clock Cycles
Reference Voltage					
Reference Voltage Tolerance	VREF + error amplifier V_{IO}	**0.594**	0.6	**0.606**	V
Error Amplifier					
DC Gain (Note 10)			80		dB
Gain-Bandwidth Product (Note 10)			7		MHz
Maximum Output Voltage	B_VCC = 5.5V	**3.5**	4.2		V
Slew Rate (Note 10)			8.5		V/µs
B_FB Input Leakage Current	B_FB = 0.6V, B_VINx = 5.5V			**250**	nA
Power MOSFET					
Packaged Upper Device $r_{DS(ON)}$	B_VINx = B_VCC = 3.0V; single B_LXx output	**80**	160	**245**	mΩ
	B_VINx = B_VCC = 5.5V; single B_LXx output	**65**	130	**210**	mΩ
Packaged Lower Device $r_{DS(ON)}$	B_VINx = B_VCC = 3.0V; single B_LXx output	**40**	90	**160**	mΩ
	B_VINx = B_VCC = 5.5V; single B_LXx output	**35**	85	**150**	mΩ
Packaged ON Resistance Matching, B_LX1 $r_{DS(ON)\_1}$ to B_LX2 $r_{DS(ON)\_2}$, Upper and Lower Device	T_A = +125°C Match = $\lvert r_{DS(ON)\_1} - r_{DS(ON)\_2} \rvert$ / AVG where AVG = $(r_{DS(ON)\_1} + r_{DS(ON)\_2}) / 2$		5	15	%
Die Upper Device $r_{DS(ON)}$	B_VINx = B_VCC = 3.0V; T_A = 25°C single B_LXx output	40	75	110	mΩ
	B_VINx = B_VCC = 5.5V; T_A = 25°C single B_LXx output	20	50	85	mΩ
Die Lower Device $r_{DS(ON)}$	B_VINx = B_VCC = 3.0V; T_A = 25°C Single B_LXx output	15	35	60	mΩ
	B_VINx = B_VCC = 5.5V; T_A = 25°C single B_LXx Output	10	30	65	mΩ
Die ON Resistance Matching, B_LX1 $r_{DS(ON)\_1}$ to B_LX2 $r_{DS(ON)\_2}$ Upper and Lower Device	B_VINx = 3.0V; T_A = +25°C Match = $\lvert r_{DS(ON)\_1} - r_{DS(ON)\_2} \rvert$ / AVG where AVG = $(r_{DS(ON)\_1} + r_{DS(ON)\_2}) / 2$		5	15	%
B_LXx Output Leakage	B_EN = B_LXx = xGND, single B_LXx output			**3**	µA
	B_EN = GND, B_LXx = 5.5V, single B_LXx output			**15**	µA
Dead Time (Note 10)		**0**	30	**50**	ns
Power-Good Signal					
B_PG Overvoltage Error Threshold	B_FB as a % of VREF	**107**	111	**115**	%
B_PG Overvoltage Error Hysteresis	B_FB as a % of VREF	**1.5**	3.5	**5**	%
B_PG Undervoltage Error Threshold	B_FB as a % of VREF	**85**	89	**93**	%

Unless otherwise noted, B_VINx = B_VCC = 3V to 5.5V; B_GND = B_PGNDx = 0V; B_EN = 2.0V; B_SYNC = B_LXx = Open Circuit; B_PG is pulled up to B_VCC with a 3kΩ resistor; VREF is bypassed to L_GND with a 22nF capacitor; B_SS is bypassed to B_GNDx with a 220nF capacitor; I_{OUT} = 0A; $T_A = T_J$ = +25°C. **Boldface limits apply across the operating temperature range, -55°C to +125°C, without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Continued)**

Parameter	Test Conditions	Min	Typ	Max	Unit
B_PG Undervoltage Error Hysteresis	B_FB as a % of VREF	**1.5**	3.5	**5**	%
B_PG Drive	B_VIN = 3V, B_PG = 0.4V, B_EN = GND	**7.2**			mA
B_PG Leakage	B_VINx = B_PG = 5.5V			**1**	µA
Protection Features					
Undervoltage Protection					
Undervoltage Trip Threshold	B_FB as a % of VREF; in test mode	**71**	75	**79**	%
Undervoltage Recovery Threshold	B_FB as a % of VREF, in test mode	**86**	90	**94**	%
Overcurrent Protection					
Overcurrent Limit		**4.0**		**6.4**	A

Note:
10. Specifications established by characterization or analysis and are not production tested.

2.4.2 LDO Electrical Specifications

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: C_{OUT} = 150µF tantalum, $T_A = T_J$ = +25°C, I_L = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 31 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** Pulse load techniques used by ATE to ensure $T_J = T_A$.

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Characteristics					
L_VIN Voltage Range	MIN ensured by L_VIN dropout testing	**0.775**		**L_VCC**	V
L_OUT Voltage Range	MIN ensured by L_VIN dropout testing; MAX ensured by L_VCC dropout testing; L_EA+ = 0.600V	**0.6**		**L_VCC - 1.5**	V
VREF Voltage		**0.591**		**0.609**	V
Power-On Reset					
L_VCC Internal UVLO Rising Threshold		**2.6**	2.8	**2.95**	V
L_VCC Internal UVLO Falling Threshold		**2.45**		**2.80**	V
L_VCC Internal UVLO Hysteresis		**75**	175	**420**	mV

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: C_{OUT} = 150µF tantalum, $T_A = T_J$ = +25°C, I_L = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 31 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** Pulse load techniques used by ATE to ensure $T_J = T_A$. **(Continued)**

Parameter	Test Conditions	Min	Typ	Max	Unit
DC Output Voltage Accuracy, L_OUTx	L_VIN = [4.15V, 5.5V], L_VCC = 5.5V, R1/R2 = 4.5, R1: L_OUT to L_EA-; R2: L_EA- to L_GND L_EA+ = 0.600V, I_{LOAD} = [10mA, 1A] L_OUTx where x = [1, 3, 5, 7]	**3.225**	3.272	**3.336**	V
	L_VIN = [4.15V, 5.5V], L_VCC = 5.5V, R1/R2 = 4.5, R1: L_OUT to L_EA-; R2: L_EA- to L_GND L_EA+ = 0.600V, I_{LOAD} = [-10mA, -1A] L_OUTx where x = [2, 4, 6, 8]	**3.285**	3.327	**3.397**	V
	L_VIN = [2V, 3V, 5.5V], L_VCC = [3.35V, 5.5V], R1/R2 = 1.5, R1: L_OUT to L_EA-; R2: L_EA- to L_GND L_EA+ = 0.600V, I_{LOAD} = [10mA, 1A] L_OUTx where x = [9, 11, 13, 15, 17, 19, 21, 23]	**1.463**	1.487	**1.519**	V
	L_VIN = [2V, 3V, 5.5V], L_VCC = [3.35V, 5.5V], R1/R2 = 1.5, R1: L_OUT to L_EA-; R2: L_EA- to L_GND L_EA+ = 0.600V, I_{LOAD} = [-10mA, -1A] L_OUTx where x = [10, 12, 14, 16, 18, 20, 22, 24]	**1.490**	1.512	**1.546**	V
	L_VIN = [1.75V, 3V, 5.5V], L_VCC = [3.1V, 5.5V], L_EA- = L_OUT, L_EA+ = 1.250V, I_{LOAD} = [10mA, 1A] L_OUTx where x = [25, 27, 29, 31, 33, 35, 37, 39]	**1.235**	1.245	**1.258**	V
	L_VIN = [1.75V, 3V, 5.5V] L_VCC = [3.1V, 5.5V], L_EA- = L_OUT, L_EA+ = 1.250V, I_{LOAD} = [-10mA, -1A] L_OUTx where x = [26, 28, 30, 32, 34, 36, 38, 40]	**1.246**	1.255	**1.269**	V
	L_VIN = [1.1V, 3V, 5.5V], L_VCC = [3V, 5.5V], L_EA- = L_OUT, L_EA+ = 0.600V, I_{LOAD} = [10mA, 1A] L_OUTx where x = [41, 43, 45, 47, 49, 51, 53, 55]	**0.585**	0.595	**0.608**	V
	L_VIN = [1.1V, 3V, 5.5V], L_VCC = [3V, 5.5V], L_EA- = L_OUT, L_EA+ = 0.600V, I_{LOAD} = [-10mA, -1A] L_OUTx where x = [42, 44, 46, 48, 50, 52, 54, 56]	**0.596**	0.605	**0.619**	V
Regulation Dead-Band	L_VOUT difference between the two current cases: I_{OUT} = [sourcing 10mA, sinking 10mA] for L_VCC = 5.5V, L_VIN = 5.5V, L_EA+ = 0.600V, L_OUT = L_EA-	**5**	10	**15**	mV
L_EA+, L_EA- Input Bias Current	L_EA+ = L_EA- = 0.6V, L_VIN = 5.5V			**1**	µA
L_VCC Pin Current	L_OUT = 1.5V; I_{LOAD} = 1A; L_VIN = 1.65V; 3.0V < L_VCC < 5.5V		7.2	**10**	mA
L_VCC Pin Current in Shutdown	L_EN = B_EN = 0V, L_VCC = 5.5V		450	**1000**	µA
L_VCC Dropout Voltage L_VCC_{DO} (Note 13)	I_{OUT} = 1A, L_OUT = 3.3V; L_VIN = 3.8V L_VCC = L_OUT + L_VCC_{DO};			**1.5**	V
L_VIN Dropout Voltage, L_VIN_{DO} (Note 12)	I_{OUT} = 1A, L_OUT = 0.6V; L_VIN = L_OUT + L_VIN_{DO}; 3.0V < L_VCC < 5.5V; T_A = -55°C		75	115	mV
	I_{OUT} = 1A, L_OUT = 0.6V; L_VIN = L_OUT + L_VIN_{DO}; 3.0V < L_VCC < 5.5V; T_A = 25°C		100	145	mV
	I_{OUT} = 1A, L_OUT = 0.6V; L_VIN = L_OUT + L_VIN_{DO}; 3.0V < L_VCC < 5.5V; T_A = 125°C		135	175	mV

Unless otherwise noted, all parameters are guaranteed over the following specified conditions: C_{OUT} = 150µF tantalum, $T_A = T_J$ = +25°C, I_L = 0A. Applications must follow thermal guidelines of the package to determine worst case junction temperature. See "Applications Information" on page 31 and TB379. **Boldface limits apply across the operating temperature range, -55°C to +125°C without irradiation. They also apply at +25°C after total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50 to 300rad(Si)/s (ISL70005SEH only) or after total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.** Pulse load techniques used by ATE to ensure $T_J = T_A$. **(Continued)**

Parameter	Test Conditions	Min	Typ	Max	Unit
Protection Features					
Positive Overcurrent Limit		**1.25**		**2**	A
Negative Overcurrent Limit		**-2**		**-1.25**	A
Thermal Shutdown Temperature (Note 11)	Junction temperature	153	175	195	°C
Thermal Shutdown Hysteresis (Rising Threshold) (Note 11)	Junction temperature		8		°C
AC Ripple Rejection and Noise Characteristics					
1kHz VIN Supply Ripple Rejection	V_{P-P} = 300mV; f = 1kHz; I_{LOAD} = 1A; L_VCC = 5V; L_VIN = 3.15V; L_OUT = 1.5V	**60**	80		dB
100kHz VIN Supply Ripple Rejection (Note 11)	V_{P-P} = 300mV; f = 100kHz; I_{LOAD} = 1A; L_VCC = 5V; L_VIN = 3.15V; L_OUT = 1.5V		50		dB
1kHz L_VCC Supply Ripple Rejection	V_{P-P} = 300mV; f = 1kHz; I_{LOAD} = 1A; L_VCC = 5V; L_VIN = 3V; L_OUT = 1.5V	**50**	70		dB
100kHz L_VCC Supply Ripple Rejection (Note 11)	V_{P-P} = 300mV; f = 100kHz; I_{LOAD} = 1A; L_VCC = 5V; L_VIN = 3V; L_OUT = 1.5V		36		dB
Output Noise Voltage (Note 11)	L_VCC = 5V; L_VIN = 1.4V; L_OUT = 1.25V; I_{LOAD} = 100mA; BW = 10Hz < f < 100kHz; L_EA- = L_OUT		11		μV_{RMS}
Enable Pin Characteristics					
L_EN Rising Threshold		**1.6**		**2.0**	V
L_EN Falling Threshold		**1.4**		**1.9**	V
L_EN Input Hysteresis		**100**	200		mV
L_EN Pull-Down Resistance	L_EN = 5.5V	**80**		**160**	kΩ
L_EN Pull-Down Resistance	L_EN = 1.4V	**60**		**130**	kΩ
PGOOD Characteristics					
L_PG Overvoltage Error Threshold	L_EA- as a % of L_EA+; L_EA+ = 0.6V	**107**	111	**115**	%
L_PG Overvoltage Error Hysteresis	L_EA- as a % of L_EA+; L_EA+ = 0.6V	**1.5**	3.5	**5**	%
L_PG Undervoltage Error Threshold	L_EA- as a % of L_EA+; L_EA+ = 0.6V	**85**	89	**93**	%
L_PG Undervoltage Error Hysteresis	L_EA- as a % of L_EA+; L_EA+ = 0.6V	**1.5**	3.5	**5**	%
L_PG Output Low Drive	L_VCC = 3V; L_PG = 0.4V; L_EN = L_GND	**7.2**			mA
L_PG Leakage Current	L_VIN = L_PG = 5.5V			**1**	µA

Notes:

11. Specifications established by characterization or design and are not production tested.
12. L_VIN dropout is defined by the difference in L_VIN and L_OUT when the regulator produces a 2% drop in L_OUT from its nominal value.
13. L_VCC dropout is defined by the difference in L_VCC and L_OUT when the regulator produces a 2% drop in L_OUT from its nominal value.

3. Typical Performance Curves

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C.

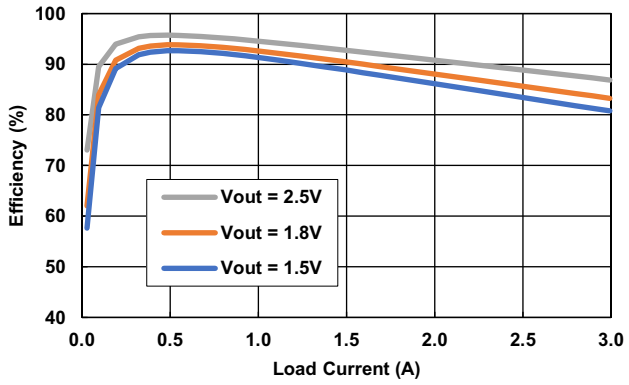


Figure 6. Efficiency vs I_{OUT}; B_VIN = 3V; 100kHz

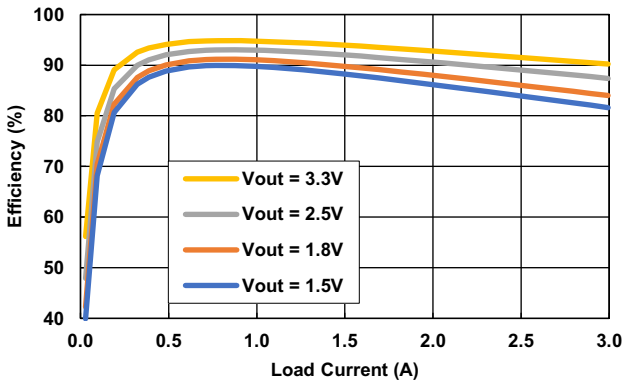


Figure 7. Efficiency vs I_{OUT}; B_VIN = 5V; 100kHz

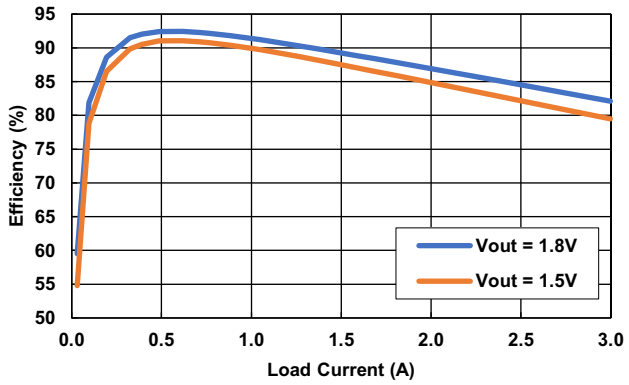


Figure 8. Efficiency vs I_{OUT}; B_VIN = 3V; 500kHz

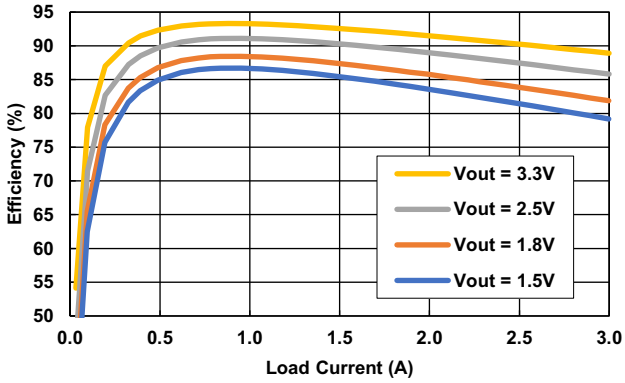


Figure 9. Efficiency vs I_{OUT}; B_VIN = 5V; 500kHz

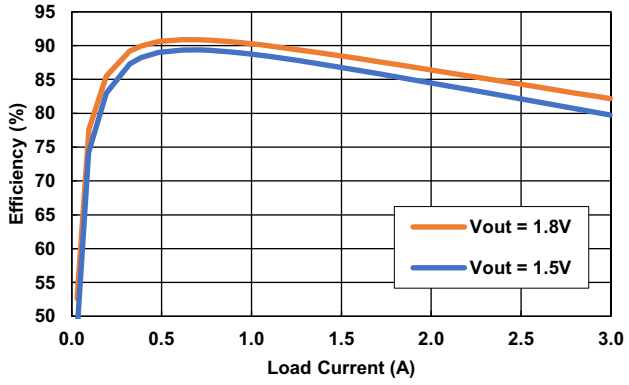


Figure 10. Efficiency vs I_{OUT}; B_VIN = 3V; 1MHz

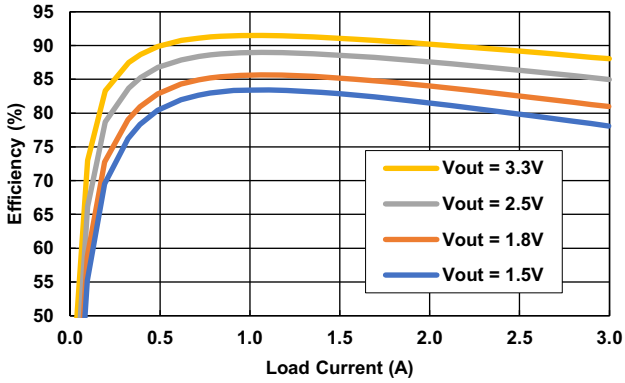


Figure 11. Efficiency vs I_{OUT}; B_VIN = 5V; 1MHz

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

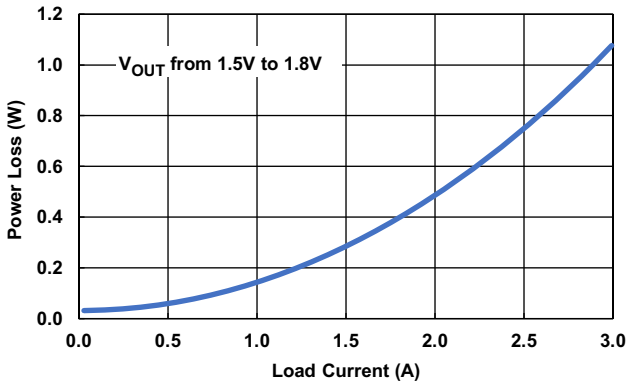


Figure 12. Power Loss vs I_{OUT}; B_VIN = 3V; 100kHz

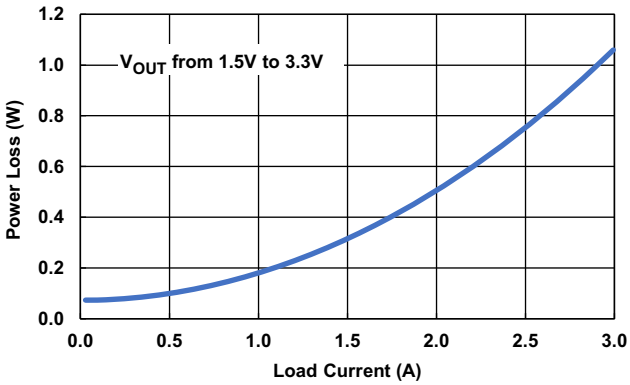


Figure 13. Power Loss vs I_{OUT}; B_VIN = 5V; 100kHz

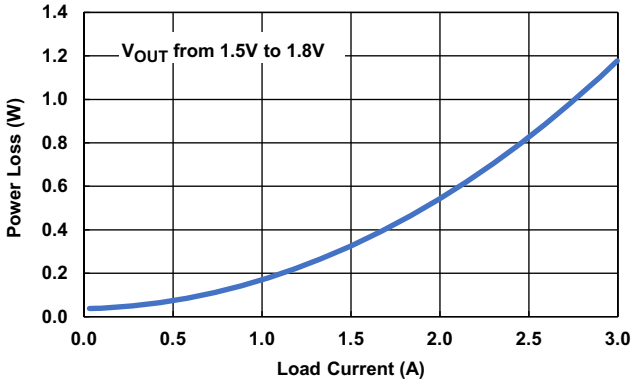


Figure 14. Power Loss vs I_{OUT}; B_VIN = 3V; 500kHz

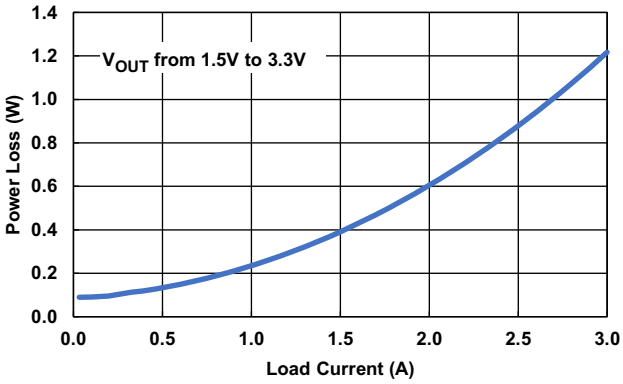


Figure 15. Power Loss vs I_{OUT}; B_VIN = 5V; 500kHz

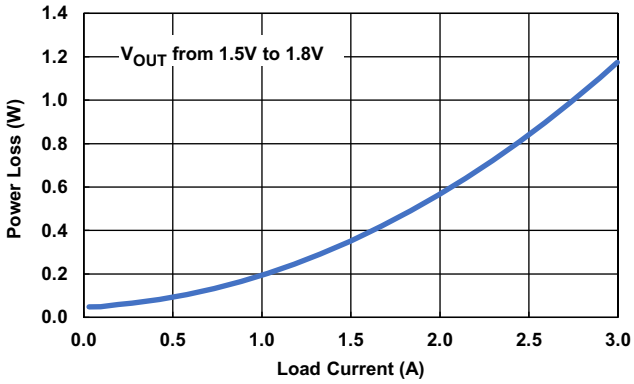


Figure 16. Power Loss vs I_{OUT}; B_VIN = 3V; 1MHz

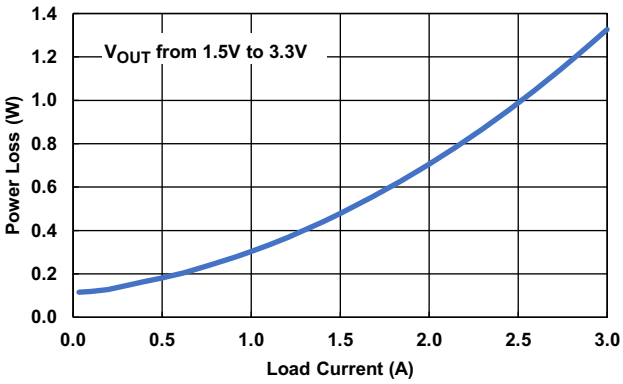


Figure 17. Power Loss vs I_{OUT}; B_VIN = 5V; 1MHz

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

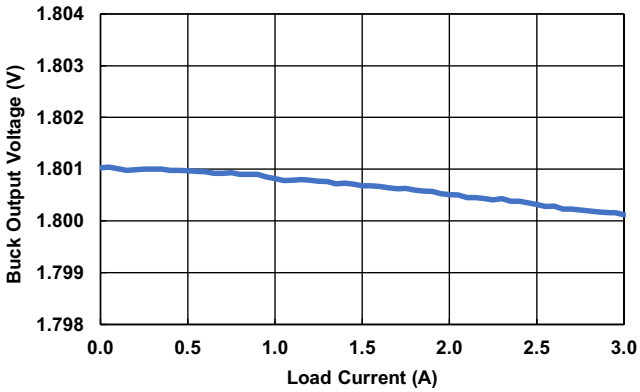


Figure 18. Buck Load Regulation; B_VIN = 3V

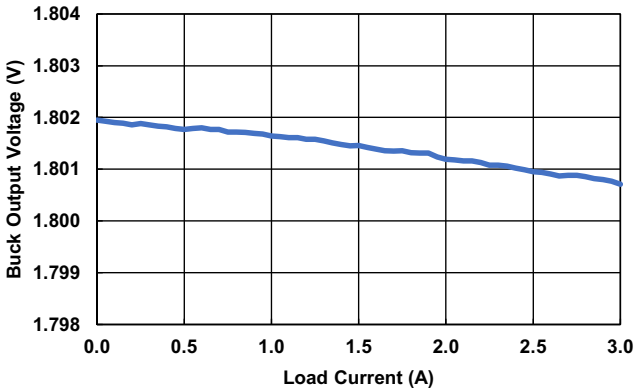


Figure 19. Buck Load Regulation; B_VIN = 5V

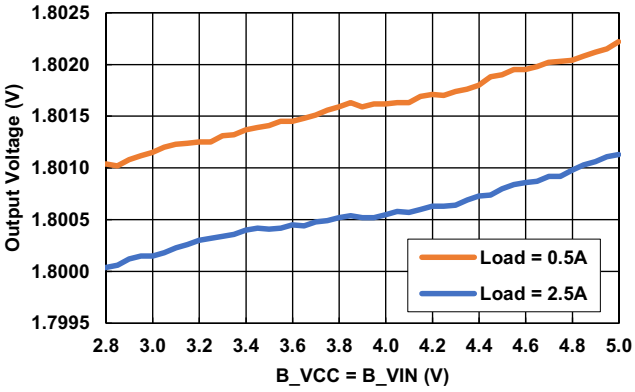


Figure 20. Buck Line Regulation; V_{OUT} = 1.8V

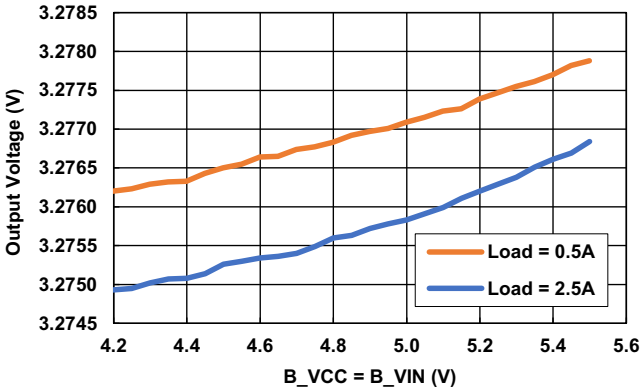


Figure 21. Buck Line Regulation; V_{OUT} = 3.3V

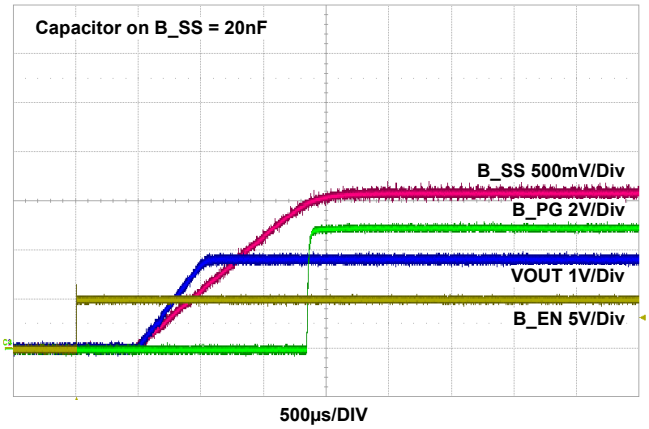


Figure 22. Buck Soft-Start; Load = 0.68Ω; LDO Disabled

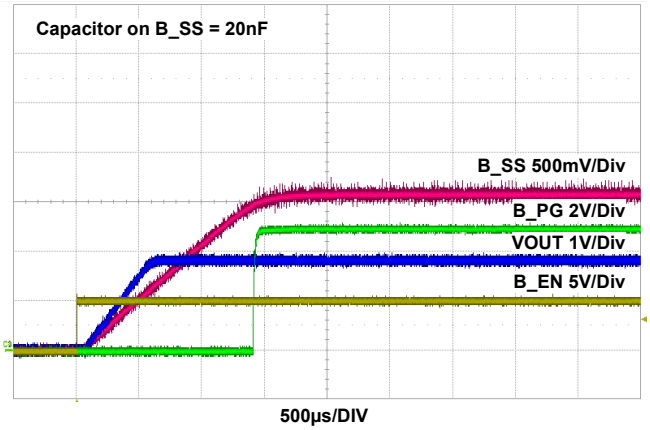


Figure 23. Buck Soft-Start; Load = 0.68Ω; LDO Enabled

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

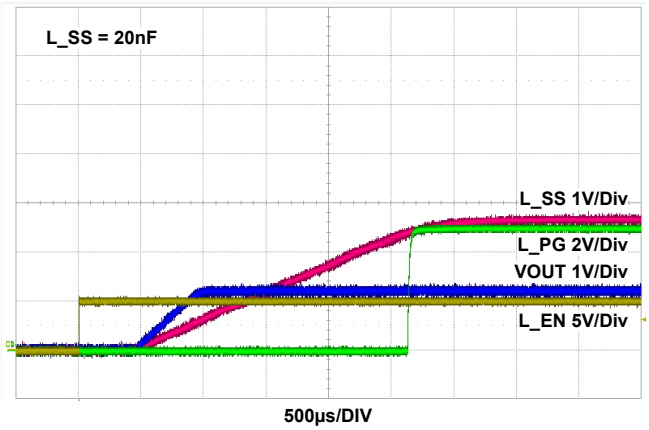


Figure 24. LDO Soft-Start; Load = 1.5Ω to GND; Buck Disabled

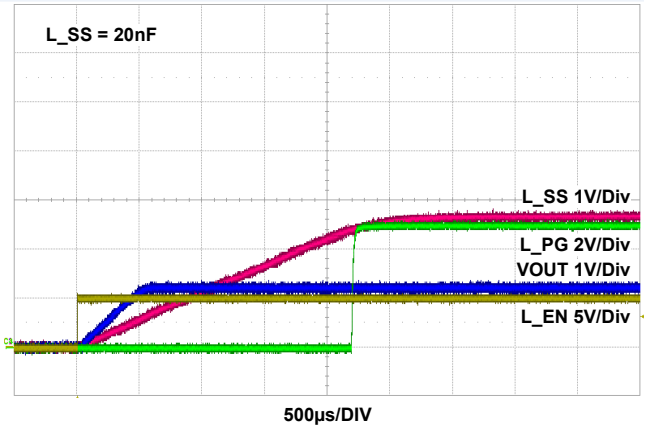


Figure 25. LDO Soft-Start; Load = 1.5Ω to GND; Buck Enabled

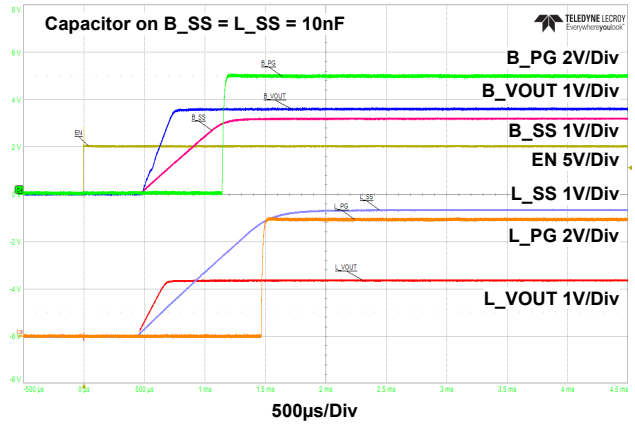


Figure 26. Buck and LDO Soft-Start; B_EN = L_EN; 0.68Ω Load on Buck; 1.5Ω Load on LDO; FPGA Configuration

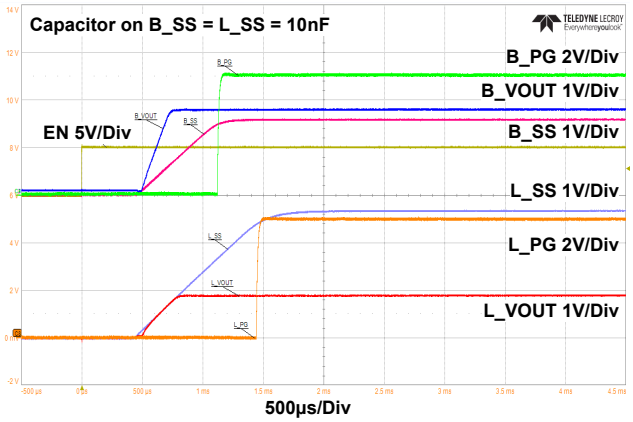


Figure 27. Buck and LDO Soft-Start; B_EN = L_EN; Load = 0A on Buck and LDO; DDR Configuration

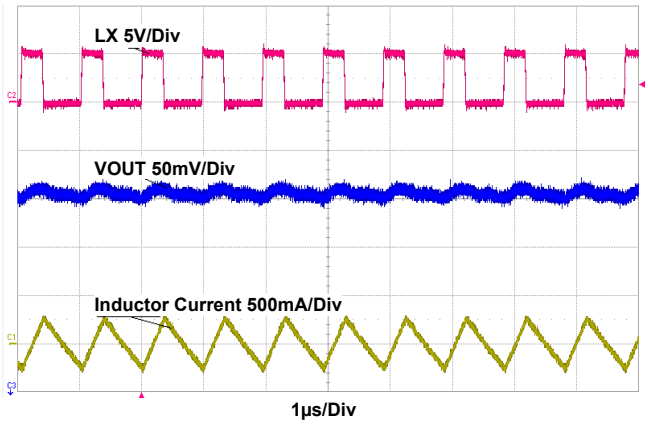


Figure 28. Buck Steady State Operation; Load = 0A

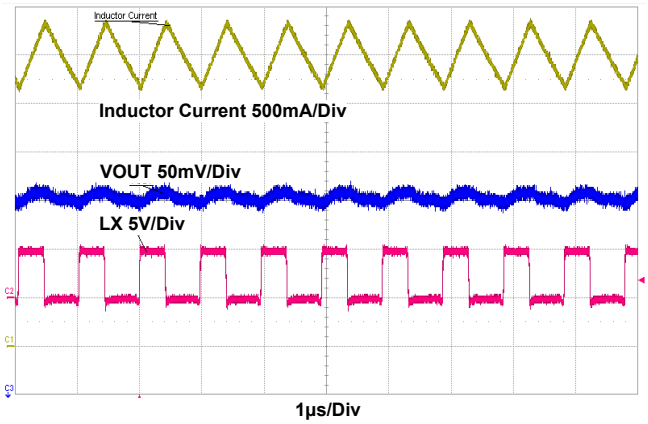


Figure 29. Buck Steady State Operation; Load = 3A

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

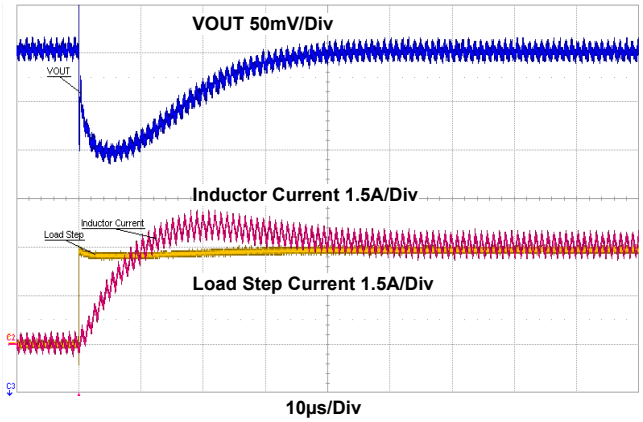


Figure 30. Buck Load Step ON Transient Response; V_{OUT} = 1.8V

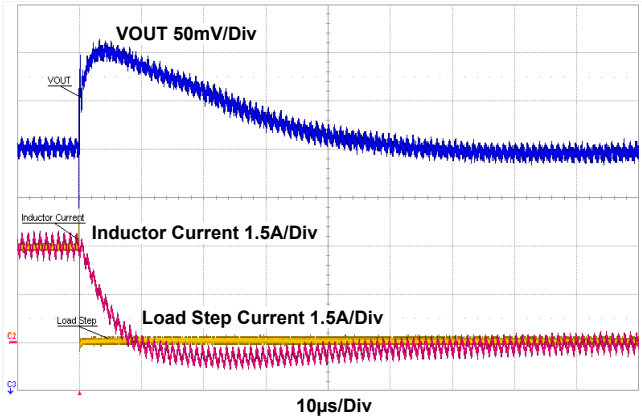


Figure 31. Buck Load Step OFF Transient Response; V_{OUT} = 1.8V

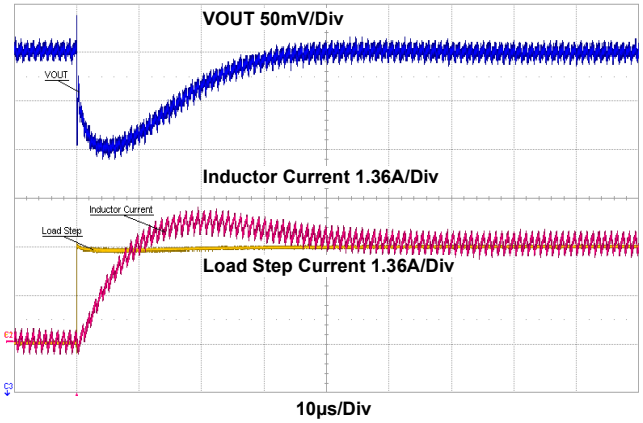


Figure 32. Buck Load Step ON Transient Response; V_{OUT} = 3.3V

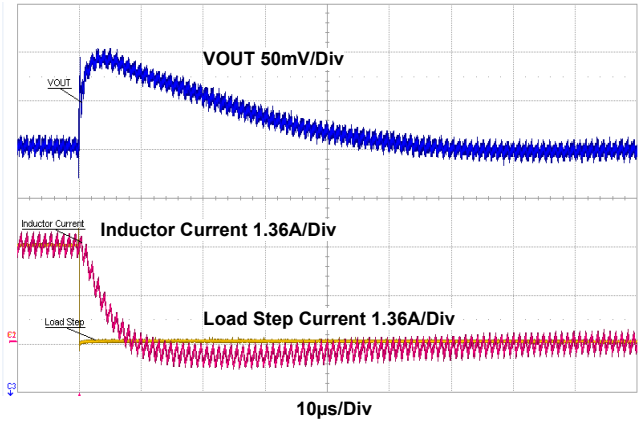


Figure 33. Buck Load Step OFF Transient Response; V_{OUT} = 3.3V

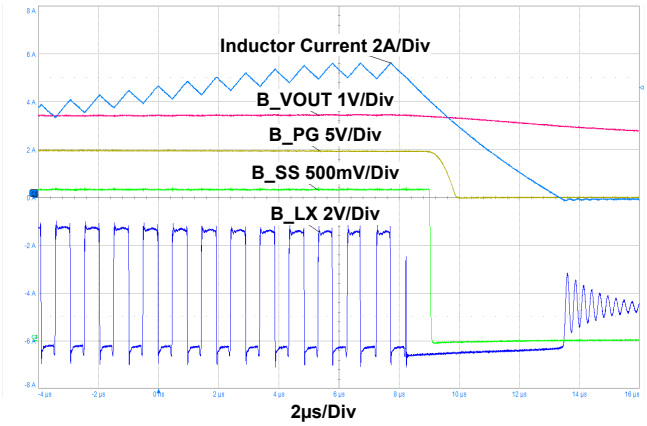


Figure 34. Buck Overcurrent Detection and Fault Response

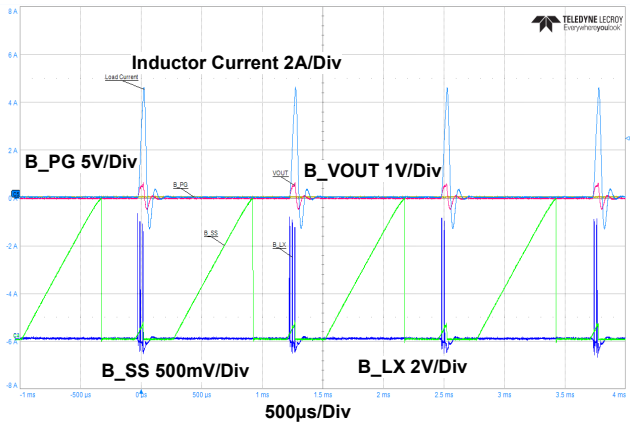


Figure 35. Buck Overcurrent Hiccup Operation

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

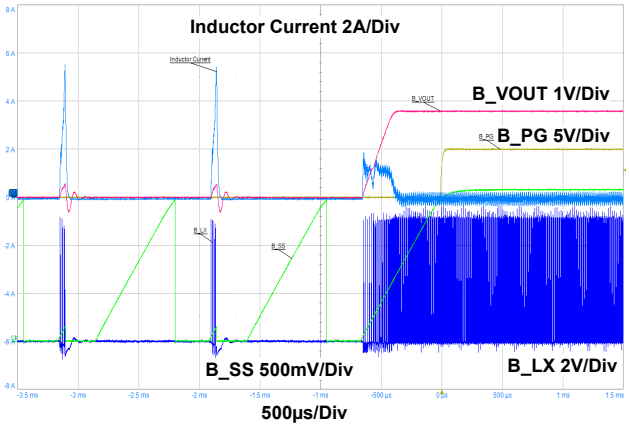


Figure 36. Buck Overcurrent Fault Recovery Response

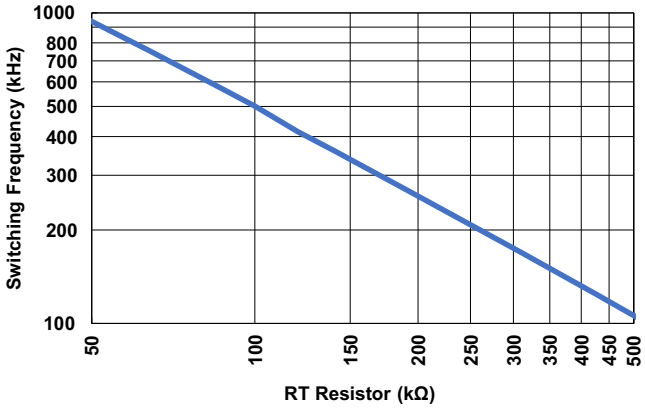


Figure 37. Buck Internal Oscillator RT vs f_{SW}

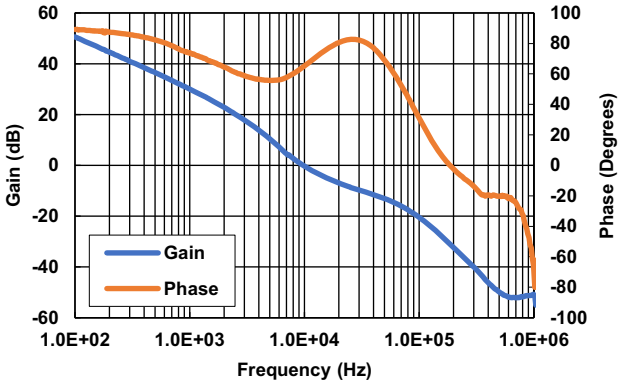


Figure 38. Buck Bode Plot; Load = 0A

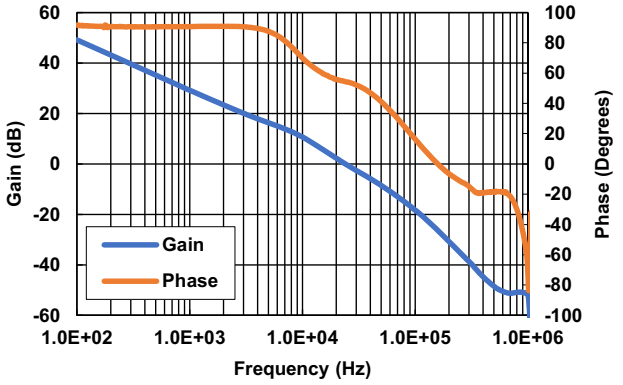


Figure 39. Buck Bode Plot; Load = 3A

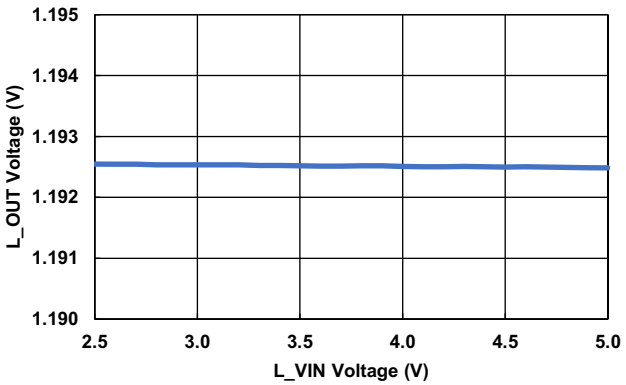


Figure 40. LDO Line Regulation; Load = 0A

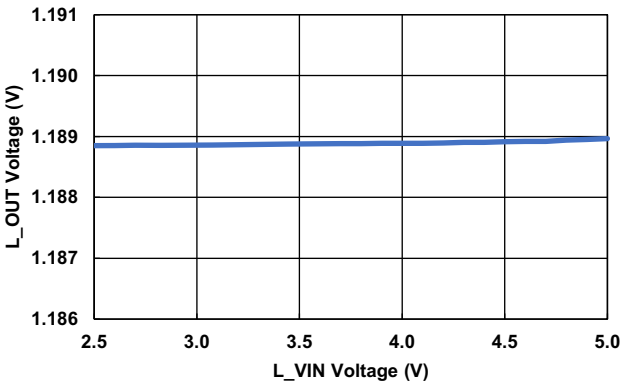


Figure 41. LDO Line Regulation; Load = 1A Sourcing

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

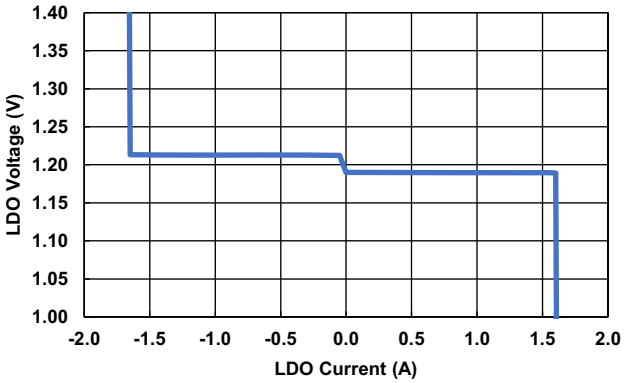


Figure 42. LDO Constant Current Limit Threshold

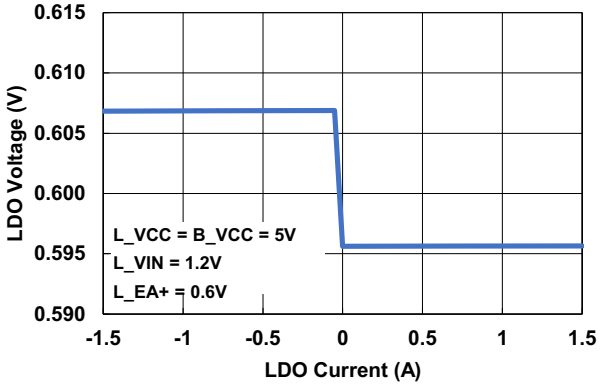


Figure 43. LDO Load Regulation; DDR4 Configuration

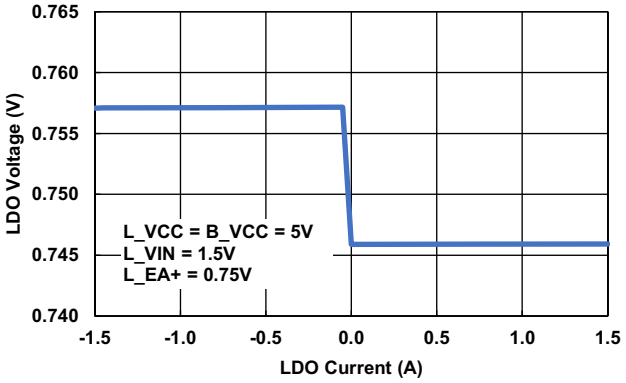


Figure 44. LDO Load Regulation DDR3 Configuration

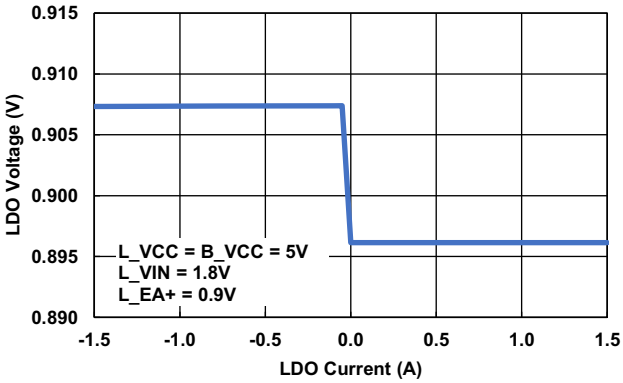


Figure 45. LDO Load Regulation DDR2 Configuration

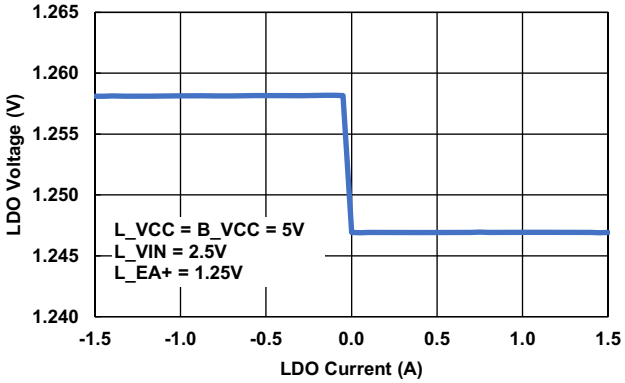


Figure 46. LDO Load Regulation DDR Configuration

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

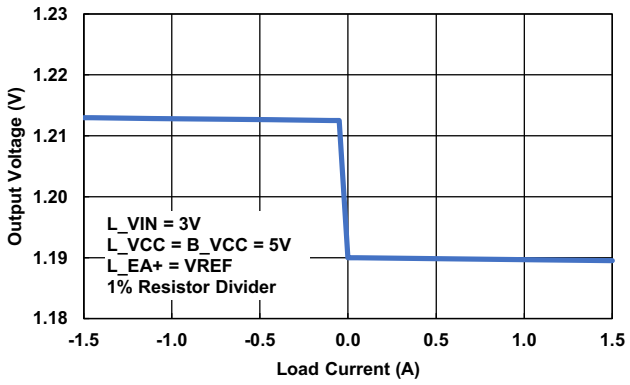


Figure 47. LDO Load Regulation Av = 2

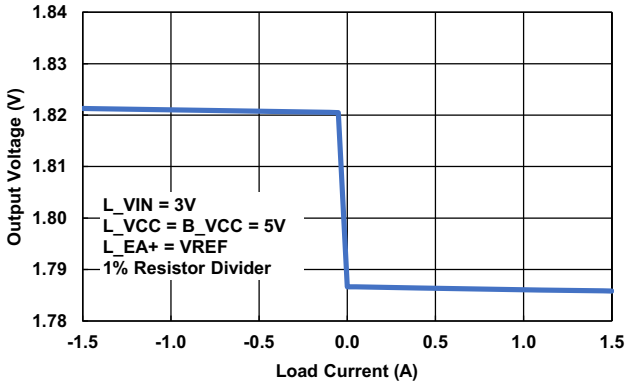


Figure 48. LDO Load Regulation Av = 3

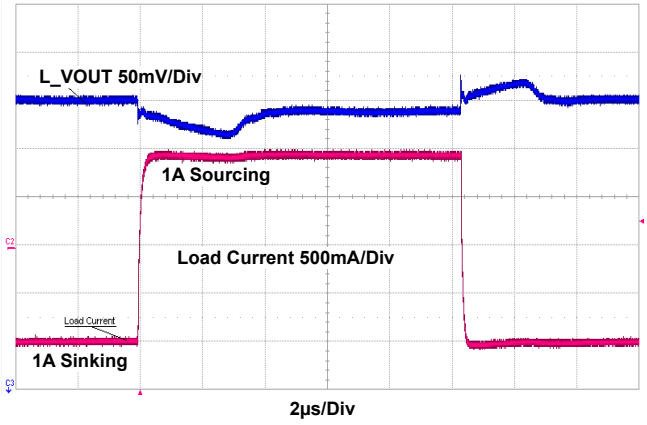


Figure 49. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.6V

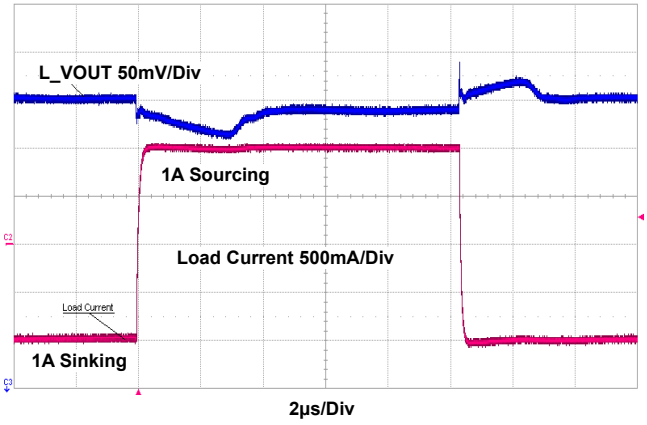


Figure 50. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.75V

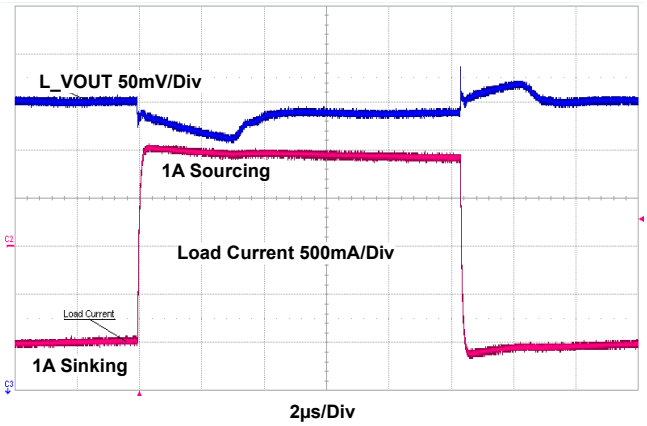


Figure 51. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 0.9V

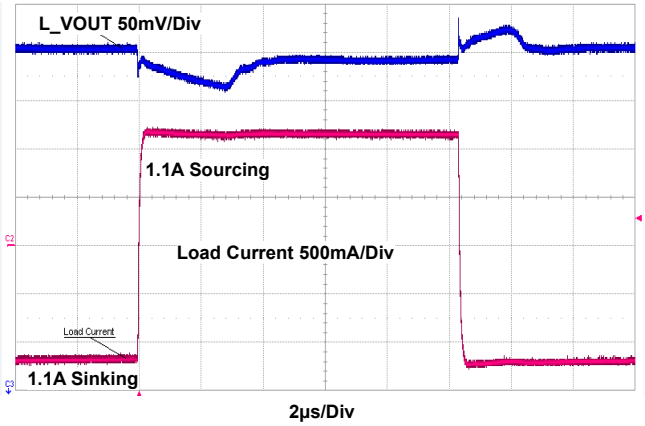


Figure 52. LDO Source-to-Sink Transient Response; L_OUT = L_EA- = L_EA+ = 1.25V

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

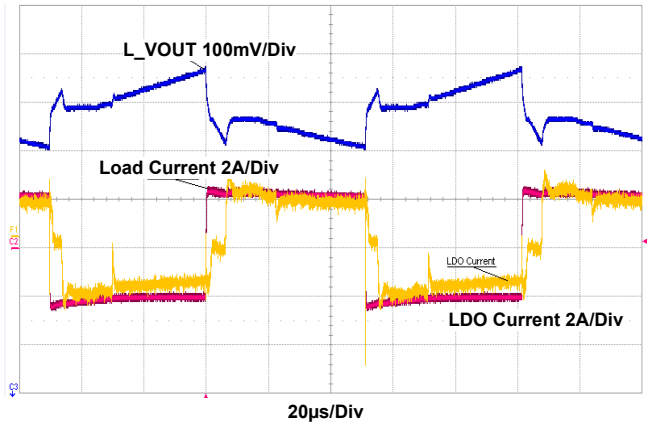


Figure 53. LDO Constant Current Limit Regulation Transient Response

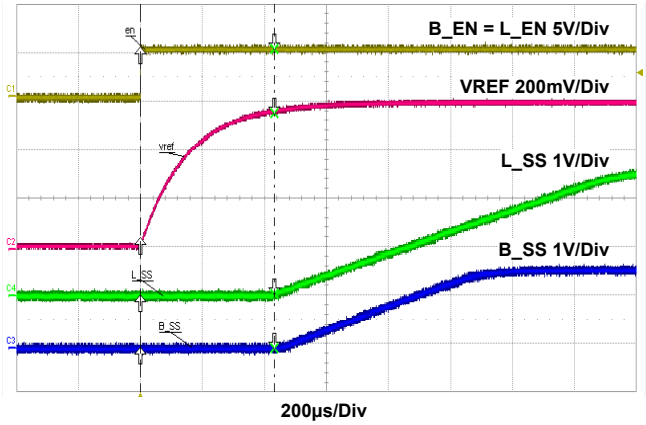


Figure 54. VREF Start-Up Timing on B_EN or L_EN Rising Edge; 100nF capacitor on VREF

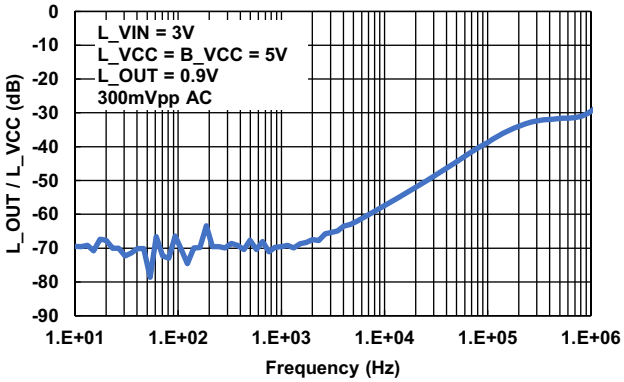


Figure 55. LDO L_VCC PSRR Curve; 1A Source

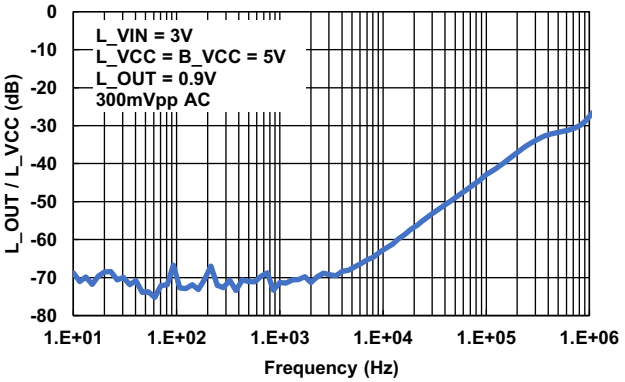


Figure 56. LDO L_VCC PSRR Curve; 1A Sink

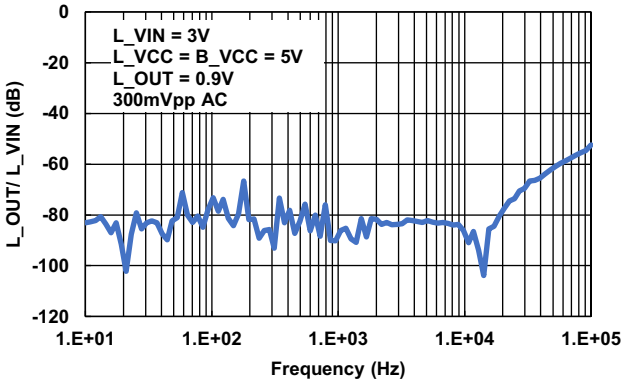


Figure 57. LDO L_VIN PSRR Curve; 1A Source

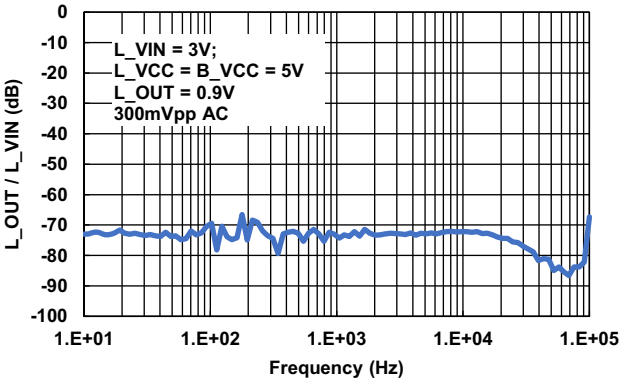


Figure 58. LDO L_VIN PSRR Curve; 1A Sink

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

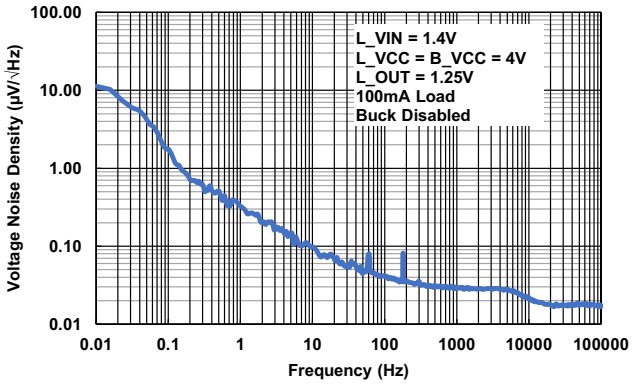


Figure 59. LDO Noise Spectral Density; Buck Disabled

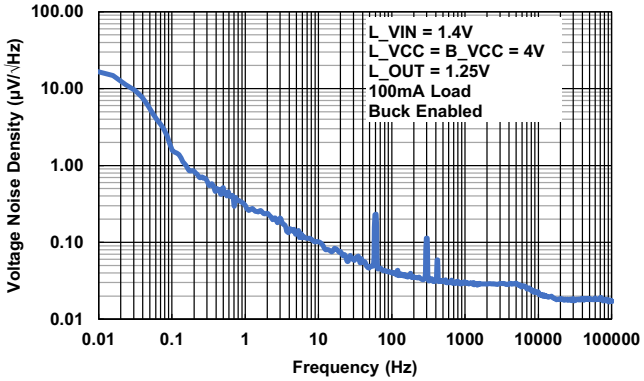


Figure 60. LDO Noise Spectral Density; Buck Enabled Dual Output FPGA Configuration

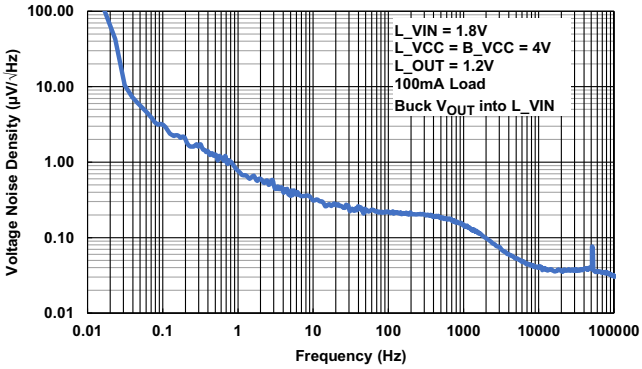


Figure 61. LDO Noise Spectral Density; B_OUT into L_VIN

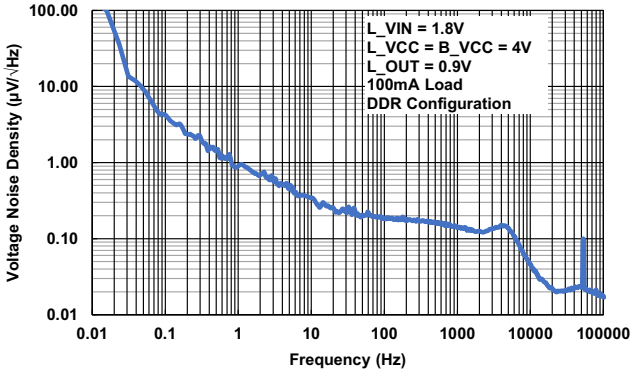


Figure 62. LDO Noise Spectral Density; DDR Configuration

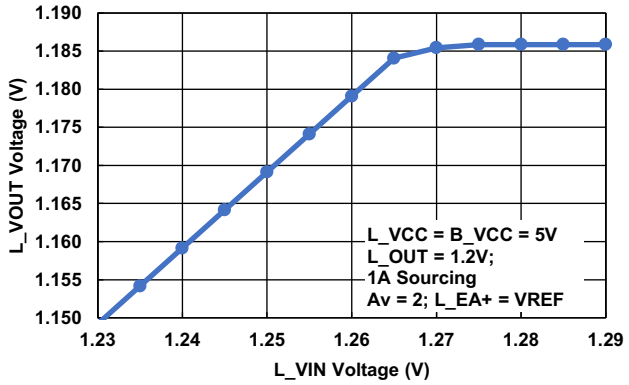


Figure 63. LDO Dropout Voltage; Av = 2

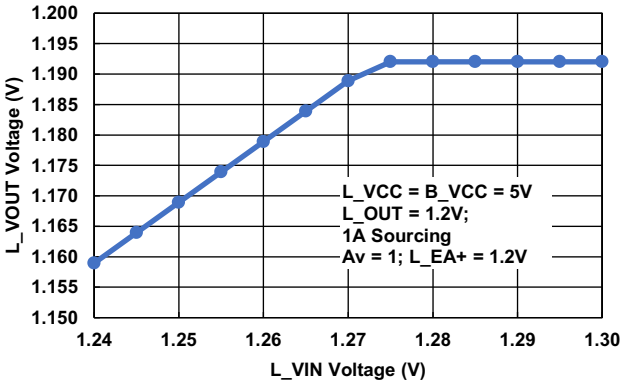


Figure 64. LDO Dropout Voltage; Av = 1

Unless otherwise noted, the test platform is the ISL70005SEHEV2Z where B_PVIN = B_VCC = L_VCC = 5V; L_VIN = 3V; B_OUT = 1.8V; f_{SW} = 1MHz; Buck C_{IN} = 150µF tantalum + 2x1µF ceramic; Buck C_{OUT} = 150µF tantalum + 2x1µF ceramic; L_{OUT} = 2.2µH; LDO C_{IN} = 150µF tantalum + 11µF ceramic; LDO C_{OUT} = 150µF tantalum +12µF ceramic; L_OUT = 1.2V; L_EA+ = VREF = 0.6V; T_A = +25°C. **(Continued)**

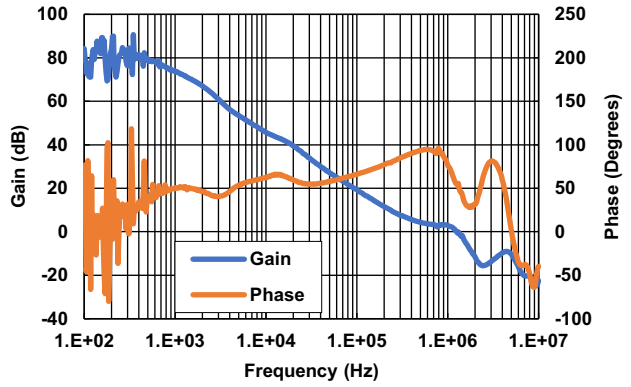


Figure 65. LDO Bode Plot; Av = 1; Sourcing 0.9A; L_VIN = 3V; L_OUT = 0.9V

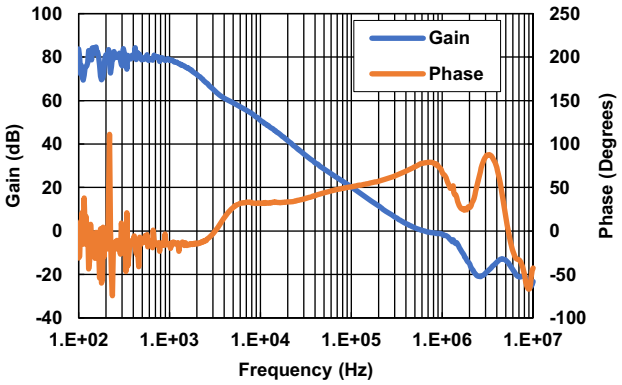


Figure 66. LDO Bode Plot; Av = 1; Sinking 0.9A; L_VIN = 3V; L_VOUT = 0.9V

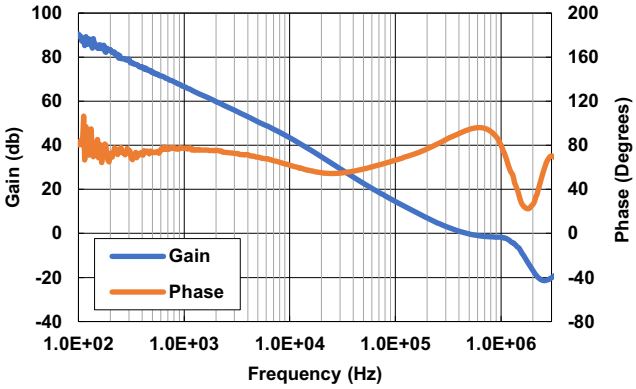


Figure 67. LDO Bode Plot; Av = 2; Sourcing 1.2A; L_VIN = 3V; L_OUT = 1.2V

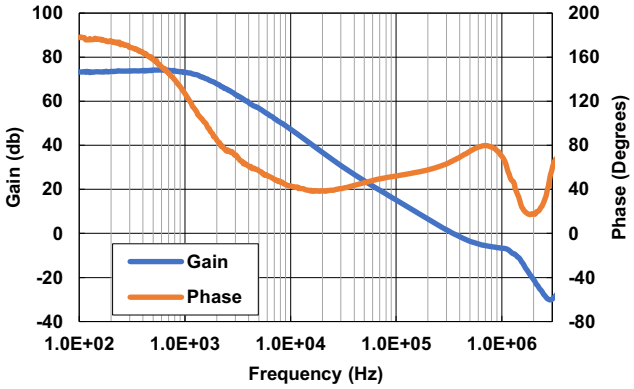


Figure 68. LDO Bode Plot; Av = 2; Sinking 1.2A; L_VIN = 3V; L_OUT = 1.2V

4. Functional Description

The ISL70005SEH and ISL73005SEH are radiation hardened dual output Point-of-Load (POL) regulators combining the high efficiency of a synchronous buck regulator with the low noise of a Low Dropout (LDO) regulator. This device is suited for systems with 3.3V or 5V power buses and can support continuous output load currents of 3A for the buck regulator and ±1A for the LDO.

The buck regulator uses a voltage mode control architecture and switches at a resistor adjustable frequency of 100kHz to 1MHz. Externally adjustable loop compensation allows for an optimum balance between stability and output dynamic performance. The internal synchronous power switches are optimized for high efficiency and excellent thermal performance.

The LDO is completely configurable independent of the switching regulator. It uses NMOS pass devices and separate chip bias voltage (L_VCC) to drive its gate, which enables the LDO to function with very low input voltages at the L_VIN NMOS input. Combined with low dropout performance, the LDO allows regulation with minimal power dissipation across a wide output voltage. The LDO can sink and source up to 1A continuously making it an ideal choice to power DDR memory.

The ISL70005SEH and ISL73005SEH offers independently on the Buck and LDO programmable soft-start and enable functions along with power-good indicators for ease of supply rail sequencing and other housekeeping requirements. In addition, these devices incorporate fault protection for the regulators. The protection features include over-temperature, input Undervoltage Lockout (UVLO), output undervoltage detection, output overvoltage detection and output overcurrent protection.

The ISL70005SEH and ISL73005SEH are available in a space saving 28 Ld ceramic dual flat-pack package or in die form and are specified to operate across the military temperature range of T_A = -55°C to +125°C.

4.1 Synchronous Buck Converter

4.1.1 Buck Architecture

The synchronous integrated FET buck regulator uses a voltage mode control architecture with external compensation. It is fabricated on a 0.6µm BiCMOS junction isolated process optimized for power management applications. With this device and a handful of external components, a complete synchronous buck DC/DC converter can be readily implemented.

4.1.2 Buck Enable Control

The B_EN pin accepts TTL/CMOS logic input levels. When the voltage on the B_EN pin exceeds its logic rising threshold, the controller monitors the POR voltage before initiating the soft-start for the PWM regulator. When B_EN is pulled low, the device enters a low power shutdown mode. The internal synchronous MOSFETs are held in a high impedance state while in shutdown mode.

4.1.3 Buck Soft-Start

The Buck regulator soft-start is enabled upon rising edge of B_EN. The soft-start function uses an internal current source and an external capacitor to create a reference ramp during start-up to minimize in-rush current to the output capacitors. The soft-start circuit clamps the error amplifier reference voltage to the lower of voltage between the external soft-start capacitor connected to the B_SS pin or the internal reference voltage (0.6V typical). The soft-start capacitor is charged by an internal current source. As the soft-start capacitor is charged, the output voltage ramps to the set point determined by the soft-start capacitor voltage and the feedback voltage. When the voltage on the B_SS pin is equal to the internal reference voltage, the soft-start interval is complete. When B_SS pin has charged to 1.6V (internally clamped) and with no fault conditions, the buck power-good B_PG pin goes high impedance. The soft-start capacitor is discharged by a 3.0Ω resistor whenever POR condition is not met or B_EN is pulled low.

The buck regulator is designed to soft-start into a pre-biased output that is less than its target regulation voltage. During soft-start there is no switching on the B_LXx pins until the B_SS voltage crosses the B_FB voltage to prevent discharging a pre-biased output. If the pre-bias output is above its target regulation voltage this is an overcharged condition for the buck regulator. For a soft-start into an overcharged condition, the buck regulator

does not complete soft-start. When the B_SS pin voltage reaches 1.6V, the soft-start capacitor is internally discharged to 0V and begins a new soft-start cycle with no switching on B_LXx. This condition repeats until the pre-bias output voltage is reduced below the target regulation voltage.

4.1.4 Switching Frequency with B_RT and B_SYNC

The buck regulator PWM switching frequency is set through the internal oscillator with an adjustable range of 100kHz to 1MHz. An external termination resistor, RT, from the B_RT pin to B_GND sets the oscillator frequency. See "Switching Frequency Selection and External Sync for Buck Regulator" on page 31 for more information on setting the RT resistor.

The switching frequency can also be synchronized to an external clock through the B_SYNC pin. During soft-start the clock at B_SYNC is ignored and the PWM controller uses the internal oscillator for switching until the soft-start voltage is above the internal 600mV reference voltage where it synchronizes to B_SYNC. The synchronization frequency range is 100kHz to 1MHz. If external synchronization is not used, tie B_SYNC to GND.

4.1.5 Buck Power-Good

The B_PG power-good indicator is an open-drain logic output. On completion of soft-start and without a fault condition on the buck regulator, the B_PG pin is high impedance. An external pull-up resistor to B_VCC is used for logic high indicating the buck output is operating in regulation. The recommended range for the pull-up resistor is 10kΩ to 100kΩ. Before soft-start completes or in a fault condition, the B_PG pin is actively pulled low to indicate buck output is not operating in regulation. To mitigate SEE, bypass the B_PG pin to B_GND with a 1nF ceramic capacitor.

4.1.6 Buck Integrated Power MOSFETs

The buck regulator integrates two synchronous operation MOSFETs for the power stage. The high-side MOSFET is a PMOS and the low-side MOSFET is an NMOS. The MOSFETs are optimized for low $r_{DS(ON)}$ to provide excellent efficiency over the 3A load current operating range.

4.1.7 Buck Error Amplifier Output

The B_COMP pin is the output of the error amplifier. The voltage on B_COMP determines the duty cycle at B_LXx. For voltage mode control, a Type III compensation network must be connected between B_FB and B_COMP to stabilize the feedback loop. See "Buck Feedback Compensation Design" on page 36 for the design of the Type III compensator. The B_COMP pin analog range is from 100mV to 0.4*B_VCC that correlates to the B_LXx duty cycle from minimum on-time to minimum off-time.

4.1.8 Buck Overcurrent Limiting

The buck regulator integrates cycle-by-cycle output overcurrent limiting. Peak inductor current is sensed on the integrated high-side PMOS FET. If the high-side switch current exceeds the overcurrent threshold (5.3A typical), the PMOS turns off and the low-side NMOS FET is turned on for the remainder of the switching cycle. After four consecutive detections of cycle-by-cycle current limiting, the Buck regulator enters an overcurrent fault protection mode as described in Buck Fault Protection. The minimum response time from the high-side PMOS turn-on to overcurrent detection is determined by the B_LX minimum on-time specified in the Electrical Specification table on page 10. The response time from overcurrent detection to the high-side PMOS turn-off is approximately 60ns. See Figure 35 and Figure 36.

4.1.9 Buck Fault Protection

The buck regulator integrates output overvoltage detection, output undervoltage protection, overcurrent protection and over-temperature protection. The fault response for output overvoltage only pulls the B_PG pin low to indicate an overvoltage condition. After recovery from an overvoltage, the B_PG pin is released. The fault response for an undervoltage or overcurrent condition pulls the B_PG pin low and starts a hiccup mode, after which a time delay causes the controller to start a soft-start cycle. The hiccup mode continues indefinitely until the fault condition recovers. If the soft-start completes with no fault condition, the B_PG pin is released. The fault response for an over-temperature condition pulls the B_PG and B_SS pins low and disables switching on B_LXx. After recovery

from over-temperature condition, a soft-start cycle is initiated. After a successful soft-start, the B_PG pin is released.

The undervoltage and overvoltage fault detection is implemented by sensing the B_FB voltage and comparing it to internal references for undervoltage and overvoltage thresholds. For the buck regulator, there are two Undervoltage (UV) thresholds. The first UV threshold (typically 89% of regulation) only flags the B_PG pin to indicate an undervoltage condition. The second UV threshold (typically 75% of regulation) produces a fault response on the buck converter where it operates in hiccup mode. See Buck Hiccup Operation for a description of Hiccup operation.

4.1.10 Buck Hiccup Operation

The buck regulator operates in hiccup mode when an output undervoltage or overcurrent condition occurs. During these fault conditions, the B_LXx pins are tri-stated and the B_SS pin is internally discharged. The buck regulator goes through a dummy soft-start cycle where the B_SS capacitor is charged by the internal current source but there is no switching on B_LXx. When the B_SS capacitor is fully charged (internally clamped to 1.6V), the B_SS pin is discharged again. The buck regulator then attempts a normal soft-start. This cycle repeats until the fault condition is removed to allow the buck regulator to go through a successful soft-start where B_PG is released.

4.2 Low Dropout Regulator (LDO)

4.2.1 LDO Architecture

The LDO on the ISL70005SEH and ISL73005SEH is designed with NMOS pull-up and NMOS pull-down FETs with source and sink capability of up to 1A. Separate gate bias (L_VCC) and pass FET input (L_VIN) pins allow output voltage regulation up to L_OUT = L_VCC-1.5V and low dropout performance down to L_VIN = 0.775V.

The LDO uses separate feedback loops for voltage regulation when sourcing and sinking current. To prevent internal shoot-through between the transition of the source and sink regulation loop, a small dead-band voltage region disables the LDO output at the LDO output current sourcing and sinking transition. During this dead-band voltage, both the LDO sourcing and sinking NMOS FETs are disabled. Any load current sources from or sinks into the output capacitor, raising or lowering the output voltage until it is out of the dead-band region where the LDO resumes voltage regulation. The dead-band voltage is precision trimmed to ±5mV around the target regulation voltage at unity gain feedback and is amplified by the feedback gain value. For example with L_EA+ = 0.6V and L_OUT = 1.2V, the dead-band voltage is ±10mV due to the feedback gain of 2. See Equation 1 for calculating the dead-band voltage above and below the LDO target regulation voltage. For sourcing current, the dead-band voltage is negative (LDO output is a dead-band voltage below target regulation voltage) and for sinking current, the dead-band voltage is positive (LDO output is a dead-band voltage above target regulation voltage). During transient loading conditions from sourcing current to sinking current (or from sinking current to sourcing current), the delay time for the LDO to resume regulation after sensing it is outside the dead-band region is typically 3µs. During this delay time, sourcing or sinking load current is provided only by the output capacitor on L_OUT. See Figure 49 through Figure 53.

(EQ. 1) $$V_{DeadBand} = \pm 5mV \bullet \left(\frac{L\_OUT}{L\_EA+}\right)$$

4.2.2 LDO Enable Control

The L_EN pin accepts TTL/CMOS logic input levels. When the voltage on the L_EN pin exceeds its logic rising threshold, the controller monitors the POR voltage before initiating the soft-start for the LDO. When L_EN is pulled low, the device enters a low power shutdown mode.

4.2.3 LDO Soft-Start

The LDO regulator soft-start is enabled on the rising edge of L_EN. The soft-start circuitry for the LDO is similar to the soft-start circuit on the buck regulator. The L_SS pin soft-start uses an internal current source and an external capacitor to create a reference ramp during start-up to minimize in-rush current to the output capacitors. The soft-start circuit clamps the error amplifier reference voltage to the lower of voltage between the external soft-start

capacitor connected to L_SS or the reference voltage connected to L_EA+. The soft-start capacitor is charged by an internal current source. As the soft-start capacitor is charged, the output voltage ramps to the set point determined by the soft-start capacitor voltage and the feedback voltage. When the voltage on the L_SS pin is equal to the L_EA+ reference voltage, the soft-start interval is complete. When the L_SS pin has charged to 2.6V (internally clamped) and with no fault conditions, the LDO power-good L_PG pin is released. The soft-start capacitor is discharged by a 3.0Ω resistor whenever the Power-On Reset (POR) condition is not met or L_EN is pulled low.

The LDO sources or sinks up to a limited constant current (1.65A typical) into a pre-biased output during soft-start to charge or discharge the output capacitor to bring L_OUT to the regulation voltage set by the ramping L_SS reference.

4.2.4 LDO Error Amplifier Inputs

The LDO has two error amplifier inputs. The L_EA- pin is the inverting feedback pin that sets the output voltage. The L_EA+ pin is the non-inverting reference pin. The L_EA+ pin must be connected to a voltage such as the VREF pin (0.6V typical) or to the buck output for tracking applications. The recommended analog voltage range of L_EA+ is 0.6V to 1.27V.

4.2.5 LDO Output Overcurrent Limiting

The LDO integrates output overcurrent protection by operating in constant current limit when the current reaches the overcurrent threshold (1.65A for sourcing or sinking, typical). In constant current limit the LDO does not regulate output voltage. Sourcing or sinking load currents beyond the constant current limit is supported by the output capacitor, causing the output voltage to rise or fall until the overcurrent condition recovers. There is a 18µs typical delay time between detecting an overcurrent condition until the constant current limiting is active for both sourcing and sinking. See Figure 42 and Figure 53.

4.2.6 LDO Power-Good

The L_PG power-good indicator is an open-drain logic output. After completion of soft-start and without a fault condition on the LDO, the L_PG pin is high impedance. An external pull-up resistor to L_VCC is used for logic high indicating the LDO output is operating in regulation. The recommended range for the pull-up resistor is 10kΩ to 100kΩ. Before soft-start completes or in a fault condition, the L_PG pin is actively pulled low to indicate LDO output is not operating in regulation. To mitigate SEE, bypass the L_PG pin to L_GND with a 1nF ceramic capacitor.

4.2.7 LDO Fault Protection

The LDO integrates output undervoltage detection, output overvoltage detection, output overcurrent protection, and over-temperature protection. When the LDO output current reaches the source or sink overcurrent threshold, it operates in constant current limit with no regulation on LDO output voltage. While the LDO operates in constant current limit but does not cross the undervoltage or overvoltage thresholds, there is no fault response on the L_PG pin. The undervoltage and overvoltage fault detection is implemented by sensing the L_EA- voltage and comparing it to internal references for the undervoltage and overvoltage thresholds. The fault response for an output undervoltage or overvoltage only pulls the L_PG pin low to indicate a fault condition. After recovery from an output undervoltage or overvoltage condition, the L_PG pin is released. The LDO integrates over-temperature thermal shutdown. The fault response to an over-temperature condition is similar to the buck regulator. The L_SS pin is discharged and the L_PG pin is pulled low while the L_OUT pin is high impedance. After recovery from an over-temperature condition, a soft-start cycle is initiated. After a successful soft-start, the L_PG pin is released.

4.3 Internal Reference Voltage

The ISL70005SEH and ISL73005SEH integrate a 0.6V reference with ±1% tolerance over line, temperature, and radiation that is precision trimmed for the buck regulator. This reference voltage is trimmed with the input offset of buck error amplifier compensated. The reference voltage coming out to the VREF pin is prior to the buck regulator error amplifier. Therefore, VREF includes the input offset voltage of the error amplifier that reduces the accuracy of VREF pin to ±1.5% tolerance.

During the first rising edge of B_EN (Buck enable) or L_EN (LDO enable), the internal reference voltage is also enabled. When the VREF pin voltage reaches 0.564V (94% of 0.6V), soft-start begins on either the B_SS (Buck soft-start) or L_SS (LDO soft-start) pin. Renesas recommends decoupling the VREF pin to L_GND for SEE mitigation. The minimum recommended value is 100nF. VREF has a typical source impedance of 1.7kΩ. Therefore, the delay from a rising edge of enable to the beginning of soft-start is determined by the RC time constant to reach 94% of 0.6V. For a 100nF capacitor on VREF, the typical delay time is approximately 500µs. See Figure 54 for an example of the VREF start-up time to the beginning of the soft-start delay.

4.4 Over-Temperature Detection

The over-temperature detection circuit on the ISL70005SEH and ISL73005SEH is located near the LDO output as this is where most of the power dissipation occurs in the circuit. When an over-temperature condition is detected, the fault response is as described in "Buck Fault Protection" on page 27 for the buck regulator and "LDO Fault Protection" on page 29 for the LDO. The over-temperature rising threshold is typically T_J = 175°C with a recovery hysteresis of 8°C. Power dissipation from the Buck or LDO causes a differential temperature from junction that triggers an over-temperature condition at a lower ambient temperature.

5. Applications Information

5.1 Power Supply Biasing

It is necessary in application to have B_VCC, L_VCC, and B_VIN biased to the same RMS DC voltage. A low pass filter can be placed on B_VIN to B_VCC and L_VCC to provide noise filtering on the analog supplies. A 1Ω resistor and 0.1µF capacitor on B_VCC = L_VCC to B_GND = L_GND is recommended. The L_VCC input UVLO threshold is specified in the electrical specification table with a typical rising threshold of 2.8V. Below UVLO both the B_LXx and L_OUT output is high impedance. B_VIN is the input to the buck synchronous power MOSFETs and L_VIN is the input to the LDO upper NMOS FET. The recommended input voltage range of B_VCC, L_VCC, and B_VIN is 3V to 5.5V. The recommended input voltage range of L_VIN is from 1.0V to L_VCC. There are no power sequencing requirements for the B_VCC = L_VCC = B_VIN and L_VIN power supplies.

5.2 Switching Frequency Selection and External Sync for Buck Regulator

The internal oscillator frequency for the synchronous buck regulator is programmable by an external resistor on the B_RT pin. Select the RT resistor based on Figure 37 and Equation 2. For external synchronization applications using the B_SYNC pin, the recommendation is for the external synchronization frequency to be as near as possible to the internal oscillator frequency set by RT resistor to minimize voltage transients at the buck output during the internal to external synchronization.

$$RT(k\Omega) = \frac{54348}{f_{SW}(kHz)} - 8.9 \quad \text{(EQ. 2)}$$

During soft-start, the PWM controller uses its internal oscillator frequency set by the B_RT resistor value. When B_SS voltage > 600mV the PWM controller synchronizes to the external clock on B_SYNC.

In application, the internal oscillator to external clock synchronization occurs after eight clock cycles on B_SYNC.

5.3 B_EN and L_EN Pins

The ISL70005SEH and ISL73005SEH internal band-gap is enabled by the logic high of B_EN or L_EN. After the band-gap is enabled, soft-start begins when VREF pin is typically 94% of the nominal 600mV. The delay time for VREF rising is typically 500µs with a 100nF capacitor on VREF. The 100nF capacitor is for SEE mitigation.

In application, the first rising edge of B_EN or L_EN includes the VREF delay time before soft-start initiates and impacts the start-up timing between B_EN or L_EN first rising to B_PG or L_PG rising. If the band-gap is already enabled, during the rising edge of B_EN or L_EN there is approximately 50µs delay before soft-start begins. For buck always on applications, tie B_EN to B_VCC = L_VCC. For LDO always on applications, tie L_EN to B_VCC = L_VCC.

See Figure 22 to Figure 27 for soft-start timing from enable to power-good indication.

5.4 Soft-Start Capacitor for Buck

Place a soft-start capacitor on B_SS pin to B_GND. A 23µA typical current source on B_SS charges the soft-start capacitor to set the voltage ramp to the error amplifier during soft-start. The value of the soft-start capacitor determines the time to ramp the buck output voltage into regulation (B_SS reaches 0.6V). B_SS is internally clamped to 1.5V. When B_SS reaches the internally clamped 1.5V and with no other fault condition, the B_PG pin is released. Use Equation 3 to determine the capacitor needed for the soft-start time to ramp the buck output voltage into regulation. Use Equation 4 to determine the time for B_PG to go high after enabling the buck.

$$C_{SS}(nF) = \frac{I_{SS}(\mu A)}{0.6V} \bullet t_{SS}(ms) \quad \text{(EQ. 3)}$$

$$t_{PG}(ms) = \frac{1.5V}{I_{SS}(\mu A)} \bullet C_{SS}(nF) \quad \text{(EQ. 4)}$$

5.5 Soft-Start Capacitor for LDO

Place a soft-start capacitor on L_SS pin to L_GND. A 23µA typical current source on L_SS charges the soft-start capacitor to set the voltage ramp to the error amplifier during soft-start. The value of the soft-start capacitor determines the time to bring the LDO output voltage into regulation (L_SS reaches L_EA+). L_SS is internally clamped to 2.6V. When L_SS reaches the internally clamped 2.6V and with no other fault condition, the L_PG pin is released. Choose a soft-start capacitor based on the soft-start time using Equation 5 below. To avoid reaching the LDO constant current limit during soft-start to charge the LDO output capacitor, choose a soft-start capacitor using Equation 6 below. The constant current limit is 1.65A typical, 1.2A minimum. Use Equation 7 to determine the time for L_PG to go high after enabling the LDO.

(EQ. 5) $$C_{SS}(nF) = \frac{I_{SS}(\mu A)}{L\_EA+} \bullet t_{SS}(ms)$$

(EQ. 6) $$C_{SS}(nF) > \frac{I_{SS}(\mu A)}{1000 \bullet I_{CCLimit}(A)} \bullet C_{OUT}(\mu F)$$

(EQ. 7) $$t_{PG}(ms) = \frac{2.6V}{I_{SS}(\mu A)} \bullet C_{SS}(nF)$$

5.6 Power-Good Indicator Pins

Use a 10kΩ or larger pull-up resistor on the B_PG and L_PG pins to B_VCC = L_VCC for power-good indication. A 1nF capacitor on the B_PG and L_PG pin to B_GND and L_GND is recommended for SEE mitigation. B_PG and L_PG can be connected together for a wired-OR single power-good indicator.

5.7 Independent Output Point-of-Load Application

The ISL70005SEH and ISL73005SEH can be used in a dual output Buck and LDO regulator for use in applications such as the FPGA core and I/O supply rail. Independent enable control, soft-start, and power-good indicator are available for the Buck and LDO (see Figure 3 on page 4).

5.8 LDO Tracking Buck for DDR Memory Application

The ISL70005SEH and ISL73005SEH can be configured for LDO tracking Buck application (see Figure 4 on page 4).

Specifically for DDR, DDR2, DDR3, and DDR4 memory applications, the 1A source and sink LDO is configured as the VTT rail regulator. The buck configured as the VDDQ regulator can be used to bias the LDO L_VIN input to minimize power dissipation in the LDO. The VDDQ output is divided by half with a resistor divider to set the reference voltage on the LDO L_EA+ pin. Connect L_OUT to L_EA- for unity gain to set L_OUT = L_EA+ = VDDQ/2. For accurate tracking, do not place any capacitance on the L_EA+ pin to L_GND. Otherwise transient voltages on the buck regulator output are not properly tracked by the LDO output due to the RC delay formed by the resistor divider and capacitor into the L_EA+ reference input. Use proper PCB layout to minimize noise into L_EA+ pin.

For accurate tracking during soft-start, the recommendation is to use a smaller soft-start capacitor on L_SS compared to B_SS. This ensures that the lowest reference voltage to the error amplifier on the LDO is only set by L_EA+, which is controlled by the ramping voltage on B_SS pin.

6. Synchronous Buck Design Guide

6.1 Buck Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot and undershoot across the internal MOSFETs of the synchronous buck regulator. Use small low ESR ceramic capacitors for high-frequency decoupling and bulk capacitors to supply the current needed each time the upper MOSFET turns on. Place the small ceramic capacitors physically close to the MOSFETs between the drain of the upper MOSFET (B_VINx pins) and the source of the lower MOSFET (B_PGNDx pins).

The important parameters for the bulk input capacitance are the voltage rating and the RMS current rating. For reliable operation, select bulk capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. Their voltage rating should be at least 1.25 times greater than the maximum input voltage, while a voltage rating of 1.5 times is a conservative guideline. For most cases, the RMS current rating requirement for the input capacitor of a buck regulator is approximately 1/2 the DC load current.

The maximum RMS current through the input capacitors may be closely approximated using Equation 8.

(EQ. 8) $$I_{CINrms} = \sqrt{\frac{V_{OUT}}{V_{IN}} x \left({I_{OUT}}_{MAX}^{2} x \left(1 - \frac{V_{OUT}}{V_{IN}} \right) + \frac{1}{12} x \left(\frac{V_{IN} - V_{OUT}}{L x f_{OSC}} x \frac{V_{OUT}}{V_{IN}} \right)^{2} \right)}$$

The recommended bulk input capacitor is a 150µF low ESR tantalum capacitor. The capacitor used for the ISL70005SEHEV2Z evaluation platform is an AVX TPM series 16V tantalum with 30mΩ ESR. Place a 0.1µF and 10nF high frequency low ESR ceramic capacitor close to the B_VINx and B_PGNDx pins. These capacitors provide the instantaneous current into the buck regulator during the high frequency switching transitions.

6.2 Buck Output Capacitor Selection

An output capacitor is required to filter the inductor ripple current and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally achieved with a combination of bulk and decoupling capacitors with careful layout.

High-frequency low ESR ceramic capacitors initially supply the transient load current and reduce the current load slew rate seen by the bulk capacitors. The bulk filter capacitor values are generally determined by the Effective Series Resistance (ESR) and voltage rating requirements rather than actual capacitance requirements. Place high-frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components.

The shape of the output voltage waveform during a load transient that represents the worst case loading conditions ultimately determines the number of output capacitors and their type. When this load transient is applied to the regulator, most of the current required by the load is initially contributed by the output capacitors. This is due to the finite amount of time required for the inductor current to slew up or down to the level of the output current required by the load. This results in a momentary undershoot or overshoot in the output voltage. At the initial edge of the transient undershoot or overshoot, the Equivalent Series Inductance (ESL) of each capacitor induces a spike that adds on top of the voltage drop due to the ESR. After the initial spike, the output voltage dips down (load step on) or peaks up (load step off) as the output capacitor sources or sinks the transient load current until the output inductor current reaches the load current. Figure 69 on page 34 shows a typical response of the output voltage to a transient load current.

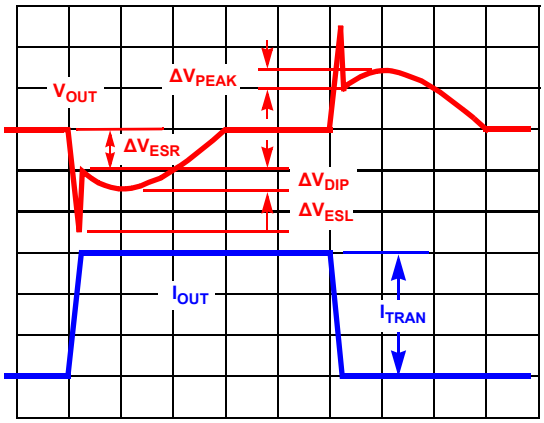


Figure 69. Typical Transient Response

The amplitudes of the voltage spikes caused by capacitor ESR and ESL is approximated by Equation 9:

(EQ. 9) $$\Delta V_{ESR} = ESR \bullet I_{TRAN}$$

$$\Delta V_{ESL} = ESL \bullet \frac{dI_{TRAN}}{dt}$$

where I_{TRAN} = Output load current transient.

In a typical converter design, the ESR of the output capacitor bank impacts the transient response. The ESR and the ESL determine the number output capacitors required to minimize the initial voltage spike at the output transient response. It may be necessary to place multiple output capacitors in parallel to reduce the parasitic ESR and ESL to achieve minimize the magnitude of the output voltage spike during a load transient response.

The ESL of the capacitor, which is an important parameter, is not usually listed in datasheets. Practically it can be approximated using Equation 10 if an Impedance vs Frequency curve is given, where f_{res} is the frequency where the lowest impedance is achieved (resonant frequency). The ESL of the capacitor becomes a concern when designing circuits that supply power to loads with high rates of change in the current.

(EQ. 10) $$ESL = \frac{1}{C(2 \bullet \pi \bullet f_{res})^2}$$

If ΔV_{DIP} and/or ΔV_{PEAK} is too large for the output voltage limits, the amount of capacitance may need to be increased. In this situation, a trade-off between output inductance and output capacitance may be necessary.

The recommended bulk output capacitor is a 150µF low ESR tantalum capacitor. The capacitor used for the ISL70005SEHEV2Z evaluation platform is an AVX TPM series 16V tantalum with 30mΩ ESR. In addition, place the high frequency ceramic decoupling closed to the load for optimal performance during transient loads.

6.3 Buck Output Inductor Selection

The output inductor is selected to minimize the response time of the regulator to a load transient and meet steady-state output voltage ripple requirements. A smaller inductance value improves transient response but increases output voltage ripple. The inductor value determines the inductor ripple current with the output voltage ripple being a function of the ripple current. The inductor ripple current and output voltage ripple are approximated using Equation 11 and Equation 12:

(EQ. 11) $$I_{RIPPLE} = \frac{(V_{IN} - V_{OUT})}{f_{SW} \bullet L} \bullet \frac{V_{OUT}}{V_{IN}}$$

(EQ. 12) $$V_{OUT\_RIPPLE} = I_{RIPPLE} \bullet ESR$$

where ESR is the output capacitor equivalent series resistance.

Increasing inductance reduces the ripple current and output voltage ripple; however, the regulator response time to transient load is increased.

One of the parameters limiting the response of the regulator to a load transient is the time required to change the inductor current. The response time is the time required to slew the inductor current from its initial level to the transient level. During this interval the difference between the inductor current and the transient load current is sourced from or sunk into the output capacitor. Minimizing the response time reduces the amount of transient voltage overshoot and undershoot on the output capacitor.

The response time to a transient is different for the transient load on and off. Equation 13 gives the approximate response time to a load step.

(EQ. 13) **Load On:** $t_{RISE} = \frac{L \bullet I_{TRAN}}{V_{IN} - V_{OUT}}$ **Load Off:** $t_{FALL} = \frac{L \bullet I_{TRAN}}{V_{OUT}}$

- I_{TRAN} is the transient load current step
- t_{RISE} is the inductor response time to a turn on load step
- t_{FALL} is the response time to a turn off load step

The worst case response time can be during either the load step on or off. Check for transient load response for both turn-on and turn-off at minimum and maximum load current.

The recommended inductor is 2.2µH for 1MHz applications. The inductor used for the ISL70005SEHEV2Z evaluation platform is a Coilcraft XFL4020 series 2.2µH with 21mΩ DCR.

The inductor saturation current rating is recommended to be above the peak overcurrent threshold of the ISL70005SEH (typical 5.35A, maximum 6.0A) to ensure that inductor does not saturate operating near the overcurrent condition. Inductor saturation along with standard tolerance over temperature and life can decrease the inductance and increase ripple current.

6.4 Buck Output Voltage Setting

The Buck regulator output voltage is set by two feedback resistors connected from the V_{OUT} to B_FB and B_FB to B_GND. See Equation 14 for setting the buck output voltage.

(EQ. 14) $\text{Buck } V_{OUT} = 0.6V \bullet \left(\frac{R_1}{R_4} + 1\right)$

where R_1 is from Buck V_{OUT} to B_FB and R_4 is from B_FB to B_GND.

The resistor R_1 is recommended to be in the range of 10kΩ to 30kΩ. The value of R_1 controls the design of the Type III Compensation network to stabilize the feedback loop (see "Buck Feedback Compensation Design" on page 36). For Buck V_{OUT} = 0.6V, connect V_{OUT} directly to B_FB.

Because of the minimum t_{ON} (325ns, maximum) and t_{OFF} times (165ns, maximum) of the ISL70005SEH and ISL73005SEH Buck B_LXx pins and the selected switching frequency f_{SW}, the buck regulator is restricted by a duty cycle limitation that bounds the upper and lower output voltage achievable. The equations for minimum and maximum buck output voltage is calculated below on Equations 15 and 16.

(EQ. 15) $V_{OUT\_MIN} = [\text{Min ON-Time (max)} + \text{Dead Time (max)}] \bullet f_{SW(max)} \bullet [V_{IN\_(MAX)} - I_{OUT\_MIN} \bullet (r_{DSON(high)} - r_{DSON(low)})] - I_{OUT\_MIN} \bullet (r_{DSON(low)} + R_{DCR})$

(EQ. 16) $V_{OUT\_MAX} = [1 - (\text{Min OFF-Time (max)} + \text{Dead Time (max)}) \bullet f_{SW(max)}] \bullet [V_{IN\_(MIN)} - I_{OUT\_MAX} \bullet (r_{DSON(high)} - r_{DSON(low)})] - I_{OUT\_MAX} \bullet (r_{DSON(low)} + R_{DCR})$

6.5 Buck Feedback Compensation Design

The ISL70005SEH and ISL73005SEH buck regulators use voltage mode control for output voltage regulation. Due to the double pole roll off in gain and phase shift at the LC output filter resonant frequency, in voltage mode control a Type III compensator is required to stabilize the feedback loop. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency with adequate Gain and Phase margin. See Figure 70 for the schematic of a Type III compensator. This feedback network is connected between the B_FB and B_COMP pin. The loop compensation design for the ISL70005SEH and ISL73005SEH is based on the guidelines in TB417 to determine the pole-zero placement of the Type III compensation.

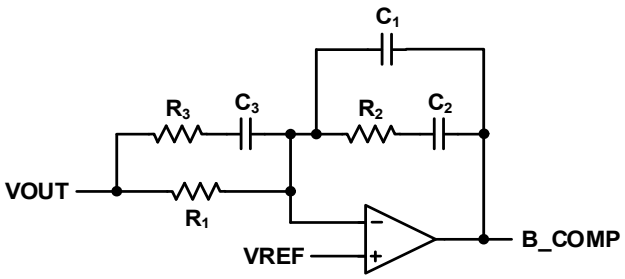


Figure 70. Type III Compensator

The following is the method of the pole-zero placement for the Type III Compensator:

1. Set the compensator loop gain such that the closed loop 0dB crossover occurs in the Type III compensator flat gain region.
2. Place one zero at 50% of the LC output filter resonant frequency F_{LC}.
3. Place one pole at the output capacitor ESR zero.
4. Place the second pole at 50% of the switching frequency f_{SW}.
5. Place the second zero at the LC output filter frequency.

(EQ. 17) $$R_2 = \frac{DBW}{F_{LC}} \cdot \frac{\Delta V_{OSC}}{V_{IN}} \cdot R_1$$

where DBW is the desired bandwidth and $\Delta V_{OSC}/V_{IN}$ = 1/2.35 = 0.425V/V

$F_{LC} = \frac{1}{(2 \cdot \pi \cdot \sqrt{LoC_{OUT}})}$ output filter resonant frequency

(EQ. 18) $$C_2 = \frac{1}{\pi \cdot R_2 \cdot F_{LC}}$$

(EQ. 19) $$C_1 = \frac{C_2}{2 \cdot \pi \cdot R_2 \cdot C_2 \cdot F_{ESR} - 1}$$

where $F_{ESR} = \frac{1}{(2 \cdot \pi \cdot ESR \cdot C_{OUT})}$

(EQ. 20) $$R_3 = \frac{R_1}{\frac{f_{SW}}{2 \cdot F_{LC}} - 1}$$

(EQ. 21) $$C_3 = \frac{1}{\pi \cdot R_3 \cdot f_{SW}}$$

Type III compensator design example for the ISL70005SEH using the Lo and C_{OUT} component values from the ISL70005SEHEV2Z evaluation board:

Note: The ISL70005SEHEV2Z evaluation board Type III loop compensation design is based on a different approach. While satisfactory for loop stability, Renesas does not recommend that approach for loop compensation design. Therefore, the loop compensation values calculated in this section will be different than the values seen on ISL70005SEHEV2Z.

1. The ISL70005SEHEV2Z buck regulator is set to operate at f_{SW} = 1MHz with a 45.3kΩ resistor on the B_RT pin. The output inductor Lo = 2.2µH used is a Coilcraft XFL4020 with DCR = 21mΩ. The bulk output capacitor C_{OUT} = 150µF used is an AVX TPM Series 16V tantalum with ESR = 30mΩ. The ceramic capacitors with much lower ESR used are only a small fraction of the bulk capacitance and can be ignored. The modulator gain of the ISL70005SEH is a fixed constant at 2.35V/V.
2. The R_1 value is set to 24.9kΩ.
3. Desired closed loop bandwidth: DBW = 30kHz.
4. Output filter resonant frequency: F_{LC} = 8.7kHz.
5. ESR zero of output capacitor: F_{ESR} = 35.4kHz.
6. Calculate the R and C values of the Type III compensator using Equation 17 through Equation 21.
   a. R_2 = 30,000/8,700 • 0.425 • 24,900 = 36.5kΩ; Use 36.5kΩ standard value
   b. C_2 = 1/(π • 36,500 • 8,700) = 1.0nF; Use 1nF standard value
   c. C_1 = 1.0E-9 / (2 • π • 36,500 • 1.0E-9 • 35,400-1) = 140pF; Use 150pF standard value
   d. R_3 = 24,900 / [1E6/(2 • 8,700) - 1] = 441Ω; Use 442Ω standard value
   e. C_3 = 1/(π • 442 • 1E6) = 720pF; Use 680pF standard value

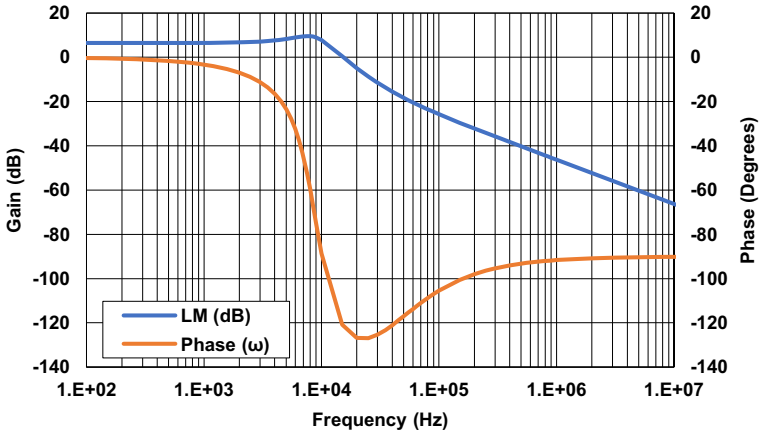


Figure 71. Modulator + LC Filter Bode Plot

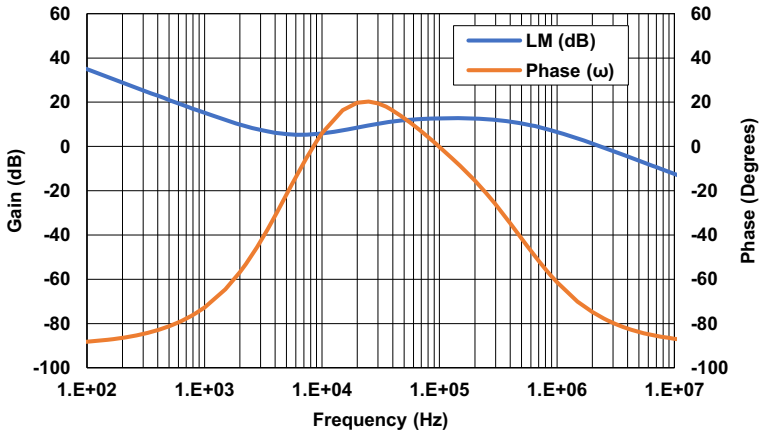


Figure 72. Type III Compensation Bode Plot

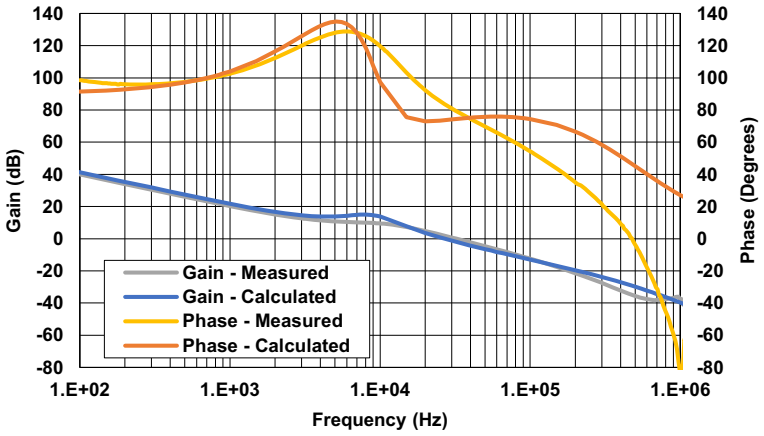


Figure 73. ISL70005SEH Buck Bode - Calculated vs Measured

7. LDO Design Guide

7.1 LDO Input and Output Capacitor Selection

The recommended bulk output capacitor is a 150µF low ESR tantalum capacitor. The capacitor used for the ISL70005SEHEV2Z evaluation platform is an AVX TPM series 150µF 16V tantalum with 30mΩ ESR. A low ESR high frequency 10µF ceramic capacitor must be placed close to the L_OUT and L_PGND pins for LDO stability. See "Example PCB Layout" on page 40 for recommended placement of the 10µF capacitor. There is no minimal requirement for input capacitance; however, it must be sized appropriately to avoid reaching dropout voltage and meet transient requirements during load step. For example, the ISL70005SEHEV2Z uses the same tantalum capacitor for bulk input and output capacitance.

7.2 LDO Output Voltage Setting

The LDO output voltage is set by two feedback resistors connected from the L_OUT to L_EA- and L_EA- to L_GND. See Equation 22 for setting the LDO output voltage.

$$\text{L\_OUT} = \text{L\_EA+} \bullet \left(\frac{R_F}{R_G} + 1 \right) \quad \text{(EQ. 22)}$$

R_F is from L_VOUT to L_EA- and R_G is from L_EA- to L_GND. L_EA+ is the non-inverting input reference voltage. The VREF pin can be connected to L_EA+ for a 600mV 1.5% accurate reference voltage. For unity gain applications, connect L_OUT directly to L_EA- to set L_OUT = L_EA+.

When the LDO is used for sourcing current only applications, careful consideration must be taken in setting the L_OUT voltage. The dead-band voltage discussed in "LDO Architecture" on page 28 introduces an offset to Equation 22 that must be nulled out. For example, if L_EA+ = VREF = 0.6V and L_OUT is targeted for 1.2V, the dead-band voltage is -10mV, which means when sourcing current, the LDO output voltage is 10mV below the target regulation voltage. Set L_OUT = 1.2V + 10mV = 1.21V for Equation 22 to achieve the targeted L_OUT = 1.2V.

8. PCB Layout Guidelines

8.1 Buck Regulator PCB Layout

PCB design is critical to high frequency switching regulator performance. Careful component placement and trace routing are necessary to reduce switching voltage spikes and minimize undesirable voltage drops. Optimize regulator performance by reducing noise from the power ground into the analog ground by avoiding high-current ground returns near sensitive analog ground. Bypass or ground pins accordingly to their respective IC ground pin. See the "Pin Descriptions" on page 7 and Figure 5 on page 5 as guidance.

Place critical components as close as possible to the IC to minimize stray inductance and resistance. Place the high-frequency ceramic decoupling capacitors for the Buck input near the B_VIN1/B_VIN2 and B_PGND1/B_PGND2 pins as they provide the instantaneous switching input currents to the Buck Regulator. Keep the connection between the B_LX1 and B_LX2 pins to the output inductor short and direct to avoid creating a large switching plane on the PCB. Void the copper on adjacent layers where the switching node is formed, to eliminate parasitic capacitance on the switching node, which impacts efficiency and causes switching spikes. To minimize output ripple voltage, place the ceramic and tantalum output capacitors near the output inductor to form a minimal ground loop return back to the B_PGND1/B_PGND2 pins. Place the output voltage feedback resistor divider as close as possible to the B_FB pin of the IC. Connect the top leg of the divider to the Buck output voltage with a Kelvin trace near the point of load to optimize load regulation performance. Connect the bottom leg of the divider directly to the B_GND1 and B_GND2 pins. Place the Type III compensation network close to the B_COMP and B_FB pins. Place the soft-start capacitor on the B_SS pin and the oscillator setting resistor on the B_RT pin close to the Buck regulator. Terminate the soft-start capacitor and timing resistor near the B_GND1 and B_GND2 pins.

For applications where the switching node voltage spikes overshoot B_VINx or undershoot B_PGNDx near the absolute maximum rating, a Schottky clamp diode across the B_LXx to B_PGNDx pins and across the B_VINx to B_LXx pins may be needed to help suppress the switching transient to protect the power MOSFETs of the Buck regulator.

8.2 LDO Regulator PCB Layout

Place the LDO input and output capacitors close to the L_VIN, L_OUT, and L_PGND connections. For the LDO output capacitors, Renesas recommends placing the 10µF ceramic capacitor closest to the L_OUT and P_GND pins to maintain LDO stability. Similar to the Buck regulator, place the LDO feedback voltage resistor dividers near the L_EA- and L_GND pins. Connect the L_OUT connection to the feedback divider with a Kelvin trace near the point of load for optimum load regulation performance. Place the LDO soft-start capacitor near the L_SS and L_GND pins.

8.3 Example PCB Layout

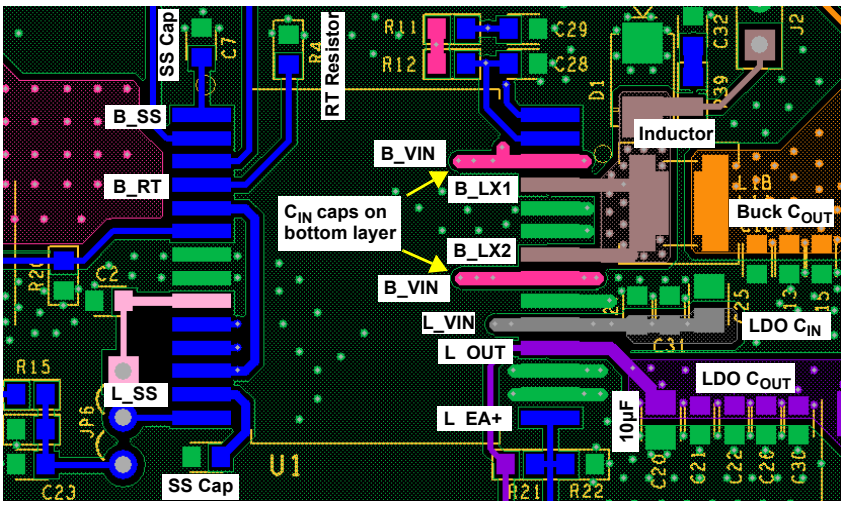


Figure 74. Top Layer PCB

9. Die and Assembly Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	6,504µm x 8,436µm (256 mils x 332 mils) Thickness: 304.8µm ± 25µm (12 mils ± 1 mil)
Interface Materials	
Glassivation	Type: Silicon Dioxide and silicon nitride Thickness: 0.3µm ± 0.03µm and 1.2µm ± 0.12µm
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 2.7µm ± 0.4µm
Backside Finish	Silicon
Process	0.6µm BiCMOS, junction isolated
Assembly Information	
Substrate and Package Lid Potential	Internal connection to B_GND1 and B_GND2
Additional Information	
Worst Case Current Density	$<2 \times 10^5$ A/cm^2
Transistor Count	7,317
Weight of Packaged Device	2.15 grams (typical) - K28.A package
Lid Characteristics	Finish: Gold Lid Potential: Internal connection to B_GND1 and B_GND2

10. Metalization Mask Layout

Table 2. Layout X-Y Coordinates (Centroid of bond pad)

Pad Name	Pad Number	X Coordinate (µm)	Y Coordinate (µm)	Pad X Dimension (µm)	Pad Y Dimension (µm)	Bond Wire Diameter (0.001”)
L_EN	1	0	0	125	125	1.5
B_EN	2	0	776	125	125	1.5
VREF	3	0	1,628	125	125	1.5
B_GND2	4	0	2,528	125	320	1.5
B_GND1	5	0	3,530	125	320	1.5
B_SYNC	6	0	4,621	125	125	1.5
B_VCC	7	0	5,364	125	320	1.5

Table 2. Layout X-Y Coordinates (Centroid of bond pad) (Continued)

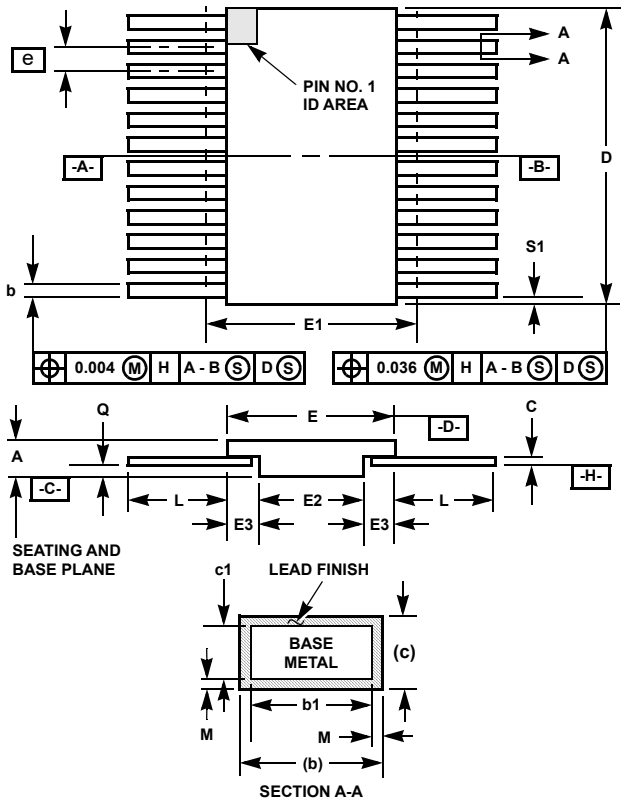
Pad Name	Pad Number	X Coordinate (µm)	Y Coordinate (µm)	Pad X Dimension (µm)	Pad Y Dimension (µm)	Bond Wire Diameter (0.001”)
B_RT	8	0	6,268	125	125	1.5
B_COMP	9	425	6,956	125	125	1.5
B_FB	10	1,106	6,956	125	125	1.5
B_SS	11	1,931	6,956	125	125	1.5
L_PG	12	2,644	6,956	125	125	1.5
B_PG	13	3,183	6,956	125	125	1.5
B_VIN2	14	5,057	6,935	508	254	3
B_LX2	15	5,238	6,016	508	254	3
B_PGND	16	5,242	4,831	254	894	3
B_LX1	17	5,238	3,646	508	254	3
B_VIN1	18	5,238	2,727	508	254	3
TEST	19	5,744	1,862	125	125	1.5
L_VIN	20	5,254	957	260	254	3
L_VIN	21	4,001	593	260	254	3
L_OUT	22	5,257	81	254	254	3
L_OUT	23	4,024	-283	254	254	3
L_PGND	24	4,820	-720	125	125	3
L_PGND	25	5,040	-720	125	125	3
L_PGND	26	5,260	-720	125	125	3
L_GND	27	2,986	-720	125	125	1.5
L_GND	28	3,334	-720	125	125	1.5
L_GND	29	3,685	-720	125	125	1.5
L_EA-	30	2,417	-720	125	125	1.5
L_EA+	31	1,838	-720	125	125	1.5
L_SS	32	1,249	-720	125	125	1.5
L_VCC	33	519	-720	320	125	1.5
L_VCC	34	921	-720	125	125	1.5

11. Revision History

Revision	Date	Description
1.04	Dec 14, 2023	Updated Title Updated Features bullets. Updated Figures 1, 2, and 4. Added Figure 43. Updated the LDO Tracking Buck for DDR Memory Application setion.
1.03	Jul 28, 2022	Removed Related Literature section. Updated Equation 16.
1.02	Feb 25, 2020	Updated Figures 3, 4, 26, 27. Replaced Figures 22, 23, 24, 25, 66, 67. Updated section 6.5 Buck Feedback Compensation Design, and replaced Figures 70, 71, and 72.
1.01	Jan 8, 2020	Fixed UVLO pin association from B_VCC to L_VCC in electrical spec table. Moved to appropriate section. Updated Power Supply Biasing section on page 31. Updated the B_COMP output voltage range in the Buck Error Amplifier Output section on page 27.
1.00	Dec 11, 2019	initial release

12. Package Outline Drawing

For the most recent package outline drawing, see K28.A.



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 lead ceramic metal seal flatpack package

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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