ISL70100M

Radiation Tolerant 40V Current Sense Amplifier

Description

The ISL70100M is a radiation tolerant 40V current sense amplifier built on the Renesas proprietary PR40 SOI process. The device has a wide power supply range of 2.7V to 40V. The input common-mode voltage is independent of the supply voltage and extends from -0.3V to 40.0V, making it ideal to use in both high-side and low-side applications.

The ISL70100M is a trans-conductance amplifier that monitors current using an external sense resistor and output a current proportional to the sensed voltage. The overall voltage gain is adjustable with a single resistor from the output to ground.

The amplifier has an extremely low offset voltage and input bias currents, making it ideal for precision sensing applications. It has a minimum bandwidth of 500kHz with a slew rate of 500µA/µs that make it useful for current feedback in telemetry applications. When the part is powered down (V+ = V- = 0V), the sense pins (RS+, RS-) are high impedance to avoid loading the monitored circuit.

The part is available in a plastic 14Ld TSSOP package. It operates across the temperature range of -55°C to +125°C.

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Power supply range: 2.7V to 40V
- Input common-mode range: -0.3V to 40V
- Transconductance: 2µA/mV (typical)
  - ±1% accuracy (T_A = 25°C)
  - ±1.5% accuracy (T_A = -55°C, 125°C)
- Voltage offset: 10µV (typical), V+ = 12V
- Adjustable gain with a single resistor
- Operating temperature range: -55°C to +125°C
- Passes NASA low outgassing specifications
- 14 Ld TSSOP with NiPdAu-Ag lead finish
- TID Radiation Lot Acceptance Testing (RLAT) (LDR: ≤ 10mrad(Si)/s)
  - ISL70100M30VZ: 30krad(Si)
  - ISL70100M50VZ: 50krad(Si)
- SEE Characterization
  - No DSEE with RS+ = 42V and V+ = 42V at 43MeV•cm^2/mg

Applications

- High-side or low-side current sensing
- Battery monitoring
- Power management
- Motor control
- Command, telemetry, and control systems

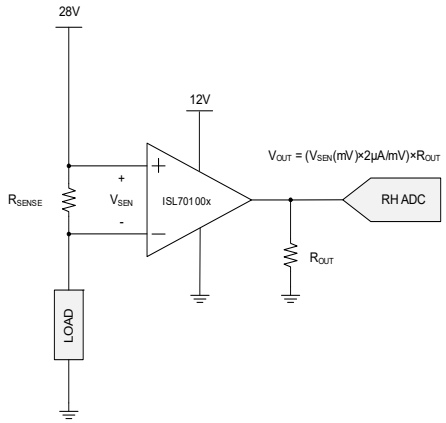

Figure 1. Typical Application: High-Side Current Sense for 28V Supply Rail

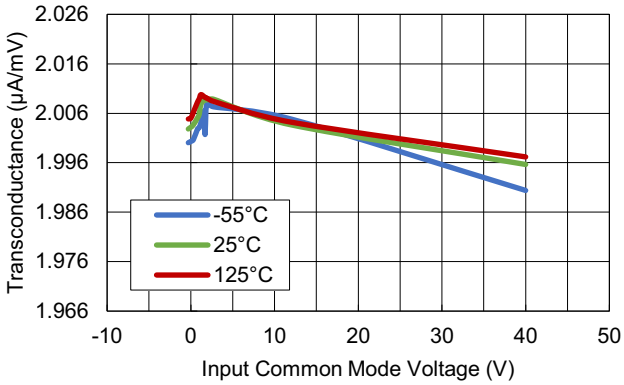

Figure 2. Transconductance, V+ = 12V

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1.1 Block Diagram

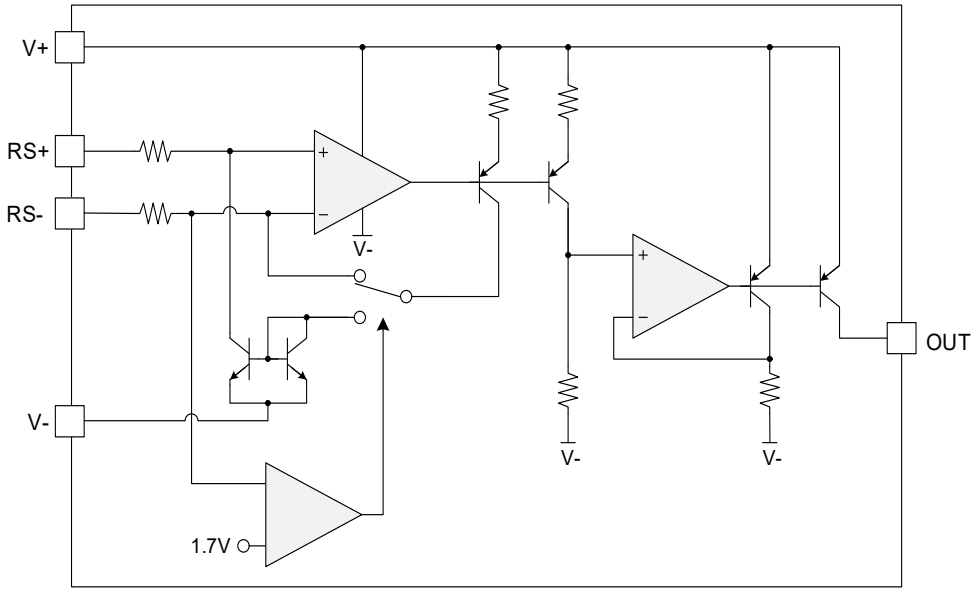


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

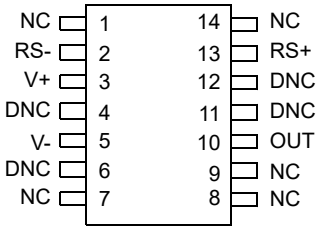
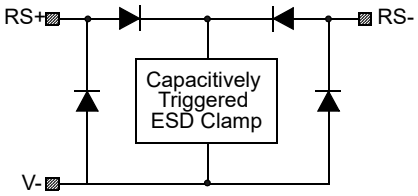


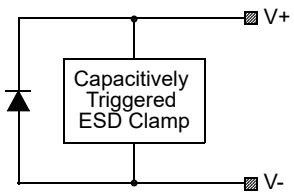
Figure 4. Pin Assignments - Top View

2.2 Pin Descriptions

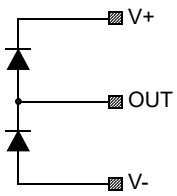
Pin Number	Pin Name	ESD Circuit	Description
1	NC	-	No Connect (Not bonded out)
2	RS-	1	Negative sense input of current sense amplifier
3	V+	2	Positive power supply
4	DNC	-	Do not connect, leave floating. This pin leaks to V-.
5	V-	-	Negative power supply
6	DNC	-	Do not connect, leave floating. This pin leaks to V-.
7	NC	-	No Connect (Not bonded out)
8	NC	-	No Connect (Not bonded out)
9	NC	-	No Connect (Not bonded out)
10	OUT	3	Output of the transconductance amplifier
11	DNC	-	Do not connect, leave floating. This pin leaks to V-.
12	DNC	-	Do not connect, leave floating. This pin leaks to V-.
13	RS+	1	Positive sense input of current sense amplifier
14	NC	-	No Connect (Not bonded out)



Circuit 1



Circuit 2



Circuit 3

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V+ to V-	-	42	V
Input Common Mode Voltage Range (VRS+, VRS-)	-0.3	42	V
Maximum Input Voltage Differential (RS+ to RS-)	-42	42	V
Maximum Differential Input Current	-	4	mA
Maximum Power Supply Ramp Rate	-	10	V/µs
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015)	-	4	kV
Charged Device Model (Tested per JS-002-2022)	-	2	kV
Latch-Up (Tested per JESD78E; Class 2, Level A), at +125°C	-	100	mA

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
V+ to V-	2.7	40	V
Input Common-Mode Voltage Range (from V-)	-0.3	40	V
Input Voltage Differential (RS+ to RS-)	0	150	mV
Temperature	-55	+125	°C

3.3 Outgas Testing

Specification (Tested per ASTM E 595, 1.5)	Value	Unit
Total Mass Lost[1]	0.06	%
Collected Volatile Condensible Material[1]	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of Total Mass Lost <1% and Collected Volatile Condensible Material of <0.1%.

3.4 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	14 Ld TSSOP Package	θ_{JA}[1]	Junction to ambient	92	°C/W
		θ_{JC}[2]	Junction to case	22	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board. See TB379 for details.
2. For θ_{JC}, the case temperature location is taken at the package top center.

3.5 Electrical Specifications

3.5.1 V+ = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ).**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.966	-	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.976	1.997	2.016	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.009	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.009	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-700	-	700	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-400	-20	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-400	10	400	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-800	-	700	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-400	-50	400	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	12	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV	**-1**	-	**1**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 12V	**-0.8**	-	**0.8**	µA

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	**-**	-	**20**	mV
Maximum Output Voltage	V_{OH}	A_V = 100, V_{SEN} = 120mV	**10.0**	10.7	**11.4**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**10**	-	**-**	V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Short-Circuit Current	-	V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1550	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1000	1250	1800	µA
Power Supply Specifications						
Power Supply Range	V+	Assured by PSRR Test	**2.7**	-	**40**	V
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	-	250	**400**	µA
Power Supply Rejection Ratio	PSRR	V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V	90	96	-	dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 0V, 40V, V+ = 2.7V, 40V, Post Radiation	90	95	-	dB
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	-3	-0.17	**-**	dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	-	0.8	-	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	-	0.32	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.25	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.90	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.80	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.25	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

3.5.2 V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ).**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.976	-	2.036	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.986	2.007	2.026	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.013	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.013	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-300	400	1000	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-600	-	1300	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-300	320	1000	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-300	250	900	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-700	-	1300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-300	100	900	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	11	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-8	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 2.7V	**-1**	-	**1**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB

Recommended operating conditions, V+ = V_{RS+} = 2.7V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 3.33kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	-	-	**14**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 100, V_{SEN} = 27mV	**0.7**	1.4	**2.1**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = Open	**0.7**	-	**-**	V
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω	**300**	600	**1100**	µA
Short-Circuit Current		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω	**300**	600	**1100**	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	-	240	**400**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	-3	-0.20	**-**	dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	-	0.8	**-**	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	-	0.4	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.2	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.75	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.1	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

3.5.3 V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ).**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Input Specifications						
Input Common-Mode Voltage Range	V_{CM}	Assured by CMRR Test	**-0.3**	-	**40**	V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Transconductance	g_m	V_{SEN} = 25mV to 150mV, V_{RS+} = V+ T_A = +25°C	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = -55°C, +125°C	1.960	-	2.020	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = V+, T_A = +25°C, Post Radiation	1.970	1.988	2.010	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V T_A = +25°C	1.940	2.011	2.060	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = -55°C, +125°C	1.930	-	2.070	µA/mV
		V_{SEN} = 25mV to 150mV, V_{RS+} = 0V, T_A = +25°C, Post Radiation	1.940	2.011	2.060	µA/mV
Input Offset Voltage	V_{OS}	V_{SEN} = 5mV T_A = +25°C	-1200	-515	300	µV
		V_{SEN} = 5mV T_A = -55°C, +125°C	-1500	-	600	µV
		V_{SEN} = 5mV T_A = +25°C, Post Radiation	-1200	-650	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C	-1100	-365	300	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = -55°C, +125°C	-1600	-	600	µV
		V_{SEN} = 5mV, V_{RS+} = 0V T_A = +25°C, Post Radiation	-1100	-635	300	µV
Input Bias Current	I_{BIAS}	V_{SEN} = 0mV	-	15	**25**	µA
		V_{SEN} = 0mV, V_{RS+} = 0V	**-25**	-9	**-**	µA
Input Offset Current	I_{OS}	V_{SEN} = 0mV, V_{RS+} = 0V, V+	**-1**	-	**1**	µA
Input Bias Current (Powered Off)	I_{OFF}	V+ = V_{SEN} = 0mV, V_{RS+} = 40V	**-0.8**	-	**0.8**	µA
Common-Mode Rejection Ratio	CMRR	V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = 2.7V, 40V, Post Radiation	90	103	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V	90	106	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, T_A = -55°C, +125°C	85	-	-	dB
		V_{SEN} = 5mV, V_{RS+} = -0.3V, 40V, Post Radiation	90	106	-	dB
Output Specifications						
Minimum Output Voltage	V_{OL}	V_{SEN} = 0mV	-	-	**4**	mV
Maximum Output Voltage	V_{OH}	Referred to V+, A_V = 400, V_{SEN} = 100mV	**38**	38.7	**39.4**	V
Minimum Guaranteed Linear Output Voltage	OVR	V_{SEN} = 150mV, R_L = OPEN	**38**	-	-	V

Recommended operating conditions, V+ = V_{RS+} = 40V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C unless otherwise specified. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M30VZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL70100M50VZ). (Cont.)**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Maximum Linear Output Current Range	I_{OUT}	R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Short-Circuit Current	I_{SC}	V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, T_A = -55°C, +25°C, +125°C	1200	1600	1800	µA
		V_{RS+} = 40V, V_{RS-} = 0V, R_{OUT} = 0Ω, Post Radiation	1100	1300	1800	µA
Power Supply Specifications						
Supply Current	I+	V_{SEN} = 0mV, V_{RS+} = 0V, V+	-	280	**420**	µA
AC Specifications						
500kHz Attenuation	Att_{500kHz}	V_{SEN} = 50mV, C_L = 10pF, A_V = 10, f_{TEST}=1kHz, 500kHz	**-3**	-0.21	-	dB
Settling Time	t_S	V_{SEN} = 5mV to 150mV (to 1% of final value)	-	0.8	-	µs
Input Step Response Time	t_{RES}	V_{SEN} = 5mV to 150mV 50% of input to 50% of output	-	-	**1**	µs
Slew Rate	SR	V_{SEN} = 5mV to 150mV (T_A = +25°C)	0.50	1.3	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +125°C)	0.50	1.9	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = -55°C)	0.45	0.8	2.50	mA/µs
		V_{SEN} = 5mV to 150mV (T_A = +25°C, Post Rad)	0.50	1.3	2.50	mA/µs

1. Typical values are at 25°C and are not guaranteed.

4. Typical Performance Curves

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified.

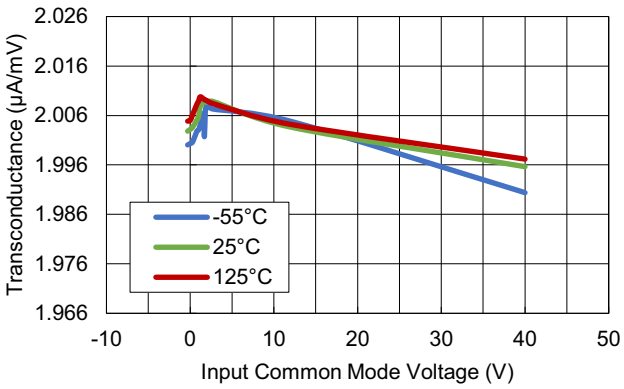


Figure 5. Transconductance, V+ = 12V

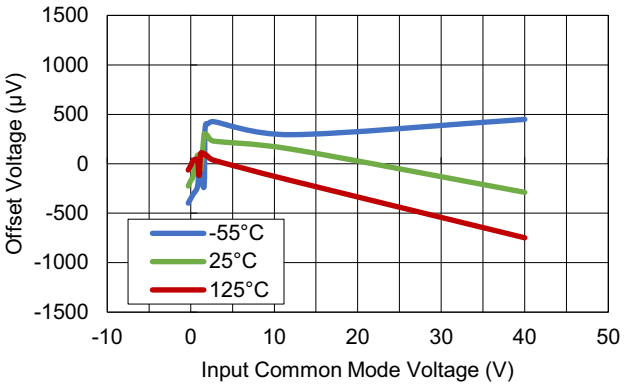


Figure 6. Common-Mode Voltage vs V_{OS}, V+ = 12V

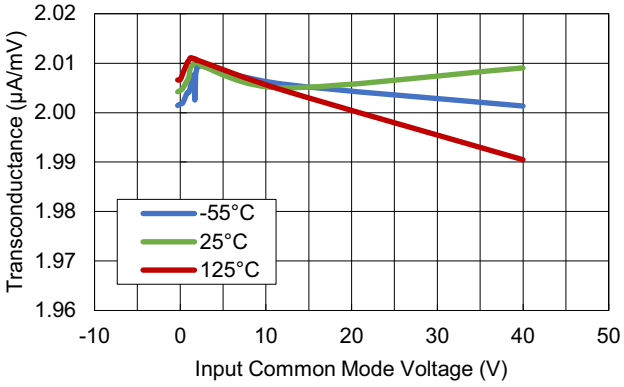


Figure 7. Transconductance, V+ = 40V

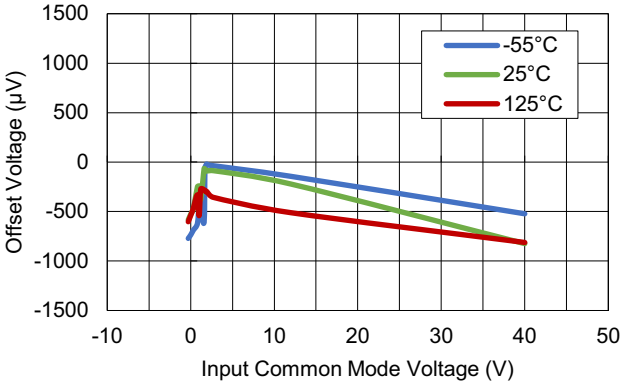


Figure 8. Common-Mode Voltage vs V_{OS}, V+ = 40V

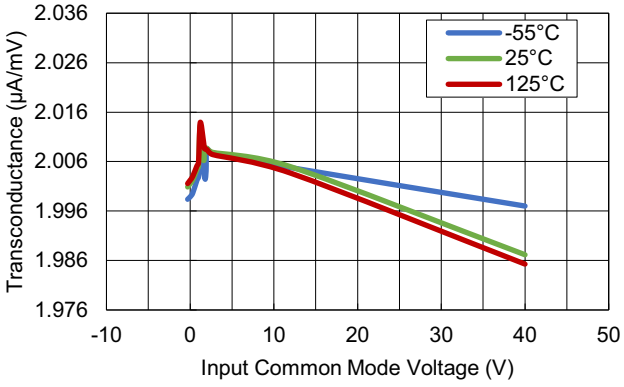


Figure 9. Transconductance, V+ = 2.7V

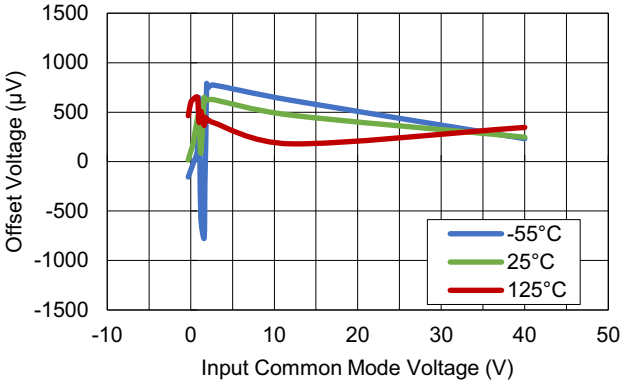


Figure 10. Common-Mode Voltage vs V_{OS}, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

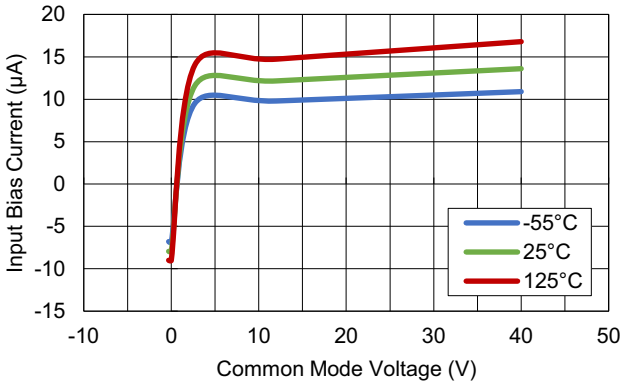


Figure 11. Input Bias Current vs VCM, V+ = 12V

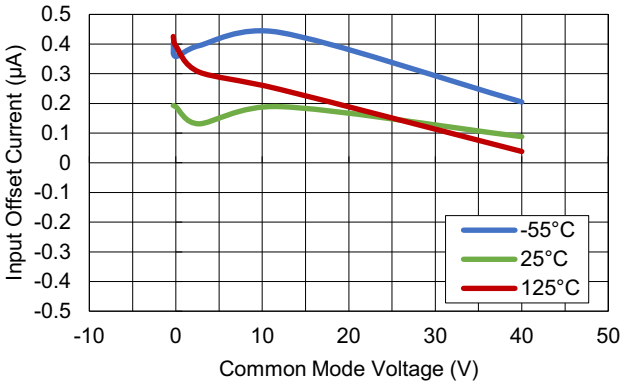


Figure 12. Input Offset Current vs VCM, V+ = 12V

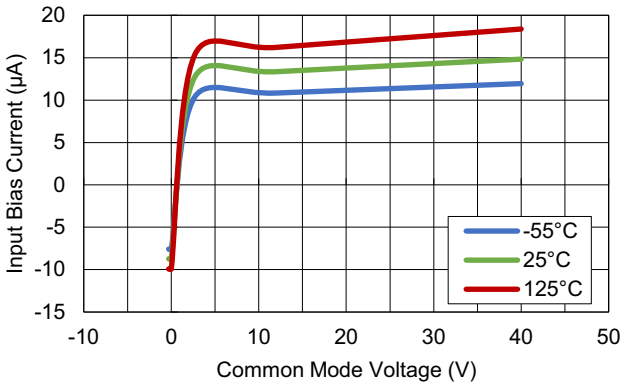


Figure 13. Input Bias Current vs VCM, V+ = 40V

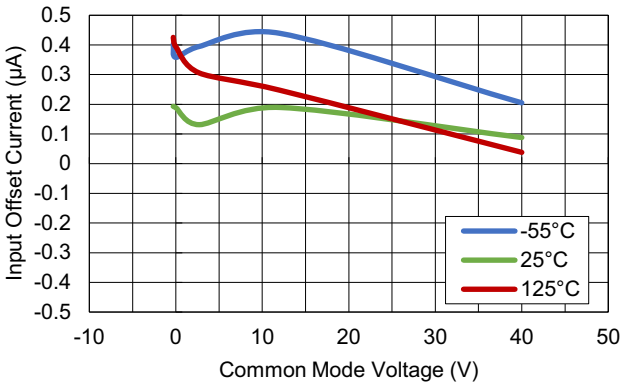


Figure 14. Input Offset Current vs VCM, V+ = 40V

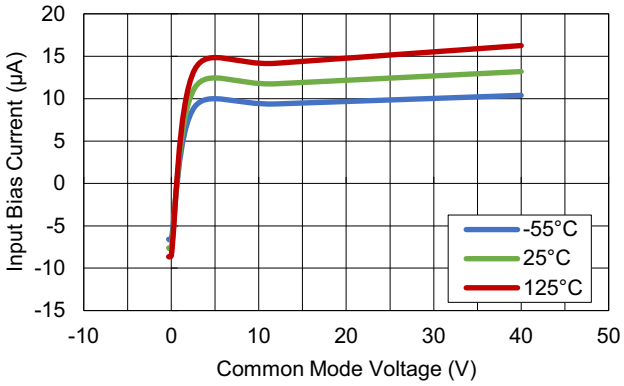


Figure 15. Input Bias Current vs VCM, V+ = 2.7V

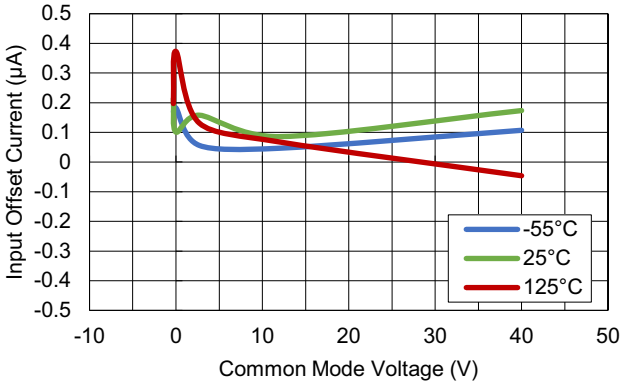


Figure 16. Input Offset Current vs VCM, V+ = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

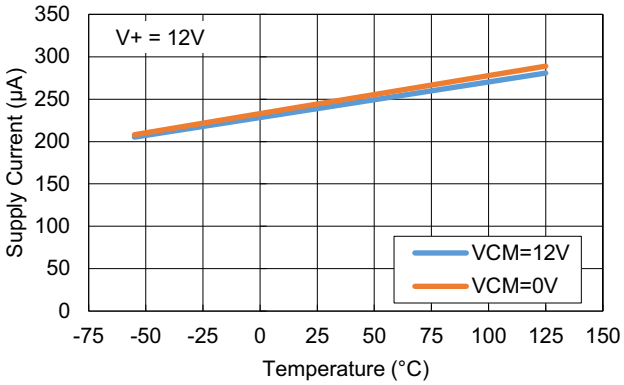


Figure 17. Supply Current, V+ = 12V

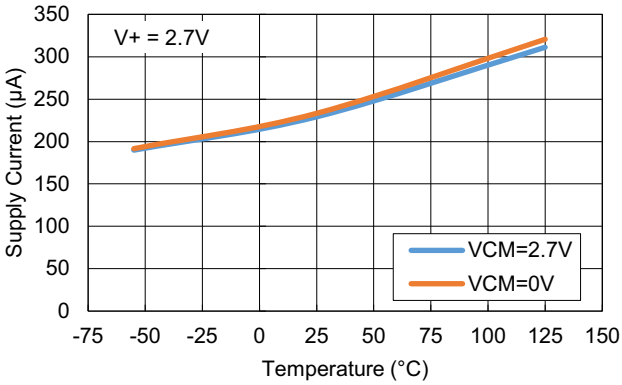


Figure 18. Supply Current, V+ = 2.7V

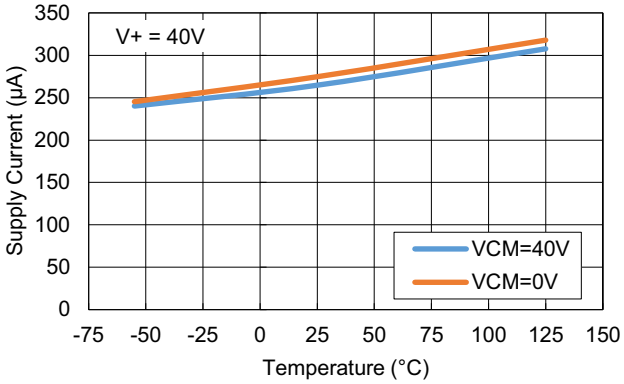


Figure 19. Supply Current, V+ = 40V

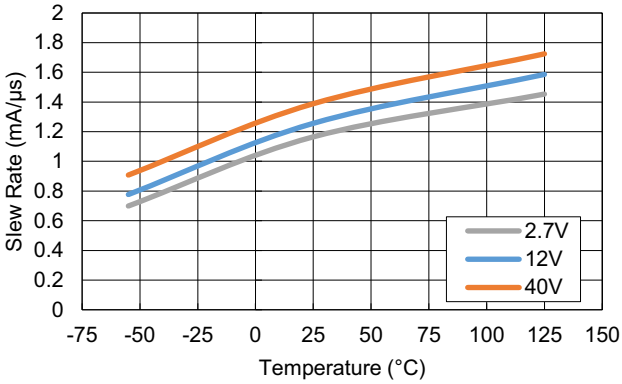


Figure 20. Slew Rate

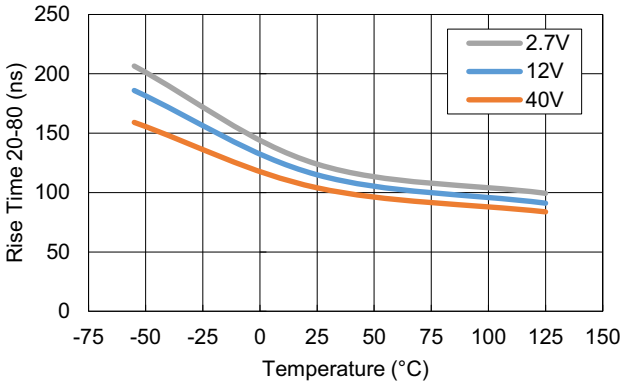


Figure 21. Rise Time

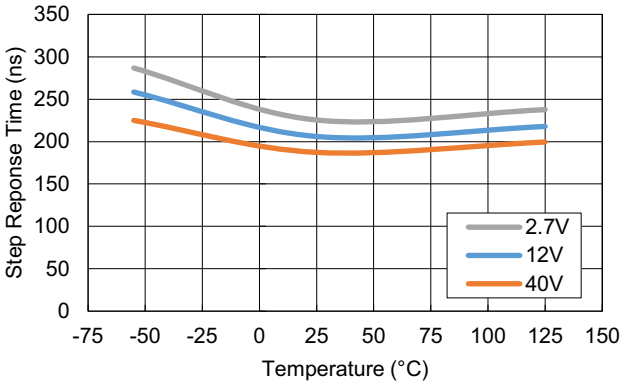


Figure 22. Step Response Time

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

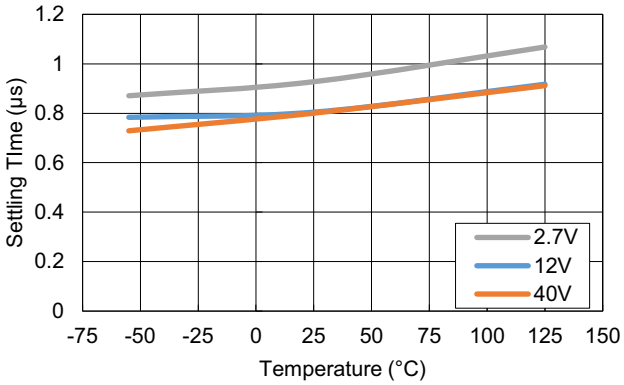


Figure 23. Settling Time

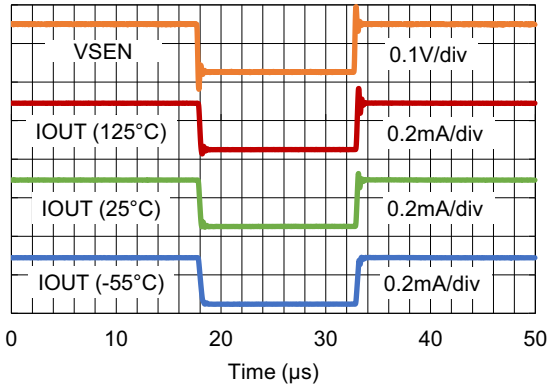


Figure 24. Input Step Response

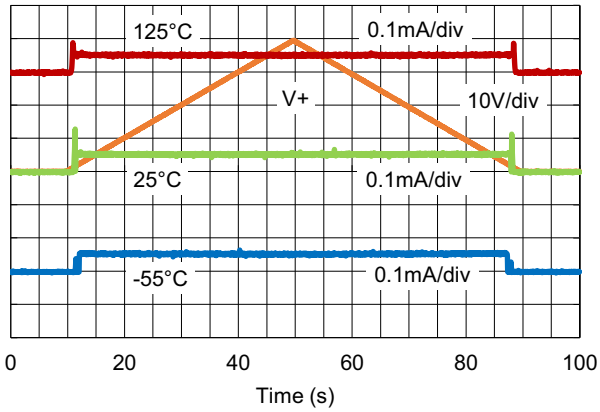


Figure 25. Power Supply Ramp at 1V/s

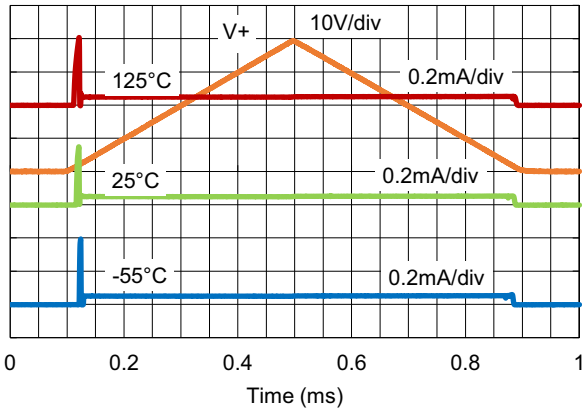


Figure 26. Power Supply Ramp at 1V/10µs

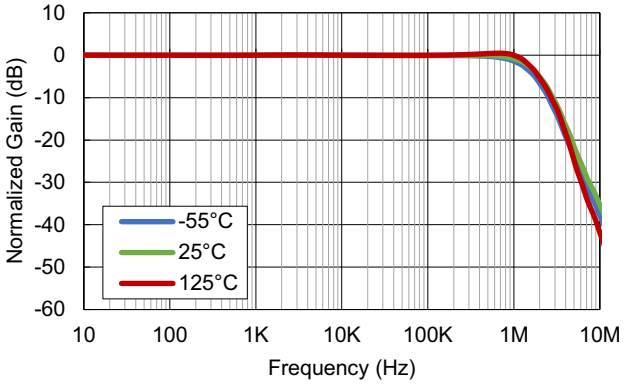


Figure 27. Normalized Gain, V+ = 12V

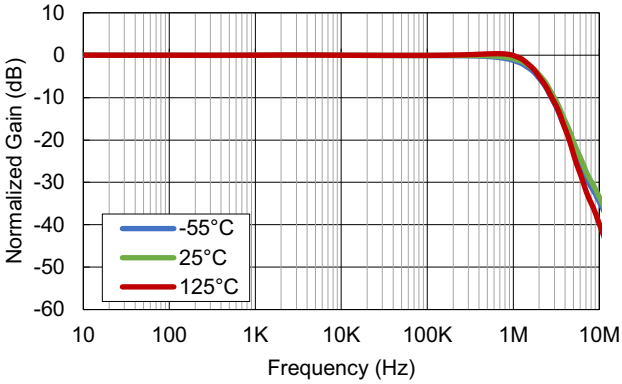


Figure 28. Normalized Gain, V+ = 40V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

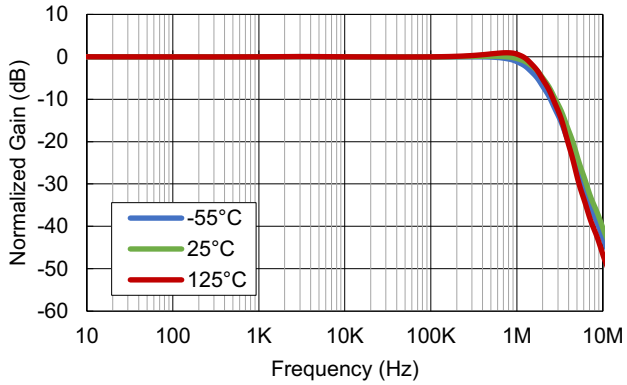


Figure 29. Normalized Gain, V+ = 2.7V

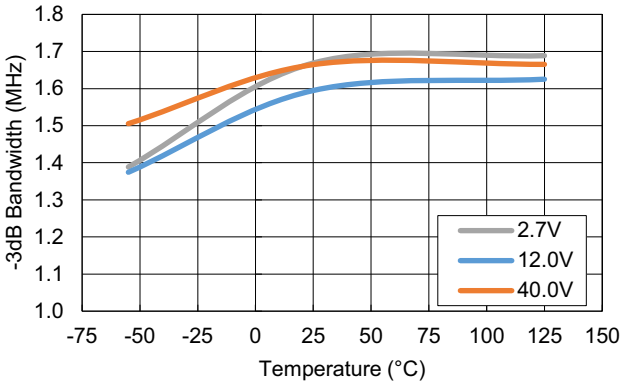


Figure 30. Bandwidth vs Temperature

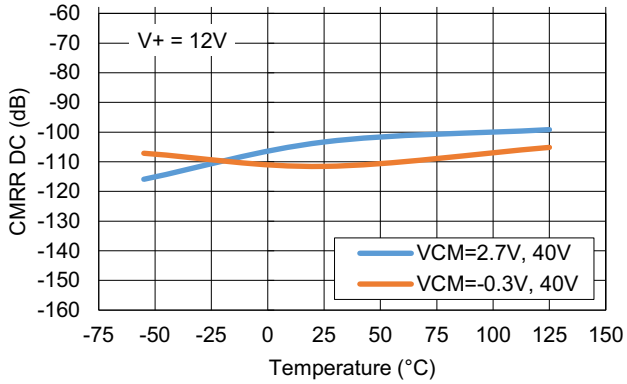


Figure 31. CMRR DC, V+ = 12V

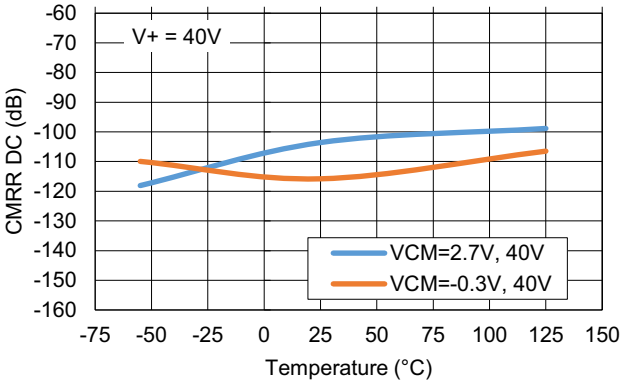


Figure 32. CMRR DC, V+ = 40V

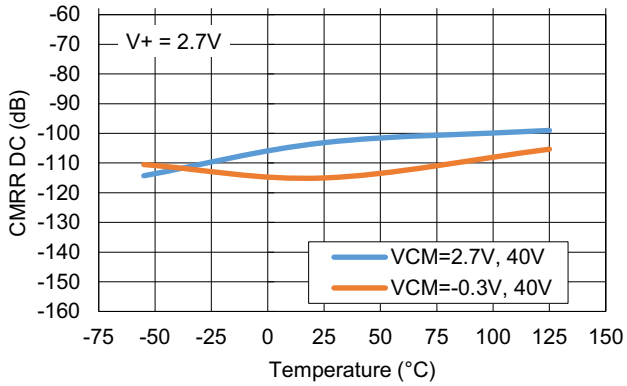


Figure 33. CMRR DC, V+ = 2.7V

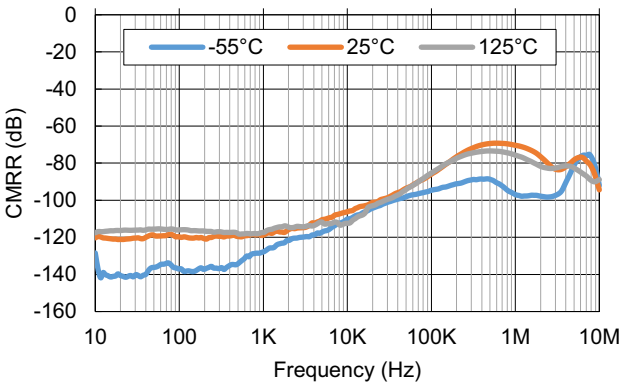


Figure 34. CMRR vs Frequency, V+ = 12V, V_{CM} = 2.7V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

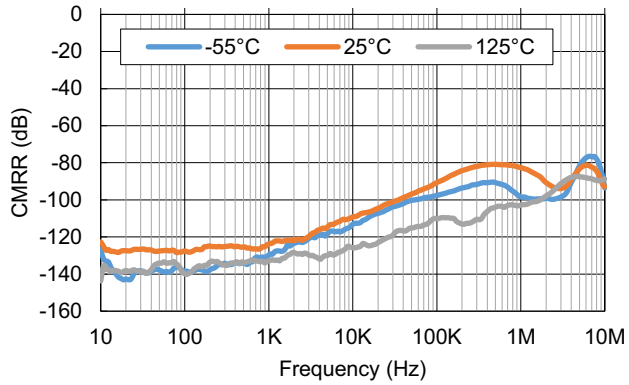


Figure 35. CMRR vs Frequency, V+ = 12V, V_{CM} = 12V

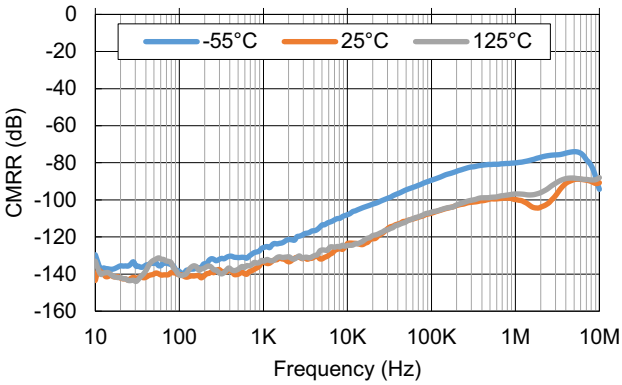


Figure 36. CMRR vs Frequency, V+ = 12V, V_{CM} = 40V

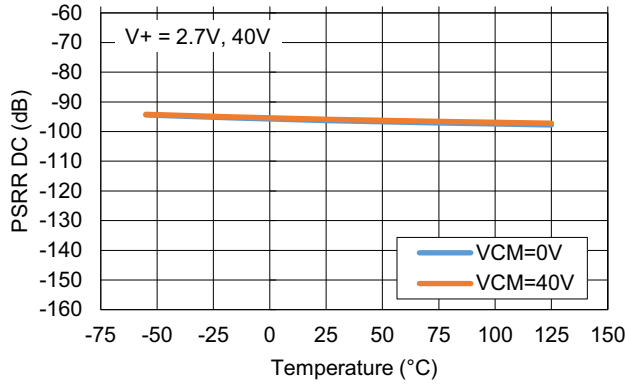


Figure 37. PSRR DC

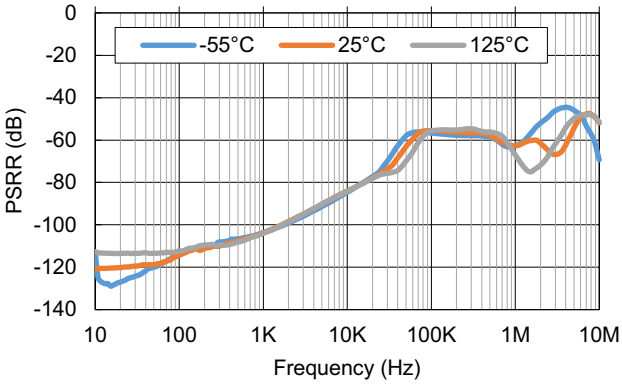


Figure 38. PSRR vs Frequency, V+ = 2.7V, V_{CM} = 12V

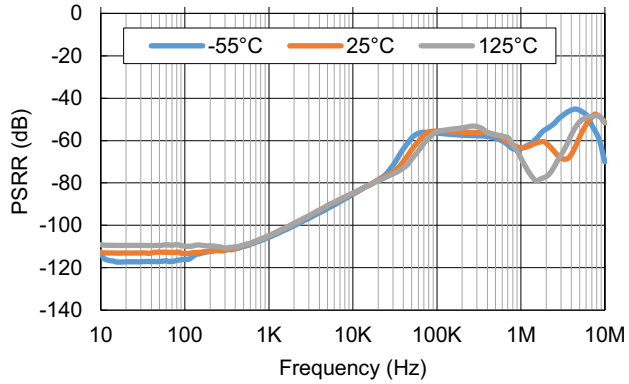


Figure 39. PSRR vs Frequency, V+ = 12V, V_{CM} = 12V

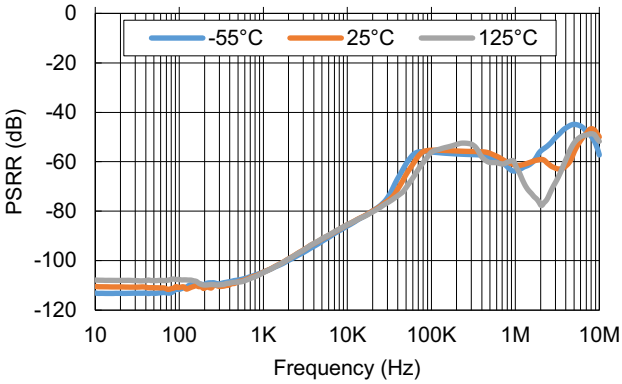


Figure 40. PSRR vs Frequency, V+ = 40V, V_{CM} = 12V

Recommended operating conditions, V+ = V_{RS+} = 12V, V- = 0V, V_{SEN} = (V_{RS+} - V_{RS-}), R_{OUT} = 25kΩ and T_A = +25°C, unless otherwise specified. (Cont.)

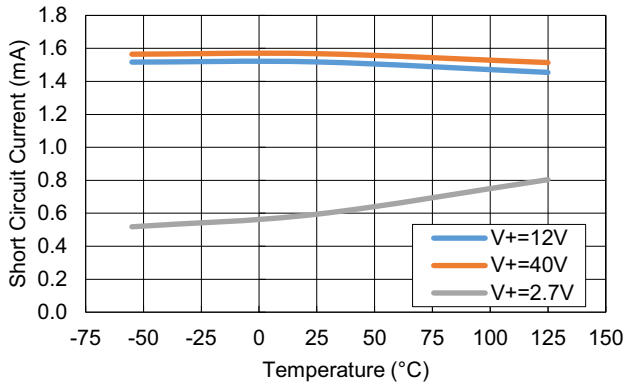


Figure 41. Short-Circuit Current

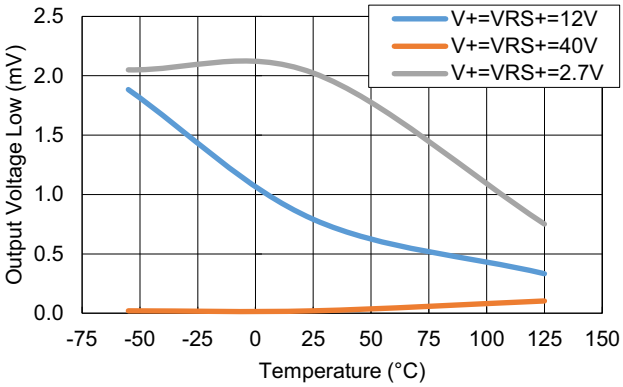


Figure 42. Output Voltage Low

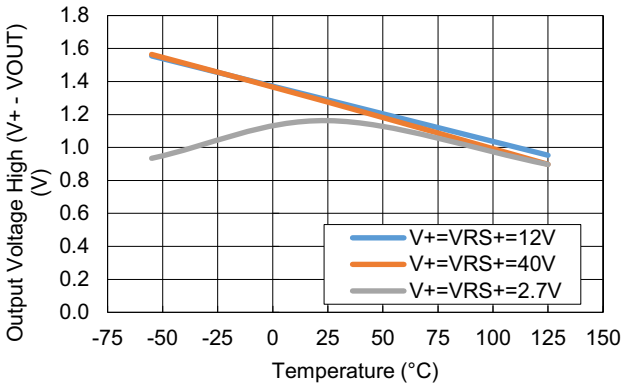


Figure 43. Output Voltage High (Referred to V+)

5. Functional Description

The ISL70100M is a transconductance current sense amplifier with a power supply range of 2.7V to 40V. Its input common-mode range extends from -0.3V to 40V, which makes it ideal for use in both low-side and high-side applications. The input common-mode voltage is independent of the power supply such that the ISL70100M can be powered by a 5V rail but sense a 40V common mode. The ISL70100M level shifts in the sensed voltage from the sensed power supply to a ground-referenced output. The output gain of the ISL70100M can be easily configured with a single resistor on the output. It outputs a current proportional to the input voltage differential and the output resistor sets the voltage gain seen by downstream devices.

The ISL70100M can be driven with bi-polar supplies with the positive voltage on V+ and the negative voltage on V-. The same voltage differentials should still be between 2.7V and 40V from V+ to V-. The output of the amplifier is referenced to V- so any downstream device must be able to handle a bipolar input.

5.1 Output Signal Range

The output range of the amplifier is limited on the low end by the input offset voltage and the saturation voltage of the output transistors on the top end. The maximum voltage is always about 2V below the voltage on V+. If the application calls for a large gain, the supply voltage may need to be increased to accommodate the full output voltage range. For example, if the supply voltage is 2.7V, the output can only get up to 0.7V before the output is saturated; this sets the maximum gain with 2.7V supply to 4.67 with a maximum sensing voltage of 150mV. If the sensing voltage range is reduced, higher gains can be used.

(EQ. 1) $$A_{CSA(MAX)} = \frac{(V+) - V_{OH}}{V_{SEN(MAX)}}$$

where:

- $A_{CSA(MAX)}$ is the maximum output gain given the maximum input differential
- V+ is the power supply voltage of the ISL7x100M in volts
- V_{OH} is output high saturation voltage referred to V+ from the electrical specifications table in volts
- $V_{SEN(MAX)}$ is the maximum input differential that the application calls for in volts

Typically, the output of the ISL70100M is connected to the input of an Analog-to-Digital Converter (ADC), which has limited input voltage ranges. Ensure that the output voltage ($I_{OUT(MAX)} \times R_{OUT}$) does not exceed the input voltage range of the downstream ADC.

5.2 Input Common-Mode Range

The input common-mode range of the ISL70100M ranges from -0.3V to 40V regardless of the voltage on V+. The electrical specifications table shows that the offset voltage of these amplifiers changes very slightly over the full common-mode range. The inputs are also capable of either RS+ or RS- dropping to 0V without damaging the amplifier, this is particularly useful in monitoring protection fuse circuits where the output goes to the positive rail if the fuse is blown. If the input differential is reversed (RS- goes above RS+), the output does not phase invert, it remains at the output low voltage specified in the electrical specifications table.

5.3 Crossover Region

The ISL70100M accomplishes the wide input common-mode range using multiple input paths that are selected based on the common-mode voltage. The transition point between the high-side and low-side is typically 1.7V but can range from 1.5V to 2.0V across temperature. When the common-mode voltage has reached the transition point, there is a soft switchover from the low-side to the high-side.

5.4 Sources of Error

5.4.1 Input Impedance of Downstream Devices

The value of the output resistance is not critical if the circuit that is being driven has a high input impedance. If the driven circuit has a low input impedance, the accuracy of V_{OUT} is reduced. Using an example where the input impedance is 100 times larger than the output resistance. It can be seen that the accuracy drops by 1%.

(EQ. 2) $$V_{OUT} = I_{OUT} \times \frac{R_{OUT} \times R_{IN}}{R_{OUT} + R_{IN}} = I_{OUT} \times \frac{100}{101} = I_{OUT} \times R_{OUT} \times 0.99$$

where:

- V_{OUT} is the output voltage in volts
- I_{OUT} is the output current in amps
- R_{OUT} is output resistance loading the output of the ISL7x100SEH in ohms
- R_{IN} is the input impedance of the downstream device in ohms

5.4.2 Input Offset Voltage

The dynamic range of the ISL70100M is inversely proportional to the input offset voltage. The dynamic range can be thought of as the maximum sense voltage divided by V_{OS}. These amplifiers have an offset voltage of 10µV typically. The electrical specification table shows how the offset voltage can vary across various operating points.

5.4.3 Input Bias and Offset Current

A typical current sense amplifier has the ability to change its transconductance by changing the input resistors. In this case, the input bias currents and offset currents can induce more error on top of the offset voltage. The ISL70100M gets around this by internalizing these input resistors and trimming out the error associated with them during production.

5.4.4 Sensed Current Error

Determine the effective current error using Equation 3. It shows the amount of current that the current-sense amplifier is blind to.

(EQ. 3) $$I_{ERROR} = \frac{V_{OS}}{R_{SENSE}}$$

where:

- V_{OS} is the offset voltage in µV.
- R_{SENSE} is the sense resistor in mΩ.
- I_{ERROR} is the current error in mA.

The R_{SENSE} can be increased to lower the current error, but this reduces the maximum current that can be sensed and increases power dissipation. Careful consideration must be made to balance power dissipation and accuracy.

6. Applications Information

6.1 Selection of the External Current-Sense Resistor

To pick the current-sense resistor value, a decision has to be made between power dissipation and measurement accuracy. As a general rule for all applications, the sense resistor should be as small as possible while still providing adequate input dynamic range across the operating range. The minimum accurately sensed input voltage is primarily limited by the offset voltage of the ISL70100M.

The sense resistor value can be calculated once the maximum sensed load current is determined. The maximum recommended sense voltage for the ISL70100M is 150mV, so dividing that by the maximum load current provides the sense resistor value.

(EQ. 4) $$R_{SENSE} = \frac{150mV}{I_{OUT(MAX)}}$$

where:

- R_{SENSE} is the sense resistor in mΩ.
- $I_{OUT(MAX)}$ is the maximum expected load current to be sensed in amps.

6.2 Gain Setting

The gain on the ISL70100M can be adjusted using a single resistor on the output. The ISL70100M outputs 2µA for every 1mV of differential across the inputs. Use Equation 5 to calculate the output load resistance to obtain a specific gain:

(EQ. 5) $$R_{OUT} = \frac{A_{CSA}}{g_m}$$

where:

- R_{OUT} is the output load resistance in kΩ.
- A_{CSA} is the required voltage gain.
- g_m is the transconductance of the ISL70100M which is 2µA/mV (typical).

6.3 Selection of Output Resistor

The output signal is a current conducted through the output resistor to generate a voltage. With a maximum input range of 150mV, the output current is 300µA. The voltage gain should be determined based on the input voltage range of the downstream device. For example, if there is a 5V ADC on the output of the ISL70100M, the output resistance should be 16.6kΩ to ensure that V_{OUT} stays under 5V. This also means that the minimum power supply voltage has to be 7V to achieve 5V on the output. Renesas recommends using resistors that have a low temperature coefficient on the output as it adds error to the measurement.

6.4 Output Filtering

Because the output of these amplifiers is a current source, filtering is straight forward. A capacitor can be placed in parallel to the output resistance to create a pole based on Equation 6:

(EQ. 6) $$f_{-3dB} = \frac{1}{2 \times \pi \times R_{OUT} \times C_{OUT}}$$

where:

- f_{-3dB} is frequency location of the pole in hertz
- R_{OUT} is the output resistance in ohms
- C_{OUT} is the output capacitance in parallel with R_{OUT} in farads

6.5 Response Time

The ISL70100M provides fast response time for circuit protection or signal transmission. The delay and speed of the response depend on the starting point of the step. If the sensed current is very low (near zero) before the transient, there may be an increased delay time to see the output react. If fast reaction times are required, increase the sense resistance such that there are a few millivolts (1-5mV) of differential across the inputs under the lowest current condition. The higher the differential is for the lowest current condition, the faster the response time is, but that results in increased DC power losses.

Figure 44 and Figure 45 show the step response difference from starting with a 0mV differential versus starting with a 25mV differential. For most applications the 40-50ns faster reaction time may not warrant the resulting power loss.

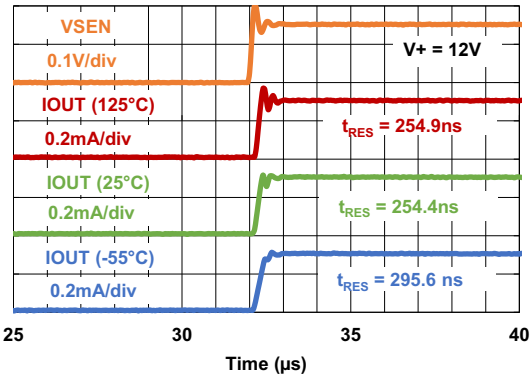


Figure 44. 0mV to 150mV Step Response

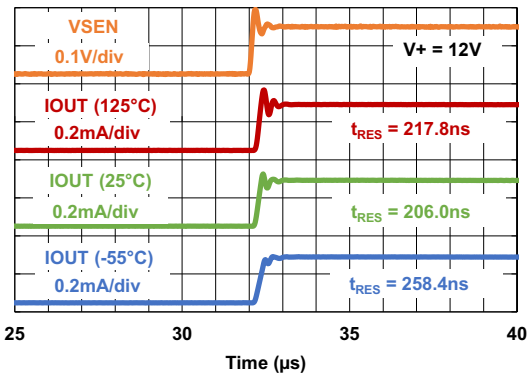


Figure 45. 25mV to 150mV Step Response

7. Radiation Tolerance

The ISL70100M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL70100MVZ is not guaranteed through radiation acceptance testing. The ISL70100M30VZ is radiation lot acceptance tested (RLAT) to 30krad(Si) and ISL70100M50VZ is RLAT to 50krad(Si). The SEE characterized performance is not guaranteed.

7.0.1 Total Ionizing Dose (TID) Testing Introduction

Total dose testing of the ISL70100M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of ten samples irradiated under bias, as shown in Table 1, and eight samples irradiated with all pins grounded (unbiased). Three control units were used. Figure 46 shows the bias configuration.

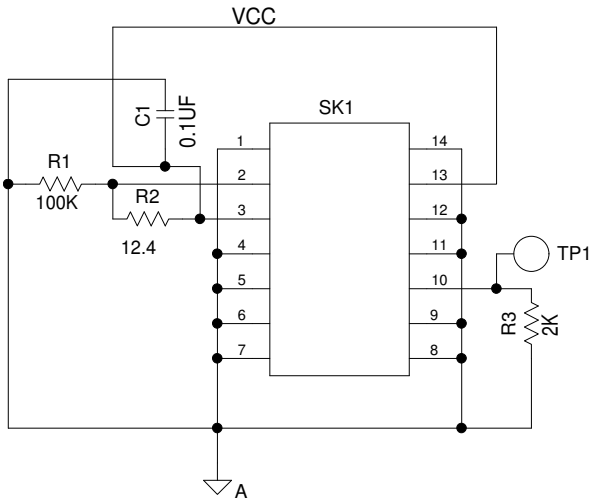


Figure 46. Irradiation Bias Configuration

Samples of the ISL70100M were drawn from wafer lots XXJ6H, XXL4L, and XXM2H, and were packaged in the production 14 lead TSSOP. The samples were screened to datasheet limits at room temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate 60Co irradiator located in the Renesas Palm Bay, Florida facility. The dose rate was 0.01rad(Si)/s (10mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Downpoints for the testing were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each downpoint. All downpoint electrical testing was performed at room temperature.

7.0.2 Results

Table 1 summarizes the attributes data. “Bin 1” indicates a device that passes all the datasheet specification limits.

Table 1. Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Downpoints	Pass	Fail
10	Figure 46	10	Pre-Rad	10	0
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
10	Grounded	8	Pre-Rad	8	0
			10krad(Si)	8	0
			30krad(Si)	8	0
			50krad(Si)	8	0

The plots in Figure 47 through Figure 62 show data for key parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions. The error bars, if visible, represent the maximum and minimum measured values. All parts showed excellent stability over irradiation and are not considered bias sensitive.

7.0.3 Typical Radiation Performance

$V+ = V_{RS+} = 12V$, $V- = 0V$, $V_{SEN} = (V_{RS+} - V_{RS-})$, $R_{OUT} = 25k\Omega$, unless otherwise specified.

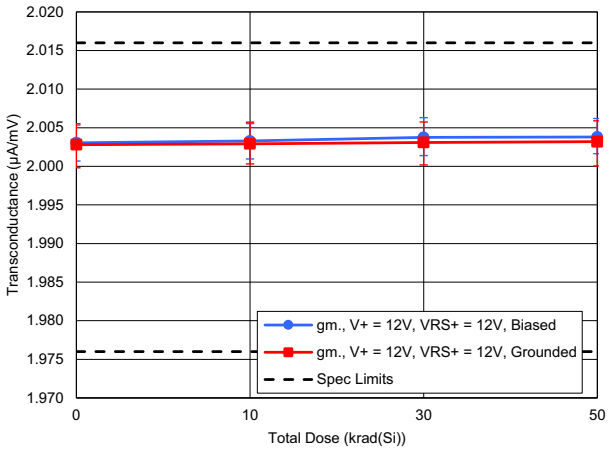


Figure 47. Transconductance vs TID

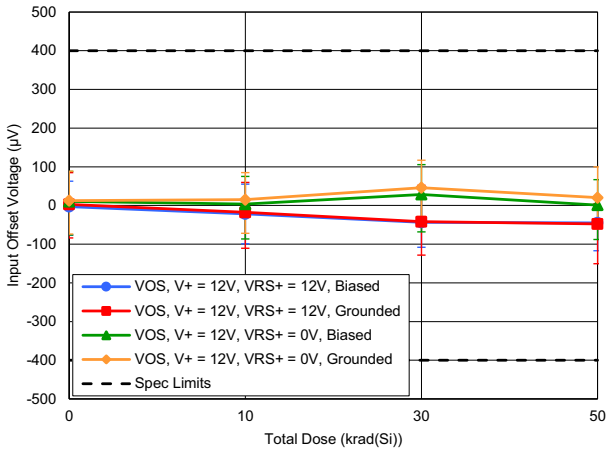


Figure 48. Input Offset Voltage vs TID

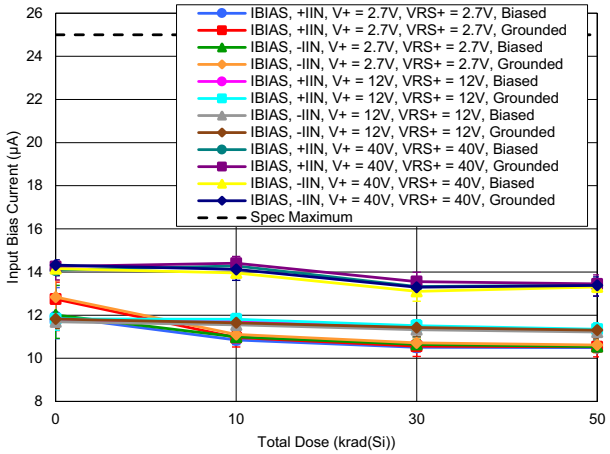


Figure 49. Input Bias Current with V_{RS+} = V+ vs TID

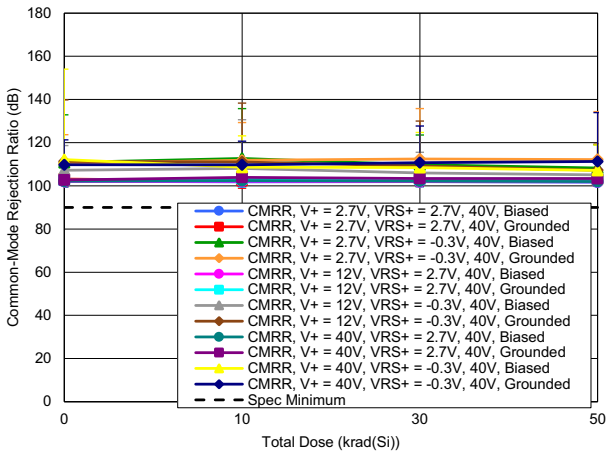


Figure 50. Common-Mode Rejection Ratio vs TID

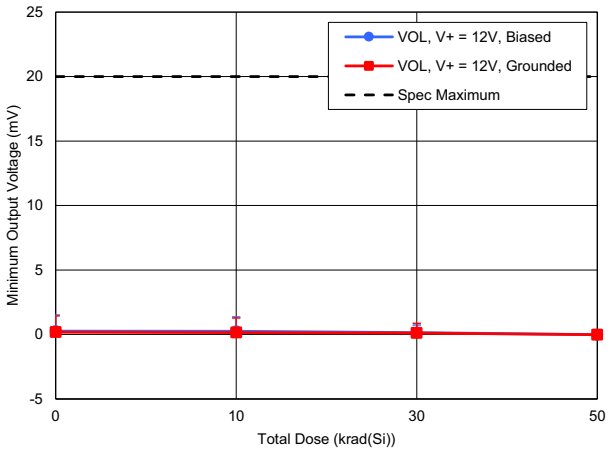


Figure 51. Minimum Output Voltage vs TID

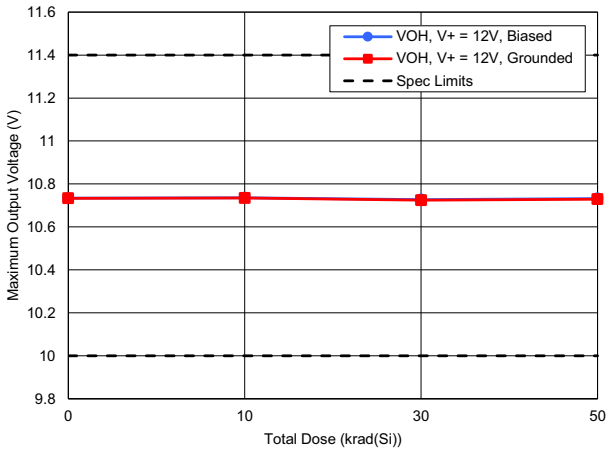


Figure 52. Maximum Output Voltage vs TID

$V+ = V_{RS+} = 12V$, $V- = 0V$, $V_{SEN} = (V_{RS+} - V_{RS-})$, $R_{OUT} = 25k\Omega$, unless otherwise specified.

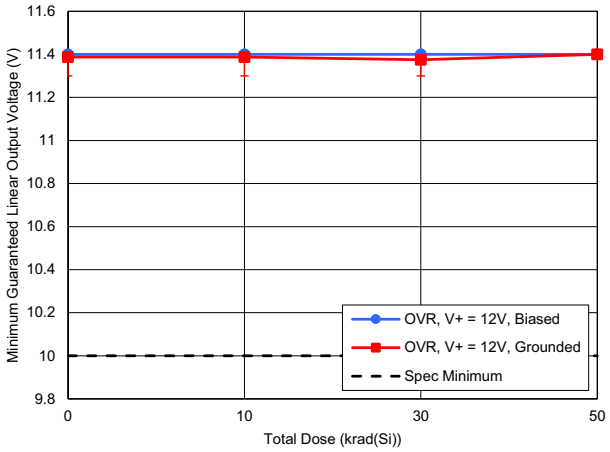


Figure 53. Minimum Guaranteed Linear Output Voltage vs TID

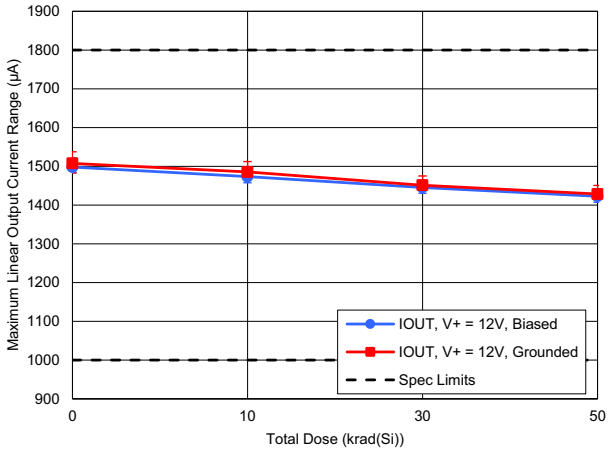


Figure 54. Maximum Linear Output Current Range vs TID

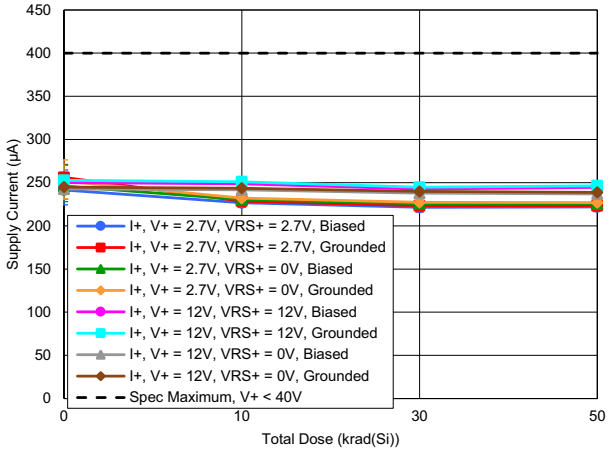


Figure 55. Supply Current vs TID

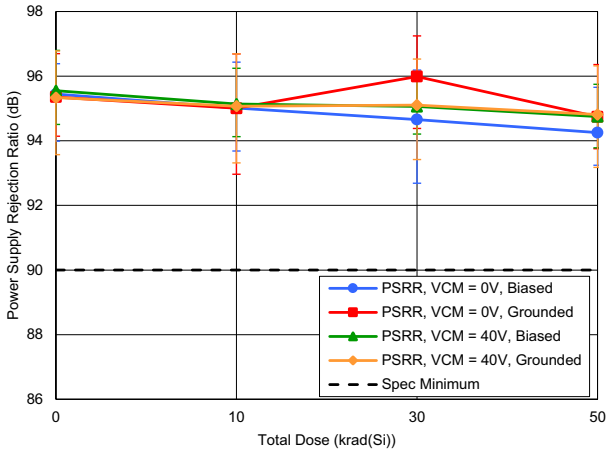


Figure 56. Power Supply Rejection Ratio vs TID

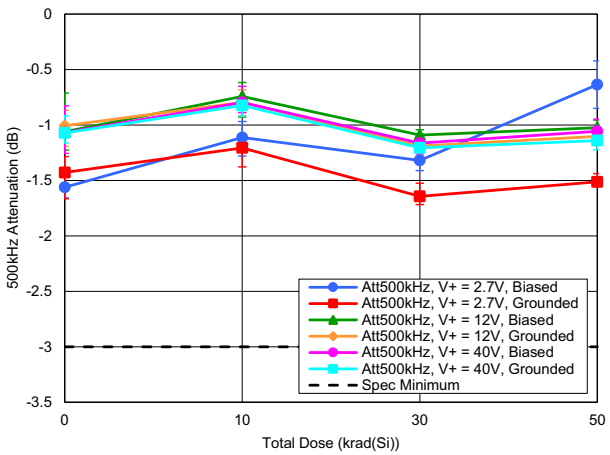


Figure 57. 500kHz Attenuation vs TID

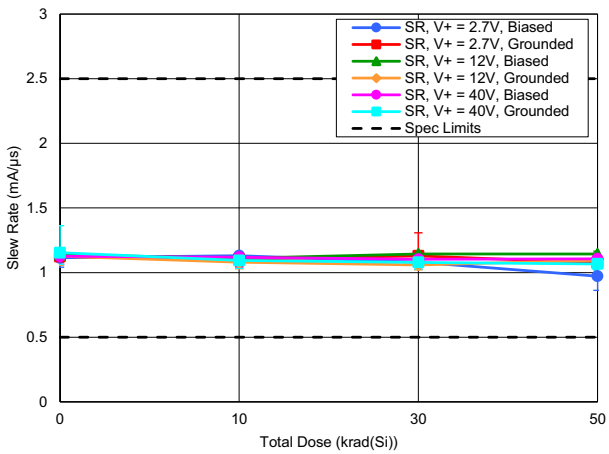


Figure 58. Slew Rate vs TID

$V+ = V_{RS+} = 12V$, $V- = 0V$, $V_{SEN} = (V_{RS+} - V_{RS-})$, $R_{OUT} = 25k\Omega$, unless otherwise specified.

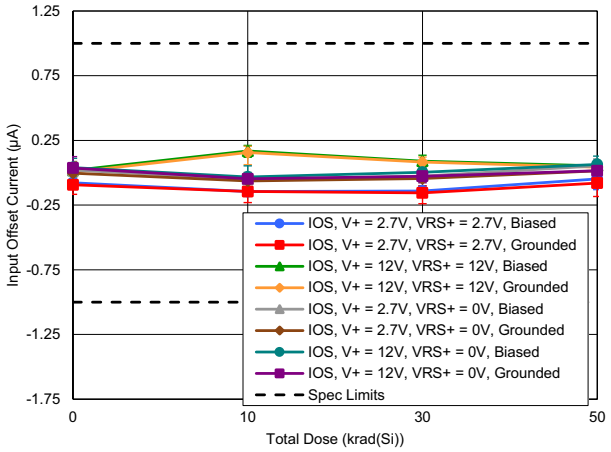


Figure 59. Input Offset Current vs TID

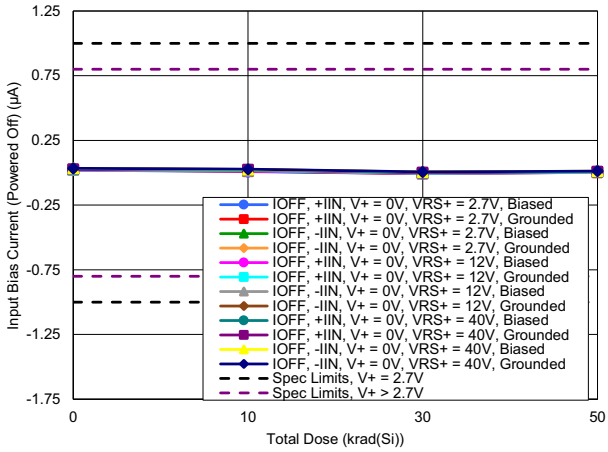


Figure 60. Input Bias Current (Powered Off) vs TID

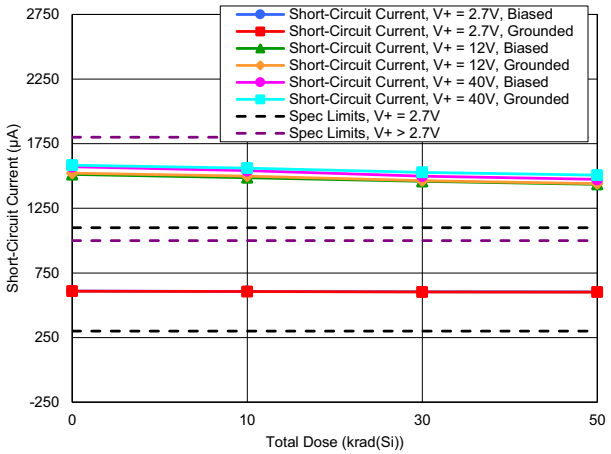


Figure 61. Short-Circuit Current vs TID

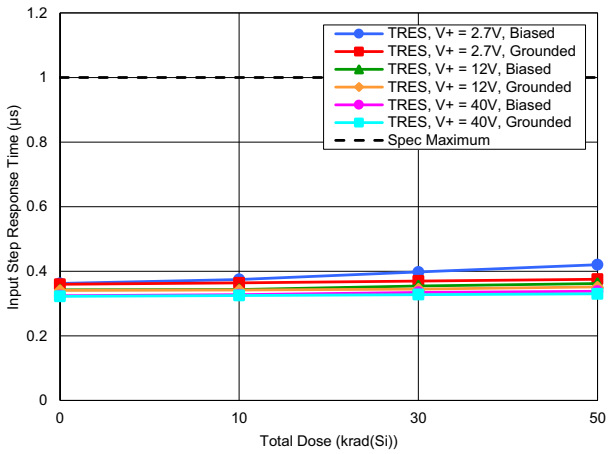


Figure 62. Input Step Response Time vs TID

7.1 Single Event Effects Testing

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response.

7.1.1 SEE Test Facility

SEE Testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels required for advanced radiation testing. SEE testing was performed with normal incidence silver ions for an LET of 43MeV·cm^2/mg at the surface of the device. Additional SET testing was performed at lower LETs so that a Weibull curve could be generated. Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room.

7.1.2 Destructive Single Event Effects (DSEE) Results

For DSEE testing, the test voltage, VTEST, was applied to the inputs RS+ and V+ while V1 and V2 were left open and V3 and V- were grounded. There was approximately a 50mV differential across RS+ and RS- when VTEST = 35V leading to a nominal output of 1V. To determine whether a DSEE had occurred the currents on RS+ and V+ were measured before and after irradiation with a failure criterion of ±10%. The output voltage was also measured before and after irradiation with a failure criterion of ±2%.

Testing showed that the ISL70100M did not exhibit any DSEE events with RS+ up to 42V and V+ up to 42V at 43MeV·cm^2/mg.

7.1.3 SET and SEFI Results

For SET testing, the ambient temperature was 25°C. The ISL70100M was tested for SETs in the five configurations shown in Table 2. For each of the configurations, the differential voltage across RS+ and RS- was approximately 50mV which yielded a nominal output of 1V. Oscilloscopes were set to capture events during which VOUT deviated by ±50mV. The ±50mV trigger criterion corresponds to ±5µA of output current for the 10kΩ load resistor. This deviation is equivalent to an input change of 2.5mV for the transconductance of 2µA/mV.

Table 2. Single Event Transient Testing Configurations

	V+ (V)	RS+ (V)	RS- (V)	V1 (V)	V2 (V)	V3 (V)	(RS+)-(RS-)	V_{OUT} (V)
Case 1	2.7	Open	-0.3	0	Open	Open	≈50mV	1.0
Case 2	35	Open	-0.3	0	Open	Open	≈50mV	1.0
Case 3	12	12	Open	Open	0	Open	≈50mV	1.0
Case 4	2.7	35	Open	Open	Open	0	≈50mV	1.0
Case 5	35	35	Open	Open	Open	0	≈50mV	1.0

Devices were tested at 43MeV·cm^2/mg (normal incidence silver), 20MeV·cm^2/mg (normal incidence copper), 8.5MeV·cm^2/mg (normal incidence argon), 2.7MeV·cm^2/mg (normal incidence neon), and 1.3MeV·cm^2/mg (normal incidence nitrogen). Four devices were tested in each condition at each LET. Irradiation runs were terminated once approximately 1,000 SET were captured or when the fluence reached 1E7ions/cm^2.

The ISL70100M exhibited positive and negative SETs. The positive deviations were limited in magnitude by the power supply voltage. When V+ = 2.7V, the maximum positive deviation was 800mV. When V+ = 12V or 35V, the maximum positive deviation was 10V. The negative deviations were limited by the output voltage, and in all cases the maximum negative deviation was -1V. The maximum duration of the SETs was approximately 80µs. More than 99.5% of the SETs were less than 30µs in duration. Figure 63 shows a composite of the 20 longest SET deviations captured in one run in Case 1. Figure 64 shows a composite of the 20 longest SET deviations captured in one run in Case 3.

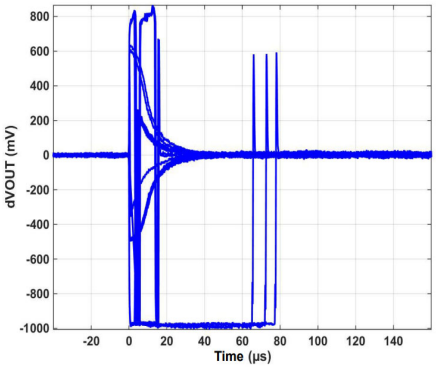


Figure 63. 20 Longest SET Deviations Captured in One Run Case 1

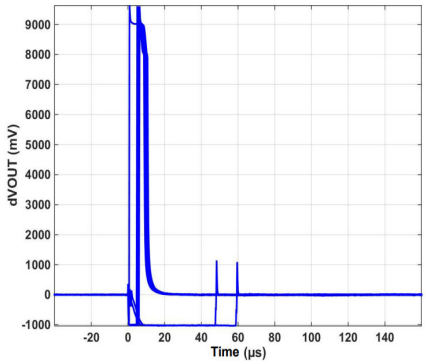


Figure 64. 20 Longest SET Deviations Captured in One Run Case 3

The magnitude and duration of the deviations was dependent on the LET of the ions, however, the ISL70100M still exhibited SETs down to an LET of 1.3MeV·cm^2/mg. At 1.3MeV·cm^2/mg, the magnitude of the SETs was limited to about +850mV and -350mV, and the maximum duration was approximately 20µs.

There were minor differences in the cross-section between the different test cases. The summary statistics for the cross-sections at each LET are shown in Table 3.

Table 3. 50mV Worse-Case-Section Statistics

LET	Cross-Section (µm^2)			
	Minimum	Mean	Maximum	2x Max
43	202,000	235,000	274,000	549,000
20	128,000	178,000	231,000	462,000
8.5	90,400	122,000	167,000	333,000
2.7	47,500	58,900	79,100	158,000
1.3	340	964	1,880	3,760

A Weibull curve was fitted to the 2x Maximum cross-section data points. The Weibull fitting was done to ensure that all data was below the fit line. The Weibull parameters are saturation cross-section = 807,100µm^2, Threshold LET = 1.151MeV·cm^2/mg, Width = 60.87MeV·cm^2/mg, and Exponent = 0.3914.

7.1.4 Conclusion

Testing showed that the ISL70100M did not exhibit any DSEE events with RS+ up to 42V and V+ up to 42V at 43MeV·cm^2/mg.

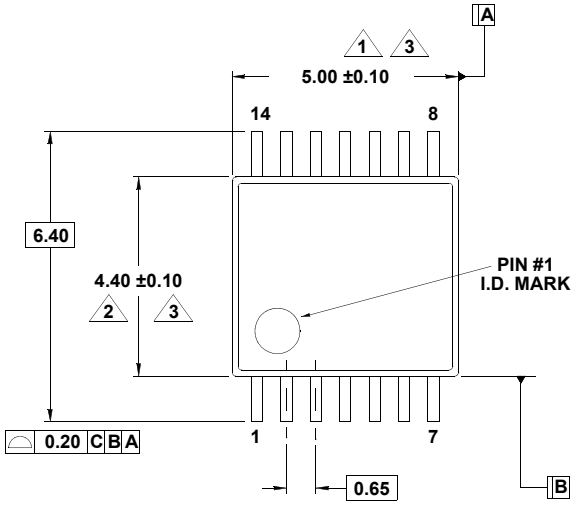
The ISL70100M exhibits ±50mV output SETs down to 1.3MeV·cm^2/mg (normal incidence nitrogen) with a cross-section of 3,760µm^2. CREME96 modeling for LEO with 100mil Al shielding at average proton density leads to a predicted 10.15 events per device day of at least ±50mV. CREME96 simulation for GEO results estimates 0.220 events per device day.

Proper application of the ISL70100M for in-orbit use must accommodate the SET. The most direct method of mitigation would be to filter the output with a capacitor across the output resistor. For example, a 0.1µF capacitor across the 10kΩ load resistor (RC = 1ms) would limit the resultant SET from the 9V positive deviations for 10µs seen in Figure 64 to 90mV. This same capacitor would limit the long (80µs) negative 1V SET (Figure 63) to about 77mV. Increasing the capacitor value would proportionally reduce the resultant SET further. This filter would, of course, significantly slow the circuit response to real changes at the input.

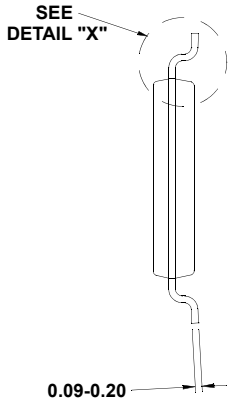
8. Package Outline Drawing

For the most recent package outline drawing, see M14.173.

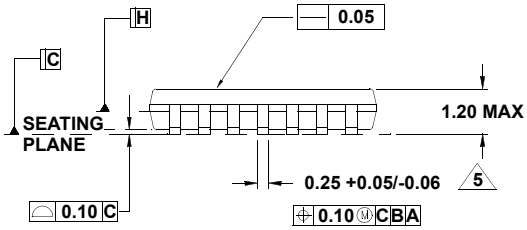
M14.173
14 Lead Thin Shrink Small Outline Package (TSSOP)
Rev 3, 10/09



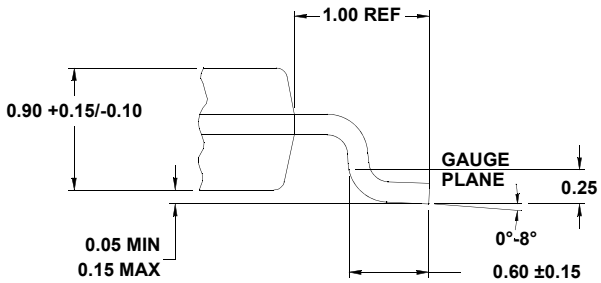
TOP VIEW



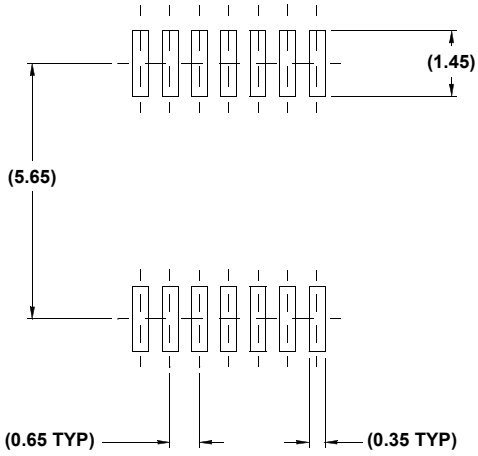
END VIEW



SIDE VIEW



DETAIL "X"



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion shall be 0.80mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimension in ( ) are for reference only.
7. Conforms to JEDEC MO-153, variation AB-1.

9. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	Package Description[3] (RoHS Compliant)	Package Drawing #	Carrier Type	Temp Range
ISL70100M30VZ	ISL70100 MVZ	LDR to 30krad(Si)	14 Ld TSSOP	M14.173	Tray	-55 to +125°C
ISL70100M50VZ		LDR to 50krad(Si)	14 Ld TSSOP	M14.173	Tray	-55 to +125°C
ISL70100MEV1Z	Evaluation Board					

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and NiPdAu-Ag plate -e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL70100M product information page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.

10. Revision History

Rev.	Date	Description
1.01	Feb 14, 2025	Minor update to footprint section in Appendix. Corrected part marking.
1.00	Jan 30, 2025	Initial release

A. ECAD Design Information

This information supports the development of the PCB ECAD model for this device. It is intended to be used by PCB designers.

A.1 Part Number Indexing

Orderable Part Number	Number of Pins	Package Type	Package Code/POD Number
ISL70100M30VZ	14	TSSOP	M14.173
ISL70100M50VZ	14	TSSOP	M14.173

A.2 Symbol Pin Information

A.2.1 14-TSSOP

Pin Number	Primary Pin Name	Primary Electrical Type	Alternate Pin Name(s)
1	NC	Passive	-
2	RS-	Input	-
3	V+	Power	-
4	DNC	Passive	-
5	V-	Power	-
6	DNC	Passive	-
7	NC	Passive	-
8	NC	Passive	-
9	NC	Passive	-
10	OUT	Output	-
11	DNC	Passive	-
12	DNC	Passive	-
13	RS+	Input	-
14	NC	Passive	-

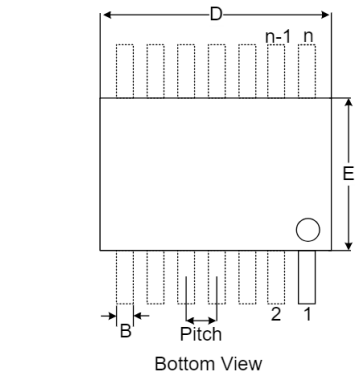
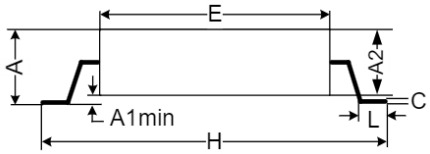
A.3 Symbol Parameters

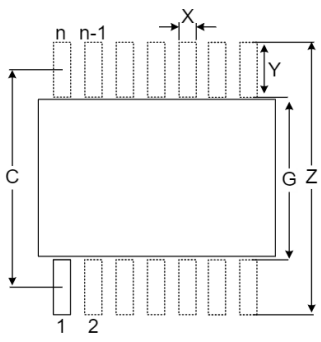
Orderable Part Number	Qualification	Radiation Qualification	LDR	Mounting Type	Min Operating Temperature	Max Operating Temperature	Min Input Voltage	Max Input Voltage	RoHS	Min Common Mode Input Voltage	Max Common Mode Input Voltage	Min Input Differential Voltage	Max Input Differential Voltage	Transconductance Accuracy 25°C	Transconductance Accuracy -55°C, 125°C
ISL70100M30VZ	Space	Radiation Tolerant	30 krad(Si)	SMD	-55 °C	125 °C	2.7 V	40 V	Compliant	-0.3 V	40 V	0 mV	150 mV	1 %	1.5 %
ISL70100M50VZ	Space	Radiation Tolerant	50 krad(Si)	SMD	-55 °C	125 °C	2.7 V	40 V	Compliant	-0.3 V	40 V	0 mV	150 mV	1 %	1.5 %

A.4 Footprint Design Information

A.4.1 14-TSSOP

IPC Footprint Type	Package Code/ POD Number	Number of Pins
SOP	M14.173	14

Description	Dimension	Value (mm)	Diagram
Minimum lead span (horizontal side)	Hmin	6.20	 Bottom View
Maximum lead span (horizontal side)	Hmax	6.60	
Minimum body span (horizontal side)	Dmin	4.90	
Maximum body span (horizontal side)	Dmax	5.10	
Minimum body span (vertical side)	Emin	4.30	
Maximum body span (vertical side)	Emax	4.50	
Minimum Lead Width	Bmin	0.19	
Maximum Lead Width	Bmax	0.30	
Minimum Lead Length	Lmin	0.45	 Side View
Maximum Lead Length	Lmax	0.75	
Maximum Height	Amax	1.20	
Minimum Standoff Height	A1min	0.05	
Minimum Lead Thickness	cmin	0.09	
Maximum Lead Thickness	cmax	0.20	
Total number of pin positions (including absent pins)	PinCount	14	
Distance between the center of any two adjacent pins	Pitch	0.65	

Recommended Land Pattern			
Description	**Dimension**	**Value (mm)**	**Diagram**
Distance between left pad toe to right pad toe.	Z	7.1	 PCB Top View
Distance between left pad heel to right pad heel.	G	4.2	
Row spacing. Distance between pad centers	C	5.65	
Pad Width	X	0.35	
Pad Length	Y	1.45	

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