ISL70244SEH, ISL73244SEH

19MHz Radiation Hardened 40V Dual Rail-to-Rail Input-Output, Low-Power Operational Amplifier

FN8592
Rev.5.00
Dec 2, 2020

The ISL70244SEH and ISL73244SEH (ISL7x244SEH) feature two low-power amplifiers optimized to provide maximum dynamic range. These operational amplifiers (op amps) feature a unique combination of rail-to-rail operation on the input and output and a slew enhanced front end that provides ultra fast slew rates positively proportional to a given step size. These features increase accuracy under both periodic and transient conditions. The ISL7x244SEH also offers low power, low offset voltage, and low temperature drift, which makes it ideal for applications requiring both high DC accuracy and AC performance. With <5µs recovery for Single Event Transients (SET) (LET_{TH} = 86.4MeV • cm^2/mg), the number of filtering components needed is drastically reduced. The ISL7x244SEH is also immune to single-event latch-up because it is fabricated in the Renesas proprietary PR40 Silicon On Insulator (SOI) process.

The amplifiers are designed to operate over a single supply range of 2.7V to 40V or a split supply voltage range of ±1.35V to ±20V. Applications for these amplifiers include precision instrumentation, data acquisition, precision power supply controls, and process controls.

The ISL7x244SEH is available in a 10 Ld hermetic ceramic flatpack that operates across the temperature range of -55°C to +125°C.

Related Literature

For a full list of related documents, visit our website:

- ISL70244SEH and ISL73244SEH device pages

Features

- **Electrically screened to DLA SMD # 5962-13248**
  Acceptance tested to 50krad(Si) (LDR) wafer-by-wafer
- **<5µs recovery from SET (LET_{TH} = 86.4MeV • cm^2/mg)**
- **Unity gain stable**
- **Rail-to-rail input and output**
- **Wide gain bandwidth product 19MHz**
- **Wide single and dual supply range. . .2.7V to 40V maximum**
- Low input offset voltage . . . . . 400µV (+25°C, maximum)
- Low current consumption (per amplifier) . . . . 1.2mA, typical
- No phase reversal with input overdrive
- Slew rate
  - Large signal 60V/µs
- Operating temperature range. . . . . -55°C to +125°C
- ISL70244SEH radiation acceptance (see TID report)
  - High dose rate (50-300rad(Si)/s). . . . . 300krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- ISL73244SEH radiation acceptance (see TID report)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V_S = ±19V) . . . . . 86.4MeV • cm^2/mg

Applications

- Precision instruments
- Active filter blocks
- Data acquisition
- Power supply control
- Process control

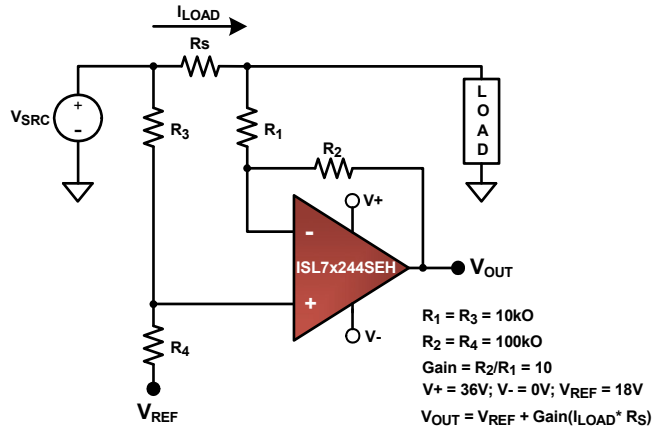


FIGURE 1. TYPICAL APPLICATION: SINGLE-SUPPLY, HIGH-SIDE CURRENT SENSE AMPLIFIER

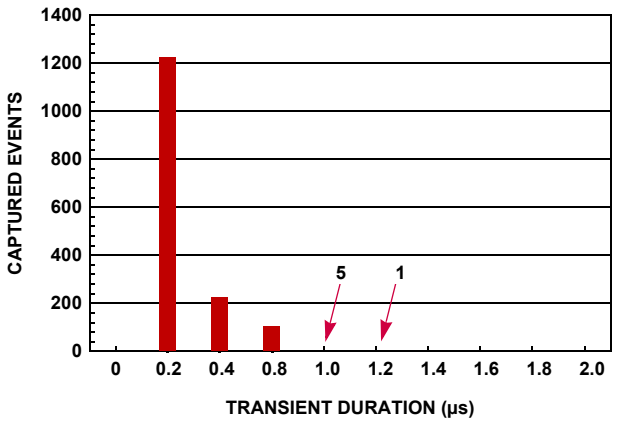
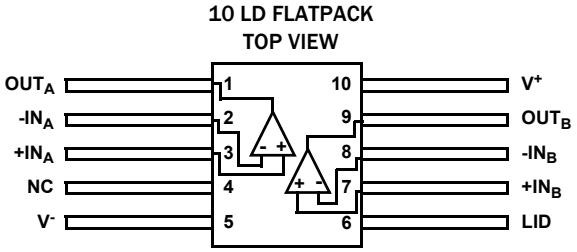


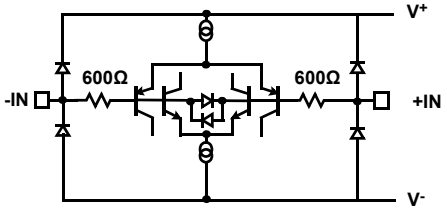
FIGURE 2. TYPICAL SINGLE EVENT TRANSIENT DURATION AT +25°C LET = 60MeV • cm^2/ mg IN UNITY GAIN (V_S = ±18V)

Pin Configuration

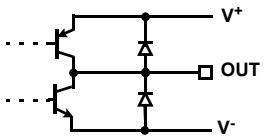


Pin Descriptions

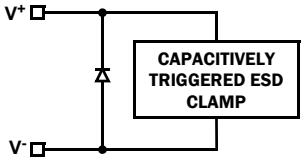
PIN NUMBER	PIN NAME	EQUIVALENT ESD CIRCUIT	DESCRIPTION
5	V$^-$	Circuit 3	Negative power supply
7	+IN$_B$	Circuit 1	Amplifier B noninverting input
8	-IN$_B$	Circuit 1	Amplifier B inverting input
9	OUT$_B$	Circuit 2	Amplifier B output
10	V$^+$	Circuit 3	Positive power supply
1	OUT$_A$	Circuit 2	Amplifier A output
2	-IN$_A$	Circuit 1	Amplifier A inverting input
4	NC	-	This pin is not electrically connected internally
3	+IN$_A$	Circuit 1	Amplifier A noninverting input
6	LID	NA	Unbiased, tied to package lid



CIRCUIT 1



CIRCUIT 2



CIRCUIT 3

Ordering Information

ORDERING SMD NUMBER (Note 2)	PART NUMBER (Note 1)	RADIATION HARDNESS (Total Ionizing Dose)	TEMP RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962F1324801VXC	ISL70244SEHVF	HDR to 300krad(Si), LDR to 50krad(Si)	-55 to +125	10 Ld Flatpack	K10.A
5962F1324801V9A	ISL70244SEHVX (Note 4)		-55 to +125	Die	-
N/A	ISL70244SEHF/PROTO (Note 3)	N/A	-55 to +125	10 Ld Flatpack	K10.A
N/A	ISL70244SEHX/SAMPLE (Notes 3, 4)	N/A	-55 to +125	Die	-
5962L1324802VXC	ISL73244SEHVF	LDR to 50krad(Si)	-55 to +125	10 Ld Flatpack	K10.A
5962L1324802V9A	ISL73244SEHVX (Note 4)		-55 to +125	Die	-
N/A	ISL73244SEHF/PROTO (Note 3)	N/A	-55 to +125	10 Ld Flatpack	K10.A
N/A	ISL73244SEHF/SAMPLE (Note 3, 4)	N/A	-55 to +125	Die	-
N/A	ISL70244SEHEV1Z (Note 5)	Evaluation Board			

NOTES:

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
4. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in Electrical Specifications starting on page 4.
5. The evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Absolute Maximum Ratings

Maximum Supply Voltage Differential (V^+ to V^-) 42V
Maximum Supply Voltage Differential (V^+ to V^-) (Note 8) 38V
Maximum Differential Input Current 20mA
Maximum Differential Input Voltage . . . . . 42V or (V^- - 0.5V) to V^+ + 0.5V
Min/Max Input Voltage . . . . . 42V or (V^- - 0.5V) to V^+ + 0.5V
Max/Min Input Current for Input Voltage >V^+ or <V^- . . . . . ±20mA
ESD Tolerance
Human Body Model (Tested per MIL-PRF-883 3015.7). 2kV
Machine Model (Tested per JESD22-A115-A) 200V
Charged Device Model (Tested per CDM-22CIOID). 750V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
10 Ld Flatpack Package (Notes 6, 7)	44	10

Storage Temperature Range. . . . . -65°C to +150°C

Recommended Operating Conditions

Ambient Operating Temperature Range . . . . . -55°C to +125°C
Maximum Operating Junction Temperature . . . . . +150°C
Single Supply Voltage . . . . . 2.7V to 39.6V
Split Rail Supply Voltage . . . . . ±1.35V to ±19.8V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

NOTES:

6. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379 for details.
7. For θ_{JC}, the case temperature location is the center of the package underside.
8. Tested in a heavy ion environment at LET = 86.4MeV • cm^2/mg at +125°C (T_C) for SEB. See the Single Event Effects Test Report for more information.

Electrical Specifications V_S = ±19.8V

V_{CM} = V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a High Dose Rate (HDR) of 50rad(Si)/s to 300rad(Si)/s (ISL70244SEH only) or over a total ionizing dose of 50krad(Si) with exposure at a Low Dose Rate (LDR) of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V	-400	25	400	µV
		V_{CM} = V^+ to V^-	**-500**	110	**500**	µV
Offset Voltage Temperature Coefficient	TCV_{OS}	V_{CM} = V^+ - 2V to V^- + 2V	-	0.5	-	µV/°C
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+	-	135	**800**	µV
		V_{CM} = V^-	-	128	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V	**-500**	210	**500**	nA
		V_{CM} = V^+	**-500**	200	**500**	nA
		V_{CM} = V^-	**-650**	290	**650**	nA
		V_{CM} = V^+ - 0.5V	**-500**	200	**500**	nA
		V_{CM} = V^- + 0.5V	**-650**	257	**650**	nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**	-	**V^+**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+	-	112	-	dB
		V_{CM} = V^- to V^+	**70**	-	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	-	111	-	dB
		V_{CM} = V^+ - 0.5V to V^- + 0.5V	**80**	-	-	dB
Power Supply Rejection Ratio	PSRR	V^- = -18V; V^+ = 0.5V to 18V; V^+ = 18V; V^- = -0.5V to -18V	-	143	-	dB
			83	-	-	dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground	-	125	-	dB
			90	-	-	dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No Load	-	26	**160**	mV
		R_L = 10kΩ	-	78	**175**	mV

Electrical Specifications V_S = ±19.8V

$V_{CM} = V_O = 0V$, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a High Dose Rate (HDR) of 50rad(Si)/s to 300rad(Si)/s (ISL70244SEH only) or over a total ionizing dose of 50krad(Si) with exposure at a Low Dose Rate (LDR) of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load	-	21	**160**	mV
		R_L = 10kΩ	-	64	**175**	mV
Output Short-Circuit Current	I_{SRC}	Sourcing; V_{IN} = 0V, V_{OUT} = -18V	**10**	-	-	mA
Output Short-Circuit Current	I_{SNK}	Sinking; V_{IN} = 0V, V_{OUT} = +18V	**10**	-	-	mA
Supply Current/Amplifier	I_S	Unity gain	-	1.6	2.2	mA
		T_A = +25°C post HDR/LDR radiation	-	-	2.2	mA
		T_A = -55°C to +125°C	-	2.2	**2.8**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBWP	A_V = 1, R_L = 10k	17	19	-	MHz
Voltage Noise Density	e_n	f = 10kHz	-	11.3	-	nV/√Hz
Current Noise Density	i_n	f = 10kHz	-	0.312	-	pA/√Hz
Large Signal Slew Rate	SR	A_V = 1, R_L = 10kΩ, $V_O = 10V_{P-P}$	**60**	-	-	V/µs

Electrical Specifications V_S = ±2.5V

V_S = ±2.5V, $V_{CM} = V_O$ = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a High Dose Rate (HDR) of 50rad(Si)/s to 300rad(Si)/s (ISL70244SEH only) or over a total ionizing dose of 50krad(Si) with exposure at a Low Dose Rate (LDR) of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V	-400	20	400	µV
		$V_{CM} = V^+$ to V^-	**-500**	80	**500**	µV
Offset Voltage Temperature Coefficient	TCV_{OS}	$V_{CM} = V^+ - 2V$ to $V^- + 2V$	-	0.5	-	µV/°C
Input Offset Channel-to-Channel Match	ΔV_{OS}	$V_{CM} = V^+$	-	132	**800**	µV
		$V_{CM} = V^-$	-	127	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V	**-400**	226	**400**	nA
		$V_{CM} = V^+$	**-400**	182	**400**	nA
		$V_{CM} = V^-$	**-580**	260	**580**	nA
		$V_{CM} = V^+ - 0.5V$	**-400**	181	**400**	nA
		$V_{CM} = V^- + 0.5V$	**-580**	224	**580**	nA
Input Offset Current	I_{OS}	$V_{CM} = V^+$ to V^-	-30	0	30	nA
			-50	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**	-	**V^+**	V
Common-Mode Rejection Ratio	CMRR	$V_{CM} = V^-$ to V^+	-	92	-	dB
		$V_{CM} = V^-$ to V^+	**70**	-	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	-	91	-	dB
		$V_{CM} = V^+ - 0.5V$ to $V^- + 0.5V$	**74**	-	-	dB

Electrical Specifications V_S = ±2.5V

V_S = ±2.5V, V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a High Dose Rate (HDR) of 50rad(Si)/s to 300rad(Si)/s (ISL70244SEH only) or over a total ionizing dose of 50krad(Si) with exposure at a Low Dose Rate (LDR) of <10mrad(Si)/s.**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Power Supply Rejection Ratio	PSRR	V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V	-	135	-	dB
		V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V T_A = +125°C, T_A = +25°C **OR** T_A = +25°C with HDR/LDR radiation	**80**	-	-	dB
		V^- = -2.5V; V^+ = 4.5V to 2.5V; V^+ = 2.5V; V^- = -4.5V to -2.5V T_A = -55°C	**70**	-	-	dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground	-	118	-	dB
		R_L = 10kΩ to ground T_A = +125°C, T_A = +25°C **OR** T_A = +25°C with HDR/LDR radiation	**90**	-	-	dB
		R_L = 10kΩ to ground T_A = -55°C	**80**	-	-	dB
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No Load	-	15	**85**	mV
		R_L = 10kΩ	-	23	**105**	mV
		R_L = 600Ω	-	-	**400**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No load	-	11	**85**	mV
		R_L = 10kΩ	-	18	**105**	mV
		R_L = 600Ω	-	-	**400**	mV
Supply Current/Amplifier	I_S	Unity gain	-	1.2	1.5	mA
		T_A = +25°C post HDR/LDR radiation	-	-	1.5	mA
		T_A = -55°C to +125°C	-	1.7	**2.0**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBWP	A_V = 1, R_L = 10k	15	17	-	MHz
Voltage Noise Density	e_n	f = 10kHz	-	12.3	-	nV/√Hz
Current Noise Density	i_n	f = 10kHz	-	0.313	-	pA/√Hz
Large Signal Slew Rate	SR	A_V = 1, R_L = 10kΩ, V_O = $3V_{P-P}$	-	35	-	V/µs

Electrical Specifications V_S = ±1.35V V_{CM} = V_O = 0V, R_L = Open, T_A= +25°C, unless otherwise noted. Boldface limits apply over the operating temperature range, -55°C to +125°C; over a total ionizing dose of 300krad(Si) with exposure of a high dose rate of 50rad(Si)/s to 300rad(Si)/s (ISL70244SEH only) or over a total ionizing dose of 50krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN (Note 9)	TYP	MAX (Note 9)	UNIT
Offset Voltage	V_{OS}	V_{CM} = 0V	-400	51	400	µV
		V_{CM} = V_+ to V^-	**-500**	80	**500**	µV
Input Offset Channel-to-Channel Match	ΔV_{OS}	V_{CM} = V^+	-	79	**800**	µV
		V_{CM} = V^-	-	119	**800**	µV
Input Bias Current	I_B	V_{CM} = 0V	**-375**	110	**375**	nA
		V_{CM} = V^+	**-375**	180	**375**	nA
		V_{CM} = V^-	**-565**	225	**565**	nA
		V_{CM} = V^+ - 0.5V	**-375**	180	**375**	nA
		V_{CM} = V^- + 0.5V	**-565**	223	**565**	nA
Input Offset Current	I_{OS}	V_{CM} = V^+ to V^-	-30	0	30	nA
			-50	0	**50**	nA
Common-Mode Input Voltage Range	V_{CMIR}		**V^-**	-	**V^+**	V
Output Voltage High (V_{OUT} to V^+)	V_{OH}	R_L = No load	-	14	**50**	mV
		R_L = 10kΩ	-	19	**70**	mV
Output Voltage Low (V_{OUT} to V^-)	V_{OL}	R_L = No Load	-	10	**50**	mV
		R_L = 10kΩ	-	14	**70**	mV
Supply Current/Amplifier	I_S	Unity gain	-	1.1	1.5	mA
		T_A = +25°C post HDR/LDR radiation	-	-	1.5	mA
		T_A = -55°C to +125°C	-	1.6	**2.0**	mA
AC SPECIFICATIONS						
Gain Bandwidth Product	GBWP	A_V = 1, R_L = 10k	**10**	15	-	MHz
Voltage Noise Density	e_n	f = 10kHz	-	12	-	nV/√Hz
Current Noise Density	i_n	f = 10kHz	-	0.312	-	pA/√Hz

NOTE:

9. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C.

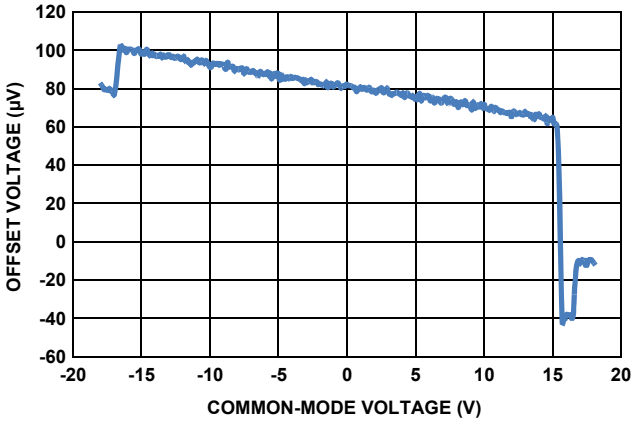


FIGURE 3. OFFSET VOLTAGE vs COMMON-MODE VOLTAGE

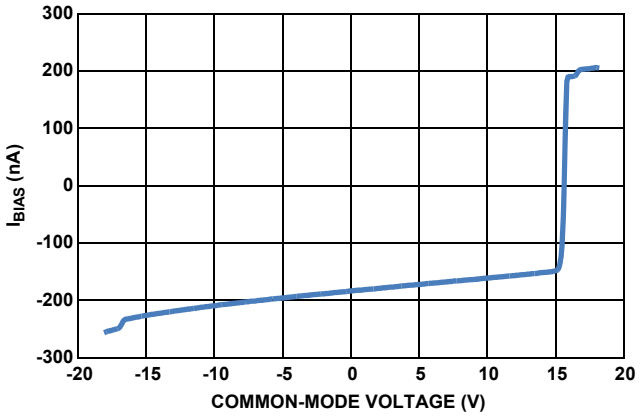


FIGURE 4. I_{BIAS} vs COMMON-MODE VOLTAGE

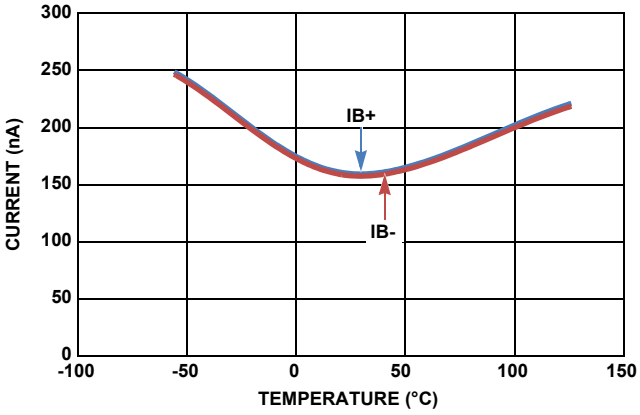


FIGURE 5. I_{BIAS} vs TEMPERATURE (V_S = ±18V)

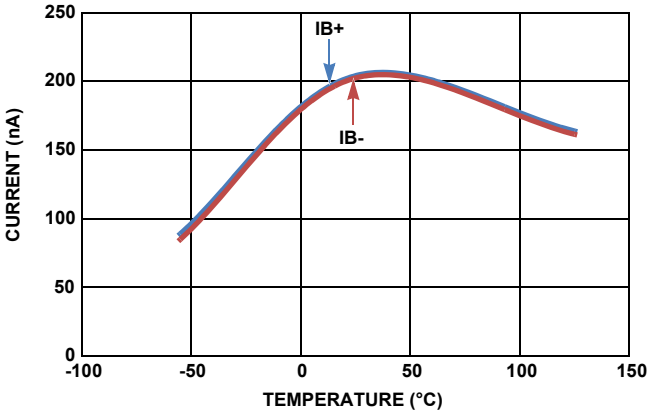


FIGURE 6. I_{BIAS} vs TEMPERATURE (V_S = ±2.5V)

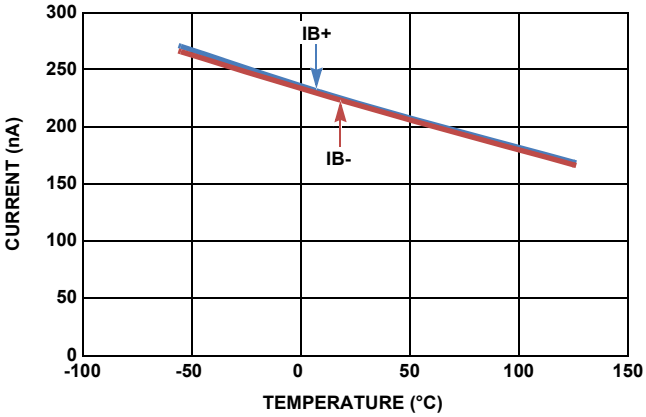


FIGURE 7. I_{BIAS} vs TEMPERATURE, (V_S = ±1.5V)

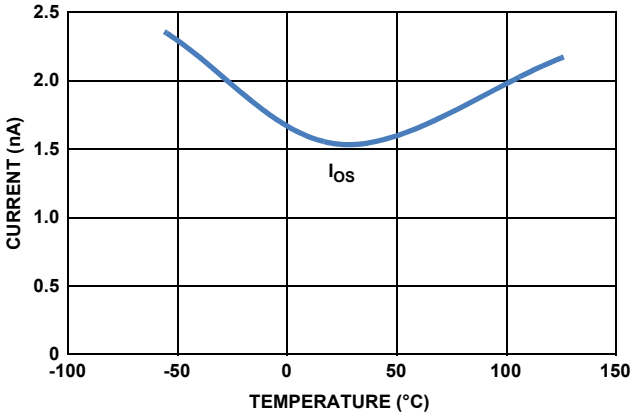


FIGURE 8. I_{OS} vs TEMPERATURE (V_S = ±18V)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

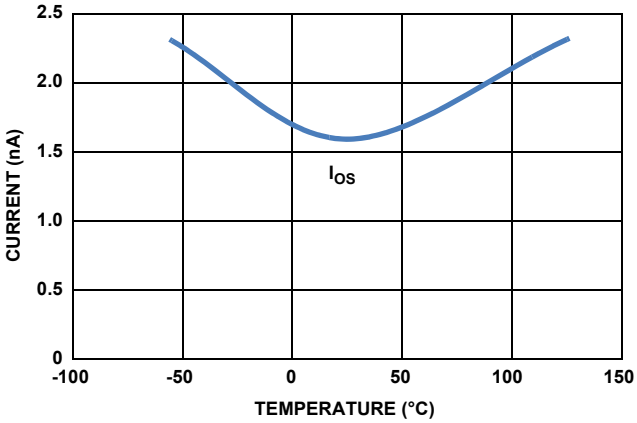


FIGURE 9. I_{OS} vs TEMPERATURE (V_S = ±2.5V)

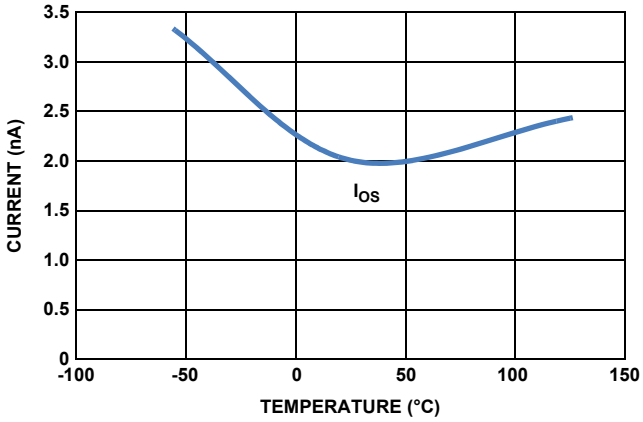


FIGURE 10. I_{OS} vs TEMPERATURE (V_S = ±1.5V)

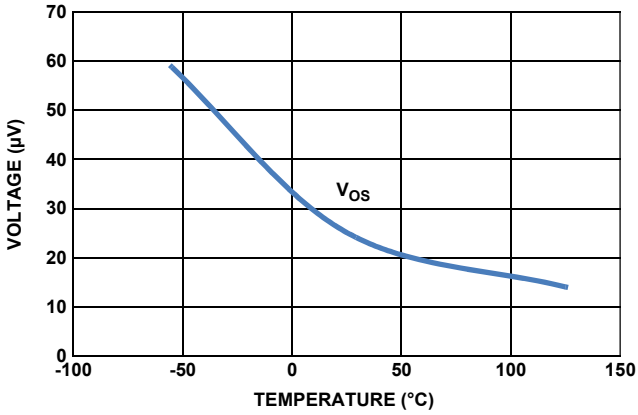


FIGURE 11. V_{OS} vs TEMPERATURE (V_S = ±18V)

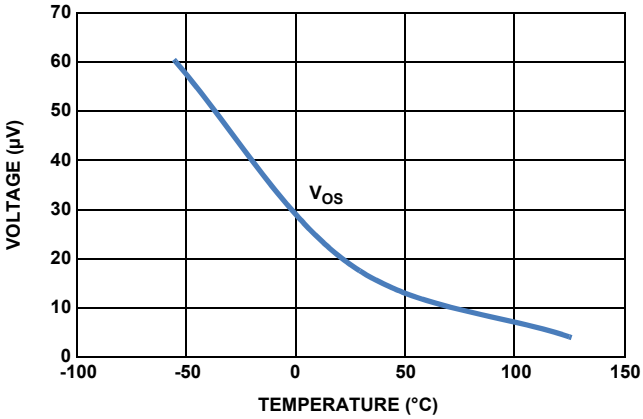


FIGURE 12. V_{OS} vs TEMPERATURE (V_S = ±2.5V)

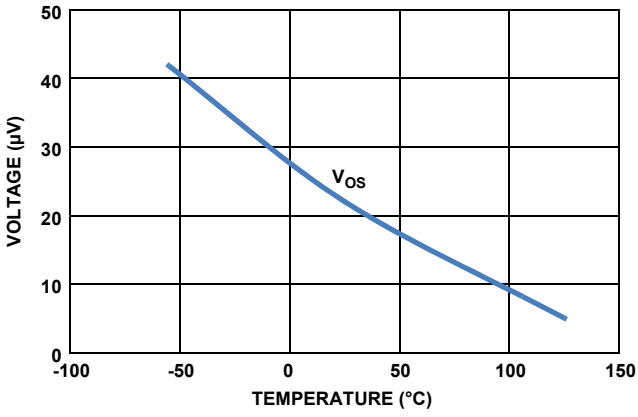


FIGURE 13. V_{OS} vs TEMPERATURE (V_S = ±1.5V)

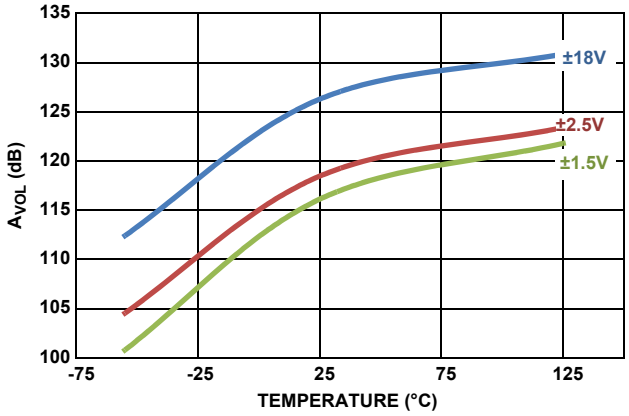


FIGURE 14. A_{VOL} vs TEMPERATURE vs SUPPLY VOLTAGE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

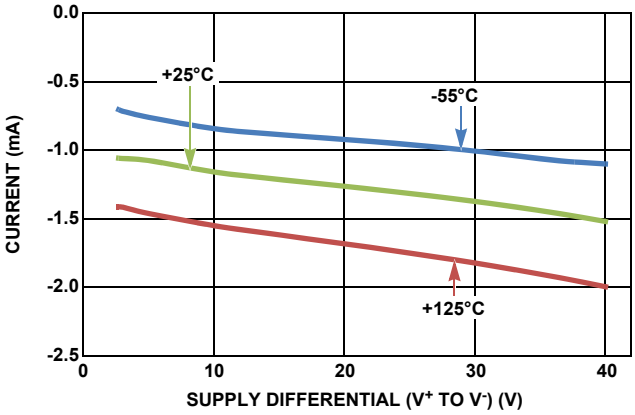


FIGURE 15. NEGATIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

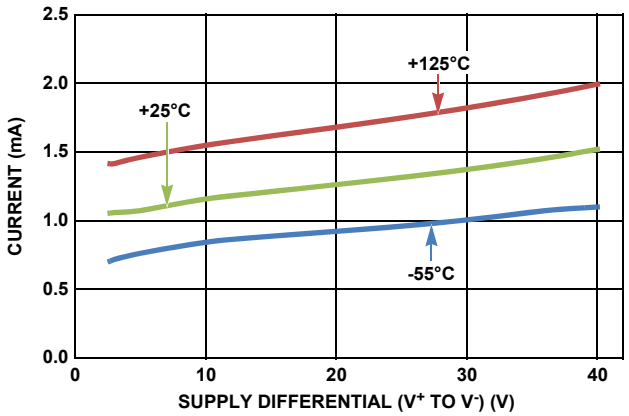


FIGURE 16. POSITIVE SUPPLY CURRENT vs SUPPLY VOLTAGE

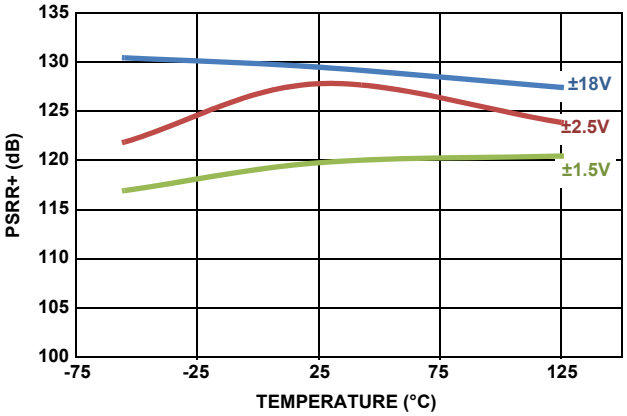


FIGURE 17. PSRR+ vs TEMPERATURE vs SUPPLY VOLTAGE

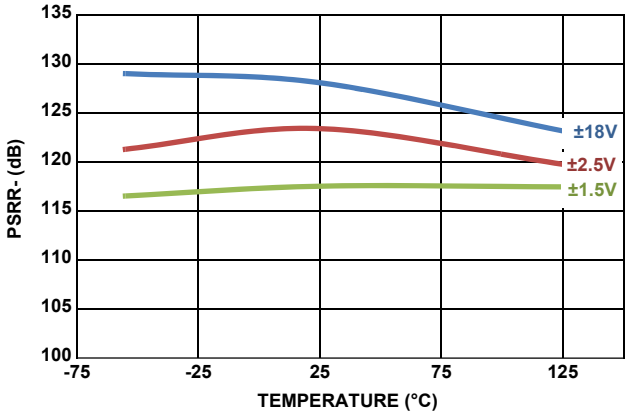


FIGURE 18. PSRR- vs TEMPERATURE vs SUPPLY VOLTAGE

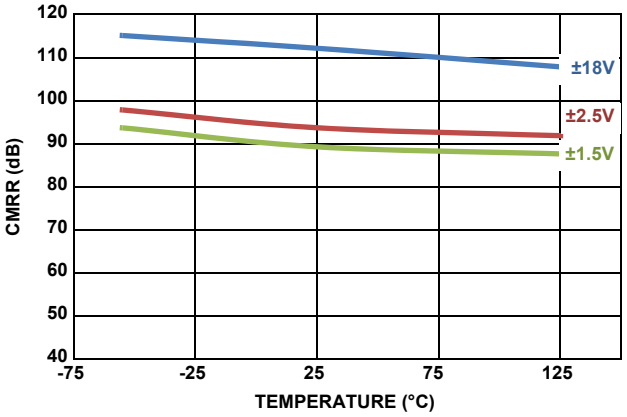


FIGURE 19. CMRR vs TEMPERATURE vs SUPPLY VOLTAGE

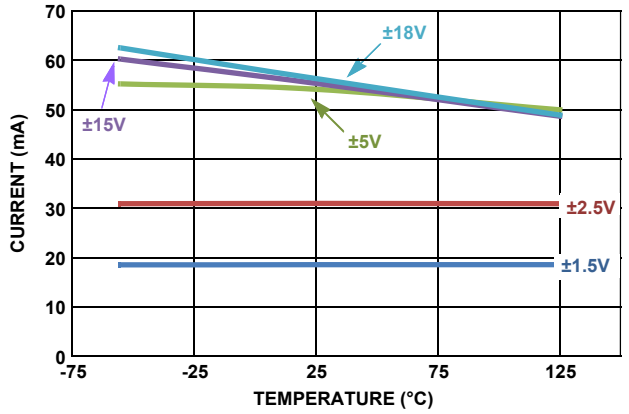


FIGURE 20. SHORT-CIRCUIT CURRENT vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

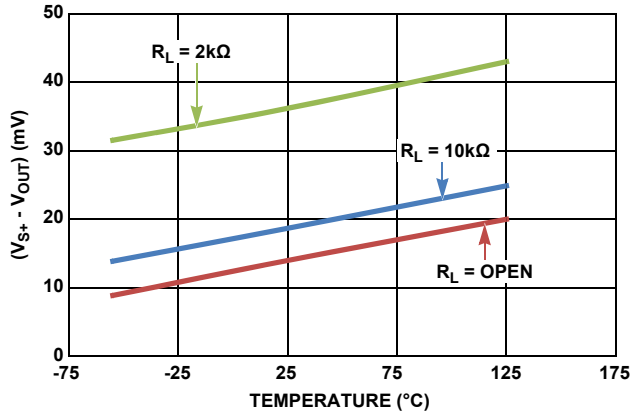


FIGURE 21. (V_S = ±1.5V) V_{OH} vs TEMPERATURE

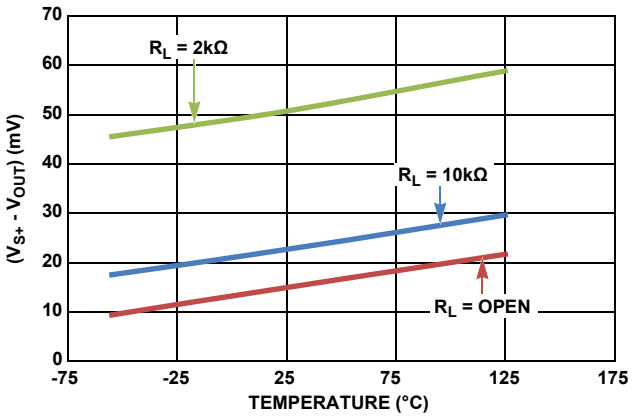


FIGURE 22. (V_S = ±2.5V) V_{OH} vs TEMPERATURE

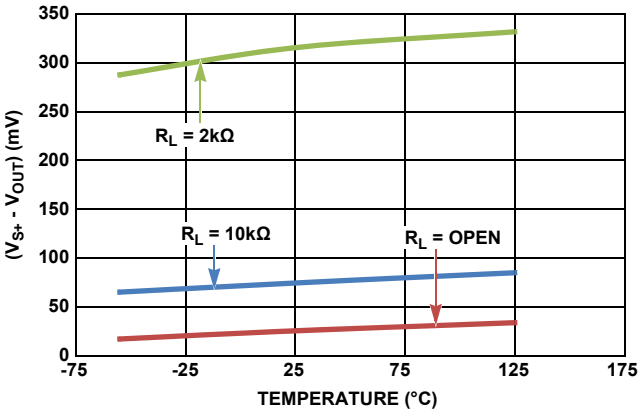


FIGURE 23. (V_S = ±18V) V_{OH} vs TEMPERATURE

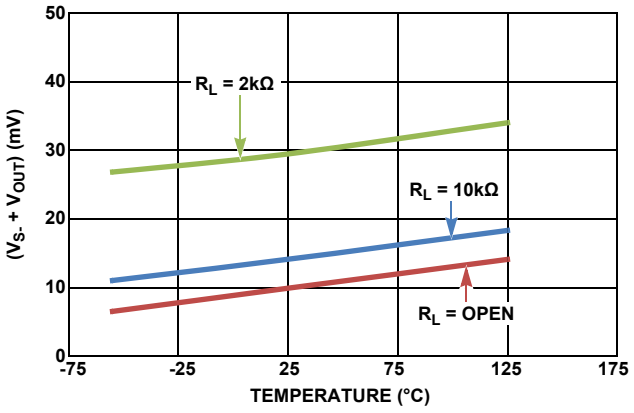


FIGURE 24. (V_S = ±1.5V) V_{OL} vs TEMPERATURE

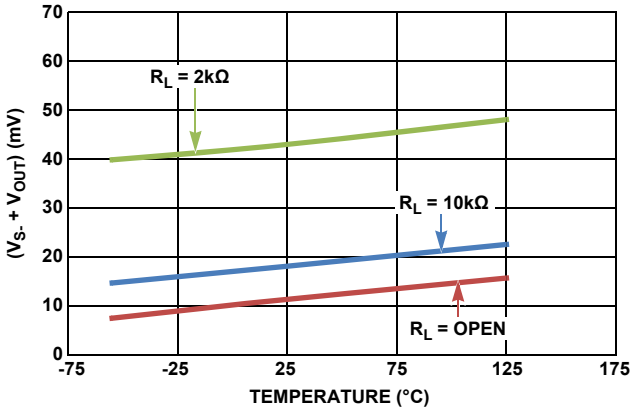


FIGURE 25. (V_S = ±2.5V) V_{OL} vs TEMPERATURE

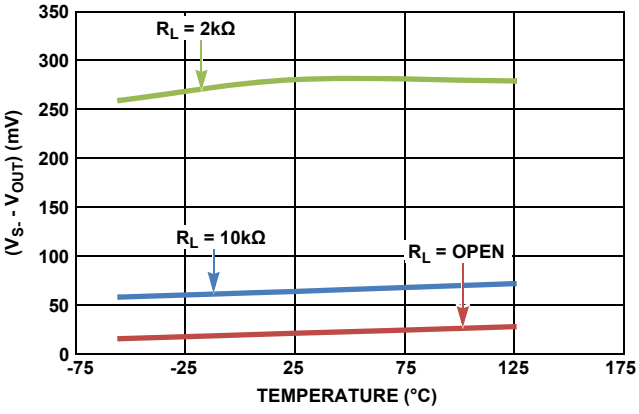


FIGURE 26. (V_S = ±18V) V_{OL} vs TEMPERATURE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

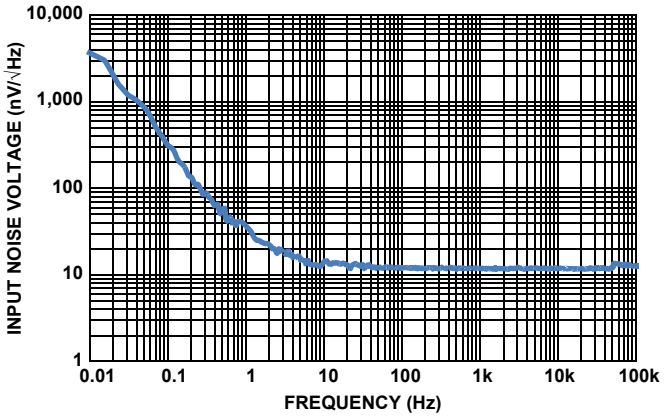


FIGURE 27. INPUT NOISE VOLTAGE SPECTRAL DENSITY (V_S = ±18V)

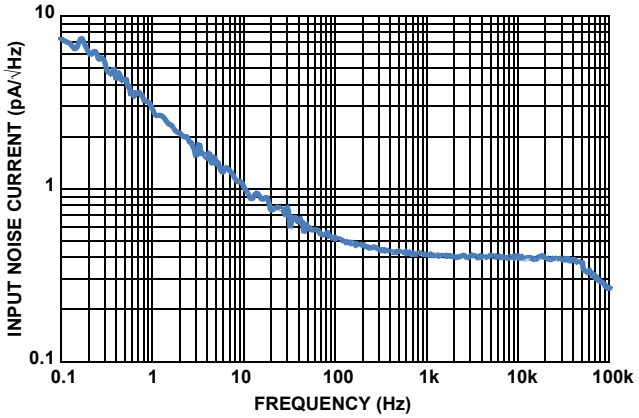


FIGURE 28. INPUT NOISE CURRENT SPECTRAL DENSITY (V_S = ±18V)

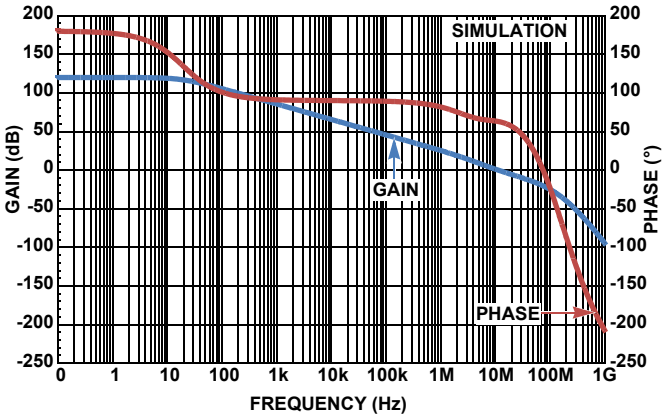


FIGURE 29. OPEN-LOOP FREQUENCY RESPONSE (C_L = 0.01pF)

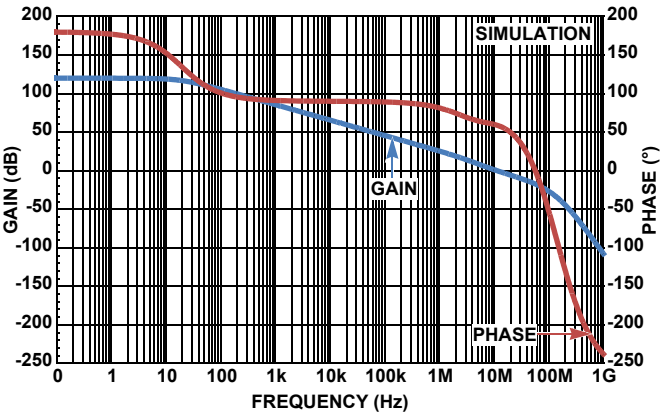


FIGURE 30. OPEN-LOOP FREQUENCY RESPONSE (C_L = 10pF)

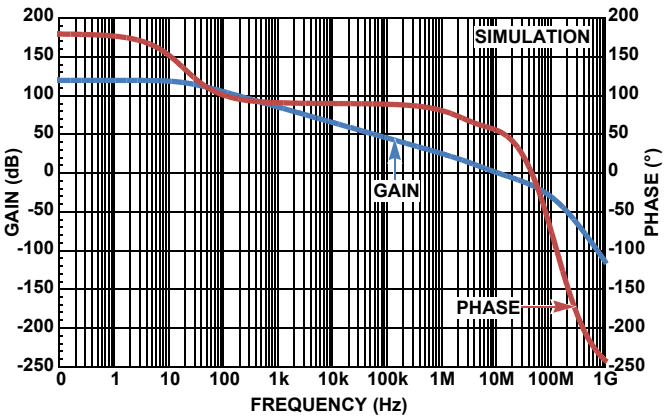


FIGURE 31. OPEN-LOOP FREQUENCY RESPONSE (C_L = 22pF)

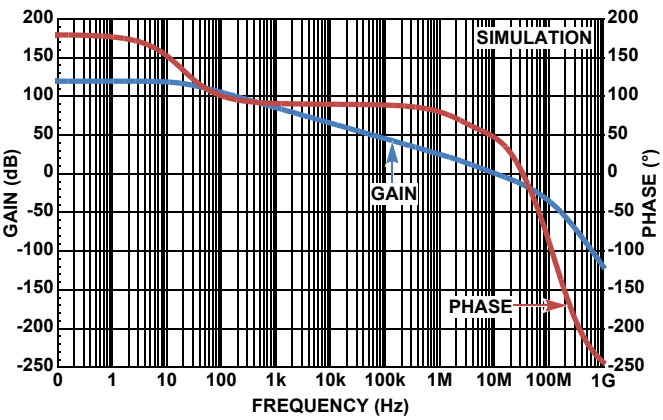


FIGURE 32. OPEN-LOOP FREQUENCY RESPONSE (C_L = 47pF)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

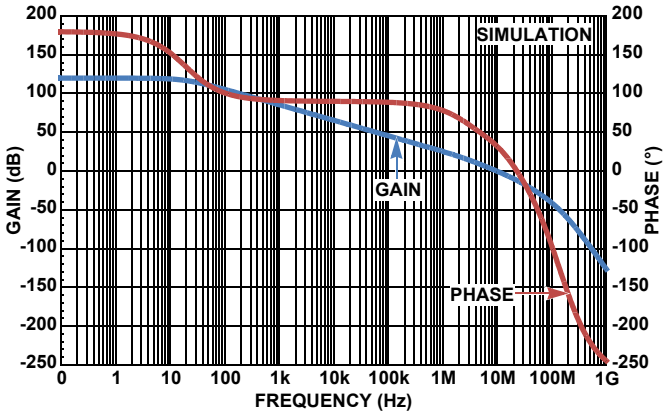


FIGURE 33. OPEN-LOOP FREQUENCY RESPONSE (C_L = 100pF)

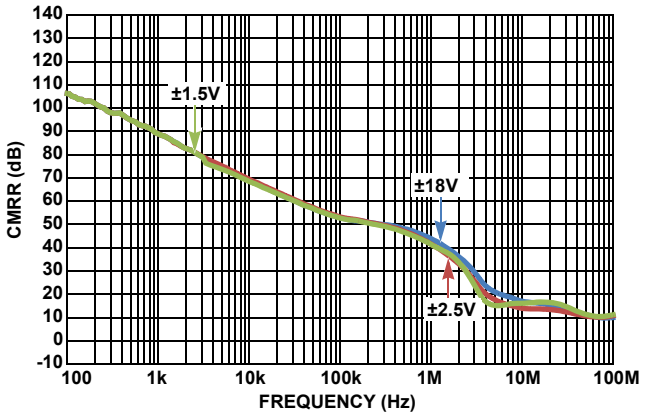


FIGURE 34. CMRR vs FREQUENCY

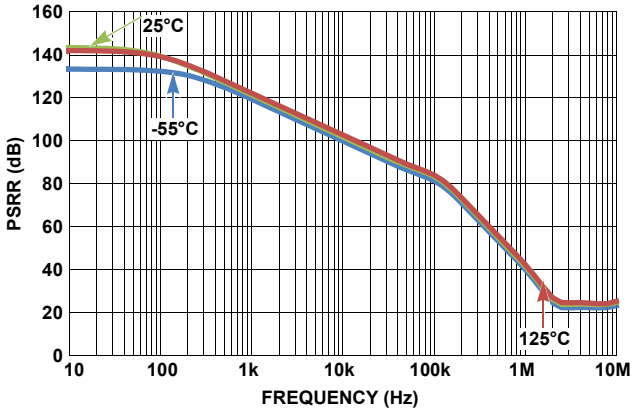


FIGURE 35. PSRR vs FREQUENCY, ±18V

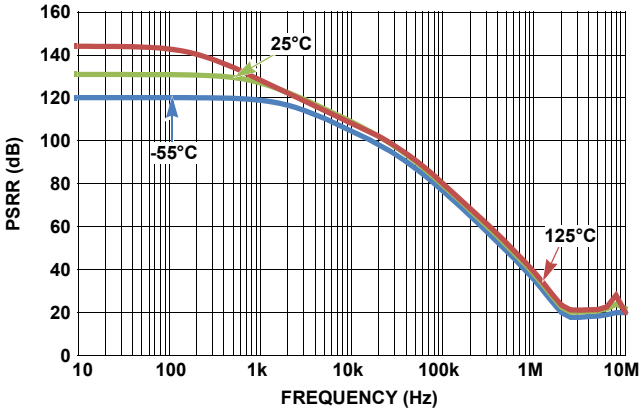


FIGURE 36. PSRR vs FREQUENCY, ±2.5V

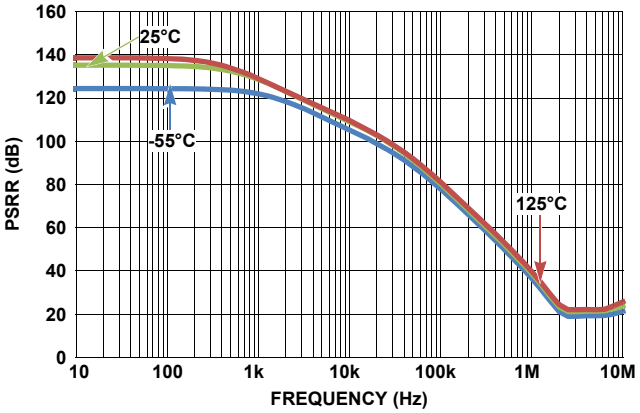


FIGURE 37. PSRR vs FREQUENCY, ±1.5V

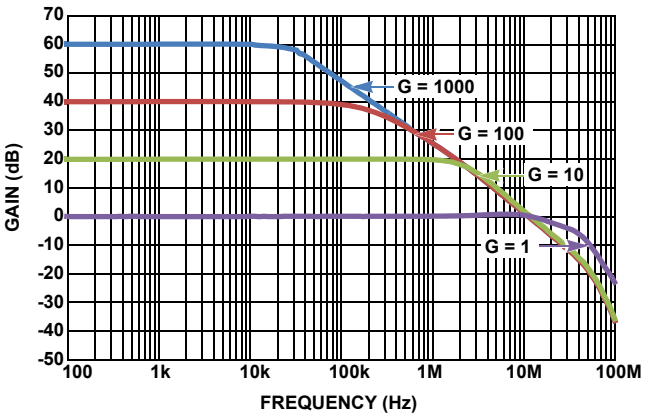


FIGURE 38. CLOSED LOOP GAIN vs FREQUENCY RESPONSE

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

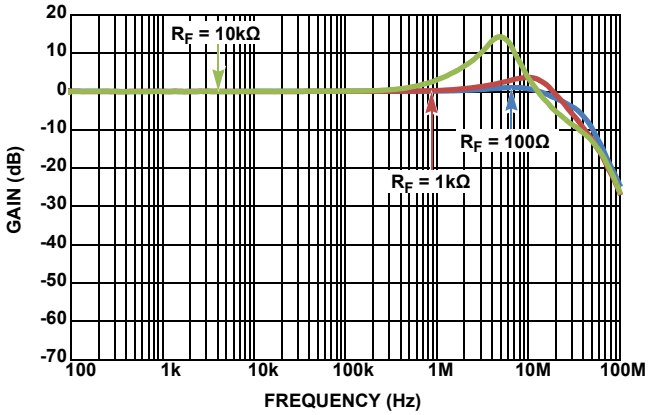


FIGURE 39. FEEDBACK RESISTANCE (R_F) vs FREQUENCY RESPONSE

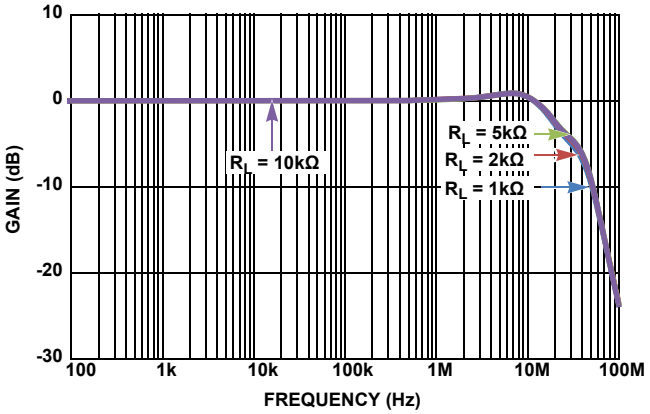


FIGURE 40. LOAD RESISTANCE vs FREQUENCY RESPONSE

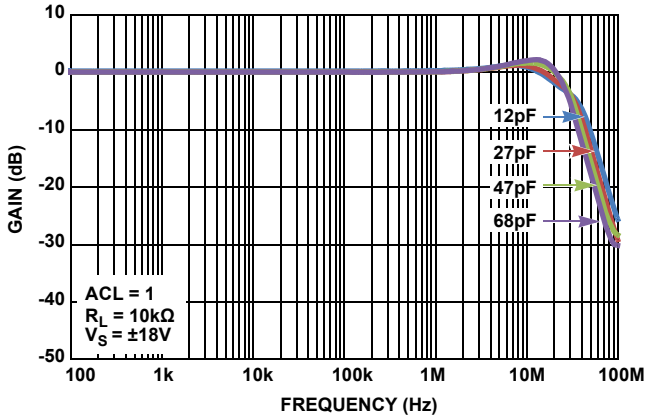


FIGURE 41. UNITY GAIN RESPONSE vs LOAD CAPACITANCE

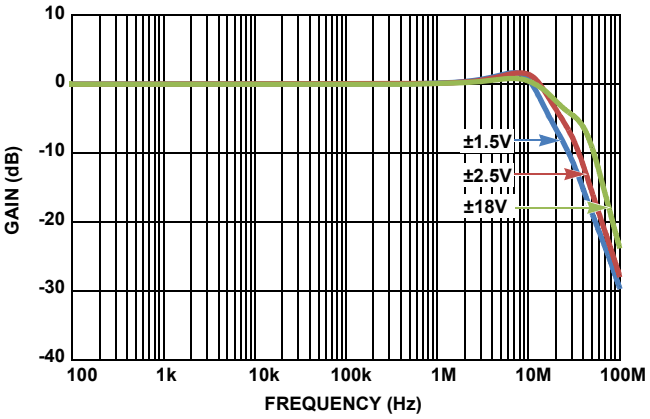


FIGURE 42. SUPPLY VOLTAGE vs FREQUENCY RESPONSE

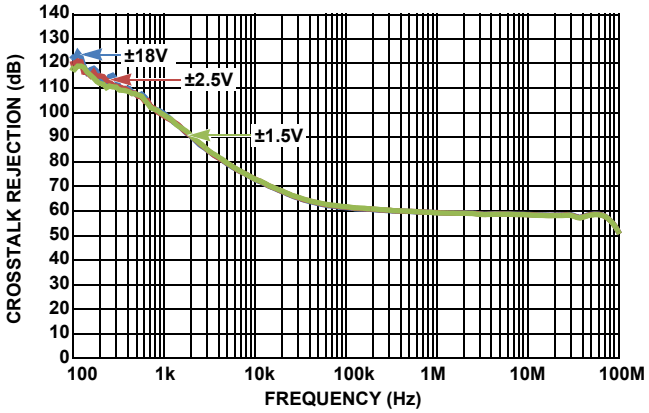


FIGURE 43. CROSSTALK REJECTION vs FREQUENCY

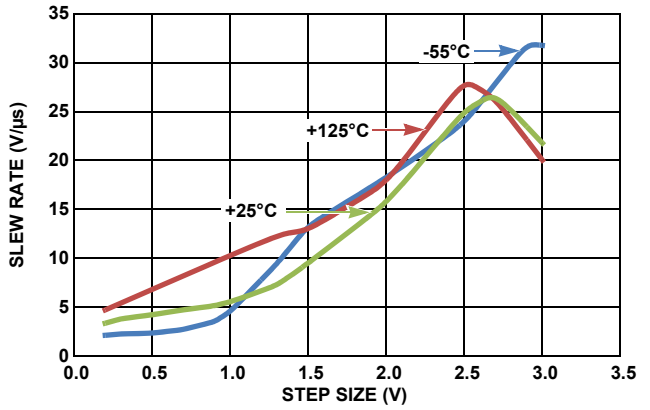


FIGURE 44. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±1.5V)

Typical Performance Curves

Unless otherwise specified, V_S ± 18V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. **(Continued)**

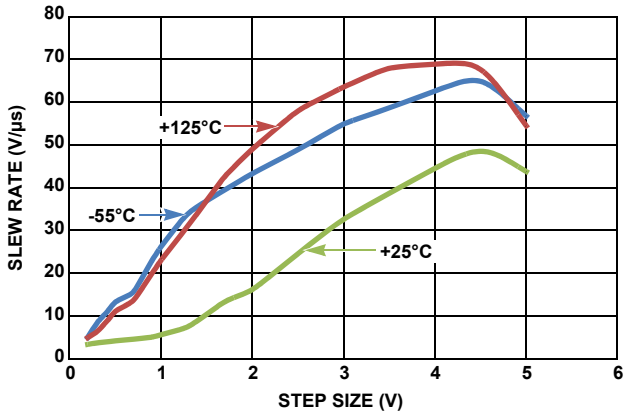


FIGURE 45. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±2.5V)

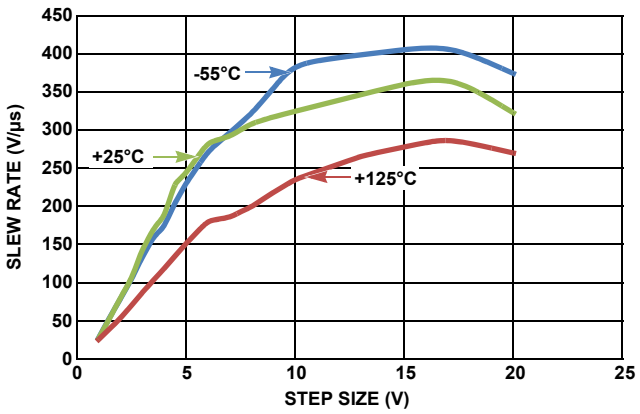


FIGURE 46. SLEW RATE vs STEP SIZE vs TEMPERATURE (V_S = ±18V)

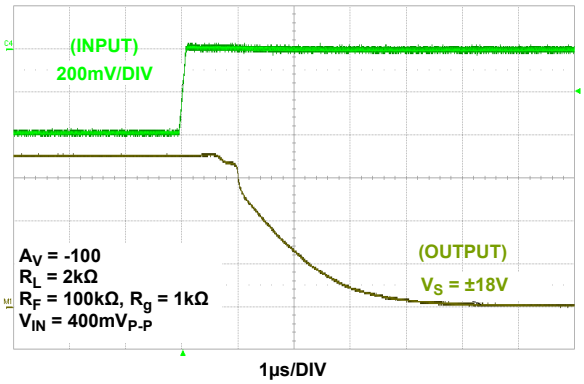


FIGURE 47. SATURATION RECOVERY (V_S = ±18V)

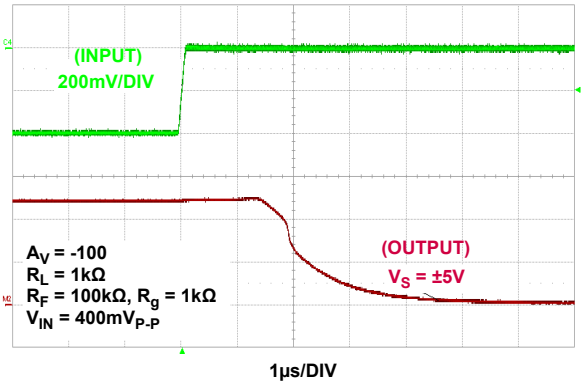


FIGURE 48. SATURATION RECOVERY (V_S = ±5V)

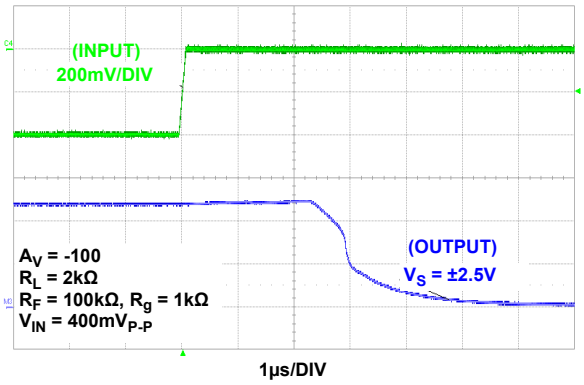


FIGURE 49. SATURATION RECOVERY (V_S = ±2.5V)

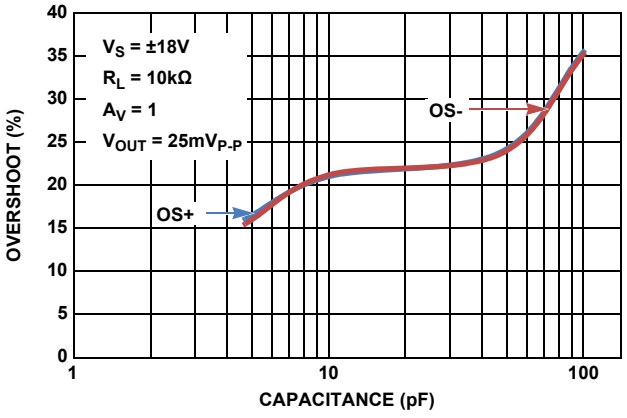


FIGURE 50. OVERSHOOT (%) vs LOAD CAPACITANCE

Typical Performance Curves Unless otherwise specified, $V_S \pm 18V$, $V_{CM} = 0V$, $V_O = 0V$, $T_A = +25°C$. **(Continued)**

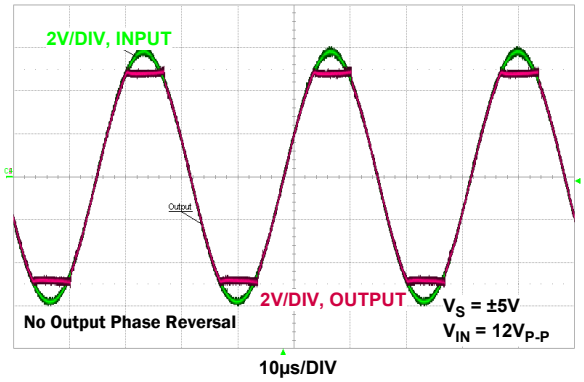


FIGURE 51. INPUT OVERDRIVE RESPONSE

Post High Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ± 19.8V, V_{CM} = 0V, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a high dose rate of 50rad(Si)/s to 300rad(Si)/s. (ISL70244SEH only) This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

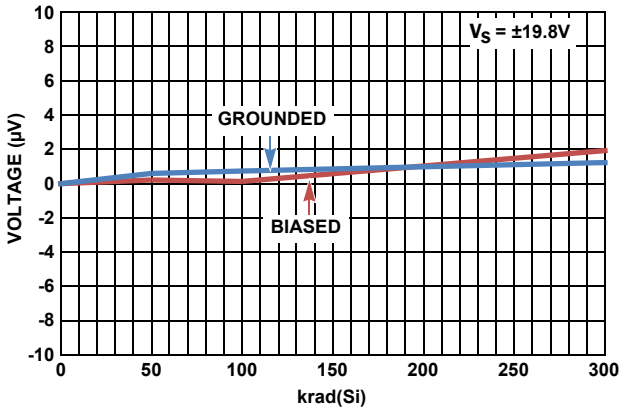


FIGURE 52. V_{OS} SHIFT vs HIGH DOSE RATE RADIATION

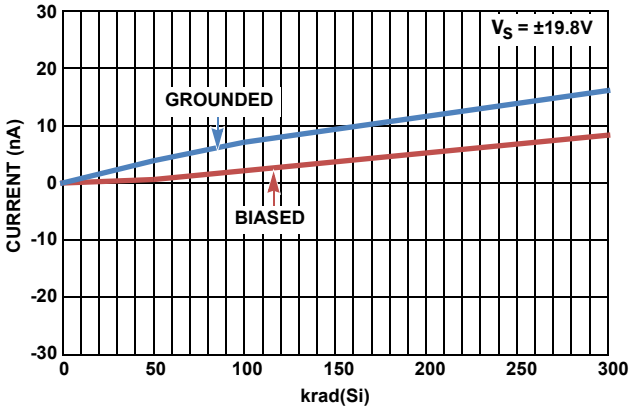


FIGURE 53. I_{BIAS+} SHIFT vs HIGH DOSE RATE RADIATION

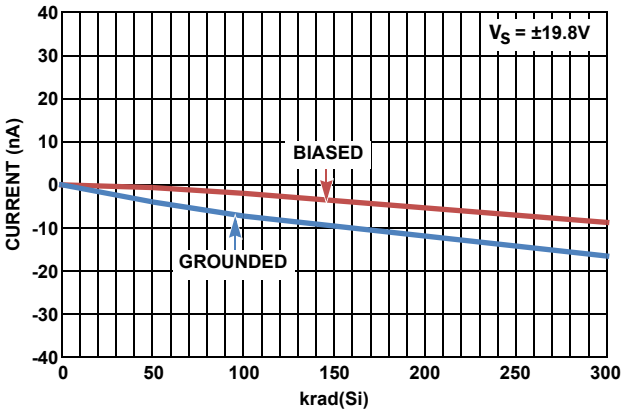


FIGURE 54. I_{BIAS-} SHIFT vs HIGH DOSE RATE RADIATION

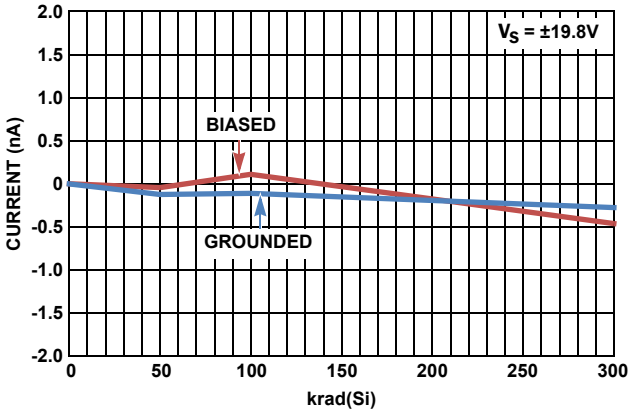


FIGURE 55. I_{OS} SHIFT vs HIGH DOSE RATE RADIATION

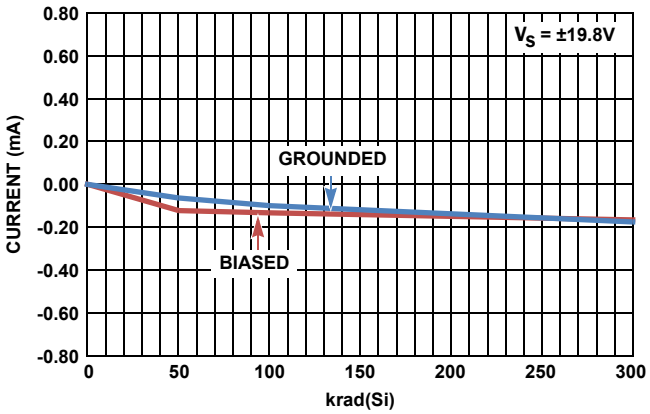


FIGURE 56. I+ vs HIGH DOSE RATE RADIATION

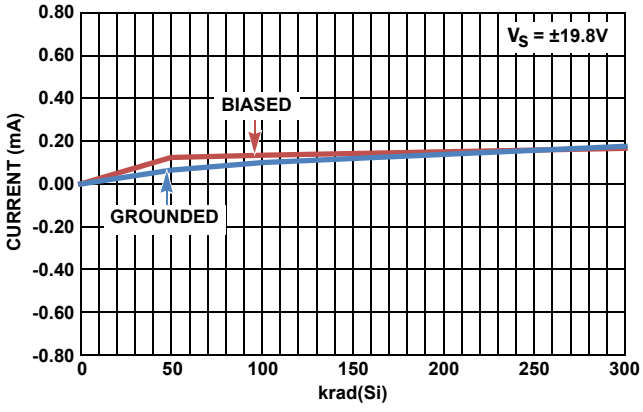


FIGURE 57. I- vs HIGH DOSE RATE RADIATION

Post Low Dose Rate Radiation Characteristics

Unless otherwise specified, V_S ± 19.8V, V_{CM} = 0, V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to high dose rate radiation. These are not limits nor are they guaranteed.

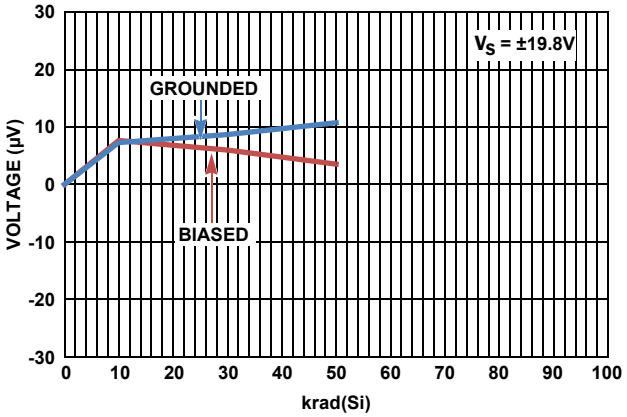


FIGURE 58. V_{OS} SHIFT vs LOW DOSE RATE RADIATION

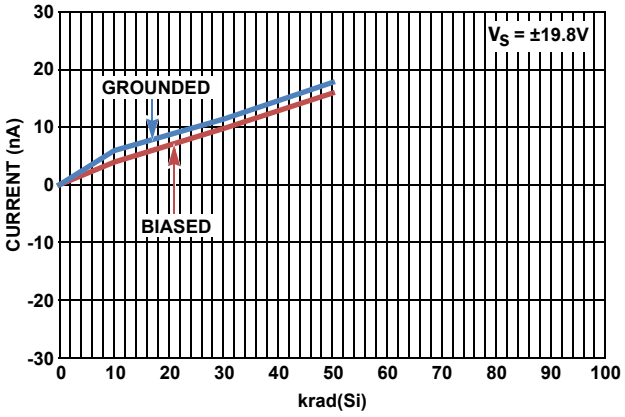


FIGURE 59. I_{BIAS+} vs LOW DOSE RATE RADIATION

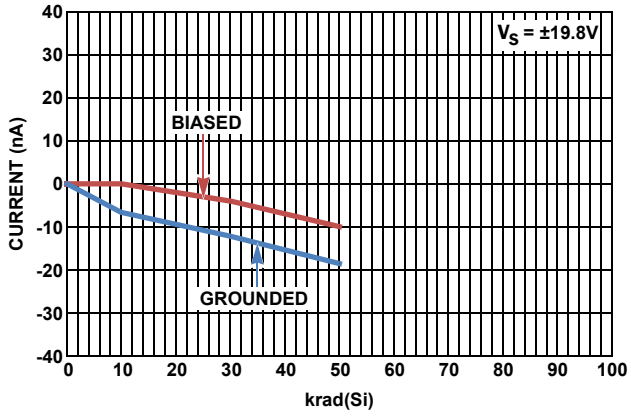


FIGURE 60. I_{BIAS-} vs LOW DOSE RATE RADIATION

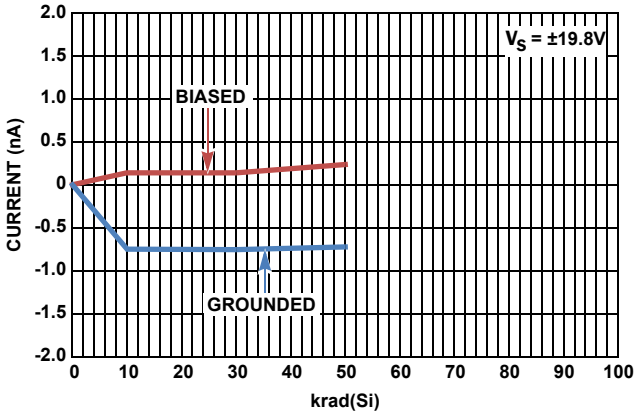


FIGURE 61. I_{OS} vs LOW DOSE RATE RADIATION

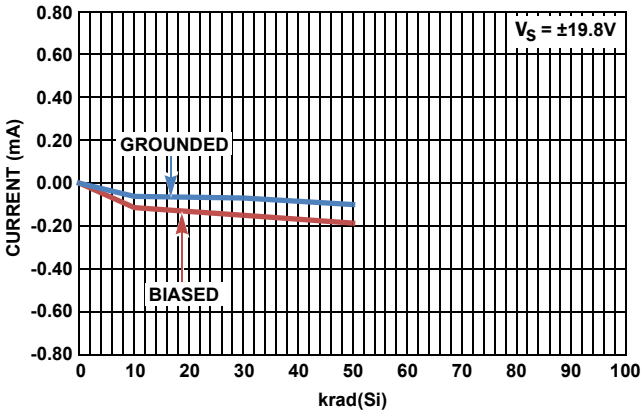


FIGURE 62. I^+ vs LOW DOSE RATE RADIATION

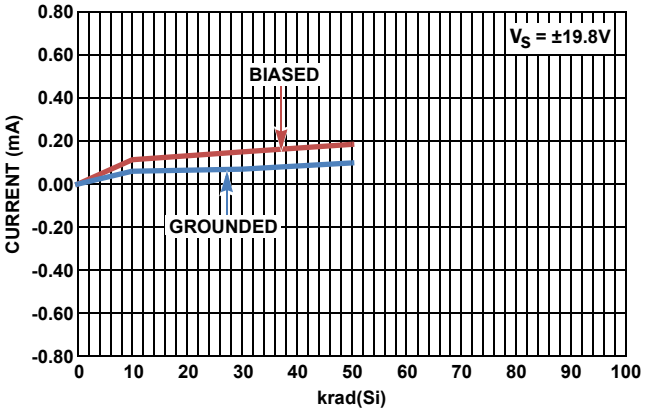


FIGURE 63. I^- vs LOW DOSE RATE RADIATION

Applications Information

Functional Description

The ISL7x244SEH contains two high speed, low power op amps designed to take advantage of the full dynamic input and output voltage range with rail-to-rail operation. By offering low power, low offset voltage and low temperature drift coupled with its high bandwidth and enhanced slew rates upwards of 50V/µs, these op amps are ideal for applications requiring both high DC accuracy and AC performance. The ISL7x244SEH is manufactured in the Renesas PR40 silicon-on-insulator process, which makes this device immune to single-event latch-up and provides excellent radiation tolerance. The ISL7x244SEH is the ideal choice for high reliability applications in harsh radiation-prone environments.

Operating Voltage Range

The device is designed to operate with a split supply rail from ±1.35V to ±20V or a single supply rail from 2.7V to 40V. The ISL7x244SEH is fully characterized in production for supply rails of 5V (±2.5V) and 36V (±18V). The power supply rejection ratio is typically 120dB with a nominal ±18V supply. The worst case Common-Mode Rejection Ratio (CMRR) over-temperature is within 1.5V to 2V of each rail. When V_{CM} is inside this range, the CMRR performance is typically >110dB with ±18V supplies. The minimum CMRR performance over the -55°C to +125°C temperature range and radiation is >70dB over the full common-mode input range for power supply voltages from ±2.5V (5V) to ±18V (36V).

Input Performance

The slew enhanced front end is a block that is placed in parallel with the main input stage and functions based on the input differential voltage.

Input ESD Diode Protection

The input terminals (IN+ and IN-) have internal ESD protection diodes to the positive and negative supply rails, series connected 600Ω current limiting resistors, and an anti-parallel diode pair across the inputs.

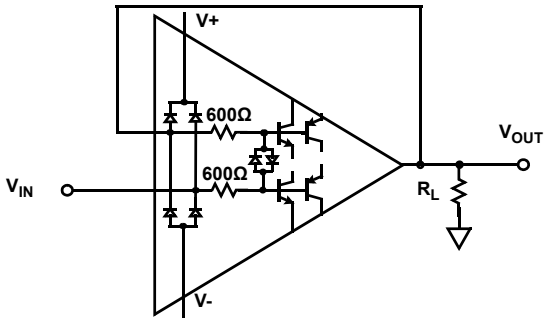


FIGURE 64. INPUT ESD DIODE CURRENT LIMITING, UNITY GAIN

Output Short-Circuit Current Limiting

The output current limit has a worst case minimum limit of ±8mA but may reach as high as ±100mA. The op amp can withstand a short-circuit to either rail for a short duration (<1s) as long as the maximum operating junction temperature is not violated. This applies to only one amplifier at a time. Continued use of the device in these conditions can degrade the long term reliability of the part and is not recommended. Figure 20 on page 10 shows the typical short-circuit currents that can be expected. The ISL7x244SEH's current limiting circuitry automatically lowers the current limit of the device if short-circuit conditions carry on for extended periods of time in an effort to protect itself from malfunction. However, extended operation in this mode degrades the output rail-to-rail performance by pulling V_{OH}/V_{OL} away from the rails.

Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL7x244SEH is immune to output phase reversal, even when the input voltage is 1V beyond the supplies. This is illustrated in Figure 51 on page 16.

Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package type need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

$$T_{JMAX} = T_{MAX} + \theta_{JA} \times PD_{MAXTOTAL} \quad \text{(EQ. 1)}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})

Calculate PD_{MAX} for each amplifier using Equation 2:

$$PPD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L} \quad \text{(EQ. 2)}$$

where:

- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package
- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application

Slew Rate Enhancement

The ISL7x244SEH has a slew enhanced front end that increases the drive on the output transistors proportional to the differential voltage across the inputs. This increase in output drive shows up as increased transient current on top of the op amp's steady state supply current. If the voltage differential between the inputs remains constant, as in comparator applications, the added drive current to the output transistors becomes steady state and increases the DC power supply current of the IC. For this reason, Renesas recommends not using the ISL7x244SEH in a comparator configuration.

Unused Channel Configuration

If the application does not require the use of all four op amps, you must configure the unused channels to prevent them from oscillating. Any unused channels oscillate if the input and output pins are floating. Oscillation results in higher than expected supply currents and possible noise injection into any of the active channels being used. To prevent oscillation, short the output to the inverting input and tie the positive input to a known voltage, such as mid-supply.

When the V^- supply is less than or equal to -1.0V, configure your op amp as in Figure 65, otherwise follow the configuration shown in Figure 66. The resistors in Figure 66 are of equal value and high resistance (≥10kΩ) to minimize current draw while keeping the positive input at mid-supply. All unused op amps can have their inputs tied to the same resistor divider to minimize the number of components.

Tying the positive input to ground in Figure 66 (where V^- = GND) produces a voltage differential across the inputs because the inverting input would be at the op amp's V_{OL} and the positive input would be at GND, which increases the steady state supply current. Although increased supply current does not damage the op amp, it results in additional unnecessary power dissipation.

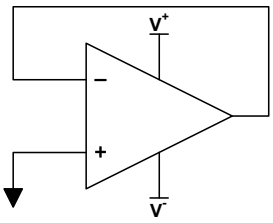


FIGURE 65. PREVENTING OSCILLATIONS IN UNUSED CHANNELS, SPLIT SUPPLY

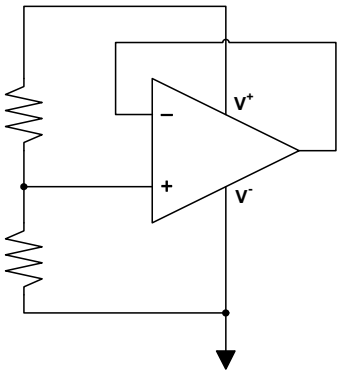


FIGURE 66. PREVENTING OSCILLATIONS IN UNUSED CHANNELS, SINGLE SUPPLY

Die Characteristics

Die Dimensions

2410µm x 1961µm (95 mils x 77 mils)
Thickness: 483µm ±25µm (19 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Nitrox
Thickness: 15kÅ

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
Thickness: 30kÅ

BACKSIDE FINISH

Silicon

PROCESS

PR40

Assembly Related Information

SUBSTRATE POTENTIAL

Floating

Additional Information

WORST CASE CURRENT DENSITY

$<2x10^5 A/cm^2$

TRANSISTOR COUNT

365

Weight of Packaged Device

0.3958 grams (typical)

Lid Characteristics

Finish: Gold
Potential: Unbiased, tied to package Pin 6
Case Isolation to Any Lead: $20x10^9$ Ω (minimum)

Metallization Mask Layout

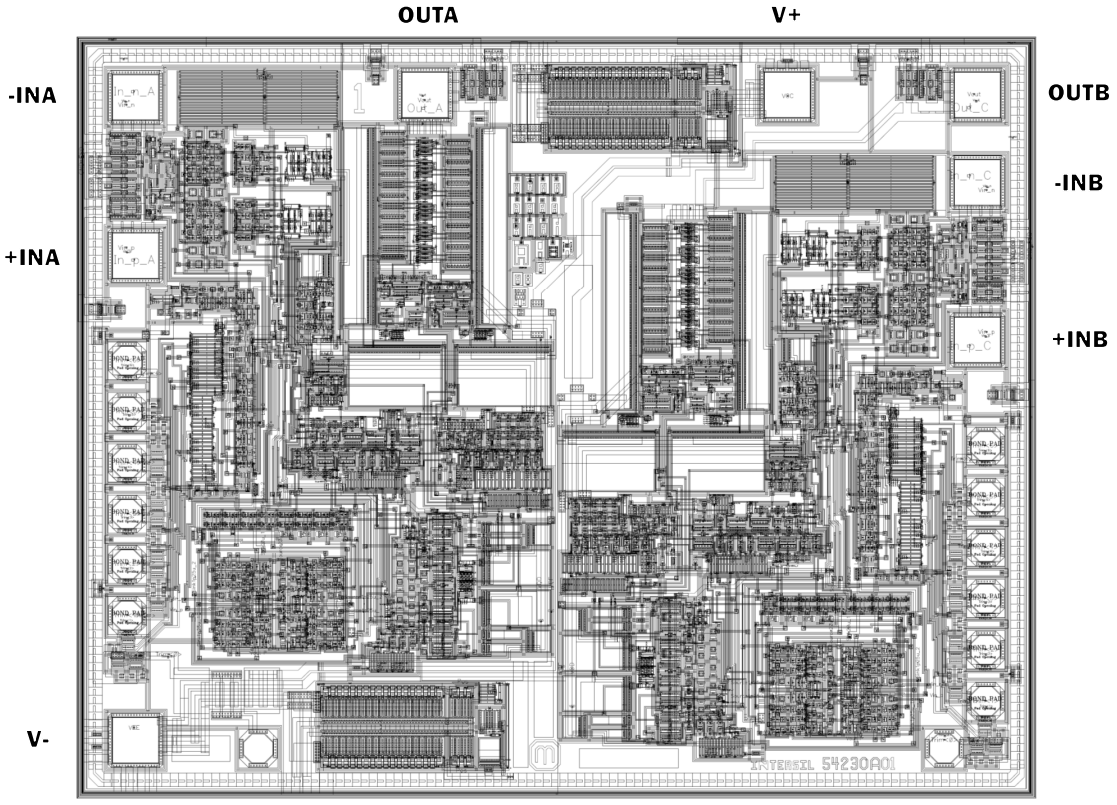


TABLE 1. DIE LAYOUT X-Y COORDINATES

PAD NAME	PAD NUMBER	X (µm)	Y (µm)	dX (µm)	dY (µm)	BOND WIRES PER PAD
OUTB	1	1015.5	664.0	110	110	1
V+	2	557.0	664.0	110	110	1
OUTA	3	-317.0	664.0	110	110	1
-INA	4	-1015.5	658.0	110	110	1
+INA	5	-1015.5	270.5	110	110	1
V-	12	-1015.5	-918.0	110	110	1
+INB	21	1015.5	62.0	110	110	1
-INB	22	1015.5	449.5	110	110	1

NOTE:

10. Origin of coordinates is the centroid of the die.

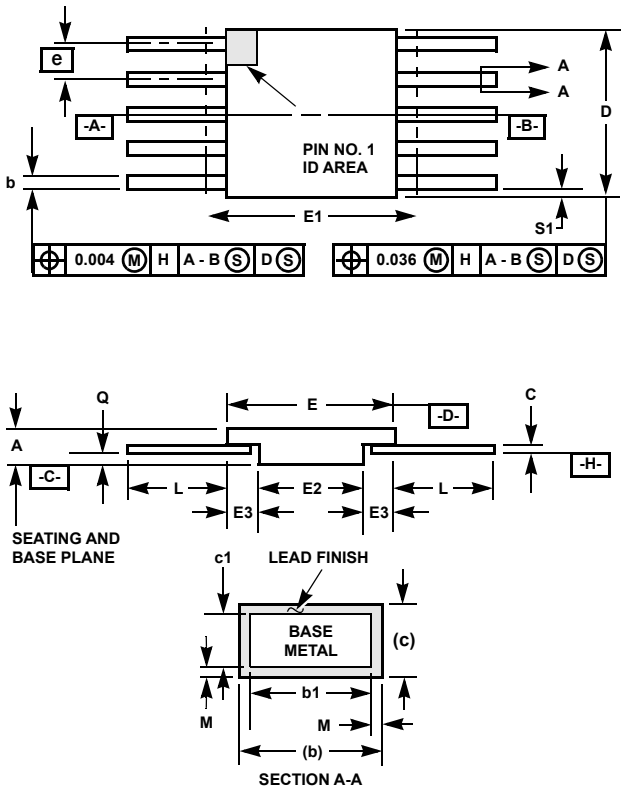
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, however, not warranted. Visit our website to make sure that you have the latest revision.

DATE	REVISION	CHANGE
Dec 2, 2020	5.00	Updated Note 3 and added Note 4. Updated Power Supply Rejection Ratio typical from 128 to 143 in the ±19.8V EC specification table. Updated Power Supply Rejection Ratio typical from 123 to 135 in the ±2.5V EC specification table. Added Figures 35 and 36. Updated Figure 37.
Aug 16, 2019	4.00	Added information about the ISL73244SEH throughout the datasheet. Updated SEE and TID ratings in Features section. Added radiation levels to ordering information table. Updated links throughout datasheet and updated disclaimer.
Feb 23, 2018	3.00	Updated Related Literature. Added Notes 3 and 5. Added “Slew Rate Enhancement” on page 19. Updated “Unused Channel Configuration” on page 20. Removed the About Intersil section and updated the disclaimer.
Sep 1, 2016	2.00	Updated x-axis and y-axis label on Figure 2 on page 1. Updated Note 2.
Jun 12, 2015	1.00	Updated Related Literature Section on page 1. In the Ordering Information Table on page 3, updated FG name from “ISL70244SEHVX/SAMPLE and ISL70244SEHF/SAMPLE” to ISL70244SEHX/SAMPLE.
Sep 22, 2014	0.00	Initial release

Package Outline Drawing

For the most recent package outline drawing, see K10.A.



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, CONFIGURATION B)
10 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

Rev. 0 3/07

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

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