

# ISL71040M

## Radiation Tolerant Low-Side GaN FET Driver

The ISL71040M is a low-side driver designed to drive enhancement mode Gallium Nitride (GaN) FETs in isolated topologies and boost type configurations. The ISL71040M operates with a supply voltage from 4.5V to 13.2V and has both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drives with a single device.

The ISL71040M has a 4.5V gate drive voltage ( $V_{DRV}$ ) generated using an internal regulator that prevents the gate voltage from exceeding the maximum gate-source rating of enhancement mode GaN FETs. The gate drive voltage features an Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps OUTL turned on to ensure the GaN FET is in an OFF state whenever  $V_{DRV}$  is below the UVLO threshold.

The ISL71040M inputs can withstand voltages up to 14.7V regardless of the  $V_{DD}$  voltage, which allows the inputs to be connected directly to most PWM controllers. The ISL71040M's split outputs offer the flexibility to adjust the turn-on and turn-off speed independently by adding additional impedance to the turn-on and turn-off paths.

The ISL71040M operates across the military temperature range from -55°C to +125°C and is offered in an 8 Ld Thin Dual Flat No-Lead (TDFN) plastic package.

### Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Wide operating voltage range of 4.5V to 13.2V
- Up to 14.7V logic inputs (regardless of  $V_{DD}$  level)
  - Inverting and non-inverting inputs
- Optimized to drive enhancement mode GaN FETs
  - Internal 4.5V regulated gate drive voltage
  - Independent outputs for adjustable turn-on/turn-off speeds
- NiPdAu-Ag Lead finish (Sn-free, Pb-free)
- Moisture Sensitivity Level (MSL) Rating: 1
- Passes NASA Low Outgassing Specifications
- Full military temperature range operation
  - $T_A = -55^\circ\text{C}$  to  $+125^\circ\text{C}$
  - $T_J = -55^\circ\text{C}$  to  $+150^\circ\text{C}$
- TID Radiation Lot Acceptance Testing (LDR:  $<0.01\text{rad}(\text{Si})/\text{s}$ )
  - ISL71040M30RTZ: 30krad(Si)
  - ISL71040M50RTZ: 50krad(Si)
- SEE Characterization
  - No DSEE with  $V_{DD} = 16.5\text{V}$  at  $43\text{MeV}\cdot\text{cm}^2/\text{mg}$
  - $\text{SET} \leq 15\mu\text{m}^2$  at  $43\text{MeV}\cdot\text{cm}^2/\text{mg}$

### Applications

- Flyback and forward converters
- Boost and PFC converters
- Secondary synchronous FET drivers

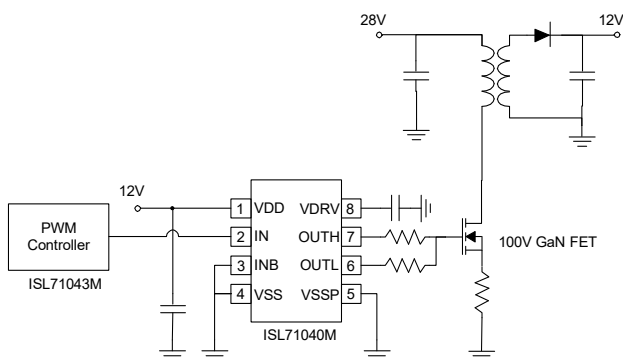


Figure 1. Typical Flyback Power Supply Application

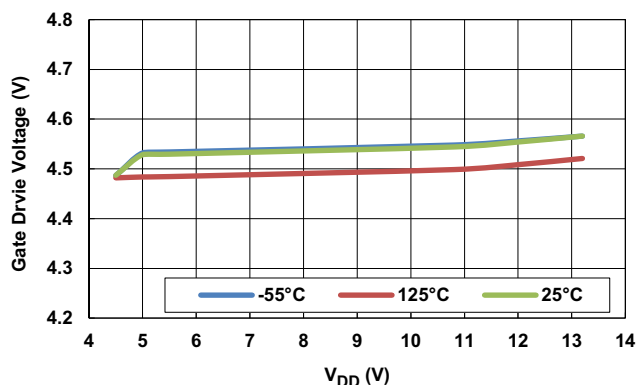


Figure 2.  $V_{DRV}$  Line Regulation vs Temperature

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# 1. Overview

## 1.1 Block Diagram

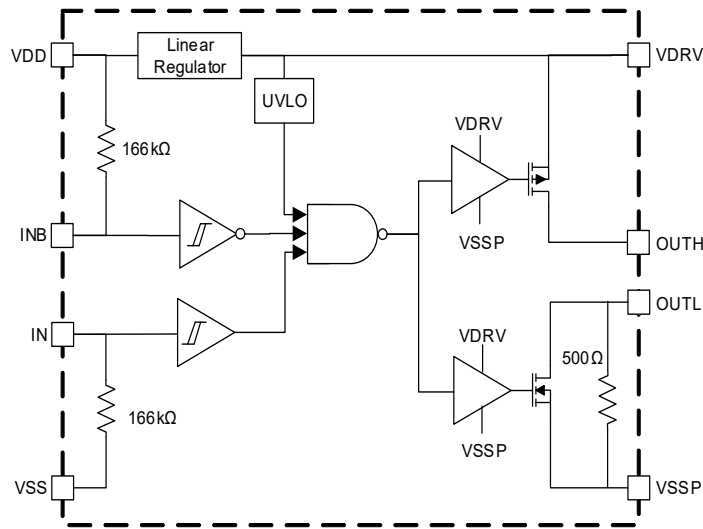


Figure 3. Block Diagram

# 2. Pin Information

## 2.1 Pin Assignments

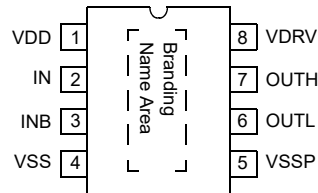


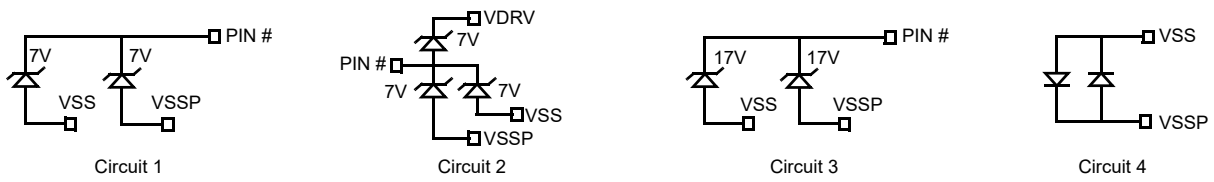
Figure 4. Pin Assignments - Top View

## 2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	VDD	3	Supply for the ISL71040M internal linear regulator. Locally bypass the supply to VDD using at least a 4.7µF ceramic capacitor.
2	IN	3	Non-inverting input pin that controls the OUTH and OUTL outputs. This input has TTL/CMOS type thresholds. When using the ISL71040M in an inverting application, tie this pin to VDD to enable the outputs.
3	INB	3	Inverting input pin that controls the OUTH and OUTL outputs. This input has TTL/CMOS type thresholds. When using the ISL71040M in a non-inverting application, tie this pin to VSS to enable the outputs.
4	VSS	4	Supply ground. Connect this pin to VSSP from the PCB ground plane.
5	VSSP	4	Power supply ground. Connect this pin to VSS from the PCB ground plane.

Pin Number	Pin Name	ESD Circuit	Description
6	OUTL	2	Output low pin that is the gate driver turn-off output. Connect this pin to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-off speed.
7	OUTH	1	Output high pin that is the gate driver turn-on output. Connect this pin to the gate of the GaN FET with a short, low inductance path. A series gate resistor can be used to adjust the turn-on speed.
8	VDRV	1	Internal linear regulator output and the gate drive voltage. Locally bypass this pin using at least a 4.7μF ceramic capacitor; 2μF to 10μF with variability.
-	EPAD	4	The exposed pad should be connected externally to VSSP. Put as many vias as possible in this pad connecting to other PCB layers to improve heat dissipation.

**ESD Circuits:**



### 3. Specifications

#### 3.1 Absolute Maximum Ratings

**Caution:** Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
V <sub>DD</sub>	-0.3	+16.5	V
IN, INB	-0.3	+16.5	V
OUTL, OUTH, VDRV	-0.3	+6.5	V
V <sub>DD</sub> <sup>[1]</sup>	-0.3	+16.5	V
IN, INB <sup>[1]</sup>	-0.3	+16.5	V
OUTL, OUTH, VDRV <sup>[1]</sup>	-0.3	+6.2	V
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2017)	-	8	kV
Charged Device Model (Tested per JS-002-2014)	-	2	kV
Latch Up (Tested per JESD-78E; Class 2, Level A) at 125°C	-	100	mA

1. Tested in a heavy ion environment at LET = 43MeV•cm<sup>2</sup>/mg at +125°C (TC) for SEB.

#### 3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Case Operating Temperature Range	-55	+125	°C
V <sub>DD</sub>	4.5	13.2	V
IN, INB	4.5	13.2	V

#### 3.3 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost <sup>[1]</sup>	0.05	%
Collected Volatile Condensable Material <sup>[1]</sup>	<0.01	%
Water Vapor Recovered	0.03	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensable material of <0.1%.

#### 3.4 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld TDFN Package	$\theta_{JA}$ <sup>[1]</sup>	Junction to ambient	40	°C/W
		$\theta_{JC}$ <sup>[2]</sup>	Junction to case	2	°C/W

1.  $\theta_{JA}$  is measured with the component mounted on a high-effective thermal conductivity test board with direct attach features in free air. See [IB379](#).

2. For  $\theta_{JC}$ , the case temperature location is the center of the package underside.

### 3.5 Electrical Specifications

$V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V, r_{OUTH} = r_{OUTL} = 0\Omega$ , no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71040M30RTZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71040M50RTZ).**

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup>	Max <sup>[1]</sup>	Unit
<b>Power Supply</b>						
Quiescent Supply Current	$I_{DDQ}$	$V_{DD} = 4.5V, IN = 0V, INB = V_{DD}$	-	1.4	<b>2.7</b>	mA
		$V_{DD} = 13.2V, IN = 0V, INB = V_{DD}$	-	1.5	<b>2.7</b>	mA
Operating Supply Current	$I_{DDO}$	$V_{DD} = 4.5V, f_{PWM} = 500kHz$	-	6.8	<b>13</b>	mA
		$V_{DD} = 13.2V, f_{PWM} = 500kHz$	-	7.3	<b>15</b>	mA
<b>Gate Drive Voltage</b>						
Output Voltage	$V_{DRV}$	$V_{DD} = 4.5V$	<b>4.29</b>	4.44	-	V
		$V_{DD} = 13.2V$	<b>4.34</b>	4.59	<b>4.76</b>	V
Current Limit of $V_{DRV}$	$I_{LIM}$	$V_{DD} = 4.5V, 13.2V$	<b>50</b>	140	<b>300</b>	mA
<b>Undervoltage Lockout (UVLO) on <math>V_{DRV}</math></b>						
UVLO Rising Threshold	$V_{RDRV}$		<b>3.75</b>	3.98	<b>4.15</b>	V
UVLO Falling Threshold	$V_{FDRV}$		<b>3.40</b>	3.74	<b>4.00</b>	V
UVLO Hysteresis	$V_{HDRV}$		<b>100</b>	238	<b>375</b>	mV
<b>Input Pins</b>						
High Level Threshold	$V_{IH}$		-	1.7	<b>2.0</b>	V
Low Level Threshold	$V_{IL}$		<b>1.0</b>	1.4	-	V
Input Hysteresis	$V_{IHYS}$		<b>120</b>	290	<b>450</b>	mV
Pull-Up/Down Resistor	$R_{INU/D}$	IN to $V_{SS}$ , INB to $V_{DD}$	<b>97</b>	166	<b>362</b>	k $\Omega$
Input Leakage Current	$I_{IN/INB}$		<b>-1</b>	-	<b>1</b>	$\mu A$
<b>OUTH Output</b>						
Peak Source Current <sup>[3]</sup>	$I_{SRC}$	$C_L = 220nF$ (Figure 6)	<b>1</b>	1.5	<b>3</b>	A
Driver Output Resistance	$r_{ONP}$	$I_{OUTH} = 45mA$	-	2.2	<b>3.2</b>	$\Omega$
Output Leakage Current	$I_{LKP}$	OUTH = 0V, 4.5V	<b>-1</b>	-	<b>1</b>	$\mu A$
<b>OUTL Output</b>						
Peak Sink Current <sup>[3]</sup>	$I_{SNK}$	$C_L = 220nF$ (Figure 6)	<b>1.5</b>	2.8	<b>4</b>	A
Driver Output Resistance	$r_{ONN}$	OUTH = $V_{DRV}$ , $I_{OUTL} = -45mA$	-	0.5	<b>1</b>	$\Omega$
		OUTH = OUTL, $I_{OUTL} = -45mA$	-	1.7	<b>3</b>	$\Omega$
Gate Hold-Off Resistance	$r_{OUTL-P}$	$V_{DD} = 0V, OUTL = 0.7V$	<b>400</b>	520	<b>700</b>	$\Omega$
<b>Switching Characteristics</b>						
Turn-On Propagation Delay	$t_{DON}$	$C_L = 1000pF$ (Figure 5)	<b>15</b>	40	<b>65</b>	ns
Turn-Off Propagation Delay	$t_{DOFF}$	$C_L = 1000pF$ (Figure 5)	<b>15</b>	39	<b>65</b>	ns
Propagation Delay Matching	$t_{DM}$	$ t_{DON} - t_{DOFF} $	<b>-10</b>	1	<b>10</b>	ns

$V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V, r_{OUTH} = r_{OUTL} = 0\Omega$ , no load on OUTH/OUTL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71040M30RTZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71040M50RTZ).** (Cont.)

Parameter	Symbol	Test Conditions	Min <sup>[1]</sup>	Typ <sup>[2]</sup>	Max <sup>[1]</sup>	Unit
Rise Time (10% to 90%) <sup>[3]</sup>	$t_{RISE}$	$C_L = 200pF$	-	6	-	ns
		$C_L = 1500pF$	-	13	-	ns
		$C_L = 10000pF$	<b>21</b>	60	<b>90</b>	ns
Fall Time (90% to 10%) <sup>[3]</sup>	$t_{FALL}$	$C_L = 200pF$	-	4.5	-	ns
		$C_L = 1500pF$	-	8	-	ns
		$C_L = 10000pF$	<b>16</b>	35	<b>60</b>	ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. Typical values shown are not guaranteed.
3. Test applies only to packaged parts due to hardware limitations at wafer probe.

### 3.6 Timing Diagrams

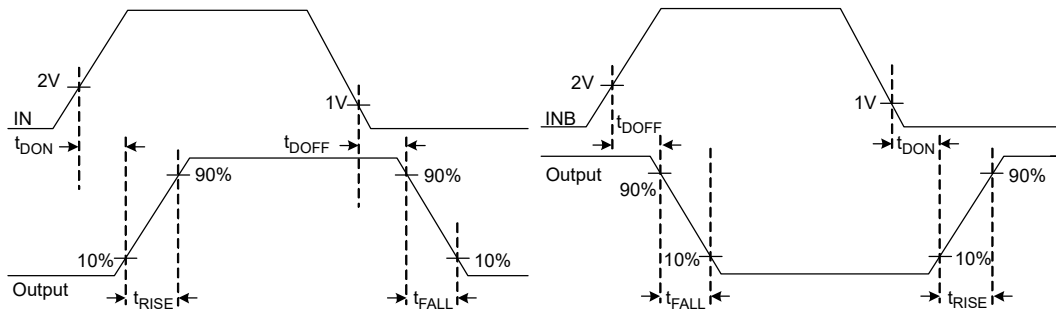


Figure 5. Timing Diagram, OUTH and OUTL Tied Together

$$i_{peak} = 220nF \times \frac{\Delta V}{\Delta t}$$

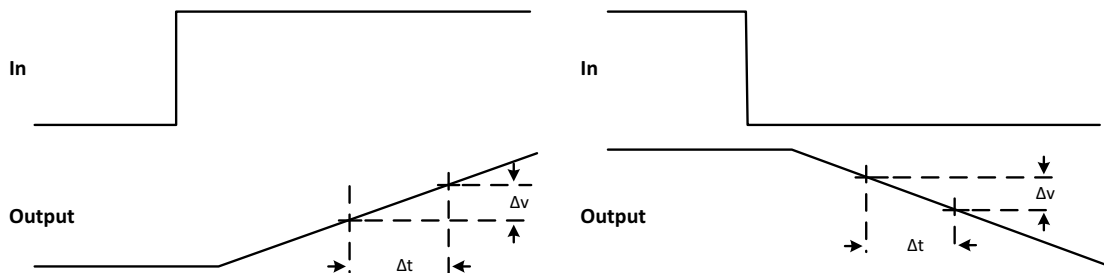


Figure 6. Peak Source/Sink Measurement

## 4. Typical Performance Curves

Unless otherwise noted,  $V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V,$  no load on OUTH/OUTL,  $r_{OUTH} = r_{OUTL} = 0\Omega$ .

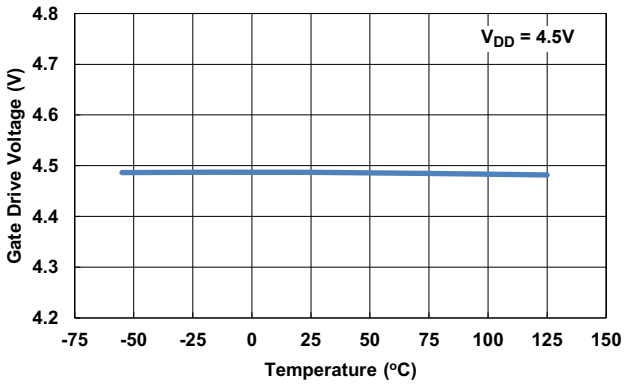


Figure 7.  $V_{DRV}$  vs Temperature

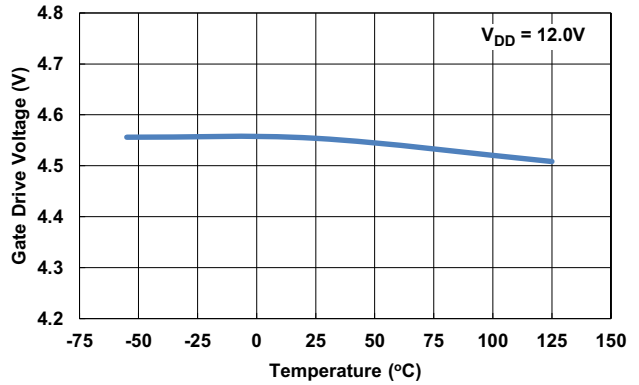


Figure 8.  $V_{DRV}$  vs Temperature

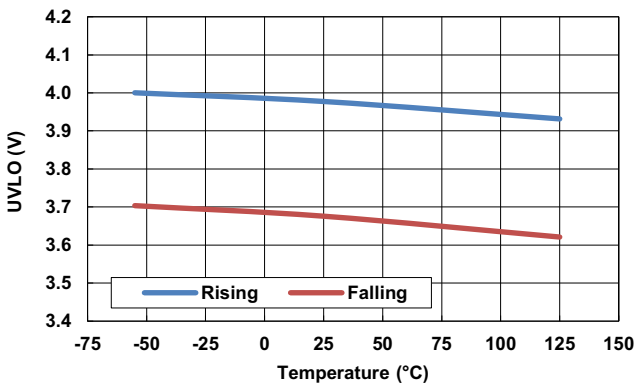


Figure 9.  $V_{DRV}$  Undervoltage Lockout Threshold

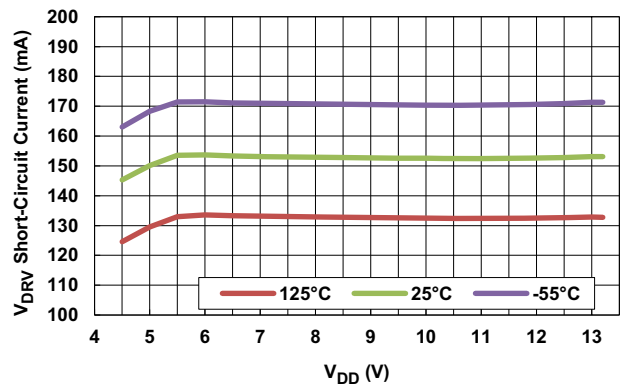


Figure 10.  $V_{DRV}$  Short-Circuit Current vs Temperature

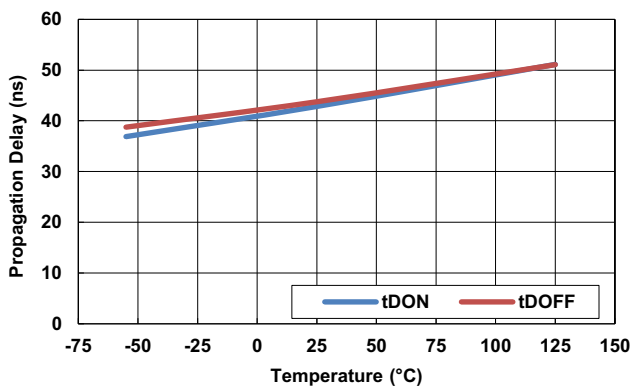


Figure 11. Input Propagation Delay vs Temperature

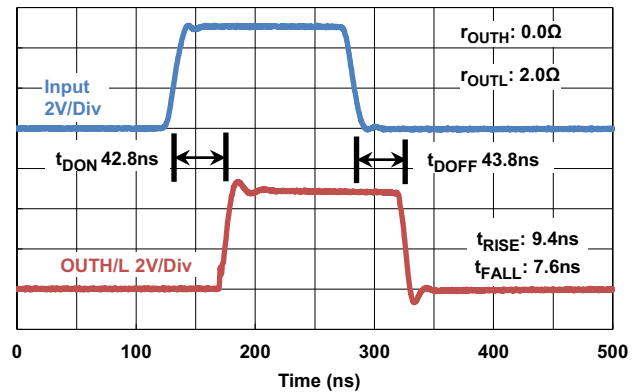


Figure 12. Input Propagation Delay



Unless otherwise noted,  $V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V$ , no load on OUTH/OUTL,  $r_{OUTH} = r_{OUTL} = 0\Omega$ . (Cont.)

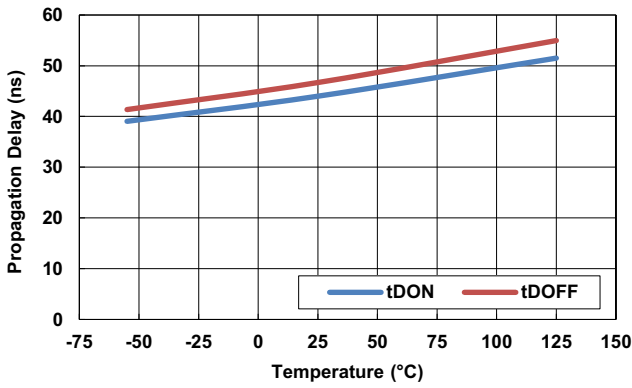


Figure 13. Input Bar Propagation Delay vs Temperature

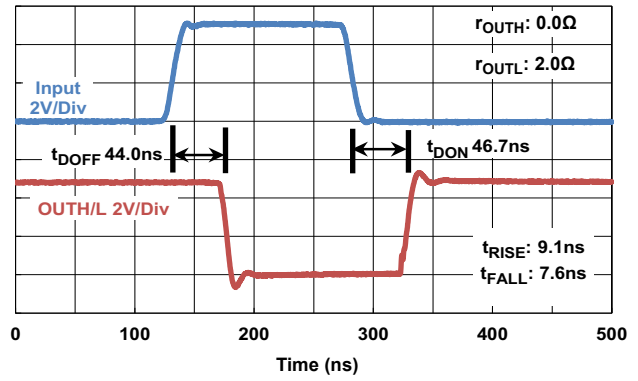


Figure 14. Input Bar Propagation Delay

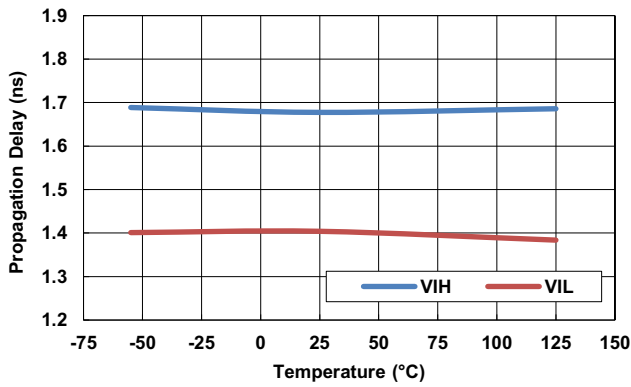


Figure 15. Input Logic Threshold vs Temperature

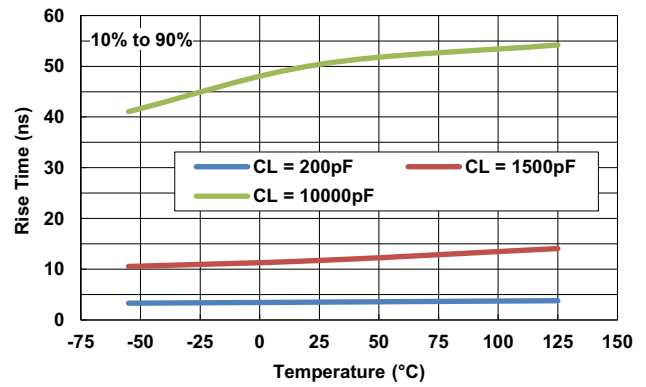


Figure 16. Output Rise Times vs Temperature

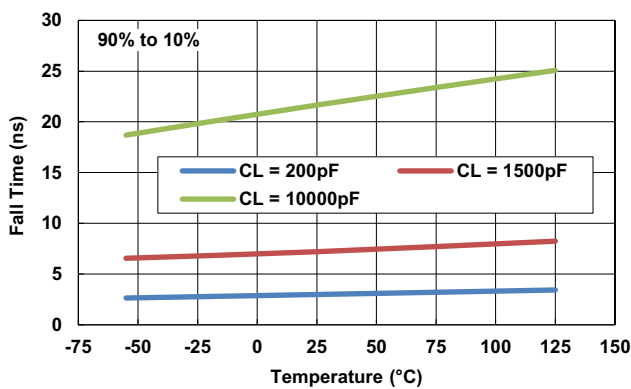


Figure 17. Output Fall Times vs Temperature

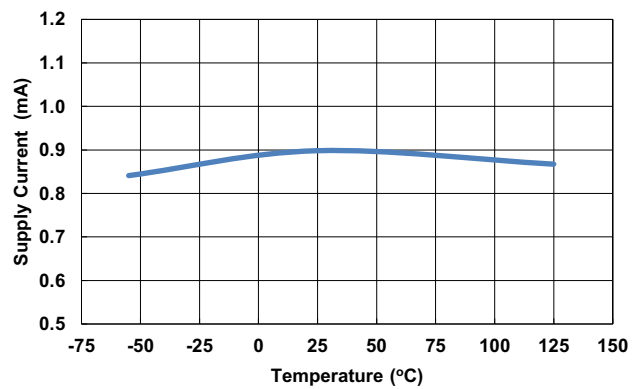


Figure 18. Quiescent Supply Current vs Temperature

Unless otherwise noted,  $V_{DD} = 4.5V, 13.2V$ ,  $V_{SS} = V_{SSP} = 0V$ ,  $C_{VDRV} = 4.7\mu F$ ,  $V_{IH} = 5.0V$ ,  $V_{IL} = 0V$ , no load on OUTH/OUTL,  $r_{OUTH} = r_{OUTL} = 0\Omega$ . (Cont.)

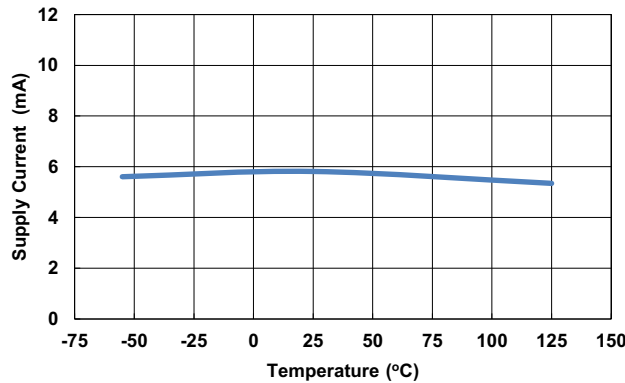


Figure 19. Operating Supply Current

## 5. Functional Description

### 5.1 Gate Drive for Enhancement N-Channel GaN FETs

New technologies based on wide-band gap semiconductors produce High Electron Mobility Transistors (HEMT). An example of a HEMT is the GaN based power transistors such as the EPC2019 and EPC2022, which offer very low  $r_{DS(ON)}$  and gate charge (Qg). These attributes make the devices capable of supporting very high switching frequency operation without suffering significant efficiency loss. However, GaN power FETs have special gate drive requirements that the ISL71040M is specifically designed to address.

The following are key properties of a gate driver for GaN FETs:

- Gate drive signals need to be sufficiently higher than the  $V_{GS}$  threshold specified in GaN FET datasheets for proper operation
- A well regulated gate drive voltage keeps the  $V_{GS}$  lower than the specified absolute maximum level of 6V
- Split pull-up and pull-down gate connections add series gate resistors to independently adjust turn-on and turn-off speed without the need for a series diode with a voltage drop that may cause an insufficient gate drive voltage
- Driver pull-down resistance  $<0.5\Omega$  (typical) eliminates undesired Miller turn-on
- High current source/sink capability and low propagation delay achieves high switching frequency operation

### 5.2 Functional Overview

The ISL71040M is a single channel high speed enhancement mode GaN FET low-side driver for isolated power supplies and Synchronous Rectifier (SR) applications.

The ISL71040M has a wide operating supply range of 4.5V to 13.2V. The gate drive voltage is generated from an internal linear regulator to keep the gate-to-source voltage below the absolute maximum level of 6V for the EPC2019 and EPC2022 GaN FET devices.

The input stage can handle inputs to the 14.7V independent of  $V_{DD}$  and has both inverting and non-inverting inputs. The split output stage can source and sink high currents and allows for independent tuning of the turn-on and turn-off times. The typical propagation delay of 40ns enables high switching frequency operation.

## 6. Applications Information

### 6.1 Undervoltage Lockout

The VDD pin accepts a recommended supply voltage range of 4.5V to 13.2V and is the input to the internal linear regulator. VDRV is the output of the regulator and is equal to 4.5V. VDRV provides the bias for all internal circuitry and the gate drive voltage for the output stage.

An UVLO circuitry monitors the voltage on VDRV and is designed to prevent unexpected glitches when VDD is being turned on or turned off. When  $VDRV < \sim 1V$ , an internal 500Ω resistor connected between OUTL and ground helps keep the gate voltage close to ground. When  $\sim 1.2V < VDRV < UVLO$ , OUTL is driven low while ignoring the logic inputs, and OUTH is in a high impedance state. The low state has the same current sinking capacity as during normal operation. This ensures that the driven FETs are held off even if there is a switching voltage on the drains that can inject charge into the gates from the Miller capacitance.

When  $VDRV > UVLO$ , the output starts to respond to the logic inputs following the next rising edge on IN or falling edge on INB. In the non-inverting operation (PWM signal applied to the IN pin) the output is in phase with the input. In the inverting operation (PWM signal applied to the INB pin), the output is out of phase with the input.

For the negative transition of  $V_{DD}$  through the UV lockout voltage, when  $VDRV < \sim 3.7V_{DC}$ , the OUTL is active low and OUTH is high impedance, regardless of the input logic states.

### 6.2 Input Stage

The ISL71040M input thresholds are based on a TTL and CMOS compatible input threshold logic that is independent of the supply voltage. With typical high threshold = 1.7V and typical low threshold = 1.4V, the logic level thresholds can be conveniently driven with PWM control signals derived from 3.3V and 5V power controllers.

The ISL71040M offers both inverting and non-inverting inputs. The state of the output pin is dependent on the bias on both input pins. [Table 1](#) summarizes the inputs to output relation.

**Table 1. Truth Table<sup>[1]</sup>**

IN	INB	OUT	OUTH	OUTL
0	0	0	Hi-Z	0
0	1	0	Hi-Z	0
1	0	1	1	Hi-Z
1	1	0	Hi-Z	0

1. OUT is the combination of OUTH and OUTL connected together. Hi-Z represents a high impedance state.

As a protection mechanism, if any of the input pins are left in a floating condition, OUTL is held in the low state and OUTH is high impedance. This state is achieved using a 300kΩ pull-up resistor on the INB pin to VDD and a 300kΩ pull-down resistor on the IN pin to VSS. For proper operation in non-inverting applications, connect INB to VSS. For proper operation in inverting applications, connect IN to VDD.

### 6.3 Enable Function

Use the unused input pin to enable and disable the ISL71040M. The following guidelines describe how to implement the enable/disable function:

- In a non-inverting configuration, the INB pin can be used to implement the enable/disable function. OUT is enabled when INB is biased low, acting as an active low enable pin.
- In an inverting configuration, the IN pin can be used to implement the enable and disable function. OUT is enabled when IN is biased high, acting as an active high enable pin.

## 6.4 Driver Power Dissipation

The ISL71040M power dissipation is dominated by the losses associated with the gate charge of the driven bridge FETs and the switching frequency. The internal bias current also contributes to the total dissipation but is usually not significant compared to the gate charge losses.

For example, the EPC2022 has a total gate charge of 13nC when  $V_{DS} = 100V$  and  $V_{GS} = 4.5V$ . This is the charge that a driver must source to turn on the GaN FET and must sink to turn off the GaN FET.

Use [Equation 1](#) to calculate the power dissipation of the driver:

$$(EQ. 1) \quad P_D = 2 \cdot Q_c \cdot \text{freq} \cdot V_{GS} \cdot \frac{r_{gate}}{r_{gate} + r_{DS(ON)}} + I_{DD}(\text{freq}) \cdot V_{DD}$$

where:

- freq = Switching frequency
- $V_{GS} = V_{DRV}$  bias of the ISL71040M
- $Q_c$  = Gate charge for  $V_{GS}$
- $I_{DD}(\text{freq})$  = Bias current at the switching frequency
- $r_{DS(ON)}$  = Driver ON-resistance
- $r_{gate}$  = External gate resistance (if any)

*Note:* The gate power dissipation is proportionally shared with the external gate resistor. Do not overlook the power dissipated by the external gate resistor.

## 6.5 PCB Layout Considerations

The ISL71040M AC performance depends significantly on the Printed Circuit Board (PCB) design. The following layout design guidelines are recommended to achieve optimum performance:

- Place the driver as close as possible to the driven power FET
- Understand where the switching power currents flow. The high amplitude di/dt currents of the driven power FET induce significant voltage transients on the associated traces
- Keep power loops as short as possible by paralleling the source and return traces
- Use planes where practical; they are usually more effective than parallel traces
- Avoid paralleling high amplitude di/dt traces with low level signal lines. High di/dt induces currents and consequently, noise voltages in the low level signal lines
- When practical, minimize impedances in low level signal circuits. The noise that is magnetically induced on a 10k $\Omega$  resistor is 10 times larger than the noise on a 1k $\Omega$  resistor
- Be aware of magnetic fields emanating from transformers and inductors. Gaps in the magnetic cores of these structures are especially bad for emitting flux
- If you must have traces close to magnetic devices, align the traces so that they are parallel to the flux lines to minimize coupling
- The use of low inductance components such as chip resistors and chip capacitors is highly recommended
- Use decoupling capacitors to reduce the influence of parasitic inductance in the VDRV, VDD, and GND leads. To be effective, these capacitors must also have the shortest possible conduction paths. If using vias, connect several paralleled vias to reduce the inductance of the vias
- It may be necessary to add resistance to dampen resonating parasitic circuits, especially on OUTH. If an external gate resistor is unacceptable, the layout must be improved to minimize lead inductance
- Keep high dv/dt nodes away from low level circuits. Guard banding can be used to shunt away dv/dt injected currents from sensitive circuits. This is especially true for control circuits that source the input signals to the ISL71040M

- Avoid placing a signal ground plane under a high amplitude dv/dt circuit. This injects di/dt currents into the signal ground paths
- Calculate power dissipation and voltage drop for the power traces. Many PCB/CAD programs have built-in tools for calculating trace resistance
- Large power components (such as power FETs, electrolytic caps, and power resistors) have internal parasitic inductance that cannot be eliminated
- If the circuits are simulated, consider including parasitic components, especially parasitic inductance
- The GaN FETs have a separate substrate connection that is internally tied to the source pin. The source and substrate should be at the same potential. Limit the inductance in the OUTH/L to Gate trace by keeping it as short and thick as possible
- For optimum thermal performance, place a pattern of vias and a thermal land on the top layer of the PCB directly underneath the EPAD. Connect the EPAD to VSSP. Connect the vias to the plane which serves as a heatsink. To ensure good thermal contact use solder to connect the EPAD to the thermal land on the PCB.

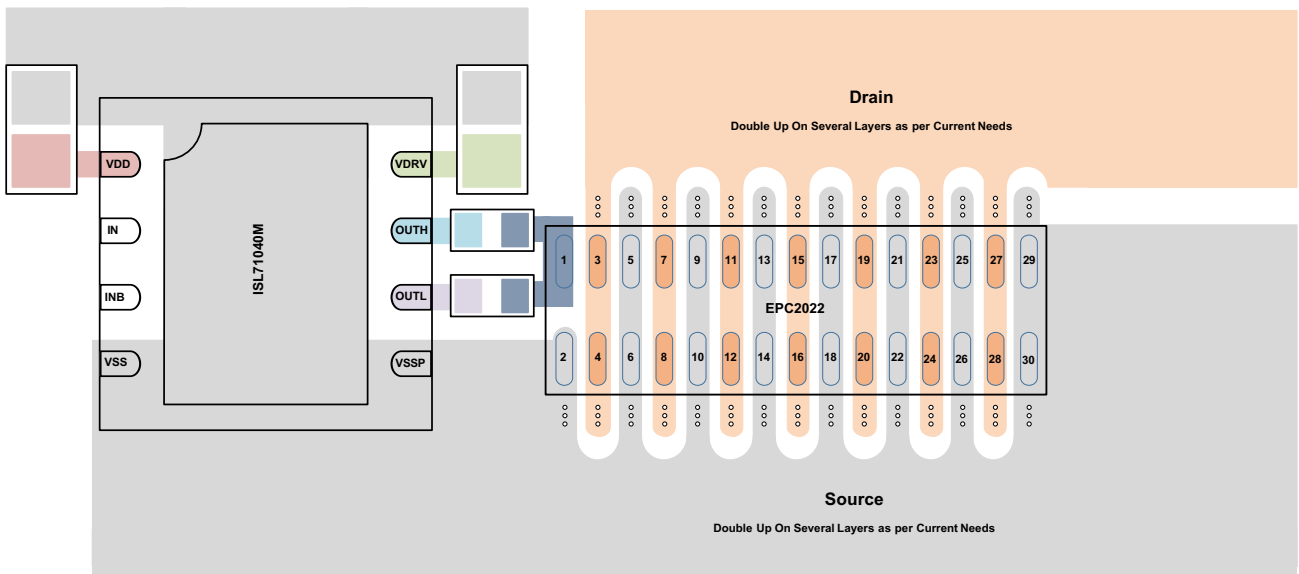


Figure 20. PCB Layout Recommendation

## 7. Radiation Tolerance

The ISL71040M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device’s response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL71040MRTZ is not guaranteed through radiation acceptance testing. The ISL71040M30RTZ is radiation lot acceptance tested (RLAT) to 30krad(Si) and ISL71040M50RTZ is RLAT to 50krad(Si). The SEE characterized performance is not guaranteed.

### 7.1 Total Ionizing Dose (TID) Testing

#### 7.1.1 Introduction

Total dose testing of the ISL71040M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 24 samples irradiated under bias, as shown in Table 2, and 24 samples irradiated with all pins grounded (unbiased). Two control units were used. Figure 21 shows the bias configuration.

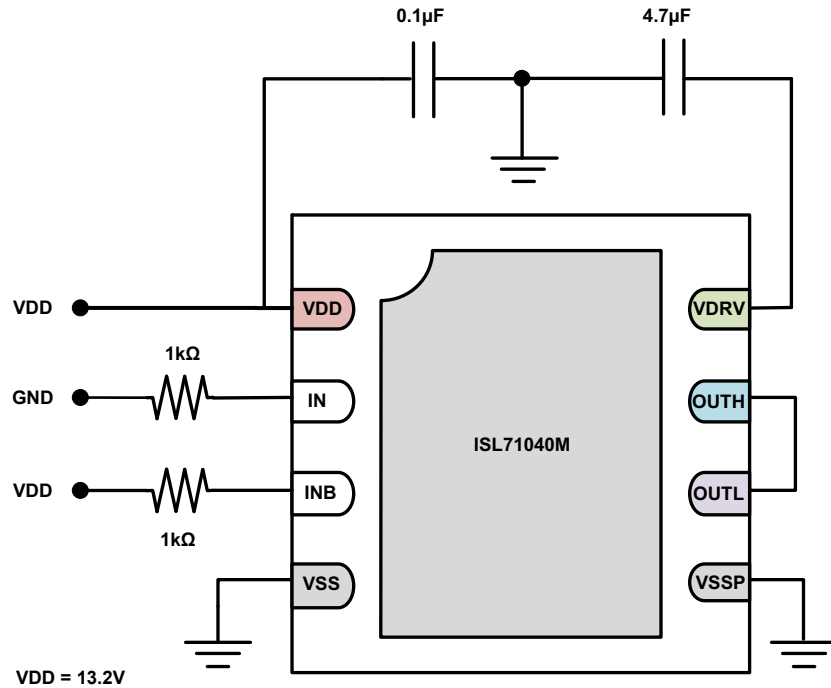


Figure 21. Irradiation Bias Configuration for the ISL71040M

Samples of the ISL71040M were drawn from fabrication lot 5V8PBA and were packaged in the production 8 Ld plastic TDFN, Package Outline Drawing (POD) L8.4x4B. The samples were screened to datasheet limits at room temperature only before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate <sup>60</sup>Co irradiator located in the Renesas Palm Bay, Florida facility. The dose rate was 0.0089rad(Si)/s (8.9mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Downpoints for the testing were 0krad(Si), 10krad(Si), 20krad(Si), 30krad(Si), and 50krad(Si).

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each downpoint. All downpoint electrical testing was performed at room temperature.

### 7.1.2 Results

Table 2 summarizes the attributes data. “Bin 1” indicates a device that passes all the datasheet specification limits.

Table 2. ISL71040M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Downpoints	Bin 1/Rejects
8.9	Figure 21	24	Pre-Rad	0
			10krad(Si)	0
			20krad(Si)	0
			30krad(Si)	0
			50krad(Si)	0

Table 2. ISL71040M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Downpoints	Bin 1/Rejects
8.9	Grounded	24	Pre-Rad	0
			10krad(Si)	0
			20krad(Si)	0
			30krad(Si)	0
			50krad(Si)	0

The plots in Figure 22 through Figure 29 show data for key parameters at all downpoints. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over irradiation.

Table 3 shows the average of other key parameters with respect to total dose in tabular form.

### 7.1.3 Typical Radiation Performance

$V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V$ , no load on OUTH/OUTL,  $r_{OUTH} = r_{OUTL} = 0\Omega$

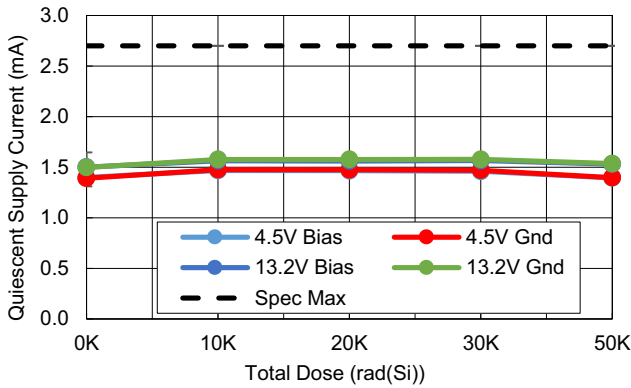


Figure 22. Quiescent Supply Current vs TID

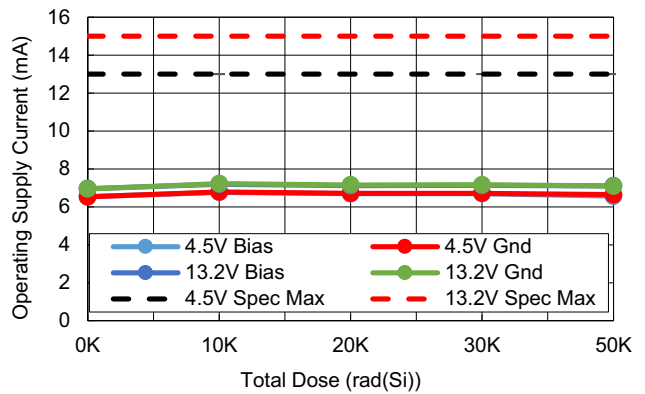


Figure 23. Operating Supply Current vs TID

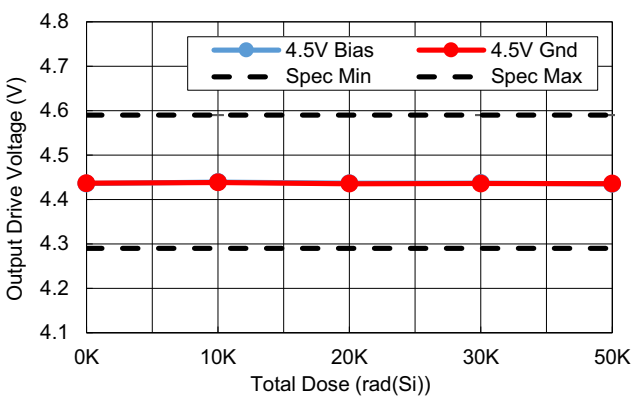


Figure 24.  $V_{DRV}$  Voltage vs TID ( $V_{DD} = 4.5V$ )

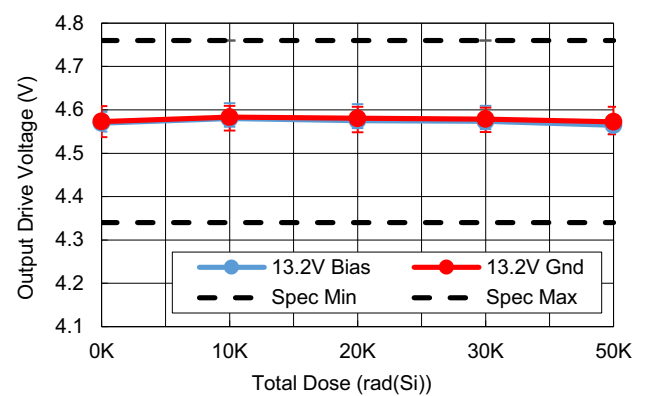


Figure 25.  $V_{DRV}$  Voltage vs TID ( $V_{DD} = 13.2V$ )

$V_{DD} = 4.5V, 13.2V, V_{SS} = V_{SSP} = 0V, C_{VDRV} = 4.7\mu F, V_{IH} = 5.0V, V_{IL} = 0V$ , no load on OUTH/OUTL,  $r_{OUTH} = r_{OUTL} = 0\Omega$  (Cont.)

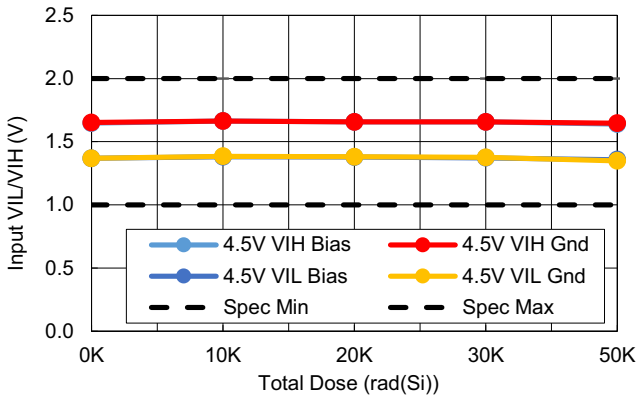


Figure 26.  $V_{IH}/V_{IL}$  Level vs TID ( $V_{DD} = 4.5V$ )

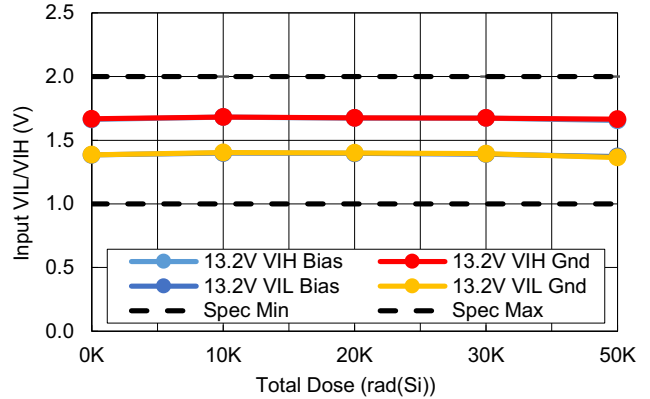


Figure 27.  $V_{IH}/V_{IL}$  Level vs TID ( $V_{DD} = 13.2V$ )

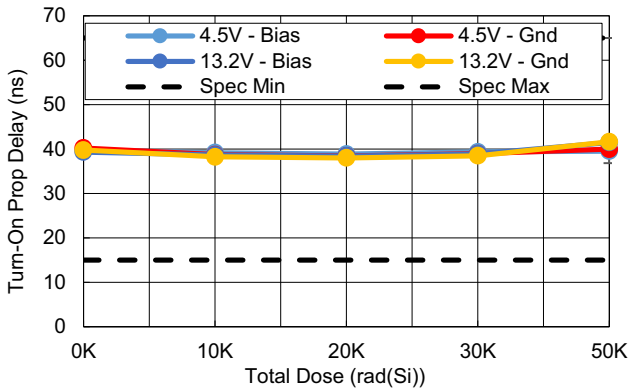


Figure 28.  $t_{DON}$  vs TID

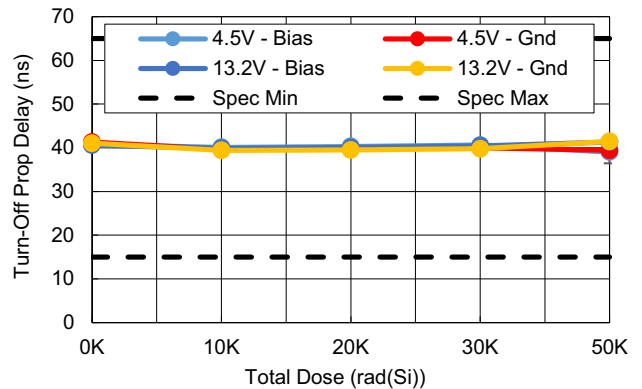


Figure 29.  $t_{DOFF}$  vs TID

Table 3. ISL71040M Response of Key Parameters vs TID

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	Pre-Rad Value	10k (rad(Si))	20k (rad(Si))	30k (rad(Si))	50k (rad(Si))	Unit
Quiescent Supply Current (4.5V)	$I_{DDQ}$	Bias	1.40	1.47	1.47	1.46	1.39	mA
		Ground	1.39	1.48	1.47	1.47	1.40	
		Limit -	0.10	0.10	0.10	0.10	0.10	
		Limit +	2.70	2.70	2.70	2.70	2.70	
Operating Supply Current (4.5V)	$I_{DDO}$	Bias	6.54	6.76	6.69	6.70	6.56	mA
		Ground	6.53	6.79	6.71	6.72	6.64	
		Limit -	1.00	1.00	1.00	1.00	1.00	
		Limit +	13.00	13.00	13.00	13.00	13.00	
Gate Drive Voltage (4.5V)	$V_{DRV}$	Bias	4.44	4.44	4.44	4.44	4.44	V
		Ground	4.44	4.44	4.44	4.44	4.44	
		Limit -	4.29	4.29	4.29	4.29	4.29	
		Limit +	4.59	4.59	4.59	4.59	4.59	



Table 3. ISL71040M Response of Key Parameters vs TID (Cont.)

Test Parameter Name and Conditions	Symbol	Irradiation Conditions	Pre-Rad Value	10k (rad(Si))	20k (rad(Si))	30k (rad(Si))	50k (rad(Si))	Unit
Gate Drive Voltage (13.2V)	$V_{DRV}$	Bias	4.57	4.58	4.58	4.57	4.56	V
		Ground	4.57	4.58	4.58	4.58	4.57	
		Limit -	4.34	4.34	4.34	4.34	4.34	
		Limit +	4.76	4.76	4.76	4.76	4.76	
Input VIL/VIH Level (4.5V)	$V_{IL}$	Bias	1.37	1.38	1.38	1.37	1.36	V
		Ground	1.37	1.38	1.38	1.38	1.35	
	$V_{IH}$	Bias	1.65	1.66	1.66	1.66	1.64	
		Ground	1.65	1.66	1.66	1.66	1.65	
	-	Limit -	1.00	1.00	1.00	1.00	1.00	
		Limit +	2.00	2.00	2.00	2.00	2.00	
Input VIL/VIH Level (13.2V)	$V_{IL}$	Bias	1.38	1.40	1.40	1.39	1.37	V
		Ground	1.39	1.40	1.40	1.39	1.36	
	$V_{IH}$	Bias	1.66	1.68	1.67	1.67	1.66	
		Ground	1.67	1.68	1.67	1.67	1.67	
	-	Limit -	1.00	1.00	1.00	1.00	1.00	
		Limit +	2.00	2.00	2.00	2.00	2.00	
Turn-On Propagation Delay (4.5V)	$t_{DON}$	Bias	39.78	39.18	38.87	39.36	39.52	ns
		Ground	40.23	38.74	38.45	38.95	39.99	
		Limit -	15.00	15.00	15.00	15.00	15.00	
		Limit +	65.00	65.00	65.00	65.00	65.00	
Turn-Off Propagation Delay (4.5V)	$t_{DOFF}$	Bias	40.79	40.10	40.29	40.64	39.02	ns
		Ground	41.31	39.64	39.76	40.02	39.43	
		Limit -	15.00	15.00	15.00	15.00	15.00	
		Limit +	65.00	65.00	65.00	65.00	65.00	

## 7.2 Single Event Effects Testing

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. This report discusses the results of SEE testing performed on the ISL71040M Low-Side GaN FET Driver.

### 7.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron that is capable of generating a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. Further details on the test facility can be found at their [website](#). The Devices Under Test (DUTs) were located in air at 30mm - 50mm from the Aramica window for the ion beam. Ion LET values are quoted at the DUT surface.

Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room. The testing reported here was conducted on December 5, 2018.

### 7.2.2 SEE Test Setup

SEE testing was carried out with the samples in an active configuration. Figure 30 shows the ISL71040M SEE test fixture schematic. Four units were mounted on every test board so that four units could be simultaneously irradiated and tested.

To test the ISL71040M for damaging SEE (collectively termed SEB), the part was placed in an operating condition with the input signal, IN, driven by a 500kHz square wave switching between GND and 10V. The INB terminal was tied to GND and the output was loaded with  $C_{OUT} = 10\text{nF}$ . The parameters monitored before and after irradiation to check for SEB were operating  $I_{DD}$  at the 500kHz input to IN, static  $I_{DD}$  at IN = 1.00V, static  $I_{DD}$  at IN = 2.0V,  $I_{IN}$  at IN = 0V,  $I_{IN}$  at IN = 13.2V,  $V_{OUT}$  at IN = 1.00V, and  $V_{OUT}$  at IN = 2.0V.  $V_{DD}$  was set to levels of 14.7V and 16.5V during the irradiation.

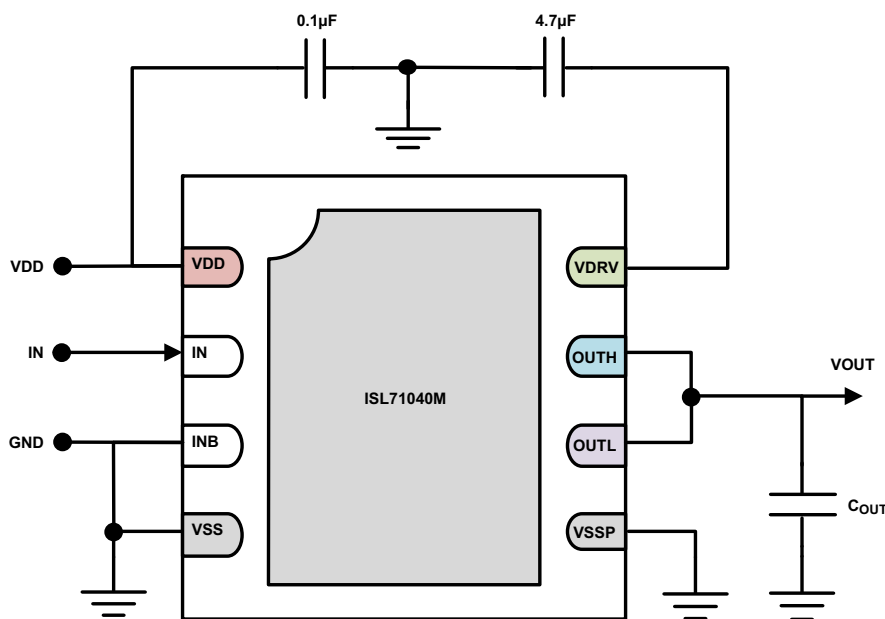


Figure 30. Simplified SEE Setup

The SET behavior of the ISL71040M was tested in both static and dynamic input cases. The  $C_{OUT}$  was removed to speed up the  $V_{OUT}$  response, and only the cable capacitance of about 700pF loaded the output. The INB input was tied to GND. In the static testing, IN was alternately set to 1.00V ( $V_{IL}$ ) and 2.0V ( $V_{IH}$ ) to provide the minimum noise margin on the input. The output,  $V_{OUT}$ , was monitored by an oscilloscope and triggered a capture whenever  $V_{OUT}$  traversed 2.0V.  $V_{DRV}$  was also captured in an SET event. The captures encompassed a time of  $-2\mu\text{s}$  to  $+18\mu\text{s}$  from the trigger point. During the dynamic testing IN was provided a 500kHz signal with a GND to 4V swing. In this case  $V_{OUT}$  was monitored and captures were triggered on  $\pm 20\text{ns}$  deviation from the nominal  $1\mu\text{s}$  pulse width.  $V_{DRV}$  was also captured for any SET, and the capture time was  $-2\mu\text{s}$  to  $+18\mu\text{s}$  from the trigger time.

### 7.2.3 SEB/SEL Results

Destructive SEE (SEB) testing of the ISL71040M proceeded with varying  $V_{DD}$  (14.7V and 16.5V) and checking the operating parameters (dynamic  $I_{DD}$  at 500kHz into 10nF, static  $I_{DD}$  at IN = 1.00V,  $I_{DD}$  at IN = 2.0V,  $I_{IN}$  at IN = 0V,  $I_{IN}$  at IN = 13.2V,  $V_{OUT}$  at IN = 1.00V,  $V_{OUT}$  at IN = 2.0V) before and after irradiation to identify any damaging effects. Irradiation was done with silver (Ag) at normal incidence for LET at the die surface (after an

Aramica window and a 30mm air gap) of 43 MeV·cm<sup>2</sup>/mg to a fluence of 1x10<sup>7</sup> ion/cm<sup>2</sup> at a flux of 5x10<sup>4</sup> ion/(cm<sup>2</sup> · s) and at a case temperature of 125°C ±10°C.

Although testing was also done at V<sub>DD</sub> = 14.7V, only the results at V<sub>DD</sub> = 16.5V are presented in Table 4. The results at the lower voltage are not shown because they were similarly unchanging and add no new information.

**Table 4. ISL71040M SEB/L Results (V<sub>DD</sub> = 16.5V, LET = 43MeV · cm<sup>2</sup>/mg at 1x10<sup>7</sup>ions/cm<sup>2</sup>, T<sub>CASE</sub> = 125°C ±10°C)**

V <sub>DD</sub> = 16.5V		I <sub>DD</sub> at 500kHz (mA)	I <sub>IN</sub> at IN = 0V (nA)	I <sub>IN</sub> at IN = 13.2V (µA)	I <sub>DD</sub> at IN = 1.0V (mA)	V <sub>OUT</sub> at IN = 1.0V (µV)	I <sub>DD</sub> at IN = 2.0V (mA)	V <sub>OUT</sub> at IN = 2.0V (V)
DUT1	Pre	31.0	0.15	71	1.80	87	10.7	4.58
	Post	30.2	0.18	71	1.80	78	10.7	4.58
	Delta	-2.5%	20.0%	0.0%	0.0%	-10.3%	0.4%	0.0%
DUT2	Pre	31.3	0.21	70	1.78	89	10.6	4.58
	Post	30.6	0.22	69	1.78	82	10.7	4.58
	Delta	-2.1%	4.8%	-1.4%	0.0%	-7.9%	0.4%	0.0%
DUT3	Pre	31.0	0.19	69	1.77	94	10.5	4.57
	Post	30.4	0.21	69	1.77	85	10.5	4.57
	Delta	-1.9%	10.5%	0.0%	0.0%	-9.6%	0.2%	0.0%
DUT4	Pre	32.0	0.23	69	1.79	80	10.5	4.59
	Post	31.5	0.22	69	1.79	74	10.5	4.59
	Delta	-1.5%	-4.3%	0.0%	0.0%	-7.5%	0.3%	0.0%

The data presented in Table 4 supports the conclusion that the ISL71040M is immune to damaging SEE for operation at V<sub>DD</sub> = 16.5V and case temperature of 125°C when irradiated with ions of LET 43MeV·cm<sup>2</sup>/mg at normal incidence. All of the monitored parameters exhibited variations within the reasonable accuracy of the measurements.

### 7.2.4 SET Results

The first ISL71040M SET test looked for the occurrence of V<sub>OUT</sub> deviations from a static output level. The test looked for V<sub>OUT</sub> transitioning through 2V for both IN = 1.00V and IN = 2.00V. Tests were run for both V<sub>DD</sub> = 4.5V and V<sub>DD</sub> = 13.2V. No static SET were captured for any of the four DUTs tested in all four of the static conditions. With four parts each irradiated to 1x10<sup>7</sup> ion/cm<sup>2</sup> at an LET of 43MeV·cm<sup>2</sup>/mg and 25°C, this put an upper bound on the cross section for a static SET at 2.5x10<sup>-8</sup> cm<sup>2</sup>.

The next SET testing looked for ±20ns perturbations on a 500kHz signal at the output. Both supply voltages, 4.5V and 13.2V, were tested. At testing with 43MeV·cm<sup>2</sup>/mg silver ions, a small number of dynamic SET were found at the 13.2V bias. Table 5 shows the results for this dynamic testing. The six SET captured spanned the pulse width deviation from the nominal 1µs of -26ns to +17ns.

**Table 5. ISL71040M ±20ns Perturbation Counts on a 500kHz Square Wave and Cross Sections for Normal Incidence Ions at 43MeV·cm<sup>2</sup>/mg at 25°C**

43 MeV · cm <sup>2</sup> /mg	±20ns SET Counts for 500kHz				Average Cross Section (cm <sup>2</sup> )
	DUT1	DUT2	DUT3	DUT4	
V <sub>DD</sub> = 4.5V	0	0	0	0	<2.5 x 10 <sup>-8</sup>
V <sub>DD</sub> = 13.2V	1	4	0	1	1.5 x 10 <sup>-7</sup>

### 7.2.5 SET Discussion and Conclusions

The ISL71040M was found to be immune to damaging SEE when run at  $V_{DD} = 16.5V$  and a case temperature of  $125^{\circ}C \pm 10^{\circ}C$  with a 500kHz signal being driven into a 10nF load capacitance and irradiated with normal silver ions for a surface LET of  $43 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . Four parts irradiated to  $1 \times 10^7 \text{ ion}/\text{cm}^2$  each showed no fundamental changes in the seven monitor parameters as presented in [Table 4](#).

The ISL71040M exhibited no static output upsets through 2V at either  $V_{DD} = 4.5V$  or  $V_{DD} = 13.2V$ , or the input at either  $IN = 1.00V (V_{IL})$  or  $IN = 2.00V (V_{IH})$ . The irradiations to  $1 \times 10^7 \text{ ion}/\text{cm}^2$  were done with normal silver for a surface LET of  $43 \text{ MeV}\cdot\text{cm}^2/\text{mg}$  at a case temperature of approximately  $25^{\circ}C$ .

For dynamic SET defined as a  $\pm 20\text{ns}$  perturbation in pulse width for a 50% duty cycle 500kHz signal, a very small cross section ( $\leq 1.5 \times 10^{-7} \text{ cm}^2$  as reported in [Table 5](#)) was found for the ISL71040M. This was determined for  $1 \times 10^7 \text{ ion}/\text{cm}^2$  on each of four parts irradiated with normal incidence silver for LET of  $43 \text{ MeV}\cdot\text{cm}^2/\text{mg}$ . As with the static SET testing  $V_{DD}$  was set to both  $V_{DD} = 4.5V$  and  $V_{DD} = 13.2V$  with the larger value yielding all the SET recorded. The six captured dynamic SET represented deviations of the pulse width from the nominal  $1\mu\text{s}$  spanning  $-26\text{ns}$  to  $+18\text{ns}$ .

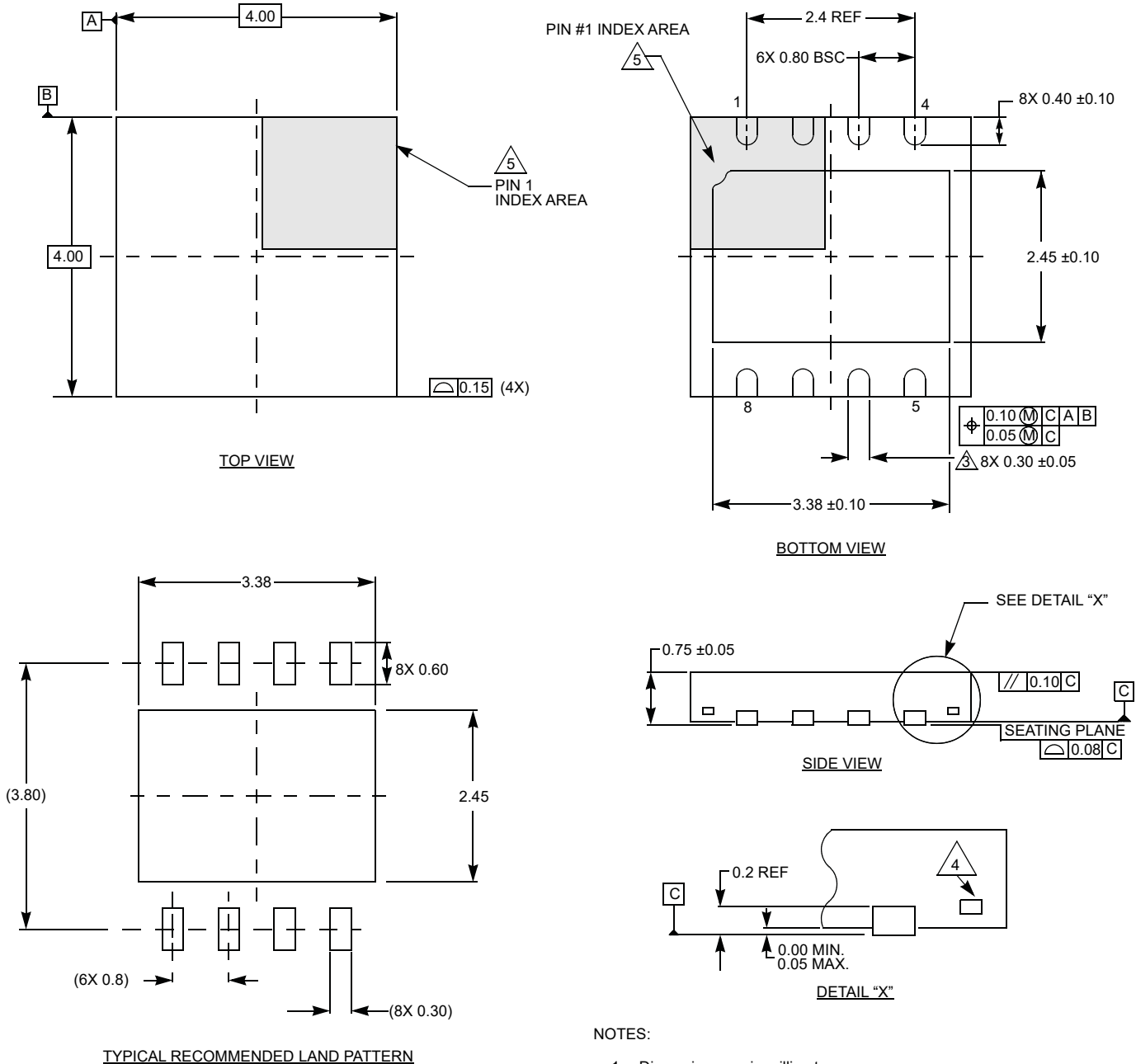
## 8. Package Outline Drawing

For the most recent package outline drawing, see [L8.4x4B](#).

L8.4x4B

8 Lead Thin Dual Flat No-Lead Plastic Package (TDFN)

Rev 0, 05/16



**NOTES:**

1. Dimensions are in millimeters.  
Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
3. Dimension applies to the metallized terminal and is measured between 0.015mm and 0.30mm from the terminal tip.
4. Tiebar shown (if present) is a non-functional feature, and may be located on any of the 4 sides (or ends).
5. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

## 9. Ordering Information

Part Number <sup>[1][2]</sup>	Part Marking	Radiation Lot Acceptance Testing	Package Description <sup>[3]</sup> (RoHS Compliant)	Pkg. Dwg. #	Carrier Type <sup>[4]</sup>	Temp Range
ISL71040MRTZ	710 40MRTZ	N/A	8 Ld TDFN	L8.4x4B	Tube	-55 to +125°C
ISL71040MRTZ-T					Reel, 6k	
ISL71040MRTZ-T7A					Reel, 250	
ISL71040M30RTZ		30krad(Si)			Tube	
ISL71040M30RTZ-T					Reel, 6k	
ISL71040M30RTZ-T7A					Reel, 250	
ISL71040M50RTZ		50krad(Si)			Tube	
ISL71040M50RTZ-T					Reel, 6k	
ISL71040M50RTZ-T7A					Reel, 250	
ISL71040MEV1Z	Standalone evaluation board for the ISL71040M.					
ISL71043MEVAL1Z	Flyback Power Supply Evaluation Board using the ISL71043M and ISL71040M.					

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the [ISL71040M](#) device page. For more information about MSL, see [TB363](#).
3. For the Pb-Free Reflow Profile, see [TB493](#).
4. See [TB347](#) for details about reel specifications.

## 10. Revision History

Rev.	Date	Description
1.02	Oct 3, 2024	Updated to the latest template. Updated Features bullets. Added ISL71040M30RTZ and ISL71040M50RTZ part information throughout document. Added Block Diagram.
1.01	Dec 15, 2022	Updated Pin Descriptions table. Updated Ordering Information table formatting. Updated PCB Layout Considerations section.
1.00	Feb 21, 2019	Initial release.

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### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

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