ISL7119RH, ISL7119EH

Radiation Hardened High Speed Dual Voltage Comparators

Description

The ISL7119RH and ISL7119EH are radiation hardened, high-speed, dual-voltage comparators fabricated on a single monolithic chip. They operate over a wide dual supply voltage range as well as a single 5V logic supply and ground. The open collector output stage facilitates interfacing with a variety of logic devices and has the ability to drive relays and lamps at output currents up to 25mA.

The ISL7119RH, ISL7119EH are fabricated on our dielectrically isolated Radiation Hardened Silicon Gate (RSG) process, which provides immunity to Single Event Latch-Up (SEL) and highly reliable performance in the natural space environment.

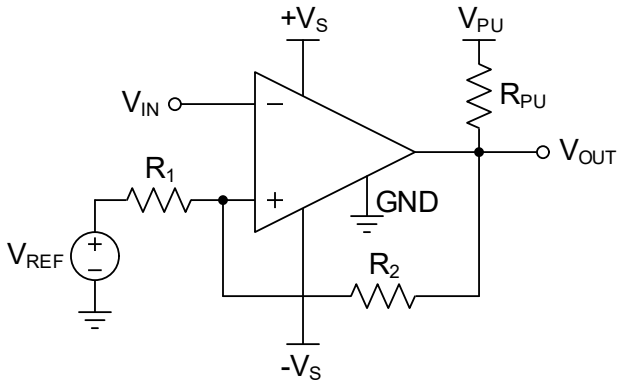
Applications

- Window detector
- Level shifter
- Relay driver
- Lamp driver

Features

- Electrically screened to DLA SMD # 5962-07215
  - QML qualified per MIL-PRF-38535 requirements
- Input offset voltage (V_{IO}): 8mV (max)
- Input bias current (I_{BIAS}): 1000nA (max)
- Input offset current (I_{IO}): 150nA (max)
- Saturation voltage at I_{SINK} = 3.2mA (V_{SAT}): 0.65V(max)
- Saturation voltage at I_{SINK} = 25mA (V_{SAT}): 1.8V(max)
- Response time (t_{PD}): 160ns (max)
- Radiation acceptance testing - ISL7119RH
  - HDR (50-300rad(Si)/s): 300krad(Si)
- Radiation acceptance testing - ISL7119EH
  - HDR (50-300rad(Si)/s): 300krad(Si)
  - LDR (0.01rad(Si)/s): 50krad(Si)
- SEE hardness (see SEE report for details)
  - SEL/SEB: Immune[1]

1. Devices use dielectrically isolated (DI) technology and latch up is physically not possible.



$$V_{TH(High)} = V_{REF} + (V_{PU} - V_{REF}) \times \frac{R_1}{R_1 + R_2 + R_{PU}}$$

$$V_{TH(Low)} = V_{REF} - (V_{REF} - V_{OL}) \times \frac{R_1}{R_1 + R_2}$$

$$V_{PU} > V_{REF} > V_{OL}$$

Figure 1. Typical Application Circuit: Inverting Comparator with Hysteresis

Contents

1. Pin Information

1.1 Pin Assignments

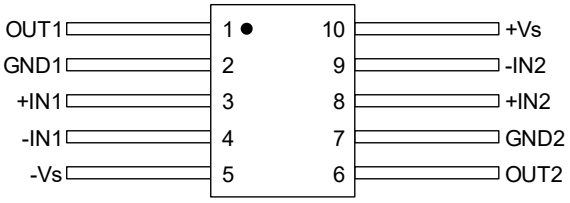


Figure 2. Pin Assignments - Top View

1.2 Pin Descriptions

Pin Name	Pin Number	Function
OUT1	1	Comparator 1: Open Collector Output
GND1	2	Comparator 1: Ground Potential
+IN1	3	Comparator 1: Noninverting Input
-IN1	4	Comparator 1: Inverting Input
-Vs	5	Negative Power Supply Input
OUT2	6	Comparator 2: Open Collector Output
GND2	7	Comparator 2: Ground Potential
+IN2	8	Comparator 2: Noninverting Input
-IN2	9	Comparator 2: Inverting Input
+Vs	10	Positive Power Supply Input

2. Specifications

2.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter		Minimum	Maximum	Unit
Total supply voltage		-	36	V
Output to negative supply voltage		-	36	V
Ground to negative supply voltage		-	25	V
Ground to positive supply voltage		-	18	V
Differential input voltage		-	±5	V
Input voltage		-	±15[1]	V
Output short-circuit duration		-	10[2]	s
Maximum power dissipation (PD) for case outline X:	T_A = +25°C	-	0.338	W
	T_A = +125°C	-	0.1	W
Maximum storage temperature range		-65	150	°C
Junction temperature (T_J)		-	175	°C
Lead temperature (soldering, 10 seconds)		-	265	°C

1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Short circuit from the output to +VS can cause excessive heating and eventual destruction.

2.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Single Supply Voltage ($+V_S$)	5	15	V
Dual Supply Voltage ($\pm V_S$)	±5	±15	V
Ambient Temperature (T_A)	-55	+125	°C

2.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	10 Ld CDFP	θ_{JA}[1]	Junction to ambient	165	°C/W
		θ_{JC}	Junction to case	60	°C/W

1. θ_{JA} is measured with the component mounted on an evaluation printed circuit (PC) board in free air.

2.4 Electrical Specifications

V_S = ±15V, GND = 0V, T_A = 25°C, unless otherwise noted

Parameter	Symbol	Test Condition[1]		Min	Max	Unit
Input Offset Voltage	V_{OS}	$+V_S$ = 15V, $-V_S$ = -15V, R_S ≤ 5kΩ, R_L = 1.4kΩ pull up to 5V	V_{CM} = 12V	-8	+8	mV
			V_{CM} = -12V			
		$+V_S$ = 5V, $-V_S$ = 0V, R_S ≤ 5kΩ, R_L = 1.4kΩ pull up to 5V	V_{CM} = 1V			
			V_{CM} = 3V			
Saturation Voltage	V_{SAT}	$+V_S$ = 15V, $-V_S$ = -15V, V_{IN} ≤ -8mV, I_{SINK} ≤ 25mA		-	1.8	V
		$+V_S$ = 3.5V, $-V_S$ = -1V, V_{IN} ≤ -8mV, I_{SINK} ≤ 3.2mA		-	0.65	V
Common-Mode Rejection Ratio	CMRR	$+V_S$ = 15V, $-V_S$ = -15V, R_S ≤ 5kΩ, R_L = 1.4kΩ pull up to 5V	V_{CM} = 12V	74	-	dB
			V_{CM} = -12V			
Input Offset Current	I_{IO}	$+V_S$ = 15V, $-V_S$ = -15V,	V_{CM} = 12V	-	150	nA
			V_{CM} = -12V			
		$+V_S$ = 5V, $-V_S$ = 0V,	V_{CM} = 1V			
			V_{CM} = 3V			
Input Bias Current	I_B	$+V_S$ = 15V, $-V_S$ = -15V, R_L = 1.4kΩ		-	1000	nA
		$+V_S$ = 5V, $-V_S$ = 0V, R_L = 1.4kΩ				
Positive Supply Current	I_{CC}	$+V_S$ = 15V, $-V_S$ = -15V, I_{SINK} ≤ 25mA		-	12	mA
Negative Supply Current	I_{EE}	$+V_S$ = 15V, $-V_S$ = -15V, I_{SINK} ≤ 25mA		-5	-	mA
Voltage Gain	A_{VOL}	$+V_S$ = 15V, $-V_S$ = -15V, R_L = 10kΩ pull up to 15V, ΔV_{OUT} = 10V		74	-	dB
		$+V_S$ = 5V, $-V_S$ = 0V, R_L = 10kΩ pull up to 5V, ΔV_{OUT} = 10V		72	-	dB
Output Leakage Current	I_{CEX}	$+V_S$ = 15V, $-V_S$ = -1V, V_{IN} < $V_{IO(min)}$, V_{OUT} = 35V		-	20	µA
Input Voltage Range	V_{IN}	$+V_S$ = 15V, $-V_S$ = -15V		-12	12	V
		$+V_S$ = 5V, $-V_S$ = 0V		1	3	V
Response Time	t_{PD}	$+V_S$ = 15V, $-V_S$ = -15V, R_L = 500Ω pull up to 5V, C_L = 50pF to GND, V_{IN} = V_{IO} + 5mV, ΔV_{IN} = 100mV		-	160	ns
		$+V_S$ = 5V, $-V_S$ = 0V, R_L = 500Ω pull up to 5V, C_L = 50pF to GND, V_{IN} = V_{IO} + 5mV, ΔV_{IN} = 100mV		-	185	ns

1. RH and EH Device meet all levels M, D, P, L, R, and F of irradiation. However, these devices are only tested at the F level in accordance with MIL-STD-883 method 1019 condition A. Pre and post irradiation values are identical unless otherwise specified in table. When performing post irradiation electrical measurements for any RHA level, T_A = +25°C (see Ordering Information). Device type 01 may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. In addition, an EH device is production lot acceptance tested on a wafer-by-wafer basis to 300krad(Si) in accordance with MIL-STD-883 method 1019 condition A, and 50krad(Si) in accordance with MIL-STD-883 method 1019 condition D.

3. Typical Performance Graphs

V_{PU} = 5V, V_{REF} = V_S/2, R_L = 500Ω, CL = 50pF, at T_A = 25°C (unless otherwise noted)

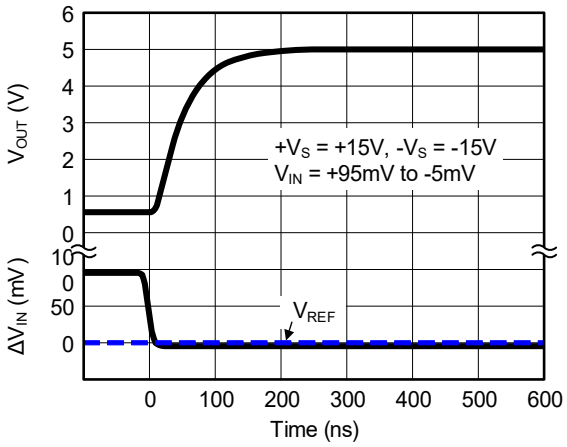


Figure 3. Response Time: Falling Edge, V_S = ±15V

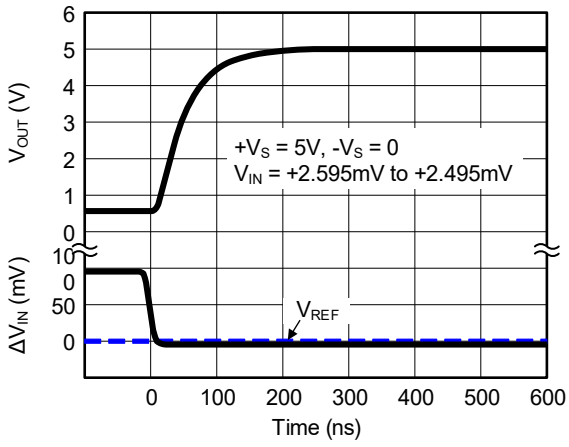


Figure 4. Response Time: Falling Edge, V_s = 5V

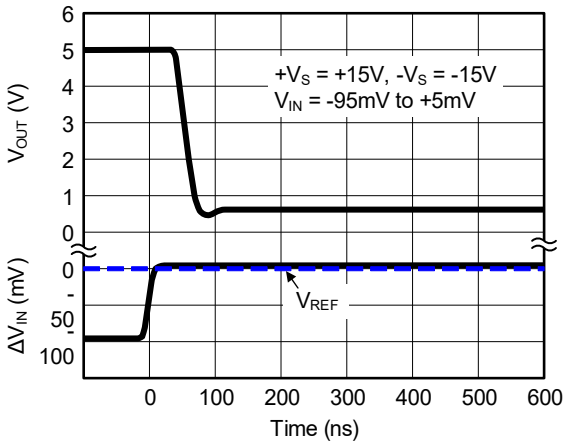


Figure 5. Response Time: Rising Edge, V_S = ±15V

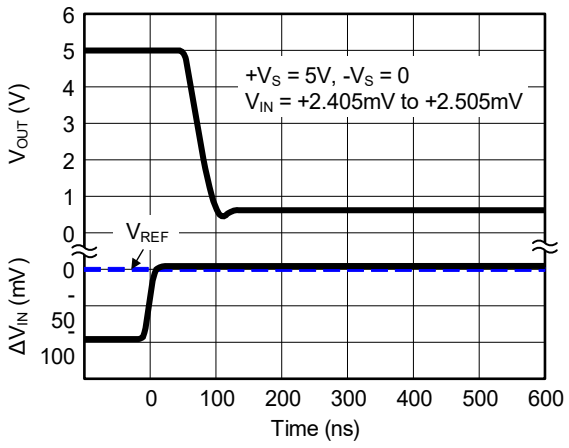


Figure 6. Response Time: Rising Edge, V_s = 5V

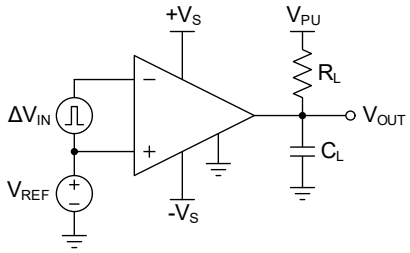
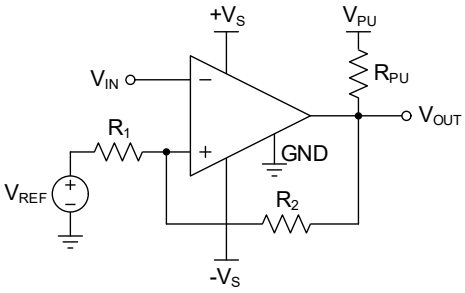


Figure 7. Response Time Test Circuit

4. Application Information

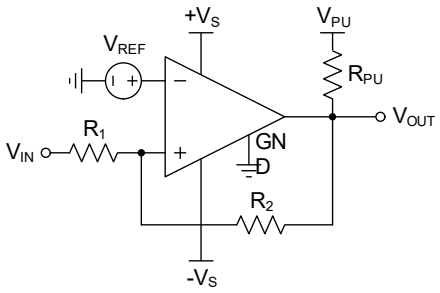


Threshold Voltages for $V_{PU} > V_{REF} > V_{OL}$

$$V_{TH(High)} = V_{REF} + (V_{PU} - V_{REF}) \times \frac{R_1}{R_1 + R_2 + R_{PU}}$$

$$V_{TH(Low)} = V_{REF} - (V_{REF} - V_{OL}) \times \frac{R_1}{R_1 + R_2}$$

Figure 8. Inverting Comparator with Hysteresis

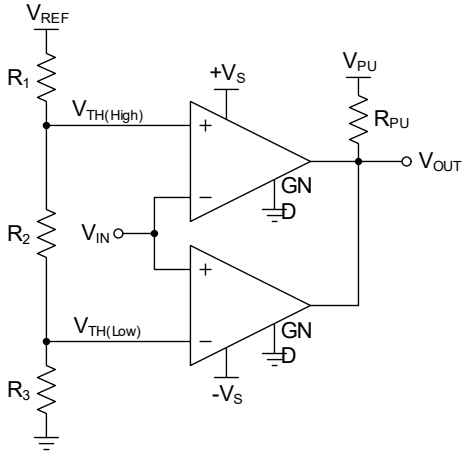


Threshold Voltages for $V_{PU} > V_{REF} > V_{OL}$

$$V_{TH(High)} = V_{REF} + (V_{REF} - V_{OL}) \times \frac{R_1}{R_2}$$

$$V_{TH(Low)} = V_{REF} - (V_{PU} - V_{REF}) \times \frac{R_1}{R_2 + R_{PU}}$$

Figure 9. Noninverting Comparator with Hysteresis



Threshold Voltages for $+V_S > V_{REF} > GND$

$$V_{TH(High)} = V_{REF} \times \frac{R_2 + R_3}{R_1 + R_2 + R_3}$$

$$V_{TH(Low)} = V_{REF} \times \frac{R_3}{R_1 + R_2 + R_3}$$

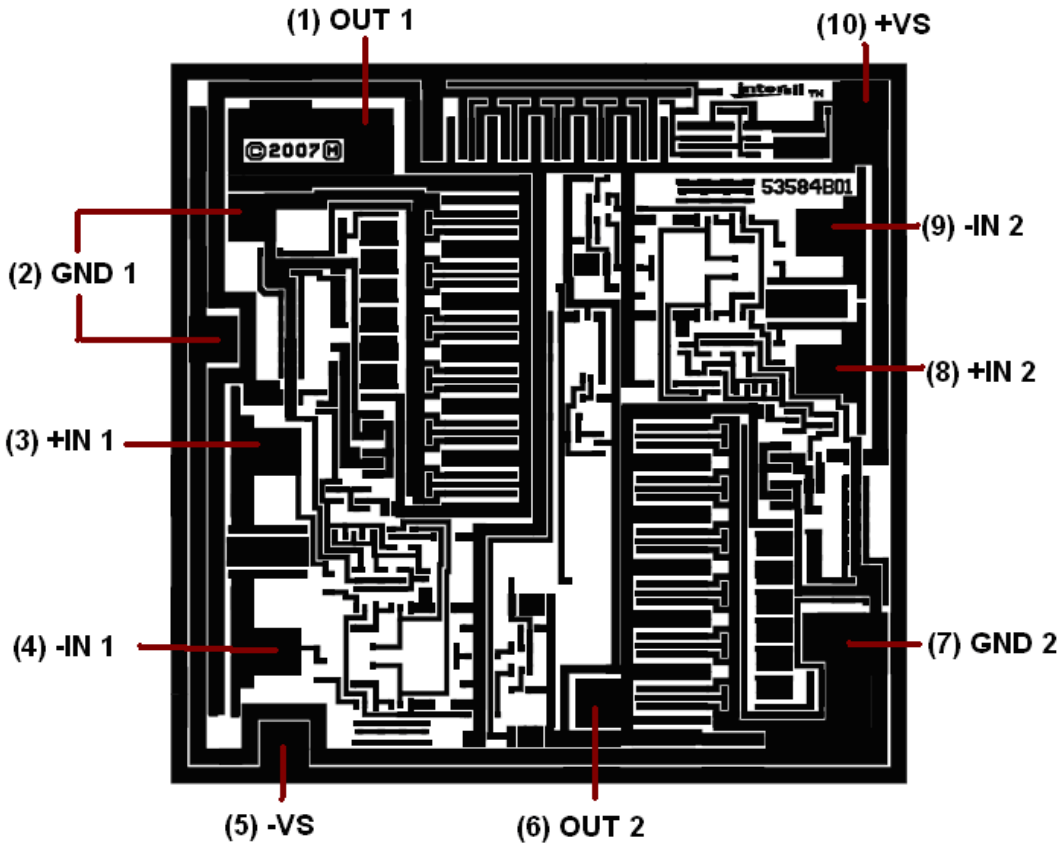
Figure 10. Window Comparator

5. Die and Assembly Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2030µm x 2030µm (~80mils x 80mils) Thickness: 483µm ±25.4µm (19mils ±1mil)
Interface Materials	
Glassivation	Type: PSG (Phosphorous Silicon Gas) Thickness: 8.0kÅ ± 1.0kÅ
Top Metallization	Type: AlSiCu Thickness: 16.0kÅ ± 2kÅ
Backside Finish	Silicon
Assembly Information	
Substrate Potential	Unbiased (DI)
Additional Information	
Worst Case Current Density	$<2.0 \times 10^5 A/cm^2$
Transistor Count	66

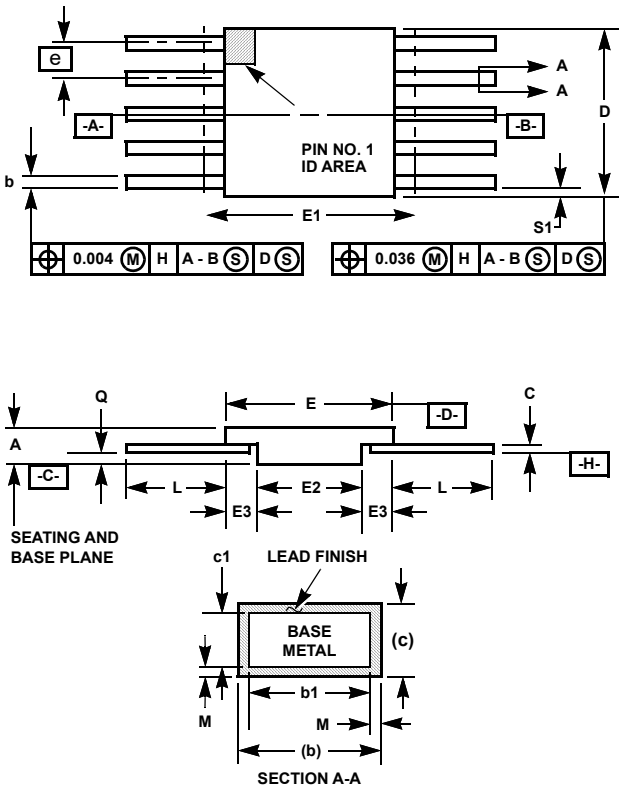
6. Metallization Mask Layout



7. Package Outline Drawing

For the most recent package outline drawing, see K10.A.

Ceramic Metal Seal Flatpack Packages (Flatpack)



K10.A MIL-STD-1835 CDFP3-F10 (F-4A, Configuration B)
10 Lead Ceramic Metal Seal Flatpack Package

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.290	-	7.37	3
E	0.240	0.260	6.10	6.60	-
E1	-	0.280	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	10		10		-

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NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

8. Ordering Information

Ordering SMD Number[1]	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Pkg. Dwg. #	Temp. Range
5962F0721501QXC	ISL7119RHQF	HDR to 300krad(Si)[3]	10 Lead Ceramic Metal Seal Flatpack	K10.A	-55 to +125°C
5962F0721501VXC	ISL7119RHVF				
5962F0721502VXC	ISL7119EHVF	HDR to 300krad(Si),[4] LDR to 50krad(Si)			
5962F0721501V9A	ISL7119RHVX[5]	HDR to 300krad(Si)	Die	N/A	
5962F0721502V9A	ISL7119EHVX[5]	HDR to 300krad(Si), LDR to 50krad(Si)			
ISL7119RHF/PROTO	ISL7119RHF/PROTO[6]	N/A	10 Lead Ceramic Metal Seal Flatpack	K10.A	
ISL7119RHX/SAMPLE	ISL7119RHX/SAMPLE[5][6]		Die	N/A	

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the table must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. The device may be dose rate sensitive in a space environment and may demonstrate enhanced low dose rate effects. The radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300krad(Si).
4. The device radiation end point limits for the noted parameters are guaranteed only for the conditions as specified in MIL-STD-883, method 1019, condition A to a maximum total dose of 300krad(Si), and condition D to a maximum total dose of 50krad(Si).
5. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in the DLA SMD.
6. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.

9. Revision History

Revision	Date	Description
5.02	Feb 13, 2025	Applied the latest template. Added Figure 1. Added the following sections: ▪ Pin Descriptions ▪ Specifications ▪ Typical Performance Graphs ▪ Application Information
5.01	Feb 9, 2023	Fixed links. Updated Radiation Acceptance feature bullets. Updated Ordering Information table. Removed About Intersil section.
5.00	Apr 15, 2016	Updated package info in ordering information for parts ending in X from 10 Lead Ceramic Metal Seal Flatpack to Die. Added Revision History and About Intersil sections. Added POD K10.A.

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