ISL71218M

Dual 36V Precision Single-Supply, Rail-to-Rail Output, Low-Power Operational Amplifier

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The ISL71218M is a radiation tolerant dual, low-power precision amplifier optimized for single-supply applications. This op amp features a common-mode input voltage range extending to 0.5V below the V^- rail, a rail-to-rail differential input voltage range, and rail-to-rail output voltage swing, which makes it ideal for single-supply applications where input operation at ground is important.

This op amp features low-power, low-offset voltage, and low-temperature drift, making it ideal for applications requiring both high DC accuracy and AC performance. It is designed to operate over a single supply range of 3V to 36V, or a split supply voltage range of +1.8V/-1.2V to ±18V. The combination of precision and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision instrumentation, data acquisition, and precision power supply controls.

The ISL71218M is available in an 8 Ld SOIC and operates across the extended temperature range of -55°C to +125°C.

Applications

- Low Earth orbit
- High altitude avionics
- Precision instruments
- Data acquisition
- Power supply control

Features

- Passes NASA low outgassing specifications
- Wide single and dual supply range: 3V to 30V (±10%)
- Low current consumption: 850µA, typical
- Low input offset voltage: 40µV, typical
- Rail-to-rail output: <10mV
- NiPdAu-Ag lead finish
- Dielectrically isolated PR40 process
- Rail-to-rail input differential voltage range for comparator applications
- Operating temperature range: -55°C to +125°C
- Below-ground (V^-) input capability to -0.5V
- Low noise voltage: 5.6nV/√Hz, typical
- Low noise current: 355fA/√Hz, typical
- Offset voltage temperature drift: 0.3µV/°C, typical
- No phase reversal
- Characterized radiation levels
  - Low dose rate (<10mrad(Si)): 30krad(Si)
  - Single event burnout LET: 43MeV•cm^2/mg

Related Literature

For a full list of related documents, visit our website

- ISL71218M product page

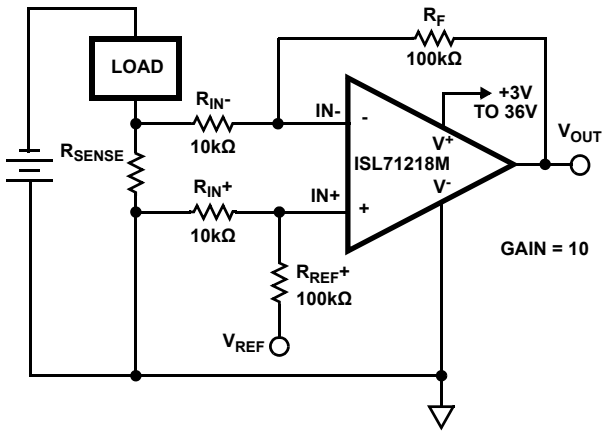

Figure 1. Typical Application: Single-Supply, Low-Side Current Sense Amplifier

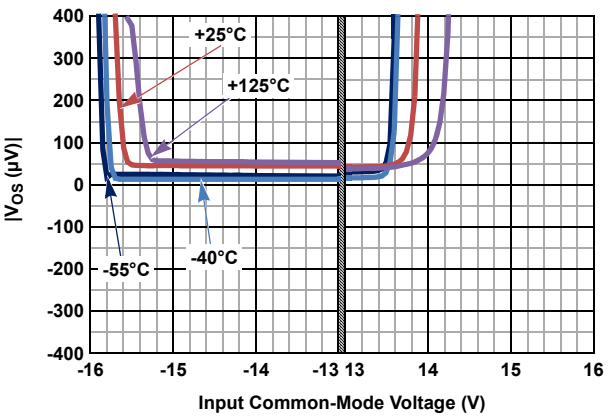

Figure 2. Input Offset Voltage vs Input Common-Mode Voltage, V_S = ±15V

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1. Overview

1.1 Ordering Information

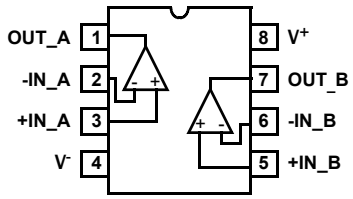
Part Number (Notes 2, 3)	Part Marking	Temp Range (°C)	Tape and Reel (Units)	Package (RoHS Compliant)	Pkg. Dwg. #
ISL71218MBZ	71218 MBZ	-55 to +125	-	8 Ld SOIC	M8.15
ISL71218MBZ-T (Note 1)	71218 MBZ	-55 to +125	1k	8 Ld SOIC	M8.15
ISL71218MBZ-T7A (Note 1)	71218 MBZ	-55 to +125	250	8 Ld SOIC	M8.15
ISL71218MEVAL1Z	Evaluation Board				

Notes:

1. See TB347 for details about reel specifications.
2. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), see the ISL71218M device page. For more information about MSL, see TB363.

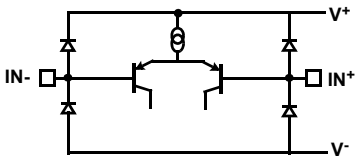
1.2 Pin Configuration

ISL71218M
(8 Ld SOIC)
Top View

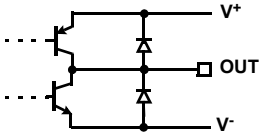


1.3 Pin Descriptions

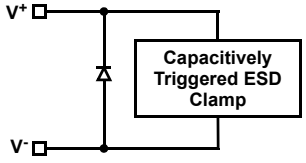
Pin Number	Pin Name	Equivalent Circuit	Description
1	OUT_A	Circuit 2	Amplifier A output
2	-IN_A	Circuit 1	Amplifier A inverting input
3	+IN_A	Circuit 1	Amplifier A non-inverting input
4	V-	Circuit 1, 2, 3	Negative power supply
5	+IN_B	Circuit 1	Amplifier B non-inverting input
6	-IN_B	Circuit 1	Amplifier B inverting input
7	OUT_B	Circuit 2	Amplifier B output
8	V+	Circuit 1, 2, 3	Positive power supply



Circuit 1



Circuit 2



Circuit 3

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage		42	V
Maximum Supply Voltage (Note 4)		40	V
Maximum Differential Input Current		20	mA
Maximum Differential Input Voltage	V^- - 0.5	V^+ + 0.5	V
Minimum/Maximum Input Voltage	V^- - 0.5	V^+ + 0.5	V
Minimum/Maximum Input Current		±20	mA
Output Short-Circuit Duration (1 output at a time)		Indefinite	
ESD Rating	**Value**		**Unit**
Human Body Model (Tested per JS-001-2014)	5.5		kV
Machine Model (Tested per JESD22-A115-C)	300		V
Charged Device Model (Tested per JS-002-2014)	2		kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	100 at +125°C		mA

Note:
4. Tested in a heavy ion environment at LET = 43MeV•cm^2/mg at +125°C (TC) for SEB.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost (Note 5)	0.06	%
Collected Volatile Condensible Material (Note 5)	<0.01	%
Water Vapor Recovered	0.03	%

Note:
5. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material of <0.1%.

2.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld SOIC Package (Notes 6, 7)	105	50

Notes:
6. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379.
7. For θ_{JC}, the case temperature location is the package top center.

Parameter	Minimum	Maximum	Unit
Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Operating Temperature Range	-55	+125	°C
Maximum Operating Junction Temperature		+150	°C
Single Supply Voltage	3	30	V
Dual Supply Voltage	+1.8/-1.2	±15	V

2.5 Electrical Specifications

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Offset Voltage	V_{OS}		-230	40	230	µV
			-320		**320**	µV
Offset Voltage Drift	TCV_{OS}			0.3	**1.4**	µV/°C
Input Offset Voltage Match Channel-to-Channel	ΔV_{OS}			44	280	µV
					365	µV
Input Offset Current	I_{OS}		-50	4	50	nA
			-75		**75**	nA
Input Bias Current	I_B		-575	-135		nA
			-800			nA
Common-Mode Input Voltage Range	V_{CMIR}	Ensured by CMRR Test	(V^-) - 0.5		(V^+) - 1.8	V
			V^-		**(V^+) - 1.8**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- to V^+ -1.8V	100	120		dB
		V_{CM} = V^- to V^+ -1.8V	**97**			dB
Power Supply Rejection Ratio	PSRR	V_S = 3V to 40V, V_{CMIR} = Valid input voltage	105	124		dB
			100			dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground, V_O = -13V to +13V	120	130		dB
			115			dB
Output Voltage High, V^+ to V_{OUT}	V_{OH}	R_L = 10kΩ			110	mV
					120	mV
Output Voltage Low, V_{OUT} to V^-	V_{OL}	R_L = 10kΩ			80	mV
					90	mV
Supply Current/Amplifier	I_S			0.85	1.10	mA
					1.40	mA
Source Current Capability	I_{S+}		**10**	20		mA
Sink Current Capability	I_{S-}		**10**	32		mA
Supply Voltage Range	V_{SUPPLY}	Ensured by PSRR Test	3		30	V
AC Specifications						
Gain Bandwidth Product	GBW	A_{CL} = 101, V_{OUT} = 100mV_{P-P}; R_L = 2k		4		MHz
Voltage Noise	e_{np-p}	0.1Hz to 10Hz, V_S = ±18V		300		nV_{P-P}
Voltage Noise Density	e_n	f = 10Hz, V_S = ±18V		8.5		nV/√Hz

V_S ±15V, V_{CM} = 0, V_O = 0V, R_L = Open, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Voltage Noise Density	e_n	f = 100Hz, V_S = ±18V		5.8		nV/√Hz
Voltage Noise Density	e_n	f = 1kHz, V_S = ±18V		5.6		nV/√Hz
Voltage Noise Density	e_n	f = 10kHz, V_S = ±18V		5.6		nV/√Hz
Current Noise Density	in	f = 1kHz, V_S = ±18V		355		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	1kHz, G = 1, V_O = $3.5V_{RMS}$, R_L = 10kΩ		0.0003		%
Transient Response						
Slew Rate	SR	A_V = 1, R_L = 2kΩ, V_O = $10V_{P-P}$	±1.0	±1.2		V/µs
			±0.4			V/µs
Rise Time 10% to 90% of V_{OUT}	t_r, t_f, Small Signal	A_V = 1, V_{OUT} = $100mV_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	200	ns
					400	ns
Fall Time 90% to 10% of V_{OUT}		A_V = 1, V_{OUT} = $100mV_{P-P}$, R_f = 0Ω, R_L = 2kΩ to V_{CM}		100	230	ns
					400	ns
Settling Time to 0.01% 10V Step; 10% to V_{OUT}	t_s	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}		8.5		µs
Positive Overshoot	OS+	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					20	%
Negative Overshoot	OS-	A_V = 1, V_{OUT} = $10V_{P-P}$, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
					20	%

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Offset Voltage	V_{OS}		230	40	230	µV
			-320		**320**	µV
Input Offset Voltage Match Channel-to-Channel	ΔV_{OS}			44	280	µV
					365	µV
Input Offset Current	I_{OS}		-50	4	50	nA
			-75		**75**	nA
Input Bias Current	I_B		-575	-135		nA
			-800			nA
Common-Mode Input Voltage Range	V_{CMIR}	Ensured by CMRR Test	(V^-) - 0.5		(V^+) - 1.8	V
			V^-		**(V^+) - 1.8**	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = V^- - 0.5V to V^+ - 1.8 V_{CM} = V^- to V^+ - 1.8V	92	117		dB
			80			dB
Power Supply Rejection Ratio	PSRR	V_S = 3V to 40V, V_{CMIR} = Valid input voltage	102	120		dB
			98			dB
Open-Loop Gain	A_{VOL}	R_L = 10kΩ to ground V_O = -3V to +3V	115	130		dB
			112			dB

V_S ±5V, V_{CM} = 0, V_O = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C. (Continued)**

Parameter	Symbol	Test Conditions	Min (Note 8)	Typ	Max (Note 8)	Unit
Output Voltage High, V^+ to V_{OUT}	V_{OH}	R_L = 10kΩ		36	65	mV
					70	mV
Output Voltage Low, V_{OUT} to V^-	V_{OL}	R_L = 10kΩ		28	45	mV
					50	mV
Supply Current/Amplifier	I_S			0.74	1.10	mA
					1.40	mA
Source Current Capability	I_{S+}	T_A = +25°C, +125°C	10	13		mA
		T_A = -55°C	6			mA
Sink Current Capability	I_{S-}		**10**	23		mA
AC Specifications						
Gain Bandwidth Product	GBW			3.2		MHz
Voltage Noise	e_{np-p}	0.1Hz to 10Hz		320		nV_{P-P}
Voltage Noise Density	e_n	f = 10Hz		9		nV/√Hz
Voltage Noise Density	e_n	f = 100Hz		5.7		nV/√Hz
Voltage Noise Density	e_n	f = 1kHz		5.5		nV/√Hz
Voltage Noise Density	e_n	f = 10kHz		5.5		nV/√Hz
Current Noise Density	in	f = 1kHz		380		fA/√Hz
Total Harmonic Distortion + Noise	THD + N	1kHz, G = 1, V_O = 1.25V_{RMS}, R_L = 10kΩ		0.0003		%
Transient Response						
Slew Rate	SR	A_V = 1, R_L = 2kΩ, V_O = 4V_{P-P}		±1		V/µs
Rise Time 10% to 90% of V_{OUT}	t_r, t_f, Small Signal	A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
Fall Time 90% to 10% of V_{OUT}		A_V = 1, V_{OUT} = 100mV_{P-P} , R_f = 0Ω, R_L = 2kΩ to V_{CM}		100		ns
Settling Time to 0.01% 4V Step; 10% to V_{OUT}	t_s	A_V = 1, V_{OUT} = 4V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		4		µs
Positive Overshoot	OS+	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%
Negative Overshoot	OS-	A_V = 1, V_{OUT} = 10V_{P-P}, R_f = 0Ω R_L = 2kΩ to V_{CM}		5		%

Note:

8. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3. Typical Performance Curves

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

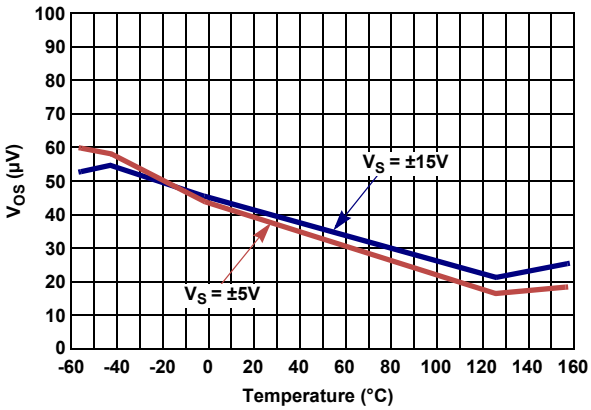


Figure 3. V_{OS} vs Temperature

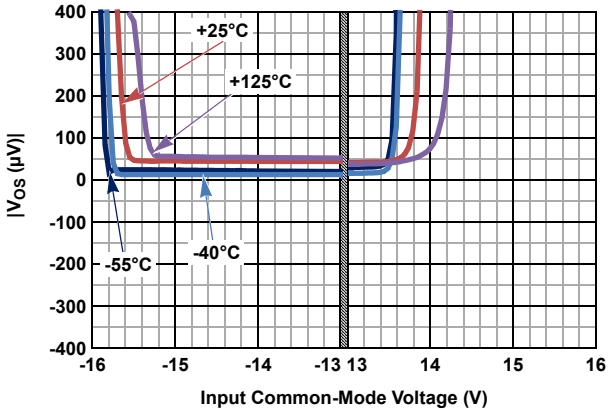


Figure 4. Input Offset Voltage vs Input Common-Mode Voltage, V_S = ±15V

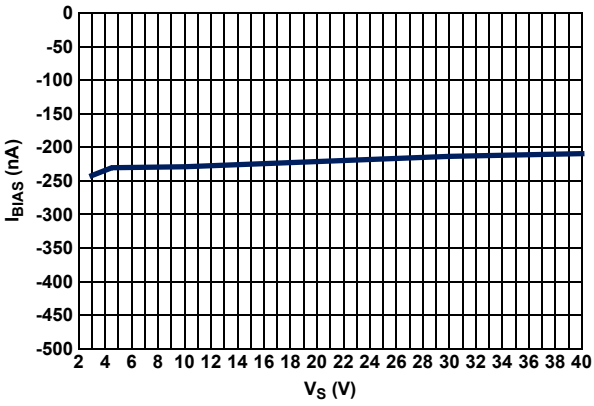


Figure 5. I_{BIAS} vs V_S

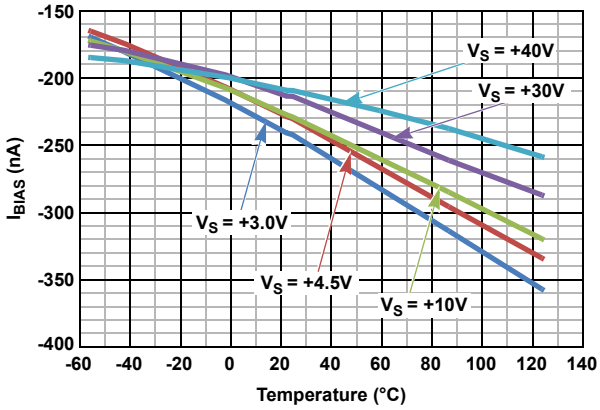


Figure 6. I_{BIAS} vs Temperature vs Supply

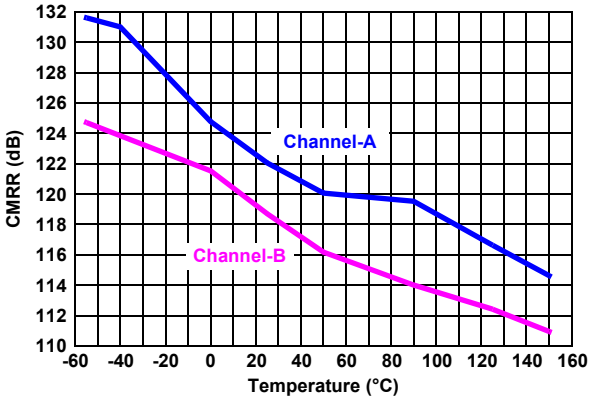


Figure 7. CMRR vs Temperature, V_S = ±15V

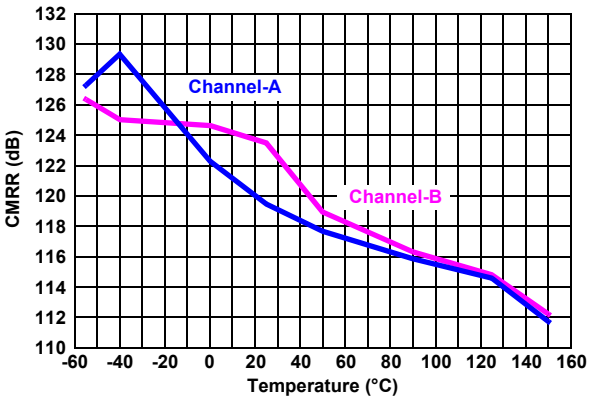


Figure 8. CMRR vs Temperature, V_S = ±5V

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

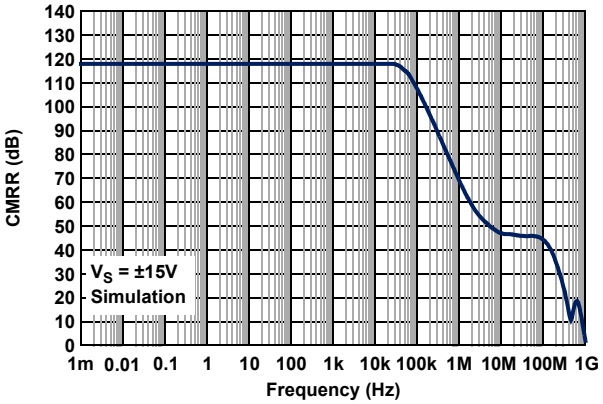


Figure 9. CMRR vs Frequency, V_S = ±15V

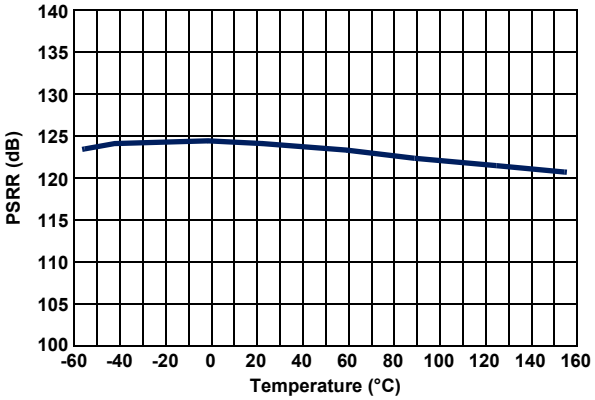


Figure 10. PSRR vs Temperature, V_S = ±15V

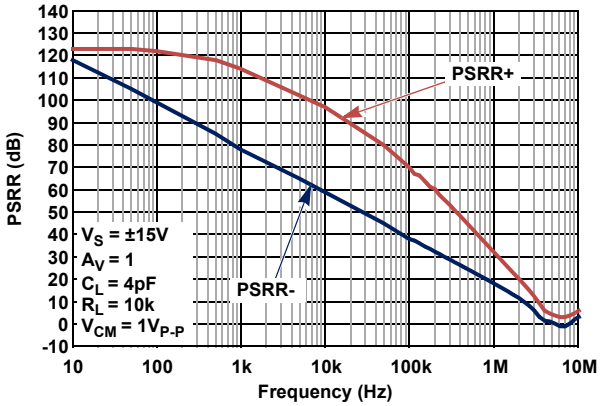


Figure 11. PSRR vs Frequency, V_S = ±15V

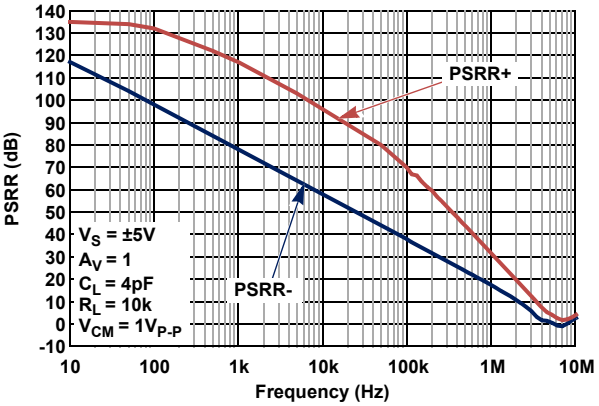


Figure 12. PSRR vs Frequency, V_S = ±5V

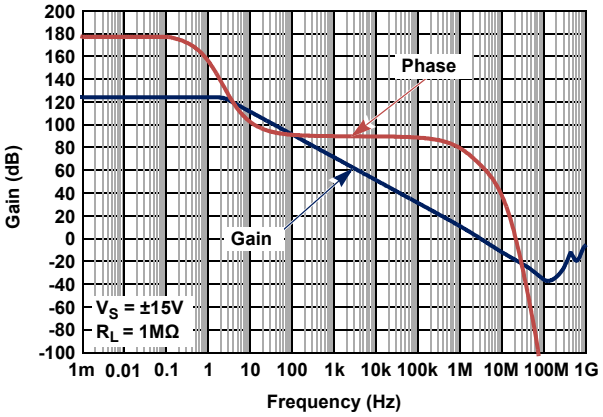


Figure 13. Open-Loop Gain, Phase vs Frequency, V_S = ±15V

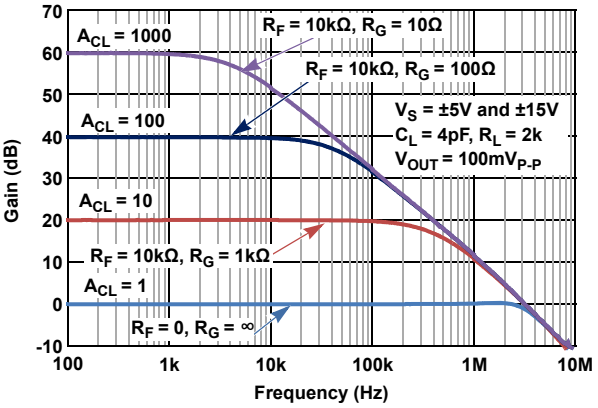


Figure 14. Frequency Response vs Closed-Loop Gain

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

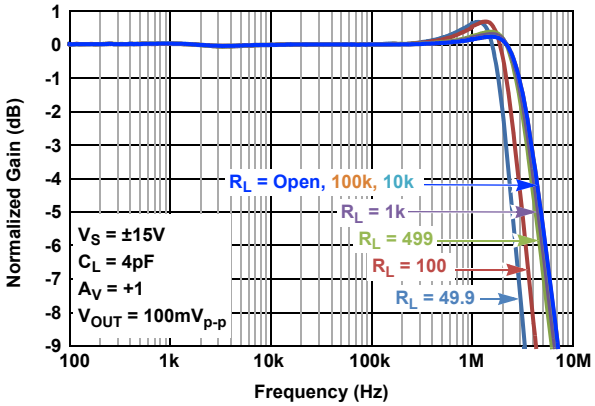


Figure 15. Gain vs Frequency vs R_L, V_S = ±15V

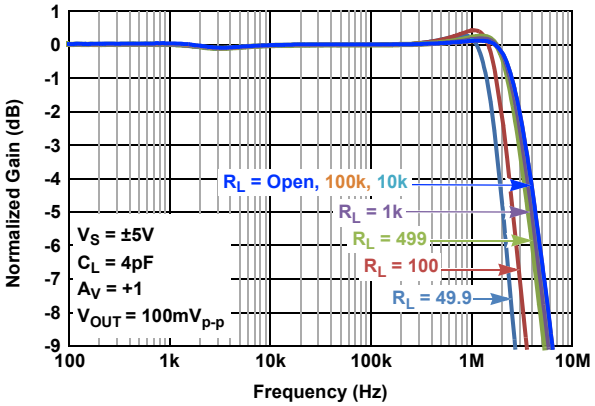


Figure 16. Gain vs Frequency vs R_L, V_S = ±5V

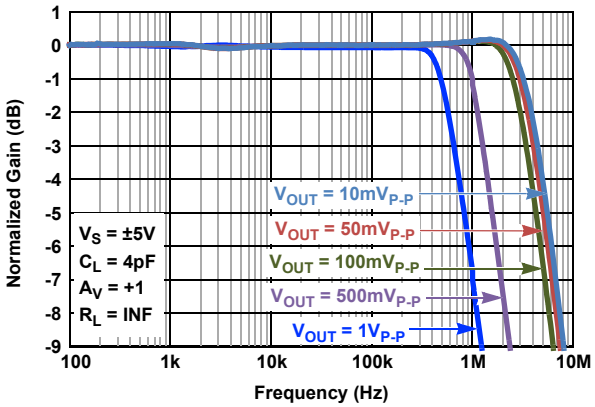


Figure 17. Gain vs Frequency vs Output Voltage

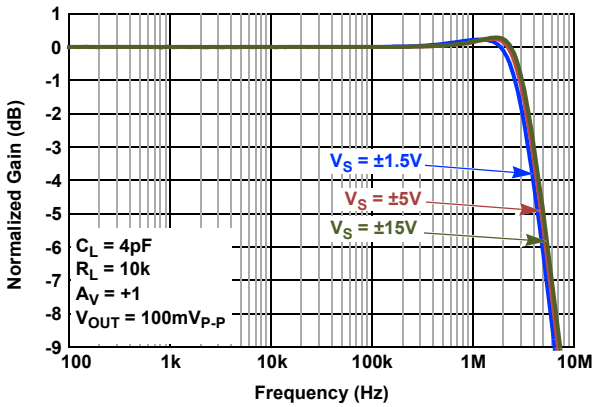


Figure 18. Gain vs Frequency vs Supply Voltage

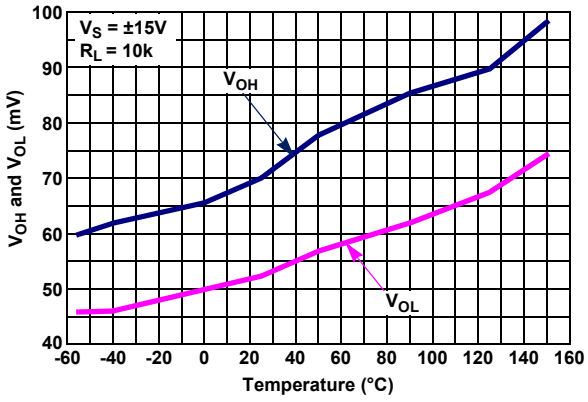


Figure 19. Output Overhead Voltage vs Temperature, V_S = ±15V, R_L = 10k

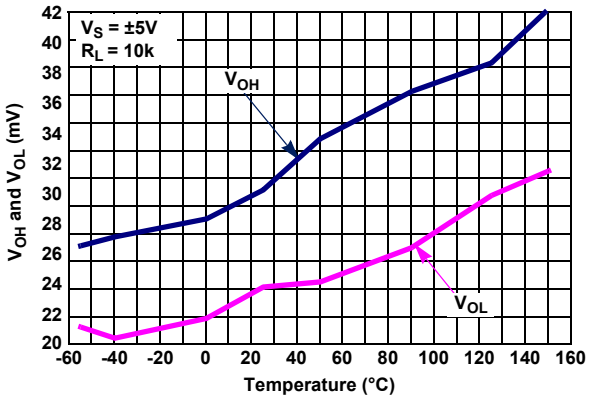


Figure 20. Output Overhead Voltage vs Temperature, V_S = ±5V, R_L = 10k

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

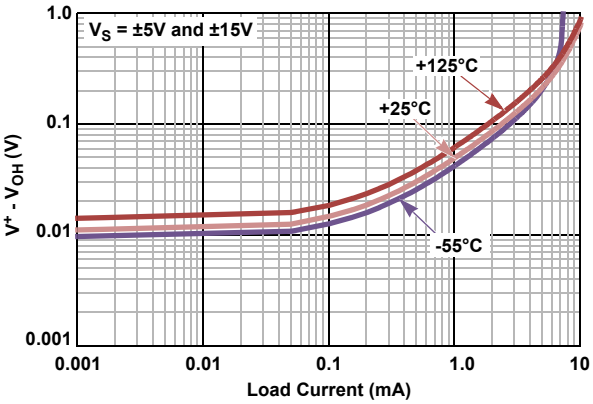


Figure 21. Output Overhead Voltage High vs Load Current, V_S = ±5V and ±15V

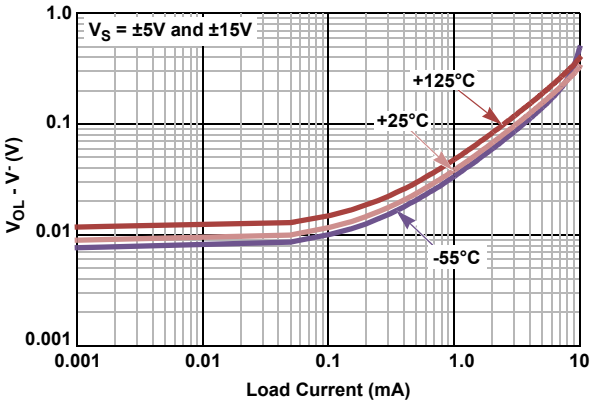


Figure 22. Output Overhead Voltage Low vs Load Current, V_S = ±5V and ±15V

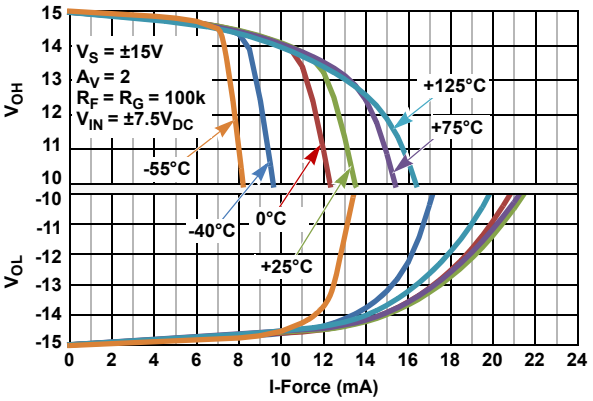


Figure 23. Output Voltage Swing vs Load Current, V_S = ±15V

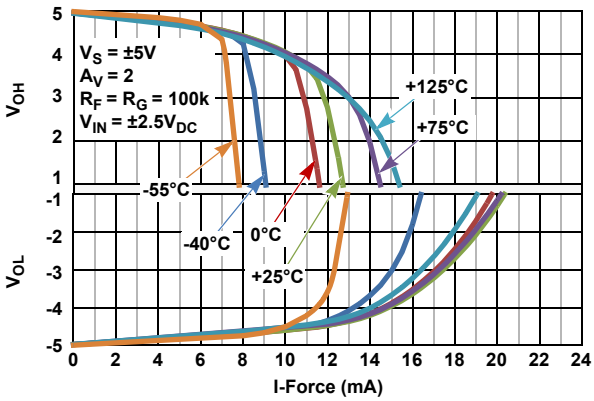


Figure 24. Output Voltage Swing vs Load Current, V_S = ±5V

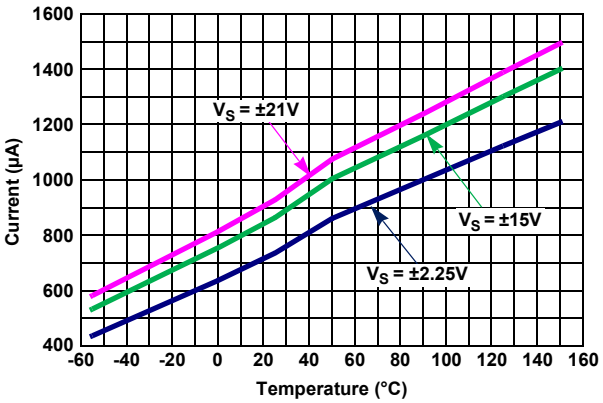


Figure 25. Supply Current vs Temperature vs Supply Voltage

Figure 26. Supply Current vs Supply Voltage

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

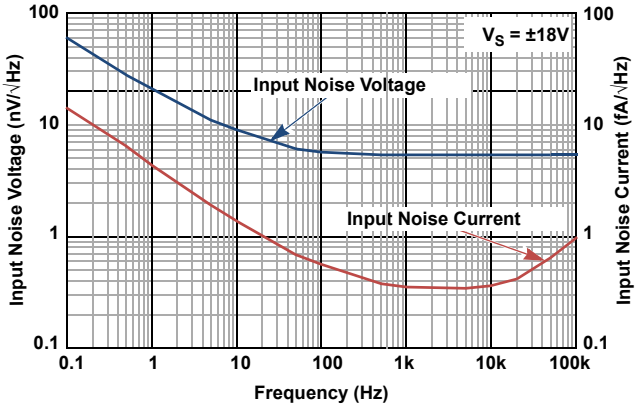


Figure 27. Input Noise Voltage (en) and Current (in) vs Frequency, V_S = ±18V

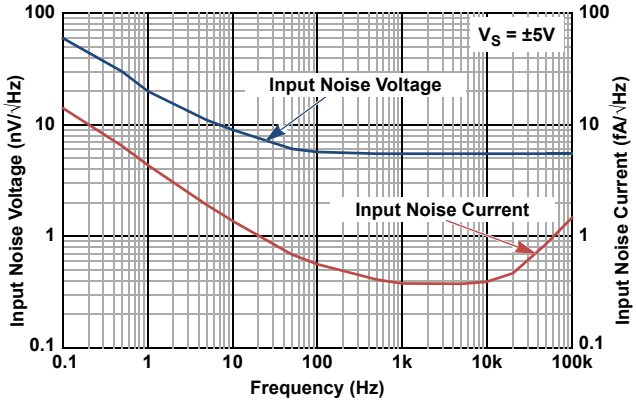


Figure 28. Input Noise Voltage (en) and Current (in) vs Frequency, V_S = ±5V

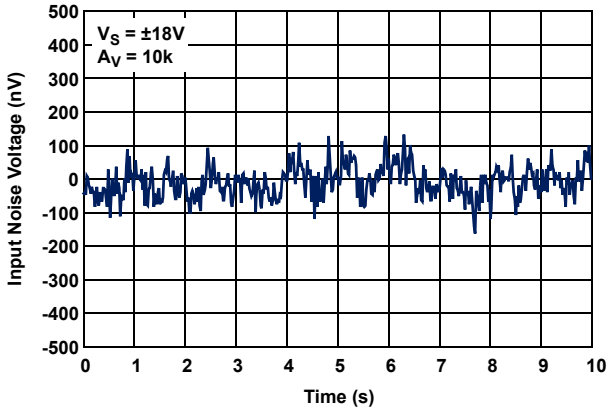


Figure 29. Input Noise Voltage 0.1Hz to 10Hz, V_S = ±18V

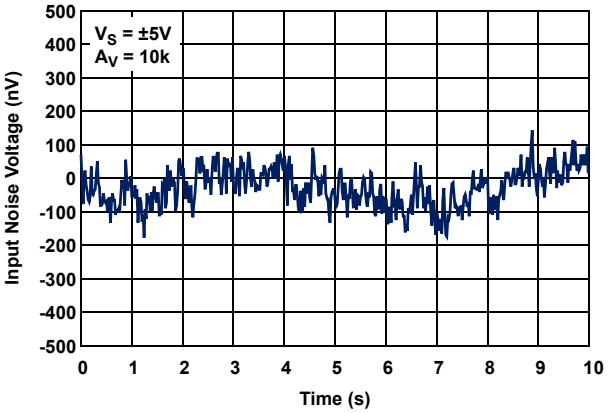


Figure 30. Input Noise Voltage 0.1Hz to 10Hz, V_S = ±5V

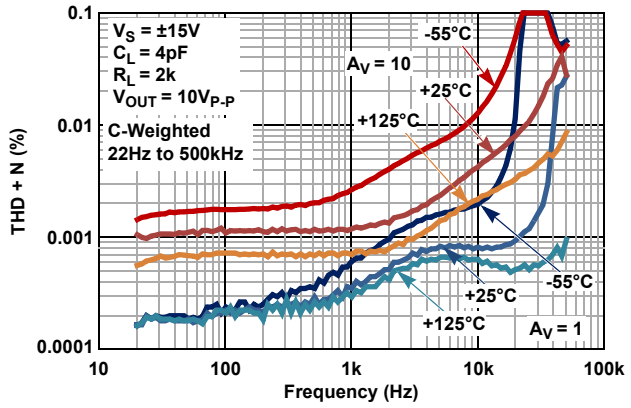


Figure 31. THD+N vs Frequency vs Temperature, A_V = 1, 10, R_L = 2k

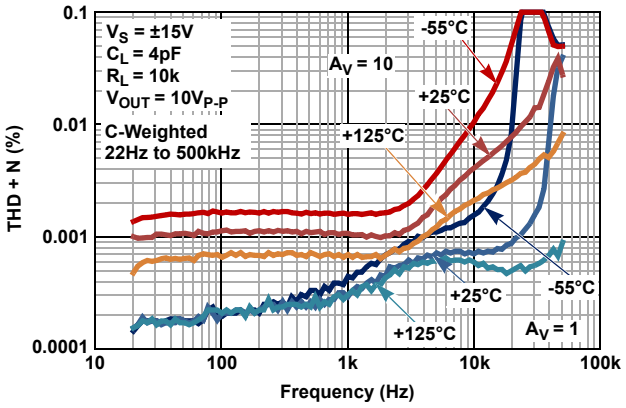


Figure 32. THD+N vs Frequency vs Temperature, A_V = 1, 10, R_L = 10k

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

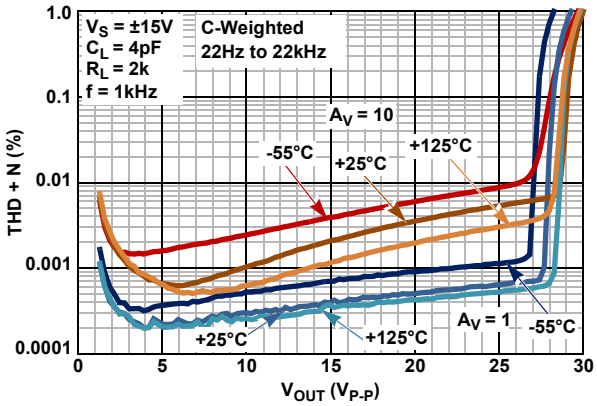


Figure 33. THD+N vs Output Voltage (V_{OUT}) vs Temperature, A_V = 1, 10, R_L = 2k

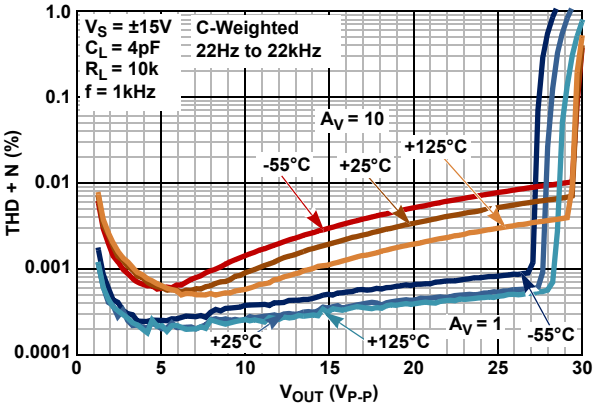


Figure 34. THD+N vs Output Voltage (V_{OUT}) vs Temperature, A_V = 1, 10, R_L = 10k

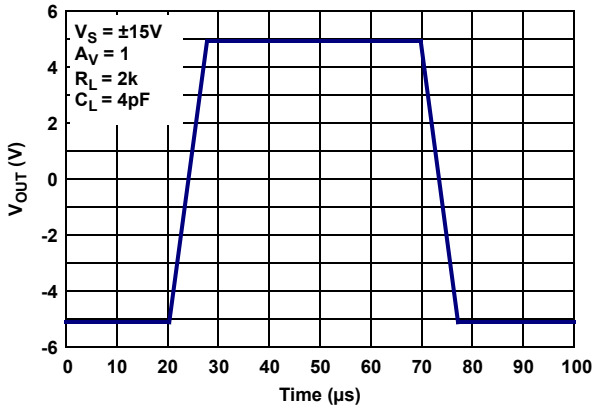


Figure 35. Large Signal 10V Step Response, V_S = ±15V

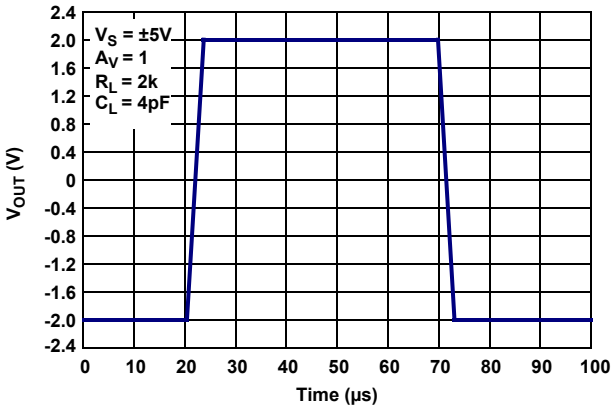


Figure 36. Large Signal 4V Step Response, V_S = ±5V

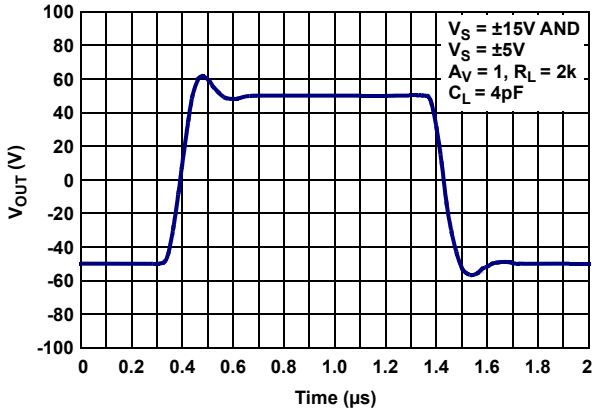


Figure 37. Small Signal Transient Response, V_S = ±5V, ±15V

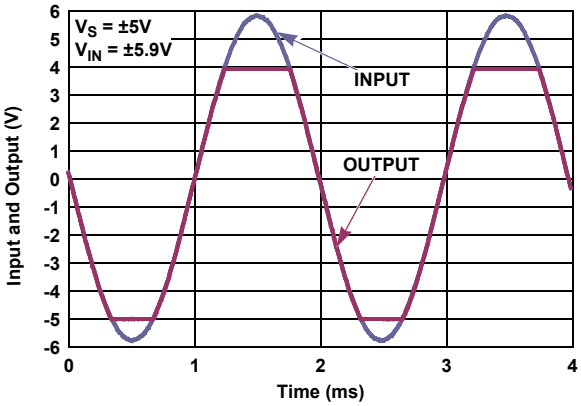


Figure 38. No Phase Reversal

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

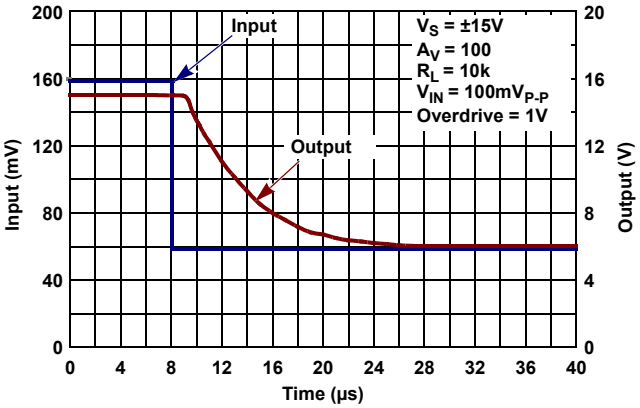


Figure 39. Positive Output Overload Response Time, V_S = ±15V

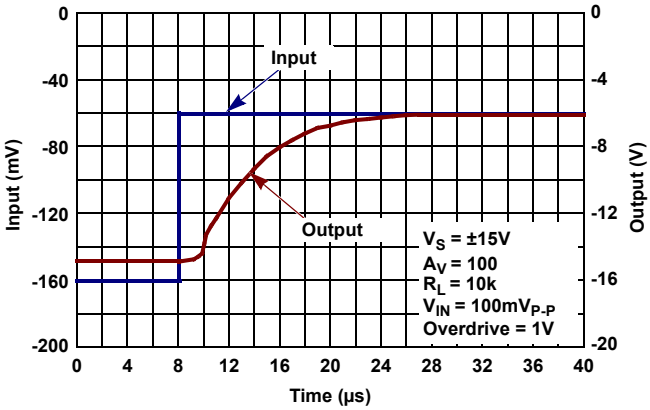


Figure 40. Negative Output Overload Response Time, V_S = ±15V

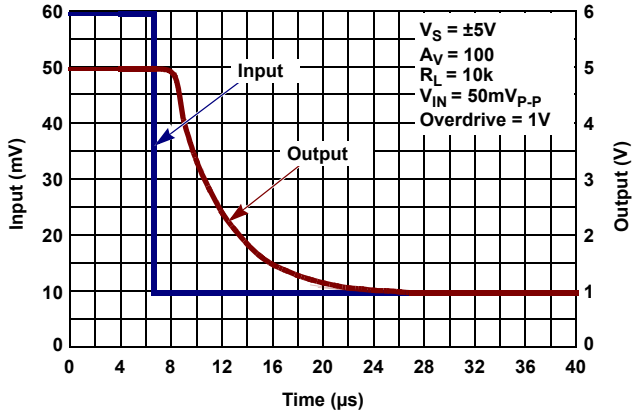


Figure 41. Positive Output Overload Response Time, V_S = ±5V

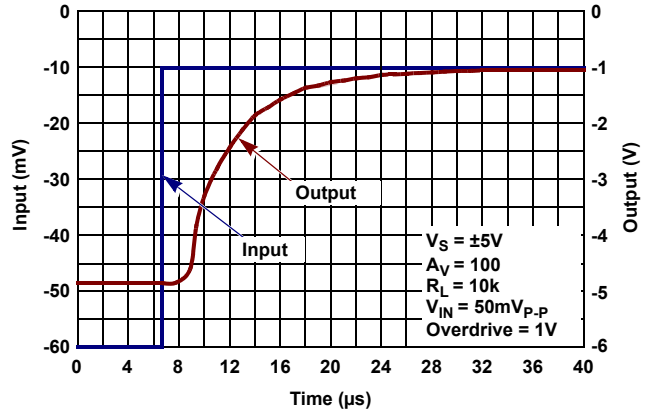


Figure 42. Negative Output Overload Response Time, V_S = ±5V

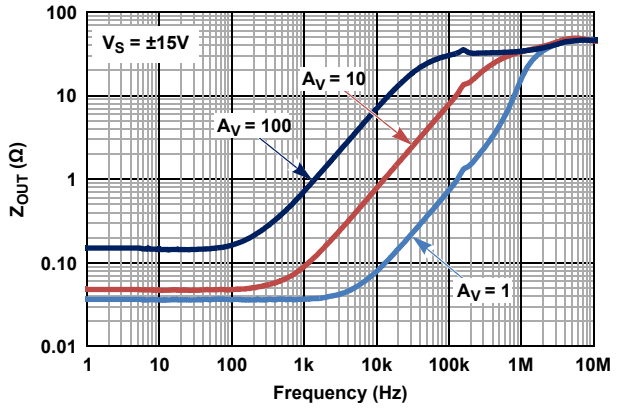


Figure 43. Output Impedance vs Frequency, V_S = ±15V

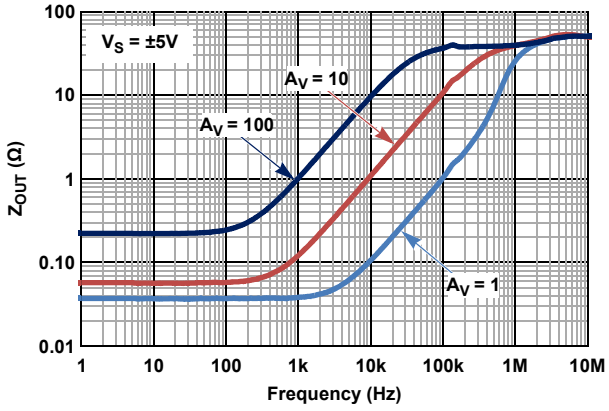


Figure 44. Output Impedance vs Frequency, V_S = ±5V

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. **(Continued)**

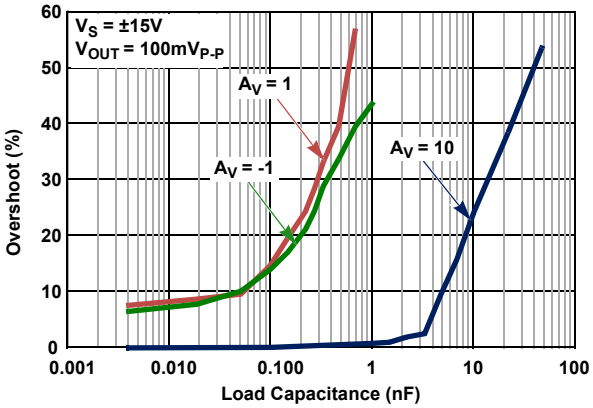


Figure 45. Overshoot vs Capacitive Load, V_S = ±15V

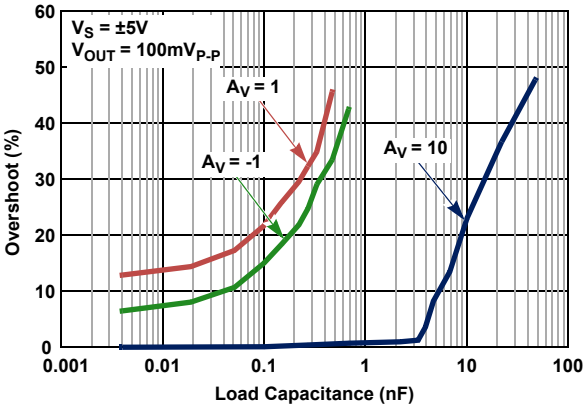


Figure 46. Overshoot vs Capacitive Load, V_S = ±5V

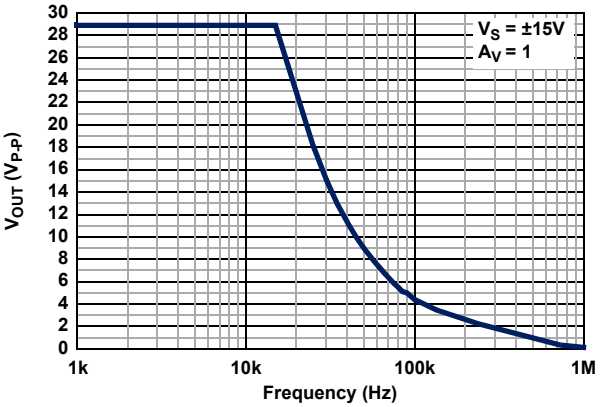


Figure 47. I_{MAX} Output Voltage vs Frequency

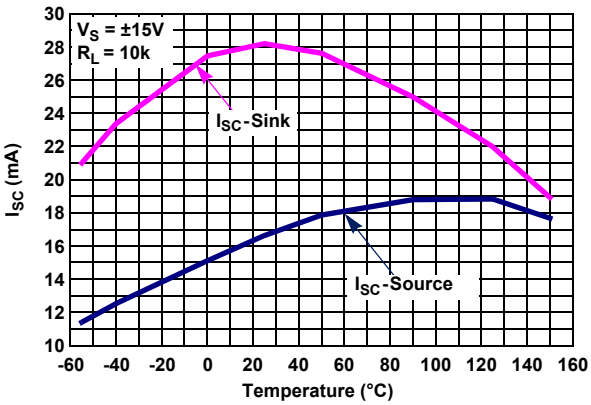


Figure 48. Short-Circuit Current vs Temperature, V_S = ±15V

4. Applications Information

4.1 Functional Description

The ISL71218M is a dual, 3.2MHz, single or dual supply, rail-to-rail output amplifier with a common-mode input voltage range extending to a range of 0.5V below the V^- rail. The input stage is optimized for precision sensing of ground-referenced signals in single-supply applications. The input stage is able to handle large input differential voltages without phase inversion, making this amplifier suitable for high-voltage comparator applications. The bipolar design features high open-loop gain and excellent DC input and output temperature stability. This op amp features very low quiescent current of 850µA, and low temperature drift. The device is fabricated in a new precision 40V complementary bipolar DI process and is immune from latch-up for up to a 36V supply range.

4.2 Operating Voltage Range

The op amp is designed to operate over a single supply range of 3V to 36V, or a split supply voltage range of +1.8V/-1.2V to ±18V. The device is fully characterized at 30V (±15V). Both DC and AC performance remain virtually unchanged over the complete operating voltage range. Parameter variation with operating voltage is shown in the "Typical Performance Curves".

The input common-mode voltage to the V^+ rail (V^+ - 1.8V across the full temperature range) may limit amplifier operation when operating from split V^+ and V^- supplies. Figure 4 shows the common-mode input voltage range variation over temperature.

4.3 Input Stage Performance

The ISL71218M PNP input stage has a common-mode input range extending up to 0.5V below ground at +25°C. Full amplifier performance is ensured for input voltage down to ground (V^-) across the -55°C to +125°C temperature range. For common-mode voltages down to -0.5V below ground (V^-), the amplifiers are fully functional, but performance degrades slightly over the full temperature range. This feature provides excellent CMRR, AC performance, and DC accuracy when amplifying low-level, ground-referenced signals. The input stage has a maximum input differential voltage equal to a diode drop greater than the supply voltage and does not contain the back-to-back input protection diodes found on many similar amplifiers. This feature enables the device to function as a precision comparator by maintaining very high input impedance for high-voltage differential input comparator voltages. The high differential input impedance also enables the device to operate reliably in large signal pulse applications, without the need for anti-parallel clamp diodes required on MOSFET and most bipolar input stage op amps. Thus, input signal distortion caused by nonlinear clamps under high slew rate conditions is avoided.

In applications in which one or both amplifier input terminals are at risk of exposure to voltages beyond the supply rails, current-limiting resistors may be needed at each input terminal (see Figure 49, R_{IN+}, R_{IN-}) to limit current through the power-supply ESD diodes to 20mA.

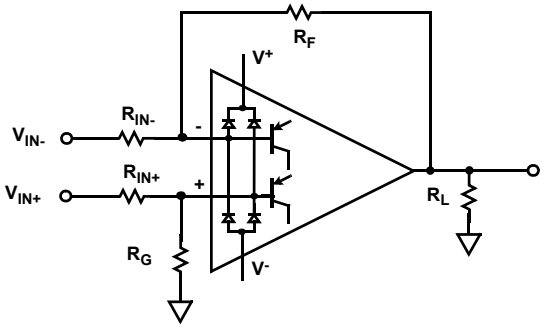


Figure 49. Input ESD Diode Current Limiting

4.4 Output Drive Capability

The bipolar rail-to-rail output stage features low saturation levels that enable an output voltage swing to less than 15mV when the total output load (including feedback resistance) is held below 50µA (Figure 21 and Figure 22). With ±15V supplies, this can be achieved by using feedback resistor values >300kΩ.

The output stage is internally current limited. Output current limit over temperature is shown in Figure 23 and Figure 24. The amplifiers can withstand a short-circuit to either rail as long as the power dissipation limits are not exceeded. This applies to only one amplifier at a time for the dual op amp. Continuous operation under these conditions may degrade long-term reliability.

The amplifiers perform well when driving capacitive loads (Figure 45 and Figure 46). The unity gain, voltage follower (buffer) configuration provides the highest bandwidth, but is also the most sensitive to ringing produced by load capacitance found in BNC cables. Unity gain overshoot is limited to 35% at capacitance values to 0.33nF. At gains of 10 and higher, the device is capable of driving more than 10nF without significant overshoot.

4.5 Output Phase Reversal

Output phase reversal is a change of polarity in the amplifier transfer function when the input voltage exceeds the supply voltage. The ISL71218M is immune to output phase reversal out to 0.5V beyond the rail ($V_{ABS\ MAX}$) limit (see Figure 38).

4.6 Single Channel Usage

The ISL71218M is a dual op amp. If the application requires only one channel, the user must configure the unused channel to prevent it from oscillating. The unused channel oscillates if the input and output pins are floating. This results in higher-than-expected supply currents and possible noise injection into the channel being used. The proper way to prevent oscillation is to short the output to the inverting input, and ground the positive input (Figure 50).

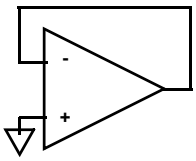


Figure 50. Preventing Oscillations in Unused Channels

4.7 Power Dissipation

It is possible to exceed the +150°C maximum junction temperatures under certain load and power supply conditions. It is therefore important to calculate the maximum junction temperature (T_{JMAX}) for all applications to determine if power supply voltages, load conditions, or package types need to be modified to remain in the safe operating area. These parameters are related using Equation 1:

(EQ. 1) $$T_{JMAX} = T_{MAX} + \theta_{JA} x PD_{MAXTOTAL}$$

where:

- $P_{DMAXTOTAL}$ is the sum of the maximum power dissipation of each amplifier in the package (PD_{MAX})
- T_{MAX} = Maximum ambient temperature
- θ_{JA} = Thermal resistance of the package

PD_{MAX} for each amplifier can be calculated using Equation 2:

(EQ. 2) $$PD_{MAX} = V_S \times I_{qMAX} + (V_S - V_{OUTMAX}) \times \frac{V_{OUTMAX}}{R_L}$$

where:

- PD_{MAX} = Maximum power dissipation of one amplifier
- V_S = Total supply voltage
- I_{qMAX} = Maximum quiescent supply current of one amplifier
- V_{OUTMAX} = Maximum output voltage swing of the application
- R_L = Load resistance

5. Radiation Tolerance

The ISL71218M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects, and Single Event Effects (SEE) has been measured, characterized, and reported in the proceeding sections. However, TID performance is not guaranteed through radiation acceptance testing, nor is the characterized SEE characterized performance guaranteed.

5.1 Total Ionizing Dose (TID) Testing

5.1.1 Introduction

Total dose testing of the ISL71218MBZ proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 11 samples irradiated under bias, as shown in Table 1, and 12 samples irradiated with all pins grounded (unbiased). Two control units were used. The bias configuration is shown in Figure 51.

Samples of the ISL71218MBZ-T were drawn from fabrication lot X8E5X and packaged in the production 8 Ld plastic SOIC (package outline drawing M8.15). The samples were screened to datasheet limits at room temperature only, before irradiation.

Total dose irradiations were performed using a Hopewell Designs N40 panoramic vault-type low dose rate 60Co irradiator located in the Resesas Palm Bay, Florida facility. The dose rate was 0.0089rad(Si)/s (8.9mrad(Si)/s). PbAl spectrum hardening filters were used to shield the test board and devices under test against low energy secondary gamma radiation.

Down-points for the testing were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). Following irradiation, the samples were subjected to a high temperature biased anneal for 168 hours at +100°C.

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each down-point. All down-point electrical testing was performed at room temperature.

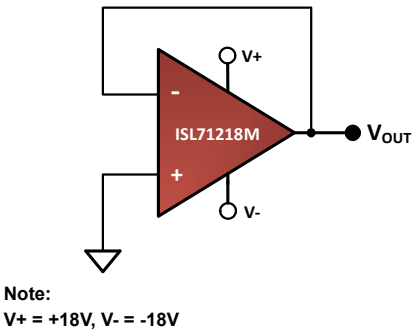


Figure 51. Irradiation Bias Configuration for the ISL71218M

5.1.2 Results

Table 1 summarizes the attributes data. “Bin 1” indicates a device that passes all the datasheet specification limits.

Table 1. ISL71218M Total Dose Test Attributes Data

Dose Rate mrad(Si)/s	Bias	Sample Size	Down Points	Bin 1/Rejects
8.9	Figure 51	11	Pre-Rad	11/0
			10krad(Si)	11/0
			20krad(Si)	11/0
			30krad(Si)	11/0
			Anneal	11/0
8.9	Grounded	12	Pre-Rad	12/0
			10krad(Si)	12/0
			20krad(Si)	12/0
			30krad(Si)	12/0
			Anneal	12/0

The plots in Figure 52 through Figure 58 show data for key parameters at all down points. The plots show the average as a function of total dose for each of the irradiation conditions; we chose to use the average because of the relatively large sample sizes. All parts showed excellent stability over irradiation.

Table 2 shows the average of other key parameters with respect to total dose in tabular form.

5.1.3 Typical Radiation Performance

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. The exposure rate for total ionizing dose was <10mrad(Si)/sec at +25°C.

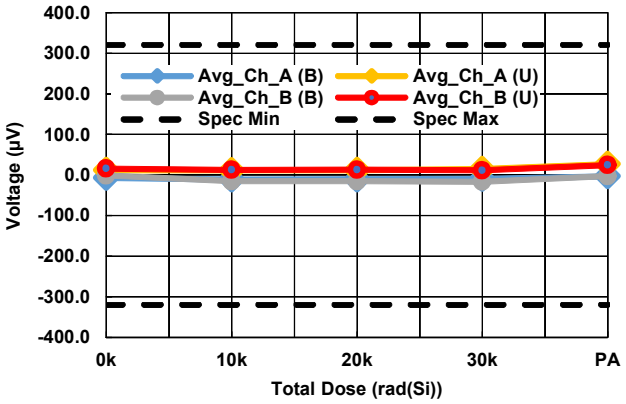


Figure 52. V_{OS} vs TID

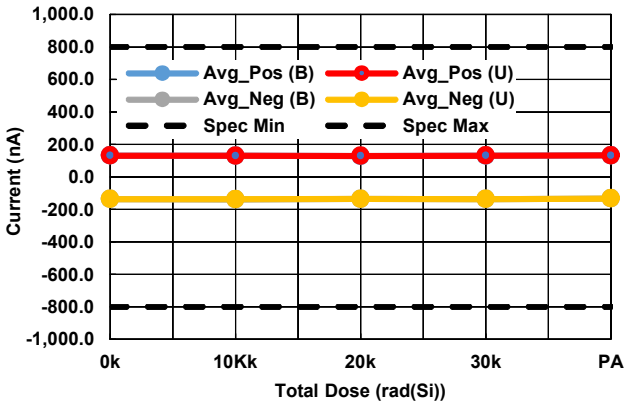


Figure 53. I_{BIAS} vs TID

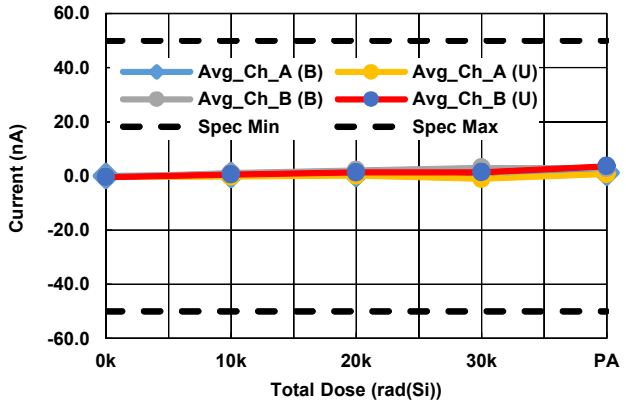


Figure 54. I_{OS} vs TID

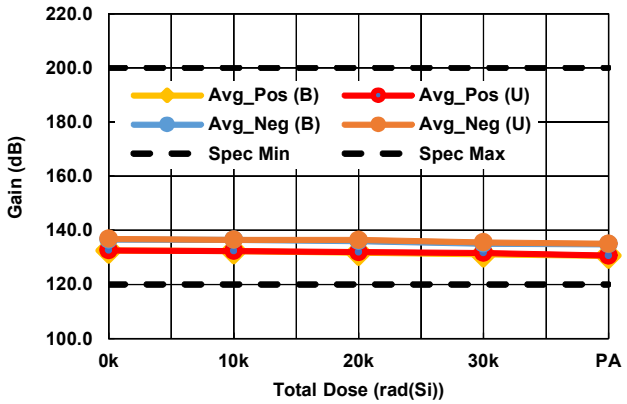


Figure 55. A_{VOL} vs TID

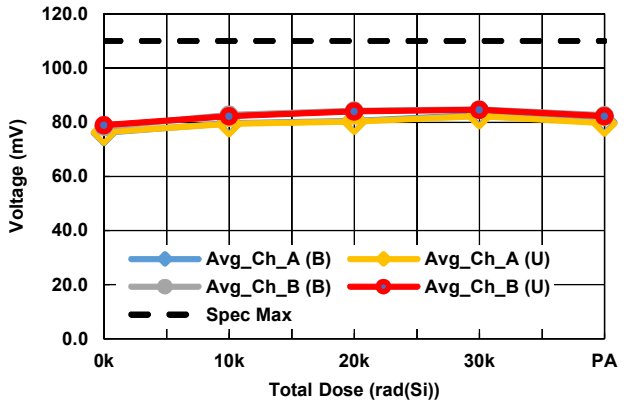


Figure 56. V_{OH} vs TID

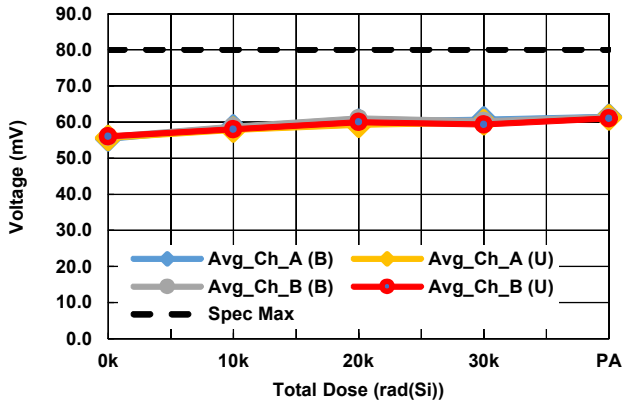


Figure 57. V_{OL} vs TID

V_S = ±15V, V_{CM} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. The exposure rate for total ionizing dose was <10mrad(Si)/sec at +25°C. **(Continued)**

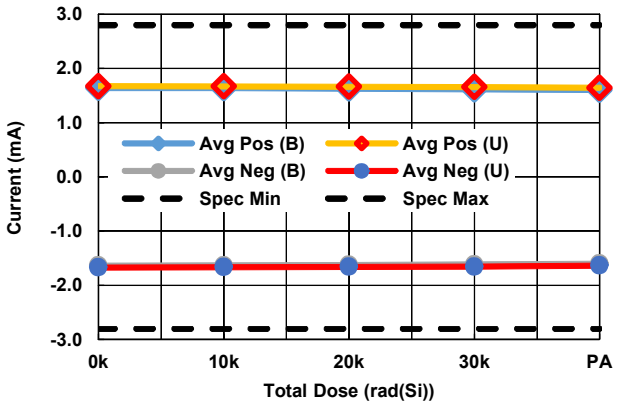


Figure 58. Supply Current vs TID

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V)

Test Parameter Name and Conditions	Symbol	V_{CC}	Irradiation Conditions	Pre-Rad Value	10k rad(Si)	20k rad(Si)	30k rad(Si)	Post Anneal	Units
Driver Electrical Characteristics									
Input Offset Voltage V_{CM} = 0V V_{CM} = V^+ to V^-	Vos	±15V	Biased	-3.98	-13.15	-13.05	-12.94	-2.81	µV
			Grounded	13.79	12.19	12.57	12.98	25.65	
		Datasheet Limit Min		**-230**	**-230**	**-230**	**-230**	**-230**	
		Datasheet Limit Max		**230**	**230**	**230**	**230**	**230**	
Input Offset Voltage Channel-to-Channel Match	ΔVos	±15V	Biased		-4.120	-4.683	-7.051	0.339	µV
			Grounded		1.267	1.090	-2.999	-2.310	
		Datasheet Limit Min		**-280**	**-280**	**-280**	**-280**	**-280**	
		Datasheet Limit Max		**280**	**280**	**280**	**280**	**280**	
Positive Input Bias Current V_{CM} = V^+ to V^-	I_{B+}	±15V	Biased	130.94	129.82	128.61	130.67	132.17	nA
			Grounded	131.13	130.08	128.89	130.97	132.46	
		Datasheet Limit Min		**0**	**0**	**0**	**0**	**0**	
		Datasheet Limit Max		**400**	**400**	**400**	**400**	**400**	
Negative Input Bias Current V_{CM} = V^+ to V^-	I_{B-}	±15V	Biased	-136.79	-138.25	-136.18	-136.78	-133.09	nA
			Grounded	-136.62	-137.99	-135.94	-136.54	-132.81	
		Datasheet Limit Min		**-400**	**-400**	**-400**	**-400**	**-400**	
		Datasheet Limit Max		**0**	**0**	**0**	**0**	**0**	
Input Offset Current V_{CM} = V^+ to V^-	I_{OS+}	±15V	Biased	-0.20	0.72	1.39	2.34	2.07	nA
			Grounded	-0.35	0.15	0.72	0.16	2.18	
		Datasheet Limit Min		**-50**	**-50**	**-50**	**-50**	**-50**	
		Datasheet Limit Max		**50**	**50**	**50**	**50**	**50**	
Positive Common-Mode Rejection Ratio V_{CM} = V^+ to V^-	$CMRR^+$	±15V	Biased	120.83	121.14	120.91	119.23	118.63	dB
			Grounded	121.90	121.99	122.08	121.90	123.72	
		Datasheet Limit Min		**100**	**100**	**100**	**100**	**100**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Continued)

Test Parameter Name and Conditions	Symbol	V_{CC}	Irradiation Conditions	Pre-Rad Value	10k rad(Si)	20k rad(Si)	30k rad(Si)	Post Anneal	Units
Negative Common-Mode Rejection Ratio V_{CM} = V+ to V-	$CMRR^-$	±15V	Biased	120.15	119.26	119.04	118.36	119.24	dB
			Grounded	121.15	122.64	122.75	123.12	122.68	
		Datasheet Limit Min		**100**	**100**	**100**	**100**	**100**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Positive Power Supply Rejection Ratio V_{CM} = V+ to V-	$PSRR^+$	±15V	Biased	122.03	122.01	122.13	122.38	122.77	dB
			Grounded	119.97	119.97	119.94	119.98	120.19	
		Datasheet Limit Min		**105**	**105**	**105**	**105**	**105**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Negative Power Supply Rejection Ratio V_{CM} = V+ to V-	$PSRR^-$	±15V	Biased	125.58	125.78	126.06	125.28	125.00	dB
			Grounded	126.81	126.28	126.07	126.02	128.33	
		Datasheet Limit Min		**105**	**105**	**105**	**105**	**105**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Positive Open-Loop Gain R_L = 10kΩ	A_{VOL+}	±15V	Biased	132.50	132.27	131.68	131.07	130.56	dB
			Grounded	132.59	132.36	131.91	131.61	130.65	
		Datasheet Limit Min		**120**	**120**	**120**	**120**	**120**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Negative Open-Loop Gain R_L = 10kΩ	A_{VOL-}	±15V	Biased	136.54	136.46	136.01	135.07	134.83	dB
			Grounded	136.80	136.50	136.39	135.53	135.02	
		Datasheet Limit Min		**120**	**120**	**120**	**120**	**120**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Output Voltage High R_L = 10kΩ	V_{OH}	±15V	Biased	77.17	81.23	82.34	83.72	81.27	mV
			Grounded	77.62	80.79	82.11	83.43	80.89	
		Datasheet Limit Min		**0**	**0**	**0**	**0**	**0**	
		Datasheet Limit Max		**110**	**110**	**110**	**110**	**110**	
Output Voltage Low R_L = 10kΩ	V_{OL}	±15V	Biased	55.63	58.63	60.56	60.48	61.40	mV
			Grounded	55.80	57.92	59.62	59.60	61.12	
		Datasheet Limit Min		**0**	**0**	**0**	**0**	**0**	
		Datasheet Limit Max		**80**	**80**	**80**	**80**	**80**	
Output Short-Circuit Current (Source) V_{OUT} = -18V	I_{src}	±15V	Biased	-19.83	-19.65	-19.32	-19.09	-18.67	mA
			Grounded	-19.90	-19.70	-19.45	-19.31	-18.75	
		Datasheet Limit Min		**10**	**10**	**10**	**10**	**10**	
		Datasheet Limit Max		**-**	**-**	**-**	**-**	**-**	
Output Short-Circuit Current (Sink) V_{OUT} = +18V	I_{snk}	±15V	Biased	31.87	31.84	31.74	31.66	31.08	mA
			Grounded	31.84	31.77	31.75	31.72	31.05	
		Datasheet Limit Min		**-10**	**-10**	**-10**	**-10**	**-10**	
		Datasheet Limit Max		**-**	**-**	**-**	**-**	**-**	
Positive Supply Current (Average per Channel)	I_{S+}	±15V	Biased	0.82	0.82	0.81	0.81	0.80	mA
			Grounded	0.84	0.83	0.83	0.83	0.82	
		Datasheet Limit Min		**-**	**-**	**-**	**-**	**-**	
		Datasheet Limit Max		**1.1**	**1.1**	**1.1**	**1.1**	**1.1**	

Table 2. ISL71218M Response of Key Parameters vs TID (V_S = ±15V) (Continued)

Test Parameter Name and Conditions	Symbol	V_{CC}	Irradiation Conditions	Pre-Rad Value	10k rad(Si)	20k rad(Si)	30k rad(Si)	Post Anneal	Units
Negative Supply Current (Average per channel)	I_{S-}	±15V	Biased	-0.82	-0.82	-0.81	-0.81	-0.80	mA
			Grounded	-0.84	-0.83	-0.83	-0.83	-0.82	
		Datasheet Limit Min		**-1.1**	**-1.1**	**-1.1**	**-1.1**	**-1.1**	
		Datasheet Limit Max		**-**	**-**	**-**	**-**	**-**	
Large Signal Slew Rate (Rising) V_{OUT} = +18V	SR+	±15V	Biased	1.17	1.17	1.17	1.17	1.14	V/µs
			Grounded	1.18	1.18	1.18	1.16	1.15	
		Datasheet Limit Min		**1**	**1**	**1**	**1**	**1**	
		Datasheet Limit Max		**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	
Large Signal Slew Rate (Falling) V_{OUT} = +18V	SR-	±15V	Biased	1.25	1.24	1.23	1.22	1.20	V/µs
			Grounded	1.26	1.25	1.24	1.24	1.21	
		Datasheet Limit Min		**1**	**1**	**1**	**1**	**1**	
		Datasheet Limit Max		**2.5**	**2.5**	**2.5**	**2.5**	**2.5**	
Output Rise Time R_L = 2kΩ	T_r	±15V	Biased	65.68	69.73	67.45	72.76	75.46	ns
			Grounded	63.49	68.43	67.01	64.70	73.23	
		Datasheet Limit Min		**-**	**-**	**-**	**-**	**-**	
		Datasheet Limit Max		**200**	**200**	**200**	**200**	**200**	
Output Fall Time R_L = 2kΩ	T_f	±15V	Biased	70.25	68.95	72.29	72.40	71.30	ns
			Grounded	70.18	68.26	72.11	71.71	69.84	
		Datasheet Limit Min		**-**	**-**	**-**	**-**	**-**	
		Datasheet Limit Max		**230**	**230**	**230**	**230**	**230**	
Positive Overshoot R_L = 2kΩ	OS+	±15V	Biased	0.05	0.04	0.04	0.05	0.03	%
			Grounded	0.05	0.04	0.04	0.04	0.03	
		Datasheet Limit Min		**-20**	**-20**	**-20**	**-20**	**-20**	
		Datasheet Limit Max		**20**	**20**	**20**	**20**	**20**	
Negative Overshoot R_L = 2kΩ	OS-	±15V	Biased	0.14	0.19	0.16	0.14	0.10	%
			Grounded	0.12	0.14	0.18	0.13	0.09	
		Datasheet Limit Min		**-20**	**-20**	**-20**	**-20**	**-20**	
		Datasheet Limit Max		**20**	**20**	**20**	**20**	**20**	

5.1.4 Conclusion

As shown in Table 2, and the selected graphs (Figure 52 through Figure 58), all parameters showed excellent stability over irradiation, with no observed bias sensitivity. Although, for brevity, only the ±15V results are shown; the ±5V results were just as stable.

5.2 Single Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single Event Effects (SEE). SEE can lead to system-level performance issues including disruption, degradation, and destruction. For predictable and reliable space system operation, individual electronic components should be characterized to determine their SEE response. The following is a summary of the SEE testing of the ISL71218M.

5.2.1 SEE Test Facility

Testing was performed at the Texas A&M University (TAMU) Cyclotron Institute heavy ion facility. This facility is coupled to a K500 superconducting cyclotron, which is capable of generating a wide range of test particles with the various energy, flux, and fluence level needed for advanced radiation testing.

5.2.2 SEE Test Setup

The part was tested for Single Event Burnout and Latch-up (SEB/L), using Au ions (LET = 43MeV•cm^2/mg) and Single Event Transient (SET) using Kr ions. The Device Under Test (DUT) was mounted in the beam line and irradiated with heavy ions of the appropriate species. The parts were assembled in 10 Ld dual in-line packages with the metal lid removed for beam exposure. The beam was directed onto the exposed die and the beam flux, beam fluence and errors in the device outputs were measured.

The tests were controlled remotely from the control room. All input power was supplied from portable power supplies connected using cable to the DUT. The supply currents were monitored along with the device outputs. All currents were measured with digital ammeters, while all the output waveforms were monitored on a digital oscilloscope for ease of identifying the different types of SEE, which the part displayed. Events were captured by triggering on changes in the output.

A schematic of the evaluation board is shown in Figure 59. Each op amp was set up in a gain of 11V/V. The IN- inputs were grounded and the input signal was applied to the IN+ pin.

Table 3. ISL71218M Oscilloscope Setup for SEE Testing

Scope	CH1	CH2	CH3	CH4	Trigger/Measurements
1	OUTA	OUTB	OUTA	OUTB	Trigger: OUTA, ±80mV window
2	OUTA	OUTB	OUTA	OUTB	Trigger: OUTB, ±80mV window

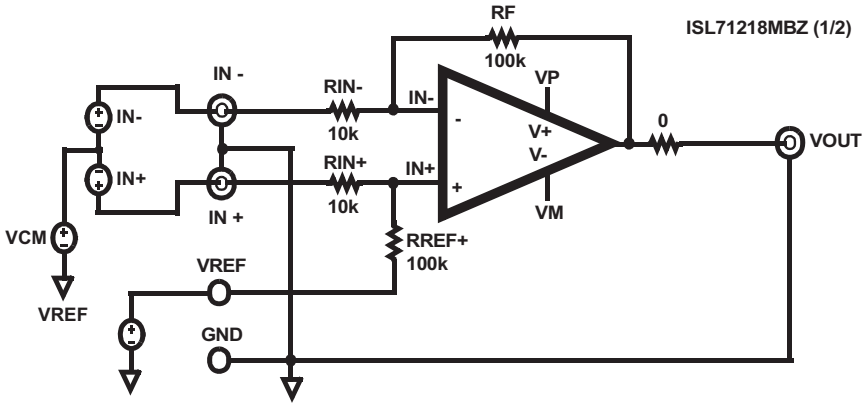


Figure 59. Simplified SEE Schematic

5.2.3 SEB/SEL Results

A failure due to burnout was indicated by a permanent change to the part's supply current after the beam was turned off. If the part's supply current reverted back to its pre-exposure value after a power cycle, the event was deemed as latch-up. A failure for burnout was indicated by a ±5% delta (which would allow for measurement repeatability) in supply current. The ISL71218M units did not exceed the aforementioned limit with V_S = ±20V at an LET of 43MeV•cm^2/mg and therefore are deemed as passing.

Table 4. ISL71218M SEB/L Results (V_S = ±20V, LET = 43MeV•cm^2/mg)

Unit	Temp (°C)	Supply Current Pre-Exposure		Supply Current Post-Exposure		SEB/L
		I+ (mA)	I- (mA)	I+ (mA)	I- (mA)	
1	+125°C	2.833	2.796	2.840	2.799	Pass
2	+125°C	3.036	2.998	3.042	3.001	Pass
3	+125°C	3.057	2.580	3.062	2.579	Pass
4	+125°C	2.888	2.410	2.892	2.413	Pass

5.2.4 SET Results

Figure 60 and Figure 61 show the typical SET performance of the ISL71218M at an LET of 28MeV•cm^2/mg with a fluence at 2x106/cm^2. In all cases the voltage deviations were within ±200mV of V_{OUT}. Transients were within 100µs and 600µs for V_S = ±18V and V_S = ±4.5V, respectively.

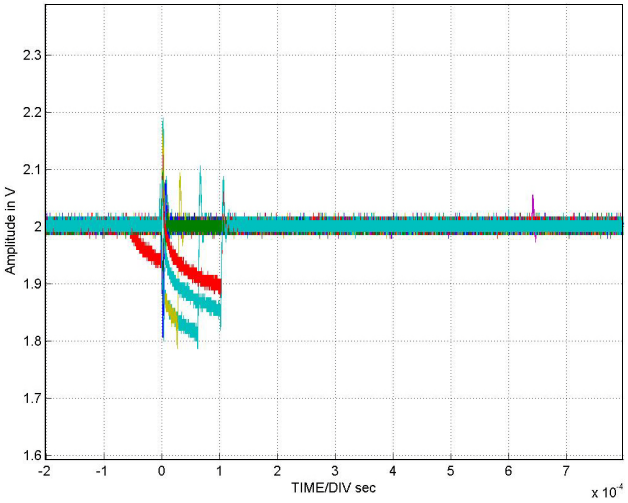


Figure 60. Typical Capture at LET of 28MeV•cm^2/mg (V_S = ±18V)

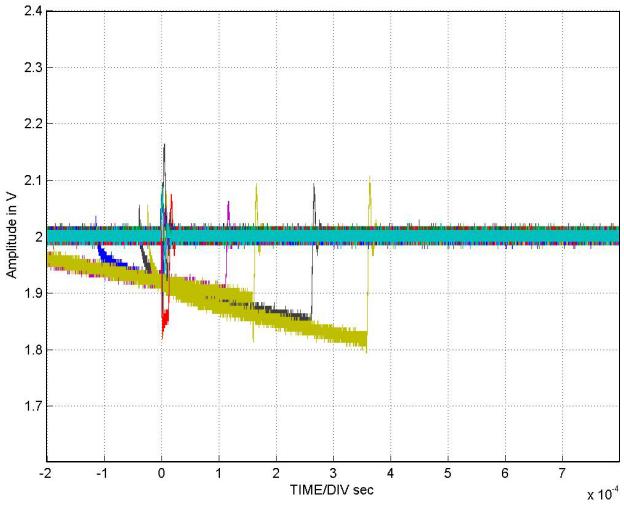


Figure 61. Typical Capture at LET of 28MeV•cm^2/mg (V_S = ±4.5V)

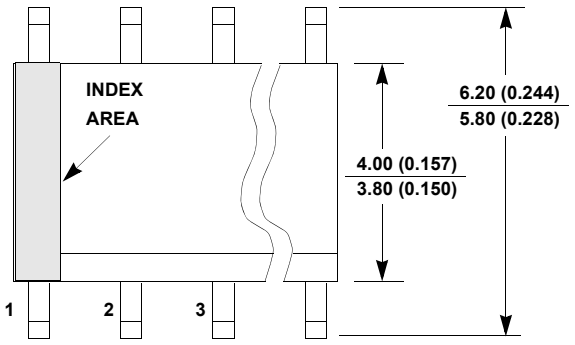
6. Revision History

Rev.	Date	Description
2.0	Jan 19, 2021	Updated links throughout Abs Max Ratings, Maximum Supply Voltage under beam - changed Max from 36V to 40V (page 4). Table 4 title, changed V_S = 20V to V_S = ±20V (on page 26). Updated Disclaimer
1.00	Mar 9, 2018	Features, page 1, added “Passes NASA Low Outgassing Specifications”. Ordering Information table, page 3, added Tape and Reel quantity column. Added tape and reel parts, and updated Note 1. Removed About Intersil section. Updated Disclaimer.
0.00	Sept 6, 2017	Initial release

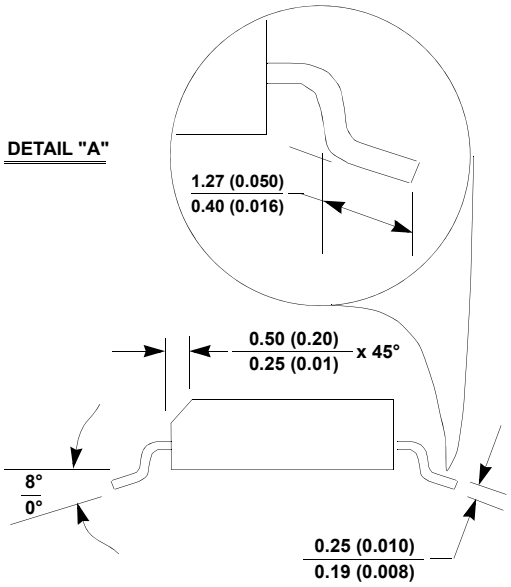
7. Package Outline Drawing

For the most recent package outline drawing, see M8.15.

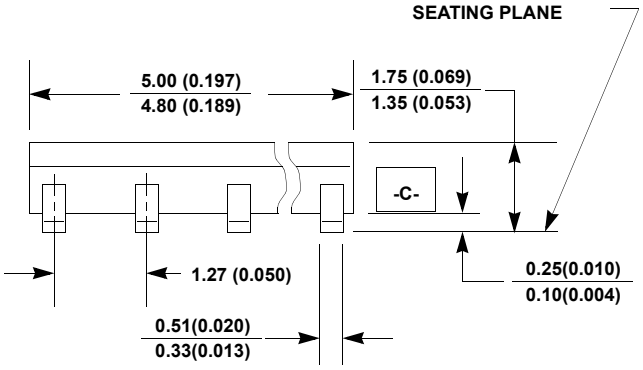
M8.15
8 Lead Narrow Body Small Outline Plastic Package
Rev 4, 1/12



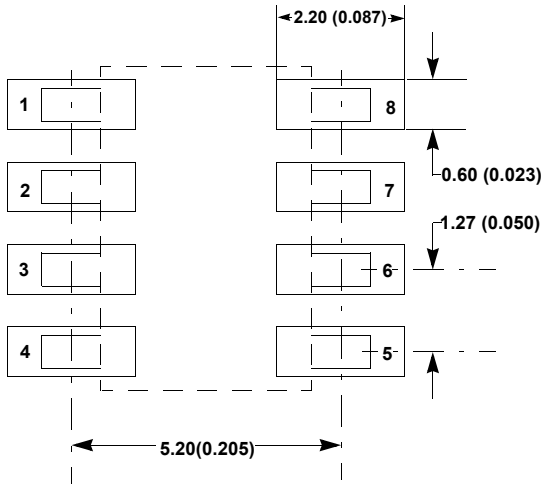
TOP VIEW



SIDE VIEW "B"



SIDE VIEW "A



TYPICAL RECOMMENDED LAND PATTERN

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

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(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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