ISL71441M

Radiation Tolerant 12V Half-Bridge GaN FET Driver

Description

The ISL71441M is a Radiation Tolerant PWM input 12V Half Bridge GaN FET Driver designed to drive low $r_{DS(ON)}$ Gallium Nitride (GaN) FETs for DC/DC switching regulators. An integrated programmable GaN FET gate drive voltage, high-side bootstrap switch, and strong gate drive current provide a compact and robust GaN FET half-bridge driver.

The ISL71441M can interface directly to the ISL73847M dual-phase PWM buck controller to create a high-efficiency point-of-load regulator to power many of the latest low voltage high current FPGA and DSP digital core rails.

The ISL71441M is offered in a 20Ld 5×5mm Quad Flat No-Lead (QFN) plastic package. It is specified to operate across an ambient temperature range of -55C to +125C.

Applications

- High current DC/DC Point-of-Load (POL) for FPGA and DSP supply rails
- 5V or 12V input to 1V output POL regulation
- GaN FET motor driver
- Combine with ISL73847M DC/DC PWM controller and Renesas GaN FETs for a complete DC/DC solution

Features

- Qualified to Renesas Rad Tolerant Screening and QCI Flow (R34TB0004EU)
- Up to 20V bootstrap voltage half-bridge driver
- Programmable 4.5V to 5.5V gate drive voltage
- Single tri-level PWM input control
- Separate source and sink driver outputs
- High-side peak drive: 2A Sourcing, 4A Sinking
- Low-side peak drive: 4A Sourcing, 8A Sinking
- High and low side programmable dead time control
- Highly matched fast propagation delay: 29ns
- Full military temperature operation T_A = -55°C to 125°C ambient range
- 20Ld Plastic 5×5mm QFN Package
- NiPdAu-Ag Lead finish (Sn-free, Pb-free)
- Passes NASA Low Outgassing Specifications
- TID Radiation Lot Acceptance Testing (LDR: ≤ 10mrad(Si)/s)
  - ISL71441M30RZ: 30krad(Si)
  - ISL71441M50RZ: 50krad(Si)
- SEE Characterization
  - No DSEE with V_{DD} = 20V, AVCC/PVCC = 6.3V, and PVIN = 16.5V at LET 46MeV·cm^2/mg
  - SEFI <10µm^2 at 46MeV·cm^2/mg
  - No Half-Bridge Shoot-Through SET at LET 46MeV·cm^2/mg

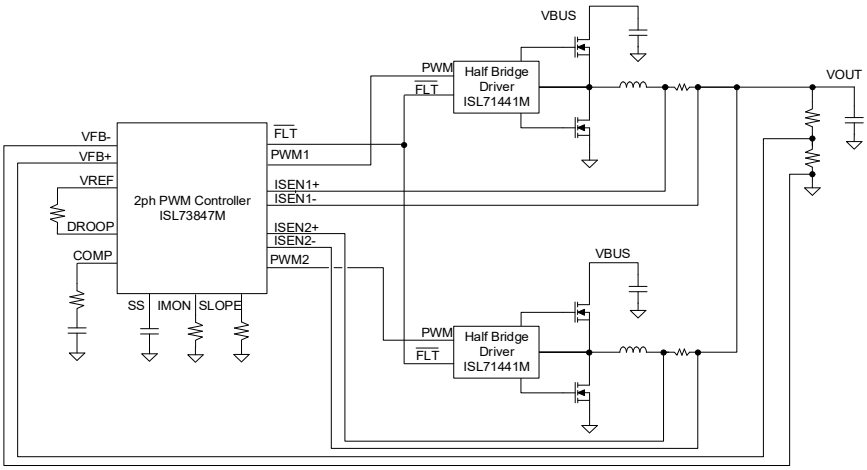


Figure 1. Typical Application Schematic: 2-Phase Controller + Bridge Driver + GaN FETs for 12V Input, 1.0V Output, 50A DC/DC Converter

Contents

1. Overview

1.1 Block Diagram

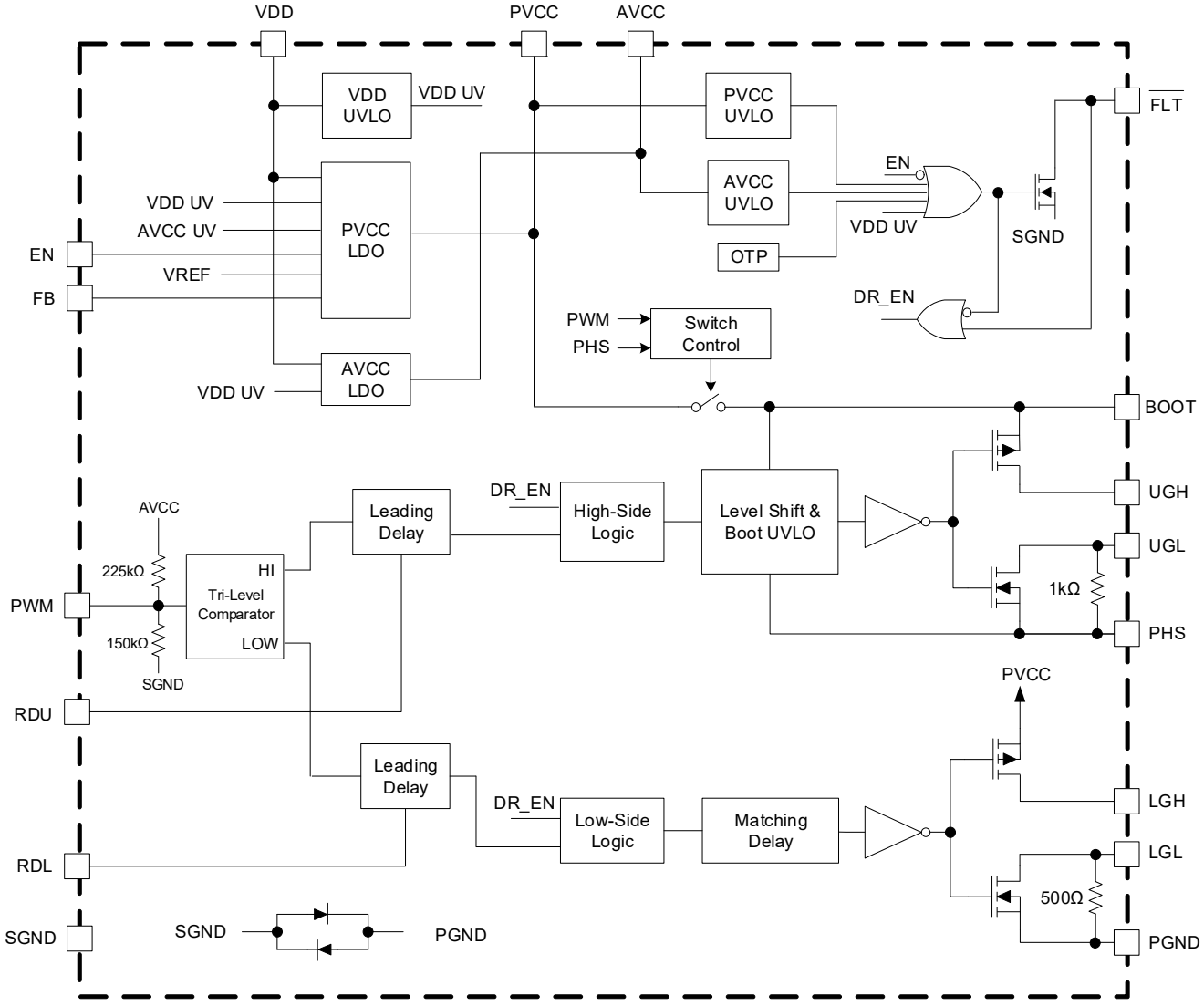


Figure 2. Circuit Block Diagram

2. Pin Information

2.1 Pin Assignments

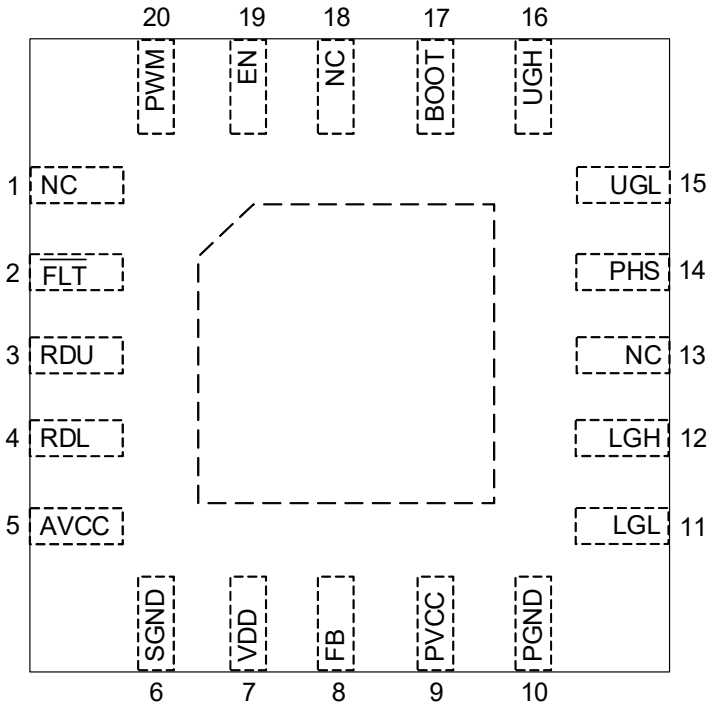


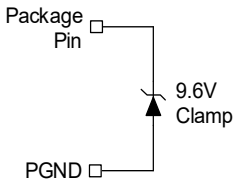
Figure 3. Pin Assignments - Top View[1]

1. The EPAD is notched on the corner to indicate pin 1 location.

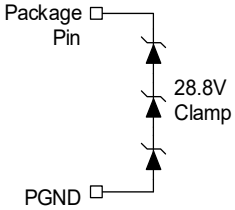
2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	NC	-	No connection
2	$\overline{FLT}$	1	I/O pin. As an open-drain output, $\overline{FLT}$ is an active low indicator for when EN = 0, VDD UVLO, AVCC UVLO, PVCC UVLO, or in an over-temperature fault. As a high-impedance input, $\overline{FLT}$ disables the driver outputs when driven low. Place a pull-up resistor on the $\overline{FLT}$ pin to AVCC. Place a 10pF capacitor from $\overline{FLT}$ to GND for SET mitigation.
3	RDU	1	Dead time delay control for the high-side turn-on. A 1.3kΩ-10kΩ resistor to SGND sets the rising edge delay of Upper Gate High (UGH) to the falling edge of Lower Gate Low (LGL) in the range of 6.5ns to 50ns.
4	RDL	1	Dead time delay control for low-side turn-on. A 1.3kΩ-10kΩ resistor to SGND sets the rising edge delay of Lower Gate High (LGH) to the falling edge of Upper Gate Low (UGL) in the range of 6.5ns-50ns.
5	AVCC	1	The output of the internal 5V LDO regulator for chip bias. Input is VDD. A minimum of 1µF ceramic decoupling capacitor is necessary on AVCC to SGND.
6	SGND	-	Analog signal GND pin. Connect to the EPAD and to the ground plane.
7	VDD	2	Input supply to chip. Recommended bias range is 4.75V to 13.2V.
8	FB	1	PVCC LDO error amplifier inverting input. A resistor divider network from FB to PVCC and SGND sets the PVCC LDO output voltage. If FB is connected to PVCC, PVCC output voltage is 4.5V.
9	PVCC	1	Output of the LDO for the gate drive voltage. Recommended PVCC range is 4.5V to 5.5V. A minimum 1µF ceramic decoupling capacitor is necessary on PVCC to PGND.

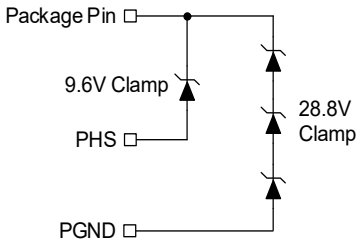
Pin Number	Pin Name	ESD Circuit	Description
10	PGND	-	Low-side driver output reference pin. For typical applications, connect PGND to the ground plane, EPAD, and SGND. Alternatively, connect PGND directly to the low-side transistor's source terminal.
11	LGL	5	Low-side sink driver for gate turn-off. Connect this pin to LGH and the GaN FET gate.
12	LGH	4	Low-side source driver for gate turn-on. Connect this pin to LGL and the GaN FET gate.
13	NC	-	No connection
14	PHS	3	High-side GaN FET source reference. Connect to the phase switching node of the half-bridge.
15	UGL	7	High-side sink driver for gate turn-off. Connect this pin to UGH and the GaN FET gate.
16	UGH	6	High-side source driver for gate turn-on. Connect this pin to UGL and the GaN FET gate.
17	BOOT	3	High-side bootstrap bias pin. Connect a bootstrap capacitor from this pin to PHS. An internal bootstrap switch connects PVCC to BOOT when PWM = 0V and PHS voltage is within 250mV of PGND.
18	NC	-	No connection
19	EN	2	Enable input pin. When EN is low, driver outputs are in a high-impedance state and do not respond to PWM inputs. The PVCC LDO is shut down, and the $\overline{FLT}$ pin is internally pulled low. When EN is high, the PVCC LDO is enabled, and the driver outputs respond to PWM inputs. EN pin is VDD voltage compliant.
20	PWM	1	Tri-Level PWM input pin. Logic high turns on the high-side gate driver. Logic low turns on the low-side gate driver. Mid-Level turns off both gate drivers. Internal pull-up and pull-down resistors bias pin to mid-level when not externally driven.
EPAD	-	-	Package bottom thermal pad. The die substrate is connected to EPAD. Connect to SGND and the ground plane.



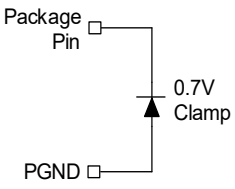
Circuit 1



Circuit 2



Circuit 3



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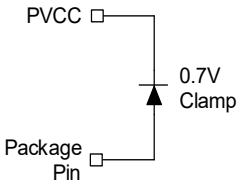

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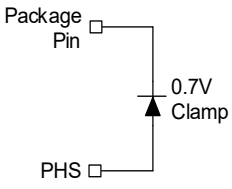

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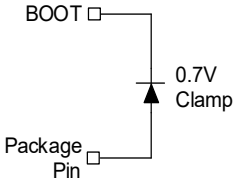


Circuit 7

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVCC to PGND; BOOT to PHS	-0.3	+6.5	V
VDD to SGND	-0.3	+20	V
SGND to PGND	-0.3	+0.3	V
PHS to PGND	-0.3V DC	+20	V
PHS to PGND (repetitive transient)	-5V (100ns)	-	V
BOOT to PGND	-0.3	+24	V
EN to SGND	-0.3	VDD+0.3	V
AVCC, FB, PWM, $\overline{FLT}$, RDU, RDL to SGND	-0.3	+6.5	V
UGH, UGL	PHS-0.3	BOOT+0.3	V
LGH, LGL	GND-0.3	PVCC+0.3	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	5	kV
Charged Device Model (Tested per JS-002-2018)	-	2	kV
Latch-Up (Tested per JESD78E; Class 2, Level A)	-	±100	mA

3.2 Outgas Testing

Specification (Tested per ASTM E595, 1.5)	Value	Unit
Total Mass Lost[1]	0.08	%
Collected Volatile Condensible Material[1]	0.01	%
Water Vapor Recovered	0.02	%

1. Outgassing results meet NASA requirements of total mass loss <1% and collected volatile condensible material <0.1%.

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	20Ld Plastic 5×5mm QFN Package	θ_{JA}[1]	Junction to air.	32	°C/W
		θ_{JC}[2]	Junction to case.	2	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temp location is the center of the package underside.

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
VDD Voltage	+4.75	+13.2	V

Parameter	Minimum	Maximum	Unit
PVCC	+4.5	+5.5	V
PHS	0	+13.2	V

3.5 Electrical Specifications

3.5.1 DC Electrical Specifications

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only).**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
VDD Power Supply							
Shutdown Supply Current	IDD_{SHDN}	EN = 0V	-55 to +125°C	-	850	**1200**	µA
Quiescent Supply Current	I_{DDQ}	PWM = Float; RDU = RDL = 1.3kΩ	-55 to +125°C	-	9	-	mA
		PWM = Float; RDU = RDL = 10kΩ		-	-	**6**	
Unloaded Operating Current	I_{DDO1}	UG and LG unloaded; PWM = 500kHz at 50% 0V to 5V	-55 to +125°C	-	21	**32**	mA
Loaded Operating Current	I_{DDO2}	5nF load on UG; 10nF load on LG; PWM = 500kHz at 50% 0V to 5V	-55 to +125°C	-	55	**70**	mA
Bootstrap Supply							
BOOT Quiescent Current	I_{Q_Boot}	PWM = Float; BOOT-PHS = 4.5V	-55 to +125°C	-	580	**650**	µA
PVCC and AVCC LDOs							
PVCC Feedback Voltage	VFB	Internal reference voltage	-55°C	1.184	1.2	1.208	V
			+25°C	1.188	1.2	1.212	
			+125°C	1.188	1.2	1.212	
PVCC Gate Drive Voltage	PVCC	PVCC = 4.5V = FB or with external resistors; I_{OUT} from 0mA to 150mA; VDD from 4.85V to 13.2V	-55°C	4.38	4.5	4.6	V
			+25°C	4.4	4.5	4.6	
			+125°C	4.38	4.5	4.6	
		PVCC = 5.5V with external FB resistors; I_{OUT} from 0mA to 150mA; VDD from 5.85V to 13.2V	-55°C	5.38	5.5	5.6	V
			+25°C	5.4	5.5	5.6	
			+125°C	5.38	5.5	5.6	
PVCC in Pass Mode	-	VDD = 4.75V; FB = PVCC; I_{OUT} = 150mA	-55 to +125°C	**4.34**	4.44	-	V
PVCC Dropout Voltage	-	I_{OUT} = 150mA; VDD voltage where PVCC drops 2% below regulation; PVCC = 4.5V to 5.5V	-55 to +125°C	-	190	**250**	mV
PVCC Output Current Limit	I_{LIMITP}	VDD = 4.75V; FB = PVCC; Force PVCC = 4.2V	-55 to +125°C	**190**	250	**350**	mA
VDD to PVCC Power Supply Rejection Ratio	$PVCC_{PSRR}$	VDD = 6V + 300mVpp AC 1kHz; PVCC = 5.5V; PVCC I_{OUT} = 150mA	-	-	70	-	dB
		VDD = 6V + 300mVpp AC 100kHz; PVCC = 5.5V; PVCC I_{OUT} = 150mA	-	-	30	-	

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only).** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
Internal LDO voltage	AVCC	VDD = 4.97V; I_{OUT} = 20mA	-55 to +125°C	**4.3**	4.6	**4.69**	V
		VDD = 5.25V to 13.2V; I_{OUT} = 0mA to 20mA		**4.7**	5.0	**5.4**	
Dropout Voltage		I_{OUT} = 20mA; VDD voltage where AVCC drops 2% below regulation	-55 to +125°C	-	-	**250**	mV
AVCC Output Current Limit	I_{LIMITA}	VDD = 4.75V; Force AVDD = 4.5V	-55 to +125°C	**25**	49	**100**	mA
VDD to AVCC Power Supply Rejection Ratio	$AVCC_{PSRR}$	VDD = 6V + 300mVpp AC 1kHz; AVCC = 5V; AVCC I_{OUT} = 20mA	-	-	70	-	dB
		VDD = 6V + 300mVpp AC 100kHz; AVCC = 5V; AVCC I_{OUT} = 20mA	-	-	30	-	
VDD Undervoltage Lockout (UVLO)							
VDD UVLO Rising Threshold	VR_{VDD}	-	-55 to +125°C	**4.46**	4.6	**4.74**	V
VDD UVLO Falling Threshold	VF_{VDD}	-		**4.41**	4.55	**4.68**	V
VDD UVLO Hysteresis	VH_{VDD}	VR_{VDD} - VF_{VDD}		**25**	50	**90**	mV
AVCC Undervoltage Lockout (UVLO)							
AVCC UVLO Rising Threshold	VR_{AVCC}	Test by recovering AVCC from constant current limit	-55 to +125°C	**4.46**	4.6	**4.74**	V
AVCC UVLO Falling Threshold	VF_{AVCC}	Test by putting AVCC into constant current limit		**4.28**	4.41	**4.52**	V
AVCC UVLO Hysteresis	VH_{AVCC}	VR_{AVCC} - VF_{AVCC}		**150**	183	**300**	mV
PVCC Undervoltage Lockout (UVLO)							
PVCC UVLO Rising Threshold	VR_{PVCC}	PVCC = 5.5V with FB resistors[3]	-55 to +125°C	**5.21**	5.34	**5.45**	V
PVCC UVLO Falling Threshold	VF_{PVCC}	PVCC = 5.5V with FB resistors[3]		**5.07**	5.17	**5.27**	V
PVCC UVLO Hysteresis	VH_{PVCC}	VR_{PVCC} - VF_{PVCC}		**100**	150	**300**	mV
BOOT Undervoltage Lockout (UVLO)							
BOOT UVLO Rising Threshold	VR_{BOOT}	-	-55 to +125°C	**3.8**	4.0	**4.2**	V
BOOT UVLO Falling Threshold	VF_{BOOT}	-		**3.6**	3.8	**4.0**	V
BOOT UVLO Hysteresis	VH_{BOOT}	VR_{BOOT} - VF_{BOOT}		**100**	240	**400**	mV
PWM and EN Input Pins							
EN High Level Threshold	VIH_{EN}	PWM = 0V	-55 to +125°C	-	1.8	**2.0**	V
EN Low Level Threshold	VIL_{EN}	PWM = 0V		**1.0**	1.5	-	V
EN Input Hysteresis	$VHYS_{EN}$	VIH_{EN} - VIL_{EN}		**100**	325	**400**	mV

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only).** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
PWM High Threshold	V_{PWMH}	VDD = 4.75V to 13.2V	-55 to +125°C	-	2.7	**2.8**	V
PWM Middle Level Range	V_{PWMM}	VDD = 4.75V to 13.2V		**1.45**	-	**2.4**	V
PWM Low Threshold	V_{PWML}	VDD = 4.75V to 13.2V		**0.95**	1.1	-	V
Mid-High Level Hysteresis	-	VDD = 4.75V to 13.2V		-	100	**200**	mV
Mid-Low Level Hysteresis	-	VDD = 4.75V to 13.2V		-	200	**350**	mV
PWM High Input Current	I_{PWMH}	PWM = 5V		**10**	33	**50**	µA
PWM Low Input Current	I_{PWML}	PWM = 0V		**-50**	-22	**-10**	µA
PWM Pin Pull-Up Resistor	R_{PWMU}	-		**150**	225	**300**	kΩ
PWM Pin Pull-Down Resistor	R_{PWML}	-		**100**	150	**200**	kΩ
PWM Pin Floating Voltage	V_{FLOAT}	-		**1.90**	2.0	**2.135**	V
Bootstrap FET Switch							
Low Current Voltage	V_{SWL}	100µA through switch	-55 to +125°C	-	1	**1.6**	mV
High Current Voltage	V_{SWH}	100mA through switch		-	-	**145**	mV
BOOT Switch Resistance	R_{SW}	100mA through switch		-	-	**1.45**	Ω
Positive Window Detect Rising Threshold	-	PWM = 0V		**160**	250	**400**	mV
Positive Window Detect Falling Threshold	-	PWM = 0V		**140**	220	**380**	mV
Negative Window Detect Rising Threshold	-	PWM = 0V		**-380**	-210	**-140**	mV
Negative Window Detect Falling Threshold	-	PWM = 0V		**-400**	-240	**-160**	mV
Positive Window Detect Hysteresis	-	PWM = 0V		**10**	25	**60**	mV
Negative Window Detect Hysteresis	-	PWM = 0V		**10**	20	**60**	mV
$\overline{FLT}$ Open Drain with Internal Detect							
Input High Leakage Current	I_{LEAK}	$\overline{FLT}$ = AVCC; VDD = 13.2V EN = VDD; No fault condition	-55 to +125°C	**-1**	-	**1**	µA
$\overline{FLT}$ Output Low Drive	V_{OL}	I_{SINK} = 10mA; EN = 0V		-	0.18	**0.4**	V
Fault Detect Input High Threshold	V_{IH}	VDD = 13.2V; EN = VDD		**2.0**	2.4	**2.8**	V
Fault Detect Input Low Threshold	V_{IL}	VDD = 13.2V; EN = VDD		**1.0**	1.6	**2.0**	V

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V; T_A= 25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only).** (Cont.)

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ.[2]	Max[1]	Unit
Upper Gate High Output (UGH)							
UGH Peak Source Current	$IUGH_{SRC}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 5V; 470nF load on UG-PHS	-	-	2	-	A
UGH Output High Voltage	VOH_{UGH}	I_{SOURCE} = 100mA; Voltage drop below BOOT	-55 to +125°C	-	90	**130**	mV
Lower Gate High Output (LGH)							
LGH Peak Source Current	$ILGH_{SRC}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 0V; 1µF load on LG-PGND	-	-	4	-	A
LGH Output High Voltage	VOH_{LGH}	I_{SOURCE} = 100mA; Voltage drop below PVCC	-55 to +125°C	-	56	**90**	mV
Upper Gate Low Output (UGL)							
UGL Peak Sink Current	$IUGL_{SNK}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 0V; 470nF load on UG-PHS	-	-	4	-	A
UGL Output Low Voltage	VOL_{UGL}	I_{SINK} = 100mA; Voltage above PHS	-55 to +125°C	-	50	**80**	mV
UGL Gate Discharge Resistor	RUGL	EN = 0		**800**	1000	**1400**	Ω
Lower Gate Low Output (LGL)							
LGL Peak Sink Current	$ILGL_{SNK}$	VDD = 4.75V; FB = PVCC; BOOT-PHS = 4.5V; PWM = 5V; 1µF load on LG-PGND	-	-	8	-	A
LGL Output Low Voltage	VOL_{LGL}	I_{SINK} = 100mA; Voltage above GND	-55 to +125°C	-	27	**50**	mV
LGL Gate Discharge Resistor	RLGL	EN = 0		**400**	500	**700**	Ω
Over-Temperature Protection (OTP)							
Rising Thermal Shutdown	OTPR	-	-	-	160	-	°C
Falling Thermal Recovery	OTPF	-	-	-	145	-	°C
Driver Response Time to Thermal Shutdown	-	Design simulation	-	-	45	-	µs

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C.
2. Typical values are not guaranteed.
3. UVLO for PVCC is detected on the FB pin. PVCC UVLO thresholds are set at 96.5% rising and 94% falling, typical at +25°C, of the set PVCC voltage. PVCC UVLO thresholds production tested only at PVCC set to 5.5V.

3.5.2 AC Electrical Specifications

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only).**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
Dead Time Delay; RDU and RDL							
Dead Time Delay LG falling to UG rising	t_{DTLU}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND	-55 to +125°C	-	6.5	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**40**	50	**55**	ns
Dead Time Delay UG falling to LG rising	t_{DTUL}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND		-	6.5	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**40**	50	**55**	ns
Dead Time Delay Match t_{DTLU} - t_{DTUL}	t_{DTM}	VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 1.3kΩ to GND		-	-0.2	-	ns
		VDD = 4.75V to 5.85V; PVCC = BOOT-PHS = 4.5V to 5.5V; RDU = RDL = 10kΩ to GND		**-3.5**	-	**3.5**	ns
PWM Propagation Delay							
UG Turn-Off Propagation Delay PWM Falling to UG Falling	t_{PDUG}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V	-55°C	**20**	27	**32**	ns
			+25°C	**23**	29	**35**	ns
			+125°C	**27**	33	**40**	ns
LG Turn-Off Propagation Delay PWM Rising to LG Falling	t_{PDLG}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V	-55°C	**20**	27	**32**	ns
			+25°C	**23**	29	**35**	ns
			+125°C	**27**	33	**40**	ns
Propagation Delay Match t_{PDUG} - t_{PDLG}	t_{PDM}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V Over-Temperature and Radiation	-55 to +125°C	**-2.5**	0	**2.5**	ns
PWM Enter Mid-Level to UG Low Delay Time	t_{PDUG1}	PWM [High to Mid] to UG Falling; RDU = RDL = 1.3kΩ	-55 to +125°C	-	80	-	ns
PWM Exit Mid-Level to UG High Delay Time	t_{PDUG2}	PWM [Mid to High] to UG Rising; RDU = RDL = 1.3kΩ		-	65	-	ns
PWM Enter Mid-Level to LG Low Delay Time	t_{PDLG1}	PWM [Low to Mid] to LG Falling; RDU = RDL = 1.3kΩ		-	80	-	ns
PWM Exit Mid-Level to LG Rising Delay Time	t_{PDLG2}	PWM [Mid to Low] to LG Rising; RDU = RDL = 1.3kΩ		-	65	-	ns

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
UG and LG Transition Times							
UG Rise Time	t_{UGR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 5nF; 10% to 90%	-55 to +125°C	-	-	**25**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 470nF; 30% to 70%	-55°C	300	470	620	ns
			+25°C	410	530	680	ns
			+125°C	480	660	780	ns
UG Fall Time	t_{UGF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 5nF; 90% to 10%	-55 to +125°C	-	-	**25**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; UG C_{LOAD} = 470nF; 70% to 30%	-55°C	150	260	330	ns
			+25°C	220	280	360	ns
			+125°C	260	330	420	ns
LG Rise Time	t_{LGR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; LG C_{LOAD} = 10nF; 10% to 90%	-55 to +125°C	-	-	**34**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; LG C_{LOAD} = 940nF; 30% to 70%	-55°C	360	550	700	ns
			+25°C	470	620	800	ns
			+125°C	600	770	950	ns
LG Fall Time	t_{LGF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V LG C_{LOAD} = 10nF; 90% to 10%	-55 to +125°C	-	-	**30**	ns
		VDD = 4.75V; PVCC = BOOT-PHS = 4.5V LG C_{LOAD} = 940nF; 70% to 30%	-55°C	150	240	420	ns
			+25°C	220	270	450	ns
			+125°C	260	350	520	ns
Mode Transition Delay							
PVCC Start-Up Delay	-	VDD = 4.75V; PVCC = FB; C_{PVCC} = 1.0µF; EN High to PVCC crossing 0.5V	-	-	115	-	µs
PVCC Start-Up Time	-	VDD = 4.75V; PVCC = FB; C_{PVCC} = 1.0µF; PVCC rise time from 0.45V to 4.05V (10% to 90% of 4.5V)	-	-	15	-	µs

Unless otherwise specified: VDD = 13.2V; EN = VDD; PVCC = 5.5V; C_{PVCC} = 2.2µF; C_{AVCC} = 2.2µF; C_{BOOT} = 100nF to PHS; PHS = PGND = 0V, T_A=25°C. UG is defined as UGH = UGL. LG is defined as LGH = LGL. **Boldface limits apply across the operating temperature range, -55°C to +125°C by characterization with production testing at +25°C; over a total ionizing dose of 30krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M30RZ); or over a total ionizing dose of 50krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s (ISL71441M50RZ only). (Cont.)**

Parameter	Symbol	Test Conditions	Temp.	Min[1]	Typ[2]	Max[1]	Unit
EN High to Driver Output Enabled Delay Time	t_{ENR}	VDD = PVCC = FB = BOOT-PHS = 4.75V	-55 to +125°C	**70**	95	**130**	µs
EN Low to Driver Output Disabled Delay Time	t_{ENF}	EN Low to UG Off; PWM = 5V EN Low to LG Off; PWM = 0V		-	4	**8**	µs
$\overline{FLT}$ Low to LG Output Falling	t_{FLTF}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; EN = VDD; PWM = 0V; $\overline{FLT}$ exercised as an input pin High to Low		-	200	**300**	ns
$\overline{FLT}$ High to LG Output Rising	t_{FLTR}	VDD = 4.75V; PVCC = BOOT-PHS = 4.5V; EN = VDD; PWM = 0V; $\overline{FLT}$ exercised as an input pin Low to High		-	300	**400**	ns
PVCC Falling Below UVLO to $\overline{FLT}$ Falling Delay	t_{PVCCF}	FB = PVCC	-	-	0.6	-	µs
PVCC Falling Below UVLO to UG Falling Delay		FB = PVCC; PWM = 5V	-	-	0.8	-	µs
PVCC Falling Below UVLO to LG Falling Delay		FB = PVCC; PWM = 0V	-	-	0.5	-	µs
PVCC Rising Above UVLO to $\overline{FLT}$ Rising Delay	t_{PVCCR}	FB = PVCC	-	-	0.6	-	µs
PVCC Rising Above UVLO to UG Rising Delay		FB = PVCC; PWM = 5V	-	-	1.0	-	µs
PVCC Rising Above UVLO to LG Rising Delay		FB = PVCC; PWM = 0V	-	-	1.0	-	µs
BOOT Falling Below UVLO to UG Falling Delay	t_{BOOTF}	FB = PVCC; PWM = 5V BOOT-PHS falling 4.5V to 3.5V	-	-	1.5	-	µs
BOOT Rising Above UVLO to UG Rising Delay	t_{BOOTR}	FB = PVCC; PWM = 5V; BOOT-PHS rising 3.5V to 4.5V	-	-	1.8	-	µs

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C..
2. Typical values are not guaranteed.

3.6 Timing Diagrams

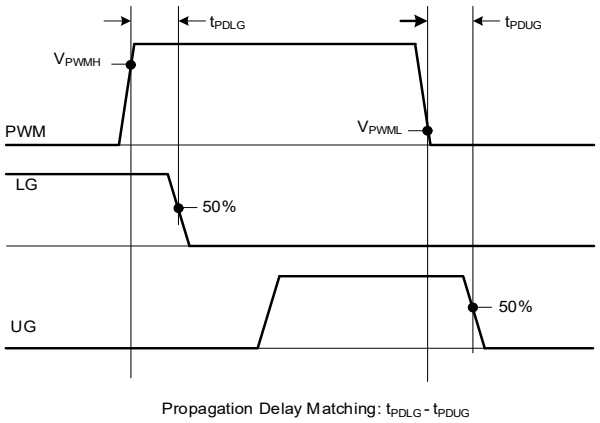


Figure 4. PWM Propagation Delay

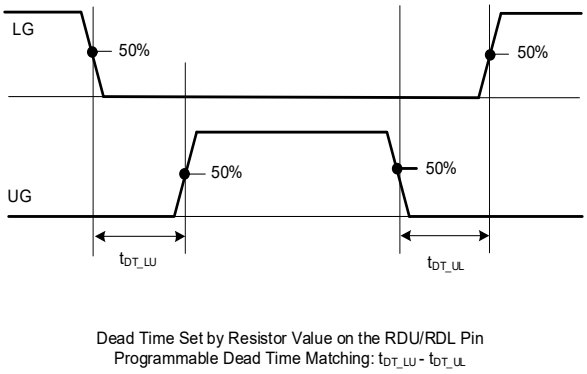


Figure 5. Programmable Dead Time

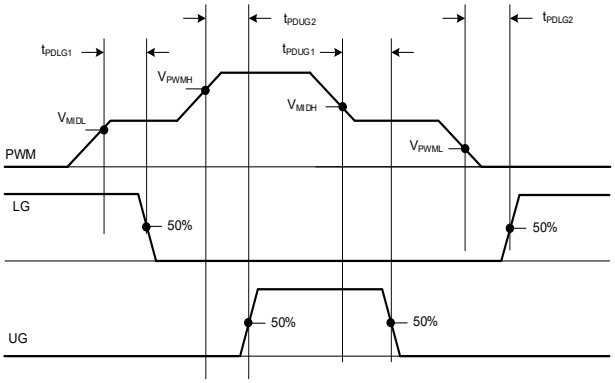


Figure 6. PWM Mid Level Propagation Delay

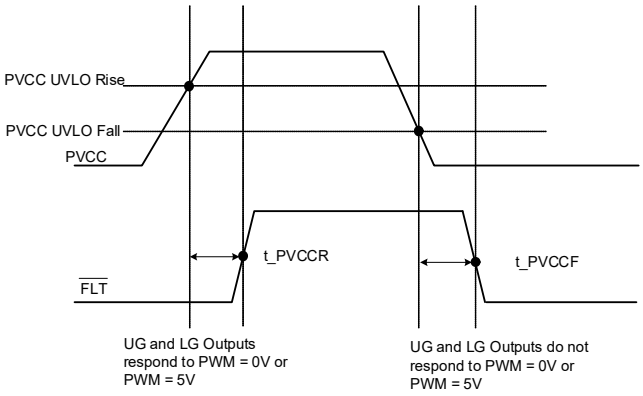


Figure 7. PVCC UVLO to $\overline{FLT}$ Propagation Delay

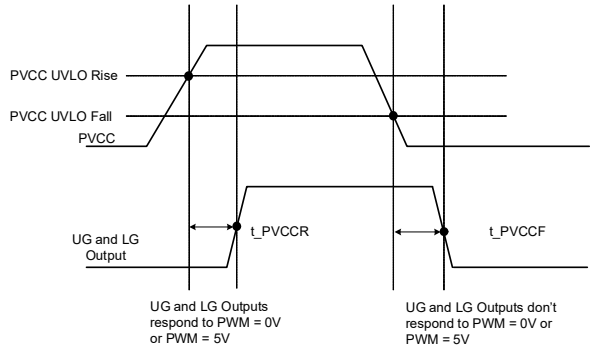


Figure 8. PVCC UVLO to UG & LG Propagation Delay

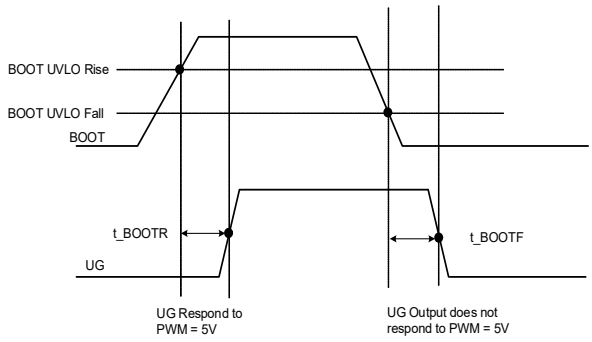


Figure 9. BOOT UVLO to UG Propagation Delay

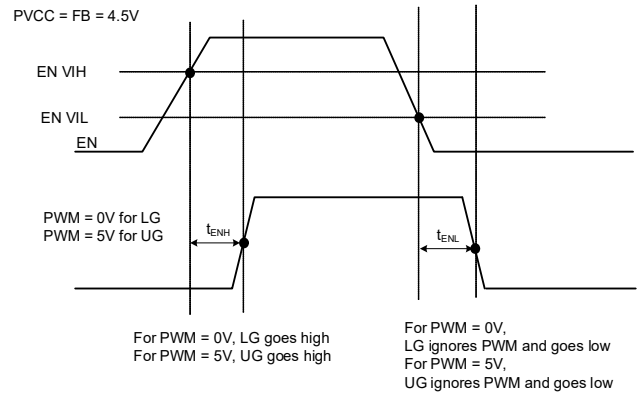


Figure 10. EN Propagation Delay

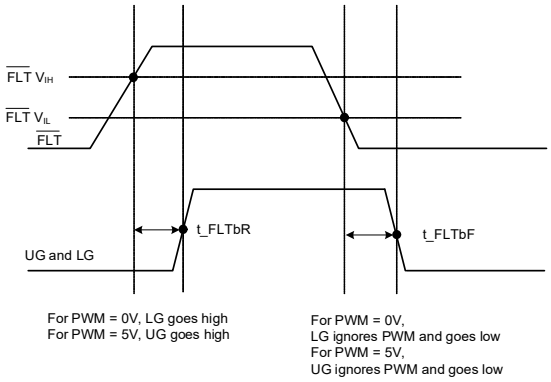


Figure 11. $\overline{\text{FTL}}$ Propagation Delay (External Driven)

4. Typical Performance Curves

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

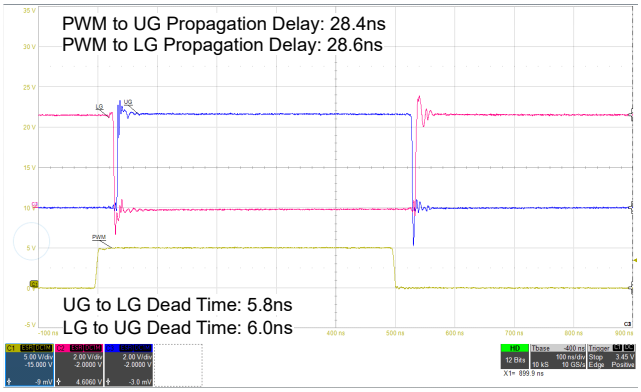


Figure 12. Prop Delay & Dead Time Delay with RDU = RDL = 1.3kΩ

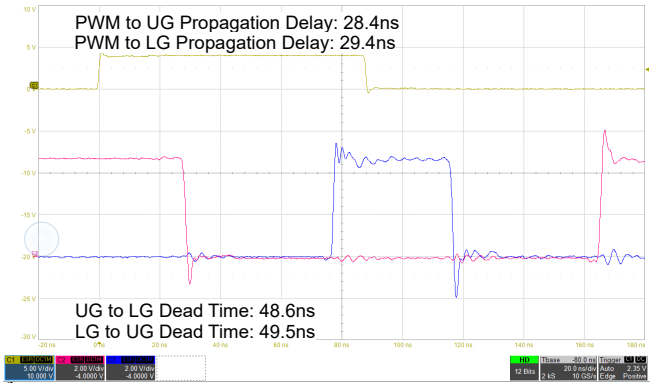


Figure 13. Prop Delay & Dead Time Delay with RDU = RDL = 10kΩ

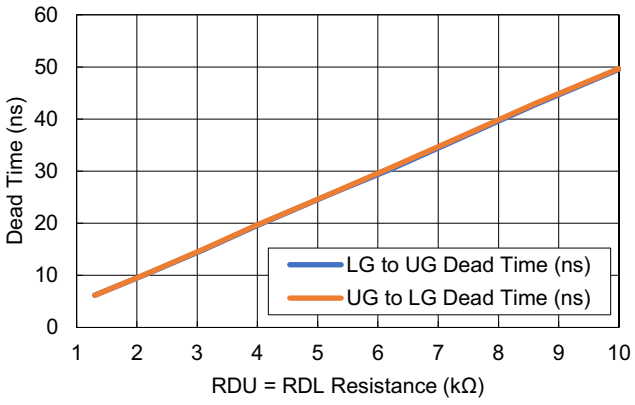


Figure 14. Programmable Dead Time Range 1.3kΩ to 10kΩ

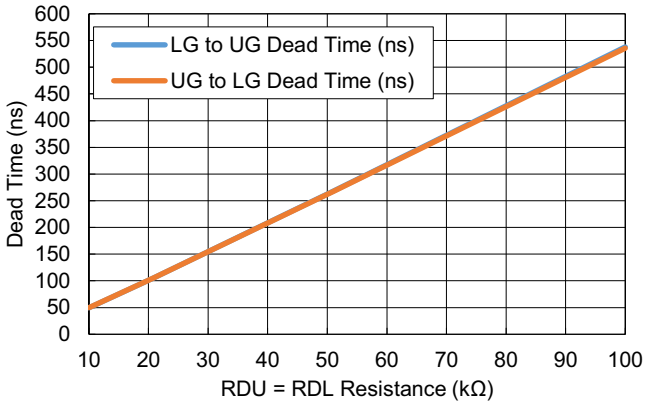


Figure 15. Programmable Dead Time Range 10kΩ to 100kΩ

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

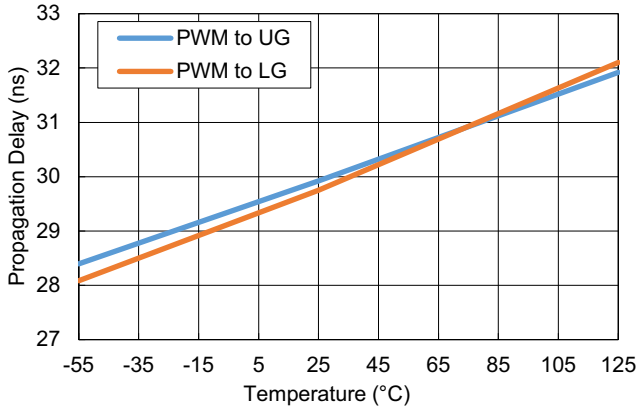


Figure 16. Propagation Delay vs Temperature

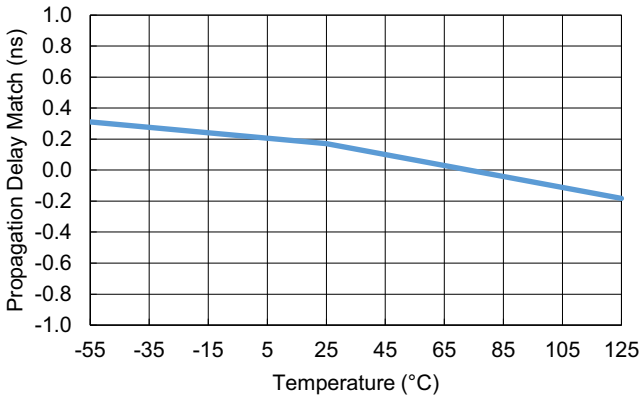


Figure 17. Propagation Delay Matching vs Temperature

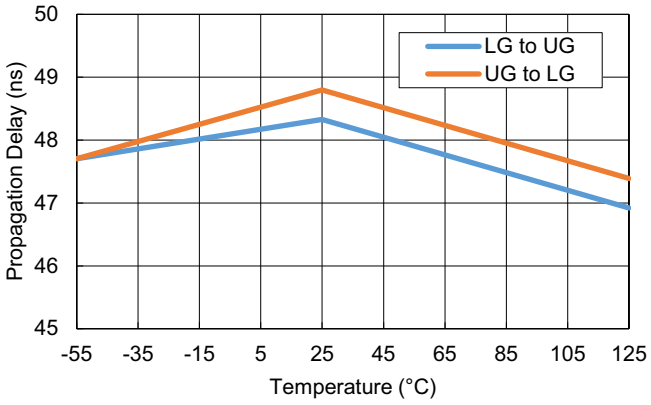


Figure 18. Dead Time Delay vs Temperature; RDU = RDL = 10kΩ

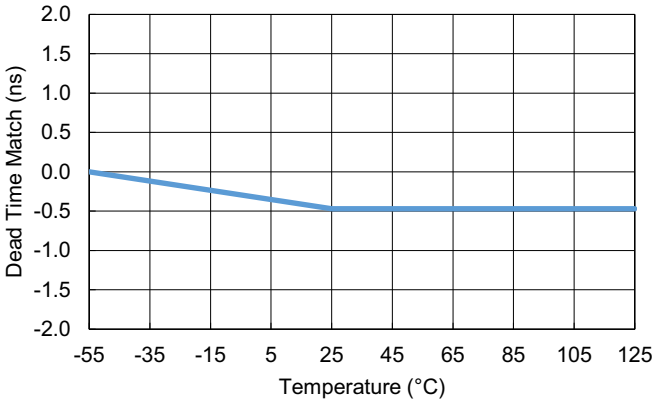


Figure 19. Dead Time Delay Matching vs Temperature; RDU = RDL = 10kΩ

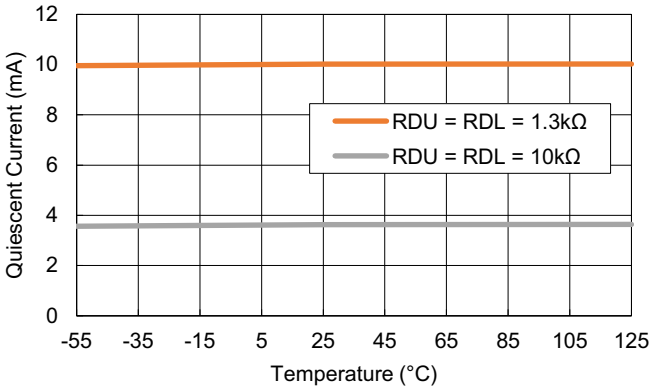


Figure 20. VDD Static Bias Current vs RDU/RDL vs Temperature; Enabled; PWM = Float

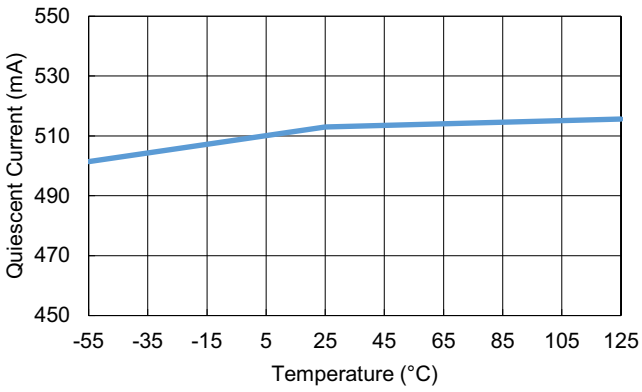


Figure 21. BOOT Static Bias Current vs Temperature; PWM = Float

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

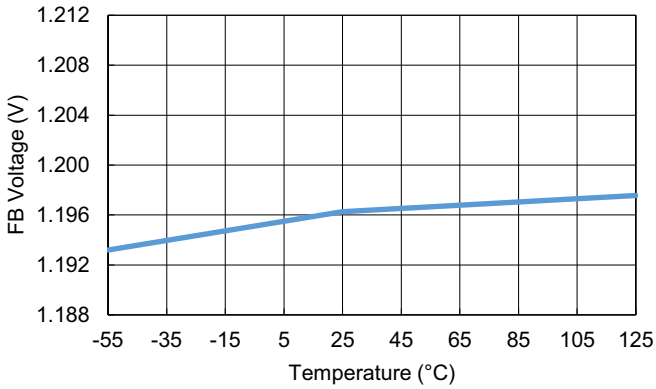


Figure 22. PVCC FB Voltage vs Temperature

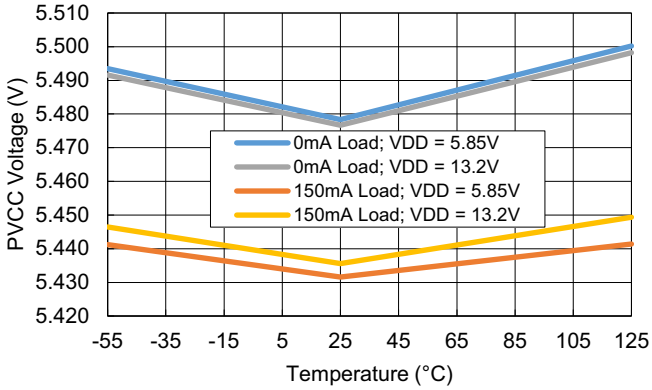


Figure 23. PVCC vs Temperature; PVCC = 5.5V

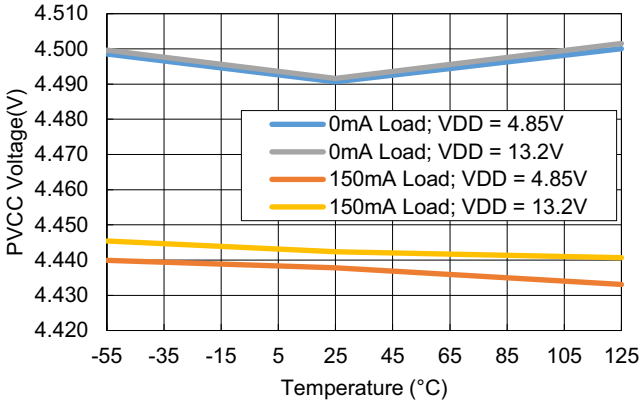


Figure 24. PVCC vs Temperature; PVCC = FB

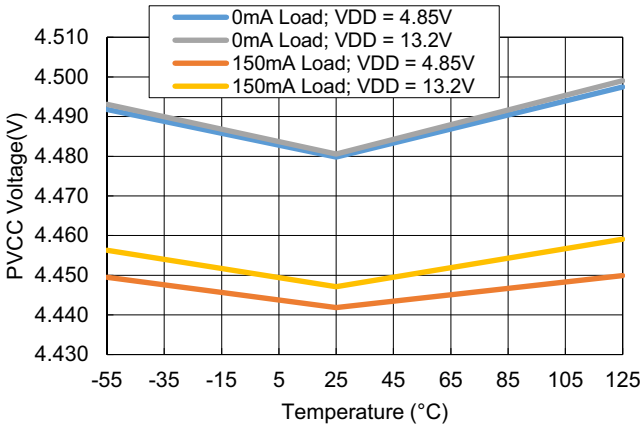


Figure 25. PVCC vs Temperature; PVCC = 4.5V

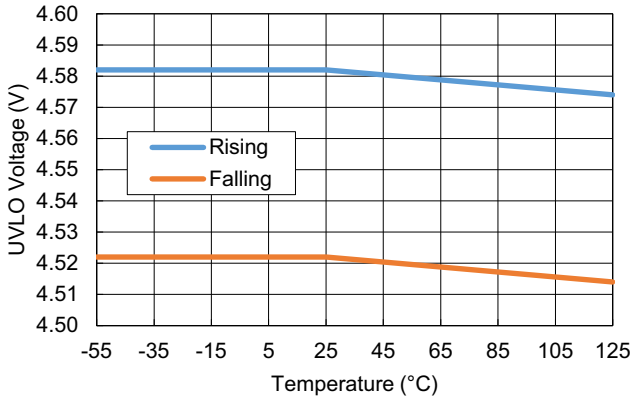


Figure 26. VDD UVLO vs Temperature

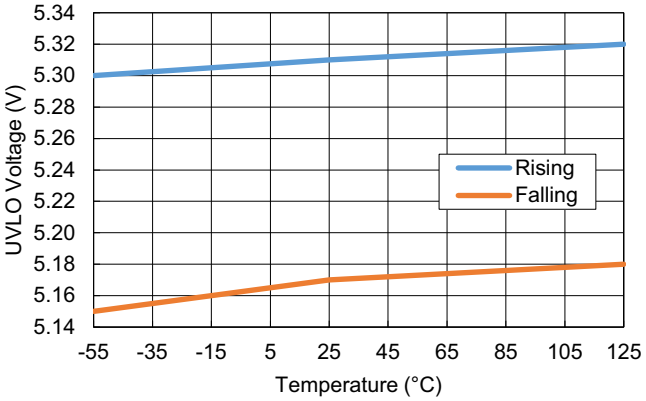


Figure 27. PVCC UVLO vs Temperature

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

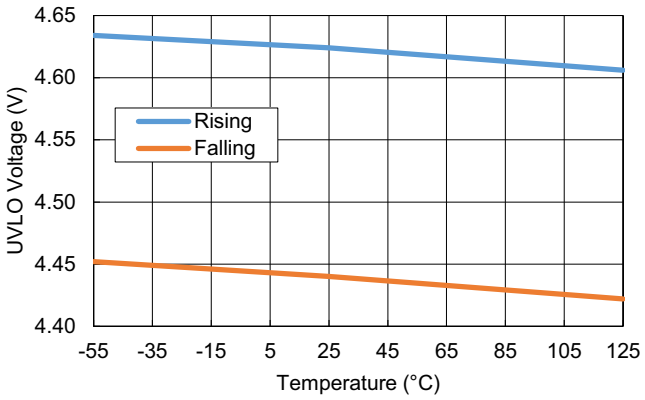


Figure 28. AVCC UVLO vs Temperature

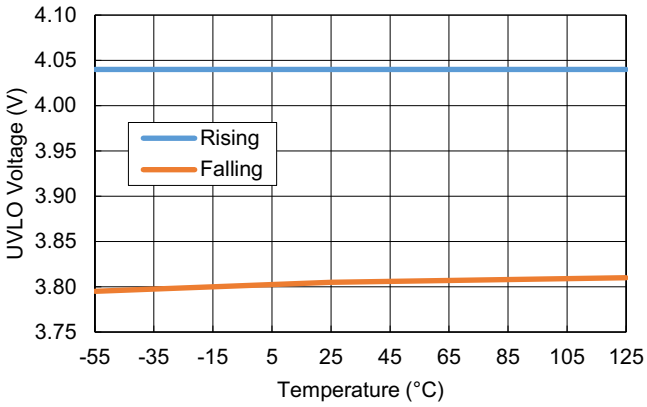


Figure 29. BOOT UVLO vs Temperature

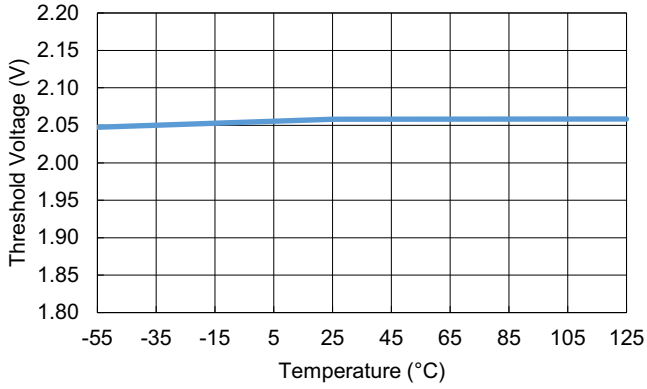


Figure 30. PWM Pin Float Voltage Vs Temperature

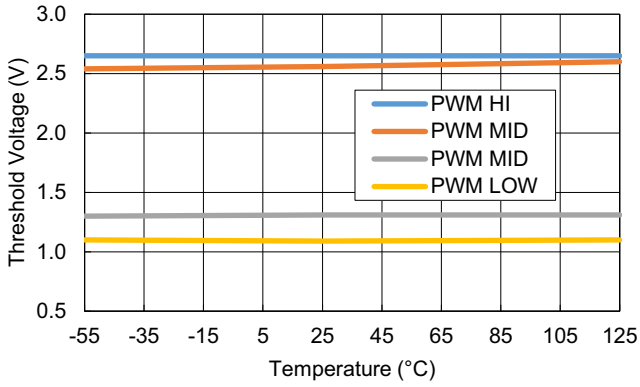


Figure 31. PWM Thresholds vs Temperature

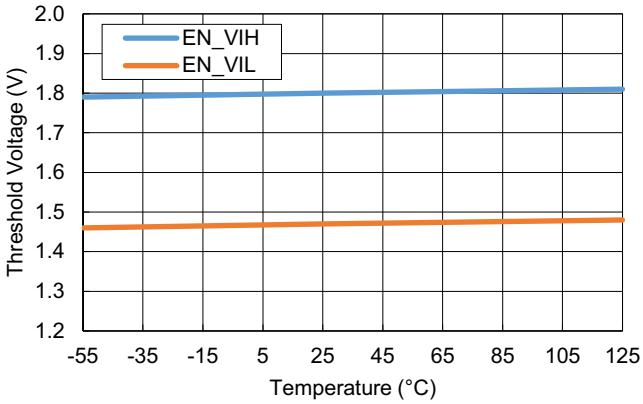


Figure 32. EN Threshold vs Temperature

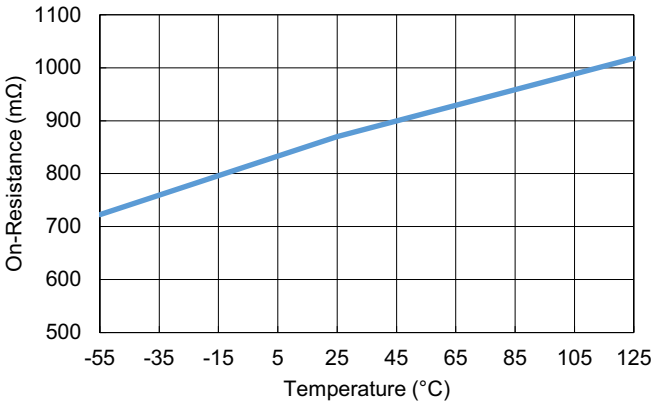


Figure 33. BOOT Switch $r_{DS(ON)}$ vs Temperature

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

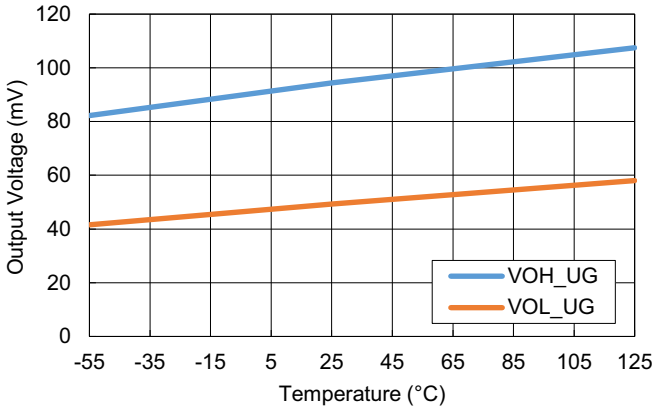


Figure 34. High-Side Driver V_{OL} and V_{OH} vs Temperature; 100mA Load

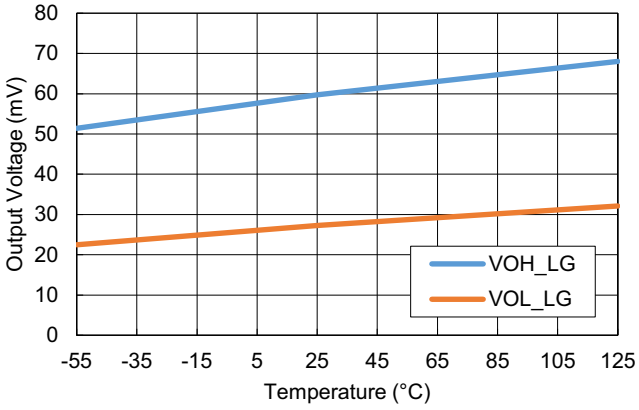


Figure 35. Low-Side Driver V_{OL} and V_{OH} vs Temperature; 100mA Load

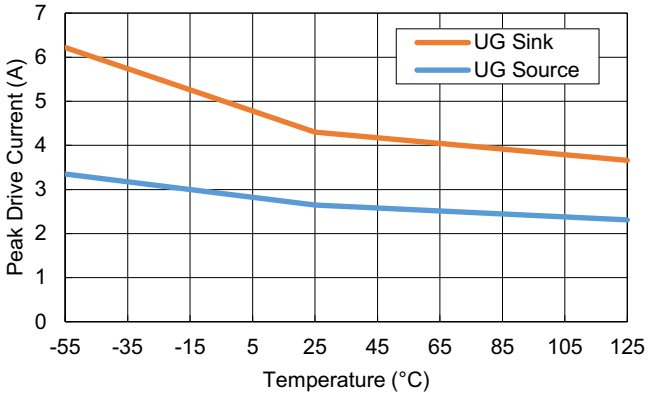


Figure 36. High-Side Driver Peak Source and Sink Current vs Temperature

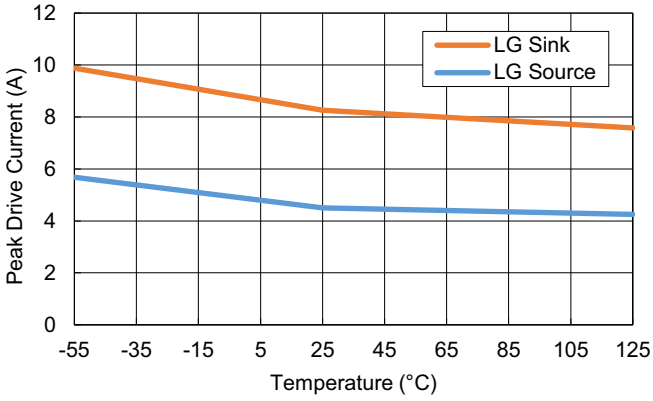


Figure 37. Low-Side Driver Peak Source and Sink Current vs Temperature

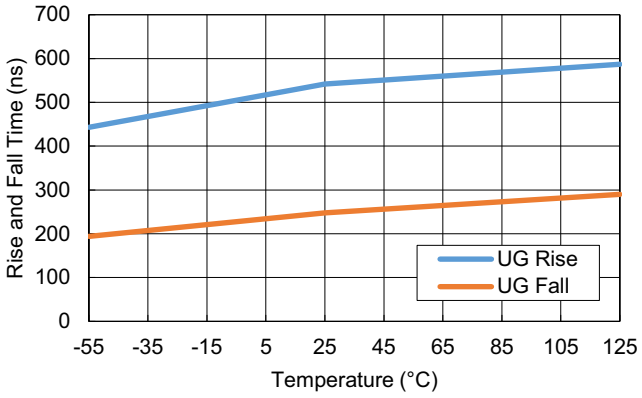


Figure 38. Rise and Fall Times with 470nF on UG and 1000nF on LG vs Temperature; 30% to 70%

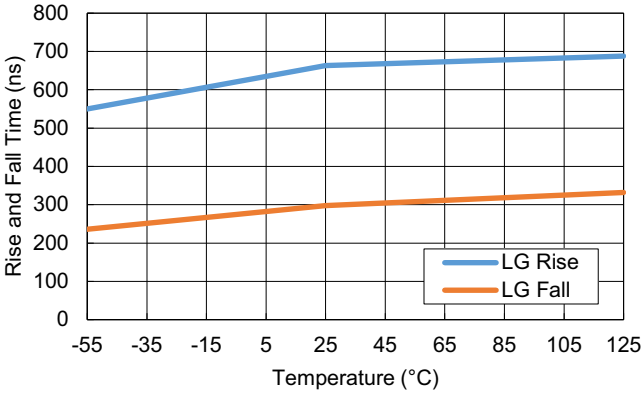


Figure 39. Rise and Fall Times with 470nF on UG and 1000nF on LG vs Temperature; 30% to 70%

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

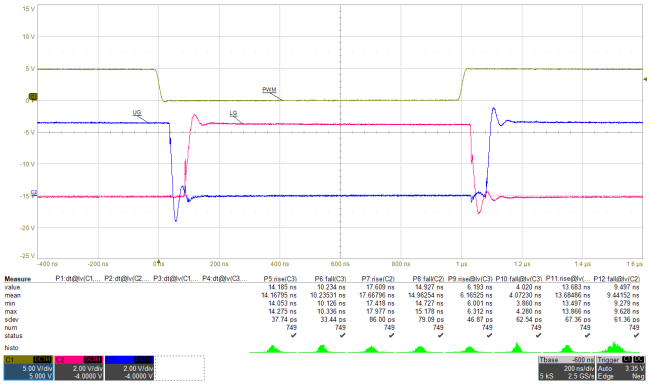


Figure 40. UG and LG Transient Response; 5.1nF on UG and 10nF on LG

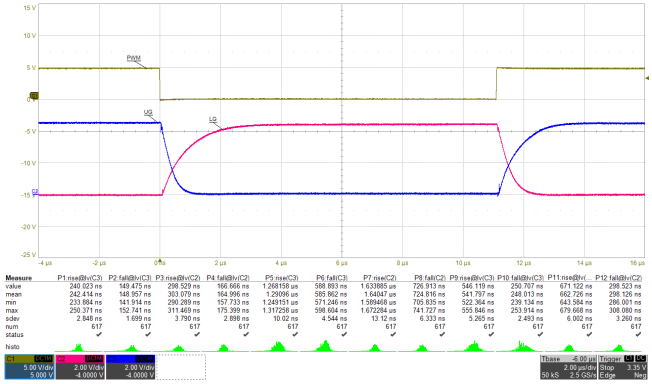


Figure 41. UG and LG Transient Response; 470nF on UG and 1000nF on LG

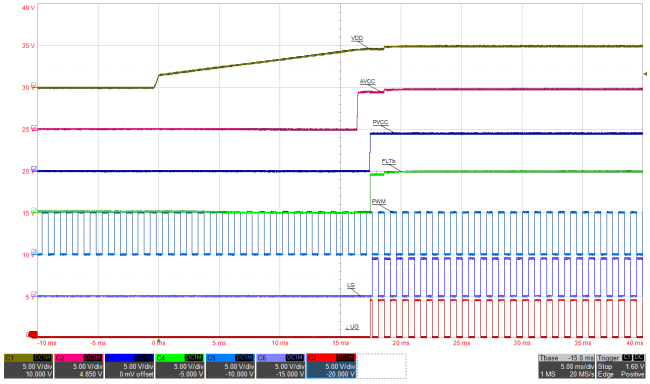


Figure 42. VDD Power-Up Sequence with EN = VDD

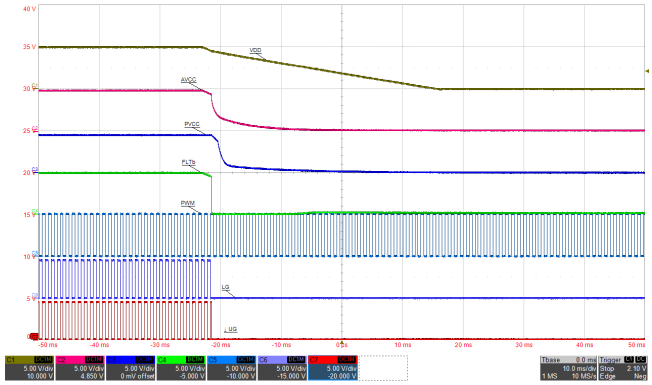


Figure 43. VDD Power-Down Sequence with EN = VDD

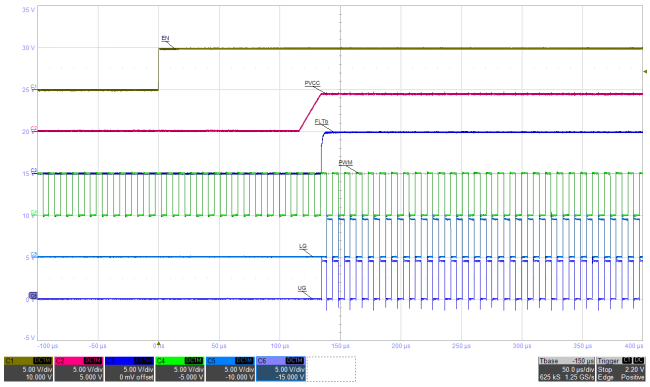


Figure 44. EN Rising Sequence

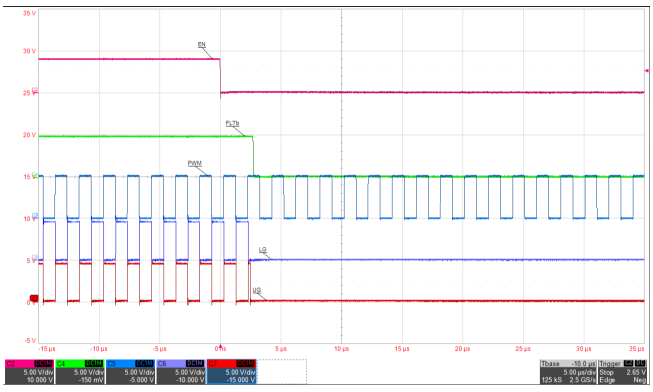


Figure 45. EN Falling Transient Response

Unless otherwise specified, typical performance curves are at VDD=12V, PHS=0V; PVCC=4.5V and T_A = +25°C.

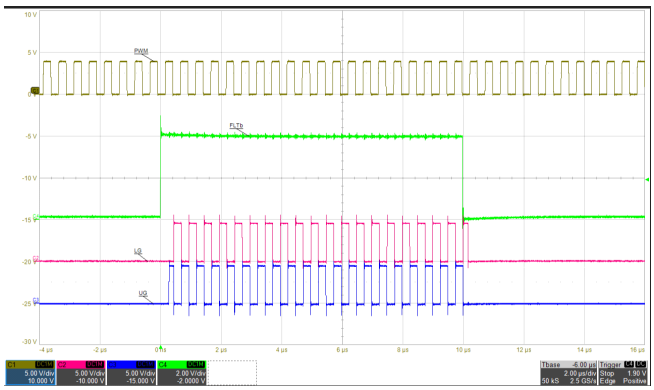


Figure 46. $\overline{FLT}$ Pin Response Time

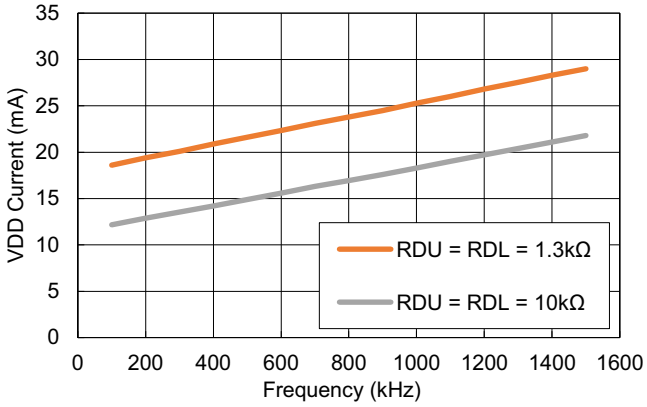


Figure 47. VDD Dynamic Operating Current vs f_{SW}; PVCC = BOOT = 4.5V; PHS = GND; No load on UG and LG

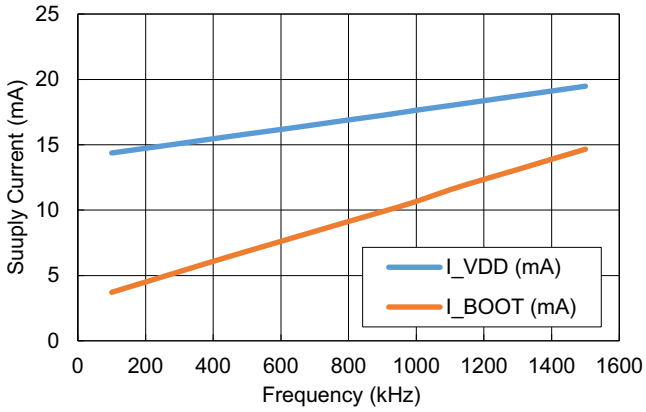


Figure 48. VDD and BOOT Dynamic Operating Current vs f_{SW}; VDD = PHS = 12V; PVCC = BOOT-PHS = 4.5V; No load on UG and LG; RDU = RDL= 1.3kΩ

5. Functional Description

5.1 Half-Bridge Driver

The ISL71441M is a high-frequency 12V Half-bridge driver for N-type GaN FETs or logic-level NMOS FETs. High peak drive current and fast propagation delay time with tight matching allows driving low $r_{DS(ON)}$ FETs in high-frequency DC/DC and motor control applications. With an integrated programmable gate drive voltage, high-side level shifter, and bootstrap switch, only a few external components are needed to drive N-type GaN or MOS FETs in a half-bridge configuration.

5.2 GaN/MOS FET Gate Drive Supply

A programmable gate drive supply from 4.5V to 5.5V allows users to optimize the gate voltage for different GaN FETs and logic-level MOSFETs. Renesas GaN FETs recommend a nominal 4.5V gate drive voltage. Other GaN FET vendors can tolerate up to 5.5V. The programmable function allows users to optimize gate drive voltage for low $r_{DS(ON)}$ and GaN FET reliability.

5.3 PWM Input

The PWM pin features a tri-level input for controlling the driver outputs.

- PWM = Low for low-side FET on
- PWM = High for the high-side FET on
- When PWM is at mid-level, both drivers are off.

A PWM input half-bridge driver inherently prevents one type of bridge shoot-through by not allowing the input logic to simultaneously command both the high-side and low-side drivers. The tri-level input allows the half-bridge to be in a high-impedance state during soft-start or hiccup of a PWM controller or for phase dropping in multi-phase regulators. The ISL71441M GaN FET Driver interfaces with the ISL73847M 2-phase PWM Controller.

5.4 Dead Time Control

Because a PWM input driver controls both drivers in a complimentary on/off state, dead time control is needed to prevent shoot-through at the half-bridge FET gates. The ISL71441M integrates independent high-side and low-side dead time control on the RDU and RDL pins for delaying the rising edge gate turn-on from the falling edge of gate turn-off. The rising edge dead time delay is programmable from 6.5ns to 50ns with a single resistor on RDU and RDL to ground.

5.5 Driver Output Architecture

The ISL71441M half-bridge driver incorporates a 2-stage output for high peak drive currents while minimizing quiescent current. The driver turn-on circuit includes a P-channel transistor and a transient N-channel transistor. When the driver output is low, the N-channel has maximum drive capability to assist in the rise time of the turn-on. As the output reaches near the high level, the N-channel no longer provides drive strength and is only held on by the P-channel. Conversely, the driver turn-off circuit includes an N-channel transistor and a transient P-channel transistor. When the driver output is high, the P-channel has maximum drive capability to assist in the fall time of the turn-off. As the output reaches near the low level, the P-channel no longer provides drive strength and is only held on by the N-channel.

5.6 Integrated BOOT Switch

The ISL71441M integrates a boot switch connected between PVCC and BOOT to charge the bootstrap capacitor. A low r_{ON} switch minimizes voltage drop compared to a bootstrap diode while quickly recharging the bootstrap capacitor, which is critical for maintaining the proper V_{gs} gate drive voltage for the high-side GaN FET. The BOOT switch only turns on when the low-side driver is on and the phase node voltage is between -250mV and +250mV. The ISL71441M internally detects the voltage on the PHS pin (connected to the phase node). The purpose of

monitoring the PHS pin voltage and requiring the low-side driver to turn on the boot switch is to prevent over-charging the bootstrap capacitor. See Application Information for more information about boot overcharge protection.

6. Application Information

6.1 Power Supply Biasing

ISL71441M is biased from the VDD pin and integrates two internal LDOs powered from VDD. The VDD pin bias range is from 4.75V to 18V. A VDD UVLO prevents operation below VDD = 4.75V. Place a 2.2µF or larger ceramic decoupling capacitor near the VDD and SGND pins for input power supply decoupling.

6.2 AVCC LDO

The AVCC LDO is for internal chip biasing. AVCC is internally regulated to 5V nominal. AVCC LDO is enabled when VDD is above the UVLO voltage. The AVCC LDO has an internal overcurrent limiting function. When AVCC LDO crosses the overcurrent limit, the AVCC LDO operates in constant current limit regulation. The current capability on AVCC is 20mA, which includes the current internally consumed by the AVCC pin. When AVCC is below the AVCC UVLO threshold, the $\overline{FLT}$ pin is pulled low to indicate a driver fault condition. Renesas does not recommend using the AVCC LDO for other external biasing; the total current consumption can trigger the constant current limit.

It is necessary to place a 1.0µF or larger decoupling capacitor near the AVCC and SGND pins for stability.

6.3 PVCC LDO

The PVCC LDO is for the low-side gate drive voltage and the high-side bootstrap circuit. PVCC voltage is externally programmable with a resistor divider to the FB pin. The programmable range is from 4.5V to 5.5V. Optionally, FB can be connected directly to PVCC to set PVCC to 4.5V nominal. The PVCC LDO is enabled by EN pin. The PVCC LDO has an internal overcurrent limiting function. When PVCC LDO crosses the overcurrent limit, the PVCC LDO operates in constant current limit regulation. When PVCC is below the UVLO threshold, the $\overline{FLT}$ pin is pulled low to indicate a driver fault condition. The current capability on PVCC is 150mA, which includes the current internally consumed by the PVCC pin. Renesas does not recommend using the PVCC LDO for other external biasing; the total current consumption can trigger the constant current limit.

It is necessary to place a 1.0µF or larger decoupling capacitor near the PVCC and PGND pins for stability. Renesas recommends using a capacitance on PVCC 10x larger than the bootstrap capacitor across BOOT-PHS pins.

6.4 Setting PVCC (Gate Drive) Voltage

The voltage on the PVCC LDO to set the gate drive voltage is determined by two resistors connected between PVCC, FB, and SGND. Equation 1 sets the voltage where R_F is connected from PVCC to FB and R_G is connected between FB and SGND.

(EQ. 1) $$PVCC = \left(\frac{R_F}{R_G} + 1\right) \times 1.2V$$

Optionally, short FB to PVCC to set PVCC = 4.5V.

6.5 PVCC and BOOT Undervoltage Lockout (UVLO)

The ISL71441M integrates a PVCC UVLO and a BOOT UVLO to prevent undervoltage gate drive to the half-bridge GaN FETs. The PVCC UVLO rising and falling thresholds are relative to the set voltage of PVCC, while the BOOT UVLO is at a fixed threshold.

Under a PVCC UVLO condition, the high-side and low-side driver outputs do not respond to PWM input commands. Under a BOOT UVLO condition, only the high-side driver does not respond to PWM input commands.

6.6 Enable Control

The EN pin controls the start-up of the driver. When EN = 0, the PVCC LDO is disabled. With no PVCC voltage, the $\overline{FLT}$ pin pulls low to indicate a driver's not-ready condition, and the driver outputs are in a high-impedance state. When EN = 1, the PVCC LDO is enabled, and if no other fault conditions exist, it releases the $\overline{FLT}$ pin and enables the driver outputs. The delay time between EN logic high and the PVCC LDO start-up is typically 115µs.

The EN pin is VDD voltage compatible and can be tied to VDD for always-enabled applications.

6.7 PWM Operation

Because of the tri-level input thresholds, the PWM pin is designed only for 0V to 5V logic level operation with a high-impedance float or external drive to establish the mid-level. In the high-impedance float state, internal pull-up and pull-down resistors bias the PWM pin at 2V. When PWM is logic high, the high-side driver is on, and the low-side driver is off. When PWM is logic low, the low-side driver is on, and the high-side driver is off. When PWM is at mid-level, both drivers are off.

The PWM operating frequency range is limited on the low end by the boot capacitance on the BOOT to PHS pin to keep the boot circuit biased. As long as sufficient boot bias exists, there is no lower limit on the PWM frequency. The upper PWM frequency is limited by acceptable signal propagation and dead time delays. The typical minimum PWM pulse width for logic high and low to change the driver output state is 20ns.

6.8 Dead Time Control Resistor Setting

The RDU and RDL pins set the rising edge dead time delay for the low-side and high-side drivers. The RDU pin controls UGH rising edge delay respective to the LGL falling edge. The RDL pin controls LGH rising edge delay respective to the UGL falling edge. A resistor to ground on RDU and RDL is required to set the dead time delay. A 1.2V reference voltage on RDU and RDL forces a current through the external resistors. This current is used to program the dead time delay. The dead time delay programmable range is from 6.5ns to 50ns using a 1.3kΩ to 10kΩ resistor. From the Typical Performance Curves Figure 14 and Figure 15, dead times beyond 50ns can be achieved, but the accuracy and dead-time matching performance is not guaranteed per the Electrical Specifications.

Use Equation 2 to calculate the resistor value for a required dead time:

(EQ. 2) $$\text{RDU or RDL}(k\Omega) = [\text{Dead Time}(ns)]/5.0$$

Although not recommended due to no Electrical Performance testing with using resistance larger than 10kΩ, if using dead time larger than 50ns, use Equation 3 to determine resistor value.

(EQ. 3) $$\text{RDU or RDL}(k\Omega) = [\text{Dead Time}(ns) + 6.5]/5.4$$

6.9 Bootstrap Capacitor Design

The high-side bootstrap capacitor provides the bias to the floating high-side circuitry to drive the high-side FET. The bootstrap capacitor recharges to PVCC voltage when the boot switch turns on. Choose the bootstrap capacitor to satisfy two conditions.

- It should be large enough to provide for the high-side driver bias current, the high-side driver DC output current (primarily the 1kΩ resistor on UGL to PHS), the high-side FET gate leakage current, and the instantaneous current to turn on the high-side FET (provide the gate charge) during the high-side on switching period, without discharging the boot voltage significantly.
- It should be small enough such that at initial start-up, the boot-refresh time meets system requirements. The resistance of the boot switch and the bootstrap capacitance determines the initial boot refresh to charge the boot capacitor from 0V to PVCC.

A good starting point is to design for a 5% discharge of the boot voltage during steady-state operation of the high-side drive. To determine the bootstrap capacitor, use Equation 4, where Q_{TOT} is the total charge required to operate the high-side driver during high-side on-time.

(EQ. 4) $$C_{BOOT} = \frac{Q_{TOT}}{V_{DROP}}$$

Q_{TOT} includes the following:

- Gate charge for the high-side FET turn-on.
- The charge for the high-side driver boot bias current.
- The charge for the high-side gate-source resistor when the driver is sourcing BOOT voltage.
- The charge for the high-side FET gate leakage current.

V_{DROP} is the amount of voltage drop across the boot capacitor. For PVCC = 4.5V: V_{DROP} = 4.5V × 0.05 = 225mV.

The following is a design example of a 12V to 1V DC/DC converter at 500kHz using ISL70023SEH 100V GaN FET as the high-side FET:

- Q_{GS1} = 25nC gate charge
- I_{BOOT} = 600µA; t_{ON} = 1V/12V × 2µs = 167ns; $Q_{BOOT} = I_{BOOT} \times t_{ON}$ = 0.1nC
- For 4.5V gate drive, Q_{GS2} = 4.5V/1kΩ × 167ns = 0.75nC
- ISL70023SEH specifies 9mA gate leakage. Q_{LEAK} = 9mA × 167ns = 1.5nC
- $C_{BOOT} = Q_{TOT}/V_{DROP}$ = 27.4nC / 225mV = 122nF (Use 100nF or 150nF standard value)

This capacitor is the minimum recommended bootstrap capacitor value to meet ripple voltage. Also, it is important to size the capacitor appropriately. During system start-up, the bootstrap capacitor is at 0V. The PWM controller must issue a boot refresh for the high-side driver to clear BOOT UVLO and have sufficient boot bias. Otherwise, the first few high-side commands do not turn on the upper FET, potentially causing system faults. The bootstrap capacitor is charged through PVCC and the internal 1Ω typical boot switch, forming an RC circuit. The boot refresh command from the PWM controller must drive PWM = 0V, and PHS must be within 250mV of PGND to turn on the boot switch and charge the capacitor. The boot refresh command needs to be of long enough duration for the RC circuit to charge above the BOOT UVLO threshold and maintain boot voltage in operation (for example, t = 3×RC would charge the capacitor to 95% of the final voltage). With a 1Ω boot switch impedance and 150nF bootstrap capacitor, this would require a boot refresh time of 450ns.

The ISL73847M PWM controller includes a built-in boot refresh command before a soft start-up during initial power-up and recovery from a hiccup. The controller issues 32 pulses of PWM switching between 0V (logic low) and 2V (mid-level). The oscillator of the ISL73847M controller sets the boot refresh pulse frequency and has a typical 100ns refresh time (PWM = 0V) to charge the boot capacitor.

6.10 Bootstrap Voltage Overcharge Protection

Traditional MOSFET applications drive the gate-source voltage anywhere from 10V-15V while retaining both 1) Low drain-source ON-resistance and 2) reliable operation. GaN FET operation has a much narrower range, usually around 4.5V to 6V, to maintain low ON-resistance and reliable operation.

The ISL71441M provides an integrated PVCC LDO to provide bias to the low-side gate driver. The ISL71441M also features unique circuitry to prevent overcharging the boot voltage in the bootstrap configuration.

Unlike a MOSFET, there is no body-drain diode in a GaN FET. However, there is still a reverse conduction path from source to drain with zero gate bias. The source-drain voltage is a function of the reverse current and is provided in the GaN FET datasheet as the VSD parameter. During dead time, when both high and low-side GaN FETs are off, the positive current flowing through the inductor is commutated through the low-side FET source-drain channel. The reverse VSD voltage pulls the PHS node of the ISL71441M driver below ground. In traditional half-bridge drivers with a boot diode implementation, the boot diode is forward-biased, and the

bootstrap capacitor is charged to PVCC + VSD. Depending on the magnitude, this can over-charge the bootstrap capacitor voltage, which provides the upper gate drive voltage.

Important: Operating the GaN FET with higher than recommended gate voltages is unreliable as this can damage the GaN FET. The recommended operating gate voltage for Renesas GaN FETs is 4.5V.

The ISL71441M implements bootstrap capacitor overcharge protection by replacing an external boot diode with an internal intelligent boot switch. The boot switch turns on only when PWM = 0V and the PHS voltage is within ±250mV of PGND. This features avoids recharging the bootstrap capacitor during dead time, where the PHS voltage can be excessively negative such that it overcharges the bootstrap capacitor. Figure 50 and Figure 51 highlight the bootstrap overcharge protection by replacing the boot diode with a boot switch.

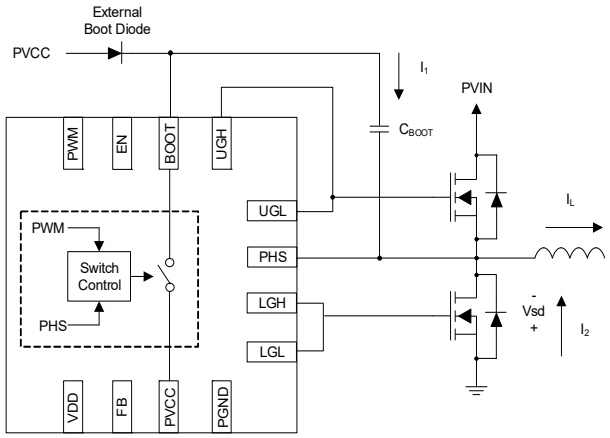


Figure 49. Bootstrap Overcharge Protection Diagram

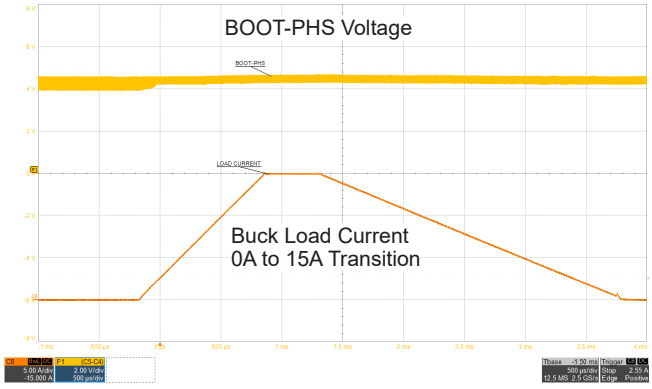


Figure 50. BOOT Switch Only

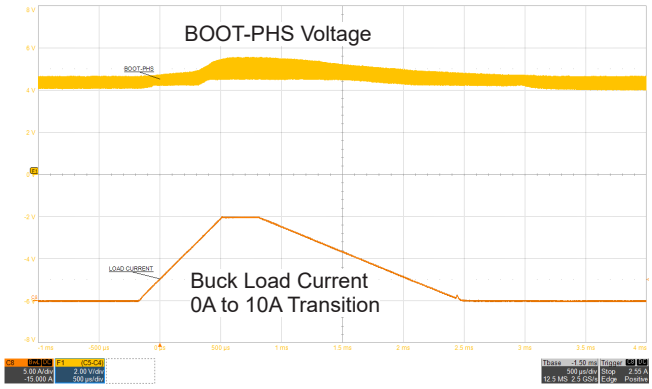


Figure 51. Schottky BOOT Diode Added

6.11 Gate Driver Outputs

The ISL71441M features independent source and sink driver outputs for the rise and fall time control. The upper gate driver is the Upper Gate High (UGH) and Upper Gate Low (UGL) pins. The lower gate driver is the Lower Gate High (LGH) and Lower Gate Low (LGL) pin. A series diode is needed on drivers without separate source and sink pins to achieve independent turn-on/off control. This issue can be problematic for GaN FETs as the diode's voltage drop from driver output to the FET gate impacts the FET ON-resistance. If no turn-on or turn-off time reduction is needed, Renesas recommends inserting a 0Ω resistor anyway. In practical layout, the Printed Circuit Board (PCB) trace length connecting the driver output to the FET gate has a parasitic inductance. Combined with the parasitic capacitance of the FET gate, this forms a resonant loop that can cause excessive ringing in the gate drive waveforms during turn-on and turn-off. The ringing overshoot may be large enough to damage a GaN FET gate in a poor layout. A small amount of resistance may be required to dampen the overshoot.

The UGx and LGx output high peak drive currents that turn on and off the FET quickly for high-frequency applications need to minimize switching losses. The high-side driver provides up to 2A source and 4A sink peak drive current. The low-side source and sink driver provides up to 4A source and 8A sink peak drive current.

There is a 1kΩ passive pull-down resistor on UGL to PHS and a 500Ω passive pull-down resistor on LGL to PGND. These passive pull-down resistors prevent charge build-up on the FET gate-source capacitance when the ISL71441M driver is unbiased. Otherwise, both half-bridge FETs can accumulate enough Vgs from leakage current or stray noise at the capacitive high impedance gate to turn on and cause shoot-through.

In normal operation, driver outputs respond to PWM input commands. Under disabled or fault conditions, the driver outputs do not respond to PWM input, and the driver outputs are in either an active off (the UGL and LGL sink drivers are on) or passive off (1kΩ pull down on UGL to PHS and 500Ω pull down on LGL to PGND) condition. Below is a list of ISL71441M states where the driver outputs do not respond to PWM input commands and their associated active or passive states.

Note: A passive off condition supersedes the active off condition.

- EN pin low (driver disabled): Passive Off
- VDD, AVCC, or PVCC UVLO: Passive Off
- PWM = Mid-level: Active Off
- $\overline{FLT}$ externally driven low: Active Off
- Over-Temperature Fault: Active Off
- BOOT UVLO: Passive off only at the high-side driver. The low-side driver is still active for PWM input commands.

6.12 $\overline{FLT}$ Pin Fault Indication

The ISL71441M includes several fault protections to prevent the operation of the half-bridge driver in a faulted condition. The $\overline{FLT}$ pin is an indicator of its fault status. The $\overline{FLT}$ pin is a dual-use open-drain output with external input control. Connect a pull-up resistor from the $\overline{FLT}$ pin to AVCC. The typical value is 10kΩ. $\overline{FLT}$ internally pulls low to indicate a fault condition when one of the following occurs:

- EN = 0 (driver disabled),
- VDD, AVCC or PVCC in UVLO, or
- ISL71441M is in an over-temperature fault condition.
- Under these fault conditions, the driver outputs do not respond to PWM inputs.

You can also use the ISL71441M $\overline{FLT}$ pin for external control input in fault broadcasting applications where all driver $\overline{FLT}$ pins are connected. If one driver or a controller enters a fault condition that pulls its $\overline{FLT}$ pin low, all other ISL71441M drivers are disabled to prevent operation when the system detects a fault condition.

Renesas recommends using a 10pF or larger capacitor on the $\overline{FLT}$ pin to SGND for SEE mitigation. This capacitor prevents false toggling of the $\overline{FLT}$ pin due to SEE transients.

6.13 $\overline{FLT}$ pin Usage with ISL73847M and other ISL71441M drivers

The ISL71441M $\overline{FLT}$ pin works with the ISL73847M PWM controller as a system-ready status to initiate soft-start (not at fault) or shutdown (fault encountered) in operation. The ISL73847M is a 2-phase controller, so both the $\overline{FLT}$ pin on the ISL71441M and the $\overline{FLT}$ pin on the ISL73847M are tied with a single pull-up resistor to either the AVCC on ISL71441M or VCC on ISL73847M.

6.14 $\overline{FLT}$ as Pseudo Enable Pin

The EN pin enables the bandgap before powering up the PVCC LDO and finally enabling the driver outputs. The propagation delay time from the EN rising edge to the driver output's enable is 95µs typical. Alternatively, for faster enable time in applications not using the ISL73847M PWM controller, an open-drain NMOS FET can be connected to the $\overline{FLT}$ pin to operate as a faster enable/disable pin. When the gate voltage is logic high, the $\overline{FLT}$ pin is low, and the driver is disabled. When the gate voltage is logic low, the pull-up resistor on the $\overline{FLT}$ pin pulls

the $\overline{FLT}$ high. The $\overline{FLT}$ high or low to the driver output's response propagation delay is 100ns typical. When using the $\overline{FLT}$ pin as the driver enable pin, connect EN to VDD.

6.15 Over-Temperature Protection

The ISL71441M integrates an Over-Temperature Protection (OTP) circuit. When the junction temperature reaches 160°C typical, the OTP threshold is triggered. In an over-temperature fault condition, the driver stops responding to PWM inputs while the UGL and LGL sink outputs are active to disable the half-bridge. The $\overline{FLT}$ pin pulls low to indicate a fault. The PVCC LDO remains enabled during an over-temperature fault condition. When the junction temperature falls below 145°C typical, the OTP condition clears. The driver automatically resumes normal operation, and the $\overline{FLT}$ pin is released.

6.16 VDD Supply Current

The VDD supply current of ISL71441M divides between static bias current and dynamic operating current. The static bias current includes the current needed to bias the dead time delay circuit. The dynamic operating current consists of the operating frequency on PWM, the duty cycle, and the capacitive load of the GaN FET.

Use Equation 5 to approximate the static bias current, where VREF = 1.2V; RDU and RDL are the resistors (in kΩ) used for the dead-time delay.

(EQ. 5) $$I\_VDD\ (static) = 4.5mA + 3 \times \left(\frac{VREF}{RDU}\right) + 3 \times \left(\frac{VREF}{RDL}\right)$$

Use Equation 6 to approximate the dynamic operating current:

(EQ. 6) $$I\_VDD\ (dynamic) = I\_VDD(f_{SW}) + I\_VDD\ (capacitor\ load) + I\_VDD\ (duty\ cycle)$$

Figure 47 shows the dynamic I_VDD current versus f_{SW}.

The dynamic current from the capacitor load is I = C × V × F, where C is the equivalent capacitive load of the GaN FET gate-source capacitance, V is the operating PVCC voltage, and F is the switching frequency (f_{SW}). Determine C by Q_{GS}/V, where Q_{GS} is the total gate charge specified in the GaN FET datasheet. Remember to sum up the low and high sides of GaN FET Q_{GS}.

The dynamic current from the duty cycle is because of the 500Ω pull-down resistor on LGL and 1kΩ resistor on UGL. During one switching cycle, the current through these resistors is Equation 7, where R1 is 1kΩ, R2 is 500Ω, and D is the duty cycle of the gate drive waveform.

(EQ. 7) $$I\_VDD\ (duty\ cycle) = \frac{PVCC}{R_1} \times D + \frac{PVCC}{R_2} \times (1 - D)$$

6.17 Power Dissipation

The power dissipation calculation for the ISL71441M half-bridge driver is not as straightforward compared to typical half-bridge drivers where most of the power is dissipated by the dynamic operating current of the driver and in the output driver stage switching the capacitive load of the FET gates. While the dynamic current and output drive dissipation are still major portions, the ISL71441M total power dissipation must also include the two internal LDOs, the current to bias the RDU and RDL dead time circuits, and the internal 1kΩ pull-down resistor on the upper gate driver and the 500Ω pull-down resistor on the lower gate driver as these attributes further increase the power dissipation. Therefore, VDD biasing voltage, PVCC LDO regulated voltage, programmed dead time, and even duty cycle operation become factors in the total power dissipation. Use the spreadsheet calculator tool on the product page to estimate the total power dissipation in the ISL71441M driver.

6.18 Dual Complimentary Low-Side GaN FET Driver

The ISL71441M can be configured as a dual complementary output low-side driver controlled by the PWM input. Such an application can be used in synchronous low-side drives of transformer-isolated topologies. Connect the

PHS pin common to PGND to ground the upper driver. Connect the BOOT pin to the PVCC pin to bypass the boot switch. The upper driver UG is in phase with the PWM input, while the lower driver LG is logically inverted from PWM. The dead time from UG falling to LG rising and LG falling to UG rising is still enforced by the dead time resistors on RDU and RDL in this configuration. Either GaN FET may be omitted in this configuration to use the ISL71441M as a single inverting (LG only) or non-inverting (UG only) GaN FET Driver.

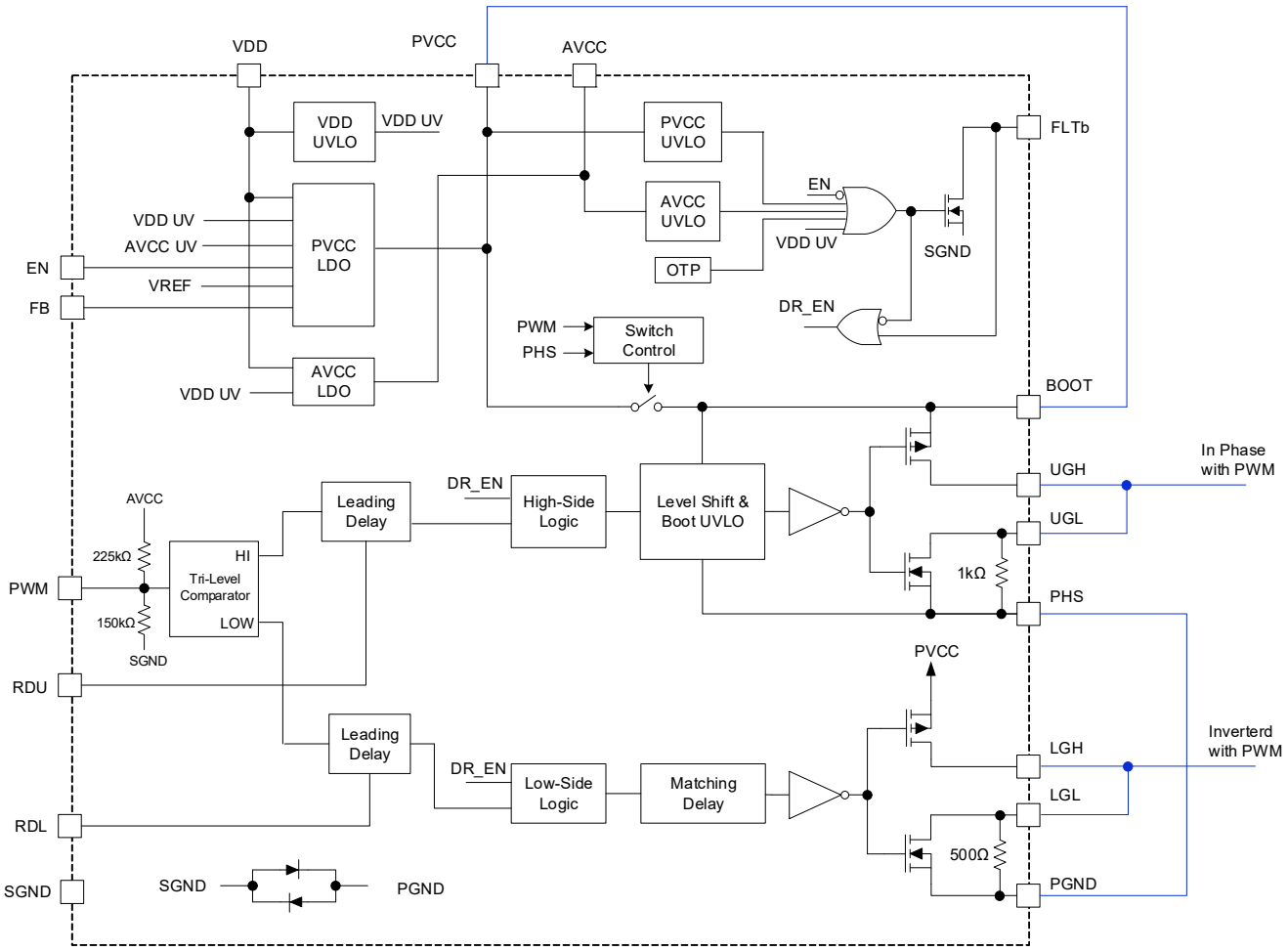


Figure 52. Connection for Dual Low-Side Driver

7. PCB Layout

7.1 Layout Guidelines

It is crucial to consider and follow the general printed circuit board layout guidelines to maximize the performance of the ISL71441M half-bridge driver and the power GaN FETs it is driving.

- Place low ESR X7R grade or better ceramic capacitors for high-frequency decoupling as close to the package pins as possible. These include the capacitors between VDD-SGND, AVCC-SGND, PVCC-PGND, and BOOT-PHS.
- Place the RDU and RDL dead-time control resistors close to their respective pins and connect them to SGND through the PCB GND plane.
- Connect the SGND pin and the bottom EPAD of the package to the top layer GND plane of the PCB. To further improve thermal performance, place at least nine vias in the GND plane under the package EPAD to another internal GND plane to dissipate heat.

- Place the ISL71441M close to the half-bridge power GaN FET to minimize trace inductance and high current loop area between the driver output and the GaN FET gate.
- The PGND pin and the low-side FET source should be connected commonly through the same PCB GND plane as SGND and the EPAD. Alternatively, the PGND pin can be connected to the low-side FET Source-Sense terminal if it is available. The components should be arranged and the trace routed to keep this PGND inductance low.
- Route the PHS pin to the switch node of the half-bridge power stage with a short and wide trace to minimize inductance and loop area.
- For the low-side drive, the PVCC capacitor, PVCC and PGND pins, low-side driver gate outputs, low-side FET gate, and GND plane form a current loop during FET turn-on and turn-off. For the high-side drive, the bootstrap capacitor, the BOOT and PHS pins, the high-side driver gate outputs, the high-side FET gate, and the switch node form a current loop during FET turn-on and turn-off. Keep these loops short and wide, and avoid overlapping with other sensitive signals.
- Size the phase node of the half-bridge (high-side FET source and low-side FET drain) area to handle the current and thermal dissipation from the FETs and switching load. The phase node copper area usually ends up being a significantly large shape. In addition, the phase node is where high voltage and high dv/dt switching occurs. In general, there are two layout practices for handling the phase node. One recommendation is to remove any conductors (including ground) that overlap the phase node on the adjacent layer of the PCB. The other recommendation is to repeat the phase node shape on every layer of the PCB. Both methods minimize the capacitive coupling of noise into the GND plane and prevent any sensitive analog signals from being routed underneath the phase node and causing unintentional common mode noise.

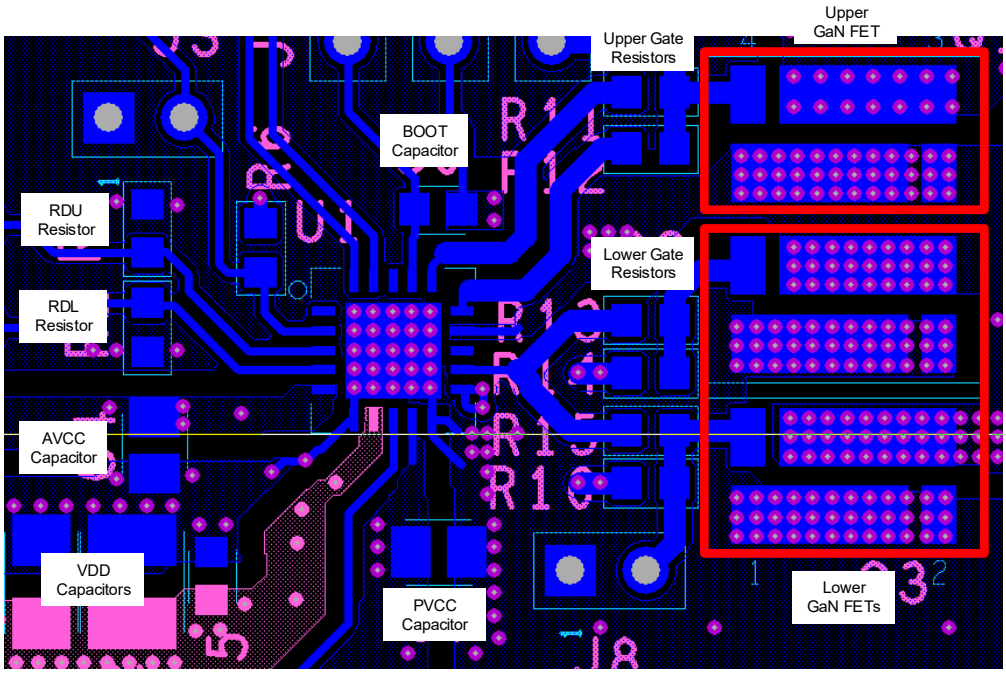


Figure 53. Layout Example

8. Radiation Tolerance

The ISL71441M is a radiation tolerant device for commercial space applications, Low Earth Orbits (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. This device's response to Total Ionizing Dose (TID) radiation effects and Single Event Effects (SEE) has been measured, characterized, and reported in the following sections. The TID performance of the ISL71441MRZ is not guaranteed through radiation lot acceptance testing. The ISL71441M30RZ is radiation lot acceptance tested (RLAT) to 30krad(Si) and ISL71441M50RZ is RLAT to 50krad(Si). The characterized SEE performance is not guaranteed.

8.1 Total Ionizing Dose (TID) Testing

8.1.1 Introduction

Total dose testing of the ISL71441M proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 10 samples irradiated under bias and eight samples irradiated with all pins grounded (unbiased). Two control units were used. Figure 54 shows the bias configuration. The wafers were drawn from wafer lot F6W015.1. All samples were packaged in the 20-pin QFN plastic package.

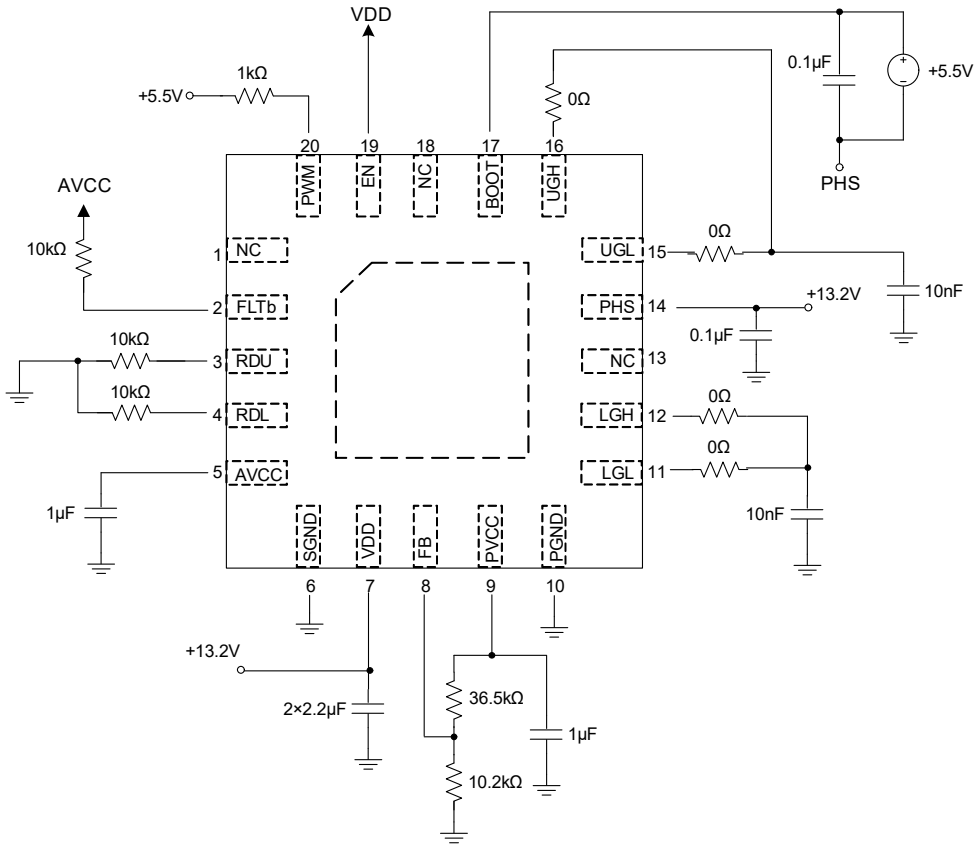


Figure 54. TID Testing Bias Configuration

Samples were irradiated at a low dose rate (LDR) of 0.01rad(Si)/s using a Hopewell Designs N40 vault-type LDR irradiator in the Palm Bay, Florida, Renesas facility. A PbAl box was used to shield the test fixture and devices under test against low energy, secondary gamma radiation. All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature. The planned irradiation downpoints were 0krad(Si), 10krad(Si), 30krad(Si), and 50krad(Si).

8.1.2 Results

Table 1 summarizes the attributes data. Bin 1 indicates a device that passes all the datasheet specification limits.

Table 1. Total Dose Test Attributes Data

Dose Rate (mrad(Si)/s)	Bias	Sample Size	Downpoint	Bin 1	Rejects
10	Figure 54	10	Pre-Rad	10	0
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
10	Grounded	8	Pre-Rad	8	0
			10krad(Si)	8	0
			30krad(Si)	8	0
			50krad(Si)	8	0

The plots in Figure 55 through Figure 64 show data for key parameters at all downpoints. The plots show the sample size average as a function of the total dose for each irradiation condition. The average was used because the large sample size obfuscates the data from being easily read. All parts showed excellent stability over irradiation.

8.1.2.1 Typical Radiation Performance

Bias configuration radiation test condition: VDD = EN = 13.2V; PHS = 13.2V; PWM = 5.5V; PVCC = BOOT-PHS = 5.5V

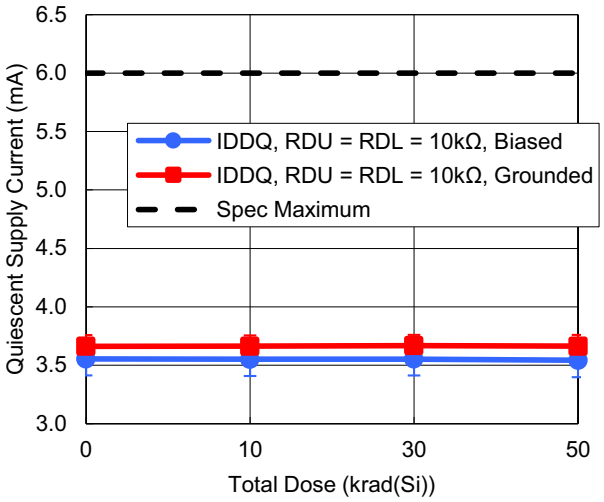


Figure 55. VDD Quiescent Supply Current

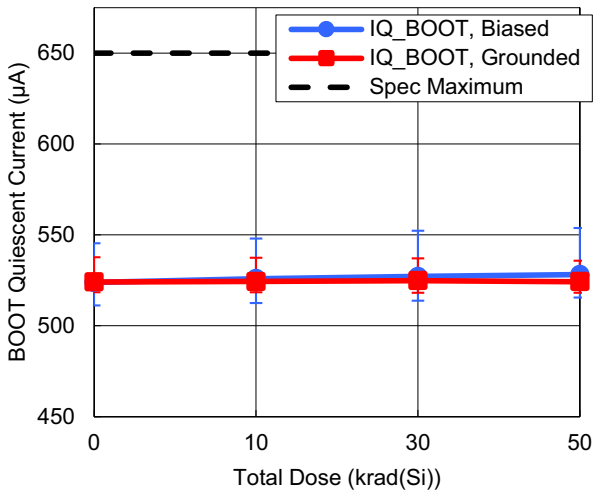


Figure 56. BOOT Quiescent Current

Bias configuration radiation test condition: VDD = EN = 13.2V; PHS = 13.2V; PWM = 5.5V; PVCC = BOOT-PHS = 5.5V (Cont.)

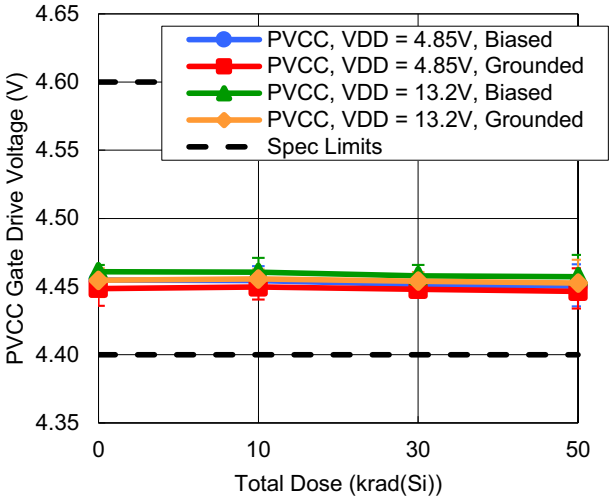


Figure 57. PVCC Gate Drive Voltage

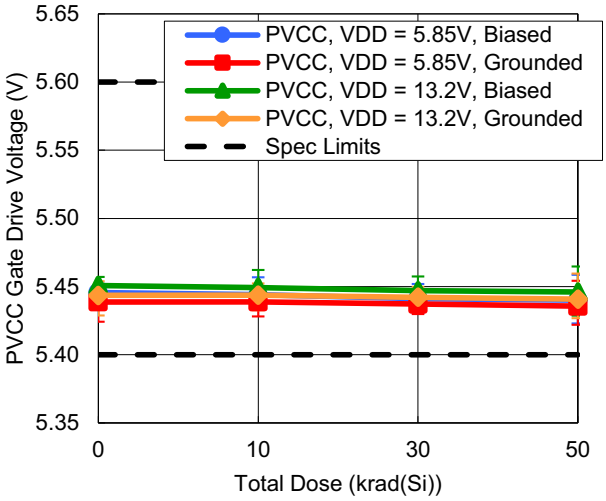


Figure 58. PVCC Gate Drive Voltage, VDD = 5.85V

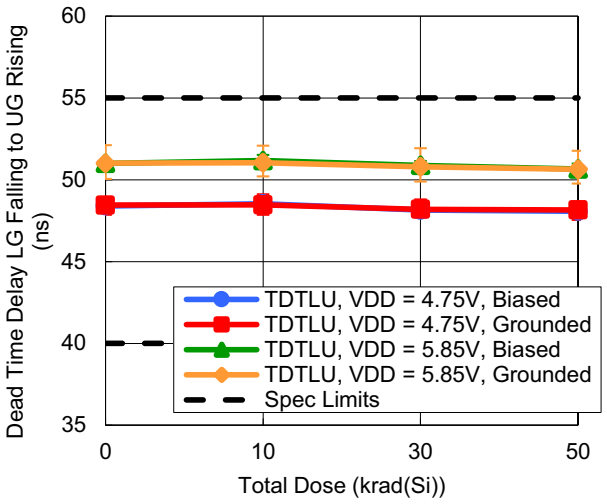


Figure 59. Dead Time Delay LG Falling to UG Rising

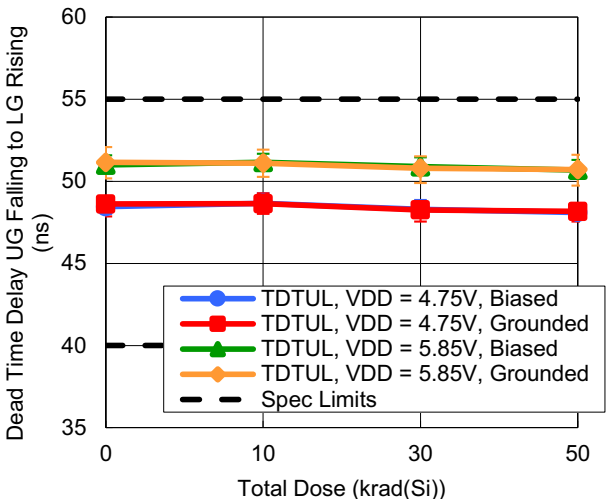


Figure 60. Dead Time Delay UG Falling to LG Rising

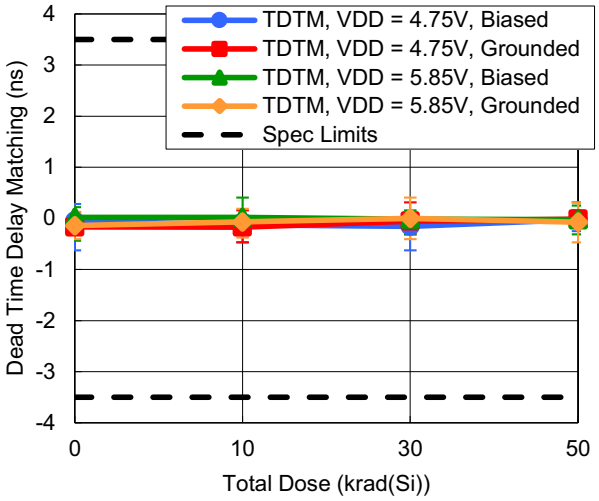


Figure 61. Dead Time Delay Matching

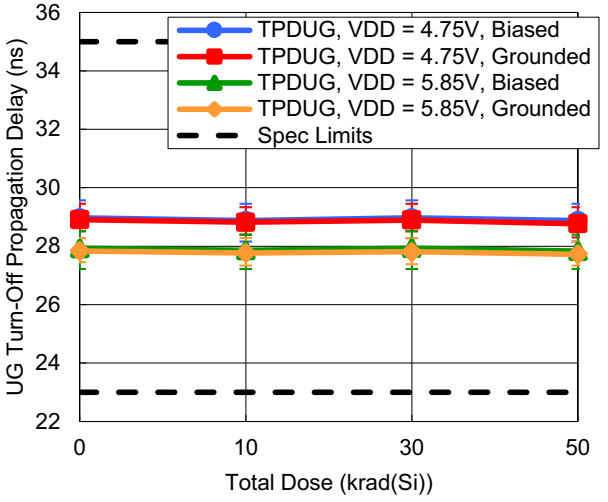


Figure 62. UG Turn-Off Propagation Delay

Bias configuration radiation test condition: VDD = EN = 13.2V; PHS = 13.2V; PWM = 5.5V; PVCC = BOOT-PHS = 5.5V (Cont.)

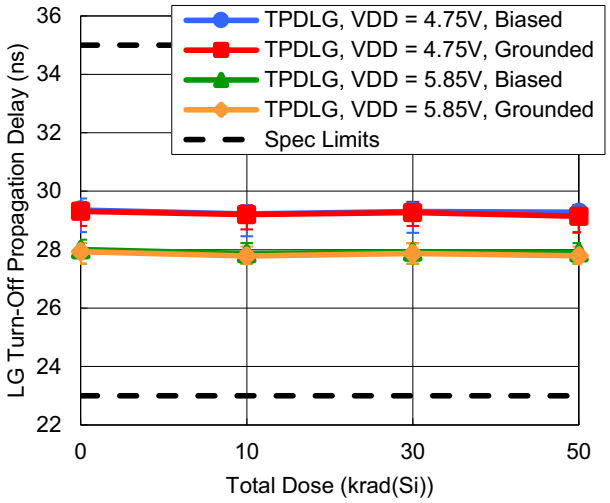


Figure 63. LG Turn-Off Propagation Delay

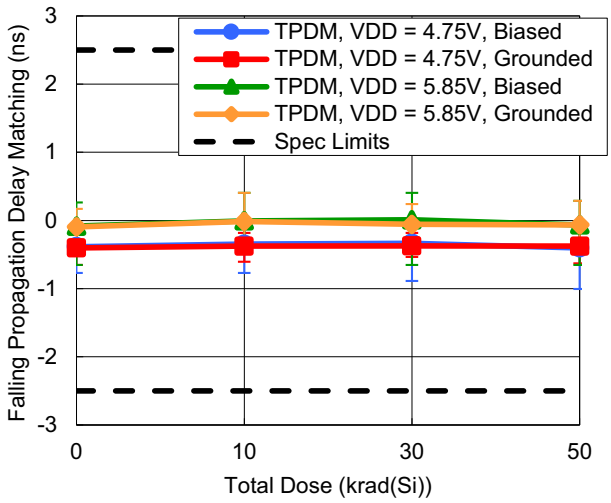


Figure 64. Falling Propagation Delay Matching

8.1.3 Conclusion

ATE characterization testing showed no rejects to the datasheet limits at all downpoints. Variables data for selected parameters are presented in Figure 55 through Figure 64. Table 2 shows the average of other key parameters with respect to total dose in tabular form. No differences between biased and unbiased irradiation were noted and the part is not considered bias sensitive.

Table 2. Response of Key Parameters vs TID

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Quiescent Supply Current	IDDQ_10kΩ	Biased	3.55	3.55	3.55	3.54	mA
		Ground	3.66	3.66	3.67	3.66	
		Limit -	-	-	-	-	
		Limit +	6	6	6	6	
BOOT Supply Current	IQ_BOOT	Biased	523.87	525.93	527.13	528.21	uA
		Ground	524.10	524.41	524.85	524.32	
		Limit -	-	-	-	-	
		Limit +	650	650	650	650	
FB Voltage	VFB	Biased	1.20	1.20	1.20	1.20	V
		Ground	1.20	1.20	1.20	1.19	
		Limit -	1.188	1.188	1.188	1.188	
		Limit +	1.212	1.212	1.212	1.212	
PVCC with FB = PVCC VDD = 4.85V	PVCC_FB	Biased	4.455	4.454	4.451	4.450	V
		Ground	4.449	4.450	4.448	4.446	
		Limit -	4.4	4.4	4.4	4.4	
		Limit +	4.6	4.6	4.6	4.6	

Table 2. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
PVCC with FB = PVCC VDD = 13.2V	PVCC_FB	Biased	4.461	4.461	4.458	4.457	V
		Ground	4.455	4.456	4.454	4.453	
		Limit -	4.4	4.4	4.4	4.4	
		Limit +	4.6	4.6	4.6	4.6	
PVCC = 5.45V with VDD = 5.85V	PVCC_FB	Biased	5.446	5.444	5.441	5.440	V
		Ground	5.439	5.439	5.437	5.436	
		Limit -	4.4	4.4	4.4	4.4	
		Limit +	4.6	4.6	4.6	4.6	
PVCC = 5.45V with VDD = 13.2V	PVCC_FB	Biased	5.451	5.449	5.447	5.446	V
		Ground	5.444	5.444	5.442	5.441	
		Limit -	4.4	4.4	4.4	4.4	
		Limit +	4.6	4.6	4.6	4.6	
AVCC LDO Voltage with VDD = 13.2V	AVCC	Biased	5.035	5.035	5.036	5.035	V
		Ground	5.037	5.035	5.038	5.042	
		Limit -	4.7	4.7	4.7	4.7	
		Limit +	5.3	5.3	5.3	5.3	
AVCC LDO Voltage with VDD = 5.25V	AVCC	Biased	5.033	5.033	5.033	5.032	V
		Ground	5.035	5.032	5.036	5.039	
		Limit -	4.7	4.7	4.7	4.7	
		Limit +	5.3	5.3	5.3	5.3	
PWM High Threshold with VDD = 4.75V	VPWMH	Biased	2.653	2.654	2.654	2.662	V
		Ground	2.655	2.653	2.654	2.655	
		Limit -	-	-	-	-	
		Limit +	2.8	3.8	4.8	5.8	
PWM High Threshold with VDD = 13.2V	VPWMH	Biased	2.654	2.658	2.661	2.660	V
		Ground	2.653	2.653	2.659	2.656	
		Limit -	-	-	-	-	
		Limit +	2.8	3.8	4.8	5.8	
PWM Mid Level Upper Range with VDD = 4.75V	VPWMMH	Biased	2.545	2.552	2.553	2.558	V
		Ground	2.550	2.555	2.559	2.554	
		Limit -	2.4	2.4	2.4	2.4	
		Limit +	2.8	3.8	4.8	5.8	
PWM Mid Level Upper Range with VDD = 13.2V	VPWMMH	Biased	2.553	2.555	2.563	2.565	V
		Ground	2.560	2.565	2.565	2.565	
		Limit -	2.4	2.4	2.4	2.4	
		Limit +	2.8	3.8	4.8	5.8	

Table 2. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
PWM Mid Level Lower Range with VDD = 4.75V	VPWMML	Biased	1.299	1.300	1.300	1.300	V
		Ground	1.300	1.299	1.300	1.299	
		Limit -	0.95	0.95	0.95	0.95	
		Limit +	1.45	1.45	1.45	1.45	
PWM Mid Level Lower Range with VDD = 13.2V	VPWMML	Biased	1.301	1.301	1.304	1.302	V
		Ground	1.301	1.302	1.304	1.301	
		Limit -	0.95	0.95	0.95	0.95	
		Limit +	1.45	1.45	1.45	1.45	
PWM Low Threshold with VDD = 4.75V	VPWML	Biased	1.095	1.096	1.095	1.091	V
		Ground	1.098	1.098	1.096	1.095	
		Limit -	0.95	0.95	0.95	0.95	
		Limit +	-	-	-	-	
PWM Low Threshold with VDD = 13.2V	VPWML	Biased	1.096	1.096	1.099	1.094	V
		Ground	1.098	1.096	1.096	1.098	
		Limit -	0.95	0.95	0.95	0.95	
		Limit +	-	-	-	-	
LG to UG Dead Time; 10kΩ	TDTLU_10kΩ	Biased	51.0	51.2	50.9	50.7	ns
		Ground	51.0	51.0	50.8	50.6	
		Limit -	40	40	40	40	
		Limit +	55	55	55	55	
UG to LG Dead Time; 10kΩ	TDTUL_10kΩ	Biased	51.0	51.2	50.9	50.7	ns
		Ground	51.2	51.1	50.8	50.7	
		Limit -	40	40	40	40	
		Limit +	55	55	55	55	
Dead Time Matching; 10kΩ	TDTM_10kΩ	Biased	0.02	0.02	-0.02	-0.03	ns
		Ground	-0.14	-0.07	0.00	-0.07	
		Limit -	-3.5	-3.5	-3.5	-3.5	
		Limit +	3.5	3.5	3.5	3.5	
PWM Low-to-UG Low Propagation Delay	TPDUG	Biased	27.9	27.9	27.9	27.8	ns
		Ground	27.8	27.8	27.8	27.7	
		Limit -	23	23	23	23	
		Limit +	35	35	35	35	
PWM High-to-LG Low Propagation Delay	TPDLG	Biased	28.0	27.9	27.9	27.9	ns
		Ground	27.9	27.8	27.9	27.8	
		Limit -	23	23	23	23	
		Limit +	35	35	35	35	

Table 2. Response of Key Parameters vs TID (Cont.)

Parameter	Symbol	Irradiation Condition	Pre-Rad Value	10krad(Si)	30krad(Si)	50krad(Si)	Unit
Propagation Delay Matching	TPDM	Biased	-0.08	-0.01	0.01	-0.07	ns
		Ground	-0.09	-0.02	-0.06	-0.07	
		Limit -	-2.5	-2.5	-2.5	-2.5	
		Limit +	2.5	2.5	2.5	2.5	

8.2 Single Event Effects Testing

8.2.1 Introduction

The intense proton and heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE) in electronic circuitry, including Single Event Upset (SEU), Single Event Transient (SET), Single Event Functional Interrupt (SEFI), Single Event Gate Rupture (SEGR), and Single Event Burnout (SEB). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. Individual electronic components should be characterized for predictable and reliable space system operation to determine their SEE response. This report discusses the SEE testing results performed on the ISL71441M Half Bridge GaN FET Driver.

8.2.2 Test Facility

SEE Testing was performed at the Texas A&M University (TAMU) Radiation Effects Facility of the Cyclotron Institute heavy ion facility. This facility is coupled to a K500 super-conducting cyclotron that can generate a wide range of particle beams with the various energy, flux, and fluence levels needed for advanced radiation testing. You can find further details on the test facility on their website. The Devices Under Test (DUTs) were in air at 40mm from the Aramica window for the ion beam. SET testing was performed on June 11, 2023, with normal incidence silver ions for LET of 45.8MeV•cm^2/mg at the surface of the device. The LET of the ions in the active silicon layer ranges from 47.9MeV•cm^2/mg to 49.8MeV•cm^2/mg. Signals were communicated to and from the DUT test fixture through 20ft cables connecting to the control room.

8.2.3 Test Setup

The test boards used for SEE testing were configured so that two devices could be irradiated simultaneously. The DUT was evaluated for SEE using a general-purpose engineering evaluation board configured in a half-bridge configuration. Specific configurations were imposed for different types of SEE testing. For Destructive SEE (DSEE) testing on VDD and AVCC/PVCC, the half-bridge drove a 1µH/660µF LC output filter representing a typical DC-DC converter application. For DSEE testing of PVIN and SET testing, as it was critical to know the exact voltage or pulse width on the PHS pin, a 500kΩ load from PHS to GND was used to synchronously control the PHS voltage and pulse width through the upper and lower GaN FET. The PWM switching frequency of 500kHz was chosen to match a typical application when used with the ISL73847SEH PWM Controller. The 25%PWM duty cycle was chosen as it is a good low-duty cycle for the PWM controller with which the driver is intended to operate, but it is not so low that SETs on a PHS pulse width may have been indiscernible.

For SET testing, the PWM input levels switched between 1.0V and 2.8V for logic level low and high; the VDD and PVIN were tested at 12V; the output capacitors for the internal AVCC and PVCC LDO were derated down to 0.68µF from their 1.0µF minimum recommended value (-32% shift); the dead-time control setting on RDU and RDL were set at 10kΩ (maximum dead-time).

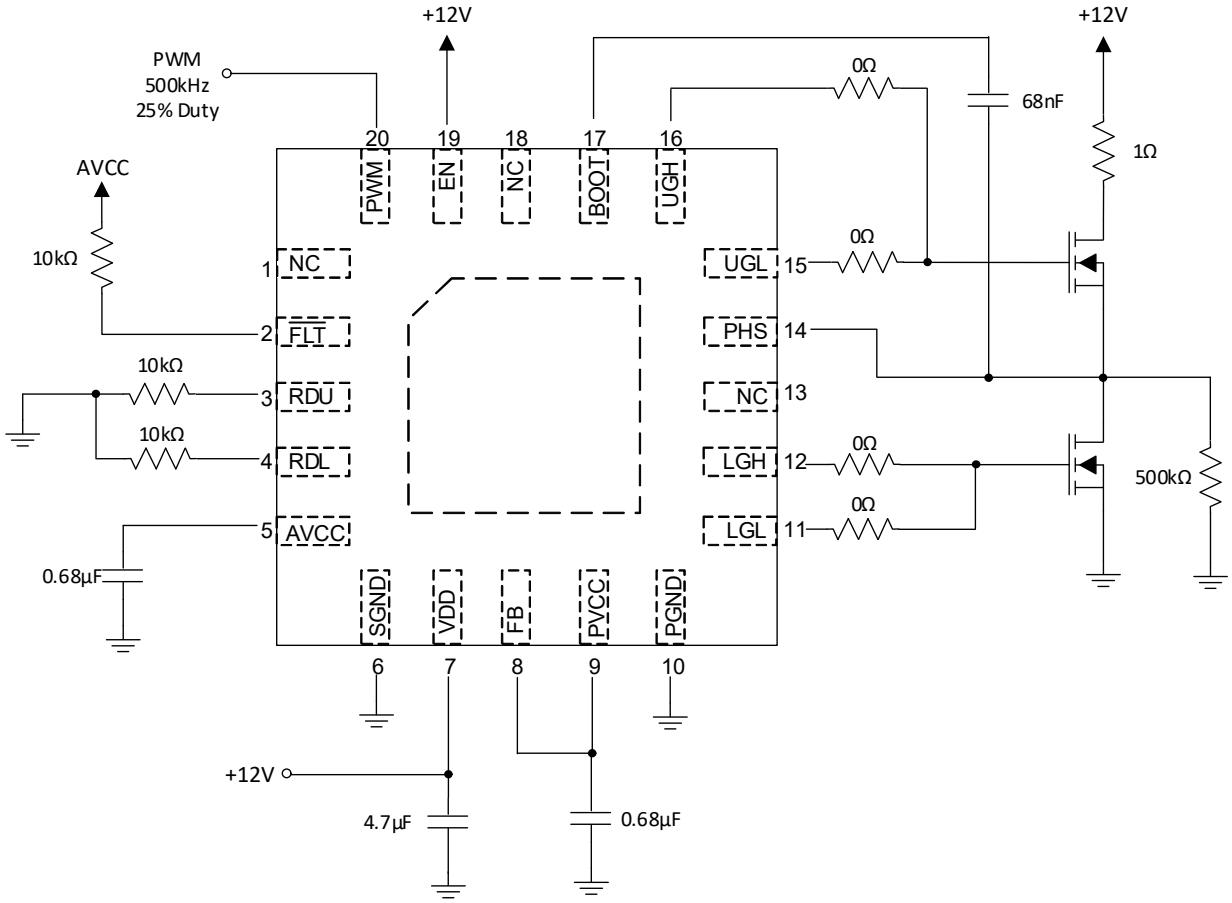


Figure 65. SET Test Board Block Diagram

8.2.4 DSEE Results

Results show the ISL71441M did not experience any DSEE events on VDD up to 20V, AVCC/PVCC up to 6.3V, and, PVIN up to 16.5V.

8.2.5 SET Results

For SET testing, the die temperature was 25°C. During SET testing, the device was monitored for two different types of SETs. The first type of SET was an event that caused a shoot-through, which is when the upper and lower gate drivers are on simultaneously. A 1Ω resistor was inserted between the drain of the high-side GaN FET and the PVIN bus voltage to capture a shoot-through SET. During a shoot-through event, both GaN FETs turn on, pulling the drain side of the resistor toward 0V while the input supply holds up the PVIN side. The drain side of this 1Ω resistor was used to monitor for a shoot-through condition. The second type of SET was a PHS pulse width deviation event. A PHS pulse width deviation SET was defined as an event that caused a pulse width deviation of PHS from the average pre-beam PHS operating pulse width beyond ±65ns for a switching frequency of 500kHz and a 25% duty cycle operation. The pulse width deviation of ±65ns was chosen because it represents a 50% delta of 135ns, the minimum on-time for the ISL73847M controller with which the ISL71441M is designed to operate. Some PHS pulse width deviations were extreme enough that the UG-PHS pulse was completely missed. For pulse width deviation events, the trigger was set to capture events in which the PHS pulse deviated by ±65ns from the operating pulse width of the driver before the beam was turned on. For shoot-through events, the trigger was set to capture events in which the high-side GaN FET drain voltage decreased by 6V.

Table 3 shows the results of the SET testing. Zero shoot-through SET events were captured on the four DUTs to a total fluence of 4.0E+7 ions/cm^2. For pulse width deviations, 614 events were captured across the four DUTs to a total fluence of 4.0E+7 ions/cm^2. Nearly all of the PHS pulse width deviations that were not extreme enough to

cause a missing UG-PHS pulse were within the ±65ns window criterion. This is because the criterion for the trigger was the difference between the average width of the PHS pulses before the beam was turned on and the width of the PHS pulse under beam. In contrast, the criterion for this analysis is the difference between the average PHS pulse width of eight cycles preceding the trigger and the pulse width of the PHS pulses of the SET trigger.

Table 3. SET Results for LET = 46MeV •cm^2/mg

# of DUTs	RDU/RDL Resistor (kΩ)	V_{DD} = PVIN (V)	Total Fluence (ions/cm^2)	Shoot-Through		Pulse Width Deviation		Missing Pulse	
				# of Events	σ (cm^2)	# of Events	σ (cm^2)	# of Events	σ (cm^2)
4	10	12	4.00E+07	0	2.50E-08	614	1.53E-05	2	5.00E-08

Figure 66 shows a histogram of the PHS pulse width deviations within the ±65ns criterion, with most being a positive pulse width deviation.

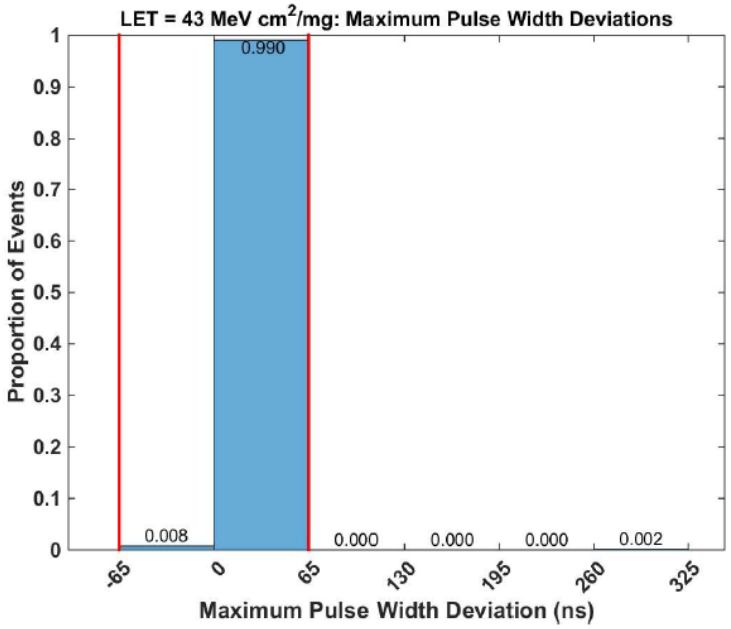


Figure 66. Histogram of Maximum Pulse Width Deviations

Figure 67 shows a typical SET of an extreme pulse width deviation causing a complete UG-PHS missing pulse. The UG-PHS pulse recovers during the next switching cycle. No loss of LG pulse was observed. *Note:* In Figure 67, the PWM data was not correctly collected and should be disregarded for analysis. However, we know PWM is functional due to the operation of the other signals dependent on a valid PWM.

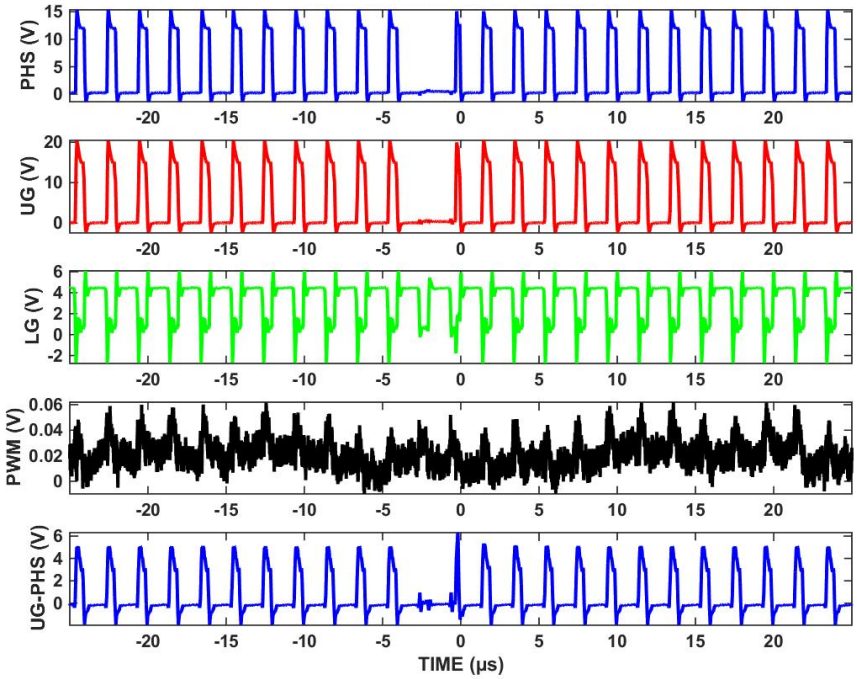


Figure 67. Typical Missing Pulse SET Transient

8.2.6 Discussions and Conclusions

The ISL71441M was found to be free from DSEE with the following maximal parameter set: VDD = 20V, AVCC/PVCC = 6.5V, and PVIN = 16.5V at a case temperature of 125°C±10°C.

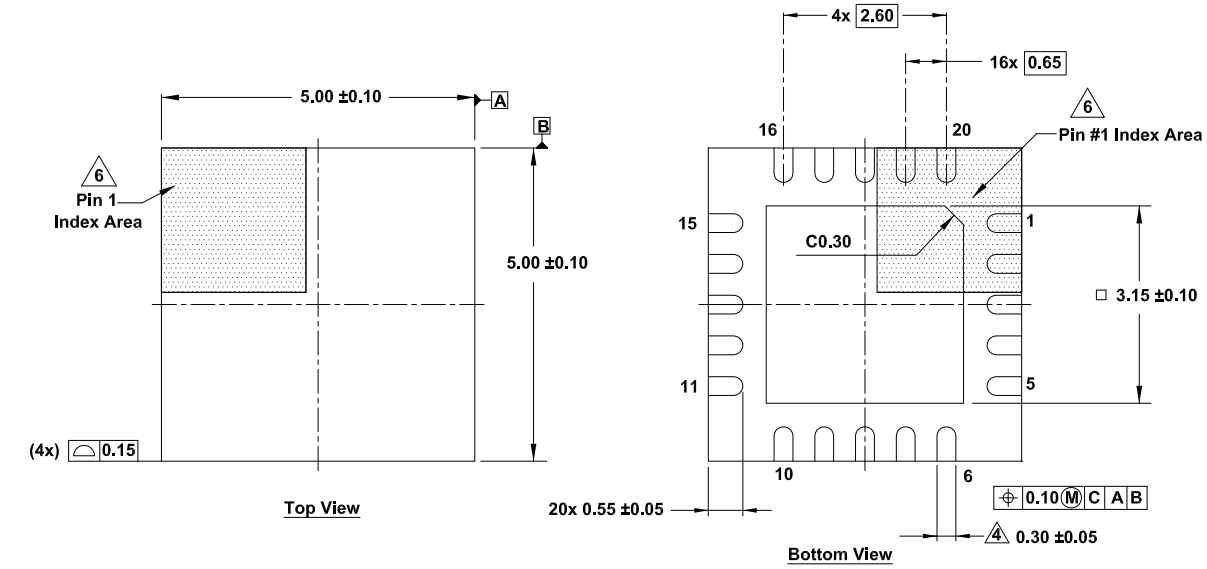
SET testing on the ISL71441M was done at VDD = PVIN = 12V, RDU and RDL resistors set to 10kΩ for maximum dead time and with the PWM input switching between 1.0V and 2.8V at 500kHz, 25% duty cycle at a case temperature of approximately 25°C.

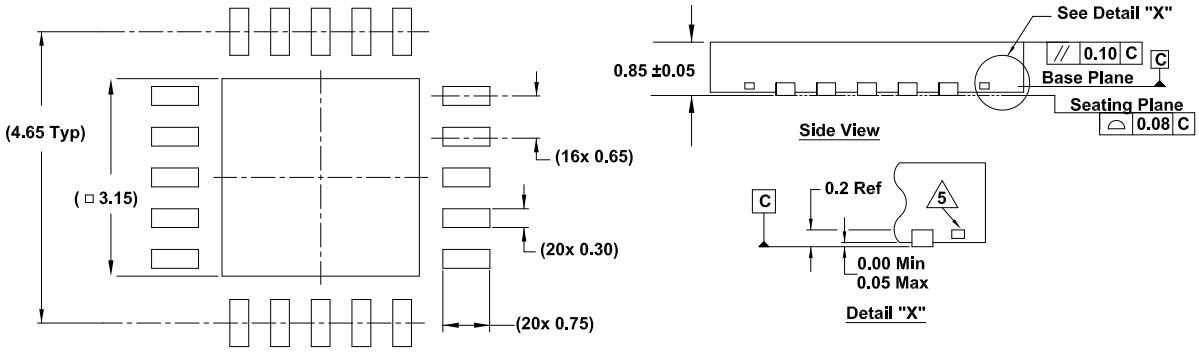
The ISL71441M exhibited zero shoot-through events. Four units were tested to a total fluence of 4.0E7ions/cm^2 with an effective cross-section of 2.5E-08cm^2. The ISL71441M exhibited 614 pulse width deviation events on the PHS pulse width that exceeded ±65ns of its pre-beam pulse width. Of the 614 pulse width deviation events, two were extreme enough to lose the entire UG pulse during that switching cycle. All 614 events recovered normal operation during the next switching cycle. The pulse width deviations were tested at the same time as the shoot-through testing with the same test conditions and total fluence of the four units to 4.0E7ions/cm^2. This represents a cross section of 1.5E-05 cm^2 for pulse width deviations and 5.0E-8cm^2 for missing pulses.

9. Package Outline Drawing

For the most recent package outline drawing, see L20.5x5B.

L20.5x5B
20 Lead Quad Flat No-Lead Plastic Package
Rev 0, 6/20





Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

10. Ordering Information

Part Number[1][2]	Part Marking	Radiation Lot Acceptance Testing	TID Data Pack Included	Package Description[3] (RoHS Compliant)	Package Drawing	Carrier Type[4]	Temp. Range
ISL71441MRZ	71441MRZ	N/A	No	20Ld 5×5mm QFN	L20.5x5B	Tray	-55 to 125°C
ISL71441MRZ-T						Reel, 2.5k	
ISL71441M30RZ		30krad(Si)	Yes			Tray	
ISL71441M30RZ-T						Reel, 2.5k	
ISL71441M50RZ		50krad(Si)	Yes			Tray	
ISL71441M50RZ-T						Reel, 2.5k	
ISL71441MEV1Z	ISL71441M Evaluation Board						
ISL73847MEV1Z	2-Phase PWM Controller + Driver + Die GaN FET Evaluation Board						
ISL73847MDEMO1Z	2-Phase PWM Controller + Driver + Die GaN FET Reference Design Board						
ISL73847MDEMO2Z	1-Phase PWM Controller + Driver + Die GaN FET Reference Design Board						

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu-Ag plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71441M product page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
1.03	Jan 16, 2025	Updated pin descriptions for SGND, PGND, and EPAD. Added SGND to PGND Parameter to the abs max section. Updated the Layout Guidelines section.
1.02	Sep 4, 2024	Added ISL71441MRZ part information. Updated SEE feature bullets. Updated the Radiation Tolerance and Test Facility sections.
1.01	Jan 5, 2024	Updated Features bullets. Updated part numbers throughout document. Added Dual Complimentary Low-Side GaN FET Driver section.
1.00	Jun 26, 2023	Initial release

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