ISL71934M

Radiation Tolerant SP2T RF Switch, 50MHz to 6000MHz

The ISL71934M is a high reliability, low insertion loss, 50Ω SP2T absorptive RF switch designed for a multitude of wireless and other RF applications. This device covers a broad frequency range from 50MHz to 6000MHz. In addition to providing low insertion loss, the ISL71934M delivers high linearity and high isolation performance while providing a 50Ω termination to the unused RF input port.

The ISL71934M uses a single positive supply voltage of 2.7V to 5.25V supporting three states using either 3.3V or 1.8V control logic.

Competitive Advantage

The ISL71934M provides the following advantages:

- Constant impedance $K_{|Z|}$ during switching transition
- Insertion loss = 0.79dB (at 2GHz)
- RFX to RFC isolation = 67dB (at 2GHz)
- IIP3 = +64dBm (at 2GHz)
- Active port operating power handling = 34dBm
- Term port operating power handling = 27dBm

Applications

- Satellite communications system
- Antenna switching
- IF switching
- Digital pre-distortion feedback

Features

- High isolation:
  - 70dB at 1GHz
  - 67dB at 2GHz
  - 65dB at 3GHz
  - 65dB at 4GHz
- High linearity:
  - IIP2 of 111dBm
  - IIP3 of 64dBm at 2GHz
- Wide single 2.75V to 5.25V supply voltage range
- 3.3V and 1.8V compatible control logic
- Operating temperature: -55°C to +125°C
- 3x3mm 16-TQFN package
- Ni/Pd/Au lead finish (Tin (Sn)-free)
- Characterized radiation levels
  - Low Dose Rate (LDR) (0.01rad(Si)/s): 30krad(Si)
  - Single event burnout LET 43MeV•cm^2/mg
- Manufactured using SOI wafer fab process

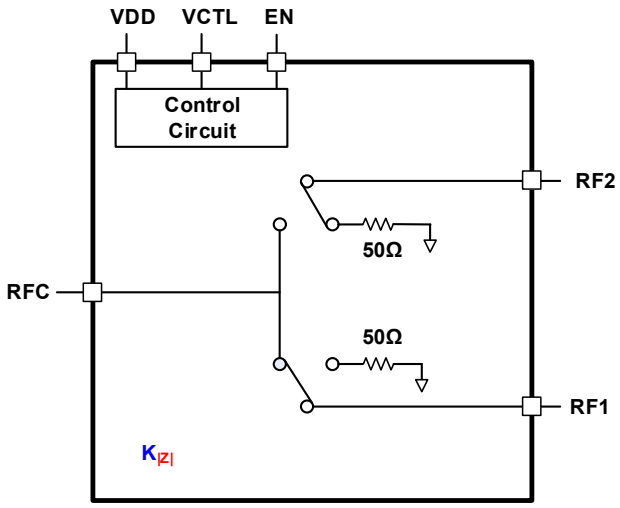


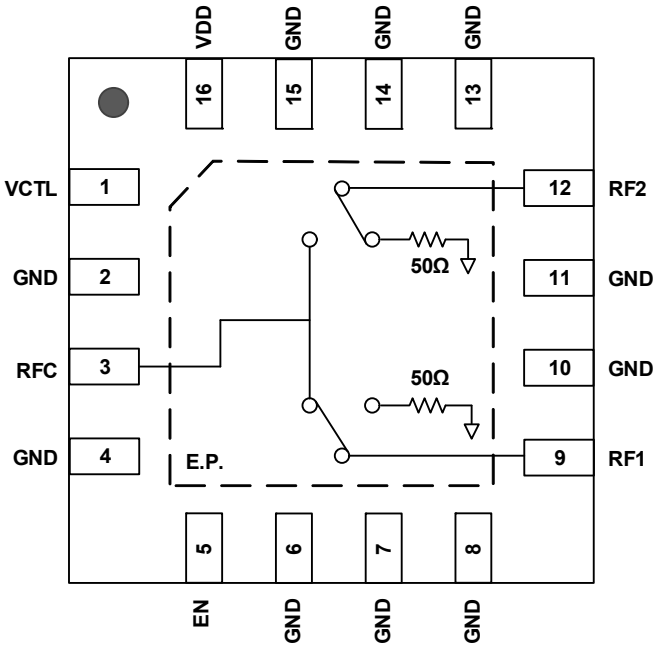
Figure 1. Block Diagram

Contents

1. Pin Information

1.1 Pin Configuration

16 Ld TQFN
Top View



1.2 Pin Descriptions

Pin	Name	Function
1	VCTL	Controls the selected path when EN is low. It is disabled when EN is logic high (see Absolute Maximum Ratings).**Note:** VDD must be applied before or concurrently to voltage being applied to this pin.
3	RFC	RF Common Port. Matched to 50Ω when one of the two RF ports is selected. **Note:** If this pin is not 0V DC, an external coupling capacitor must be used.
2, 4, 6, 7, 8, 10, 11, 13, 14, 15	GND	Ground. Also, internally connected to the ground paddle. Ground this pin as close to the device as possible.
5	EN	EN as a logic low allows VCTL to control the selected switch path. With EN set to logic high puts the part in all paths off state and disables the control of VCTL (Absolute Maximum Ratings). **Note:** VDD must be applied before or concurrently to voltage being applied to this pin.
9	RF1	RF1 Port. Matched to 50Ω. **Note:** If this pin is not 0V DC, an external coupling capacitor must be used.
12	RF2	RF2 Port. Matched to 50Ω. **Note:** If this pin is not 0V DC, an external coupling capacitor must be used.
16	VDD	Power Supply. Bypass to GND with capacitors shown in the Typical Application Circuit as close as possible to pin.
	EP	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device and into the PCB ground planes. These multiple ground vias are also required to achieve the specified RF performance.

2. Specifications

2.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter/Condition		Symbol	Minimum	Maximum	Unit
VDD to GND		V_{DD}	-0.3	+5.5	V
VCTL, EN to GND		V_{logic}	-0.3	3.6	V
RF1, RF2, RFC to GND		V_{RF}	-0.3	+0.3	V
RF Input Power[1]	RF1 or RF2 as an input (Connected to RFC)	P_{RF12}		36	dBm
	RFC as an input (Connected to RF1 or RF2)	P_{RFC}		36	
	RFC as an input (All off state)	P_{RFC_OFF}		30	
	RF1 or RF2 as input (Terminated states)	P_{RF12_TERM}		30	
	RF1 and RF2 as inputs (All off state)	P_{RF12_OFF}		30[2]	
ESD Rating		**Value**			**Unit**
Human Body Model (Tested per JESD22-A114)		V_{ESDHBM}	1.5		kV
Charged Device Model (Tested per JESD22-C101)		V_{ESDCDM}	2		kV

1. V_{DD} = 2.7V to 5.25V, 250MHz ≤ F_{RF} ≤ 6000MHz, T_C = 105°C, Z_S = Z_L = 50Ω.
2. Each port.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
16 Ld TQFN	59	17

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature (T_{JMAX})		+125	°C
Storage Temperature Range (T_{ST})	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

2.3 Recommended Operating Conditions

Parameter	Symbol	Condition		Minimum	Typical	Maximum	Units
Supply Voltage	V_{DD}			2.7		5.25	V
Operating Temperature Range	T_{CASE}	Exposed Paddle Temperature		-55		+125	°C
RF Frequency Range	F_{RF}			50		6000	MHz
RF Continuous Input CW Power (Non-Switched)[1]	P_{RF}	RFC connected to RF1 or RF2[2]				34	dBm
		RF1/ RF2 Input, Terminated State[3][4]				27	dBm
		RFC Input, All off State				27	dBm
RF Continuous Input Power (RF Hot Switching CW)[1]	P_{RFSW}	RFC Input, switching between RF1 and RF2.	T_C = 85 ºC			30	dBm
			T_C = 105 ºC			30	dBm
		RFC Input, switching into or out of, All off State.	T_C = 85 ºC			27	dBm
			T_C = 105 ºC			27	dBm
		RF1 or RF2 as input, switched between RFC and Term.	T_C = 85 ºC			27	dBm
			T_C = 105 ºC			27	dBm
		RF1 and RF2 as inputs, switching into or out of All off State.[4]	T_C = 85 ºC			27	dBm
			T_C = 105 ºC			27	dBm
RF1/2 Port Impedance	Z_{RFx}				50		Ω
RFC Port Impedance	Z_{RFC}				50		Ω

1. Levels based on: V_{DD} = 3.1V to 5.25V, 250MHz ≤ F_{RF} ≤ 6000MHz, Z_S = Z_L = 50Ω. See Figure 2 for power handling derating vs. RF frequency.
2. Input could be: RFC, RF1, or RF2 (applied to only one input).
3. Any RF1 / RF2 termination state. Power level specified is for each port.
4. Power level specified is for each port.

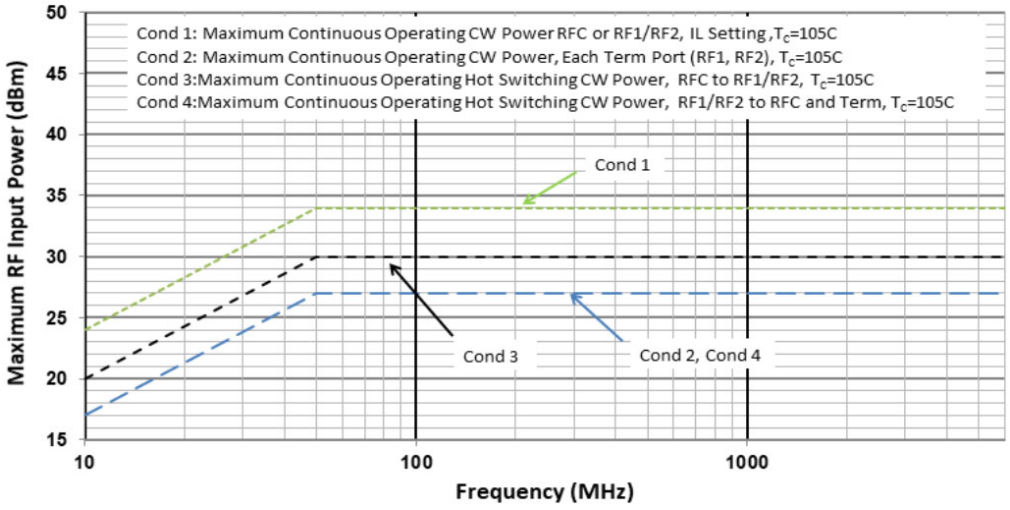


Figure 2. Maximum RF Input Operating Power vs. Frequency

2.4 Electrical Specifications

Typical Application Circuit, V_{DD} = 5.0V, T_C = +25°C, F_{RF} = 2000MHz, Driven Port = RF1 or RF2, input power = 10dBm, ZS = ZL = 50Ω, PCB board trace and connector losses are de-embedded unless otherwise noted.

Parameter	Symbol	Condition	Minimum[1][2]	Typical	Maximum[1][2]	Units
Logic Input High Threshold	V_{IH}		**1.1**		**3.6**	V
Logic Input Low Threshold	V_{IL}		**-0.3**		**0.6**	V
Logic Current	I_{IH}, I_{IL}	For each control pin	**-1**		**+1**	µA
DC Current	I_{DD}	V_{DD} = 3.3 V		200	**400**	µA
		V_{DD} = 5.0 V		260	**450**	µA
Insertion Loss RFC to RF1 / RF2	IL	50MHz		0.68		dB
		1GHz		0.73		dBm
		2GHz		0.87	**1.1**	dBm
		3GHz		0.82		dBm
		4GHz		0.93		dBm
		6GHz		1.06		dBm
Isolation RFC to RF1 / RF2	ISOC	50MHz	76	79		dB
		1GHz	67	70		dBm
		2GHz	62	67		dBm
		3GHz	61	65		dBm
		4GHz	58	65		dBm
		6GHz	47	58		dBm
Isolation RF1 to RF2	ISOX	50MHz		86		dB
		1GHz		64		dBm
		2GHz		58		dBm
		3GHz		54		dBm
		4GHz		51		dBm
		6GHz		45		dBm
Return Loss RFC, RF1, RF2	RF_{RL}	50MHz		25		dB
		1GHz		25		dBm
		2GHz		21		dBm
		3GHz		18		dBm
		4GHz		16		dBm
		6GHz		15		dBm
Return Loss RF1, RF2 terminated	RFT_{RL}	50MHz		40		dBm
		1GHz		31		dBm
		2GHz		35		dBm
		3GHz		23		dBm
		4GHz		17		dBm
		6GHz		19		dBm

Typical Application Circuit, V_{DD} = 5.0V, T_C = +25°C, F_{RF} = 2000MHz, Driven Port = RF1 or RF2, input power = 10dBm, ZS = ZL = 50Ω, PCB board trace and connector losses are de-embedded unless otherwise noted. **(Cont.)**

Parameter	Symbol	Condition		Minimum[1][2]	Typical	Maximum[1][2]	Units
Input 1dB Compression[3]	ICP_{1dB}	50MHz			33		dBm
		1GHz			35		dBm
		2GHz			36		dBm
		3GHz			36		dBm
		4GHz			35		dBm
Input 0.1dB Compression[3]	$ICP_{0.1dB}$	V_{DD} = 5.0 V	50MHz		30		dBm
			2GHz		32		dBm
			3GHz		32		dBm
			4GHz		32		dBm
		V_{DD} = 3.1 V	50MHz		30		dBm
			2GHz		32		dBm
			3GHz		32		dBm
			4GHz		32		dBm
Input IP2	IIP2	F_{RF1} = 2000MHz, F_{RF2} = 1990MHz RFIN = RF1 or RF2 PIN = +20dBm / tone $F_{IP2} = F_{RF1} + F_{RF2}$			111		dBm
Input IP3	IIP3	RF Input = RF1 or RF2 PIN = +15 dBm/tone Δ F = 1MHz	50MHz		58		dBm
			1GHz		64		dBm
			2GHz		64		dBm
			2.5GHz		63		dBm
			4GHz		63		dBm
Non-RF Driven Spurious[4]	$Spur_{MAX}$	At any RF port when externally terminated into 50Ω			-114		dBm
Switching Time[5]	T_{SW}	50% control to 90% RF			325		ns
		50% control to 10% RF			255		ns
Maximum Switching Rate[6]	SW_{RATE}				25		kHz

1. Items in minimum/maximum columns in bold are established by Test.
2. Items in minimum/maximum columns that are not bold are established by Design Characterization.
3. The input 1dB compression point is a linearity figure of merit. For the maximum operating power levels, see Recommended Operating Conditions.
4. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 5.2MHz.
5. F_{RF} = 1GHz.
6. Minimum time required between switching of states = 1 / Maximum Switching Rate.

2.5 Control Mode

Table 1. Switch Control Truth Table

VCTL	EN	RFC to RF1	RFC to RF2
0	0	OFF	ON
1	0	ON	OFF
0	1	OFF	OFF
1	1	OFF	OFF

3. Typical Performance Graphs

V_{DD} = 3.3V, T_C = +25°C (T_C = Temperature of Exposed Paddle), F_{RF} = 2000MHz, Z_S = Z_L = 50Ω, P_{IN} = +10dBm for all small signal tests, RF1 or RF2 is the driven RF port and RFC is the output port, all unused RF ports terminated into 50Ω, unless otherwise specified

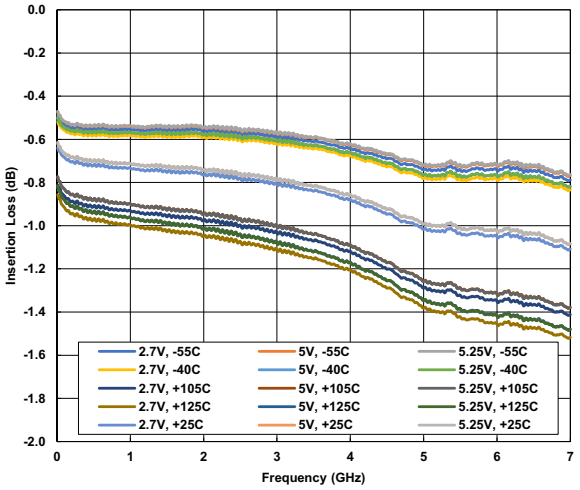


Figure 3. RF1 to RFC Insertion Loss

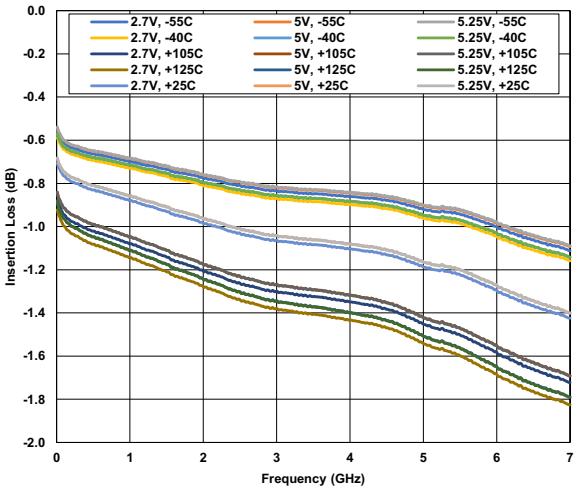


Figure 4. RF2 to RFC Insertion Loss

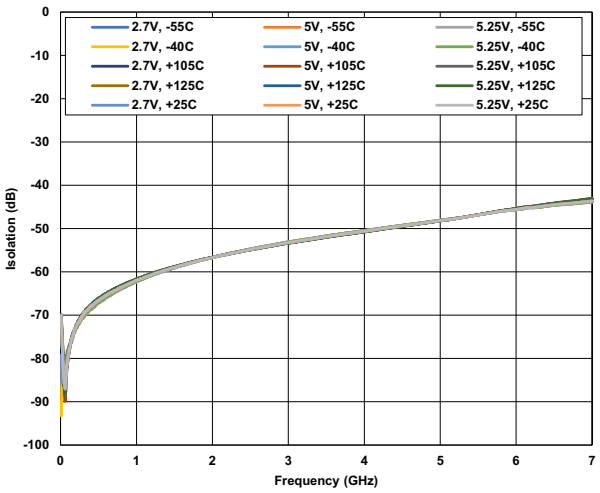


Figure 5. RF1 to RF2 to Isolation [RF1 Enabled]

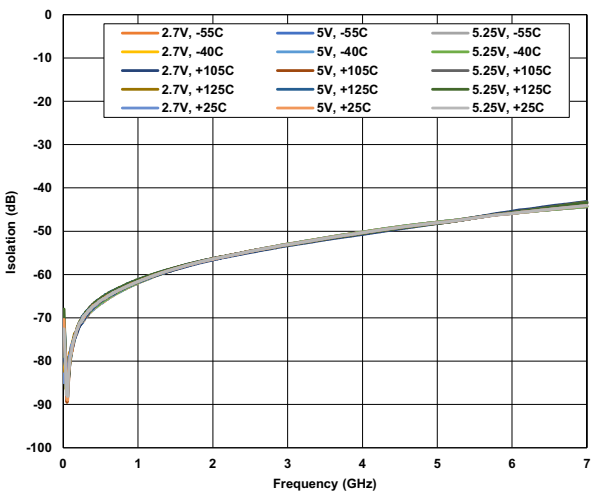


Figure 6. RF2 to RF1 Isolation [RF1 Enabled]

V_{DD} = 3.3V, T_C = +25°C (T_C = Temperature of Exposed Paddle), F_{RF} = 2000MHz, Z_S = Z_L = 50Ω, P_{IN} = +10dBm for all small signal tests, RF1 or RF2 is the driven RF port and RFC is the output port, all unused RF ports terminated into 50Ω, unless otherwise specified **(Cont.)**

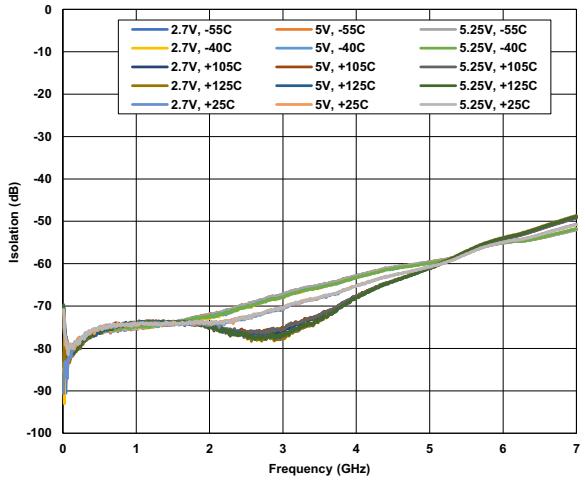


Figure 7. RF1 to RFC Isolation [RF2 Enabled]

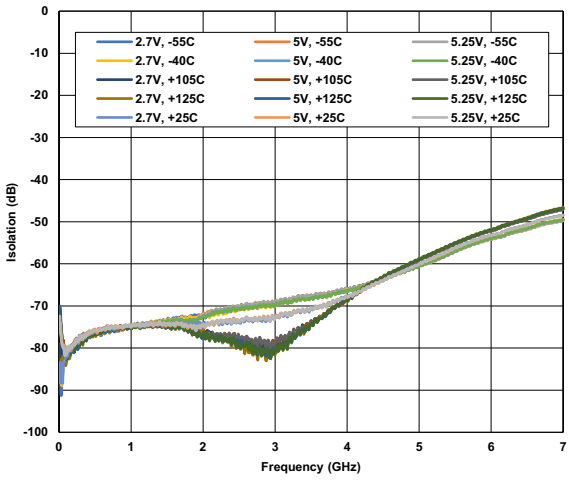


Figure 8. RF2 to RFC Isolation [RF1 Enabled]

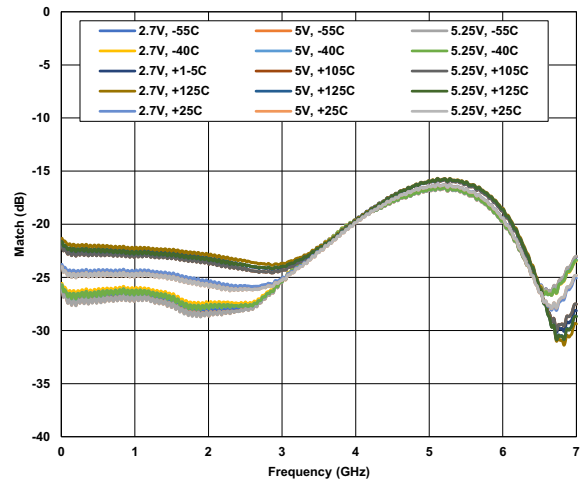


Figure 9. RF1 Port Match [RF1 Enabled]

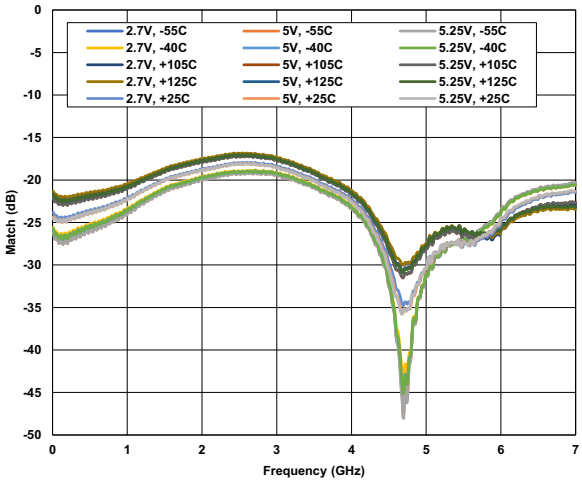


Figure 10. RF2 Port Match [RF2 Enabled]

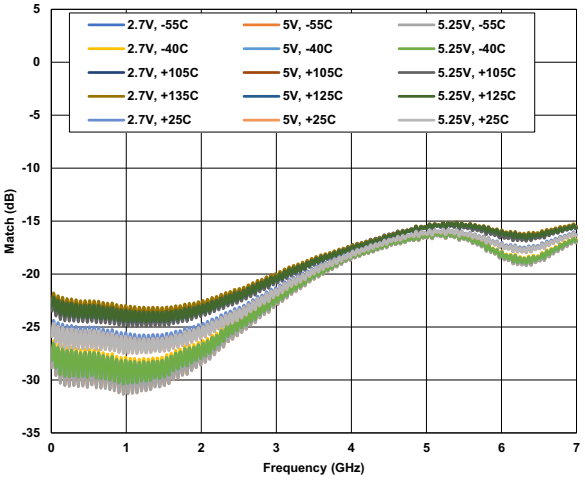


Figure 11. RFC Port Match [RF1 Enabled]

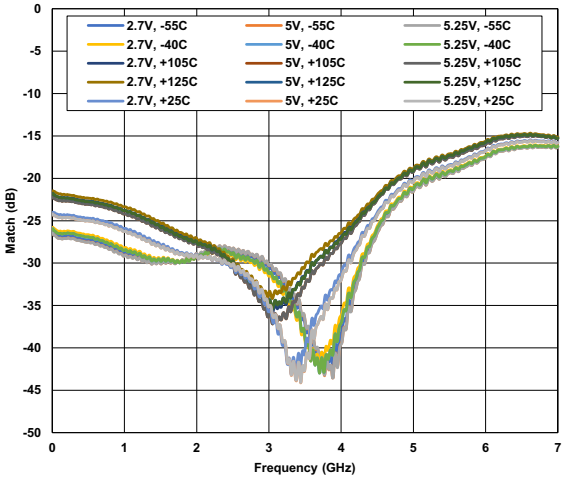


Figure 12. RFC Port Match [RF2 Enabled]

4. Applications Information

4.1 Default Start-up

There are no internal pull-up or pull-down resistors on the VCTL or EN pins.

4.2 Logic Control

Control pins VCTL and EN are used to set the state of the SP2T switch (see Absolute Maximum Ratings).

4.3 Power Supplies

Use a common V_{CC} power supply for all pins requiring DC power. Bypass all supply pins with external capacitors to minimize noise and fast transients. Supply noise can degrade noise figures and fast transients can trigger ESD clamps and cause them to fail. Supply voltage change or transients should have a slew rate smaller than 1V/20µs. In addition, keep all control pins at 0V (±0.3V) while the supply voltage ramps or while it returns to zero.

4.4 Control Pin Interface

If control signal integrity is a concern and clean signals cannot be ensured because of issues such as overshoot, undershoot, and ringing, the following circuit at the input of each control pin is recommended. This applies to control Pin 1 (VCTL) and Pin 5 (EN) as shown in Figure 13.

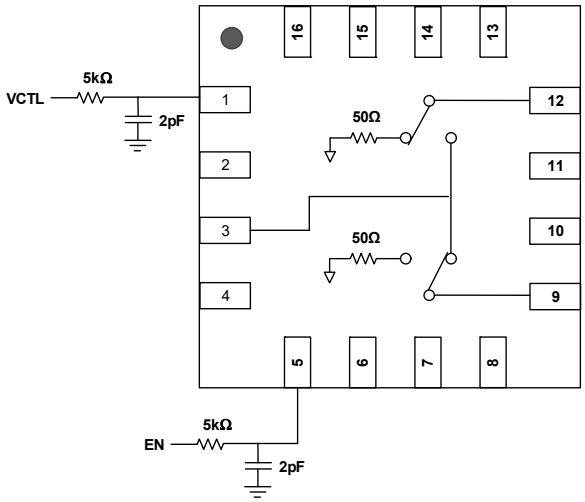


Figure 13. Typical Application Circuit

5. Radiation Tolerance

The ISL71934M is a radiation tolerant device for commercial space applications, Low Earth Orbit (LEO) applications, high altitude avionics, launch vehicles, and other harsh environments. The response of the device to Total Ionizing Dose (TID) radiation effects and Single-Event Effects (SEE) has been measured, characterized, and reported in the following sections. However, TID performance is not guaranteed through radiation acceptance testing, nor is the SEE characterized performance guaranteed.

5.1 Total Ionizing Dose (TID) Testing

5.1.1 Introduction

To determine the sensitivity of the ISL71934M to the total dose environment, the TID test was conducted. Test downpoints were 0krad(Si), 10krad(Si), 20krad(Si), and 30krad(Si). Total dose testing was performed using a Hopewell Designs N40 panoramic 60Co irradiator. The irradiations were performed at a dose rate of 0.00875rad(Si)/s. A PbAl box shielded the test fixture and devices under test against low energy secondary gamma radiation. The characterization matrix consisted of 18 samples irradiated under bias and 18 samples irradiated with all pins grounded. All electrical testing was performed outside the irradiator using Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

The bias configuration is shown in Figure 14.

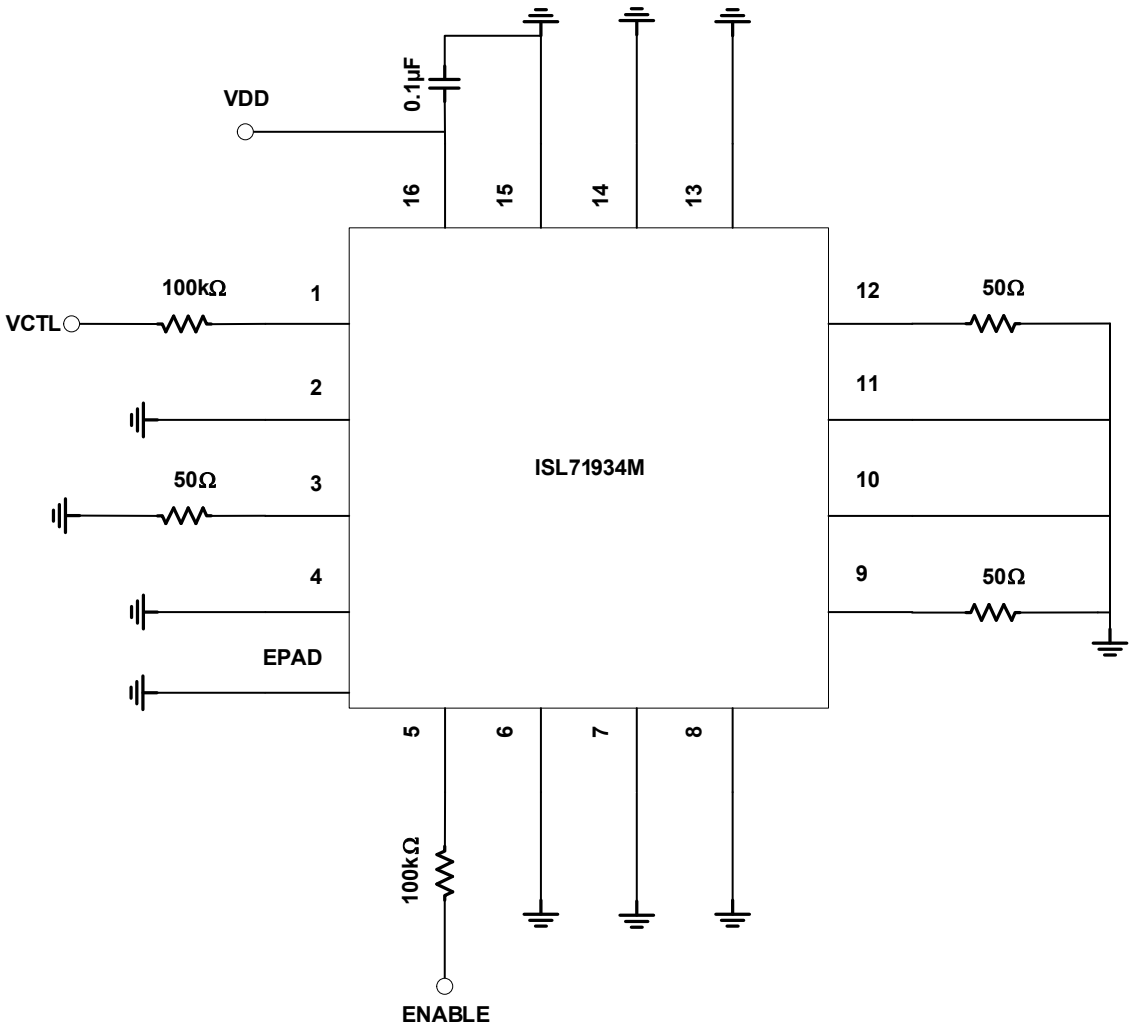


Figure 14. Bias Configuration

5.1.2 TID Results

Figure 15 through Figure 18 show the performance parameters for key specifications over TID.

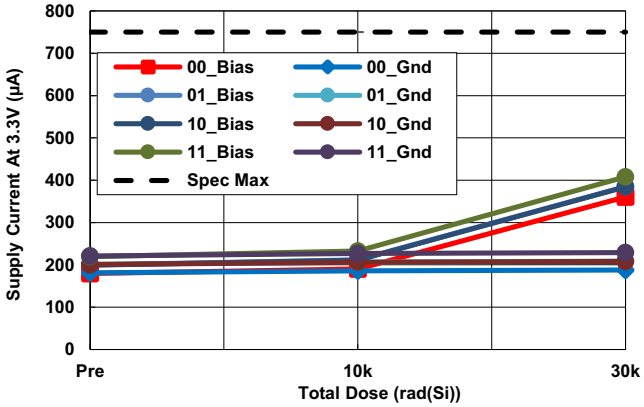


Figure 15. I_{DD} for V_{DD} = 3.3V vs TID

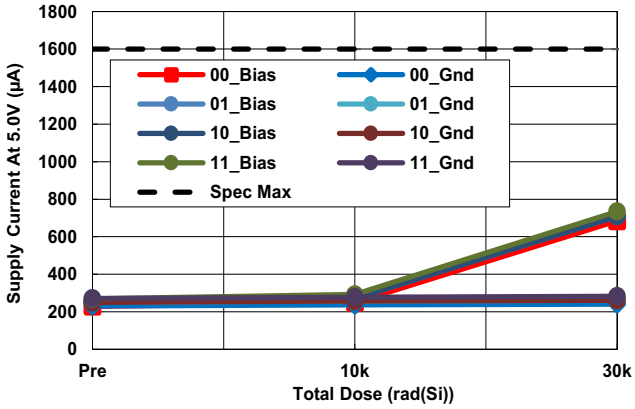


Figure 16. I_{DD} for V_{DD} = 5V vs TID

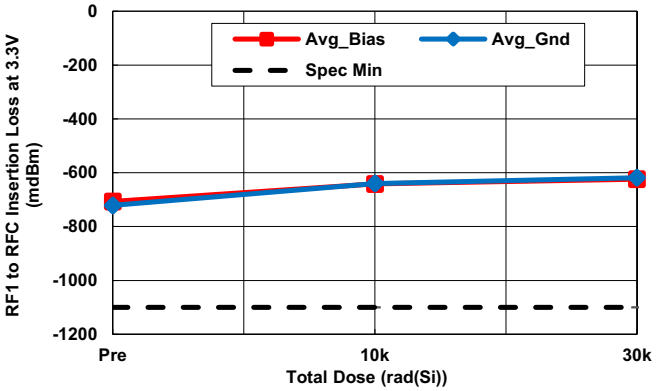


Figure 17. Insertion Loss RF1 to RFC at 2GHz and V_{DD} = 3.3V vs TID

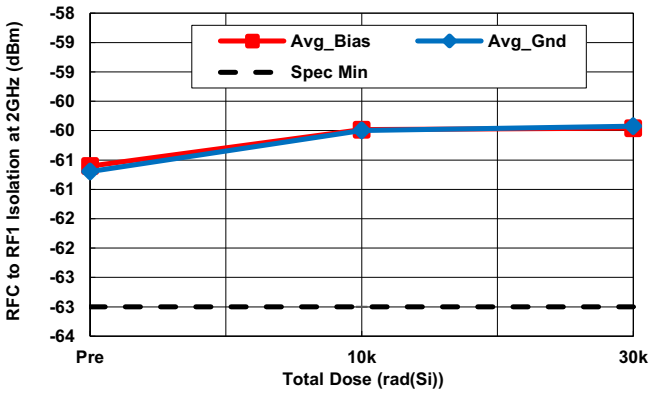


Figure 18. RFC to RF1 Isolation at 2GHz and V_{DD} = 3.3V vs TID

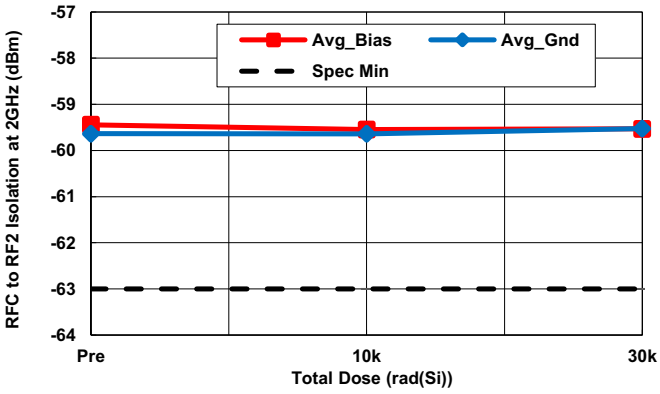


Figure 19. RFC to RF2 Isolation at 2GHz and V_{DD} = 3.3V vs TID

5.2 Single-Event Effects Testing

The intense heavy ion environment encountered in space applications can cause a variety of Single-Event Effects (SEE). SEE can lead to system-level performance issues, including disruption, degradation, and destruction. For predictable and reliable space system operation, characterize individual electronic components to determine their SEE response. The following is a summary of the ISL71934M SEE testing.

5.2.1 SEE Test Facility

Testing was performed at Texas A&M University (TAMU Cyclotron Institute heavy ion facility. The overall test setup includes the test jig containing the evaluation cards mounted and wired through 20ft cable to the data room. The input pins RFC, RF1, and RF2 were connected with a series 10µF capacitor to ensure that only AC signals were applied to the ISL71934M. The power and control pins VDD, VCLT, and EN all had a 1µF decoupling capacitor to ground to minimize noise.

5.2.2 SEE Test Setup

For SEB and SEL testing, VDD was set to 5.5V, 5.8V, 6.2V, and 6.8V. The RFC pin was stimulated using a 10MHz signal with a peak amplitude of ±5V (24dBm). The inputs VCLTL and EN were set to 2.5V so that all three RF inputs were open. The supply current through the VDD pin was monitored to look for increases because of radiation.

5.2.3 Single Event Burnout and Latch-Up (SEB/L) Results

No SEB was observed for the device LET of 43MeV·cm^2/mg (+125°C) for V_{DD} = 5.5V, 5.8V, and 6.2V. Runaway currents were observed for 1 DUT at V_{DD} = 6.5V. For V_{DD} = 5.5V, 5.8V, and 6.2V, no current increases were seen outside of ±2%.

5.2.4 SET Results

The SET testing was performed with VCTL = 1.1V (logic 1) and EN = 0V (logic 0). This enables the connection from the RFC to RF1 pins, with minimal margin on the digital control pins. A 10MHz, ±5V peak sine wave was applied to RFC. Both RF1 and RF2 were monitored using an oscilloscope. The oscilloscope was set to trigger on a ±10ns deviation in zero crossings. The part was operated at V_{DD} = 2.7V and 4.5V. The oscilloscope did not trigger on any of the four parts tested, indicating no SET events.

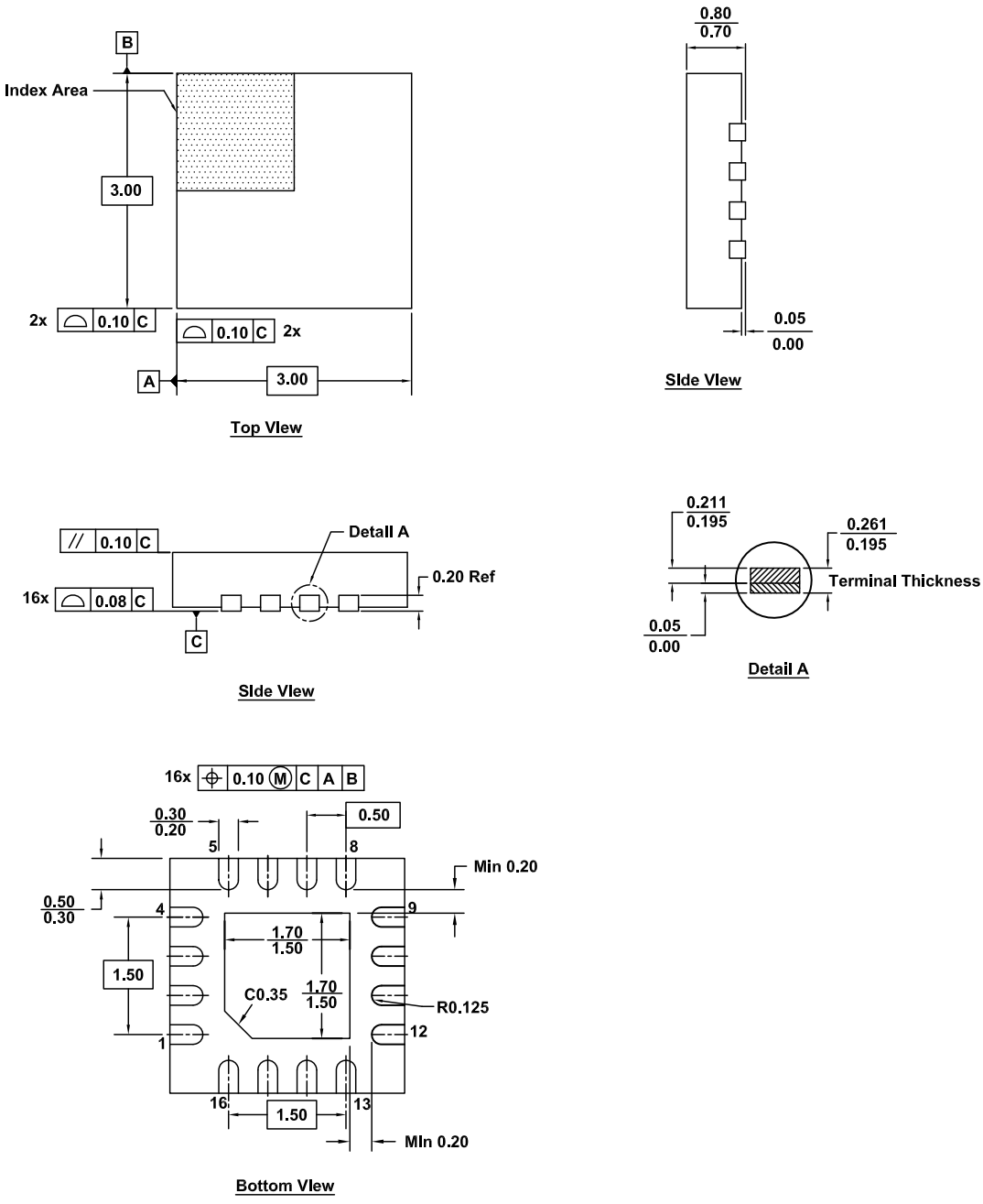
5.2.5 Conclusion

The ISL71934M shows no sensitivity to SEB/L or exhibits any SET for the full supply voltage range, including margin up to V_{DD} = 6.2V under the condition of LET value of 43MeV·cm^2/mg.

6. Package Outline Drawing

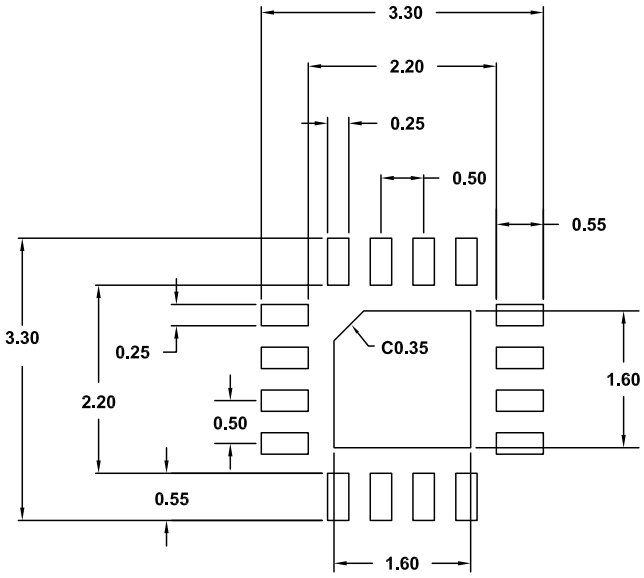
For the most recent package outline drawing, see L16.3x3F.

L16.3x3F
16 Lead Thin Quad Flat No-Lead Package
Rev 0, 2/20



Notes :

1. All dimensions are in mm. Angles are in degrees.
2. Coplanarity applies to the exposed pad and the terminals. Coplanarity shall not exceed 0.05mm.
3. Warpage shall not exceed 0.05mm.
4. The package length and package width are considered as special characteristics.
5. See JEDEC MO-220.



Recommended Land Pattern Dimension

Notes:

1. All dimensions are in mm. Angles are in degrees.
2. Top down view. As viewed on PCB.
3. Land pattern recommendation per IPC-7351B generic requirement for surface mount design and land pattern.

7. Ordering Information

Part Number[1] [2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp. Range
ISL71934MRTZ	71934	16 Ld TQFN	L16.3x3F	Tray	-55 to +125 (°C)
ISL71934MRTZ-T				Reel, 1k	

1. These Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and NiPdAu plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL71934M device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

8. Revision History

Rev.	Date	Description
1.1	Feb 24, 2021	Updated the Ordering Information table and moved it to the end to follow new formatting.
1.0	Dec 4, 2020	Initial release

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