

ISL72026ASEH

3.3V Radiation Tolerant CAN Transceiver with Listen Mode and Loopback

FN8861
Rev. 1.00
Jul 27, 2017

The Intersil [ISL72026ASEH](#) is a radiation tolerant, 3.3V CAN transceivers that is compatible with the ISO11898-2 standard for applications calling for Controller Area Network (CAN) serial communication in satellites and aerospace communications and telemetry data processing in harsh industrial environments.

This device can transmit and receive at bus speeds up to 5Mbps. It can drive a 40m cable at 1Mbps per the ISO11898-2 specification. The device is designed to operate over a common mode range of -7V to +12V, with a maximum of 120 nodes. The device has three discrete selectable driver rise/fall time options, a Listen mode feature, and loopback test capability.

The Receiver (Rx) inputs feature a “full fail-safe” design, which ensures a logic high Rx output if the Rx inputs are floating, shorted, or terminated but undriven.

The ISL72026ASEH is available in an 8 Ld hermetic ceramic flatpack and die form that operate across the temperature range of -55°C to +125°C.

Other CAN transceivers available are the [ISL72027ASEH](#) and [ISL72028ASEH](#). For a list of differences between these devices, see [Table 1 on page 4](#).

Applications

- Satellites and aerospace communications
- Telemetry data processing
- High-end industrial environments and harsh environments

Related Literature

- For a full list of related documents, visit our website
 - [ISL72026ASEH](#) product page

Features

- Electrically screened to SMD [5962-15228](#)
- ESD protection on all pins: 4kV HBM
- Compatible with ISO11898-2
- Operating supply range: 3.0V to 3.6V
- Bus pin fault protection to ±20V
- Undervoltage lockout
- Cold spare: powered down devices/nodes do not affect active devices operating in parallel
- Three selectable driver rise and fall times:
 - Fast speed (RS = 0V) - edges and propagation delays optimized for a data rate of 1Mbps
 - Medium speed (RS = 10kΩ) - edges and propagation delays optimized for a data rate of 500kbps
 - Slow Speed (RS = 50kΩ) - edges and propagation delays optimized for a data rate of 250kbps
- Glitch free bus I/O during power-up and power-down
- Full fail-safe (open, short, terminated/undriven) receiver
- Hi-Z input allows for 120 nodes on the bus
- High data rates: up to 5Mbps
- Quiescent supply current: 7mA (max)
- Listen mode supply current: 2mA (max)
- -7V to +12V common mode input voltage range
- 5V tolerant logic inputs
- Thermal shutdown
- Acceptance tested to 75krad(Si) (LDR) wafer-by-wafer
- Radiation tolerance
 - SEL/B immune to LET_{TH}: 86.4MeV•cm²/mg
 - Low dose rate (0.01rad(Si)/s): 75krad(Si)

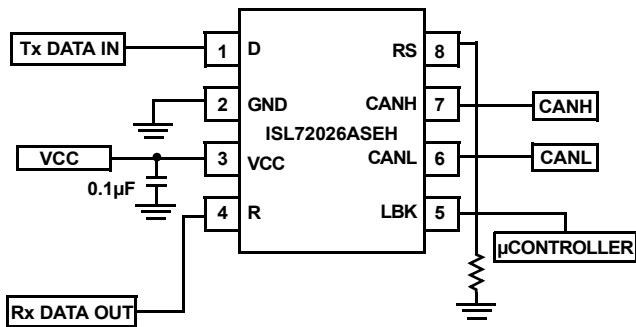


Figure 1. Typical Application

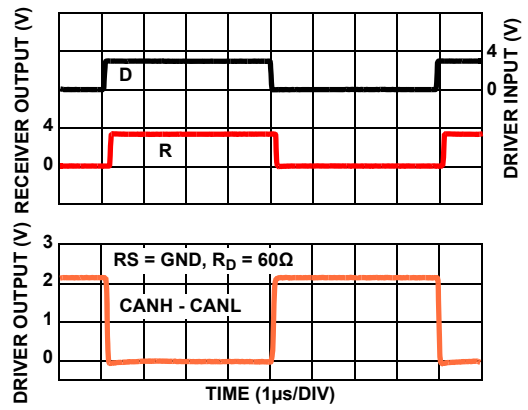


Figure 2. Fast Driver and Receiver Waveforms

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1. Overview

1.1 Ordering Information

Ordering/SMD Number (Note 1)	Part Number (Note 2)	Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing #
5962L1522807VXC	ISL72026ASEHVF	-55 to +125	8 Ld Ceramic Flat Pack	K8.A
N/A	ISL72026ASEHF/PROTO, (Note 3)	-55 to +125	8 Ld Ceramic Flat Pack	K8.A
5962L1522807V9A	ISL72026ASEHVX	-55 to +125	Die	
N/A	ISL72026ASEHX/SAMPLE, (Note 3)	-55 to +125	Die	
N/A	ISL72026ASEHEVAL1Z, (Note 4)	Evaluation Board		

Notes:

- Specifications for Radiation Tolerant QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions over-temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening over-temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because there is no Radiation Assurance testing and they are not DLA qualified devices.
- Evaluation boards utilize the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. ISL7202xSEH Product Family Feature Table

Specification	ISL72026ASEH	ISL72027ASEH	ISL72028ASEH
Loopback Feature	Yes	No	No
VREF Output	No	Yes	Yes
Listen Mode	Yes	Yes	No
Shutdown Mode	No	No	Yes
VTHRLM	900mV (Max)	900mV (Max)	N/A
VTHFLM	325mV (Min)	325mV (Min)	N/A
VHYSLM	40mV (Min)	40mV (Min)	N/A
Supply Current, Listen Mode	2mA (Max)	2mA (Max)	N/A
Supply Current, Shutdown Mode	N/A	N/A	50µA (Max)
VREF Leakage Current	N/A	±25µA (Max)	±25µA (Max)

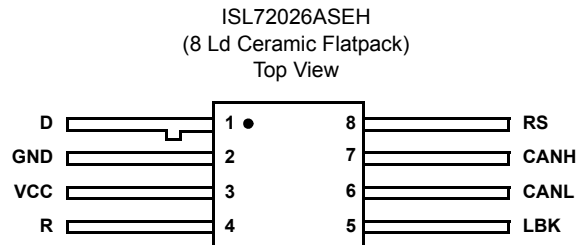
N/A: Not Applicable

Table 2. Product Family Comparison for Optimal Data Rate and Total Dose Radiation Testing

Specification	ISL7202xSEH	ISL7202xASEH	ISL7202xBSEH	ISL7202xCSEH
Data Rate: RS = 0V	1Mbps	1Mbps	1Mbps	1Mbps
Data Rate: RS = 10kΩ	250kbps	500kbps	250kbps	500kbps
Data Rate: RS = 50kΩ	125kbps	250kbps	125kbps	250kbps
High Dose Rate (HDR) - 100krad(Si) Testing	No	No	Yes	Yes
Low Dose Rate (LDR) - 75krad(Si) Testing	Yes	Yes	Yes	Yes

Note: HDR = High Dose Rate, LDR = Low Dose Rate

1.2 Pin Configuration



1.3 Pin Descriptions

Pin Number	Pin Name	Function
1	D	CAN driver digital input. A Low bus state is Dominant and a High bus state is Recessive. Internally tied High.
2	GND	Ground connection.
3	VCC	System power supply input (3.0V to 3.6V). The typical voltage for the device is 3.3V.
4	R	CAN Data Receiver Output. A Low bus state is Dominant and a High bus state is Recessive.
5	LBK	A HIGH on this pin places the CANH and CANL pins in a high impedance state. The rest of the circuit remains active so that the TX and RX can loopback diagnostic information. Internally tied LOW.
6	CANL	CAN bus line for low level output.
7	CANH	CAN bus line for high level output.
8	RS	A resistor to GND from this pin controls the rise and fall time of the CAN output waveform. Drive RS HIGH to put the device into Listen mode.

1.4 Equivalent Input and Output Schematic Diagrams

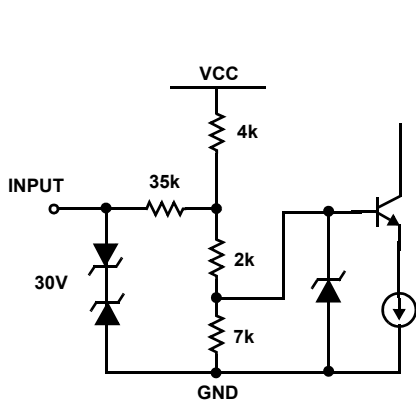


Figure 3. CANH and CANL Inputs

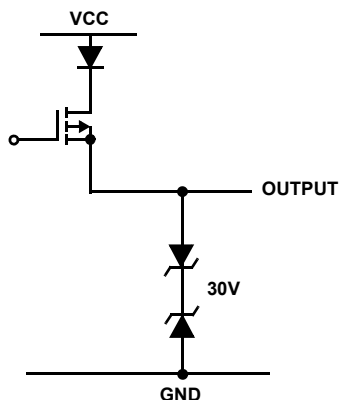


Figure 4. CANH Output

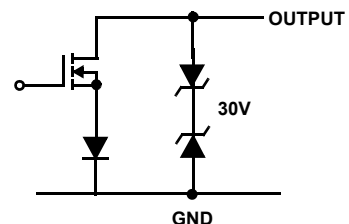


Figure 5. CANL Output

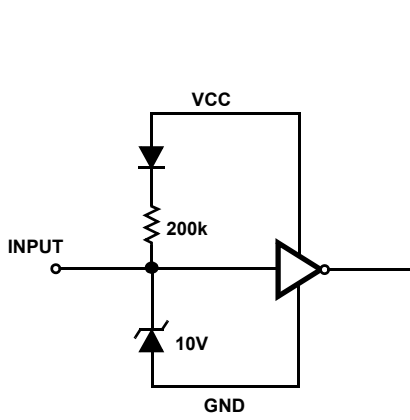


Figure 6. D Input

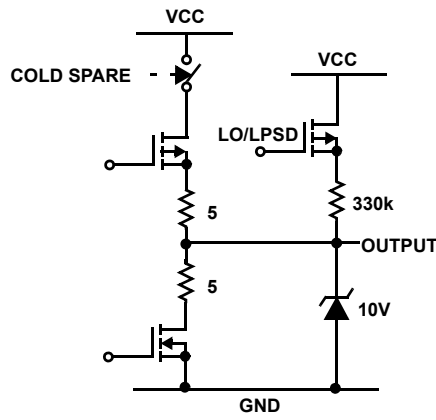


Figure 7. R Output

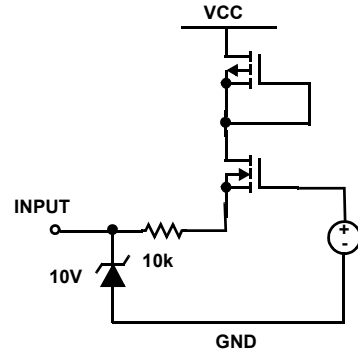


Figure 8. RS Input

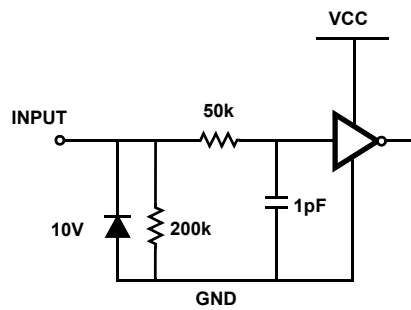


Figure 9. LBK Input

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
VCC to GND With/Without Ion Beam	-0.3	5.5	V
CANH, CANL, VREF Under Ion Beam		±20	V
CANH, CANL, VREF		±20	V
I/O Voltages D, R, RS	-0.5	7	V
Receiver Output Current	-10	10	mA
Output Short-Circuit Duration	Continuous		
ESD Rating	Value		Unit
Human Body Model (Tested per MIL-STD-883 TM3015.7)			
CANH, CANL Bus Pins		4	kV
All Other Pins		4	kV
Charged Device Model (Tested per JS-002-2014)		750	V
Machine Model (Tested per JESD22-A115C)		200	V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

2.2 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld FP Package (Notes 5, 6)	39	7

Notes:

- θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board (two buried 1oz copper planes) with "direct attach" features package base mounted to PCB thermal land with a 10 mil gap fill material having a thermal conductivity of 1W/m-K. Refer to [TB379](#).
- For θ_{JC} , the "case temp" location is the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature Range	-55	+125	°C
V _{CC} Supply Voltage	3.0	3.6	V
Voltage on CAN I/O	-7	12	V
V _{IH} D Logic Pin (D, LBK)	2	5.5	V
V _{IL} D Logic Pin (D, LBK)	0	0.8	V
I _{OH} Driver (CANH - CANL = 1.5V, V _{CC} = 3.3V)		-40	mA
I _{OH} Receiver (V _{OH} = 2.4V)		-4	mA
I _{OL} Driver (CANH - CANL = 1.5V, V _{CC} = 3.3V)		40	mA
I _{OL} Receiver (V _{OL} = 0.4V)		4	mA

2.4 Electrical Specifications

Test Conditions: $V_{CC} = 3.0V$ to $3.6V$. Typical values are at $T_A = +25^\circ C$ (Note 9); unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$ and over a total ionizing dose of $75krad(Si)$ at $+25^\circ C$ with exposure at a low dose rate of $<10mrad(Si)/s$.**

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit	
Driver Electrical Characteristics								
Dominant Bus Output Voltage	$V_{O(DOM)}$	D = 0V, CANH, RS = 0V, Figures 10 and 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	2.25	2.85	V_{CC}	V
		D = 0V, CANL, RS = 0V, Figures 10 and 11		Full	0.10	0.65	1.25	V
Recessive Bus Output Voltage	$V_{O(REC)}$	D = 3V, CANH, RS = 0V, 60Ω and no load, Figures 10 and 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	1.8	2.3	2.7	V
		D = 3V, CANL, RS = 0V, 60Ω and no load, Figures 10 and 11		Full	1.8	2.3	2.8	V
Dominant Output Differential Voltage	$V_{OD(DOM)}$	D = 0V, RS = 0V, $3.0V \leq V_{CC} \leq 3.6V$, Figures 10 and Note 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	1.5	2.2	3.0	V
		D = 0V, RS = 0V, $3.0V \leq V_{CC} \leq 3.6V$, Figures 11 and 12		Full	1.2	2.1	3.0	V
Recessive Output Differential Voltage	$V_{OD(REC)}$	D = 3V, RS = 0V, $3.0V \leq V_{CC} \leq 3.6V$, Figures 10 and 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	-120	0.2	12	mV
		D = 3V, RS = 0V, $3.0V \leq V_{CC} \leq 3.6V$, no load		Full	-500	-34	50	mV
Logic Input High Voltage (D, LBK)	V_{IH}	$3.0V \leq V_{CC} \leq 3.6V$, Note 10	$3.0V \leq V_{CC} \leq 3.6V$	Full	2.0	-	5.5	V
Logic Input Low Voltage (D, LBK)	V_{IL}	$3.0V \leq V_{CC} \leq 3.6V$, Note 10	$3.0V \leq V_{CC} \leq 3.6V$	Full	0	-	0.8	V
Logic High Level Input Current (D, LBK)	I_{IH}	D = 2.0V, $3.0V \leq V_{CC} \leq 3.6V$, Note 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	-30	-3	30	μA
Logic Low Level Input Current (D, LBK)	I_{IL}	D = 0.8V, $3.0V \leq V_{CC} \leq 3.6V$, Note 11	$3.0V \leq V_{CC} \leq 3.6V$	Full	-30	-7	30	μA
RS Input Voltage for Listen Mode	$V_{IN(RS)}$	$3.0V \leq V_{CC} \leq 3.6V$	$3.0V \leq V_{CC} \leq 3.6V$	Full	0.75 V_{CC}	1.9	5.5	V
Output Short-Circuit Current	I_{OSC}	$V_{CANH} = -7V$, CANL = OPEN, $3.0V \leq V_{CC} \leq 3.6V$, Figure 25	$3.0V \leq V_{CC} \leq 3.6V$	Full	-250	-100	-	mA
		$V_{CANH} = +12V$, CANL = OPEN, $3.0V \leq V_{CC} \leq 3.6V$, Figure 25	$3.0V \leq V_{CC} \leq 3.6V$	Full	-	0.4	1	mA
		$V_{CANL} = -7V$, CANH = OPEN, $3.0V \leq V_{CC} \leq 3.6V$, Figure 25	$3.0V \leq V_{CC} \leq 3.6V$	Full	-1	-0.4	-	mA
		$V_{CANL} = +12V$, CANH = OPEN, $3.0V \leq V_{CC} \leq 3.6V$, Figure 25	$3.0V \leq V_{CC} \leq 3.6V$	Full	-	100	250	mA
Thermal Shutdown Temperature	T_{SHDN}	$3.0V < V_{IN} < 3.6V$	$3.0V < V_{IN} < 3.6V$	-	-	163	-	°C
Thermal Shutdown Hysteresis	T_{HYS}	$3.0V < V_{IN} < 3.6V$	$3.0V < V_{IN} < 3.6V$	-	-	12	-	°C

Test Conditions: $V_{CC} = 3.0V$ to $3.6V$. Typical values are at $T_A = +25^\circ C$ (Note 9); unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$ and over a total ionizing dose of $75krad(Si)$ at $+25^\circ C$ with exposure at a low dose rate of $<10mrad(Si)/s$.** (Continued)

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
Receiver Electrical Characteristics							
Input Threshold Voltage (Rising)	V_{THR}	LBK = 0V, RS = 0V, 10k, 50k, (recessive to dominant), Figure 17 and Table 3	Full	-	700	900	mV
Input Threshold Voltage (Falling)	V_{THF}	LBK = 0V, RS = 0V, 10k, 50k, (dominant to recessive), Figure 17 and Table 3	Full	500	625	-	mV
Input Hysteresis	V_{HYS}	$(V_{THR} - V_{THF})$, RS = 0V, 10k, 50k, Figure 17 and Table 3	Full	40	80	-	mV
Listen Mode Input Threshold Voltage (Rising)	V_{THRLM}	RS = V_{CC} , (recessive to dominant), Figure 17	Full	-	650	900	mV
Listen Mode Input Threshold Voltage (Falling)	V_{THFLM}	RS = V_{CC} , (dominant to recessive), Figure 17	Full	325	550	-	mV
Listen Mode Input Hysteresis	V_{HYSLM}	$(V_{THR} - V_{THF})$, RS = V_{CC} , Figure 17	Full	40	100	-	mV
Receiver Output High Voltage	V_{OH}	$I_O = -4mA$	Full	2.4	$V_{CC} - 0.2$	-	V
Receiver Output Low Voltage	V_{OL}	$I_O = +4mA$	Full	-	0.2	0.4	V
Input Current for CAN Bus	I_{CAN}	CANH or CANL at 12V, D = 3V, other bus pin at 0V, LBK = RS = 0V	Full	-	470	600	μA
		CANH or CANL at 12V, D = 3V, $V_{CC} = 0V$, other bus pin at 0V, LBK = RS = 0V	Full	-	170	275	μA
		CANH or CANL at -7V, D = 3V, other bus pin at 0V, LBK = RS = 0V	Full	-500	-350	-	μA
		CANH or CANL at -7V, D = 3V, $V_{CC} = 0V$, other bus pin at 0V, LBK = RS = 0V	Full	-175	-100	-	μA
Input Capacitance (CANH or CANL)	C_{IN}	Input to GND, D = 3V, LBK = RS = 0V	25	-	35	-	pF
Differential Input Capacitance	C_{IND}	Input to Input, D = 3V, LBK = RS = 0V	25	-	15	-	pF
Input Resistance (CANH or CANL)	R_{IN}	Input to GND, D = 3V, LBK = RS = 0V	Full	20	40	50	k Ω
Differential Input Resistance	R_{IND}	Input to Input, D = 3V, LBK = RS = 0V	Full	40	80	100	k Ω
Supply Current							
Supply Current, Listen Mode	$I_{CC(L)}$	RS = D = V_{CC} , LBK = 0V, $3.0V \leq V_{CC} \leq 3.6V$	Full	-	1	2.0	mA
Supply Current, Dominant	$I_{CC(DOM)}$	D = LBK = RS = 0V, no load, $3.0V \leq V_{CC} \leq 3.6V$	Full	-	5	7.0	mA
Supply Current, Recessive	$I_{CC(REC)}$	D = V_{CC} , LBK = RS = 0V, no load, $3.0V \leq V_{CC} \leq 3.6V$	Full	-	2.6	5.0	mA
Cold Sparing Bus Current							
CANH Leakage Current	$I_{L(CANH)}$	$V_{CC} = 0.2V$, CANH = -7V or 12V, CANL = float, D = V_{CC} , RS = 0V	Full	-25	-4	25	μA
CANL Leakage Current	$I_{L(CANL)}$	$V_{CC} = 0.2V$, CANL = -7V or 12V, CANH = float, D = V_{CC} , RS = 0V	Full	-25	-4	25	μA

Test Conditions: $V_{CC} = 3.0V$ to $3.6V$. Typical values are at $T_A = +25^\circ C$ (Note 9); unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, $-55^\circ C$ to $+125^\circ C$ and over a total ionizing dose of $75krad(Si)$ at $+25^\circ C$ with exposure at a low dose rate of $<10mrad(Si)/s$.** (Continued)

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
Driver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PDLH1}	RS = 0V, Figure 14	Full	-	90	160	ns
Propagation Delay LOW to HIGH	t_{PDLH2}	RS = 10k Ω , Figure 14	Full	-	350	550	ns
Propagation Delay LOW to HIGH	t_{PDLH3}	RS = 50k Ω , Figure 14	Full	-	475	800	ns
Propagation Delay HIGH to LOW	t_{PDHL1}	RS = 0V, Figure 14	Full	-	115	180	ns
Propagation Delay HIGH to LOW	t_{PDHL2}	RS = 10k Ω , Figure 14	Full	-	410	600	ns
Propagation Delay HIGH to LOW	t_{PDHL3}	RS = 50k Ω , Figure 14	Full	-	550	900	ns
Output Skew	t_{SKEW1}	RS = 0V, ($ t_{PHL} - t_{PLH} $), Figure 14	Full	-	20	65	ns
Output Skew	t_{SKEW2}	RS = 10k Ω , ($ t_{PHL} - t_{PLH} $), Figure 14	Full	-	60	275	ns
Output Skew	t_{SKEW3}	RS = 50k Ω , ($ t_{PHL} - t_{PLH} $), Figure 14	Full	-	75	400	ns
Output Rise Time	t_{r1}	RS = 0V, (fast speed - 1Mbps), Figure 14	Full	15	30	85	ns
Output Fall Time	t_{f1}		Full	10	20	65	ns
Output Rise Time	t_{r2}	RS = 10k Ω , (medium speed - 500kbps), Figure 14	Full	125	250	550	ns
Output Fall Time	t_{f2}		Full	100	250	425	ns
Output Rise Time	t_{r3}	RS = 50k Ω , (slow speed - 250kbps), Figure 14	Full	200	360	800	ns
Output Fall Time	t_{f3}		Full	175	390	600	ns
Total Loop Delay, Driver Input to Receiver Output, Recessive to Dominant	$t_{(LOOP1)}$	RS = 0V, Figure 21	Full	-	140	225	ns
		RS = 10k Ω , Figure 21	Full	-	380	600	ns
		RS = 50k Ω , Figure 21	Full	-	500	800	ns
Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive	$t_{(LOOP2)}$	RS = 0V, Figure 21	Full	-	160	285	ns
		RS = 10k Ω , Figure 21	Full	-	450	700	ns
		RS = 50k Ω , Figure 21	Full	-	575	950	ns
Listen to Valid Dominant Time	t_{L-DOM}	Figure 19	Full	-	5	15	μs
Receiver Switching Characteristics							
Propagation Delay LOW to HIGH	t_{PLH}	Figure 17	Full	-	50	110	ns
Propagation Delay HIGH to LOW	t_{PHL}	Figure 17	Full	-	50	110	ns
Rx Skew	t_{SKEW1}	$ t_{PHL} - t_{PLH} $, Figure 17	Full	-	2	35	ns
Rx Rise Time	t_r	Figure 17	Full	-	2	-	ns
Rx Fall Time	t_f	Figure 17	Full	-	2	-	ns
LBK Delay I/O to Rx Output	t_{LBK}	Figure 23 , Note 11	Full	-	40	90	ns

Test Conditions: $V_{CC} = 3.0V$ to $3.6V$. Typical values are at $T_A = +25^{\circ}C$ (Note 9); unless otherwise specified (Note 7). **Boldface limits apply across the operating temperature range, $-55^{\circ}C$ to $+125^{\circ}C$ and over a total ionizing dose of $75krad(Si)$ at $+25^{\circ}C$ with exposure at a low dose rate of $<10mrad(Si)/s$.** (Continued)

Parameter	Symbol	Test Conditions	Temp (°C)	Min (Note 8)	Typ (Note 9)	Max (Note 8)	Unit
RS Pin Characteristics							
RS Input Current	$I_{RS(H)}$	$R_S = 0.75 \times V_{CC}$	Full	-10	-0.2	-	μA
	$I_{RS(L)}$	$V_{RS} = 0V$	Full	-450	-125	0	μA

Notes:

- All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to device ground unless otherwise specified.
- Parameters with MIN and/or MAX limits are 100% tested at $-55^{\circ}C$, $+25^{\circ}C$, and $+125^{\circ}C$, unless otherwise specified.
- Typical values are at $3.3V$. Parameters with a single entry in the "TYP" column apply to $3.3V$. Typical values shown are not guaranteed.
- Parameter included in functional testing.
- Performed during the 100% screening operations over the full operating temperature range. Not performed as part of TCI Group E and Group C. Radiation characterization testing performed as part of the initial release and any major changes in design.

2.5 Test Circuits and Waveforms

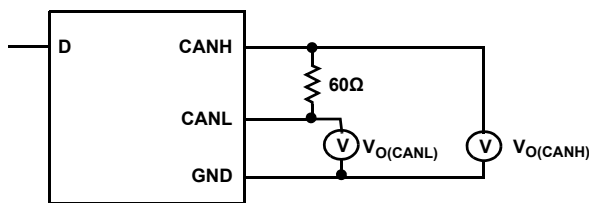


Figure 10. Driver Test Circuit

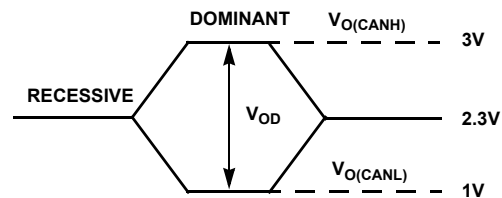


Figure 11. Driver Bus Voltage Definitions

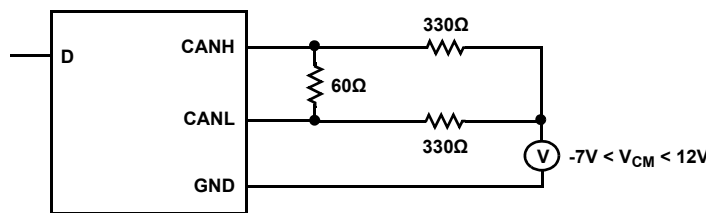
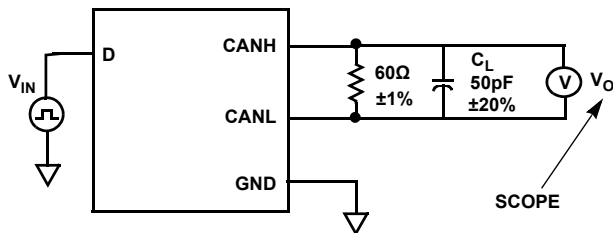


Figure 12. Driver Common Mode Circuit



$V_{IN} = 125kHz$, $0V$ TO V_{CC} , DUTY CYCLE 50%, $t_r = t_f \leq 6ns$, $Z_O = 50\Omega$
 C_L INCLUDES FIXTURE AND INSTRUMENTATION CAPACITANCE

Figure 13. Driver Timing Test Circuit

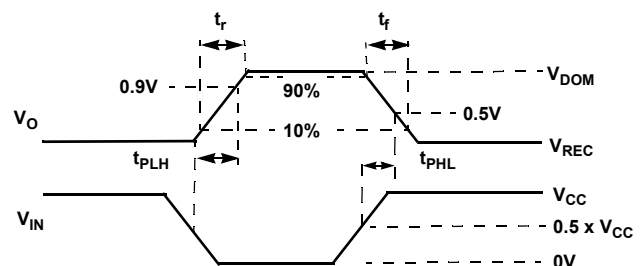


Figure 14. Driver Timing Measurement Points

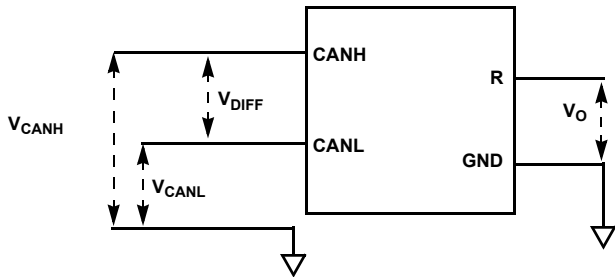


Figure 15. Receiver Voltage Definitions

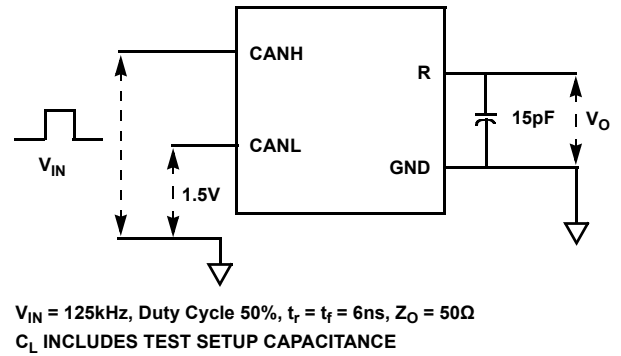


Figure 16. Receiver Test Circuit

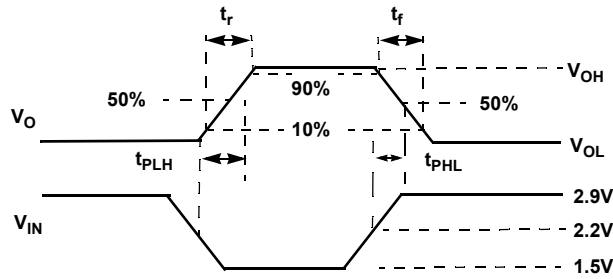
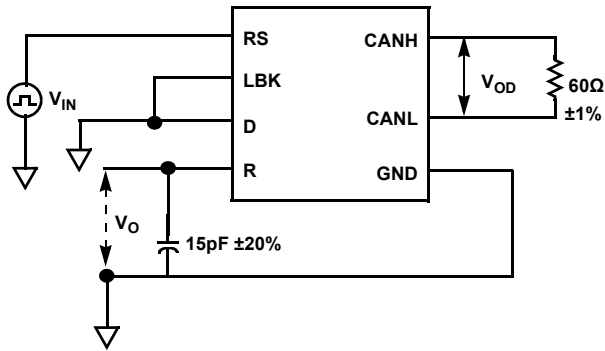


Figure 17. Receiver Test Measurement Points

Table 3. Differential Input Voltage Threshold Test

Input		Output	Measured
VCANH	VCANL	R	VDIFF
-6.1V	-7V	L	900mV
12V	11.1V	L	900mV
-1V	-7V	L	6V
12V	6V	L	6V
-6.5V	-7V	H	500mV
12V	11.5V	H	500mV
-7V	-1V	H	6V
6V	12V	H	6V
Open	Open	H	X



$V_{IN} = 125\text{kHz}$, $0\text{V TO } V_{CC}$, DUTY CYCLE 50%, $t_r = t_f \leq 6\text{ns}$

Figure 18. Listen to Valid Dominant Time Test Circuit

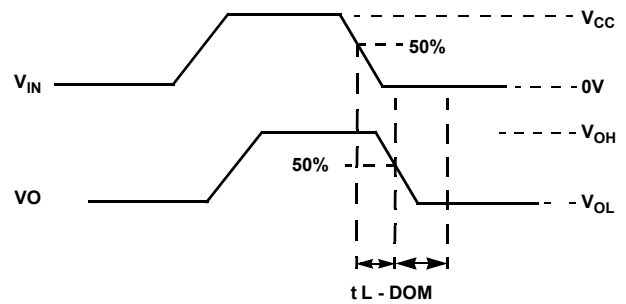
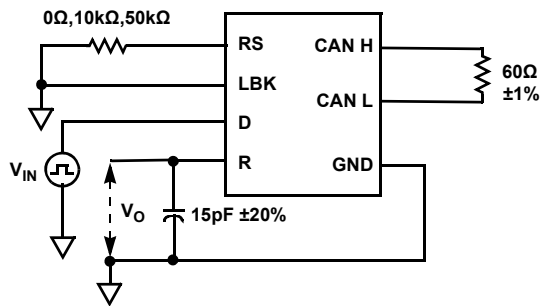


Figure 19. Listen to Valid Dominant Time Measurement Points



$V_{IN} = 125\text{kHz}$, DUTY CYCLE 50%, $t_r = t_f \leq 6\text{ns}$.

Figure 20. Total Loop Delay Test Circuit

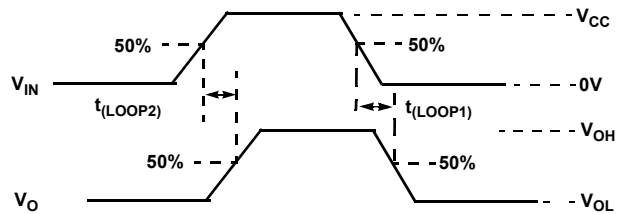
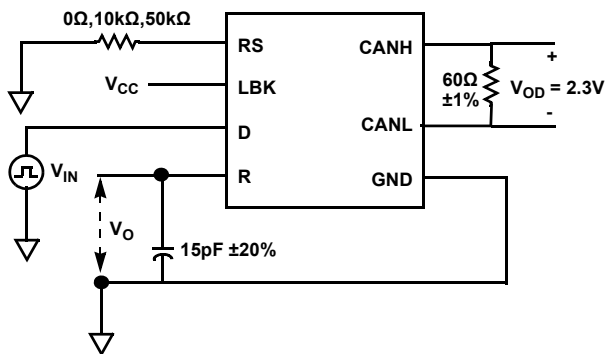


Figure 21. Total Loop Delay Measurement Points



$V_{IN} = 125\text{kHz}$, $0\text{V TO } V_{CC}$, DUTY CYCLE 50%, $t_r = t_f \leq 6\text{ns}$

Figure 22. Loop Back Delay to Dominant Time Test Circuit

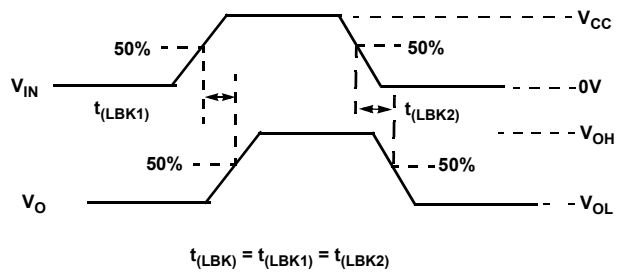


Figure 23. Loop Back Delay to Dominant Measurement Points

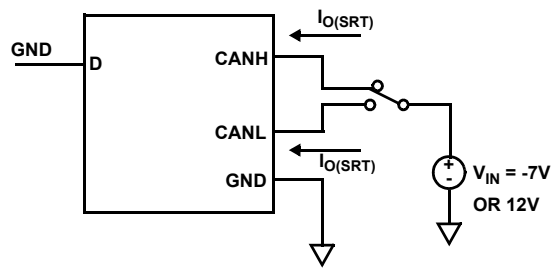


Figure 24. Output Short-Circuit Current Test Circuit

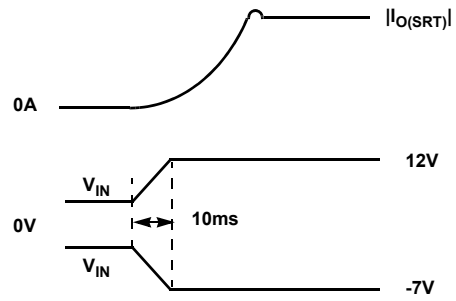


Figure 25. Output Short-Circuit Current Waveforms

3. Typical Performance Curves

CL = 15pF, TA = +25°C; unless otherwise specified.

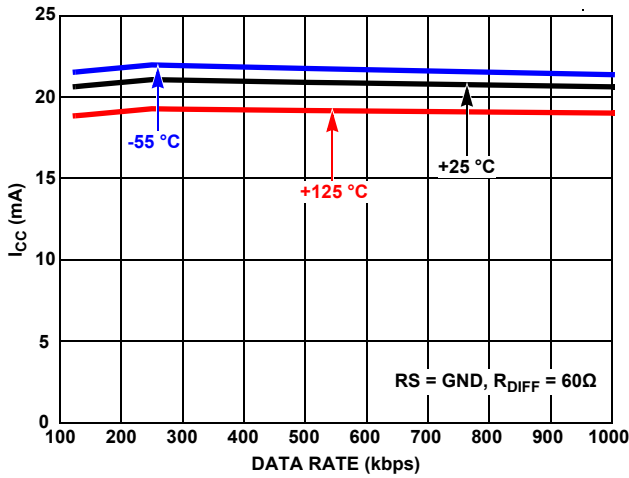


Figure 26. Supply Current vs Fast Data Rate vs Temperature

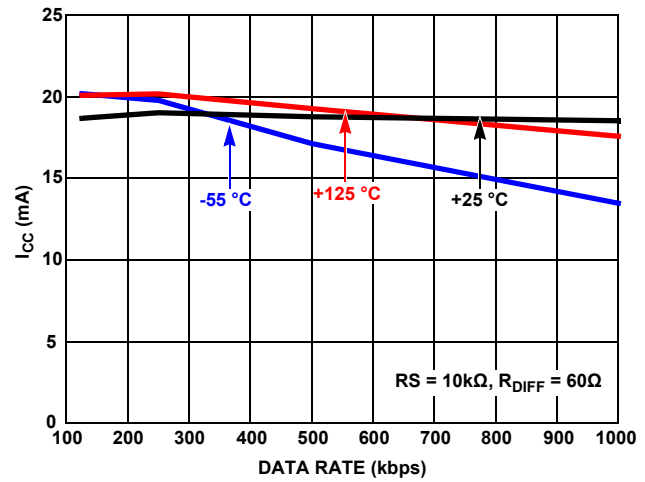


Figure 27. Supply Current vs Medium Data Rate vs Temperature

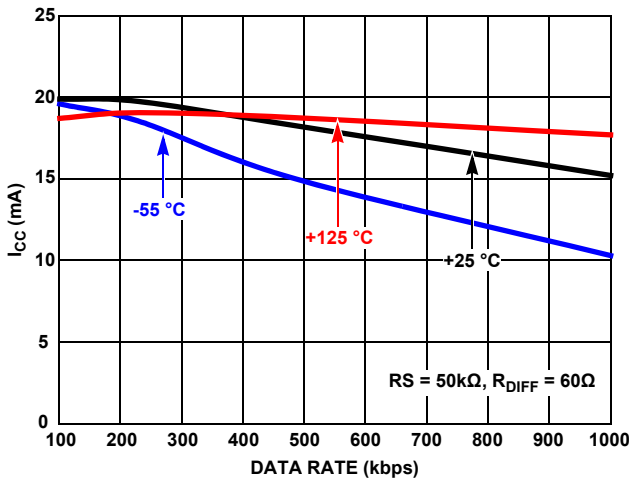


Figure 28. Supply Current vs Slow Data Rate vs Temperature

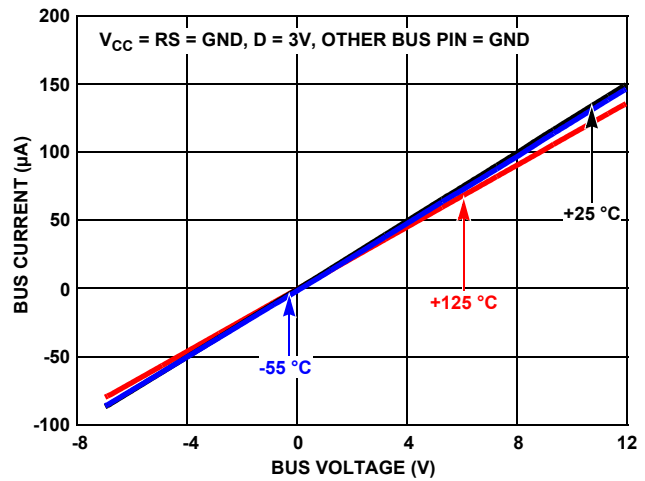


Figure 29. Bus Pin Leakage vs V_{CM} at $V_{CC} = 0V$

CL = 15pF, TA = +25°C; unless otherwise specified. (Continued)

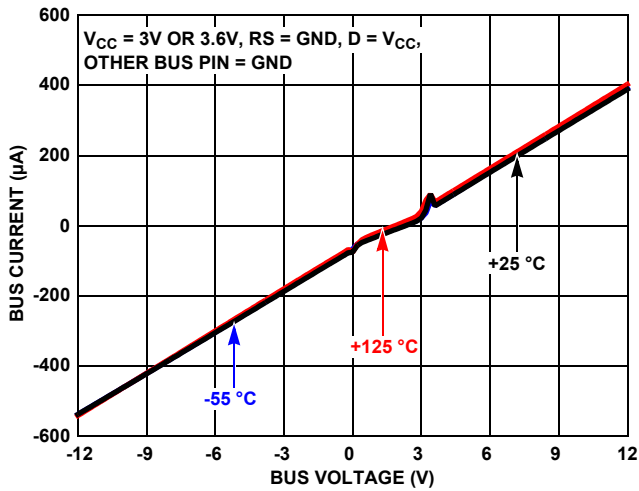


Figure 30. Bus Pin Leakage vs $\pm 12V V_{CM}$

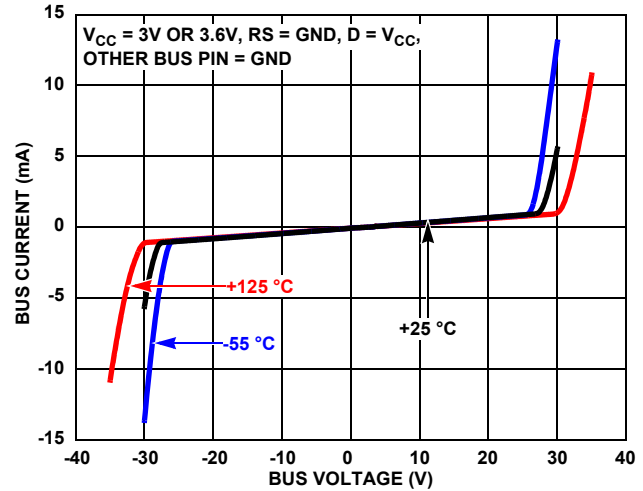


Figure 31. Bus Pin Leakage vs $\pm 35V V_{CM}$

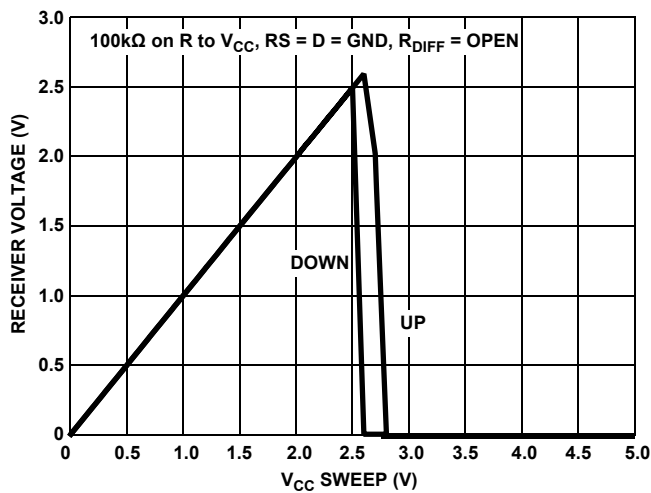


Figure 32. V_{CC} Undervoltage Lockout

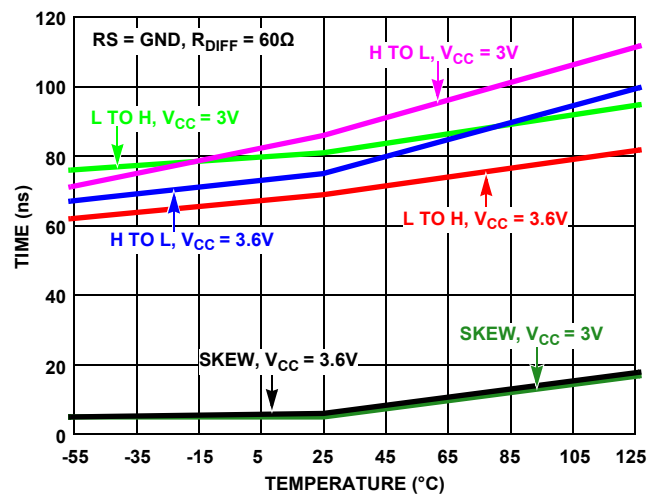


Figure 33. Transmitter Propagation Delay and Skew vs Temperature at Fast Speed

CL = 15pF, TA = +25°C; unless otherwise specified. (Continued)

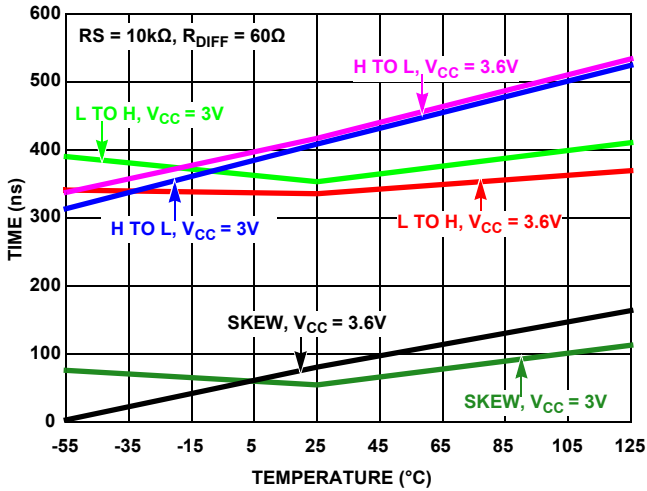


Figure 34. Transmitter Propagation Delay and Skew vs Temperature at Medium Speed

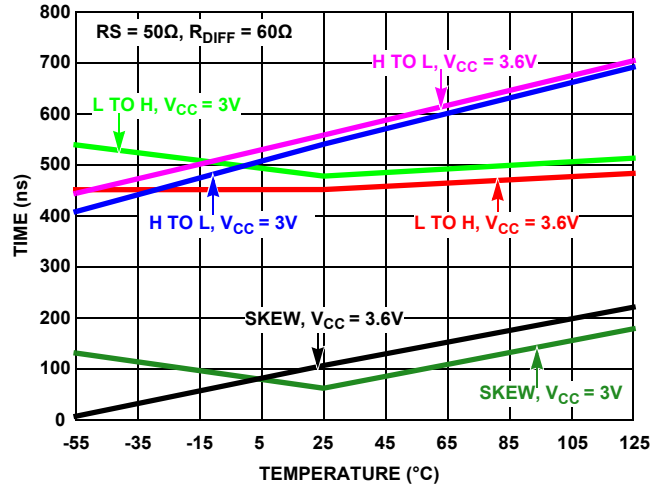


Figure 35. Transmitter Propagation Delay and Skew vs Temperature at Slow Speed

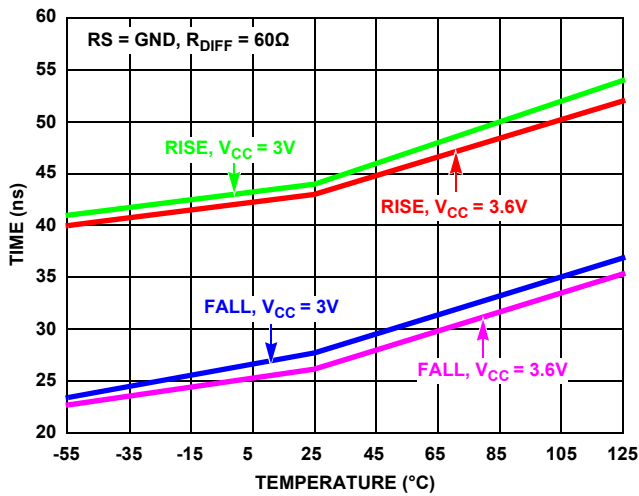


Figure 36. Transmitter Rise and Fall Times vs Temperature at Fast Speed

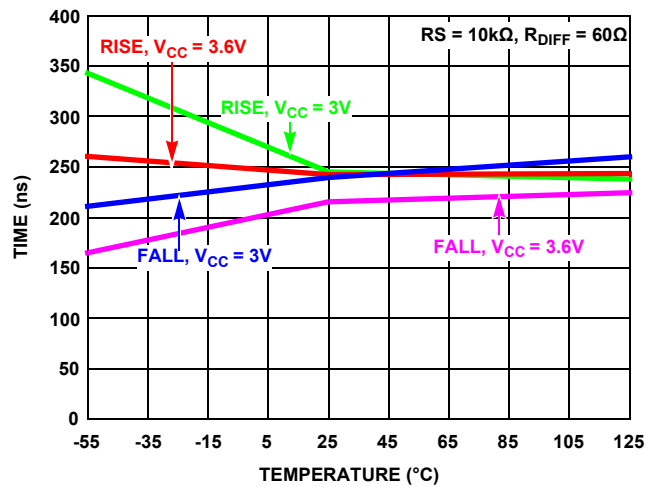


Figure 37. Transmitter Rise and Fall Times vs Temperature at Medium Speed

CL = 15pF, TA = +25°C; unless otherwise specified. (Continued)

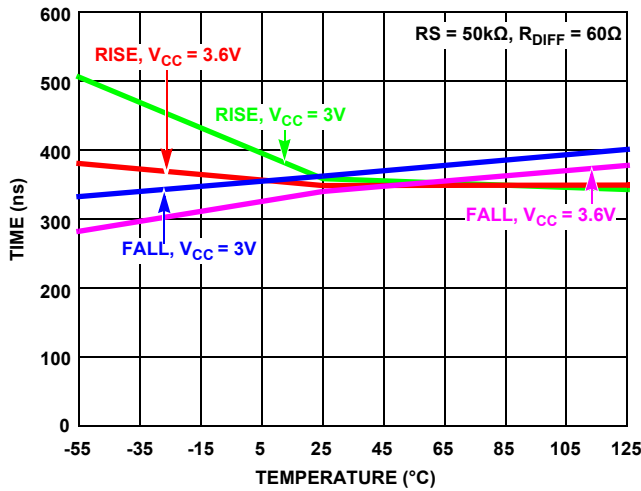


Figure 38. Transmitter Rise and Fall Times vs Temperature at Slow Speed

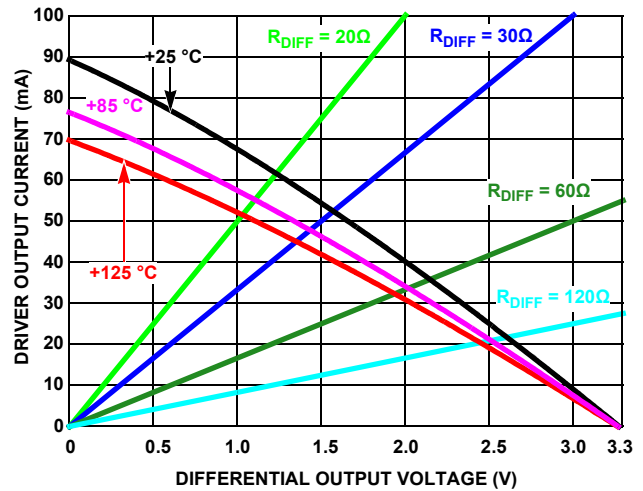


Figure 39. Driver Output Current vs Differential Output Voltage

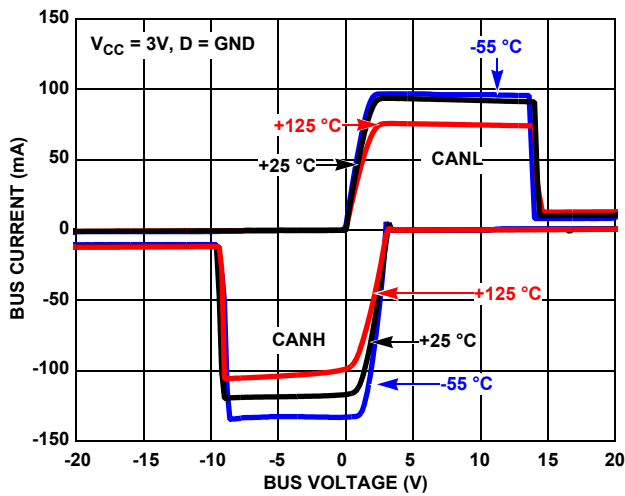


Figure 40. Driver Output Current vs Short-Circuit Voltage vs Temperature

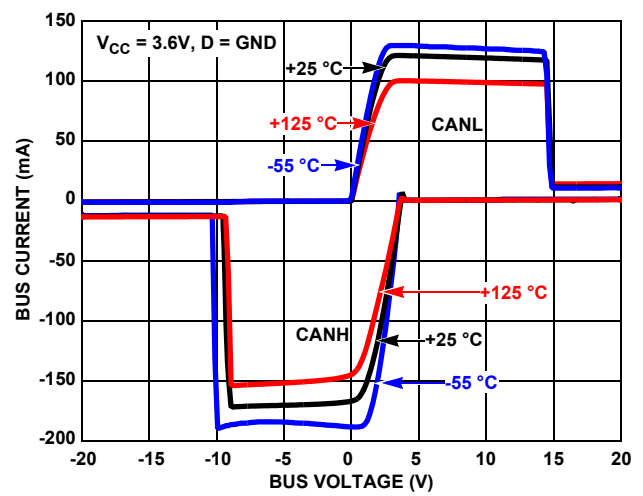


Figure 41. Driver Output Current vs Short-Circuit Voltage vs Temperature

CL = 15pF, TA = +25°C; unless otherwise specified. (Continued)

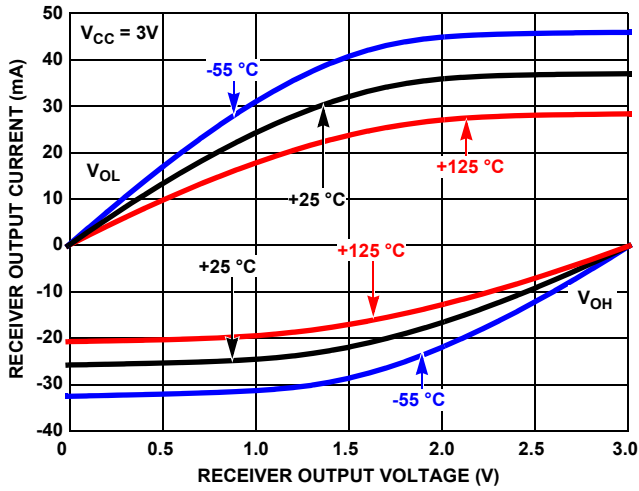


Figure 42. Receiver Output Current vs Receiver Output Voltage at $V_{CC} = 3V$

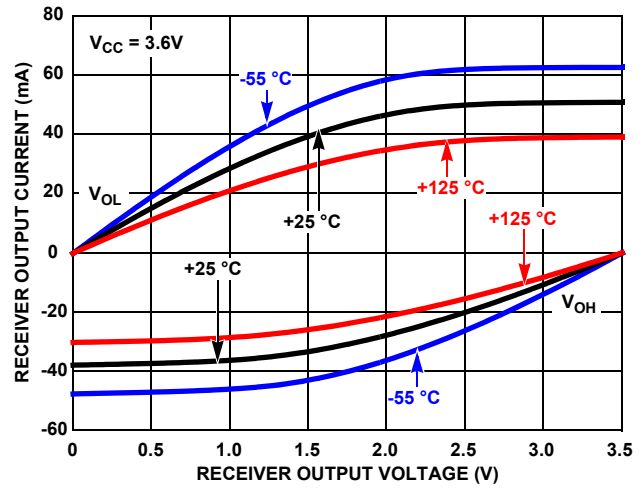


Figure 43. Receiver Output Current vs Receiver Output Voltage at $V_{CC} = 3.6V$

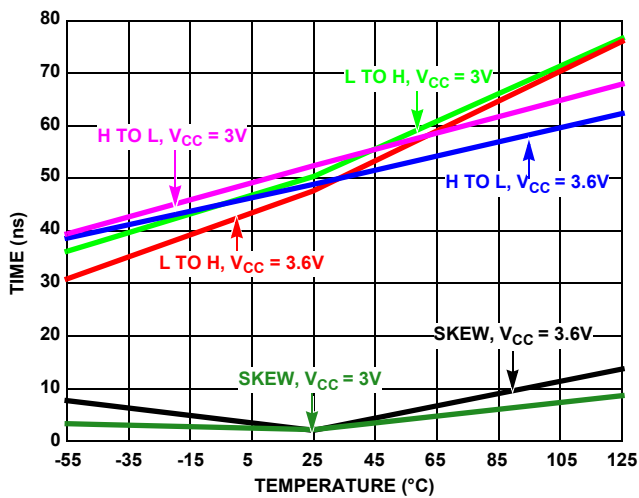


Figure 44. Receiver Propagation Delay and Skew vs Temperature

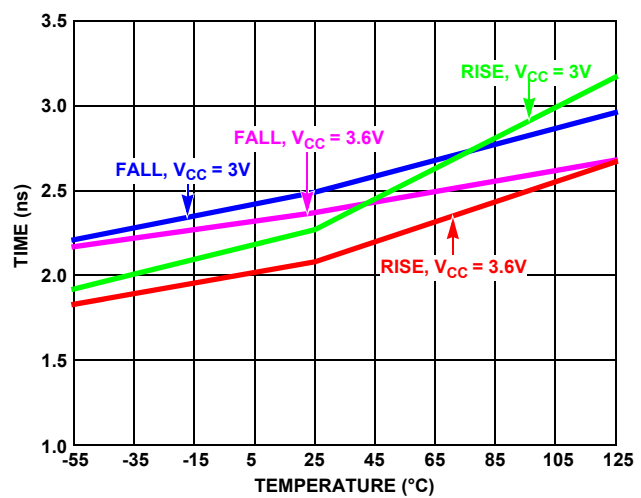


Figure 45. Receiver Rise and Fall Times vs Temperature

CL = 15pF, TA = +25°C; unless otherwise specified. (Continued)

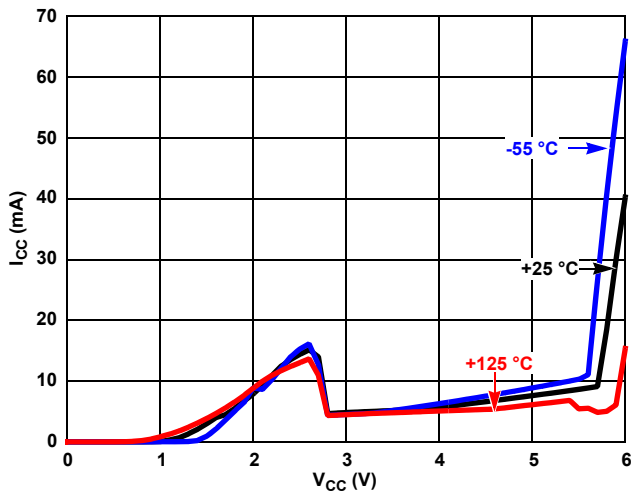


Figure 46. Supply Current vs Supply Voltage vs Temperature

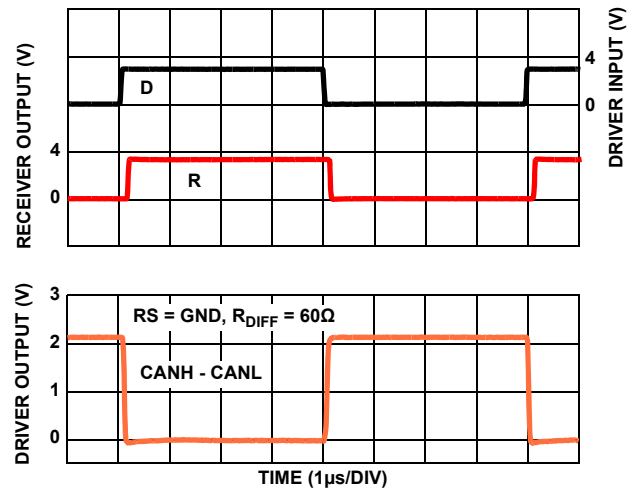


Figure 47. Fast Driver and Receiver Waveforms

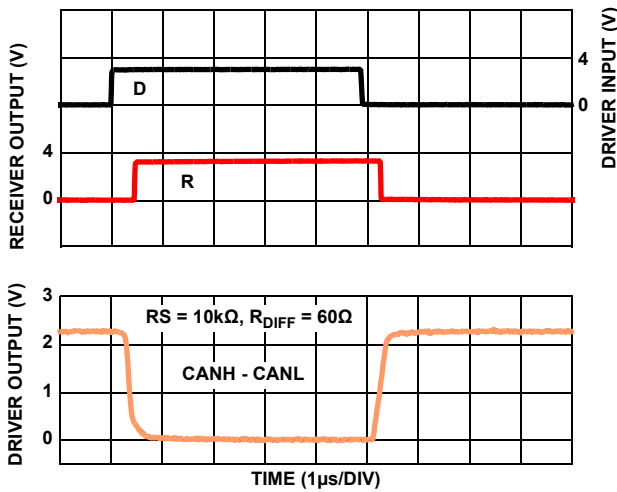


Figure 48. Medium Driver and Receiver Waveforms

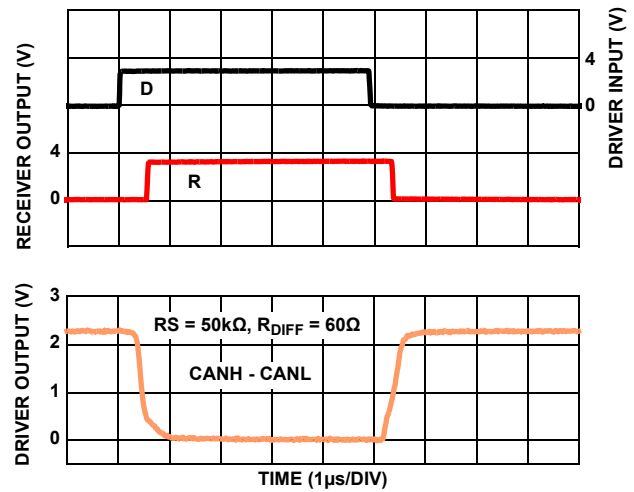


Figure 49. Slow Driver and Receiver Waveforms

4. Functional Description

4.1 Overview

The Intersil ISL72026ASEH is a 3.3V radiation tolerant CAN transceiver that is compatible with the ISO11898-2 standard for use in Controller Area Network (CAN) serial communication systems.

The device performs transmit and receive functions between the CAN controller and the CAN differential bus. It can transmit and receive at bus speeds up to 5Mbps. It is designed to operate across a common-mode range of -7V to +12V, with a maximum of 120 nodes. The device is capable of withstanding $\pm 20V$ on the CANH and CANL bus pins outside of ion beam and $\pm 16V$ under ion beam.

4.2 Slope Adjustment

The transceiver driver has three programmable rise/fall time options programmed by the resistor value connected from the RS pin to GND. A 0Ω resistor sets the part in Fast Speed Mode. A resistor of $10k\Omega$ sets the part in Medium Speed Mode. A resistor of $50k\Omega$ puts the part in Slow Speed Mode. Putting a high logic level on the RS pin places the part in Listen mode. Refer to [“Listen Mode” on page 22](#) for more information.

4.2.1 Fast Speed Mode

Connecting the RS pin directly to GND (0Ω resistor) results in the fastest driver output switching times, limited only by the drive capability of the output state. In Fast Speed mode ($RS = 0V$), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 1Mbps.

4.2.2 Medium Speed Mode

In Medium Speed mode ($RS = 10k\Omega$), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 500kbps. $RS = 10k\Omega$ provides for a typical slew rate of $12V/\mu s$. The slower edges in Medium Speed mode at 500kbps provide better EMI results than running at 500kbps in Fast Speed mode.

4.2.3 Slow Speed Mode

In Slow Speed mode ($RS = 50k\Omega$), the rise/fall times, propagation delays, and total loop delays are optimized for a data rate of 250kbps. $RS = 50k\Omega$ provides for a typical slew rate of $8V/\mu s$. The slower edges in Slow Speed mode at 250kbps provide better EMI results than running at 250kbps in Medium Speed mode.

4.3 Cable Length

The device can operate according to the ISO11898 specification with a 40m cable and stub length of 0.3m and 60 nodes at 1Mbps. These specifications are greater than the ISO requirement of 30 nodes. The cable type specified is twisted pair (shielded or unshielded) with a characteristic impedance of 120Ω . Resistors equal to this impedance must be terminated at both ends of the cable. Keep stubs as short as possible to prevent reflections.

4.4 Cold Spare

To reduce the risk of a single-point failure, use redundant bus transceivers in parallel. In this arrangement, both active and quiescent devices can be present simultaneously on the bus. The quiescent devices are powered down as cold spares and do not affect the communication of the other active nodes.

The powered down transceiver ($V_{CC} < 200mV$) has a resistance between the CANH or CANL bus pin to the V_{CC} supply rail of $>480k\Omega$ (max) with a typical resistance $>2M\Omega$. The resistance between CANH and CANL of a powered-down transceiver is typically $80k\Omega$. The receiver output (R pin) of a powered-down transceiver ($V_{CC} < 200mV$) is internally connected to ground. Therefore, the receiver outputs of an active transceiver and a cold spare transceiver cannot be connected together in the redundant application.

4.5 Listen Mode

When a high level is applied to the RS pin, the device enters Low Power Listen mode. The driver of the transceiver is switched off to conserve power while the receiver remains active. In Listen mode, the transceiver draws 2mA (max) of current.

A low level on the RS pin brings the device back to normal operation.

4.6 Loopback Mode

When a high level is applied to the LBK pin, the device enters the loopback state. The transceiver CANH and CANL pins are disconnected from the bus. The driver and receiver circuitry of the transceiver remains active to allow for diagnostic testing of the node.

4.7 Using 3.3V Devices in 5V Systems

The differential voltages and common-mode outputs are the same for both the 3.3V and 5V devices. The dominant common-mode output voltage for the 3.3V device is slightly lower than that of the 5V counterparts. The receiver specifications for both devices are also the same. Although the electrical parameters appear compatible, perform necessary system testing to verify interchangeable operation.

5. Die Characteristics

Table 4. Die and Assembly Related Information

Die Information	
Dimensions	2413 μ m x 3322 μ m (95 mils x 130.79 mils) Thickness: 305 μ m \pm 25 μ m (12 mils \pm 1 mil)
Interface Materials	
Glassivation	Type: 12k Å Silicon Nitride on 3k Å Oxide
Top Metallization	Type: 300 Å TiN on 2.8 μ m AlCu In Bondpads, TiN has been removed.
Backside Finish	Silicon
Process	P6SOI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	1.6 x 10 ⁵ A/cm ²
Transistor Count	4055
Weight of Packaged Device	0.31 grams
Lid Characteristics	Finish: Gold Potential: Grounded, tied to package Pin 2

5.1 Metallization Mask Layout

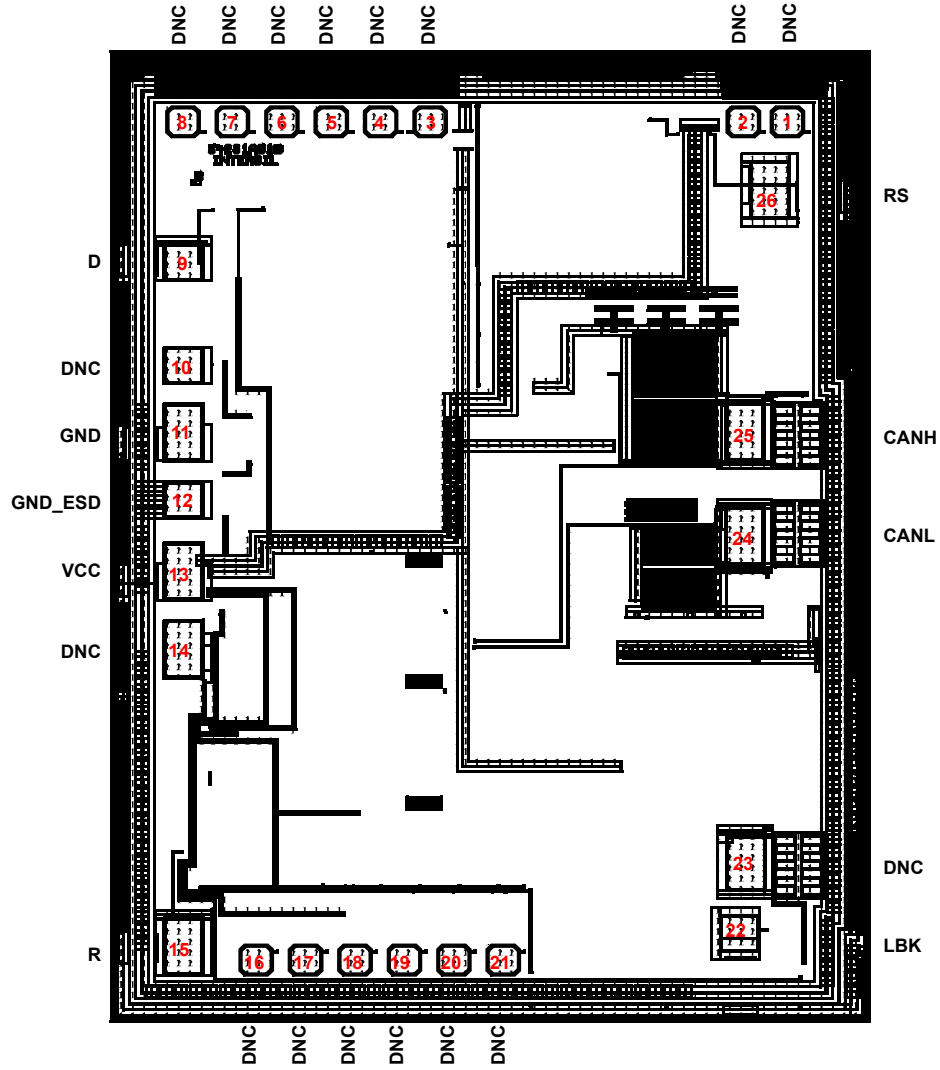


Table 5. ISL72026ASEH Die Layout X-Y Coordinates

Pad Number	Pad Name	X (μm)	Y (μm)	X	Y
1	DNC	90.0	90.0	901.4	1365.6
2	DNC	90.0	90.0	767.4	1365.6
3	DNC	90.0	90.0	-183.23	1365.6
4	DNC	90.0	90.0	-333.25	1365.6
5	DNC	90.0	90.0	-483.25	1365.6
6	DNC	90.0	90.0	-633.25	1365.6
7	DNC	90.0	90.0	-783.25	1365.6
8	DNC	90.0	90.0	-933.25	1365.6
9	D	110.0	110.0	-931.1	901.85
10	DNC	110.0	110.0	-931.1	563.25
11	GND	110.0	180.0	-931.1	342.25
12	GND_ESD	110.0	110.05	-931.1	119.42
13	VCC	110.0	180.0	-931.1	-115.05
14	DNC	110.0	180.05	-931.1	-371.08
15	R	110.0	180.0	-931.1	-1350.0
16	DNC	90.0	90.0	-711.1	-1394.95
17	DNC	90.0	90.0	-561.1	-1394.95
18	DNC	90.0	90.0	-411.1	-1394.95
19	DNC	90.0	90.0	-261.1	-1394.95
20	DNC	90.0	90.0	-111.1	-1394.95
21	DNC	90.0	90.0	38.9	-1394.95
22	LBK	110.0	110.0	756.9	-1307.3
23	DNC	110.0	180.0	775.3	-1072.3
24	CANL	110.0	180.0	772.1	2.15
25	CANH	110.0	180.05	772.1	343.33
26	RS	110.0	180.0	848.1	1140.6

Note: Origin of coordinates is the center of the die. DNC - Do Not Connect

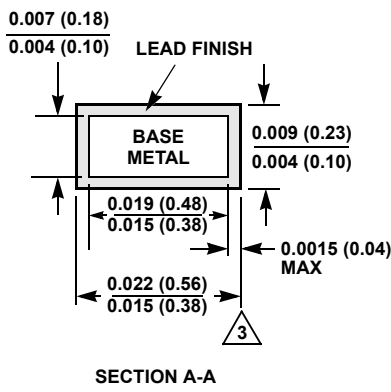
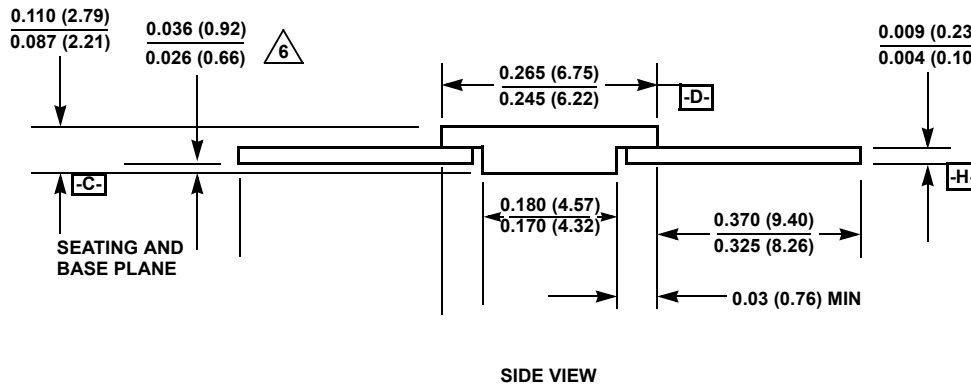
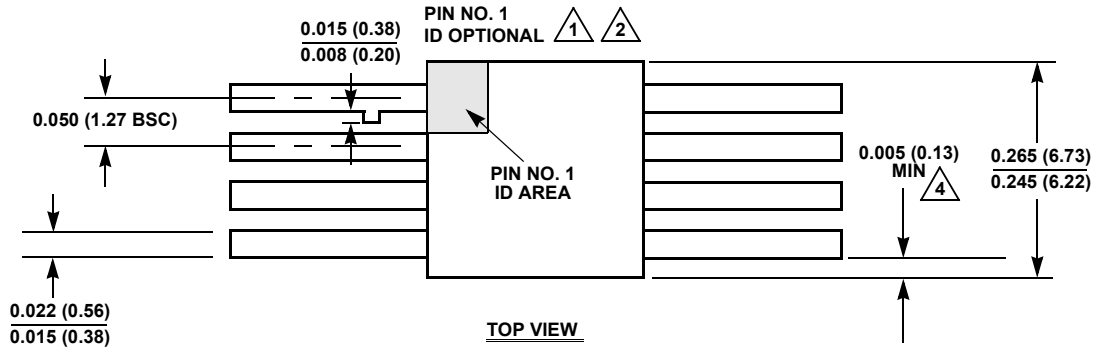
6. Revision History

Rev.	Date	Description
1.00	Jul 27, 2017	Changed the Maximum value for Propagation Delay HIGH to LOW, $t_{PD_{LH2}}$, from 650ns to 600ns. Changed the Maximum value for Total Loop Delay, Driver Input to Receiver Output, Dominant to Recessive, $t_{(LOOP2)}$, $R_S = 10k\Omega$ from 750ns to 700ns.
0.00	Mar 17, 2017	Initial release

7. Package Outline Drawing

For the most recent package outline drawing, see [K8.A](#).

K8.A
 8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE
 Rev 4, 12/14



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

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(Rev.1.0 Mar 2020)

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