ISL73141SEH

Radiation Hardened 14-Bit 1MSPS SAR ADC

The ISL73141SEH is a radiation hardened high precision 14-bit, 1Msps SAR Analog-to-Digital Converter (ADC) that features SNR of 82.1dBFS and dissipates only 60mW when operating from a 5V supply. With a 3.3V supply, the ISL73141SEH operates at 750ksps with a power consumption of 28mW.

The product features 1Msps throughput with no data latency and features excellent linearity and dynamic accuracy. The ISL73141SEH provides a high-speed SPI-compatible serial interface that supports logic ranging from 2.2V to 3.6V using a separate digital I/O supply pin.

The ISL73141SEH provides a separate power-down pin that reduces power dissipation to <50µW. The analog input signal range is determined by an external reference.

The ISL73141SEH operates across the military temperature range from -55°C to +125°C and is available in a 14 Ld hermetically sealed Ceramic Dual Flat-Pack (CDFP) package.

Applications

- Precision signal processing in satellite payloads
- Satellite telemetry systems
- Satellite propulsion and orbit control
- Attitude control of satellites
- High-end industrial
- Down-hole drilling

Features

- Qualified to Renesas Rad Hard QML-V Equivalent Screening and QCI flow (R34TB0001EU)
    - All screening and QCI is in accordance with MIL-PRF- 38535L Class-V
- 1Msps throughput rate with no data latency
- Excellent linearity: ±0.2 LSB DNL, ±0.5 LSB INL
- No missing codes
- Low noise: 82.1dB SNR
- 3.3V or 5V AV_{CC} supply options
- Separate 2.2V to 3.6V digital I/O supply
- Low power: 60mW at 1Msps
    - AV_{CC} = 5V, DV_{CC} = 2.5V
- Power-down mode with <50µW power consumption
- High speed SPI-compatible serial I/O
- Full military temperature range operation
    - T_A = -55°C to +125°C
- TID Rad Hard Assurance (RHA) testing
    - LDR (0.01rad(Si)/s): 75krad(Si)
- SEE Characterization (see SEE report for details)
    - No DSEE for AV_{CC} = 6.3V, DV_{CC} = 4.6V, and V_{REF} = 5.1V at 86MeV•cm^2/mg
    - SEFI <4.2µm^2 at LET 86MeV•cm^2/mg

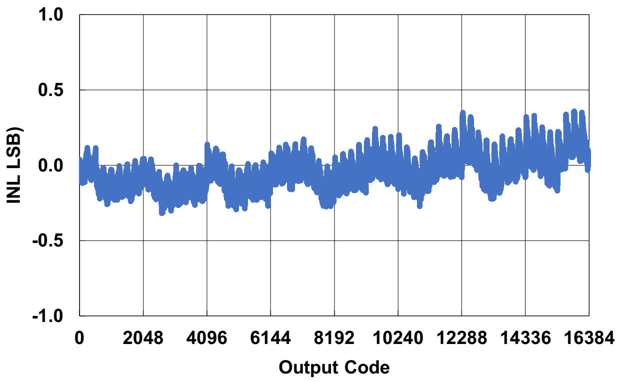


Figure 1. INL vs Output Code

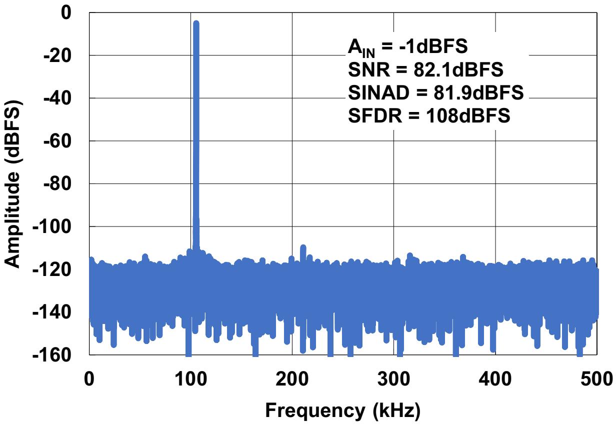


Figure 2. 32k FFT - 105.3kHz

Contents

1. Overview

1.1 Typical Application Schematic

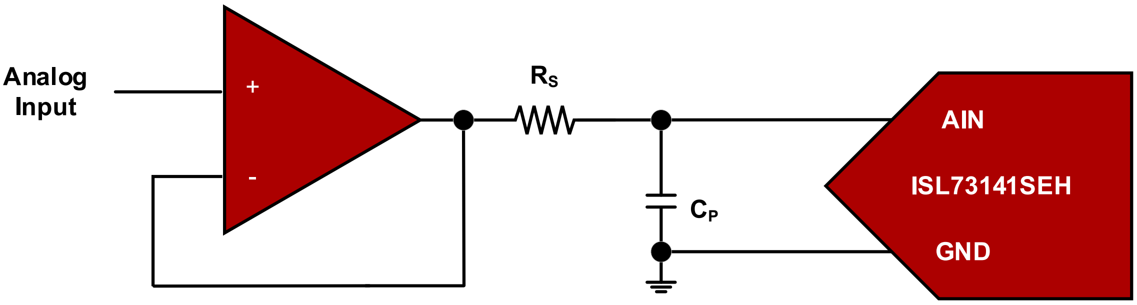


Figure 3. Typical Application Example Circuit

1.2 Functional Block Diagram

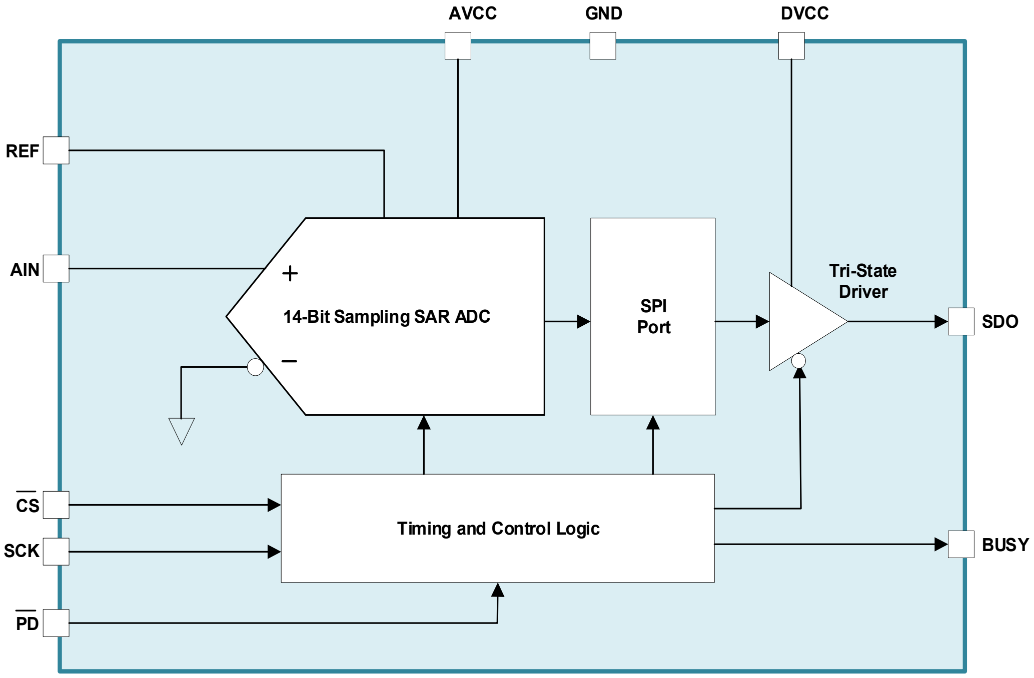
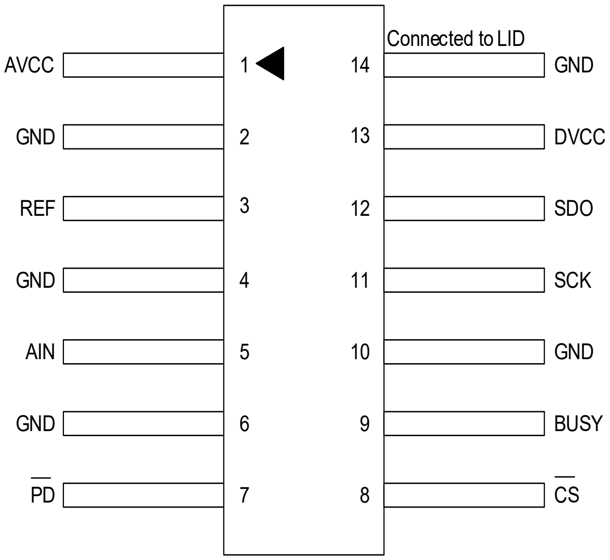


Figure 4. ISL73141SEH Block Diagram

2. Pin Information

2.1 Pin Assignments



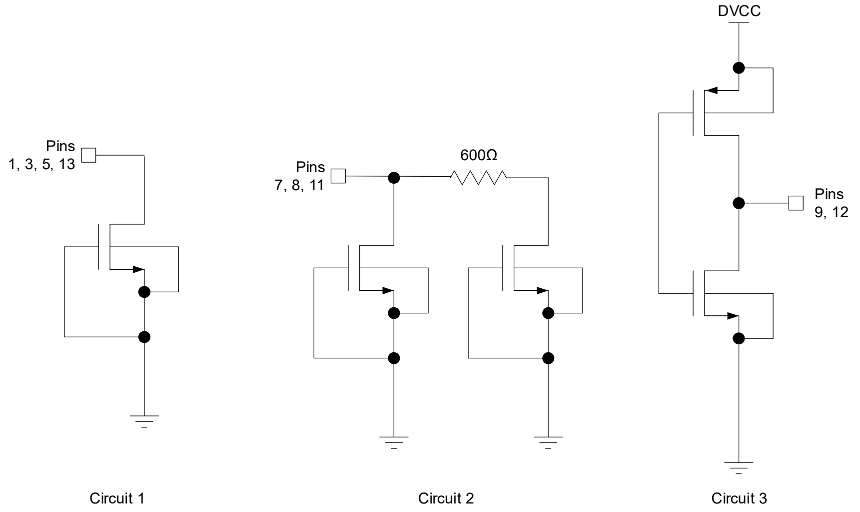
Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 5. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1	AVCC	1	Analog supply. The supply range is 3V to 3.6V (ISL73141SEHMFN) or 4.5V to 5.5V (ISL73141SEHMF7). Bypass this pin to GND with a 10µF ceramic capacitor.
2, 4, 6, 10, 14	GND	-	Analog and digital supply ground. Connect these pins directly to the PCB GND plane. Pin 14 (GND pin) is electrically connected to the package seal ring and lid.
3	REF	1	Reference input. The input range of REF is 1.95V to AV_{CC} for the ISL73141SEHMFN and 3.9V to 4.2V for the ISL73141SEHMF7. The voltage at the REF pin (V_{REF}) defines the input range of the analog input as 0V to V_{REF}. Bypass REF to GND with a low ESR 10µF ceramic capacitor.
5	AIN	1	Analog input. AIN supports an input voltage range of 0V to V_{REF}.
8	$\overline{\text{CS}}$	2	Convert Start Low input. A falling edge on this input starts a new conversion. The conversion is timed using an internal oscillator. The device automatically powers down following the conversion process. The logic state of the $\overline{\text{CS}}$ pin controls the state of the SDO pin. A logic high on the $\overline{\text{CS}}$ pin disables the SDO pin driver and the SDO pin impedance is Hi-Z. A logic low on the $\overline{\text{CS}}$ pin enables the SDO driver (unless $\overline{\text{PD}}$ is low) and allows data to be read out following a conversion.
7	$\overline{\text{PD}}$	2	Power-down low input. When this pin is brought low the ADC enters power-down mode. If this occurs during a conversion, the conversion is halted and the SDO pin is placed in Hi-Z. Logic levels are determined by DV_{CC}.
9	BUSY	3	Busy output. A logic high indicates a conversion is in progress. The BUSY indicator returns low following the completion of a conversion. Logic levels are determined by DV_{CC}.
11	SCK	2	Serial data clock input. When $\overline{\text{CS}}$ is low and the BUSY indicator is low, the conversion result is shifted out on SDO on the rising edges of SCK, Most Significant Bit (MSB) first to Least Significant Bit (LSB) last. Logic levels are determined by DV_{CC}. SCK should be held low when it is not being asserted.

Pin Number	Pin Name	ESD Circuit	Description
12	SDO	3	Serial data output. The current conversion result is serially shifted out on this pin on the rising edges of SCK, MSB first to LSB last. The data stream is composed of 14 bits of conversion data followed by trailing zeros. Logic Levels are determined by DV_{CC}.
13	DVCC	1	Digital I/O supply. Voltage range on this pin is 2.2V to 3.6V. DV_{CC} is nominally set to the same supply voltage as the host interface (2.5V or 3.3V). Bypass DVCC to GND with 0.1µF capacitor.
LID	N/A	N/A	Package Lid is internally connected to GND through Pin 14.



3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Min	Max	Unit
Supply Voltage (AV_{CC}, DV_{CC})	-0.3	6.4	V
Supply Voltage (AV_{CC})[1]	-0.3	6.3	V
Supply Voltage (DV_{CC})[1]	-0.3	4.6	V
AIN, REF[2]	-0.3	AV_{CC} + 0.3	V
AIN, REF[1][2]	-0.3	5.1	V
Digital Input Voltage ($\overline{PD}$, $\overline{CS}$, SCK)	-0.3	DV_{CC} + 0.3	V
Digital Output Voltage (BUSY, SDO)	-0.3	DV_{CC} + 0.3	V
AIN Input Current[3]	-3	3	mA
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM3015.7)	-	2.5	kV
Charged Device Model (Tested per JS-002-2014)	-	600	V

1. Tested in a heavy ion environment at LET = 86MeV•cm^2/mg at 125°C.
2. AIN voltage should not exceed REF voltage by more than 300mV or device damage can occur.
3. When an input voltage exceeds maximum operating conditions (voltage at the AIN pin less than GND or greater than AVCC), limit the input current to less than ±3mA.

3.2 Recommended Operating Conditions

Parameter	Min	Max	Unit
Temperature	-55	+125	°C
Analog Supply Voltage, A_{VCC} (ISL73141SEHMFN)	3.0	3.6	V
Analog Supply Voltage, A_{VCC} (ISL73141SEHMF7)	4.5	5.5	V
Digital Supply Voltage, D_{VCC}	2.2	3.6	V
Reference Input Voltage, V_{REF} (ISL73141SEHMFN)	1.95	3.6	V
Reference Input Voltage, V_{REF} (ISL73141SEHMF7)	3.9	4.2	V
Analog Input Voltage, A_{IN}	0	V_{REF}	V

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	CDFP Package K14.A	θ_{JA}[1]	Junction to ambient	34	°C/W
		θ_{JC}[2]	Junction to case	6	°C/W

1. θ_{JA} is measured in free air with the component on high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the package underside..

3.4 Electrical Specifications

3.4.1 ISL73141SEHMF7 - 5V Operation

Unless otherwise noted: AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 4.096V, GND = 0V, f_{SAMP} = 1Msps, A_{IN} = -1dBFS.**Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise	-	RMS noise, 14-bit LSB	-	0.3	-	LSB_{RMS}
Integral Non-Linearity	INL	Measured with full scale input signal.	**-1.0**	±0.4	**1.0**	LSB
Differential Non-Linearity	DNL	Measured with full scale input signal.	**-0.5**	±0.2	**0.5**	LSB
Zero Scale Error	VOFF	Measured with input grounded.	**-5**	0	**5**	LSB
Zero Scale Error Drift	VOFFD	Measured with input grounded.	-	±0.006	-	LSB/°C
Full Scale Error	FSE	Measured with input connected to VREF	**-7**	±1	**7**	LSB
Full Scale Error Drift	FSED	Measured with input connected to VREF	-	±0.004	-	LSB/°C
Dynamic Accuracy						
Signal to Noise Ratio	SNR	F_{IN} = 105kHz	**80**	82.1	-	dBFS
Signal to Noise + Distortion Ratio	SINAD	F_{IN} = 105kHz	**79**	81.9	-	dBFS
Effective Number of Bits	ENOB	F_{IN} = 105kHz	**12.5**	13.3	-	bits
Total Harmonic Distortion	THD	F_{IN} = 105kHz, first five harmonics	**85**	92	-	dBFS
Spurious Free Dynamic Range	SFDR	F_{IN} = 105kHz, first five harmonics excluded	**90**	108	-	dBFS
Input Bandwidth G		Source impedance = 25Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	2.5	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	1	-	ps_{RMS}
Analog Input Characteristics (A_{IN})						
Input Voltage Range, A_{IN}	A_{IN}	Recommended operating condition	**0**	-	$\mathbf{V_{REF}}$	V
Absolute Input Range, A_{IN}	-	-	**-0.1**	-	$\mathbf{AV_{CC} + 0.1}$	V
Input Leakage Current	IA_{IN}	-	**-1**	-	**1**	µA
Input Capacitance	-	Sample Mode	-	15	-	pF
		Hold Mode	-	3	-	pF
Reference Input Characteristics (REF)						
REF Input Voltage Range	V_{REF}	-	**3.9**	-	**4.2**	V
REF Input Current	I_{REF}	-	-	135	**200**	µA
Power Supply Characteristics (AVCC, DVCC)						
Analog Supply Voltage	AV_{CC}	-	**4.5**	-	**5.5**	V
Analog Supply Current - Active	I_{AVCC}	Active, f_{SAMP} = 1Msps	-	12	**14.5**	mA

Unless otherwise noted: AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 4.096V, GND = 0V, f_{SAMP} = 1Msps, A_{IN} = -1dBFS.**Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Analog Supply Current - Static	I_{Static}	$\overline{\text{CS}}$ held High	-	4.3	**7**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{\text{PD}}$ held Low	-	4.8	**12**	µA
Digital Supply Voltage	DV_{CC}	-	**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	f_{SCK} = 50MHz	-	72	**90**	µA
Digital Supply Current - Static	I_{STDVCC}	$\overline{\text{CS}}$ held High	-	26.4	**35**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{\text{PD}}$ held Low	-	6	**8**	µA
P_D	P_{ACTIVE}	Sample rate = 1Msps	-	60	**72.8**	mW
	P_{STATIC}	$\overline{\text{CS}}$ held High	-	21.6	**35.1**	mW
	P_{SLEEP}	$\overline{\text{PD}}$ held Low	-	39	**80**	µW
Digital Inputs and Outputs ($\overline{\text{PD}}$, $\overline{\text{CS}}$, SCK, BUSY, SDO)						
High Level Input	V_{IH}	-	**0.8×DV_{CC}**	-	-	V
Low Level Input	V_{IL}	-	-	-	**0.2×DV_{CC}**	V
Input Current ($\overline{\text{CS}}$, SCK)	I_{IN}	V_{IN} = 0V to DV_{CC}	**-1**	-	**1**	µA
Input Capacitance	C_{IN}	-	-	5	-	pF
High Level Output	V_{OH}	DV_{CC} - Output, I_O = -500µA	**DV_{CC} - 0.2**	-	-	V
Low Level Output	V_{OL}	I_O = 500µA	-	-	**0.2**	V
Output Source Current	I_{SRC}	V_{OUT} = 0V to DV_{CC}	-	-10	-	mA
Output Sink Current	I_{SNK}	V_{OUT} = 0V to DV_{CC}	-	10	-	mA
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0V to DV_{CC}	**-1**		**1**	µA
$\overline{\text{PD}}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to D_{VCC}	**400**	500	**600**	kΩ

1. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.4.2 ISL73141SEHMFN - 3.3V Operation

Unless otherwise noted: AV_{CC} = 3.3V; DV_{CC} = 2.5V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Converter Characteristics						
Resolution	-	-	**14**	-	-	bits
No Missing Codes	-	-	**14**	-	-	bits
Transition Noise	-	RMS noise, 14-bit LSB	-	0.4	-	LSB_{RMS}
Integral Non-Linearity	INL	Measured with full scale input signal	**-1.5**	±0.5	**1.5**	LSB
Differential Non-Linearity	DNL	Measured with full scale input signal	**-0.5**	±0.25	**0.5**	LSB
Zero Scale Error	VOFF	Measured with input grounded	**-5**	0	**5**	LSB

Unless otherwise noted: AV_{CC} = 3.3V; DV_{CC} = 2.5V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS. (Cont.)**Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Zero Scale Error Drift,	VOFFD	Measured with input grounded	-	±0.01	-	LSB/°C
Full Scale Error	FSE	Measured with input connected to VREF	**-7**	±1	**7**	LSB
Full Scale Error Drift	FSED	Measured with input connected to VREF	-	±0.02	-	LSB/°C
Dynamic Accuracy						
Signal to Noise Ratio	SNR	F_{IN} = 105kHz	**77**	80.3	-	dB
Signal to Noise + Distortion Ratio	SINAD	F_{IN} = 105kHz	**76**	80.1	-	dB
Effective Number of Bits	ENOB	F_{IN} = 105kHz	**12.3**	12.8	-	bits
Total Harmonic Distortion	THD	F_{IN} = 105kHz, first five harmonics	**85**	92	-	dB
Spurious Free Dynamic Range	SFDR	F_{IN} = 105kHz, first five harmonics excluded	**90**	108	-	dB
Input Bandwidth	-	Source impedance = 25Ω, -3dB point	-	50	-	MHz
Aperture Delay	t_{AD}	$\overline{CS}$ falling edge to sample edge	-	4	-	ns
Aperture Jitter	$t_{AJITTER}$	-	-	1	-	ps_{RMS}
Analog Input Characteristics (A_{IN})						
Input Voltage Range, A_{IN}	A_{IN}	Recommended operating condition	**0**	-	**V_{REF}**	V
Absolute Input Range, A_{IN}	-	-	**-0.1**	-	**AV_{CC} + 0.1**	V
Input Leakage Current	IA_{IN}	-	**-1**	-	**1**	µA
Input Capacitance	-	Sample Mode	-	15	-	pF
		Hold Mode	-	3	-	pF
Reference Input Characteristics (REF)						
REF Input Voltage Range	V_{REF}	-	**1.95**	-	**AV_{CC}**	V
REF Input Current	I_{REF}	-	-	82	**150**	µA
Power Supply Characteristics (AV_{CC}, DV_{CC})						
Analog Supply Voltage	AV_{CC}	-	**3**	-	**3.6**	V
Analog Supply Current - Active	I_{AVCC}	Active, f_{SAMP} = 750ksps	-	8.5	**10.5**	mA
Analog Supply Current - Static	I_{Static}	$\overline{CS}$ held High	-	3.7	**6.5**	mA
Analog Supply Current - Sleep	I_{SLAVCC}	$\overline{PD}$ held Low	-	4.6	**10**	µA
Digital Supply Voltage	DV_{CC}		**2.2**	-	**3.6**	V
Digital Supply Current - Active	I_{DVCC}	f_{SCK} = 33MHz, 10pF load	-	70	**90**	µA
Digital Supply Current - Static	I_{STDVCC}	$\overline{CS}$ held High	-	27	**35**	µA
Digital Supply Current - Sleep	I_{SLDVCC}	$\overline{PD}$ held Low	-	6	**8**	µA
P_D	P_{ACTIVE}	Sample rate = 750ksps	-	28	**33.9**	mW
	P_{STATIC}	$\overline{CS}$ held High	-	12.3	**21.6**	mW
	P_{SLEEP}	$\overline{PD}$ held Low	-	30.2	**53**	µW

Unless otherwise noted: AV_{CC} = 3.3V; DV_{CC} = 2.5V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS. (Cont.)**Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.** (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Digital Inputs and Outputs ($\overline{\text{PD}}$, $\overline{\text{CS}}$, SCK, BUSY, SDO)						
High Level Input	V_{IH}	-	**0.8×DV_{CC}**	-	-	V
Low Level Input	V_{IL}	-	-	-	**0.2×DV_{CC}**	V
Input Current ($\overline{\text{CS}}$, SCK)	I_{IN}	V_{IN} = 0V to DV_{CC}	**-1**	-	**1**	µA
Input Capacitance	C_{IN}	-	-	5	-	pF
High Level Output	V_{OH}	DV_{CC} - Output, I_O = -500µA	**DV_{CC} - 0.2**	-	-	V
Low Level Output	V_{OL}	I_O = 500µA	-	-	**0.2**	V
Output Source Current	I_{SRC}	V_{OUT} = 0V to DV_{CC}	-	-10	-	mA
Output Sink Current	I_{SNK}	V_{OUT} = 0V to DV_{CC}	-	10	-	mA
Hi-Z Output Leakage Current	I_{OZ}	V_{OUT} = 0V to DV_{CC}	**-1**	-	**1**	µA
$\overline{\text{PD}}$ Input Resistance	R_{INPDL}	Internal pull-up resistance to D_{VCC}	**400**	500	**600**	kΩ

1. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.4.3 ISL73141SEHMF7 - 5.0V Operation Burn-In Deltas

AV_{CC} = 5.0V; DV_{CC} = 2.5V, REF = 4.096V, GND = 0V, f_{SAMP} = 1000ksps, A_{IN} = -1dBFS; T_A = +25°C; unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Integral Non-Linearity	INL	Measured with full scale input signal	-0.35	0.35	LSB
Signal to Noise Ratio	SNR	F_{IN} = 105kHz	-1	1	dBFS
Effective Number of Bits	ENOB	F_{IN} = 105kHz	-0.2	0.2	bits

3.4.4 ISL73141SEHMFN - 3.3V Operation Burn-In Deltas

AV_{CC} = 3.3V; DV_{CC} = 2.5V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS; T_A = +25°C;unless otherwise noted.

Parameter	Symbol	Test Conditions	Min	Max	Unit
Integral Non-Linearity	INL	Measured with full scale input signal	-0.5	0.5	LSB
Signal to Noise Ratio	SNR	F_{IN} = 105kHz	-1	1	dBFS
Effective Number of Bits	ENOB	F_{IN} = 105kHz	-0.2	0.2	bits

3.5 Timing Specifications

3.5.1 5V Operation

Unless otherwise noted: AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 4.096V, GND = 0V, f_{SAMP} = 1Msps, A_{IN} = -1dBFS. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Timing Characteristics						
Maximum Sampling Frequency	f_{SAMP}	-	-	-	**1**	MHz
Conversion Time	t_{CONV}	BUSY Output High Time	-	595	**665**	ns
$\overline{\text{CS}}$ High Time	t_{CSH}	-	**40**	-	-	ns

Unless otherwise noted: AV_{CC} = 4.5V to 5.5V; DV_{CC} = 2.2V to 3.6V, REF = 4.096V, GND = 0V, f_{SAMP} = 1Msps, A_{IN} = -1dBFS. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
SCK Held Low to $\overline{\text{CS}}$↓	t_{QUIET}	-	**40**	-	-	ns
$\overline{\text{CS}}$ Falling Edge to BUSY↑	t_{BUSYLH}	C_L = 10pF	-	17	**25**	ns
SCK Period	t_{SCK}	-	**20**	-	-	ns
SCK High Time	t_{SCKH}	-	**8**	-	-	ns
SCK Low Time	t_{SCKL}	-	**8**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-2.6	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**18.5**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**8**	13	-	ns
SDO Bus Acquisition Time from $\overline{\text{CS}}$↓	$t_{DCSLSDOL}$	C_L = 10pF	-	11	**20**	ns
SDO Bus Relinquish Time after $\overline{\text{CS}}$↑	$t_{DCSHSDOZ}$	C_L = 10pF	-	12	**20**	ns
Wake-Up time from Power-Down Mode	t_{WAKE}	Time to wait after $\overline{\text{PD}}$↑ to first sample	-	20	-	µs

1. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.5.2 3.3V Operation

Unless otherwise noted: AV_{CC} = 3.0V to 3.6V; DV_{CC} = 2.2V to 3.6V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

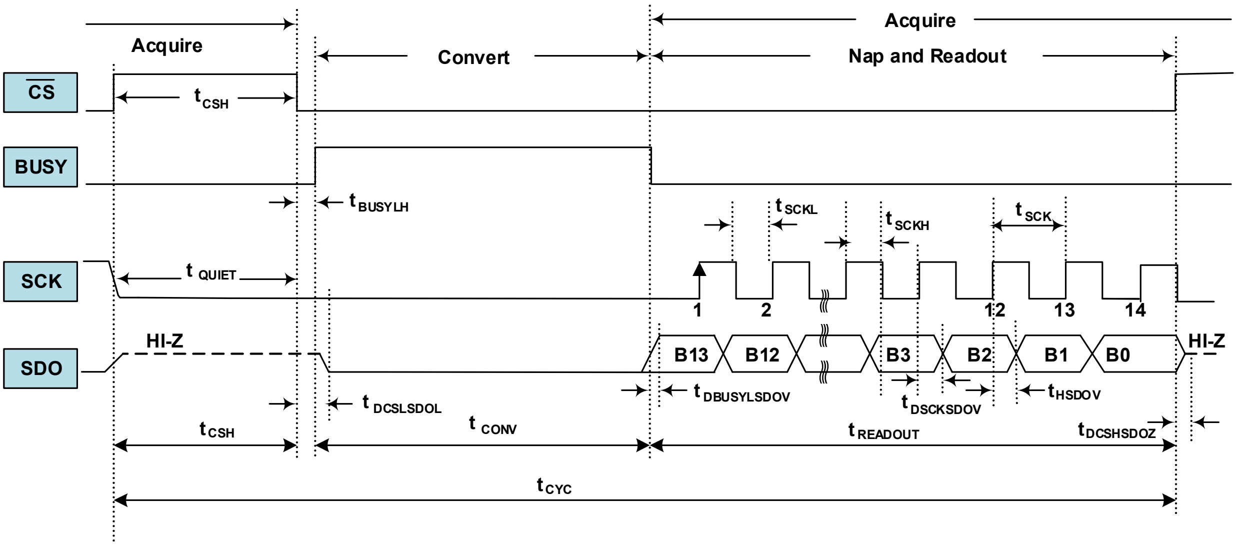
Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
Timing Characteristics						
Maximum Sampling Frequency	f_{SAMP}	-	-	-	**750**	kHz
Conversion Time	t_{CONV}	BUSY Output High Time	-	760	**850**	ns
$\overline{\text{CS}}$ High Time	t_{CSH}	-	**50**	-	-	ns
SCK Held Low to $\overline{\text{CS}}$↓	t_{QUIET}	-	**50**	-	-	ns
$\overline{\text{CS}}$ Falling Edge to BUSY↑	t_{BUSYLH}	C_L = 10pF	-	21	40	ns
SCK Period	t_{SCK}	-	**30**	-	-	ns
SCK High Time	t_{SCKH}	-	**12**	-	-	ns
SCK Low Time	t_{SCKL}	-	**12**	-	-	ns
SDO Data Valid Delay from BUSY↓	$t_{DBUSYLSDOV}$	C_L = 10pF	-	-5	**0**	ns
SDO Data Valid Delay from SCK↑	$t_{DSCKSDOV}$	C_L = 10pF	-	-	**25**	ns
SDO Data Valid Hold Time from SCK↑	t_{HSDOV}	C_L = 10pF	**8**	16	-	ns
SDO Bus Acquisition Time from $\overline{\text{CS}}$↓	$t_{DCSLSDOL}$	C_L = 10pF	-	12	**30**	ns

Unless otherwise noted: AV_{CC} = 3.0V to 3.6V; DV_{CC} = 2.2V to 3.6V, REF = 3.0V, GND = 0V, f_{SAMP} = 750ksps, A_{IN} = -1dBFS. **Boldface limits apply across the operating temperature range, -55°C to +125°C by production testings; over a total ionizing dose of 75krad(Si) at +25°C with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min	Typ[1]	Max	Unit
SDO Bus Relinquish Time after $\overline{CS}$↑	$t_{DCSHSDOZ}$	C_L = 10pF	-	14	**30**	ns
Wake-Up time from Power-Down Mode	t_{WAKE}	Time to wait after $\overline{PD}$↑ to first sample	-	20	-	µs

1. Typical values shown are not guaranteed. Values derived from +25°C median data.

3.6 Timing Diagrams



Serial Data Bits B[13:0] Correspond to the Current Conversion

Figure 6. ISL73141SEH Operational Timing Diagram

4. Typical Performance Curves

4.1 5.0V Curves

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 1Msps; T_A = +25°C

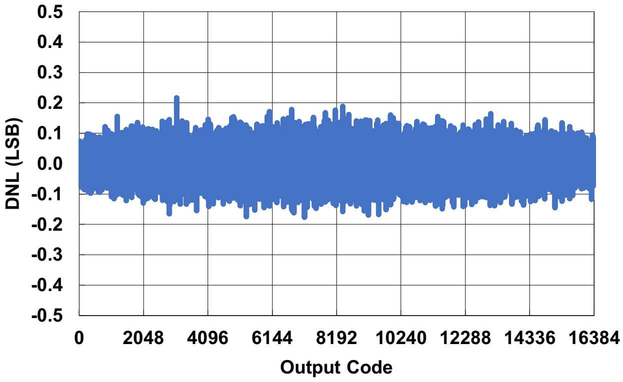


Figure 7. Differential Non-Linearity (DNL)

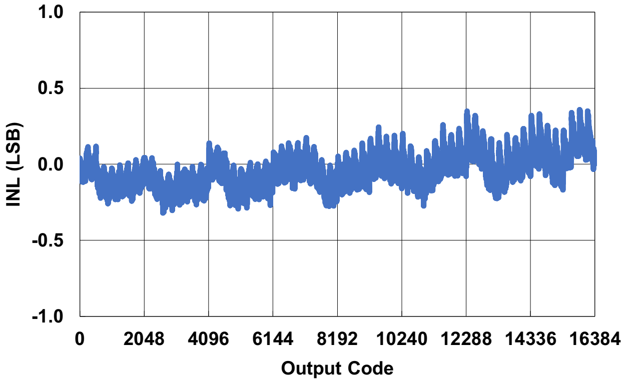


Figure 8. Integral Non-Linearity (INL)

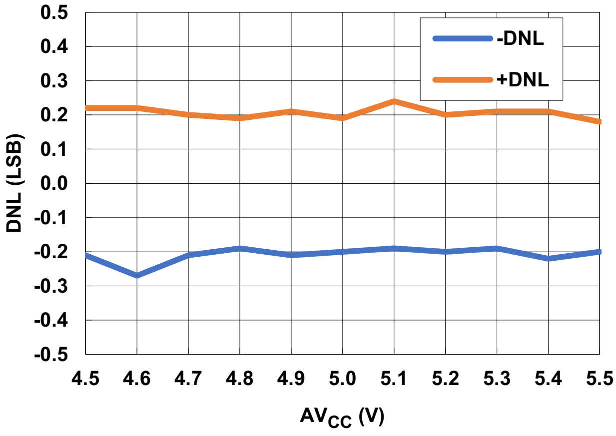


Figure 9. DNL vs AV_{CC}

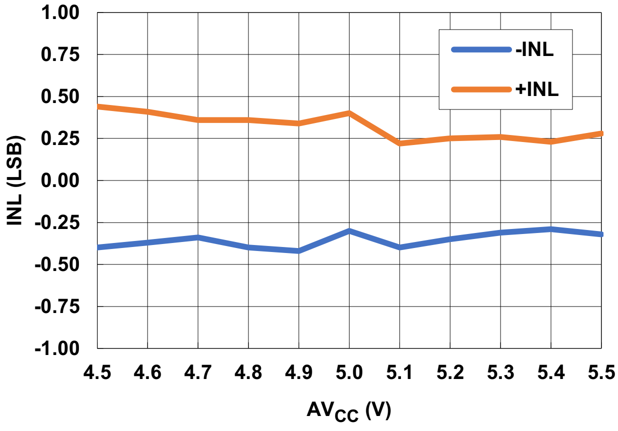


Figure 10. INL vs AV_{CC}

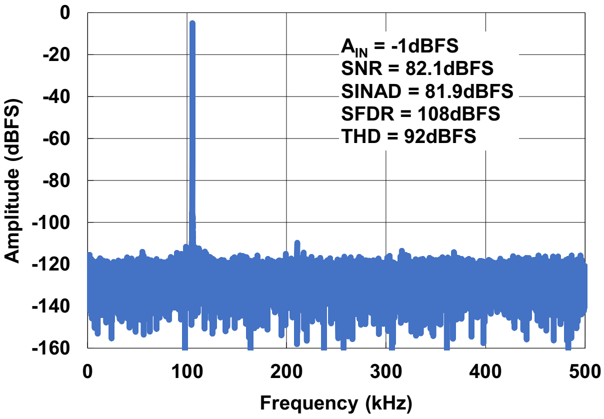


Figure 11. 32k FFT - 105.3kHz

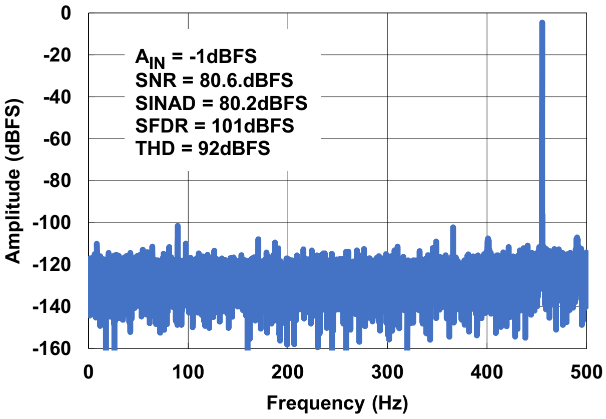


Figure 12. 32k FFT - 455.3kHz

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 1Msps; T_A = +25°C (Cont.)

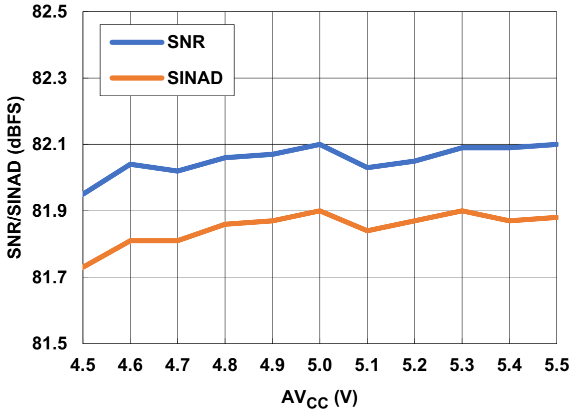


Figure 13. SNR and SINAD vs AV_{CC}

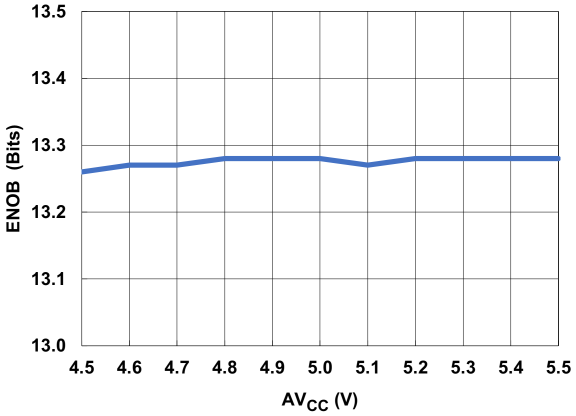


Figure 14. ENOB vs AVCC

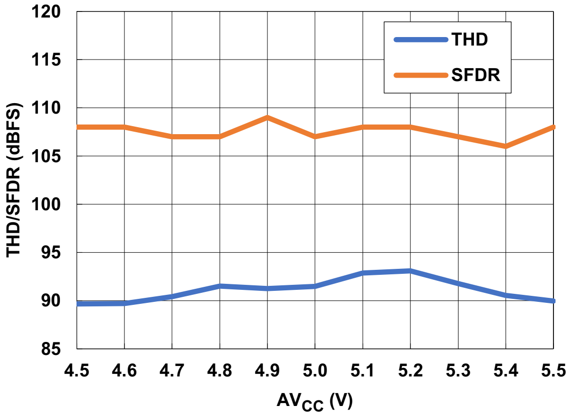


Figure 15. THD and SFDR vs AV_{CC}

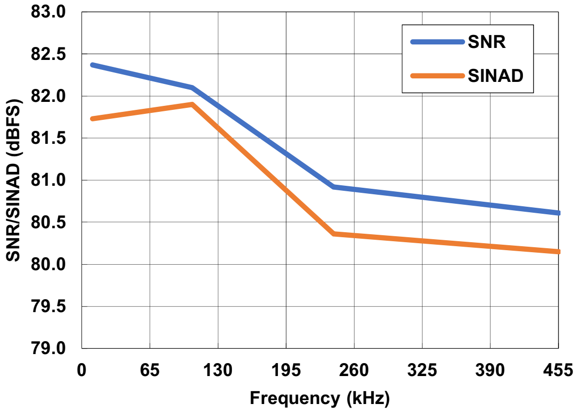


Figure 16. SNR and SINAD vs Frequency

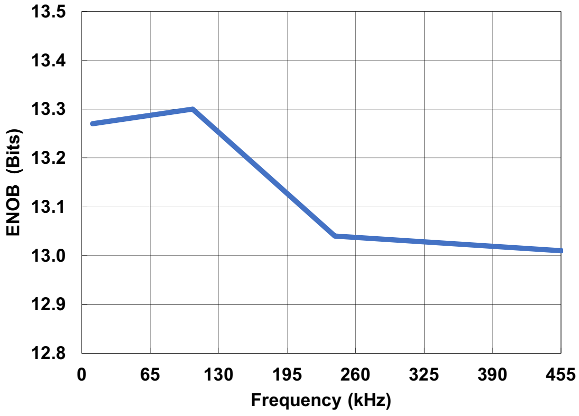


Figure 17. ENOB vs Frequency

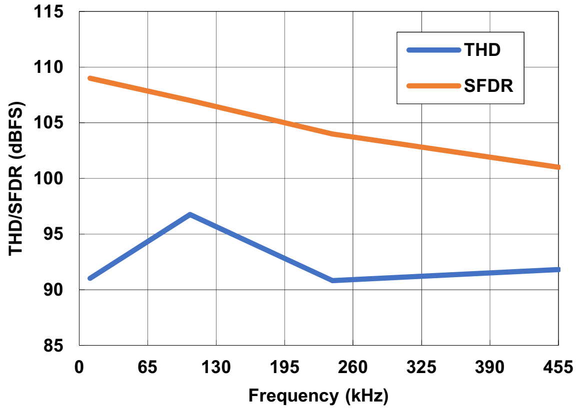


Figure 18. THD and SFDR vs Frequency

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 1Msps; T_A = +25°C (Cont.)

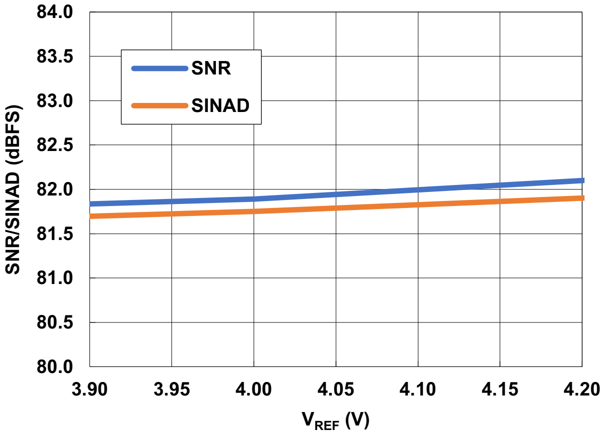


Figure 19. SNR and SINAD vs V_{REF}

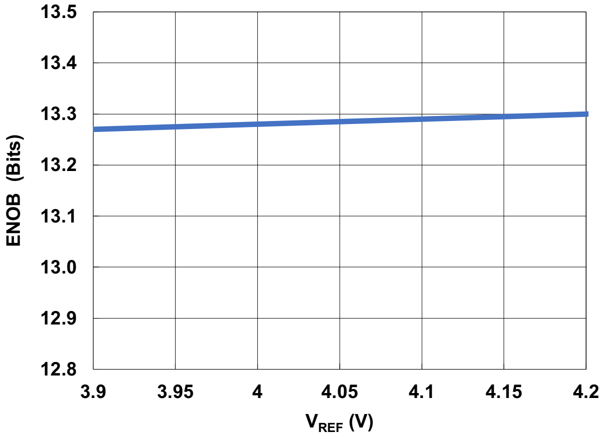


Figure 20. ENOB vs V_{REF}

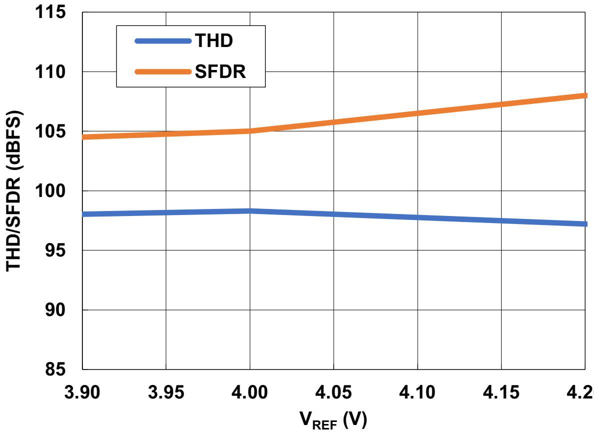


Figure 21. THD and SFDR vs V_{REF}

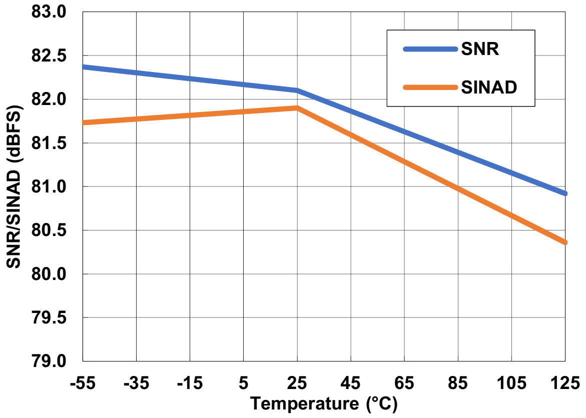


Figure 22. SNR and SINAD vs Temperature

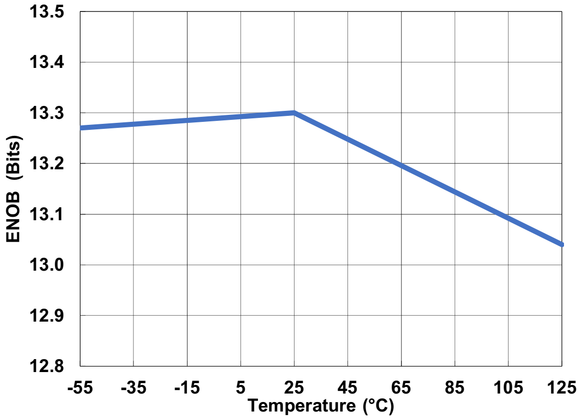


Figure 23. ENOB vs Temperature

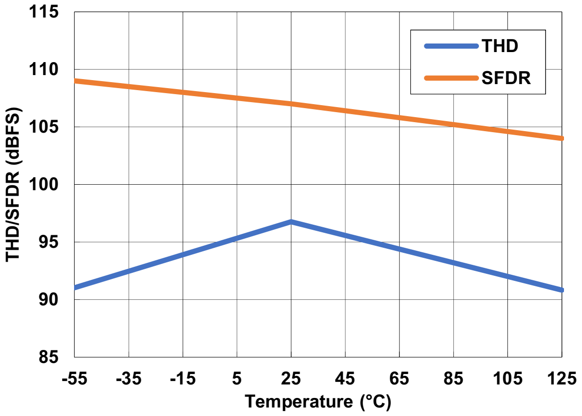


Figure 24. THD and SFDR vs Temperature

Unless otherwise noted, AV_{CC} = 5.0V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 1Msps; T_A = +25°C (Cont.)

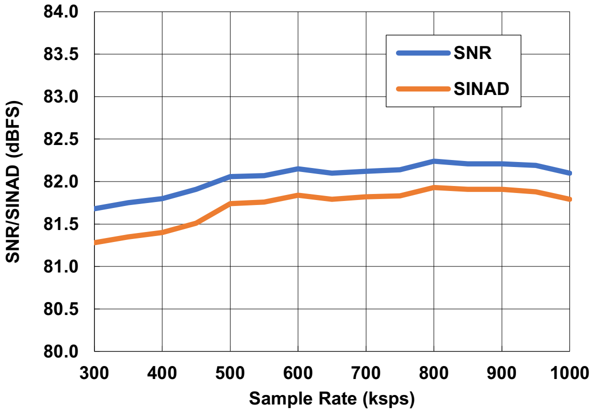


Figure 25. SNR and SINAD vs Sample Rate

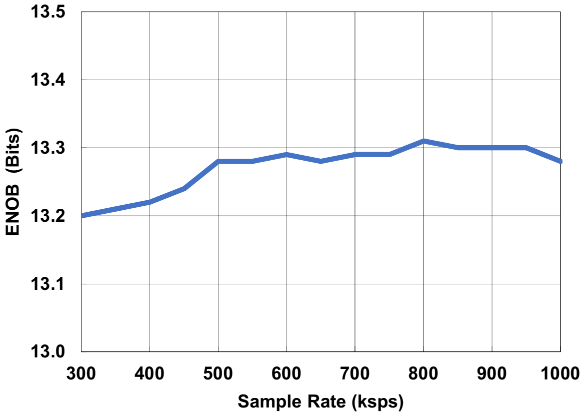


Figure 26. ENOB vs Sample Rate

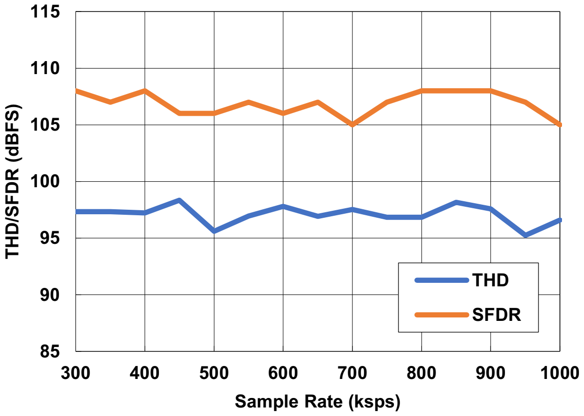


Figure 27. THD and SFDR vs Sample Rate

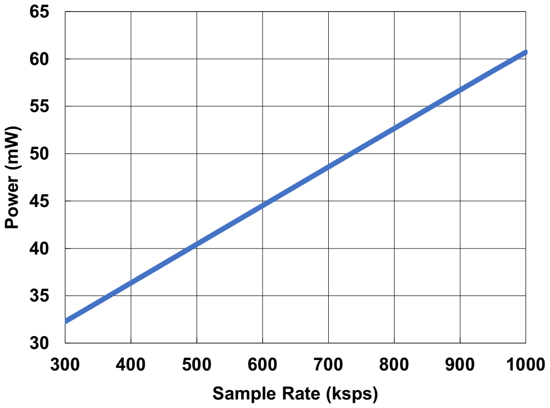


Figure 28. Power vs Sample Rate

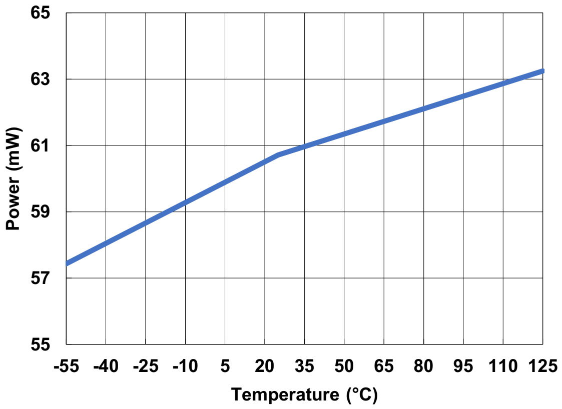


Figure 29. Power vs Temperature

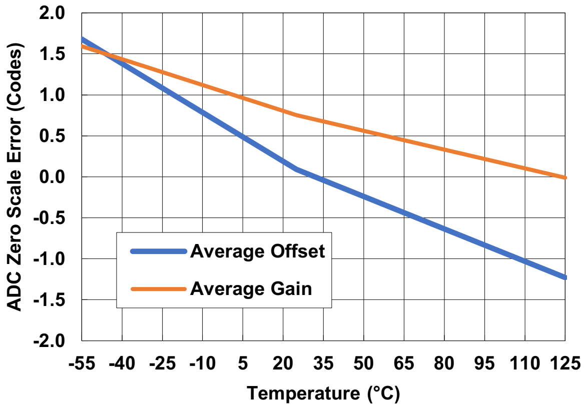


Figure 30. Zero and Full Scale Error vs Temperature

4.2 3.3V Curves

Unless otherwise noted, AV_{CC} = 3.3V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 750ksps; T_A = +25°C

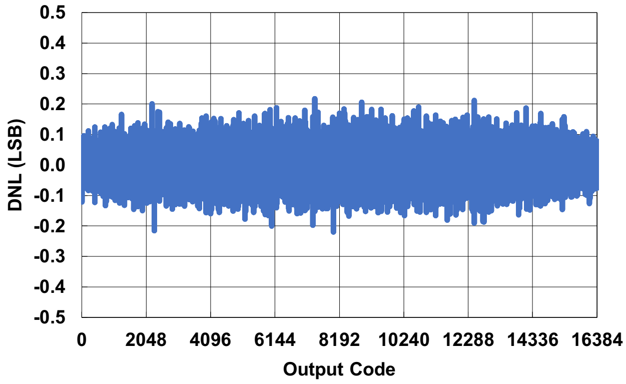


Figure 31. Differential Non-Linearity (DNL)

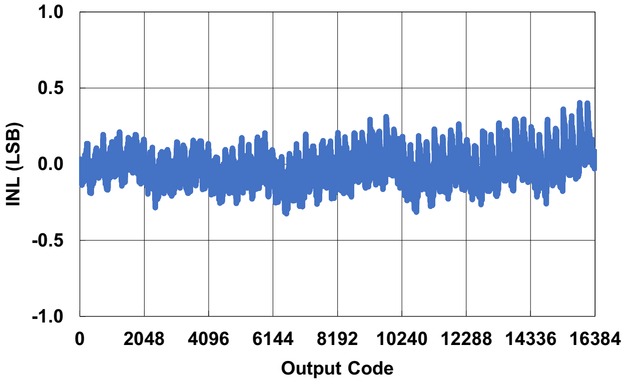


Figure 32. Integral Non-Linearity (INL)

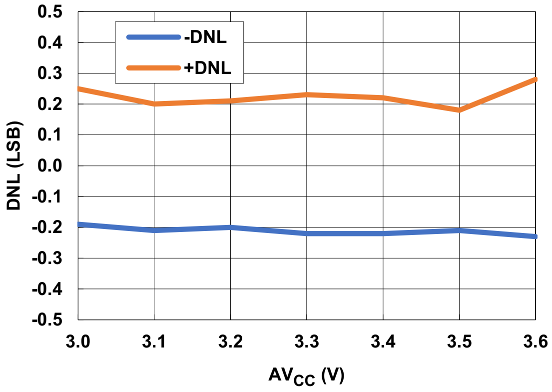


Figure 33. DNL vs AV_{CC}

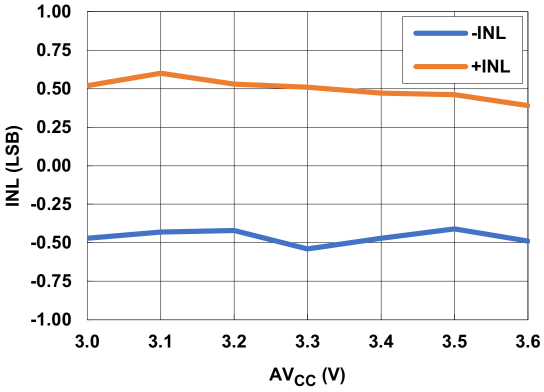


Figure 34. INL vs AV_{CC}

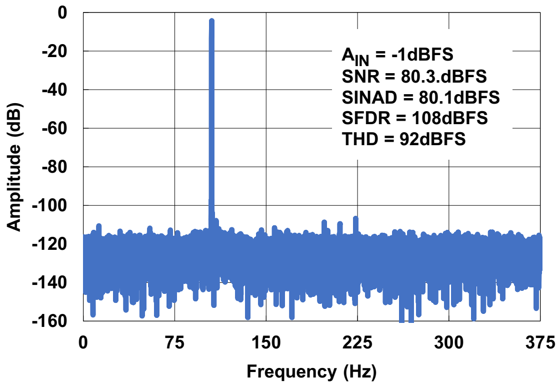


Figure 35. 32k FFT - 105.3kHz

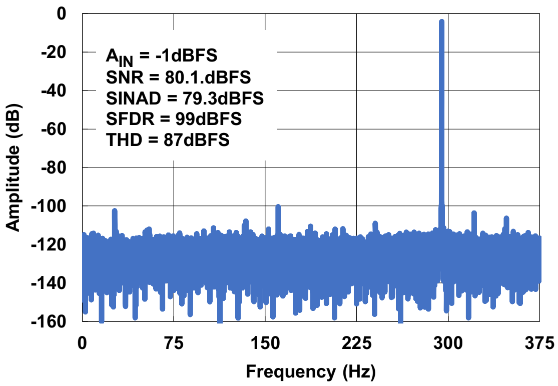


Figure 36. 32k FFT - 455.3kHz

Unless otherwise noted, AV_{CC} = 3.3V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 750ksps; T_A = +25°C (Cont.)

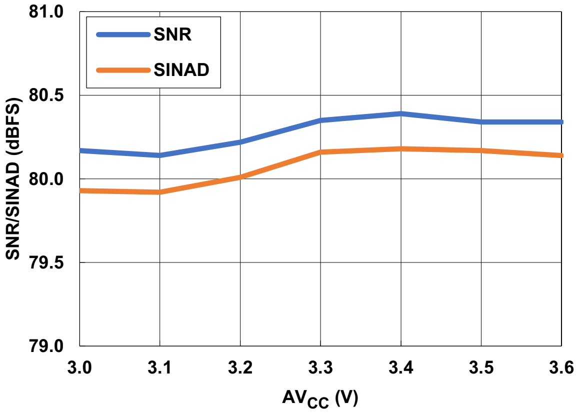


Figure 37. SNR and SINAD vs AV_{CC}

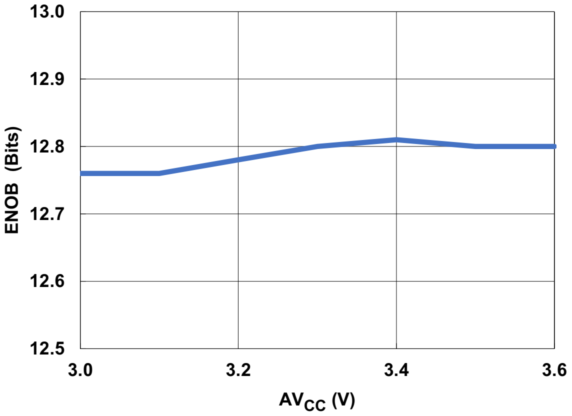


Figure 38. ENOB vs AV_{CC}

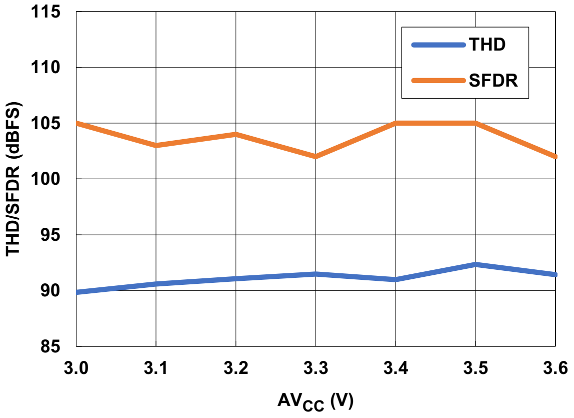


Figure 39. THD and SFDR vs AV_{CC}

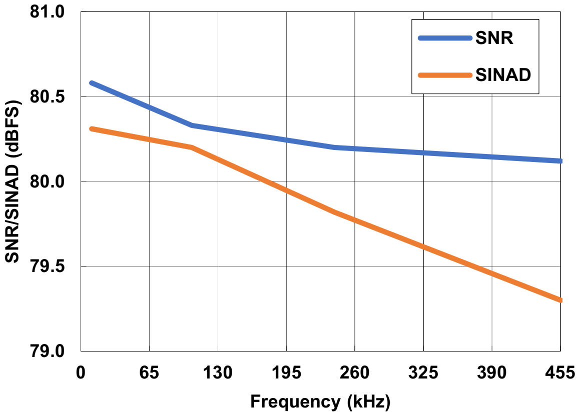


Figure 40. SNR and SINAD vs Frequency

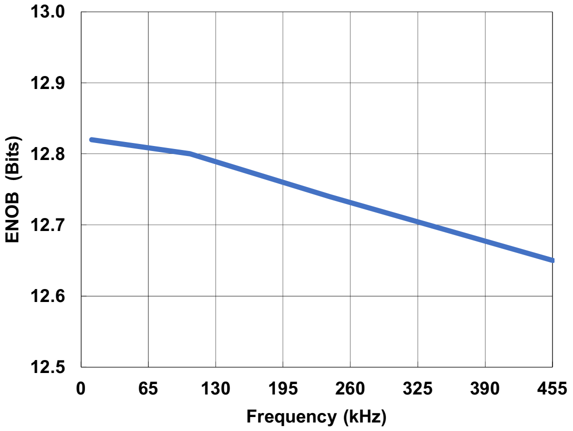


Figure 41. ENOB vs Frequency

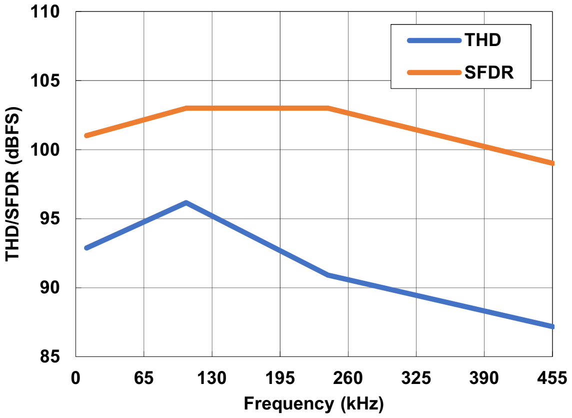


Figure 42. THD and SFDR vs Frequency

Unless otherwise noted, AV_{CC} = 3.3V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 750ksps; T_A = +25°C (Cont.)

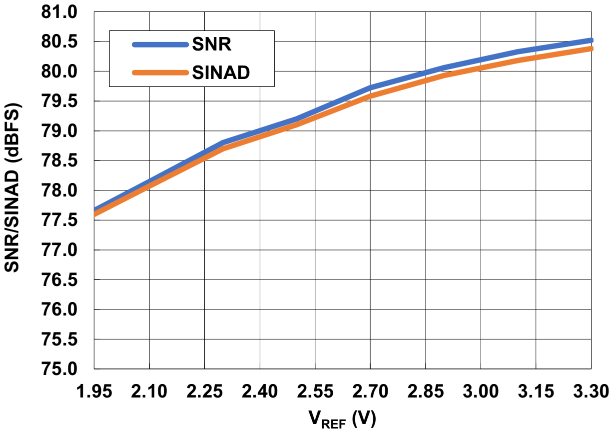


Figure 43. SNR and SINAD vs V_{REF}

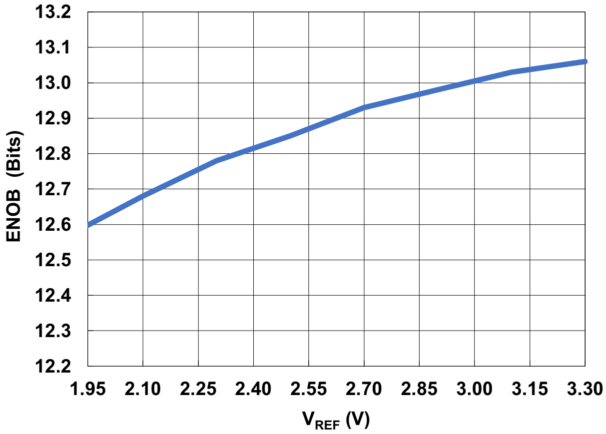


Figure 44. ENOB vs V_{REF}

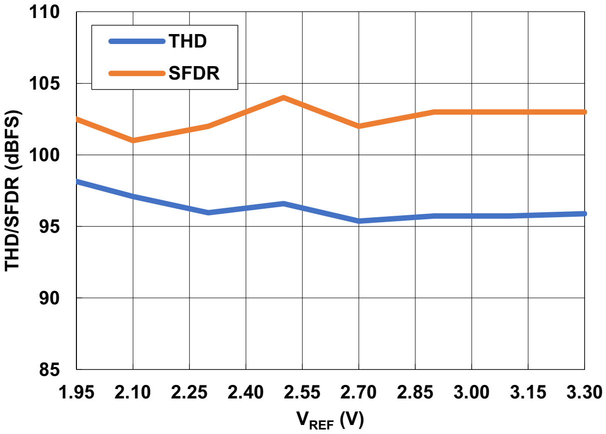


Figure 45. THD and SFDR vs V_{REF}

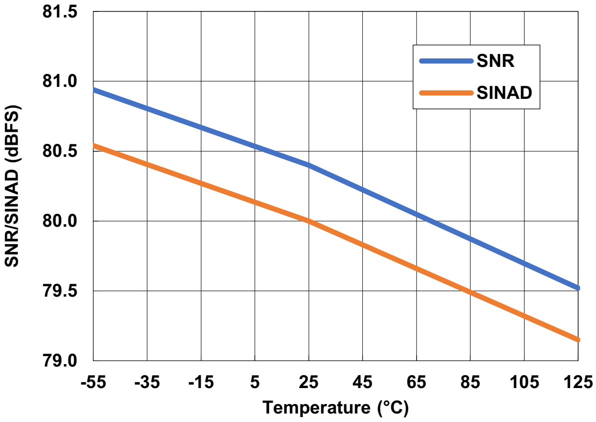


Figure 46. SNR and SINAD vs Temperature

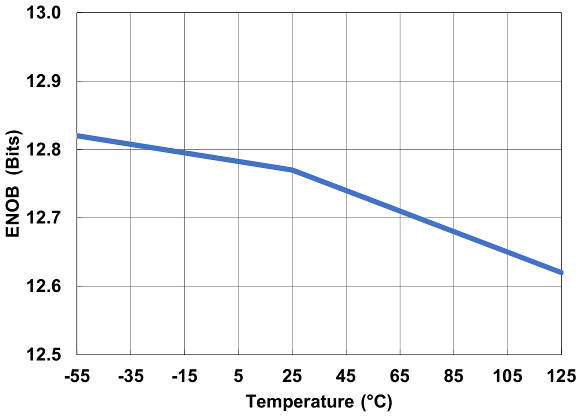


Figure 47. ENOB vs Temperature

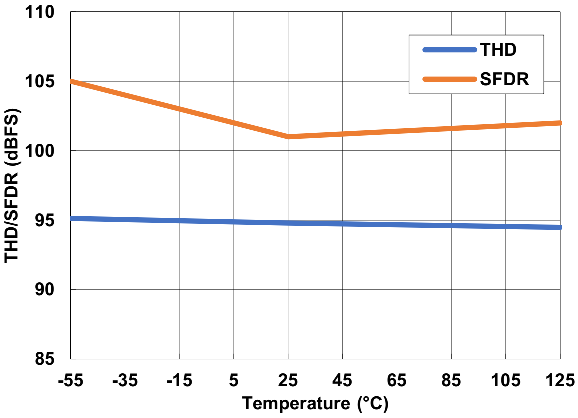


Figure 48. THD and SFDR vs Temperature

Unless otherwise noted, AV_{CC} = 3.3V; DV_{CC} = 2.5V; f_{IN} = 105.3kHz; f_{SAMP} = 750ksps; T_A = +25°C (Cont.)

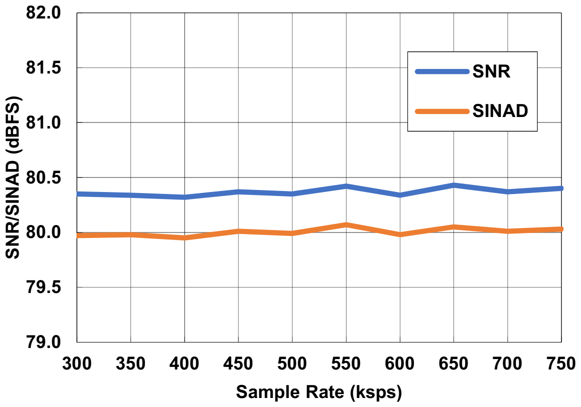


Figure 49. SNR and SINAD vs Sample Rate

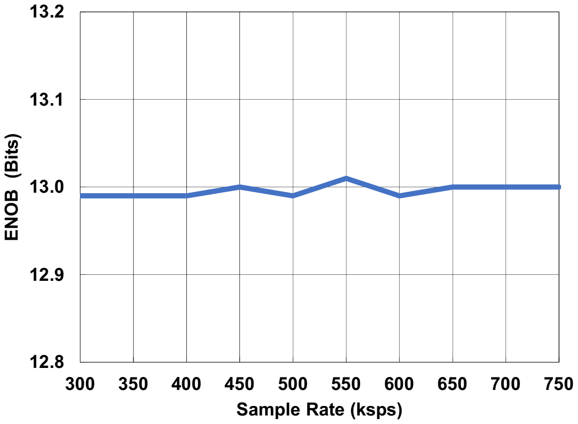


Figure 50. ENOB vs Sample Rate

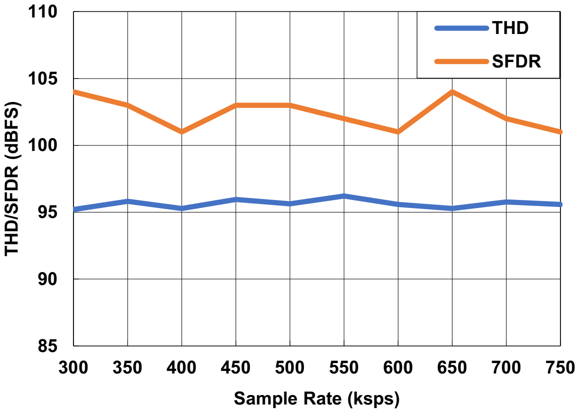


Figure 51. THD and SFDR vs Sample Rate

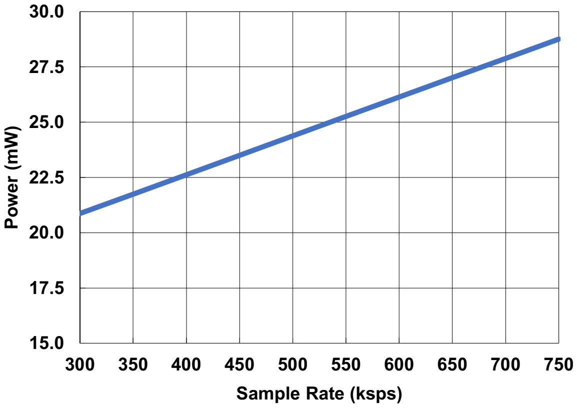


Figure 52. Power vs Sample Rate

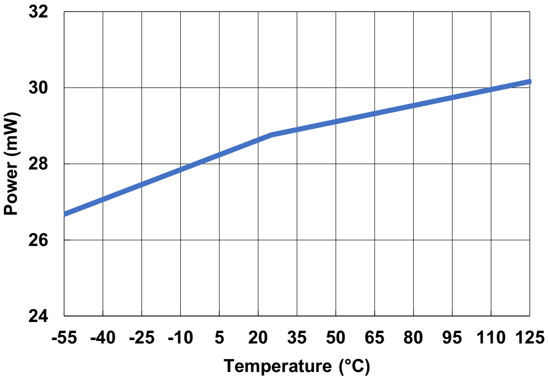


Figure 53. Power vs Temperature

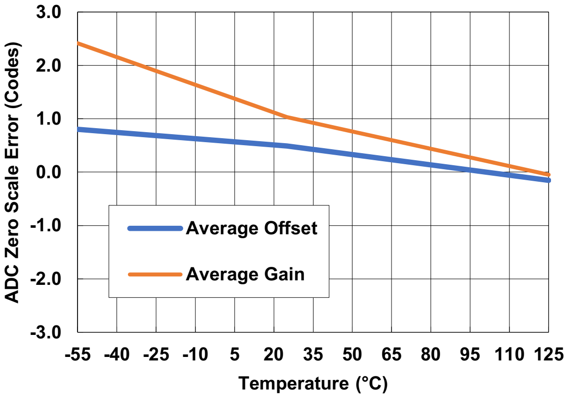


Figure 54. Zero and Full Scale Error vs Temperature

5. Applications Information

5.1 Overview

The ISL73141SEH is a radiation hardened, high precision, low noise, 14-bit Successive Approximation Register (SAR) ADC. The device operates from an analog supply voltage range of 3V to 3.6V or 4.5V to 5.5V, a digital supply voltage range of 2.2V to 3.6V, and has a dedicated reference input (REF). The ISL73141SEH supports sample rates up to 1Msps with an analog supply voltage range of 4.5V to 5.5V. It also supports sample rates up to 750ksps with an analog supply voltage range of 3V to 3.6V, which allows you to optimize your system based on the range of the analog signal being sampled. The ISL73141SEH samples at a rate of 1Msps and achieves excellent dynamic performance (82.1dB SNR, 100dB THD) and linearity (INL ±1LSB, DNL ±0.5 LSB) while still maintaining a low power consumption of 60mW from a 5V supply. Additionally, the device offers a Sleep mode that minimizes power consumption to <50µW during idle operation.

The IS73141SEH offers a high-speed serial interface with an independent digital supply (DV_{CC}) range of 2.2V to 3.6V, making it ideal to interface to 2.5V or 3.3V systems. The conversion data is output on the SDO pin with no latency. The ISL73141SEH supports up to a 50MHz serial data read clock on the SCK input.

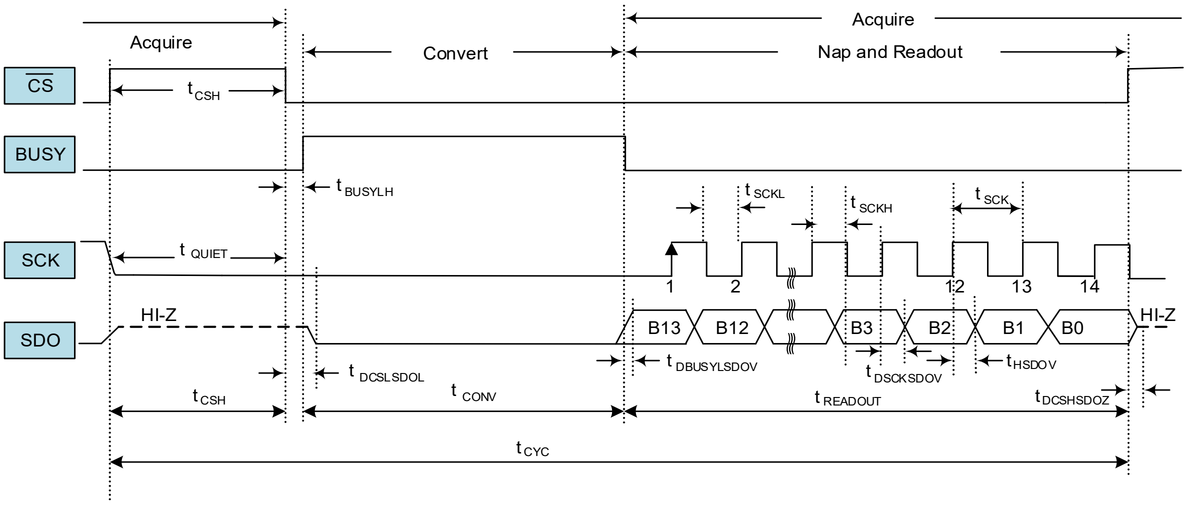
The single-ended analog input voltage (A_{IN}) is sampled on the falling edge of $\overline{CS}$. The input range of the ISL73141SEH is determined by the REF pin voltage to GND. The ISL73141SEH supports excellent THD and SFDR sampling input signal frequencies up to and beyond Nyquist (such as $f_{IN} \geq 500kHz$ with $f_{SAMP} = 1Msps$). The ISL73141SEH uses the external reference input (REF) as the positive reference and the GND pin of the device as the negative reference.

5.2 Serial Interface and BUSY

The ISL73141SEH uses a 3-wire serial port interface to communicate with other devices such as microcontrollers and other external circuitry. A falling edge on $\overline{CS}$ initiates conversion in the ISL73141SEH. Renesas requires holding $\overline{CS}$ high for at least 40ns before initiating the conversion. The conversion is timed by an internal oscillator. During the conversion process, the BUSY signal is asserted high. When the conversion is complete, BUSY is de-asserted. Renesas requires holding SCK low during t_{CONV}. When BUSY is de-asserted, the MSB is immediately available on the SDO pin. Each subsequent rising edge of SCK serially outputs data on SDO from the MSB-1 to the LSB. The input logic level of $\overline{CS}$ and SCK is determined by the DV_{CC} supply voltage that operates across a range of 2.2V up to 3.6V. Similarly, the output voltage level of BUSY is also determined by the DV_{CC} supply voltage.

5.3 Operational Phases and Timing

The conversion result MSB is available for serial readout at the SDO pin immediately following a completed conversion. The BUSY indicator flag is high during conversion, and transitions low following completion of the conversion. When the BUSY indicator flag goes LOW after a conversion, the MSB of the conversion result (B13) is immediately available at the SDO pin. Subsequent rising edges of SCK shift bits MSB-1 (B12) through the LSB (B0) to SDO for readout. The output voltage level of SDO is determined by the DV_{CC} supply voltage which operates across a range of 2.2V up to 3.6V. Figure 55 shows the basic timing of the ISL73141SEH in a conversion cycle.



Serial Data Bits B[13:0] Correspond to the Current Conversion

Figure 55. ISL73141SEH Timing Diagram

The following are the three phases of operation in the ISL73141SEH that are shown in Figure 55.

- Acquisition
- Conversion
- Readout

The Acquisition phase begins immediately following the completion of the conversion. During $\overline{CS}$ high, the SDO pin is held in high impedance (high-Z). The falling edge of $\overline{CS}$ defines the sampling instant of the ISL73141SEH, initiates a conversion, and also enables the SDO output to a low state. The conversion cycle is internally timed through an internal oscillator and takes an ensured maximum time of t_{CONV} to complete. Following conversion, several internal blocks are powered down to reduce power consumption. This phase of power-down is referred to as NAP mode. The ISL73141SEH stays in NAP mode until the next rising edge of $\overline{CS}$ where the ISL73141SEH is fully powered up.

The following is an example of timing calculation in an application operating the ISL73141SEHMF7 at 1Msps. When deriving timing it is imperative to use the appropriate maximum and minimum specifications. The $\overline{CS}$ input must be held high for 40ns (t_{CSH}). The time between the falling edge of $\overline{CS}$ and the rising edge of BUSY is a maximum of 30ns (t_{BUSYLH}). The conversion time (t_{CONV}) is a maximum of 660ns. To clock the data out of the ADC there must be 14 rising edges of SCK ($t_{READOUT}$). The 14th SCK falling edge must be coincident with the rising edge of $\overline{CS}$ for the subsequent sample. Using the maximum SCK frequency of 50MHz yields:

$$13 \times 20\text{ns} + 10\text{ns} = 270\text{ns}$$

Note: The 14th SCK edge is coincident with the rising edge of $\overline{CS}$ so there is only a 1/2 period for the 14th SCK. To calculate and validate the sample timing use Equation 1:

(EQ. 1) $$t_{CYC} = t_{CSH} + t_{BUSYLH} + t_{CONV} + t_{READOUT}$$

For a sample rate of 1Msps using the timing calculates to:

$$t_{CYC} = 40\text{ns} + 30\text{ns} + 660\text{ns} + 270\text{ns} = 1000\text{ns}$$

5.4 Convert Start ($\overline{\text{CS}}$) Pin

The convert start input ($\overline{\text{CS}}$) initiates a conversion in the ISL73141SEH. The input logic level of $\overline{\text{CS}}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. A falling edge on this input starts a new conversion. The conversion is timed using an internal oscillator. The logic state of the $\overline{\text{CS}}$ pin controls the state of the SDO pin. A logic high on the $\overline{\text{CS}}$ pin disables the SDO pin driver resulting in a high-impedance state on the SDO pin. A logic low on the $\overline{\text{CS}}$ pin enables the SDO driver (unless $\overline{\text{PD}}$ is low) and allows data to be read out following a conversion.

5.5 Power Down ($\overline{\text{PD}}$) Pin

The ISL73141SEH has a power down pin that is active low ($\overline{\text{PD}}$). When this pin is asserted the ISL73141SEH is powered down to ≤50µW of total power dissipation. If $\overline{\text{PD}}$ is asserted during a conversion, the conversion is halted and the SDO pin is held in high impedance (high-Z). The input logic level of $\overline{\text{PD}}$ is determined by the DV_{CC} supply voltage, which operates across a range of 2.2V up to 3.6V. There is an internal 500kΩ pull-up resistor connected to DV_{CC} on this pin.

5.6 Reference Input (REF) Pin

The ISL73141SEH has a voltage reference input that determines the full scale input range. The input voltage range of this pin is from 1.95V to 3.6V (ISL73141SEHMFN) or 3.9V to 4.2V (ISL73141SEHMF7). Decouple this pin to ground with a high quality, low ESR 10µF ceramic capacitor. Renesas recommends using a capacitor with a voltage rating of 10V or greater and to place the capacitor as close as possible to the REF pin.

Use a low noise, low temperature drift reference to drive this pin. Input noise from the input reference directly impacts the noise performance of the device. Temperature drift of the external reference affects the full scale error for the over-temperature of the device.

5.7 ISL73141 Transfer Function

Figure 56 gives the transfer function of the device. Code transitions in the digital outputs bits of the device occur at midway points between successive integer LSB values that range from 0.5 LSB, 1.5 LSB, 2.5 LSB, 3.5 LSB... and FS - 3.5 LSB, FS - 2.5 LSB, FS - 1.5 LSB, FS - 0.5 LSB. The device is a 14-bit ADC with an output code range in decimal from 0 to 2^N-1 where N = 14, making the total code range 0 to 16383 inclusive.

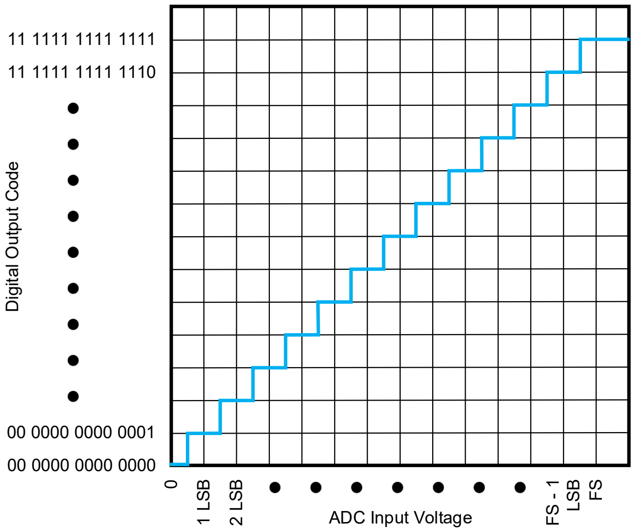


Figure 56. ISL73141SEH Transfer Function

5.8 Power Supply Sequencing

The ISL73141SEH does not have any specific power sequencing requirements when increasing the supply voltages. ***IMPORTANT***: You must follow the guidelines in the recommended operating conditions and take care in observing the maximum supply voltage conditions outlined in the Absolute Maximum Ratings section.

5.9 Analog Input (AIN) Pin

The ISL73141SEH supports single-ended input drive only. ***IMPORTANT***: Ensure that proper grounding techniques and supply decoupling are used in circuit board layout to achieve optimum performance. The ISL73141SEH evaluation board can be used as a guide for proper circuit optimization. The analog input is a high-impedance input that exhibits a capacitive load of approximately 15pF during sample mode and 3pF during hold mode. Due to the high bandwidth (50MHz) of the analog input, Renesas recommends using an Anti-Alias Filter (AAF) appropriate for the desired application. It is not required to operate the ISL73141SEH with an input amplifier, but it can improve performance and/or provide gain in certain applications. An example topology is given in Figure 57, which uses a driver amplifier and an RC input filter. Care must be taken to choose an amplifier with low noise and distortion because the ADC performance is directly impacted. It is also important to choose feedback resistance values that are less than 1kΩ (typically, 100Ω to 200Ω) to minimize the impact of resistor thermal noise. The noise of the resistor is directly related to its value by Equation 2.

(EQ. 2) $$\text{Power Spectral Density (PSD)} = 4kTR\ (V^2/Hz)$$

where

- k = Boltzmans constant (1.38 x 10^{-23})
- T = Temperature in Kelvin (room temperature = 27°C = 300K)
- R = Resistance value

At the input to the ADC, a simple RC filter should be sufficient for most applications. Choose the RC circuit values appropriately for the application. A low-value resistor ($R_S \leq 50$) is recommended for low noise performance. Add a high-quality shunt capacitor (C_P) as close as possible to the AIN pin to shunt charge kickback from the ADC during sampling and to limit the input bandwidth to the ADC. The recommended values for the C_P range is from 220pF to 680pF. Larger values for C_P can be used for slower conversion rates.

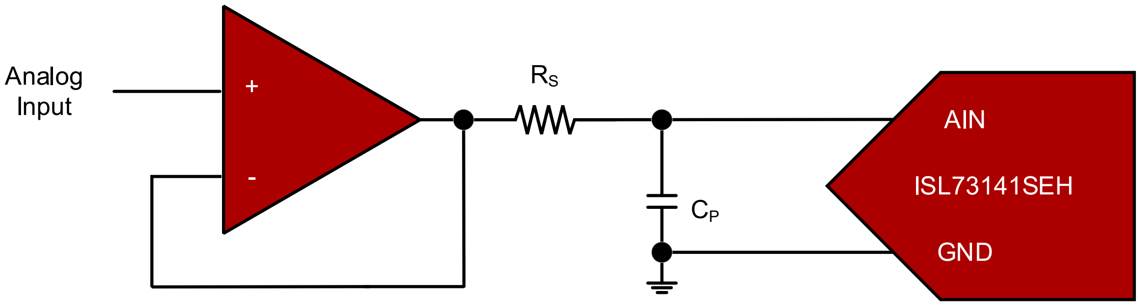


Figure 57. ISL73141SEH Analog Input Amplifier Example Circuit

Due to the switched capacitance of the analog input, Renesas recommends limiting series inductance in the analog input path, particularly the inductance near the analog input pins of the device. Renesas also recommends using a high quality ceramic capacitor (C_P) in shunt on the analog input that is at an appropriate value for the required application. Choose the series resistance in the analog input circuit based on the output impedance of the driver amplifier and the application requirements. An example topology is given in Figure 58, which converts a 0V input common-mode voltage to the ADC input common-mode voltage of $V_{REF}/2$. This circuit is employed on the ISL73141SEH evaluation board to allow the ADC to be driven from various types of signal generators.

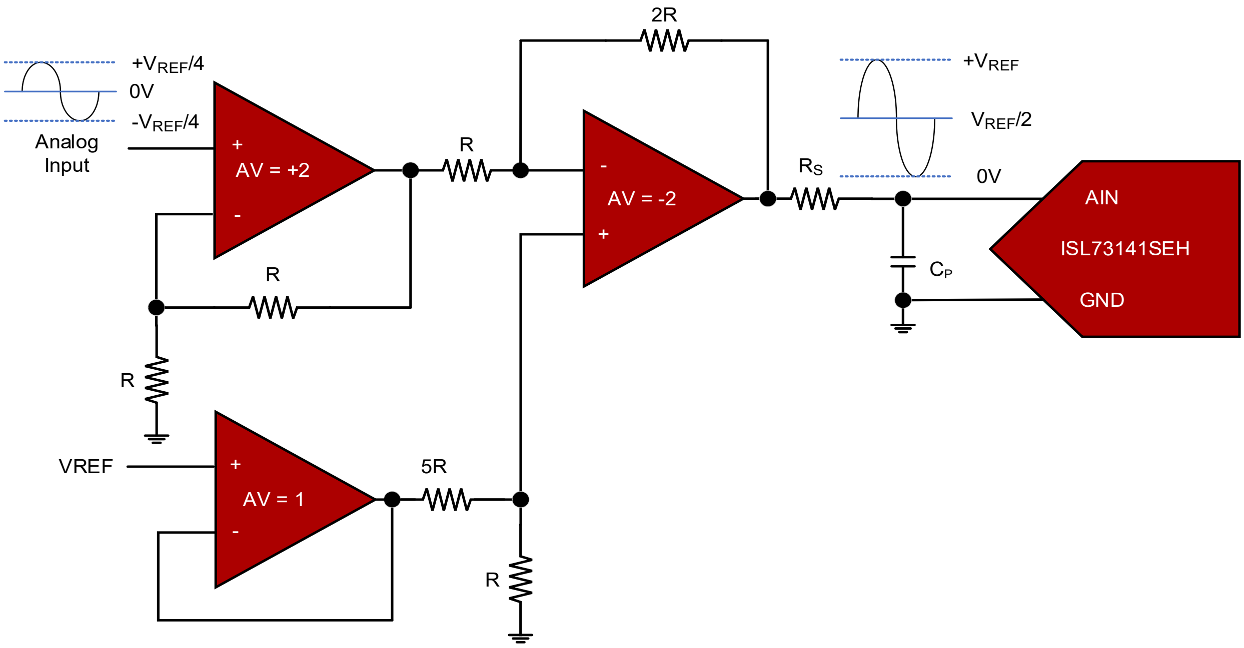


Figure 58. ISL73141SEH Common-Mode Conversion Amplifier Example Circuit

It is important to understand the settling time associated with the analog input of the ISL73141SEH and the impacts of R_S and C_P. To allow the ISL73141SEH to accurately resolve the input signal, it is important that the input signal is settled completely before the signal is sampled by the ISL73141SEH. To meet the datasheet specifications, the settling time must be met for the input signals on the analog input of the ISL73141SEH. To accurately resolve to 1 LSB, the settling time is defined by Equation 3:

(EQ. 3) $$\frac{1}{2^N} = e^{-t/\tau}$$

Simplifying this results in Equation 4:

(EQ. 4) $$\ln(2^N) = -\frac{t}{\tau}$$

Solving for t results in:

$t = -\tau \times \ln(2^N)$, which can be written as $t = N \times \tau \times \ln(2)$ and further simplified to $t = 0.693 \times N \times \tau$.

Settling time is t, $R_S \times C_P$ is τ, and the resolution of the ADC is N.

The ISL73141SEH is a 14-bit ADC, which means the settling time to attain 1 LSB accuracy is $9.7 \times \tau$. For example, the ISL73141SEHEV1Z evaluation board employs a 24Ω resistor for R_S and a 470pF capacitor for C_P, which means that the required settling time would be t = 0.693 × 14 × 24Ω × 470pF = 109.4ns. If different R_S and C_P values are used, calculate the settling time for those conditions. These calculations assume the settling time of the input network R_S and C_P are much larger than the settling time of any amplifier driving the ISL73141SEH analog input. If this is not the case, the settling time of the input network must be root-sum-squared with the settling time of the amplifier to determine the required settling time using Equation 5:

(EQ. 5) $$t = \sqrt{(t_{AMP})^2 + (t_{RC})^2}$$

6. Die and Assembly Characteristics

Table 1. Die and Assembly Related Information

Die Information	
Dimensions	2410µm x 3910µm (95 mils x 154 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Passivation	Oxide/Nitride Total Thickness 24.5 kÅ
Top Metallization	Top metal/Bond Pad Composition 99.5% Al, 0.5%Cu
Process	0.25um CMOS
Assembly Information	
Substrate Potential	GND
Additional Information	
Transistor Count	37700
Weight of Packaged Device	0.572 grams (typical) - K14.A package
Lid Characteristics	Finish: Gold Lid Potential: Connected to package Pin 14 (DGND)

7. Package Outline Drawing

The package outline drawing is located at the end of this document and is accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

8. Ordering Information

Part Number[1]	AV_{CC} Supply Voltage	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	Package Drawing	Carrier Type	Temp Range
ISL73141SEHMFN	3.3V	LDR to 75krad(Si)	14 Ld CDFP Packaged Device (QML-V Level Screening)	K14.A	Tray	-55 to +125°C
ISL73141SEHMF7	5V					
ISL73141SEHFN/PROTO[2]	3.3V	N/A	14 Ld CDFP Packaged Device			
ISL73141SEHF7/PROTO[2]	5V					
ISL73141SEHFNEV1Z[3]	Single IC Evaluation Board for ISL73141SEHMFN					
ISL73141SEHF7EV1Z[3]	Single IC Evaluation Board for ISL73141SEHMF7					

1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO is not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in this datasheet. These part types do not come with a Certificate of Conformance.
3. Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

9. Revision History

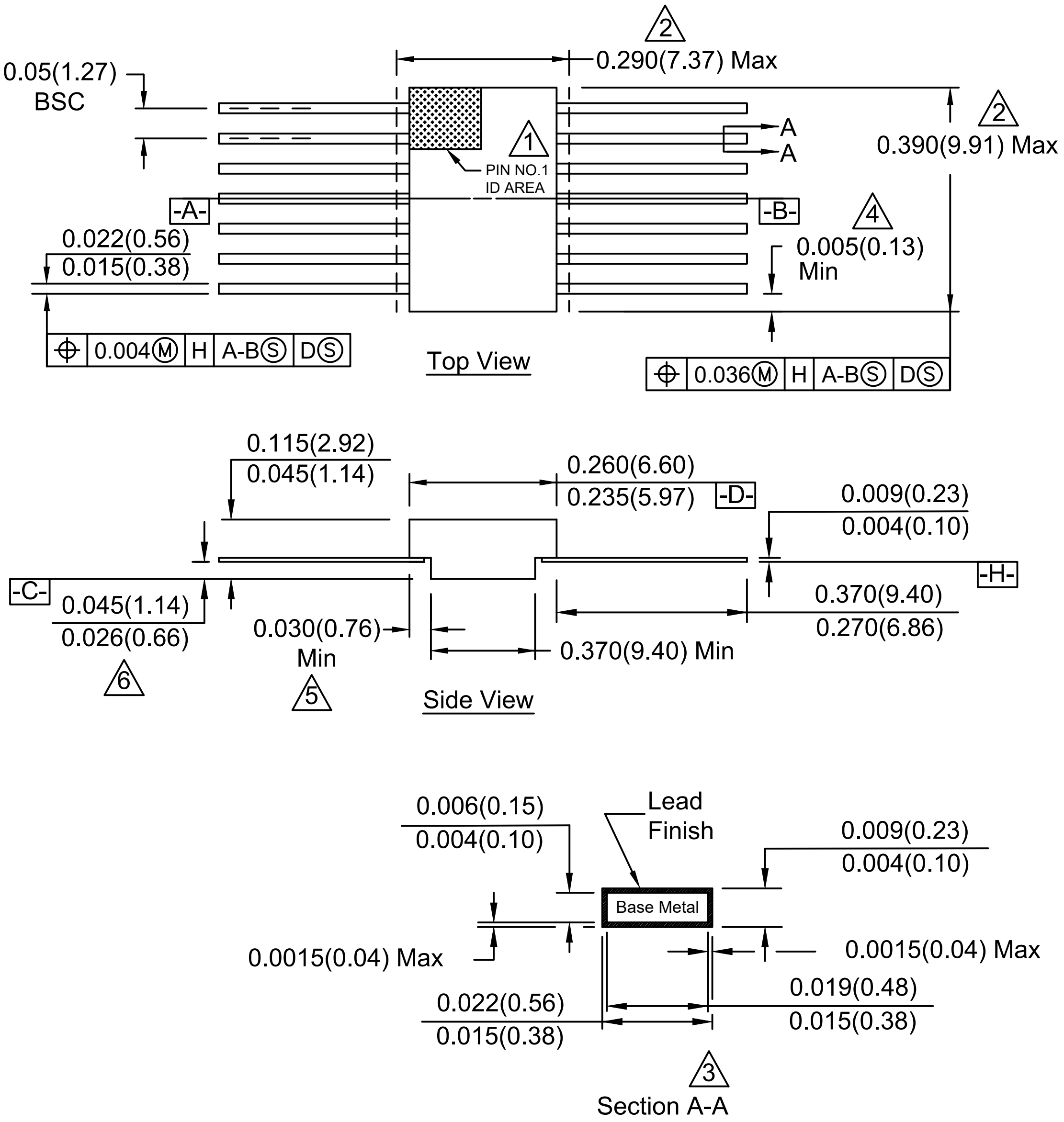
Rev.	Date	Description
5.02	Feb 12, 2025	Updated POD to the latest version; changes are as follows: ▪ Applied latest template ▪ Corrected typo in the mm value for dimension E1 from 7.11 to 7.37mm (i.e. the dim equivalent to E1 from the table in the previous revision) to make it equal to the 0.290 inch dim & compliant to MIL-STD-1835
5.01	Nov 18, 2024	Added AIN Input Current spec and note to Absolute Maximum Ratings section.
5.00	May 1, 2024	Applied new template. Updated Features section. Updated boldface statements for all EC tables.
4.2	Feb 23, 2023	Added Feature bullet. Removed Related Literature. Updated Ordering information table package descriptions.
4.1	Jun 24, 2021	Added the Die and Assembly Characteristics section.
4.0	May 14, 2021	Updated Ordering information table formatting. Updated the SDO Data Valid Delay from SCK↑ specs changed 5V operation maximum from 16ns to 18.5ns and changed 3.3V operation maximum from 24ns to 25n. Updated Figures 5 and 54.
3.1	Jan 28, 2021	Added ESD circuits to the pin description table.

Rev.	Date	Description
3.0	Dec 9, 2020	Corrected typo in the REF pin description by changing the capacitor value from 10F to 10µF. Updated the Effective Number of Bits minimum value on page 7 from 12.8 to 12.5 for 5V specification table. Updated the Analog Supply Current - Active test condition changed from 1MSPS to 750ksps in the 3.3V specification table.
2.0	Oct 21, 2020	Changed Radiation Tolerant to Radiation Hardened in Title and throughout datasheet. Updated 3rd paragraph of description on page 1. Pin Description table: updated pin 3/REF input range. Recommended Operating Conditions and Electrical Spec tables: updated Reference Input Voltage, VREF from 1.5V to: 1.95 for ISL73141SEHMFN) and 3.9V for ISL73141SEHMF7) Updated Figures 18, 19, 20, 42, 43, 44 Reference Input (REF) Pin section, page 22: updated input voltage range
1.0	Sep 1, 2020	Initial release

Package Outline Drawing

14 Lead Ceramic Metal Seal Flatpack

POD No: K14.A, Revision No: 01, Date Created: Jan 28, 2025



Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacture's identification shall not be used as a pin one identification mark.
2. This dimension allows for off-center lid, meniscus, and glass overrun.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. This dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. This dimension's minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Dimensions: Inch(mm). Controlling dimension: INCH.
9. Compliant to MIL-STD-1835 CDFP3-F14 (F-2A, Configuration B).

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2025 Renesas Electronics Corporation. All rights reserved.