ISL78215

Improved Industry Standard Single-Ended Current Mode PWM Controller

FN7673
Rev 1.00
December 7, 2013

The ISL78215 family of adjustable frequency, low power, pulse width modulating (PWM) current mode controllers is designed for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Peak current mode control effectively handles power transients and provides inherent overcurrent protection.

This advanced BiCMOS design is pin compatible with the industry standard 384x family of controllers and offers significantly improved performance. Features include low operating current, 60µA start-up current, adjustable operating frequency to 2MHz, and high peak current drive capability with 20ns rise and fall times.

The ISL78215 is tested to AEC-Q100 specifications.

Features

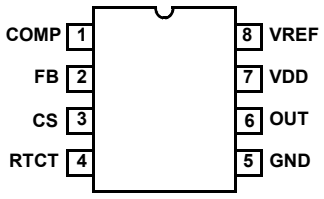
- 1A MOSFET Gate Driver
- 60µA Start-up Current, 100µA Maximum
- 25ns Propagation Delay Current Sense to Output
- Fast Transient Response with Peak Current Mode Control
- Adjustable Switching Frequency to 2MHz
- 20ns Rise and Fall Times with 1nF Output Load
- Trimmed Timing Capacitor Discharge Current for Accurate Deadtime/Maximum Duty Cycle Control
- High Bandwidth Error Amplifier
- Tight Tolerance Voltage Reference Over Line, Load, and Temperature
- Tight Tolerance Current Limit Threshold
- Pb-Free (RoHS Compliant)
- AEC-Q100 Tested

Applications

- Automotive Power
- Telecom and Datacom Power
- Wireless Base Station Power
- File Server Power
- Industrial Power Systems
- PC Power Supplies
- Isolated Buck and Flyback Regulators
- Boost Regulators

Pin Configuration

ISL78215
(8 LD MSOP)
TOP VIEW



Pin Description

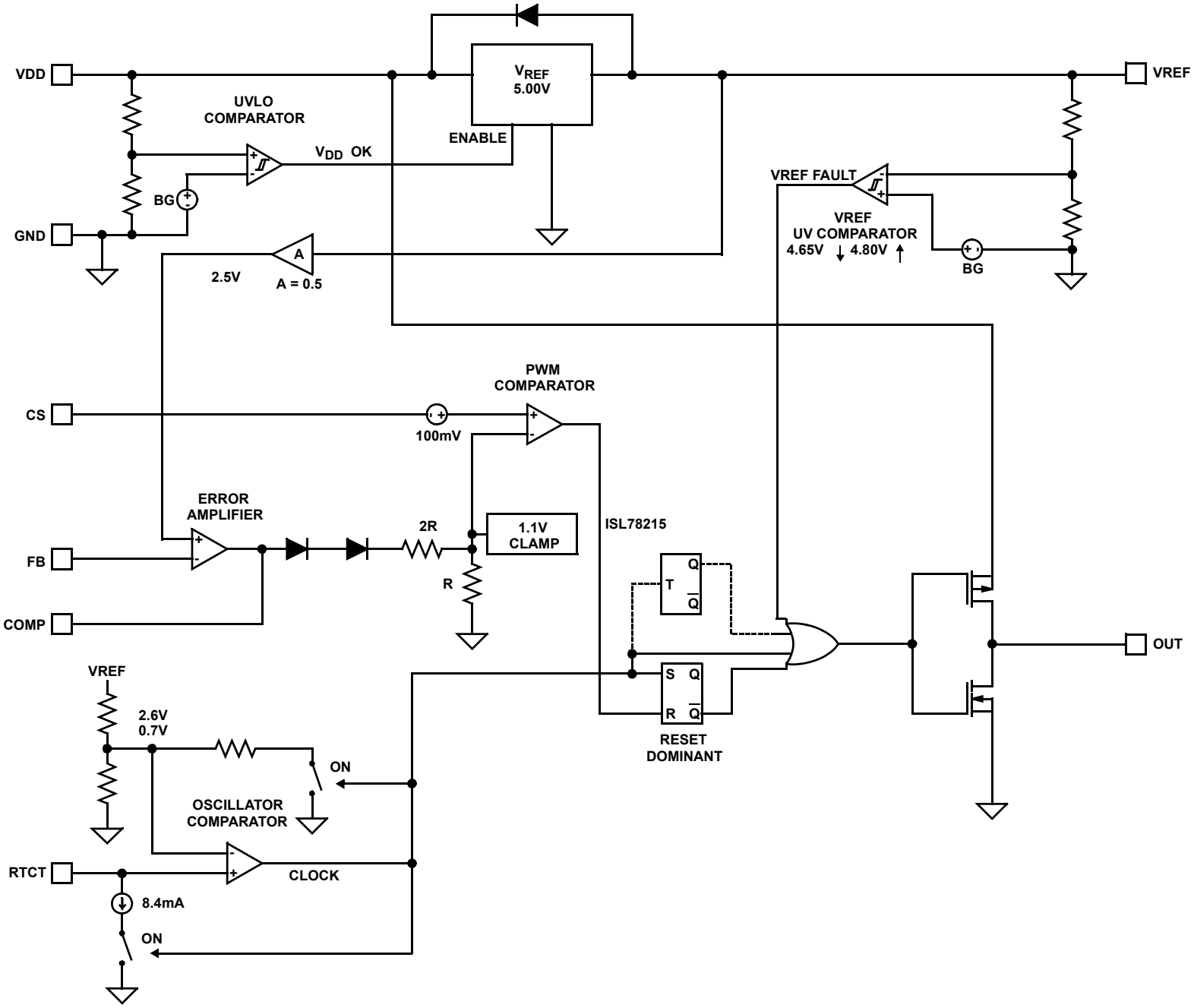
PIN	SYMBOL	DESCRIPTION
1	COMP	COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.
2	FB	The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The non-inverting input of the error amplifier is internally tied to a reference voltage.
3	CS	This is the current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.
4	RTCT	This is the oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, tC, the discharge time, tD, the switching frequency, f, and the maximum duty cycle, Dmax, can be calculated from Equations 1, 2, 3 and 4: $t_C \approx 0.583 \bullet RT \bullet CT$ (EQ. 1) $t_D \approx -RT \bullet CT \bullet \ln\left(\frac{0.0083 \bullet RT - 4.3}{0.0083 \bullet RT - 2.4}\right)$ (EQ. 2) $f = 1/(t_C + t_D)$ (EQ. 3) $D = t_C \bullet f$ (EQ. 4) Figure 4 may be used as a guideline in selecting the capacitor and resistor values required for a given frequency.
5	GND	GND is the power and small signal reference ground for all functions.
6	OUT	This is the drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A.
7	VDD	VDD is the power connection for the device. The total supply current will depend on the load applied to OUT. Total IDD current is the sum of the operating current and the average output current. Knowing the operating frequency, f, and the MOSFET gate charge, Qg, the average output current can be calculated in Equation 5: $I_{OUT} = Qg \times f$ (EQ. 5) To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.
8	VREF	The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. Bypass to GND with a 0.1µF to 3.3µF capacitor to filter this output as needed.

Ordering Information

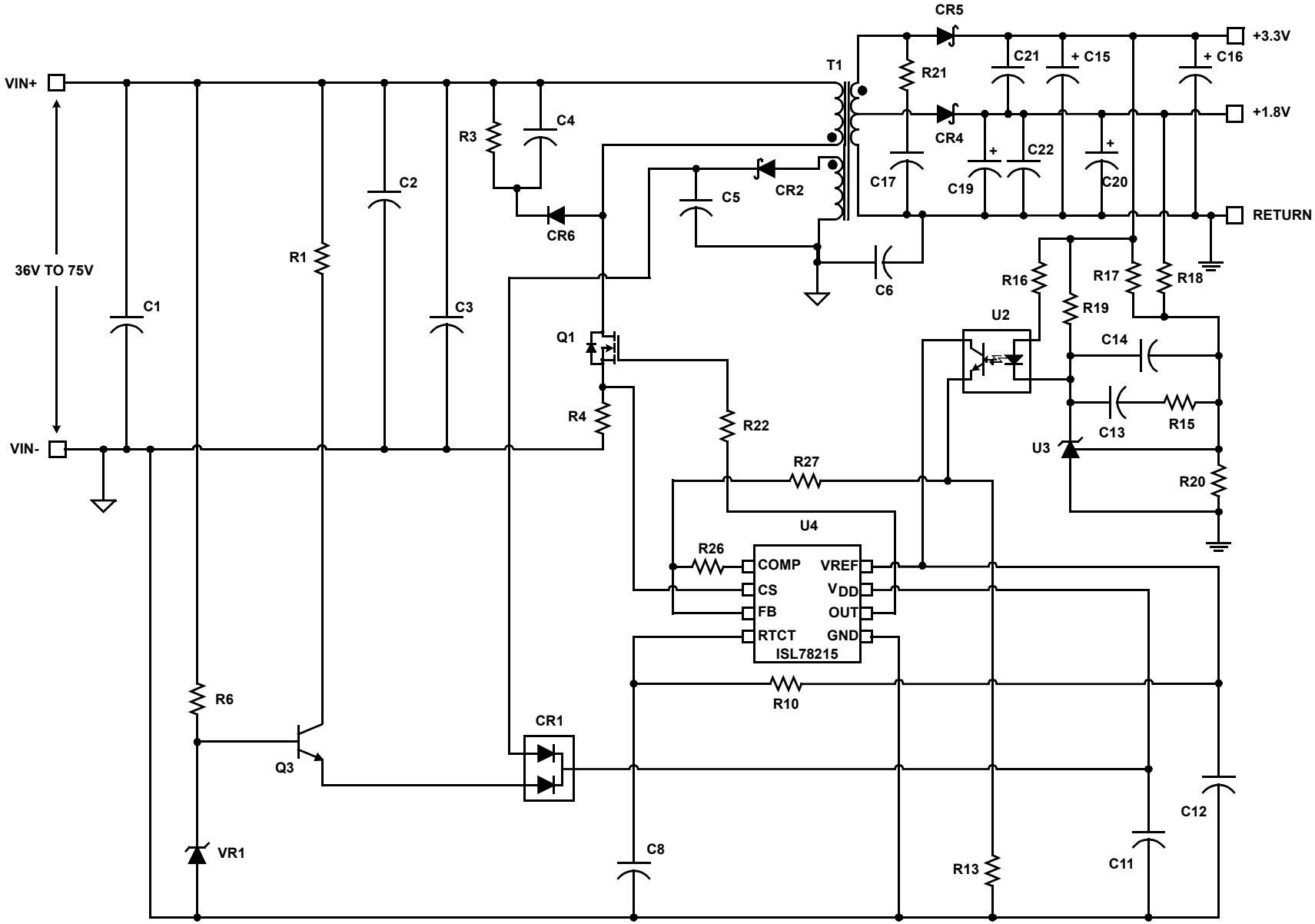
PART NUMBER (Notes 2, 3)	PART MARKING	TEMP RANGE (°C)	PACKAGE (Pb-free)	PKG. DWG. #
ISL78215AUZ	78215	-40 to +105	8 Ld MSOP	M8.118
ISL78215AUZ-T (Note 1)	78215	-40 to +105	8 Ld MSOP	M8.118

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL78215. For more information on MSL please see techbrief TB363.

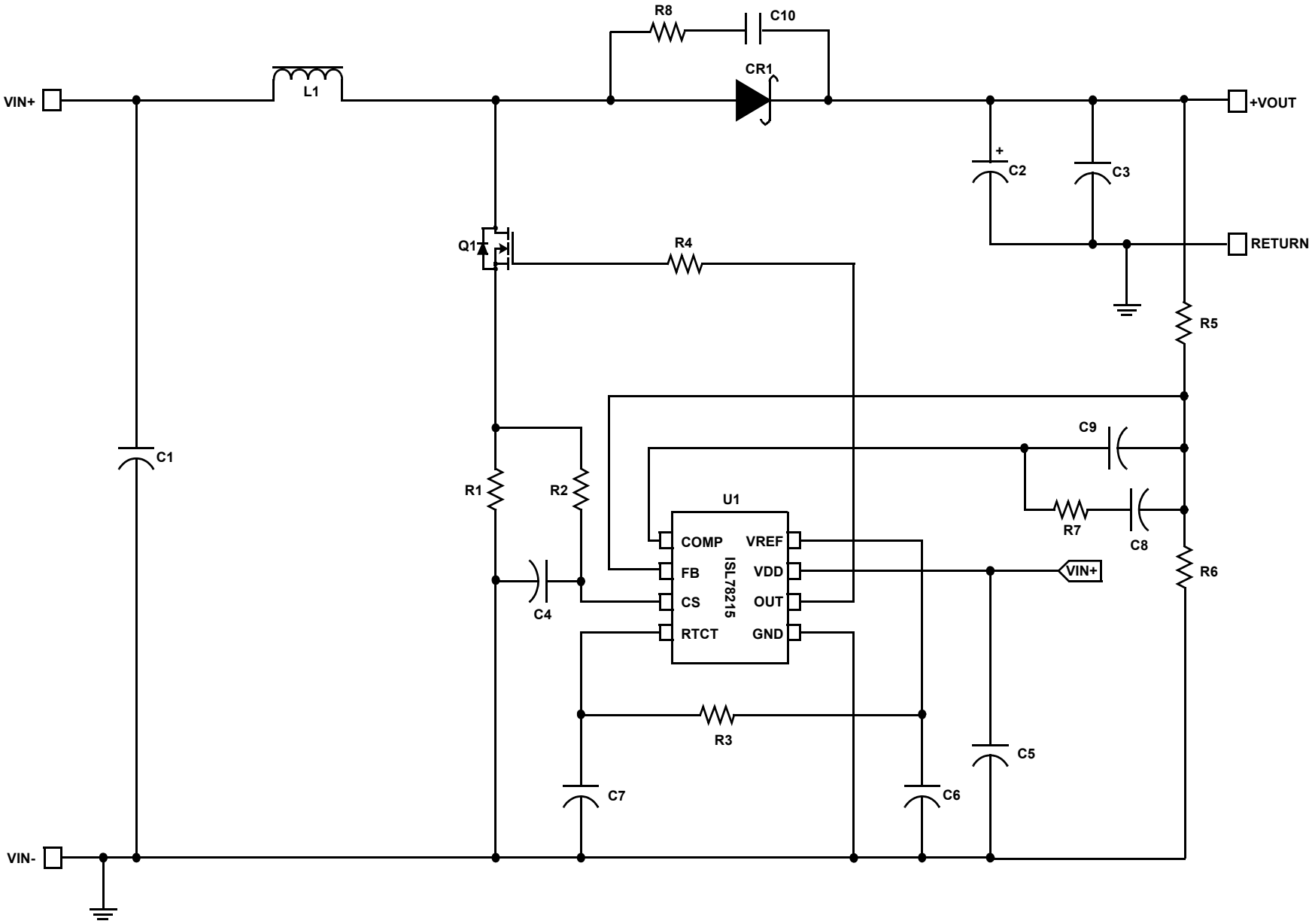
Functional Block Diagram



Typical Application - 48V Input Dual Output Flyback



Typical Application - Boost Converter



Absolute Maximum Ratings

Supply Voltage, V_{DD} . . . . . GND - 0.3V to +20.0V
OUT . . . . . GND - 0.3V to V_{DD} + 0.3V
Signal Pins . . . . . GND - 0.3V to 6.0V
Peak GATE Current 1A
ESD Rating
Human Body Model (Tested per JESD22-A11) 2500V
Machine Model (Tested per JESD22-C101) 75V
Charged Device Model (Tested per JESD22-A115) 1500V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
MSOP Package (Notes 4, 5)	170	60

Maximum Junction Temperature . . . . . -55°C to +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Operating Conditions

Temperature Range . . . . . -40°C to +105°C
Supply Voltage Range (Typical, Note 6) . . . . . 7.5V to 18V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
5. For θ_{JC}, the "case temp" location is taken at the package top center.
6. All voltages are with respect to GND.

Electrical Specifications

Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 3 and "Typical Application" schematics on page 4 and 5. V_{DD} = 15V (Note 10), R_t = 10kΩ, C_t = 3.3nF, T_A = -40 to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
UNDERVOLTAGE LOCKOUT					
START Threshold		**6.5**	7.0	**7.5**	V
STOP Threshold		**6.1**	6.6	**6.9**	V
Hysteresis		-	0.4	-	V
Start-up Current, I_{DD}	V_{DD} < START Threshold	-	60	**100**	µA
Operating Current, I_{DD}	(Note 8)	-	3.3	**4.0**	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.1	**5.5**	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line (V_{DD} = 12V to 18V), load, temperature	**4.925**	5.000	**5.050**	V
Long Term Stability	T_A = +125°C, 1000 hours (Note 9)	-	5	-	mV
Fault Voltage		**4.40**	4.65	**4.85**	V
VREF Good Voltage		**4.60**	4.80	**VREF - 0.05**	V
Hysteresis		**50**	165	**250**	mV
Current Limit, Sourcing		**-20**	-	-	mA
Current Limit, Sinking		**5**	-	-	mA
CURRENT SENSE					
Input Bias Current	V_{CS} = 1V	**-1.0**	-	**1.0**	µA
CS Offset Voltage	V_{CS} = 0V (Note 9)	**95**	100	**105**	mV
COMP to PWM Comparator Offset Voltage	V_{CS} = 0V (Note 9)	**0.80**	1.15	**1.30**	V
Input Signal, Maximum		**0.91**	0.97	**1.03**	V
Gain, $A_{CS} = \Delta V_{COMP}/\Delta V_{CS}$	0 < V_{CS} < 910mV, V_{FB} = 0V (Note 9)	**2.5**	3.0	**3.5**	V/V
CS to OUT Delay	(Note 9)	-	25	**40**	ns

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to "Functional Block Diagram" on page 3 and "Typical Application" schematics on page 4 and 5. V_{DD} = 15V (Note 10), R_t = 10kΩ, C_t = 3.3nF, T_A = -40 to +105°C, Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +105°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 7)	TYP	MAX (Note 7)	UNITS
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 9)	**60**	90	-	dB
Unity Gain Bandwidth	(Note 9)	**3.5**	5	-	MHz
Reference Voltage	$V_{FB} = V_{COMP}$	**2.475**	2.514	**2.55**	V
FB Input Bias Current	V_{FB} = 0V	**-1.0**	-0.2	**1.0**	µA
COMP Sink Current	V_{COMP} = 1.5V, V_{FB} = 2.7V	**1.0**	-	-	mA
COMP Source Current	V_{COMP} = 1.5V, V_{FB} = 2.3V	**-0.4**	-	-	mA
COMP VOH	V_{FB} = 2.3V	**4.80**	-	**VREF**	V
COMP VOL	V_{FB} = 2.7V	**0.4**	-	**1.0**	V
PSRR	Frequency = 120Hz, V_{DD} = 12V to 18V (Note 9)	**60**	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, T_J = +25°C	**49**	52	**55**	kHz
Frequency Variation with V_{DD}	T = +25°C ($f_{18V} - f_{12V}$)/f_{12V}	-	0.2	1.0	%
Temperature Stability	(Note 9)	-	-	**5**	%
Amplitude, Peak-to-Peak		-	1.9	-	V
RTCT Discharge Voltage		-	0.7	-	V
Discharge Current	RTCT = 2.0V	**7.2**	8.4	**9.5**	mA
OUTPUT					
Gate VOH	V_{DD} to OUT, I_{OUT} = -200mA	-	1.0	**2.0**	V
Gate VOL	OUT to GND, I_{OUT} = 200mA	-	1.0	**2.0**	V
Peak Output Current	C_{OUT} = 1nF (Note 9)	-	1.0	-	A
Rise Time	C_{OUT} = 1nF (Note 9)	-	20	**40**	ns
Fall Time	C_{OUT} = 1nF (Note 9)	-	20	**40**	ns
PWM					
Maximum Duty Cycle		**47**	48		%
Minimum Duty Cycle		-	-	0	%

NOTES:

7. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
8. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
9. Limits established by characterization and are not production tested.
10. Adjust V_{DD} above the start threshold and then lower to 15V.

Typical Performance Curves

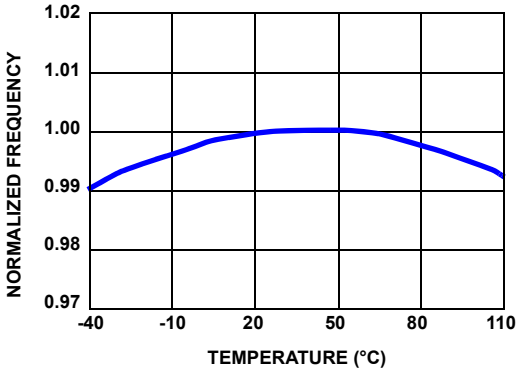


FIGURE 1. FREQUENCY vs TEMPERATURE

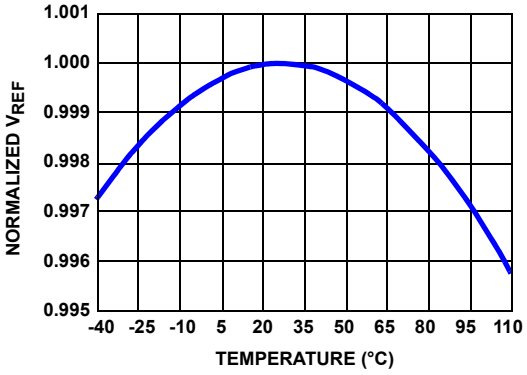


FIGURE 2. REFERENCE VOLTAGE vs TEMPERATURE

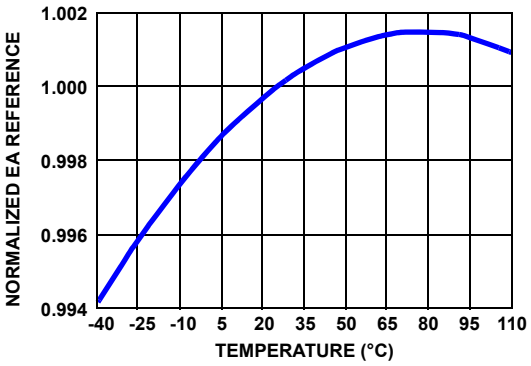


FIGURE 3. EA REFERENCE vs TEMPERATURE

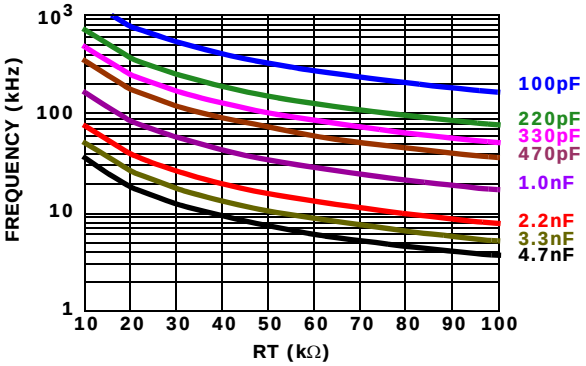


FIGURE 4. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Functional Description

Features

The ISL78215 current mode PWMs make an ideal choice for low-cost flyback and forward topology applications. With its greatly improved performance over industry standard parts, it is the obvious choice for new designs or existing designs which require updating.

Oscillator

The ISL78215 controllers have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from VREF and a capacitor to GND on the RTCT pin. (Please refer to Figure 4 for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated in Figure 5, clamps the voltage on COMP.

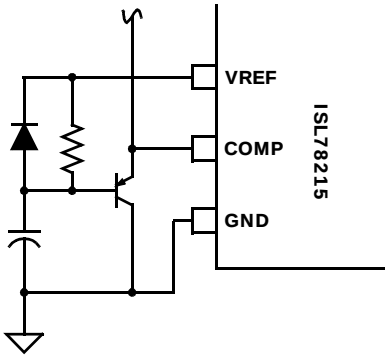


FIGURE 5. SOFT-START

Gate Drive

The ISL78215 is capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FET's input capacitance.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability. The minimum amount of slope compensation required corresponds to 1/2 the inductor downslope. Adding excessive slope compensation, however, results in a control loop that behaves more as a voltage mode controller than as a current mode controller.

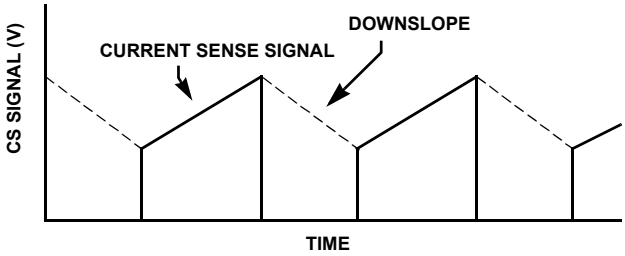


FIGURE 6. CURRENT SENSE DOWNSLOPE

Slope compensation may be added to the CS signal shown in Figure 7.

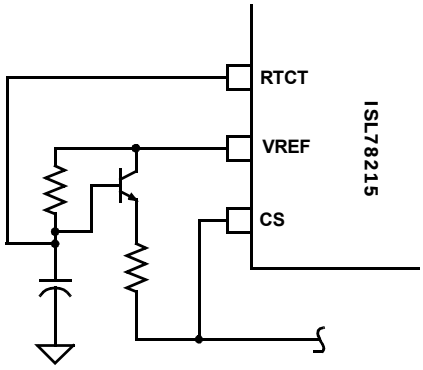


FIGURE 7. SLOPE COMPENSATION

Fault Conditions

A Fault condition occurs if VREF falls below 4.65V. When a Fault is detected, OUT is disabled. When VREF exceeds 4.80V, the Fault condition clears, and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
December 7, 2013	FN7673.1	Updated to newest template Page 1 - updated copyright information Page 10 - 2nd line of the disclaimer changed from: “Intersil products are manufactured, assembled and tested utilizing ISO9001 quality systems as noted” to: “Intersil Automotive Qualified products are manufactured, assembled and tested utilizing TS16949 quality systems as noted” Page 11 - updated M8.118 to newest rev .4: Changes from ref .3: Corrected lead width dimension in side view 1 from "0.25 - 0.036" to "0.25 - 0.36"
August, 16, 2010	FN7673.0	Initial Release.

About Intersil

Intersil Corporation is a leader in the design and manufacture of high-performance analog, mixed-signal and power management semiconductors. The company's products address some of the largest markets within the industrial and infrastructure, personal computing and high-end consumer markets. For more information about Intersil, visit our website at www.intersil.com.

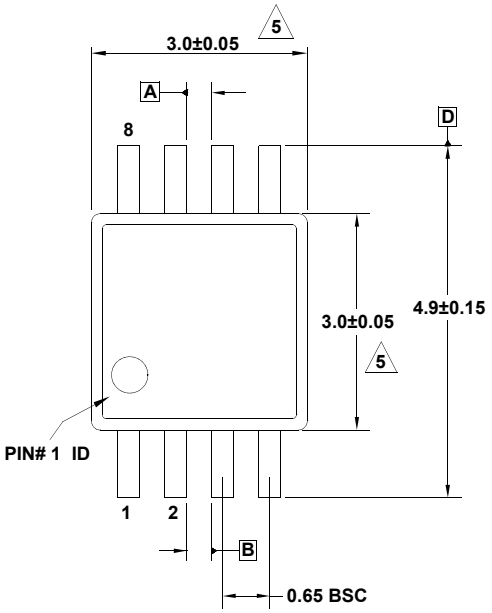
For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com. You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/en/support/ask-an-expert.html. Reliability reports are also available from our website at http://www.intersil.com/en/support/qualandreliability.html#reliability

Package Outline Drawing

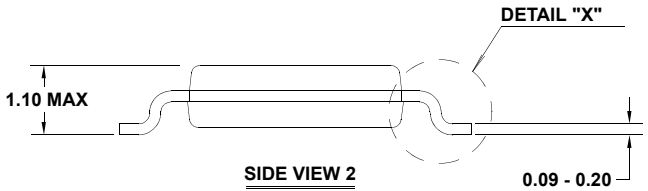
M8.118

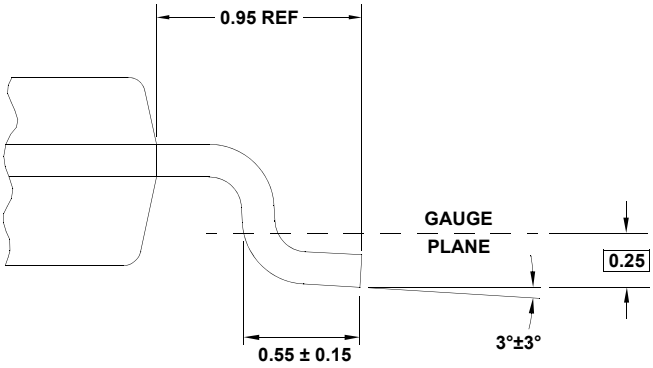
8 LEAD MINI SMALL OUTLINE PLASTIC PACKAGE

Rev 4, 7/11

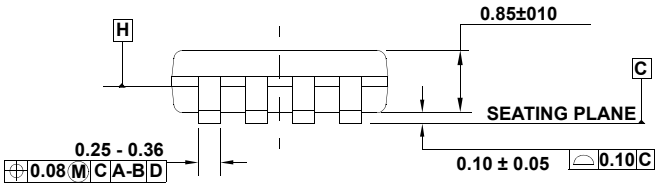


TOP VIEW

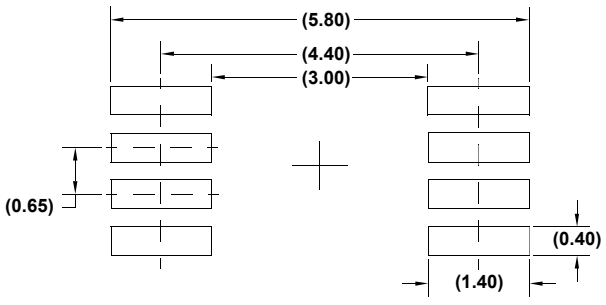




DETAIL "X"



SIDE VIEW 1



TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensions are in millimeters.
2. Dimensioning and tolerancing conform to JEDEC MO-187-AA and AMSEY14.5m-1994.
3. Plastic or metal protrusions of 0.15mm max per side are not included.
4. Plastic interlead protrusions of 0.15mm max per side are not included.
5. Dimensions are measured at Datum Plane "H".
6. Dimensions in ( ) are for reference only.