ISL81100

100V Synchronous Buck Controller

Description

The ISL81100 is a synchronous buck controller that generates a stepped-down output for various applications in industrial and general-purpose segments. Its wide input and output voltage ranges make it suitable for telecommunication, data center, and computing applications.

The ISL81100 uses fixed frequency peak current mode PWM control. It has a voltage regulator, current monitor, and average current regulator to provide independent average voltage and current control. The internal oscillator is adjustable from 100kHz to 2MHz and can be synchronized to an external clock signal for frequency synchronization and phase interleaving applications. It can also support accurate, current sharing for parallel applications.

The ISL81100 offers programmable soft-start, accurate threshold enable functions, and a power-good indicator for ease of supply rail sequencing requirements. It also provides complete protection features such as OVP, VIN_UVLO, OTP, average and peak current limits in a forward direction, and negative peak current limits in a reverse direction to ensure high reliability. The IC is available in a space-conscious 25 Ld 5mm x5mm TQFN package. This package uses an EPAD to improve thermal dissipation and noise immunity. The complete feature design with low pin count makes the ISL81100 ideal for quick-to-market simple power supply designs.

Features

- Wide input voltage range: 4.5V to 100V
- Wide output voltage range: 0.8V to 96V
- Two MOSFET drivers with adaptive shoot-through protection
- Constant output voltage and output current feedback loop control
- Light-load efficiency enhancement
  - Low ripple diode emulation mode operation
- Programmable soft-start
- Supports pre-biased output with SR soft-start
- Programmable frequency: 100kHz to 2MHz
- Support current sharing
- External clock sync
- PGOOD indicator
- Output current monitor
- Selectable mode between PWM/DEM
- Accurate VIN_UVLO threshold: ±3%
- Low shutdown current: 4µA
- Complete protection: OCP (pulse by pulse and optional hiccup or constant current mode), negative peak current limit, OVP, OTP, and UVP

Applications

- Telecommunication
- Server and data center
- Automotive electronics
- Industrial equipment
- Power system

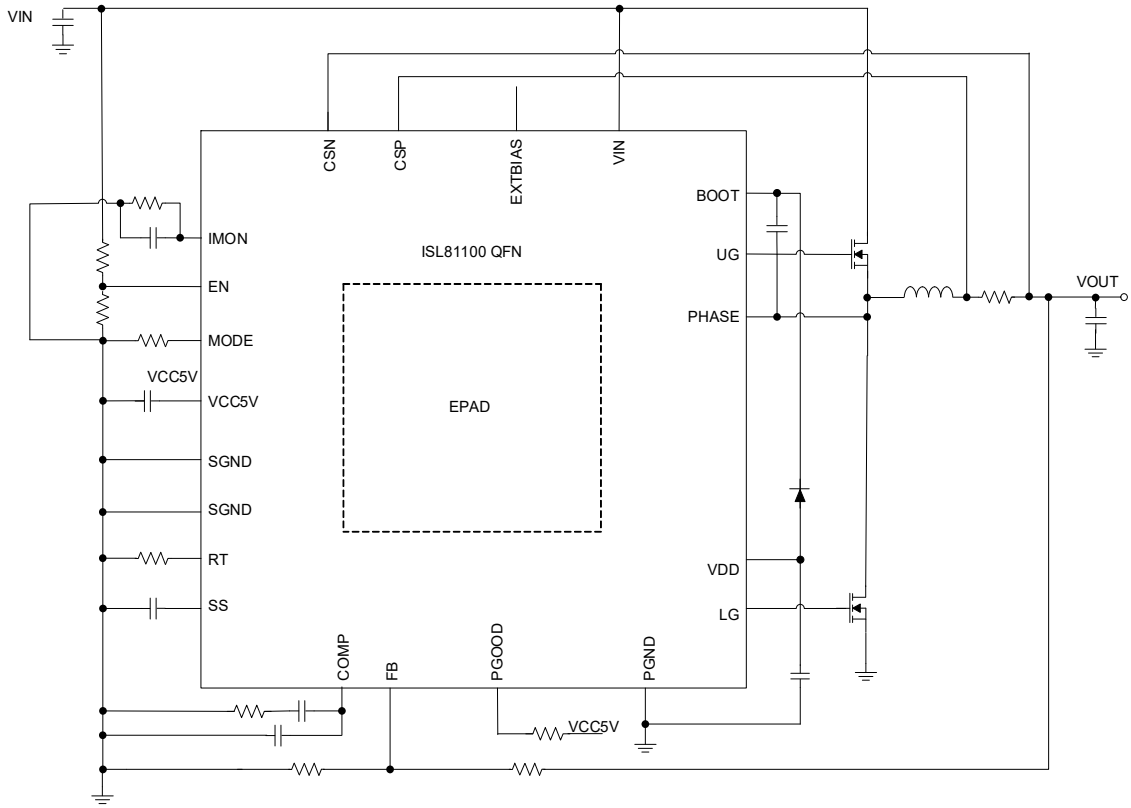

Figure 1. Typical Application Diagramss

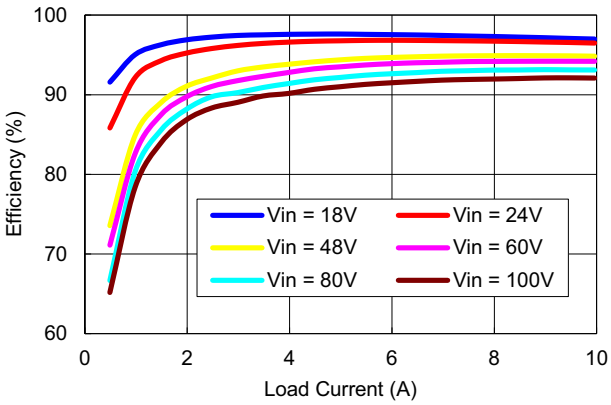

Figure 2. Efficiency (V_{OUT} = 12V, Forced PWM)

Contents

1. Overview

1.1 Typical Application Schematics

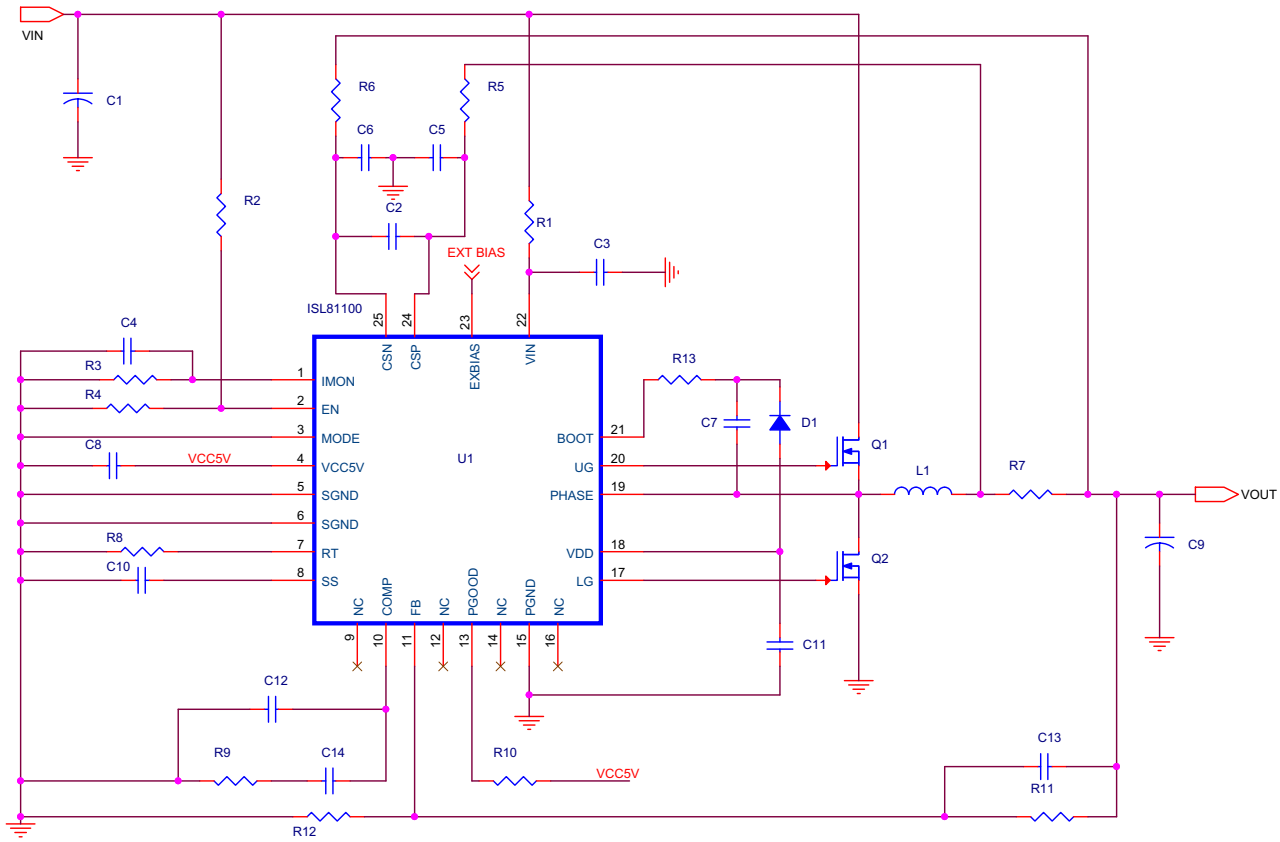

Figure 3. ISL81100EVAL1Z (V_{IN} = 18V to 100V, V_{OUT} = 12V, I_{OUT} = 10A) Evaluation Board Schematic

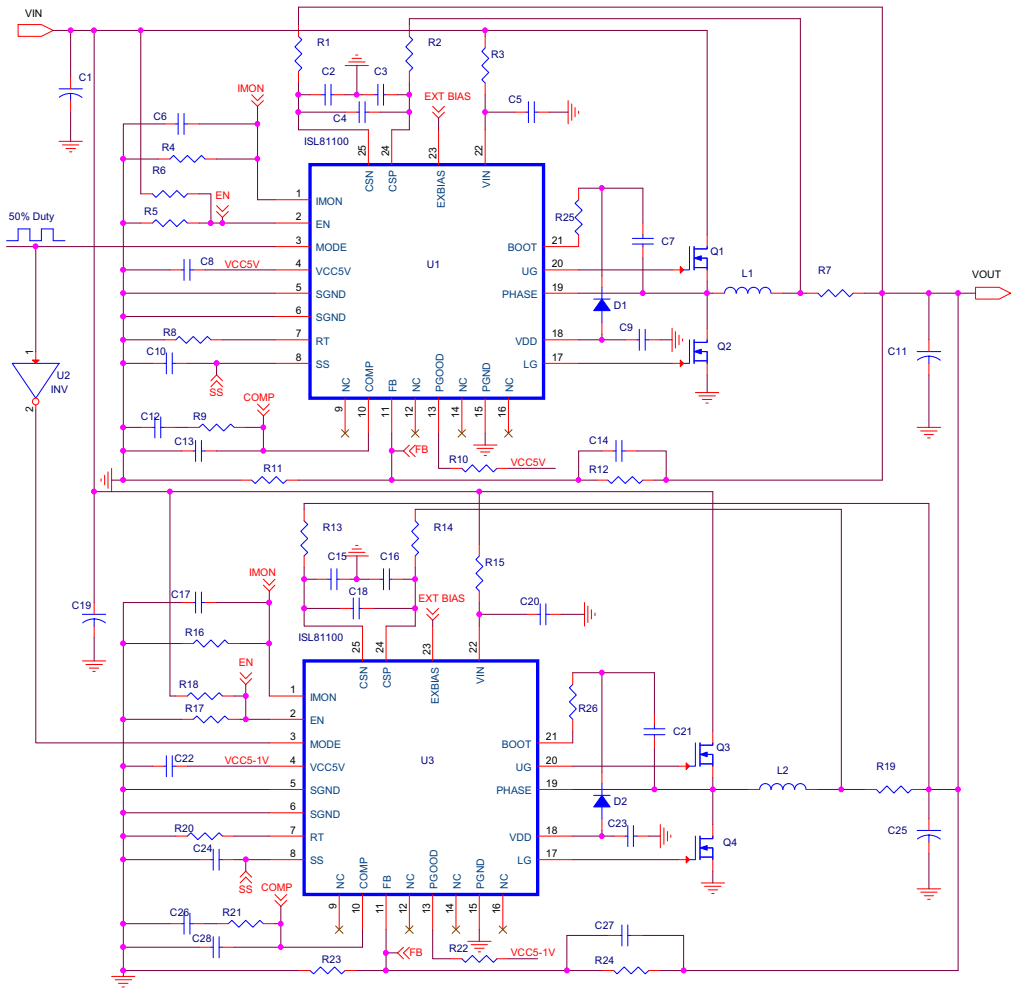

Figure 4. ISL81100EVAL2Z (V_{IN} = 18V to 100V, V_{OUT} = 12V, I_{OUT} = 20A) Parallel Operation Schematic

1.2 Block Diagram

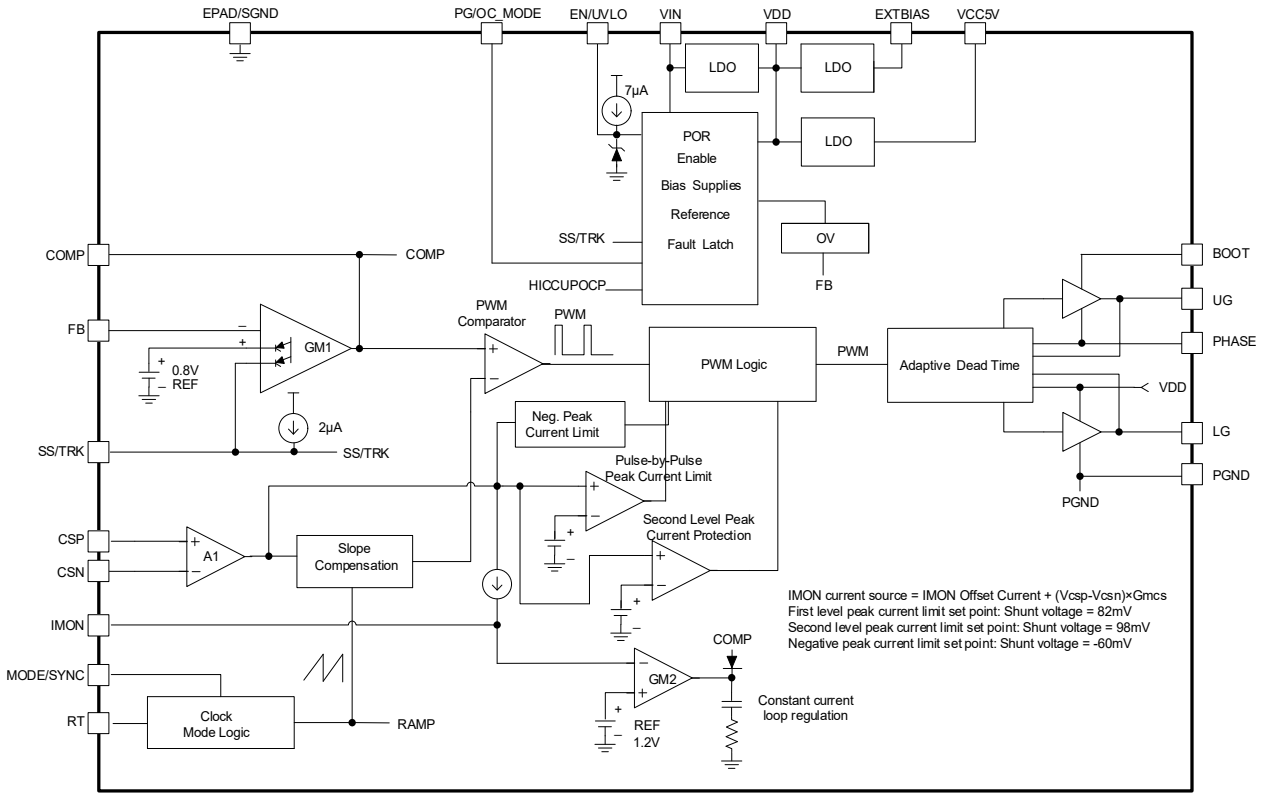

Figure 5. Block Diagram

2. Pin Information

2.1 Pin Assignments

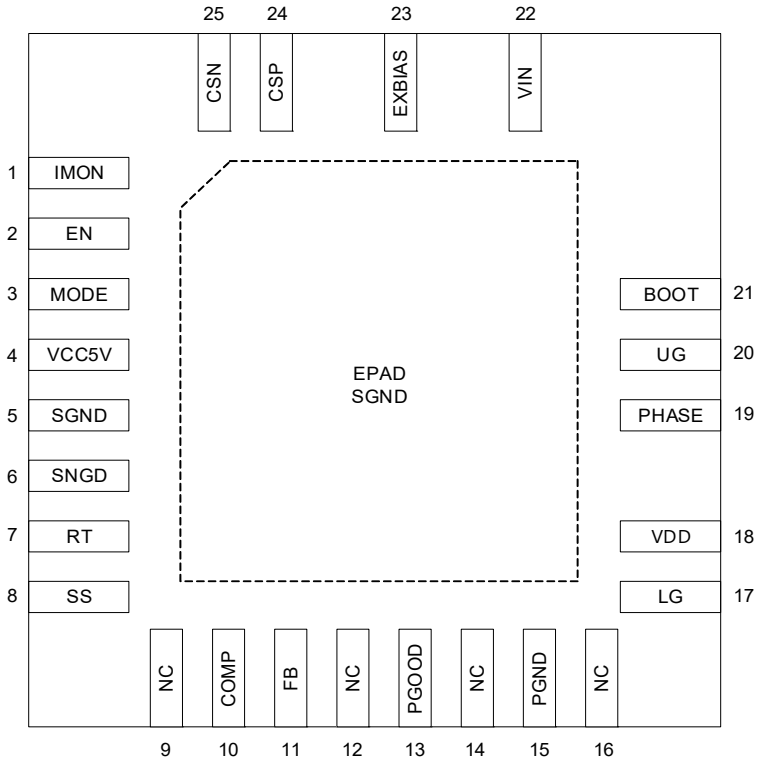

Figure 6. Pin Assignments - Top View

2.2 Pin Descriptions

Pin #	Pin Name	Function
1	IMON	Output current monitor. The current from this pin is proportional to the differential voltage between the CSP and CSN pins. Connect a resistor and capacitor network between the pin and SGND to make the pin voltage proportional to the average output current. When the pin voltage reaches 1.2V, the internal average current limit loop reduces the output voltage to keep the output current constant when constant current OCP mode is set by PG/OC_MODE pin.
2	EN/UVLO	The EN/UVLO pin provides an enable/disable to the IC and accurate UVLO function. The output is disabled when the pin is pulled to ground. When the voltage on the pin reaches 1.05V, the VDD and VCC5V LDOs become active. When the voltage on the pin reaches 1.8V, the PWM modulator is enabled. When the pin is floating, it is enabled by default by an internal pull-up.
3	MODE/ SYNC	Dual function pin. Connect this pin to an external clock for synchronization. When synchronized with an external clock, the controller operates in PWM Mode at light load. The converter is set to Forced PWM mode if the pin voltage is less than 0.8V. The converter is set to DEM mode if the pin voltage is higher than 0.8V and less than 3.8V.
4	VCC5V	The output of the internal 5V linear regulator. This output supplies bias for the IC. The VCC5V pin must always be decoupled to SGND ground with a minimum 4.7µF ceramic capacitor placed close to the pin.
5, 6	SGND	SGND

Pin #	Pin Name	Function
7	RT	A resistor from this pin to ground adjusts the switching frequency from 100kHz to 2MHz. The switching frequency of the PWM controller is determined by the resistor, R_T, as shown in Equation 1, where f_{SW} is the switching frequency in MHz. **(EQ. 1)** $R_T = \left(\frac{44}{f_{SW}} - 7.5\right) \times k\Omega$ When this pin is tied to ground, the output frequency is 520kHz. When this pin is tied to VCC5V or floating, the output frequency is 110kHz.
8	SS/TRK	Soft-start or track control pin. A soft-start capacitor is connected from this pin to ground when used for soft-start control. A regulated 2µA soft-starting current charges up the soft-start capacitor. The value of the soft-start capacitor sets the output voltage ramp. When used for tracking control, an external supply rail is configured as the master, and the output voltage of the master supply is applied to this pin using a resistor divider. The output voltage tracks the master supply voltage.
9, 12, 14, 16	NC	Not Connected.
10	COMP	Voltage error GM amplifier output. It sets the reference of the inner current loop. The feedback compensation network is connected between the COMP and SGND pins. When the COMP pin is pulled below 1.2V, the PWM duty cycle reduces to 0%.
11	FB	Output voltage feedback input pin. Connect FB to a resistive voltage divider from the output to SGND to adjust the output voltage. The FB pin voltage is regulated to the internal 0.8V reference. After the soft-start is done, when FB < 0.1V, the output UVP is triggered. The converter shuts down. After 50ms, the converter starts up again.
13	PG/OC_MODE	The open-drain logic output indicates the status of output voltage and OCP mode set pin. This pin is pulled down when the output is not within +12.5% -15% of the nominal voltage or the EN pin is pulled LOW. The OCP mode is set by a pull-up resistor connected from the pin to a fixed voltage during the initiation stage before soft-start. The pin would sink current through the pull-up resistor during the initiation stage. If the current into the pin is higher than 190µA, the converter is set to stand-alone constant current limit OCP mode. If the current into the pin is more than 60µA and less than 190µA, the converter is set to current sharing constant current limit OCP mode for multiple ISL81100 parallel operations. If the current into the pin is less than 60µA, the converter is set to stand-alone hiccup OCP mode.
15	PGND	Power ground connection. This pin should be connected to the sources of the lower MOSFETs and the (-) terminals of the external input capacitors.
17	LG	Low-side MOSFET gate driver output is controlled by the PWM signal.
18	VDD	The output of the internal 8V linear regulator is supplied by either VIN or EXTBIAS. This output supplies bias for the IC low-side drivers and the boot circuitries for the high-side drivers. The VDD pin must always be decoupled to SGND ground with a minimum 4.7µF ceramic capacitor placed very close to the pin. Do not allow the voltage at VDD to exceed VIN at any time.
19	PHASE	Phase node connection of the buck converter. This pin is connected to the junction of the upper MOSFET source, filter inductor, and lower MOSFET drain of the converter.
20	UG	High-side MOSFET gate driver output is controlled by the PWM signal.
21	BOOT	Bootstrap pin that provides bias for the high-side driver. The positive terminal of the bootstrap capacitor connects to this pin. An external bootstrap diode between boot cap and VDD creates a bias for the high-side driver. A boot resistor from boot cap to the boot pin is required for noise reduction. When the BOOT to PHASE voltage drops to less than 5.4V, LG is forced high for 300ns to maintain the high-side bias voltage.
22	VIN	This pin should be tied to the input rail. It provides power to the internal LDO for VDD. Decouple this pin with a small ceramic capacitor (0.1µF to 1µF) to ground.
23	EXTBIAS	External bias input for the optional VDD LDO. An internal switch disconnects the VIN LDO when the EXTBIAS voltage is higher than 7.6V. When the EXTBIAS voltage is lower than 6.6V, switch back VIN to LDO. Decouple this pin to ground with a small ceramic capacitor (0.1µF to 1µF) when used; otherwise, tie this pin to ground. DO NOT float this pin.
24	CSP	Output current sense signal positive input pin.
25	CSN	Output current sense signal negative input pin.
EPAD	EPAD SGND	EPAD at ground potential. EPAD is connected to SGND internally. However, Renesas highly recommends soldering it directly to the ground plane for better thermal performance and noise immunity. This is the small-signal ground common to all control circuitry. Renesas recommends routing this separately from the high current ground (PGND). SGND and PGND can be tied together if one solid ground plane has no noisy currents around the chip. All voltage levels are measured with respect to this pin.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VCC5V, EN/UVLO	-0.3	+5.9	V
VDD to GND	-0.3	+9	V
EXTBIAS to GND	-0.3	+40	V
VIN	-0.3	+105	V
CSP, CSN to GND	-0.3	+105	V
BOOT, UG to PHASE	-1	+12	V
BOOT to GND	0	+120	V
PHASE to GND[1]	-4(<20ns)/ -1 (DC)	+105	V
FB, SS/TRK, COMP, RT, MODE/SYNC, PG/OC_MODE, IMON to GND	-0.3	VCC5V + 0.3	V
LG to GND	-0.3	V_{DD} + 0.3	V
CSP to CSN	-0.3	+0.3	V
VCC5V, VDD Short-Circuit to GND Duration	-	1	s
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per JS-001-2023)	-	1.5	kV
Charge Device Model (Tested per JS-002-2022)	-	1	kV
Latch-Up (Tested per JESD78E; Class II, Level A, +125°C (T_J))	-	100	mA

1. Using a 2-series diodes back-to-back connection for isolation between PGND and SGND might be required due to -1V DC rating.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Operating Temperature	-40	+125	°C
VIN to GND	4.5	100	V
VCC5V, EN/UVLO to GND	0	5.4	V
VDD to GND	0	8.4	V
EXTBIAS to GND	0	36	V

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	25 Ld QFN Package	θ_{JA}[1]	Junction to ambient.	30.4	°C/W
		θ_{JC}[2]	Junction to case.	2.0	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 100V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}	-	**4.5**	-	**100.0**	V
V_{IN} Supply Current						
Shutdown Current[2]	I_{VINQ}	EN = 0V, PG/OC_MODE is floating	-	4	**10.0**	µA
Operating Current[3]	I_{VINOP}	PG/OC_MODE is floating	-	3.5	**7.0**	mA
VCC5V Supply						
Internal LDO Output Voltage	V_{CC5V}	V_{IN} = 8V, I_L = 0mA	**4.65**	5.0	**5.4**	V
		V_{IN} = 100V, I_L = 0mA	**4.65**	5.0	**5.4**	
		V_{IN} = 4.5V, I_L = 5mA	**3.9**	4.2	-	
		V_{IN} > 5.6V, I_L = 10mA	**4.65**	5.0	-	
Maximum Supply Current of Internal LDO	I_{VCC_MAX}	V_{VCC5V} = 0V, V_{IN} = 8V	-	100	-	mA
V_{DD} Supply						
Internal LDO Output Voltage	V_{DD}	V_{IN} = 12V, EXTBIAS = 0V, I_L = 0mA	**7.5**	8.0	**8.5**	V
		V_{IN} = 100V, EXTBIAS = 0V, I_L = 0mA	**7.5**	8.0	**8.5**	
		V_{IN} = 4.5V, EXTBIAS = 12V, I_L = 0mA	**7.5**	8.0	**8.5**	
		V_{IN} = 100V, EXTBIAS = 12V, I_L = 0mA	**7.6**	8.0	**8.5**	
		V_{IN} = 4.5V, EXTBIAS = 0V, I_L = 30mA	**3.9**	4.3	-	
		V_{IN} = 4.5V, EXTBIAS = 7.8V, I_L = 30mA	**7.4**	7.6	-	
		V_{IN} > 8.6V, EXTBIAS = 0V, I_L = 75mA	**7.3**	7.8	-	
		V_{IN} = 4.5V, EXTBIAS > 9.0V, I_L = 75mA	**7.3**	7.8	-	
Maximum Supply Current of Internal LDO	I_{VDD_MAX}	V_{VDD} = 0V, EXTBIAS = 0V, V_{IN} = 12V	-	100	-	mA
		V_{VDD}= 4.5V, EXTBIAS = 12V, V_{IN} = 4.5V	-	170	-	mA
EXTBIAS Supply						
Switch Over Threshold Voltage, Rising	V_{EXT_THR}	EXTBIAS voltage	**7.10**	7.38	**7.60**	V
Switch Over Threshold Voltage, Falling	V_{EXT_THF}	EXTBIAS voltage	**6.60**	6.85	**7.20**	V
V_{IN} UVLO						
V_{IN} Rising UVLO Threshold	$V_{UVLOTHR}$	V_{IN} voltage, 0mA on VCC5V and VDD	-	3.5	-	V
V_{IN} Falling UVLO Threshold	$V_{UVLOTHF}$	V_{IN} voltage, 0mA on VCC5V and VDD	-	3.3	-	V
VCC5V Power-On Reset						
VCC5V Rising POR Threshold	V_{PORTHR}	VCC5V voltage, 0mA on VCC5V and VDD	**3.7**	4.0	**4.3**	V
VCC5V Falling POR Threshold	V_{PORTHF}	VCC5V voltage, 0mA on VCC5V and VDD	**3.30**	3.55	**3.80**	V
EN/UVLO Threshold						
EN Rise Threshold for LDO	V_{EN_THR}	V_{IN} > 5.6V	**0.75**	1.05	**1.30**	V

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 100V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
EN Fall Threshold for LDO	V_{EN_THF}	V_{IN} > 5.6V	**0.60**	0.90	**1.10**	V
EN Hysteresis	V_{EN_HYST}	V_{IN} > 5.6V	**70**	150	**300**	mV
UVLO Rise Threshold for PWM switching	V_{UVLO_THR}	V_{IN} > 5.6V	**1.745**	1.80	**1.836**	V
UVLO Fall Threshold for PWM switching	V_{UVLO_THF}	V_{IN} > 5.6V	**1.7**	1.750	**1.785**	V
UVLO Low Source Current	I_{UVLO_LSC}	V_{EN} < V_{UVLO_THR}	**0.75**	1.2	**1.6**	µA
UVLO Hysteresis Current	I_{UVLO_HYST}	V_{IN} = 12V, EN/UVLO = 1.815V	**3**	4	**5**	µA
Soft-Start Current						
SS/TRK Soft-Start Charge Current	I_{SS}	SS/TRK = 0V	-	2.00	-	µA
Default Internal Minimum Soft-Starting						
Default Internal Output Ramping Time	t_{SS_MIN}	SS/TRK open	-	1.7	-	ms
Power-Good Monitors						
PG/OC_MODE Upper Threshold	V_{PGOV}	-	**106**	109	**112**	%
PG/OC_MODE Lower Threshold	V_{PGUV}	-	**83**	86	**90**	%
PG/OC_MODE Low Level Voltage	V_{PGLOW}	I_SINK = 2mA	-	-	**0.35**	V
PG/OC_MODE Leakage Current	I_{PGLKG}	PG/OC_MODE = 5V	-	0	**150**	nA
PGOOD Timing						
V_{OUT} Rising Threshold to PG/OC_MODE Rising[4]	t_{PGR}	-	-	1.1	**5**	ms
V_{OUT} Falling Threshold to PG/OC_MODE Falling	t_{PGF}	-	-	80	-	µs
OCP and Single/Parallel Mode Selection on PG/OC_MODE pin						
Single IC Constant Current Limit OCP Window	-	PG/OC_MODE sink current at startup	**280**	-	-	µA
Parallel IC Constant Current Limit OCP Window	-	PC/OC_MODE sink current at startup	**85**	-	**120**	µA
Single IC Hiccup Current OCP Mode Window	-	PC/OC_MODE sink current at startup	-	-	**25**	µA
Reference Section						
Internal Voltage Loop Reference Voltage	V_{REF}	-	-	0.800	-	V
Reference Voltage Accuracy	V_{REF}	T_A = 0°C to +85°C	**-0.75**	-	**+0.75**	%
		T_A = -40°C to +125°C	**-1.00**	-	**+1.00**	
PWM Controller Error Amplifiers						
FB Pin Bias Current	$I_{FBOUTLKG}$	-	**-50**	0	**+50**	nA
FB Error Amp GM	Gm1	-	-	1.75	-	mS
FB Error Amp Voltage Gain	AV	-	-	82	-	dB

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 100V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
FB Error Amp Gain-BW Product	GBW	-	-	8	-	MHz
FB Error Amp Output Current Capability	-	-	-	±300	-	µA
COMP Max High Voltage	V_{COMP_HIGH}	FB_OUT = 0V	-	4.5	-	V
COMP Min Low Voltage	V_{COMP_LOW}	FB_OUT = 1V	-	0.5	-	V
PWM Regulator						
PWM Minimum Off-Time	t_{OFF_MIN}	-	-	190	**250**	ns
PWM Minimum On-Time	t_{ON_MIN}	-	-	80	**155**	ns
PMW Peak-to-Peak Sawtooth Amplitude	DV_{RAMP}	V_{IN} = V_{OUT}, f_{SW} = 300kHz	-	1	-	V
PMW Ramp Offset	$V_{ROFFSET}$		**1.1**	1.2	**1.3**	V
Current Sense, Current Monitors, and Average Current Loop						
Current Sense Differential Voltage Range	V_{CSP} - V_{CSN}	-	**-80**	-	**+150**	mV
Current Sense Common-Mode Voltage Range	$CMIR_{CS}$	-	**0**	-	**100**	V
CSP Bias Current	-	CSP = CSN = 12V	-	-	**3**	µA
CSN Bias Current	-	CSP = CSN = 12V	-	-	**500**	µA
IMON Offset Current	$I_{CSOFFSET}$	CSP = CSN = 12V	**16.7**	20	**22**	µA
Current Sense Voltage to IMON Current Source Gain	A1Gm	12V common-mode voltage applied to CSP/N pins, 0 to 40mV differential voltage	**155**	190	**230**	µS
IMON Error Amp GM	Gm2	-	-	12	-	µS
IMON Error Amp Voltage Gain	AVC	-	-	72	-	dB
IMON Error Amp Gain-BW Product	GBWC	-	-	5	-	MHz
Switching Frequency						
Switching Frequency	f_{SW}	R_T = 165kΩ	**225**	250	**275**	kHz
		R_T = 80.6kΩ	**460**	500	**540**	kHz
		R_T = 36.5kΩ	**950**	1000	**1050**	kHz
		R_T = 14.3kΩ	**1.84**	2.02	**2.2**	MHz
		R_T = VCC5V, Floating	85	110	130	kHz
		R_T = 0Ω	420	520	600	kHz
RT Voltage	V_{RT}	R_T = 36.5kΩ	-	770	-	mV
MODE/SYNC						
SYNC Synchronization Range	f_{SYNC}	-	**140**	-	**2000**	kHz
SYNC Input Logic High	V_{SYNCH}	-	**1**	-	-	V
SYNC Input Logic Low	V_{SYNCL}	-	-	-	**0.5**	V
PWM_MODE Window						
Forced PWM MODE/SYNC Window	-	MODE/SYNC Pin	-	-	**0.7**	V

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Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Diode Emulation Mode						
Diode Emulation (DE) MODE/SYNC Window	-	MODE/SYNC Pin	**1.0**	-	**VCC5V-1.8V**	V
DE Mode Phase Threshold	V_{CROSS}	V_{IN}=12V	-	0	-	mV
SS pin DEM to Forced PWM Transition Threshold	$V_{SS\_DE\_CC}$	-	-	0.8	-	V
SS pin DEM reset Threshold	$V_{SS\_DE\_SET}$	-	-	0.3	-	V
PWM Gate Drivers						
Driver BOOT Refresh Trip Voltage	V_{BOOTRF}	BOOT voltage - PHASE voltage	**5.4**	5.85	**6.3**	V
Driver Source Upper Sink Current	I_{GSRC}	-	-	2000	-	mA
Driver Lower Sink Current	I_{GSNK}	-	-	2200	-	mA
Driver Upper Drive Pull-Up	R_{UG_UP}	-	-	1.6	-	Ω
Driver Upper Drive Pull-Down	R_{UG_DN}	-	-	1.25	-	Ω
Driver Lower Drive Pull-Up	R_{LG_UP}	-	-	1.6	-	Ω
Driver Lower Drive Pull-Down	R_{LG_DN}	-	-	1	-	Ω
Driver Upper Drive Rise Time	t_{GR_UP}	C_{OUT} = 1000pF	-	15	-	ns
Driver Upper Drive Fall Time	t_{GF_UP}	C_{OUT} = 1000pF	-	15	-	ns
Driver Lower Drive Rise Time	t_{GR_DN}	C_{OUT} = 1000pF	-	15	-	ns
Driver Lower Drive Fall Time	t_{GF_DN}	C_{OUT} = 1000pF	-	15	-	ns
Driver Dead Time	t_{D_LU}	C_{OUT} = 1000pF, LG falling edge 1V to UG rising edge 1V	-	25	-	ns
Driver Dead Time	t_{D_UL}	C_{OUT} = 1000pF,UG falling edge 1V to LG rising edge 1V	-	23	-	ns
Overvoltage Protection						
Output OVP Threshold	V_{OVTH_OUT}	-	**117**	119	**122**	%
Overcurrent Protection						
Pulse-by-Pulse Peak Current Limit Input Shunt Set Point	$V_{OCSET-CS}$	V_{CSP} - V_{CSN} 12V common-mode voltage applied to CSP/N pins	**68**	82	**101**	mV
Second Level Hiccup Peak Current Limit Output Shunt Set Point	$V_{OCSET-CS-HIC}$	V_{CSP} - V_{CSN}	**82**	98	**128**	mV
Pulse-by-Pulse Negative Peak Current Limit Output Shunt Set Point	$V_{OCSET-NEG}$	V_{CSP} - V_{CSN}, 12V common-mode voltage applied to ISEN± pins	**-60**	-50	**-40**	mV
Output Constant Current and Hiccup Current Limit Set Point	V_{IMONCC}	IMON Pin Voltage	**1.18**	1.2	**1.23**	V

Recommended operating conditions unless otherwise noted. See Block Diagram and Typical Application Schematics. V_{IN} = 4.5V to 100V, or V_{DD} = 8V ±10%, C_VCC5V = 4.7µF, T_A = -40°C to +125°C, Typical values are at T_A = +25°C, unless otherwise specified. **Boldface limits apply across the operating temperature range, -40°C to +125°C. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Output Constant and Hiccup Current Limit Set Point at CSP/N Input	V_{AVOCP_CS}	V_{CSP} - V_{CSN}, 12V common-mode applied to CSP/N pins, R_{IMON1} = 40.2k, T_J = -40°C to +125°C	-	52	-	mV
Hiccup OCP Off-Time	t_{HICC_OFF}	-	-	55	-	ms
Over-Temperature						
Over-Temperature Shutdown	T_{OT-TH}	-	-	153	-	°C
Over-Temperature Hysteresis	T_{OT-HYS}	-	-	9	-	°C

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.
2. This is the total shutdown current with V_{IN} = 5.6V and 100V.
3. Operating current is the supply current consumed when the device is active but not switching. It does not include gate drive current.
4. When soft-start time is less than 4.5ms, t_{PGR} increases. With internal soft-start (the fastest soft-start time), t_{PGR} increases close to its max limit 5ms.

4. Typical Performance Curves

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted.

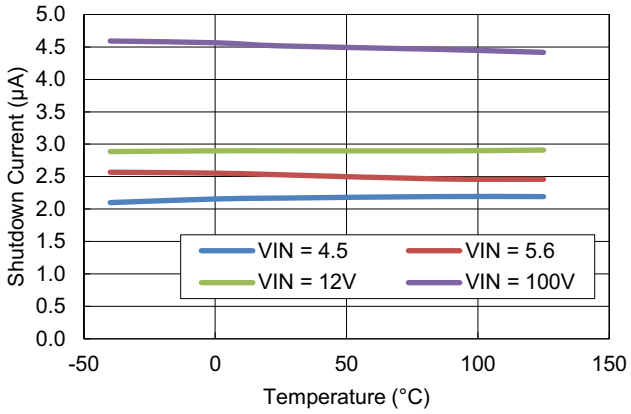


Figure 7. Shutdown Current vs Temperature

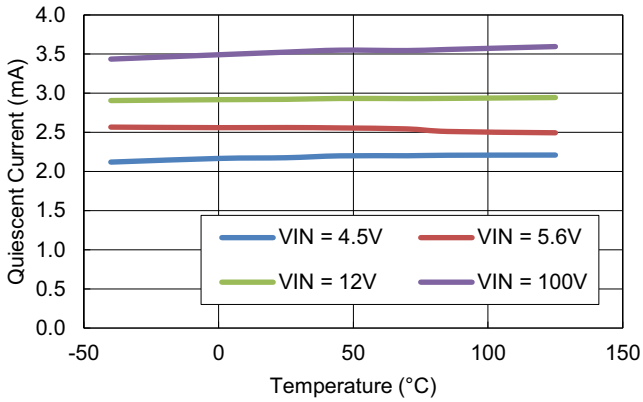


Figure 8. Quiescent Current vs Temperature

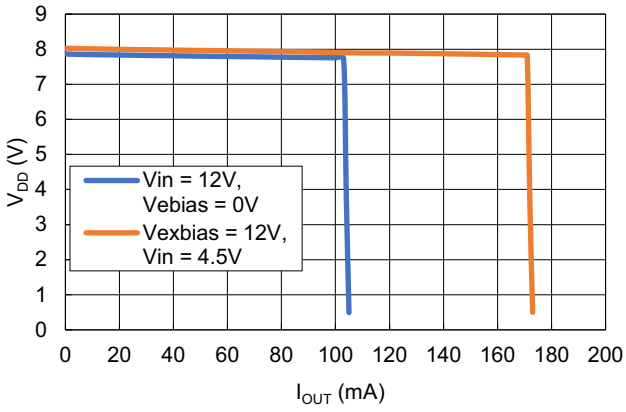


Figure 9. V_{DD} Load Regulation at 12V Input

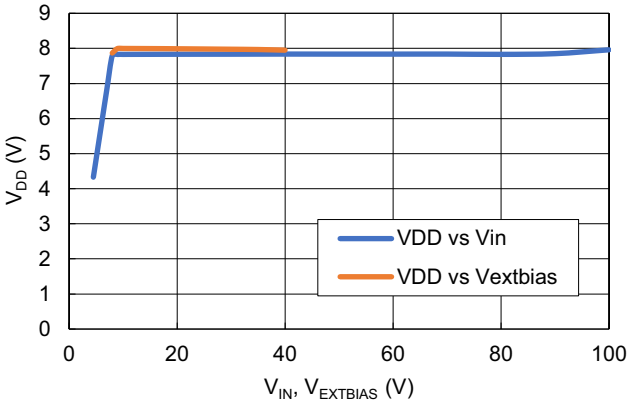


Figure 10. V_{DD} Line Regulation at 20mA Load

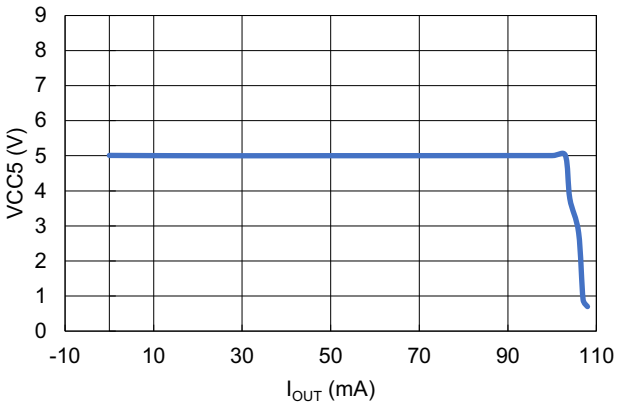


Figure 11. V_{CC5V} Load Regulation at $12V_{IN}$

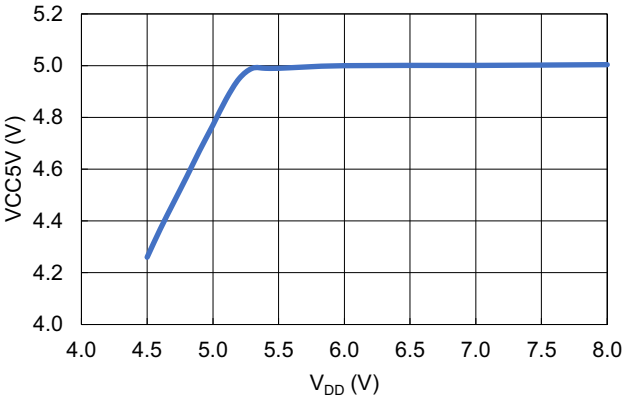


Figure 12. V_{CC5V} Line Regulation at 20mA Load

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted. (Cont.)

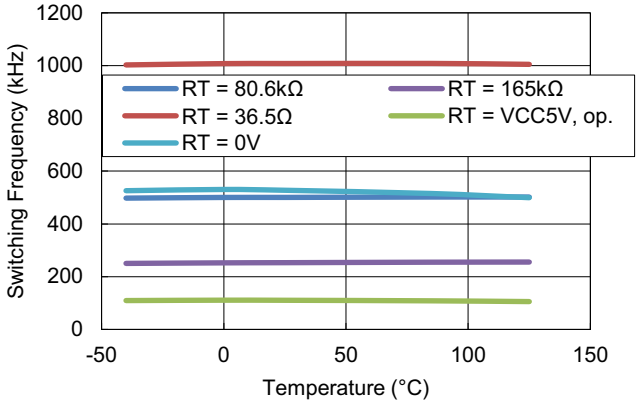


Figure 13. Switching Frequency vs Temperature

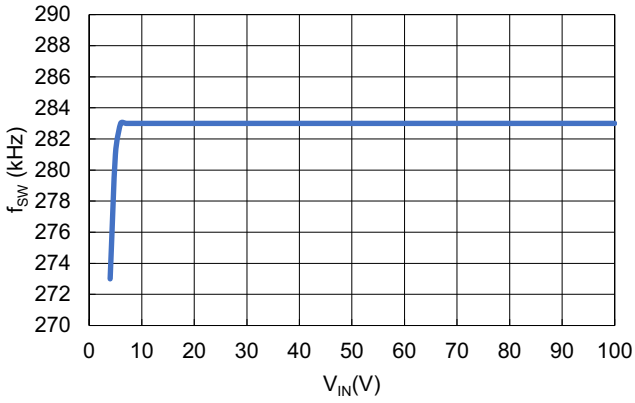


Figure 14. Switching Frequency vs V_{IN}, R_T = 144k

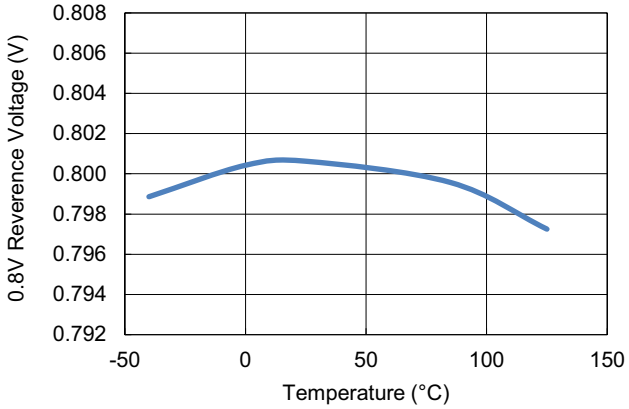


Figure 15. 0.8V Reference Voltage vs Temperature

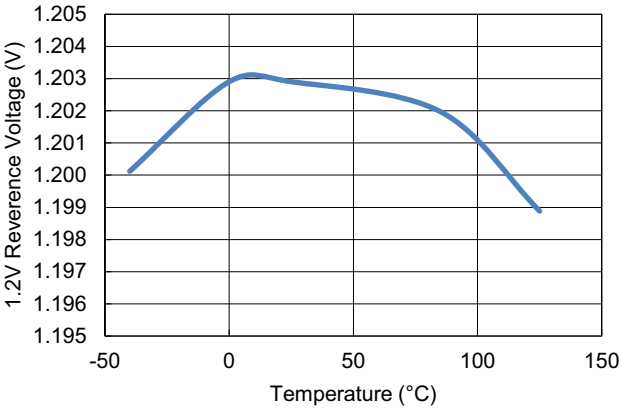


Figure 16. 1.2V Reference Voltage vs Temperature

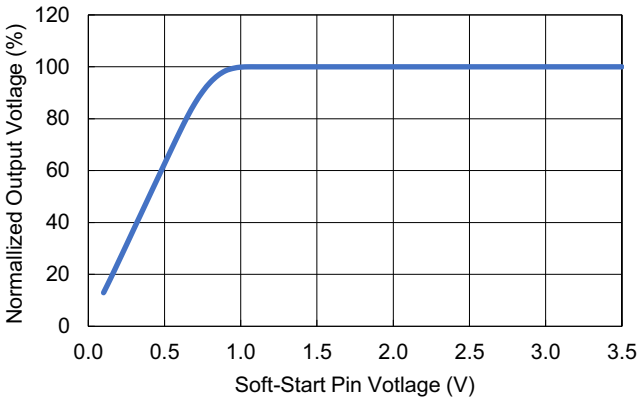


Figure 17. Normalized Output Voltage vs Voltage on Soft-Start Pin

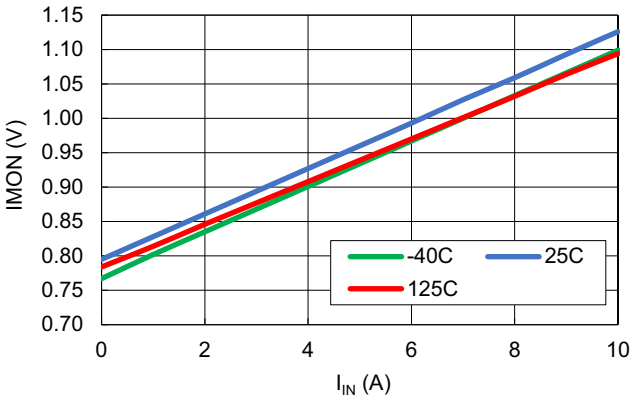


Figure 18. Output Current I_{OUT} (DC) vs IMON_OUT Pin Voltage, R_{S_OUT} = 4mΩ, R_{IM_OUT} = 40.2k

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted. (Cont.)

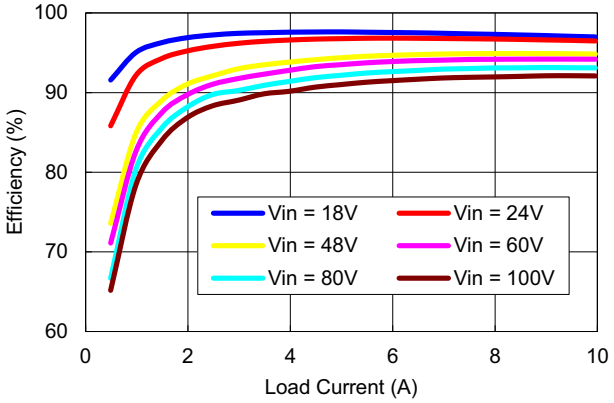


Figure 19. Forced PWM Mode Efficiency

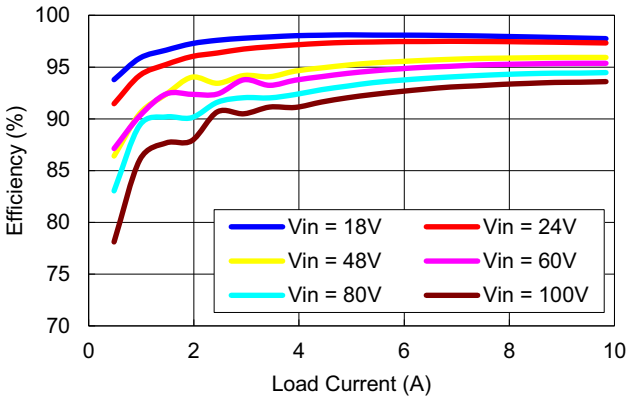


Figure 20. DE Mode Efficiency

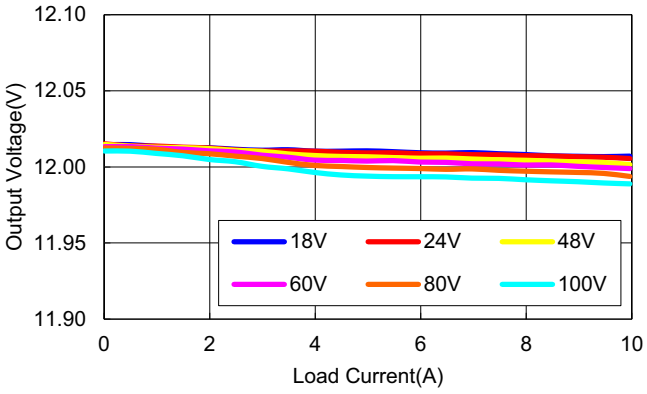


Figure 21. Forced PWM Load Regulation at +25°C

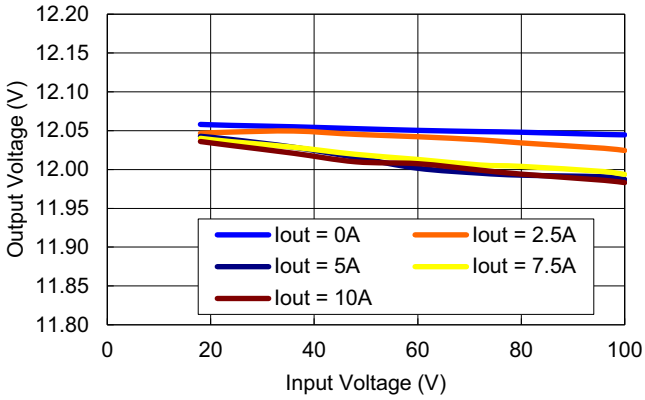


Figure 22. Forced PWM Line Regulation at 10A Load +25°C

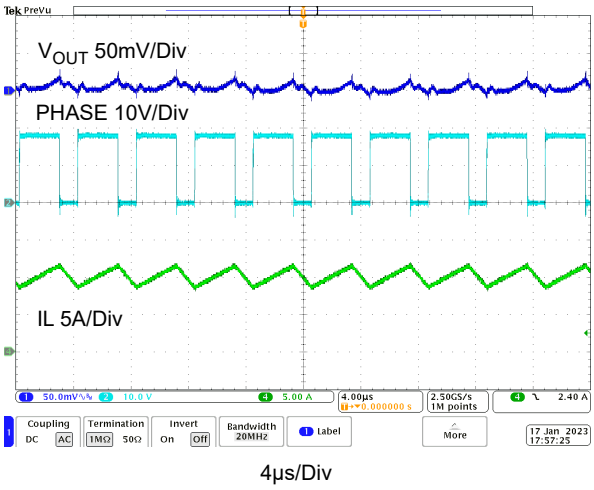


Figure 23. V_{IN} = 18V, I_{OUT} = 10A, Forced PWM Mode

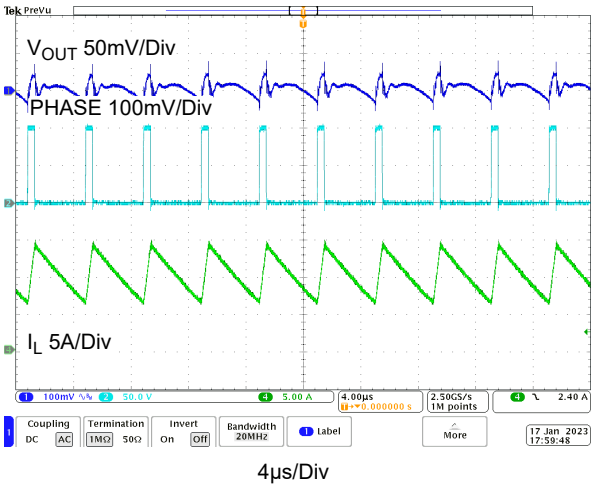


Figure 24. V_{IN} = 100V, I_{OUT} = 10A, Forced PWM Mode

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted. (Cont.)

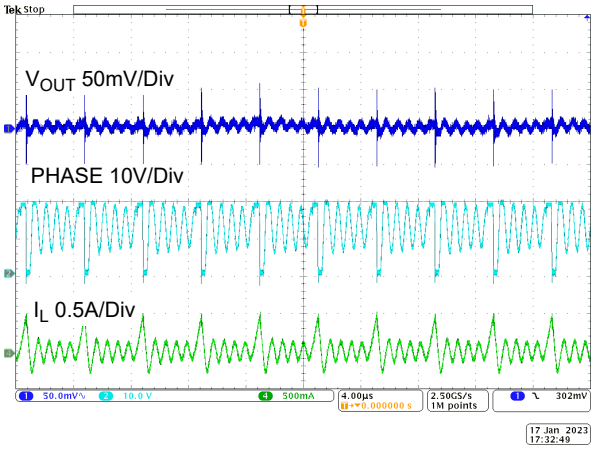


Figure 25. DEM Mode Waveforms, V_{IN} = 18V, I_{OUT} = 0A

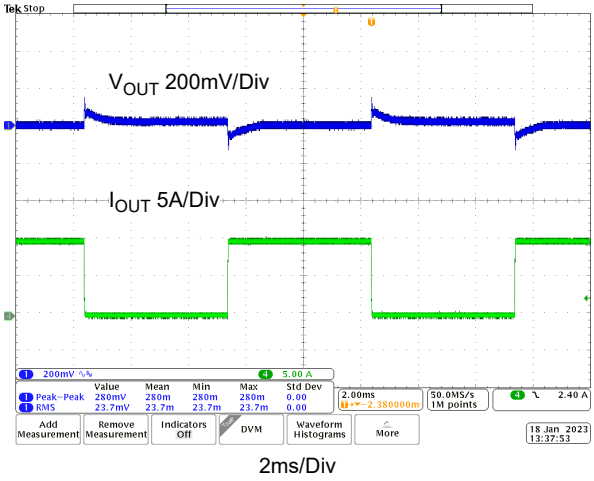


Figure 26. Load Transient, V_{IN} = 18V, I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM

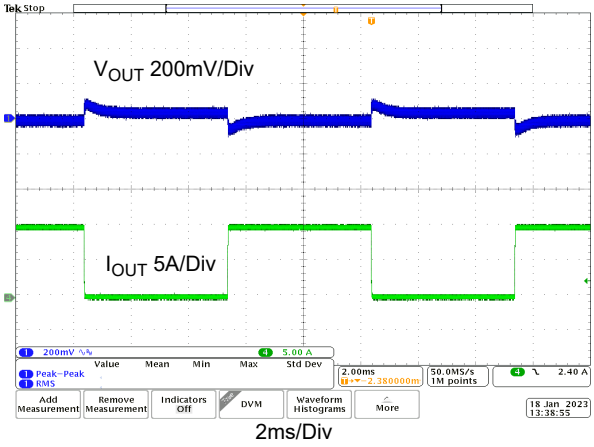


Figure 27. Load Transient, V_{IN} = 48V, I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM

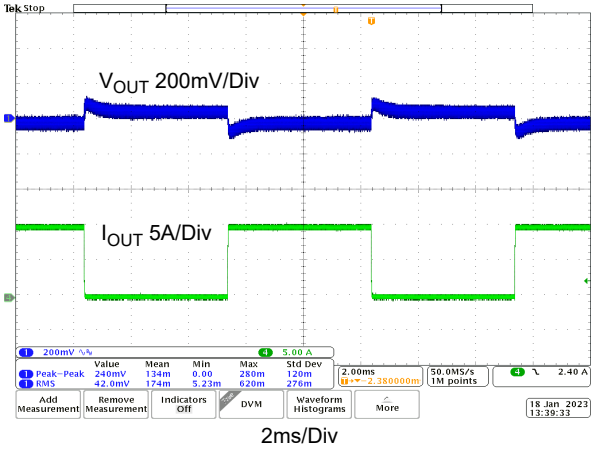


Figure 28. Load Transient, V_{IN} = 100V I_{OUT} = 0A to 10A, 2.5A/µs, Forced PWM

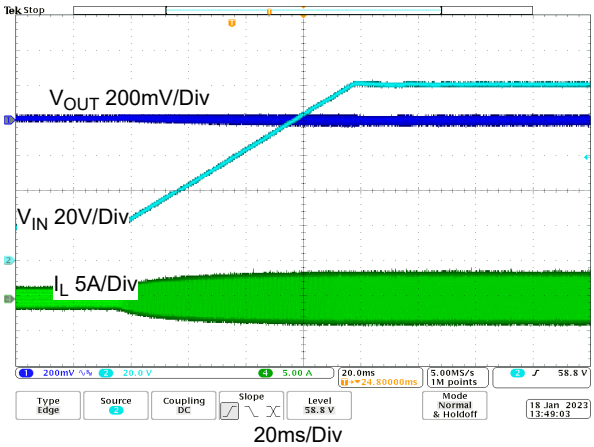


Figure 29. Line Transient, V_{IN} = 18V-100V, 1V/ms, I_{OUT} = 0A

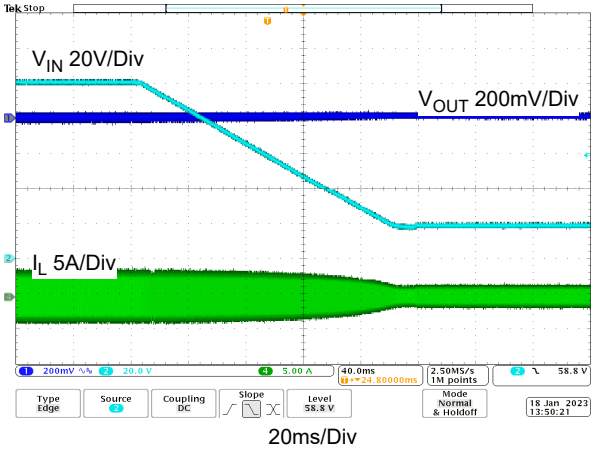


Figure 30. Line Transient, V_{IN} = 100V-18V, 1V/ms, I_{OUT} = 0A

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted. (Cont.)

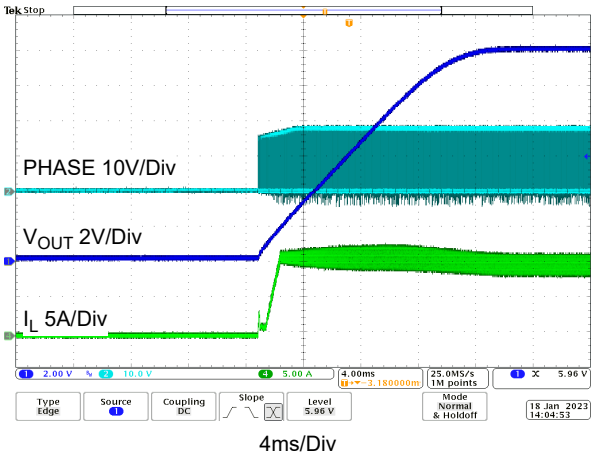


Figure 31. Start-Up Waveform, V_{IN} = 18V I_O = 10A Forced PWM

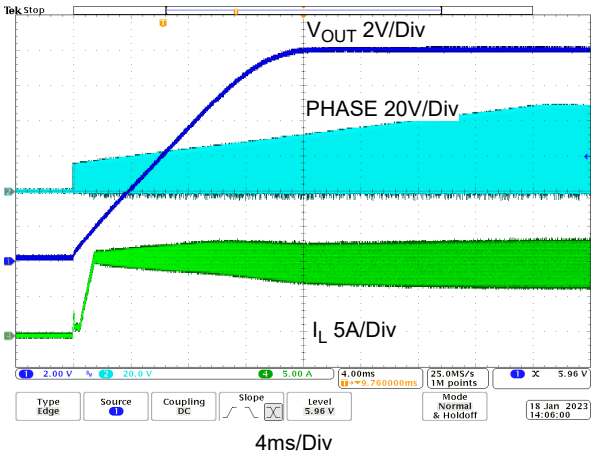


Figure 32. Start-Up Waveform, V_{IN} = 48V I_O = 10A, Forced PWM

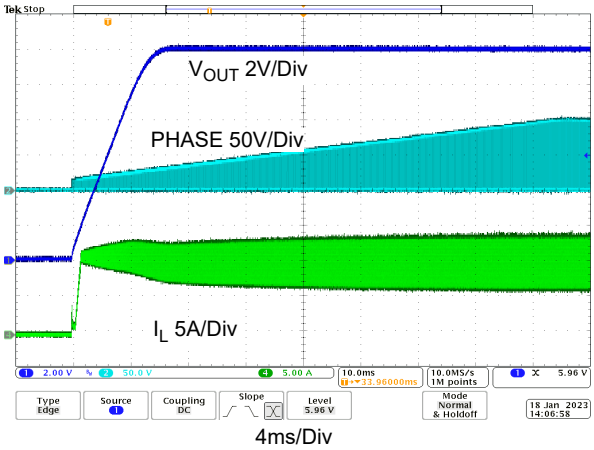


Figure 33. Start-Up Waveform, V_{IN} = 100V I_O = 10A, Forced PWM

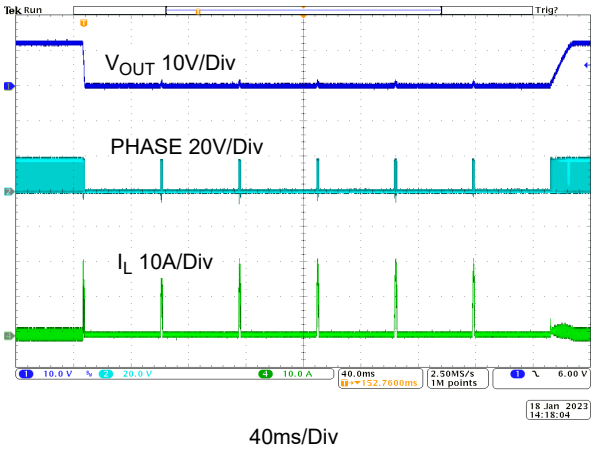


Figure 34. OCP Response, Output Short-Circuited from No Load to Ground and Released, Forced PWM Mode, V_{IN} = 48V

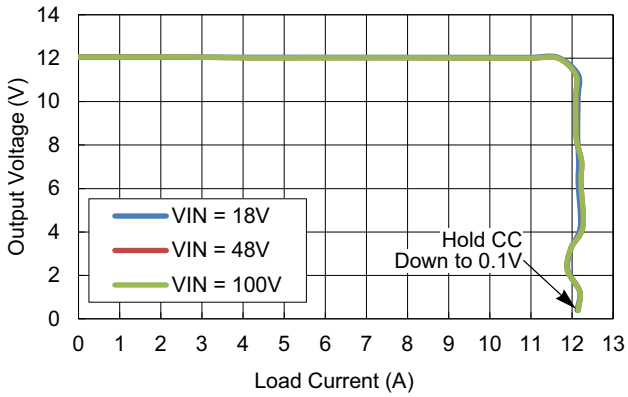
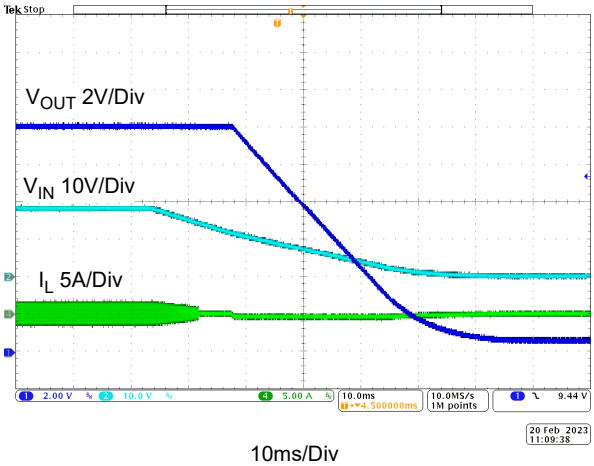


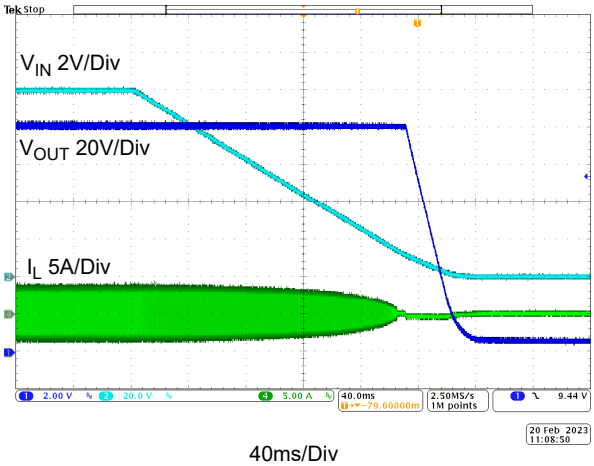
Figure 35. Constant Voltage (CV) and Constant Current (CC) Operation

Oscilloscope plots are taken using the ISL81100EVAL1Z evaluation board, V_{IN} = 16V to 100V, V_{OUT} = 12V, I_{OUT} = 10A unless otherwise noted. (Cont.)



10ms/Div

Figure 36. V_{IN} Shutdown V_{IN} = 18V I_O = 0A



40ms/Div

Figure 37. V_{IN} Shutdown V_{IN} = 100V I_O = 0A

5. Functional Description

5.1 General Description

The ISL81100 implements synchronous buck control with a PWM controller, internal drivers, references, protection circuits, current and voltage control inputs, PLL clock and sync control logic, and current monitor outputs. See Figure 5.

The ISL81100 is a peak-current mode controller. The controller integrates two control loops to regulate V_{OUT} and average maximum I_{OUT}. The driver and protection circuits are also integrated to simplify the end design.

The part has an independent enable/disable pin, providing flexible power-up sequencing and a simple V_{IN} UVP implementation. The soft-start time is programmable by adjusting the soft-start capacitor on the SS/TRK pin.

5.2 Internal 8V Linear Regulator (VDD), External Bias Supply (EXTBIAS), and 5V Linear Regulator (VCC5V)

The ISL81100 provides two input pins, VIN and EXTBIAS, and internal LDOs for the VDD gate driver supply. A second LDO generates VCC5V from VDD. VCC5V delivers power to all internal functional circuits other than the gate drivers. Bypass the linear regulator's outputs (VDD) with a 10µF capacitor to the power ground. Also, bypass the second linear regulator output (VCC5V) with a 10µF capacitor to the signal ground. A power-on reset circuit monitors VCC5V, disabling all regulators when VCC5V falls below 3.55V.

LDOs from VIN and EXTBIAS can source 75mA for VDD to power the gate drivers. When driving large FETs at a high switching frequency, little or no regulator current may be available for external loads. The LDO from VDD to VCC5V can also source over 75mA to supply the IC internal circuit. Although the current consumed by the internal circuit is low, the current provided by VCC5V to the external loads is limited by VDD. For example, a single large FET with a 15nC total gate charge requires 15nC x 300kHz = 4.5mA (15nC x 600kHz = 9mA).

Also, the power dissipation across the internal 8V LDO increases at higher input voltages with larger FETs. Avoid excessive power dissipation across this regulator to prevent junction temperature rise. Thermal protection can be triggered if the die temperature increases above +150°C due to excessive power dissipation.

When large MOSFETs or high input voltages are used, an external 8V bias voltage can be applied to the EXTBIAS pin to alleviate excessive power dissipation. When the voltage at the EXTBIAS pin is higher than the typical 7.38V, the LDO from EXTBIAS activates, and the LDO from VIN is disconnected. The recommended maximum voltage at the EXTBIAS pin is 36V. For applications with V_{OUT} significantly lower than V_{IN}, EXTBIAS is usually back-biased by V_{OUT} to reduce the LDO power loss. EXTBIAS can only activate after the soft-start is finished to avoid early activation during the V_{OUT} rising stage. An external UVLO circuit might be necessary to ensure smooth soft-starting. Renesas recommends adding a 10µF capacitor on the EXTBIAS pin and using a diode to connect the EXTBIAS pin to V_{OUT} to prevent the EXTBIAS pin voltage from being pulled low due to a V_{OUT} short-circuit condition.

The two VDD LDOs have an overcurrent limit for short-circuit protection. The VIN to VDD LDO current limit is set to a typical 100mA. The EXTBIAS to VDD LDO current limit is set to a typical 170mA.

5.3 Enable (EN/UVLO) and Soft-Start Operation

ISL81100 provides an enable pin EN/UVLO. Pulling the pin high or low can enable or disable the output. When the pin voltage is higher than 1.05V, the three LDOs are enabled. After the VCC5V reaches the POR threshold, the controller is powered up to initialize its internal circuit. The soft-start circuitry becomes active when EN/UVLO exceeds the 1.8V accurate Undervoltage Lockout (UVLO) threshold. An internal 2µA current source begins charging the soft-start capacitor connected from the soft-start pin SS/TRK to GND. The error amplifier reference voltage is clamped to the SS/TRK pin voltage. Therefore, the output voltage rises from 0V to regulation as the soft start pin rises from 0V to 0.8V. Charging of the soft-start capacitor continues until the voltage on the soft-start pin reaches 3V. The soft-start pin can be used for tracking.

Set the soft-start time by the value of the soft-start capacitor connected from the soft-start pin to GND. Alleviate the inrush current during start-up by adjusting the soft-start time.

Use Equation 2 to set the typical soft-start time.

(EQ. 2) $$t_{SS} = 0.8V\left(\frac{C_{SS}}{2\mu A}\right)$$

When the soft-start time set by external CSS or tracking is less than 1.7ms, an internal soft-start circuit of 1.7ms takes over the soft-start.

PG/OC_MODE toggles to high when the output voltage is in regulation.

Pulling the EN/UVLO pin lower than the UVLO falling threshold V_{UVLO_THF} typical 1.75V disables the PWM output. Pulling the EN/UVLO pin lower than the EN falling threshold V_{EN_THF} typical 0.9V disables internal LDOs to achieve low standby current. The SS/TRK is also discharged to GND by an internal MOSFET with 70Ω $r_{DS(ON)}$. For applications with more than 1µF capacitor on the soft start-pin, Renesas recommends adding a 100Ω to 1kΩ resistor in series with the capacitor to share the power loss during the discharge.

Using the UVLO threshold, an accurate VIN Under Voltage Protection (UVP) feature is implemented by feeding the VIN into the EN/UVLO pin using a voltage divider (RUV1 and RUV2) as shown in Figure 38.

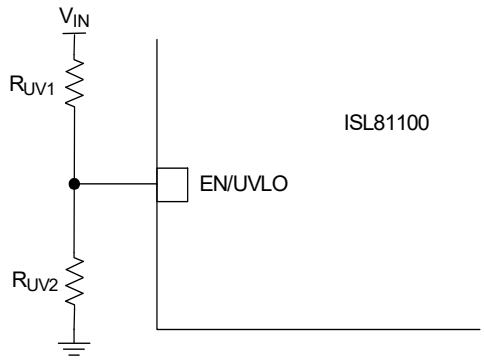


Figure 38. V_{IN} Undervoltage Protection

When V_{IN} rising and V_{IN} falling thresholds are selected, use Equation 3 to calculate R_{UV1}, where V_{UVLO_THR} is the EN/UVLO pin UVLO rising threshold, typically 1.8V.

(EQ. 3) $$R_{UV1} = \frac{V_{INRISE}V_{UVLO\_THF} - V_{INFALL}V_{UVLO\_THR}}{I_{UVLO\_HYST}V_{UVLO\_THR} - I_{UVLO\_LSC}V_{UVLO\_THF}}$$

Use Equation 4 to calculate R_{UV2}, where I_{UVLO_HYST} is the UVLO hysteresis current, typically 4.4µA. Refer to the ISL81100 Excel design spread.

(EQ. 4) $$R_{UV2} = \frac{V_{INRISE}V_{UVLO\_THF} - V_{INFALL}V_{UVLO\_THR}}{I_{UVLO\_HYST} \times (V_{INRISE} - V_{UVLO\_THR}) - I_{UVLO\_LSC} \times (V_{INFALL} - V_{UVLO\_THR})}$$

5.4 Tracking Operation

The ISL81100 output can track an external supply. Connect a resistive divider between the external supply output and ground to implement tracking. Connect the center point of the divider to the SS/TRK pin. The resistive divider ratio sets the ramping ratio between the two voltage rails. To implement coincident tracking, set the tracking resistive divider ratio the same as the resistive output divider given by Equation 5. Ensure that the voltage at SS/TRK is more than 0.8V when the master rail reaches regulation.

To minimize the impact of the 2µA soft-start current on the tracking function, Renesas recommends using resistors less than 10kΩ for the tracking resistive divider.

When the external tracking source pulls the SS/TRK pin voltage to less than 0.3V, the pre-bias startup DE mode function is enabled again. The output voltage may not be able to be pulled down if the load current is not high enough.

When Overcurrent Protection (OCP) is triggered, the internal minimum soft-start circuit determines the 55ms OCP soft-start hiccup off-time.

5.5 Control Loops

The ISL81100 integrates a buck controller, providing output voltage below the input voltage. Peak current mode PWM control algorithm is used in the controller. The Renesas proprietary control architecture uses a current sense resistor in series with the inductor to sense the inductor current (See Figure 1 and Figure 5). By using an RC network, the inductor current signal can also be derived from the inductor voltage using DCR sensing. The inductor current is controlled by the voltage on the COMP pin, which is the lowest output of the error amplifiers Gm1. As the simplest example, when the output is regulated to a constant voltage, the FB pin receives the output feedback signal, which is compared to the internal reference by Gm1. Lower output voltage creates higher COMP voltage, leading to a higher PWM duty cycle to deliver more current to the output. Conversely, higher output voltage creates lower COMP voltage, which leads to a lower PWM duty cycle to reduce the current supplied to the output.

The ISL81100 has two error amplifiers, which can control output voltage (Gm1) and current (Gm2). In this architecture, it can provide constant voltage and constant current output.

5.5.1 Output Voltage Regulation Loop

The ISL81100 provides a precision 0.8V internal reference voltage to set the output voltage. Based on this internal reference, the output voltage is set from 0.8V to a level determined by the feedback voltage divider, as shown in Figure 39.

A resistive divider from the output to ground sets the output voltage. Connect the center point of the divider to the FB_OUT pin. The output voltage value is determined by Equation 5, where R_{FBO1} is the top resistor of the feedback divider network, and R_{FBO2} is the bottom resistor connected from FB_OUT to ground as shown in Figure 39.

(EQ. 5) $$V_{OUT} = 0.8V\left(\frac{R_{FBO1} + R_{FBO2}}{R_{FBO2}}\right)$$

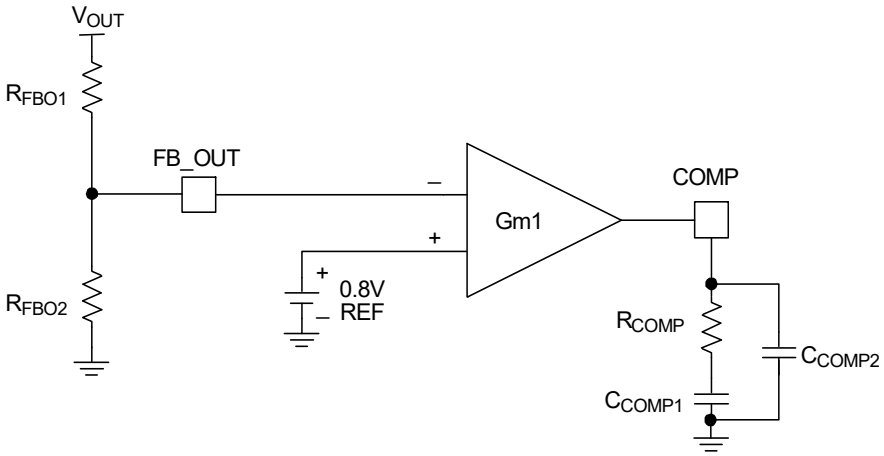


Figure 39. Output Voltage Regulator

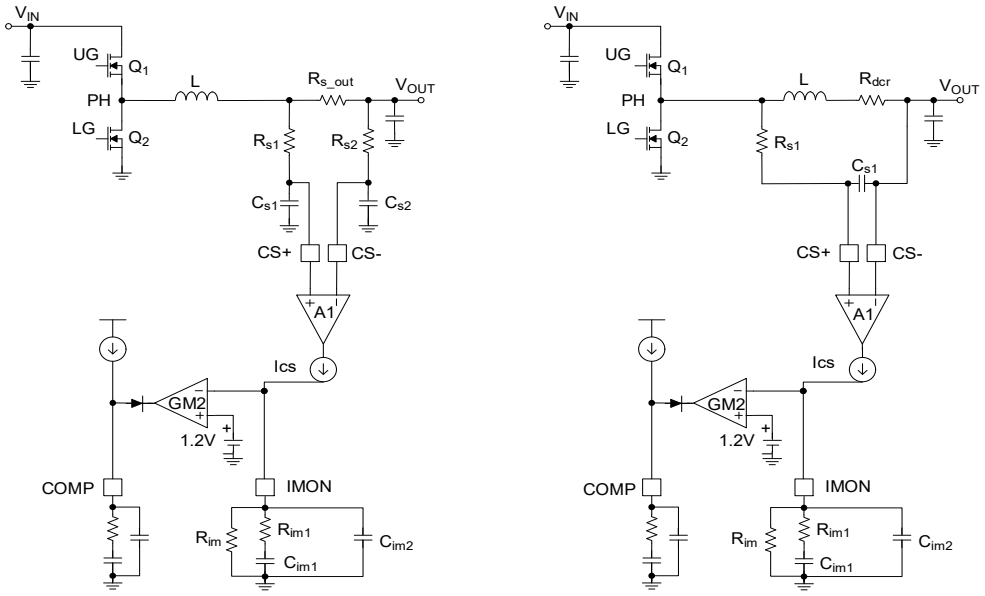
As shown in Figure 39, the R_{COMP}, C_{COMP1}, and C_{COMP2} network connected on the Gm1 regulator output COMP pin is required to compensate the loop for stable operation. The loop stability can be affected by many factors, such as V_{IN}, V_{OUT}, load current, switching frequency, inductor value, output capacitance, and the compensation

network on the COMP pin. For most applications, 68nF is a good value for C_{COMP1}. A larger C_{COMP1} makes the loop more stable by giving a larger phase margin, but the loop bandwidth is lower. C_{COMP2} is typically 1/10th to 1/30th of C_{COMP1} to filter high-frequency noise. A good starting value for R_{COMP} is 5k. Lower R_{COMP} improves stability but slows the loop response. Optimize the final compensation network with a bench test.

5.5.2 Output Average Current Monitoring and Constant Output Current Regulation Loops

The ISL81100 has a current-sense operational amplifier (op amp) A1 that monitors the output current. Figure 40 shows the ISL81100 current shunt sense and monitor circuit. The voltage signal on the current-sense resistor R_{S_OUT} is sent to the differential input of CS+/CS- after the RC filters R_{S1}/C_{S1} and R_{S2}/C_{S2}. Renesas recommends using a 1Ω value for R_{S1} and R_{S2} and a 10nF value for C_{S1} and C_{S2} to effectively dampen the switching noise without significantly delaying the current signal or introducing too much error by the op-amp bias current. The A1 amplifier converts the current-sense voltage signal to the current signal I_{CS}. See Equation 6 where I_{OUT} is the inductor current, $I_{ICSOFFSET}$ is the A1 output offset current typical 20µA, and A1Gm is the gain, typical 200µS.

(EQ. 6) $$I_{CS} = A1Gm(I_{OUT})R_{S\_OUT} + I_{CSOFFSET}$$



A. I_{OUT} Average Current Loop with Shunt Sense

B. I_{OUT} Average Current Loop with DCR Sense

Figure 40. Output Average Current Monitoring and Regulation Loops

By connecting the resistor R_{IM} on the IMON pin, the I_{CS} current signal is transferred to the voltage signal. The RC network on the IMON pin ($R_{IM1}/C_{IM1}/C_{IM2}$) is required to remove the AC content in the I_{CS} signal and ensure stable loop operation. The average voltage at the IMON pin is regulated to 1.2V by Gm2 for constant current control.

Use Equation 7 to calculate the output constant current set point I_{OUTCC}. See V_{AVOCP_CS} in the Electrical Specifications table to estimate the set point tolerance.

(EQ. 7) $$I_{OUTCC} = \frac{1.2 - I_{ICSOFFSET} \times R_{IM}}{R_{IM} \times R_{S\_OUT} \times A1Gm}$$

Like the voltage control loops, the average current loop stability can be affected by many factors, such as V_{IN}, V_{OUT}, switching frequency, inductor value, output and input capacitance, and the RC network on the IMON pin. Due to the high AC content in I_{CS}, a large C_{IM1} is required. A larger C_{IM1} can stabilize the loop by giving a larger phase margin, but the loop bandwidth is lower. For most applications, 47nF is a good value for C_{IM1}. C_{IM2} is typically 1/10th to 1/30th of C_{IM1} to filter high-frequency noise. R_{IM1} is required to boost the phase margin. A good starting value for R_{IM1} is 5k. Optimize the final compensation network with iSim simulation and bench testing. Because the device has a peak-by-peak current limit protection feature, it starts to engage with the current-sense signal at 82mV (typical). To design for constant output current operation, the current sense resistor value and larger Rim should ensure that 1.2V on IMON pin voltage is reached before the 82mV is reached for the current-sense signal.

Figure 40 B shows the ISL81100 inductor DCR current sense and monitor circuit. Rdcr plays the same role as R_{S_OUT} in the shunt current sense circuit. Renesas recommends keeping Rs1 × Cs1 = L/Rdcr. To minimize the error caused by the A1 input bias current, Renesas recommends keeping Rs1 less than 10k.

5.6 Modes of Operation and Light-Load Efficiency Enhancement

Set ISL81100 to DE mode to improve light-load efficiency. The MODE/SYNC pin sets the DE or PWM mode operation in the initialization period before soft-start. The converter is set to Forced PWM mode if the pin voltage is less than 0.8V. If the pin voltage exceeds 0.8V and is less than VCC5V-1V, the converter is set to diode emulation mode (DEM). When synchronized with an external clock, the controller operates in PWM Mode at light load.

In PWM mode, the device operates in typical peak current mode control. UG is turning the high-side MOSFET on, driven by the switching frequency clock. In the PWM on time interval, the COMP pin voltage is compared with the summing signal of the current sense and the internal ramp. When the combined current sense and ramp signal exceeds the COMP voltage, the high-side MOSFET turns off, and low-side MOSFET turns on. The switching cycle repeats when the switching cycle clock initiates the turn-off of the low-side MOSFET and the turn-on of the high-side MOSFET.

When DE mode is set, the sync FET driven by LG runs in diode emulation mode. The inductor current cannot reverse (discontinuous operation) depending on the zero cross-detection reference level V_{CROSS} for sync FET. At very light-load conditions, when the output current decreases to zero, the ISL81100 skips some cycles to regulate the output voltage.

5.7 Pre-Biased Power-Up

ISL81100 can soft-start with a pre-biased output by running in forced DE mode during soft-start. The output voltage is not pulled down during pre-biased start-up. The PWM mode is inactive until the soft-start ramp reaches 90% of the output voltage set point times the feedback resistive divider ratio. Forced DE mode is set again when an internal or external circuit pulls the SS/TRK pin voltage to less than 0.3V.

The overvoltage protection function is still operating during soft-start in DE mode.

5.8 Frequency Selection

Switching frequency selection is a trade-off between efficiency and component size. Low switching frequency improves efficiency by reducing MOSFET switching loss. Operating at a low switching frequency requires larger inductance and output capacitance to meet the output ripple and transient load requirements. The switching frequency of the ISL81100 is set by a resistor connected from the RT/SYNC pin to GND according to Equation 1.

The frequency setting curve shown in Figure 41 assists in selecting the correct value for R_T.

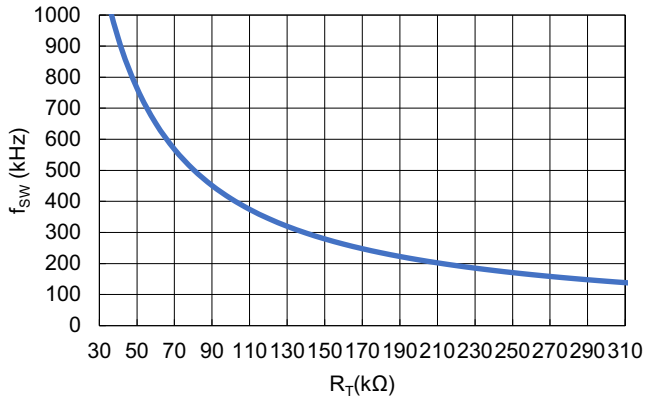


Figure 41. R_T vs Switching Frequency f_{SW}

5.9 Frequency Synchronization

If the MOD/SYNC pin is connected to an external clock, the ISL81100 synchronizes with this external clock frequency. For proper operation, the frequency set by resistor RT should be lower than the external clock frequency. When frequency synchronization occurs, the controllers enter forced PWM mode at light load. The synchronization signal's falling edge must be far from the UG turn-off edge. Adding RC filters can slow the signal to the IC if a fast edge external synchronization signal is used.

5.10 Gate Drivers

The ISL81100 integrates a high-voltage driver pair to drive the buck MOSFET pair. The driver pair consists of a gate control logic circuit, a low-side driver, a level shifter, and a high-side driver.

The low-side gate driver is supplied from VDD and provides a 2A peak sink and source current. The high-side gate driver can deliver the same currents as the low-side gate driver. A flying capacitor boot circuit generates a gate-drive voltage for the upper N-channel MOSFET. A boot capacitor connected from the BOOT pin to the PHASE node provides power to the high-side MOSFET driver. An external resistor is placed between the BOOT pin and the boot capacitor as a high-side MOSFET turn resistor. The external boot diode is required to charge up the boot capacitor. The boot diode is a high-voltage diode that bears the maximum input voltage plus the 8.5V between the boot and the phase pin with an extra margin.

If the diode voltage drop is ignored at startup, the low-side MOSFET turns on first and forces PHASE to ground to charge the BOOT capacitor to 8V. After the low-side MOSFET turns off, the high-side MOSFET is turned on by closing an internal switch between BOOT and UGATE. This feature provides the gate-to-source voltage to turn on the upper MOSFET, which boosts the 8V gate drive signal above V_{IN}. The current required to drive the upper MOSFET is drawn from the internal 8V VDD regulator.

Place a small resistor between the BOOT pin and the bootstrap capacitor's positive terminal to optimize EMI performance or reduce phase node ringing.

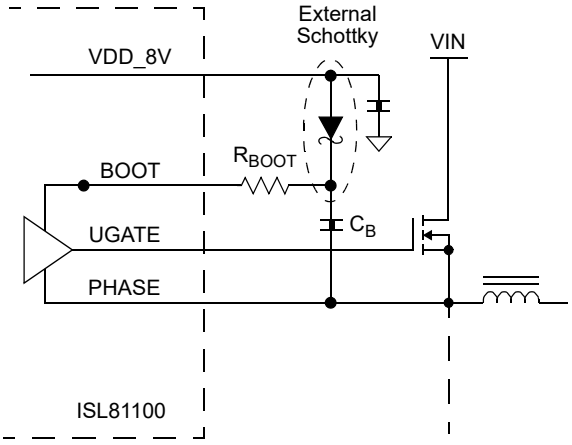


Figure 42. Upper Gate Driver Circuit

5.11 Power-Good Indicator

The power-good pin can monitor the status of the output voltage. PG/OC_MODE is true (open drain) 1.1ms after the FB pin is within ±11% of the reference voltage. The pin pulls down when the output is not within ±11% of the nominal voltage or the EN pin is pulled LOW.

No extra delay occurs when the PG/OC_MODE pin is pulled LOW.

5.12 Current Sharing with Parallel Operation

Connecting multiple ISL81100s in parallel for multiphase operation is possible. To set the controller in Current Sharing Constant Current Limit OCP mode, use a 49.9kΩ resistor from the VCC5V pin to each controller's PG/OC_MODE pin. Do not connect the PG/OC_MODE pins of the controllers together.

Connect the FB pins of each controller as shown in Figure 4, and similarly connect COMP, SS, EN, IMON, and EXTBIAS if using this function. Connect an external clock signal to the MODE/SYNC pins. To create an interleaved N-phase multiphase solution, provide clock signals that are out of phase by 360°/N. See the Frequency Synchronization section for more details on synchronization.

Fault monitoring can be accomplished by monitoring one of the controller's PG/OC_MODE pins. The ±11% PG indicator triggers at similar levels on both ICs, so it is unnecessary to logically OR these together. The +120% OV fault also triggers at similar levels, and the response of the first IC to trigger causes all ICs in the system to shut down. Overcurrent is implemented as a constant current mode, so each controller delivers constant current when this threshold is reached. Over-temperature protection on one IC causes all of the controllers in the system to shut down.

6. Protection Circuits

The converter output and input are monitored and protected against overload, overvoltage, and undervoltage conditions.

6.1 Input Undervoltage Lockout (UVLO)

The ISL81100 includes input UVLO protection, which resets the device until a proper operating voltage is applied. UVLO protection shuts down the ISL81100 if the input voltage drops below the VIN Fall Voltage. The controller is disabled when UVLO is asserted. When UVLO is asserted, Power-Good (PG/OC_MODE) is de-asserted. If the EN pin voltage rises above 1.8V, UVLO is de-asserted to allow the start-up operation.

6.2 VCC5V Power-On Reset (POR)

When supplied by V_{IN}, the ISL81100 sets its VCC5V POR rising threshold at 3.5V and the falling threshold at 3.3V.

6.3 Overcurrent Protection (OCP)

6.3.1 Output Average Overcurrent Protection

As described in Output Average Current Monitoring and Constant Output Current Regulation Loops, the ISL81100 can regulate the output current with close loop control. This feature provides a constant current type of overcurrent protection. It can be set to a hiccup type of protection by selecting a different pull-up resistor value connected from the PG/OC_MODE pin to a fixed voltage.

The output constant or hiccup average OCP set points I_{OUTCC} is calculated using Equation 7 in Output Average Current Monitoring and Constant Output Current Regulation Loops.

The average OCP mode is set by a pull-up resistor connected from the PG/OC_MODE pin to a fixed voltage during the initiation stage before soft-start. The pin would sink current through the pull-up resistor during the initiation stage. If the current into the pin is higher than 190µA, the converter is set to stand-alone constant current limit OCP mode. If the current into the pin is higher than 60µA and less than 190µA, the converter is set to current sharing constant current limit OCP mode for parallel operation. If the current into the pin is less than 60µA, the converter is set to stand-alone hiccup OCP mode.

In hiccup OCP mode, after the average current is higher than the set point for 32 consecutive switching cycles, the converter turns off for 50ms before a restart is issued.

6.3.2 First Level Pulse-by-Pulse Peak Current Limit

As shown in Figure 40 in Output Average Current Monitoring and Constant Output Current Regulation Loops, the inductor peak current is sensed by the shunt resistor R_{S_OUT} and op-amp A1. When the voltage drops and R_{S_OUT} reaches the set point $V_{OCSET-CS}$ typical 82mV, Q_1 is turned off. Use Equation 8 to calculate the first level peak current limit set point I_{OCPP1}.

(EQ. 8) $$I_{OCPP1} = \frac{V_{OCSET-CS}}{R_{S\_OUT}}$$

If the constant current operation is the design target, use a large IMON pin resistor so that when the load current reaches the required constant current operation, the current sense signal on the CS sense pins is less than 82mV.

6.3.3 Second Level Hiccup Peak Current Protection

A minimum on or blanking time is set to the PWM signal to avoid any false trip in peak current-mode operation. The first level, a pulse-by-pulse current limit circuit, cannot further reduce the PWM duty cycle to the minimum on-time. In an output dead short condition, especially at high V_{IN}, the inductor current increases rapidly, even with the minimum on-time PWM duty cycle. The ISL81100 integrates a second-level hiccup type of peak current

protection. When the voltage drop on R_{S_OUT} reaches the set point $V_{OCSET\text{-}CS\text{-}HIC}$ (typical 100mV), the converter turns off by turning off all switches for 50ms before a restart is issued. Use Equation 9 to calculate the second level peak current protection set point I_{OCPP2}.

(EQ. 9) $$I_{OCPP2} = \frac{V_{OCSET\text{-}CS\text{-}HIC}}{R_{S\_OUT}}$$

6.3.4 Pulse-by-Pulse Negative Peak Current Limit

The inductor current becomes negative in reverse direction operation and OVP protection cases. The negative current is sensed by the shunt resistor R_{S_OUT} and amplifier A1, as shown in Figure 40. The negative peak current limit would be triggered when the voltage drop on R_{S_OUT} reaches the set point $V_{OCSET\text{-}ISEN}$ (typical -50mV). Use Equation 10 to calculate the set point I_{OCPPN}.

(EQ. 10) $$I_{OCPPN} = \frac{V_{OCSET\text{-}ISEN}}{R_{S\_OUT}}$$

The device can be damaged in negative peak current limit conditions. In these conditions, the energy flows from output to input. If the input source lacks current-sinking capability, the V_{IN} voltage increases. When V_{IN} increases to higher than its maximum limit, the IC can be damaged.

6.4 Overvoltage Protection (OVP)

The overvoltage set point is at 119% of the nominal output voltage set by the feedback resistors. If an overvoltage event occurs, the IC would work in tri-state, and Q_1 would be turned off. Q_2 keeps turning on until the inductor current reaches the negative current limit. If the overvoltage condition is corrected and the output voltage drops to the nominal voltage, the controller resumes normal PWM switching.

6.5 Over-Temperature Protection (OTP)

The ISL81100 incorporates an over-temperature protection circuit that shuts the IC down when the die temperature reaches +153°C. Normal operation resumes when the die temperature drops below +144°C through the initiation of a complete soft-start cycle. During OTP shutdown, the IC consumes only 100µA current. When the controller is disabled, thermal protection is inactive. This feature helps achieve a low shutdown current of 5µA.

7. Layout Guidelines

Careful attention to layout requirements is necessary to implement an ISL81100-based DC/DC converter successfully. The ISL81100 switches at a very high frequency, so the switching times are very short. At these switching frequencies, even the shortest trace has significant impedance. Also, the peak gate drive current rises significantly in an extremely short time. The transition speed of the current from one device to another causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, generate EMI, and increase device voltage stress and ringing. Careful component selection and proper Printed Circuit Board (PCB) layout minimize the magnitude of these voltage spikes.

The three sets of critical components in a DC/DC converter using the ISL81100 are:

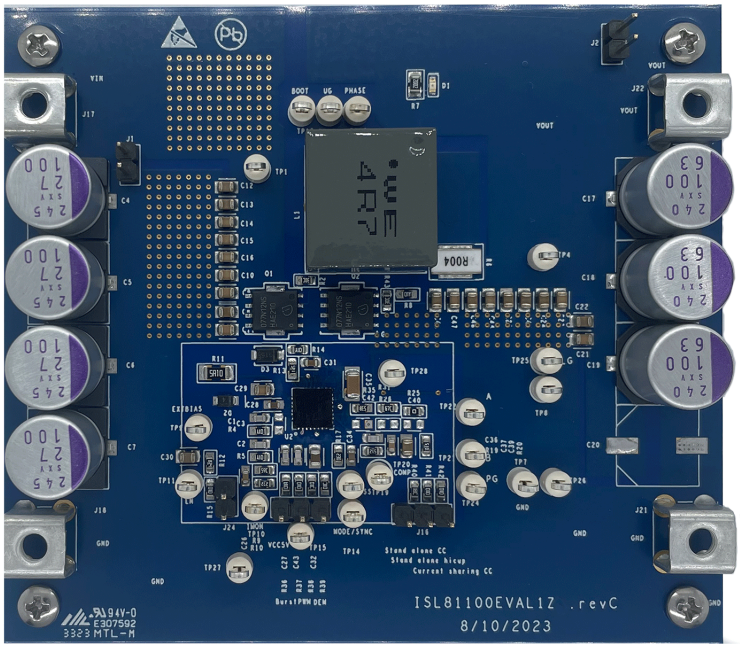
- Controller
- Switching power components
- Small signal components

The switching power components are the most critical from a layout point of view because they switch a large amount of energy, which tends to generate a large amount of noise. The critical small signal components are those connected to sensitive nodes or those supplying essential bias currents. Renesas recommends using a multilayer PCB.

7.1 Layout Considerations

- Place the input capacitors, buck FETs, inductor, and output capacitor first. Isolate these power components on dedicated areas of the board with their ground terminals adjacent to one another. Place the input and output high-frequency decoupling ceramic capacitors close to the MOSFETs.
- If signal components and the IC are placed separately from the power train, use full ground planes in the internal layers with shared SGND and PGND to simplify the layout design. Otherwise, use separate planes for the power and small-signal grounds. Connect the SGND and PGND close to the IC. DO NOT connect them anywhere else.
- Keep the loop formed by the input capacitor, the buck top FET, and the buck bottom FET as small as possible.
- Keep the current paths from the input capacitor to the buck FETs, the power inductor, and the output capacitor as short as possible with maximum allowable trace widths.
- Place the PWM controller IC close to the lower FETs. The low-side FET gate drive connections should be short and wide. Place the IC over a quiet ground area. Avoid switching ground loop currents in this area.
- Place the VDD bypass capacitor close to the VDD pin of the IC and connect its ground end to the PGND pin. Connect the PGND pin to the ground plane using a via. Do not directly connect the PGND pin to the SGND EPAD.
- Place the gate drive components (BOOT diodes and BOOT capacitors) together near the controller IC.
- Place the output capacitors as close to the load as possible. Use short, wide copper regions to connect output capacitors to load to avoid inductance and resistances.
- Use copper-filled polygons or wide short traces to connect the junction of the upper FET, lower FET, and output inductor. Also, keep the PHASE node's connection to the IC short. DO NOT oversize the copper islands for the PHASE nodes. Because the phase nodes are subject to high dv/dt voltages, the stray capacitor formed between these islands and the surrounding circuitry tends to couple switching noise.
- Route all high-speed switching nodes away from the control circuitry.
- Create a separate small analog ground plane near the IC. Connect the SGND pin to this plane. Connect all small signal grounding paths, including feedback resistors, current monitoring resistors and capacitors, soft-starting capacitors, loop compensation capacitors and resistors, and EN pull-down resistors to this SGND plane.
- Use a pair of traces with a minimum loop for the input or output current sensing connection.
- Ensure the feedback connection to the output capacitor is short and direct.

The ISL81100EVAL1Z shows an example of a good layout.



7.2 General EPAD Design Considerations

Figure 43 shows how to use vias to remove heat from the IC.

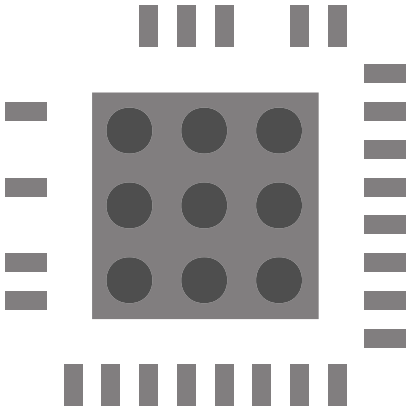


Figure 43. PCB Via Pattern

Fill the thermal pad area with vias. A typical via array fills the thermal pad footprint so that their centers are three times the radius apart from each other. Keep the vias small but not so small that their inside diameter prevents the solder from wicking through during reflow.

Connect all vias to the ground plane. The vias must have low thermal resistance for efficient heat transfer. Ensure a complete connection of the plated through hole to each plane.

8. Component Selection Guideline

8.1 MOSFET Considerations

The MOSFETs are chosen for optimum efficiency given the potentially wide input voltage range and output power requirement. Select these MOSFETs based on $r_{DS(ON)}$, gate supply requirements, and thermal management considerations.

The maximum V_{IN} voltage decides the maximum operation voltage of the MOSFET. Choose the MOSFETs based on their maximum operation voltage with sufficient margin for safe operation.

The power dissipation of the MOSFET is based on conduction loss and switching loss. Use Equation 11 to calculate the power loss of the upper MOSFET and Equation 12 to calculate the lower MOSFETs.

(EQ. 11) $$P_{UPPER} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{OUT})}{V_{IN}} + \frac{(I_{OUT})(V_{IN})(t_{SW})(f_{SW})}{2}$$

(EQ. 12) $$P_{LOWER} = \frac{(I_{OUT}^2)(r_{DS(ON)})(V_{IN} - V_{OUT})}{V_{IN}}$$

The conduction losses are the primary source of power dissipation for the lower MOSFET. Only the upper MOSFET has significant switching losses because the lower device turns on and off into near zero voltage. The equations assume linear voltage-current transitions and do not model power loss because of the reverse recovery of the lower MOSFET body diode. These equations also take $V_{OUT} \times I_{OUT}^2 / V_{IN}$ instead of I_{RMS}^2 because the two values are very close.

A large gate charge increases the switching time (t_{SW}), which increases the switching losses of the buck upper MOSFETs. Ensure all four MOSFETs are within their maximum junction temperature at high ambient temperature by calculating the temperature rise according to package thermal resistance specifications.

8.2 Inductor Selection

The inductor is selected to meet the output voltage ripple requirements. The inductor value determines the converter's ripple current, and the ripple voltage is a function of the ripple current and the output capacitor(s) ESR. The capacitor selection section gives the ripple voltage expression, and the ripple current is approximated by Equation 13.

(EQ. 13) $$\Delta I_{L(BUCK)} = \frac{(V_{IN} - V_{OUT})(V_{OUT})}{(f_{SW})(L)(V_{IN})}$$

The ripple current ratio is usually 30% to 70% of the average inductor current at the full output load condition.

8.3 Output Capacitor Selection

In general, select the output capacitors to meet the dynamic regulation requirements, including ripple voltage and load transients. The selection of output capacitors depends on the inductor, so some inductor analysis is required to select the output capacitors.

One of the parameters limiting the converter's response to a load transient is the time required for the inductor current to slew to its new level. The ISL81100 provides either 0% or maximum duty cycle in response to a load transient.

The response time is the interval required to slew the inductor current from an initial current value to the load current level. During this interval, the difference between the inductor current and the transient current level must be supplied by the output capacitor(s). The output capacitance is minimized if faster loop compensation is used. Also, if the load transient rise time is slower than the inductor response time, it reduces the requirement on the output capacitor.

The maximum capacitor value required to provide the complete, rising step transient load current during the response time of the inductor is shown in Equation 14, where C_{OUT} is the output capacitor(s) required, L is the inductor, I_{TRAN} is the transient load current step, V_{IN} is the input voltage, V_{OUT} is the output voltage, and DV_{OUT} is the drop in output voltage allowed during the load transient.

(EQ. 14) $$C_{OUT} = \frac{(L)(I_{TRAN})^2}{2(V_{IN} - V_{OUT})(DV_{OUT})}$$

High-frequency capacitors initially supply the transient current and slow the load rate of change seen by the bulk capacitors. The Equivalent Series Resistance determines the bulk filter capacitor values (ESR), voltage rating, and actual capacitance requirements.

The output voltage ripple is a combination of the inductor ripple current and the ESR of the output capacitors as defined by Equation 15, where ΔI_{LBUCK} is calculated in Equation 13.

(EQ. 15) $$V_{RIPPLE} = \Delta I_{LBUCK}(ESR)$$

Place high-frequency decoupling capacitors as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the usefulness of these low inductance components. Consult with the manufacturer of the load circuitry for specific decoupling requirements.

Use only specialized low-ESR capacitors intended for switching regulator applications for bulk capacitors. In most cases, multiple small-case electrolytic capacitors perform better than one large one.

The stability requirement on the output capacitor selection is that the ESR zero (f_Z) is between 2kHz and 60kHz. The ESR zero can help increase the phase margin of the control loop. Equation 16 shows this requirement.

(EQ. 16) $$C_{OUT} = \frac{1}{2\pi(ESR)(f_Z)}$$

In conclusion, the output capacitors must meet the following criteria:

- They must have sufficient bulk capacitance to sustain the output voltage during a load transient while the output inductor current is slewing to the value of the load transient.
- Due to the supplied ripple current, the ESR must be sufficiently low to meet the required output voltage ripple.
- Place the ESR zero in a large range to provide an additional phase margin.

8.4 Input Capacitor Selection

The critical parameters for the input capacitor(s) are the voltage rating and the RMS current rating. For reliable operation, select input capacitors with voltage and current ratings above the maximum input voltage and largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage, and 1.5 times is a conservative guideline. The AC RMS input current varies with the load given in Equation 17, where D is the duty cycle, ignoring the inductor's ripple current.

(EQ. 17) $$I_{RMS} = \sqrt{D - D^2} \times I_{OUT}$$

The maximum RMS current supplied by the input capacitance occurs at V_{IN} = 2 X V_{OUT}, DC = 50%, as shown in Equation 18:

(EQ. 18) $$I_{RMS} = \frac{1}{2} \times I_{OUT}$$

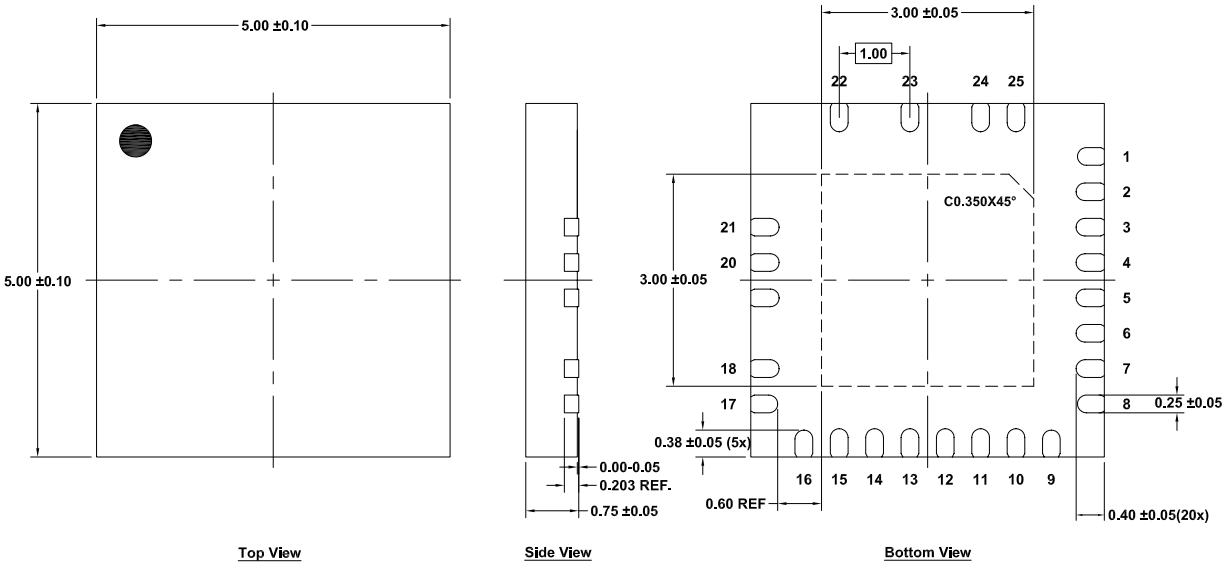
Use a mix of input bypass capacitors to control the voltage ripple across the MOSFETs. Use ceramic capacitors for the high-frequency decoupling and bulk capacitors to supply the RMS current. Place small ceramic capacitors close to the MOSFETs to suppress the voltage induced by parasitic circuit impedances.

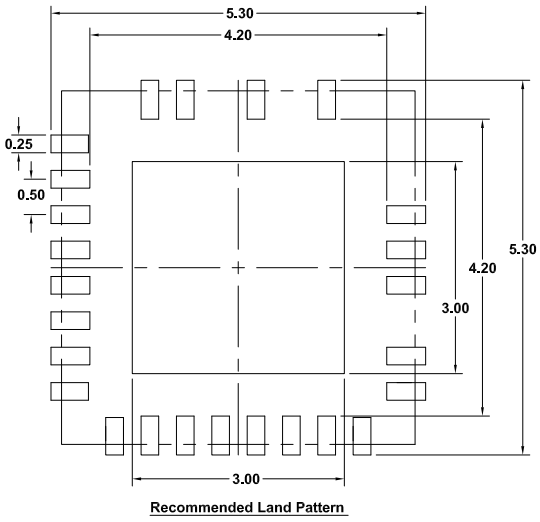
Solid tantalum capacitors can be used, but use caution concerning the capacitor surge current rating. These capacitors must be capable of handling the surge current at power-up.

9. Package Outline Drawing

For the most recent package outline drawing, see L25.5x5.

L25.5x5
25 Lead Thin Quad Flat No-Lead Plastic Package (TQFN)
Rev 0, 6/2022





Notes

1. Dimensions and tolerancs conform to ASME Y 14.5M - 1994.
2. All dimensions are in millimeters.
3. Dimensions in ( ) for reference only.

10. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temp. Range
ISL81100FRTZ-T	81100 FRTZ	25 Ld 5x5 QFN	L25. 5X5	Reel, 3k	-40 to +125°C
ISL81100EVAL1Z	Evaluation Board				
ISL81100EVAL2Z	Parallel operation board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. For Moisture Sensitivity Level (MSL), see the ISL81100 device page. For more information about MSL, see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

11. Revision History

Rev.	Date	Description
1.00	Dec 17, 2024	Initial Release

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