

NP35N055YUK

55 V – 35 A – N-channel Power MOS FET
 Application: Automotive

R07DS1002EJ0200
 Rev.2.00
 May 24, 2018

Description

The NP35N055YUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
 $R_{DS(on)} = 6.7 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 18 \text{ A)}$
- Non logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

| Part No. | Lead Plating | Packing | | Package |
|----------------------|---------------|------------------|------------------|------------|
| NP35N055YUK-E1-AY *1 | Pure Sn (Tin) | Tape 2500 p/reel | Taping (E1 type) | 8-pin HSON |
| NP35N055YUK-E2-AY *1 | | | Taping (E2 type) | |

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

| Item | Symbol | Ratings | Unit |
|---|----------------|-------------|------------------|
| Drain to Source Voltage ($V_{GS} = 0 \text{ V}$) | V_{DSS} | 55 | V |
| Gate to Source Voltage ($V_{DS} = 0 \text{ V}$) | V_{GSS} | ± 20 | V |
| Drain Current (DC) ($T_C = 25^\circ\text{C}$) | $I_{D(DC)}$ | ± 35 | A |
| Drain Current (pulse) *1,4 | $I_{D(pulse)}$ | ± 140 | A |
| Total Power Dissipation ($T_C = 25^\circ\text{C}$) | P_{T1} | 97 | W |
| Total Power Dissipation ($T_A = 25^\circ\text{C}$) *2 | P_{T2} | 1.0 | W |
| Channel Temperature | T_{ch} | 175 | $^\circ\text{C}$ |
| Storage Temperature | T_{stg} | -55 to +175 | $^\circ\text{C}$ |
| Repetitive Avalanche Current *3,4 | I_{AR} | 24 | A |
| Repetitive Avalanche Energy *3,4 | E_{AR} | 58 | mJ |

Thermal Resistance

| | | | |
|---------------------------------------|-------------------|------|--------------------|
| Channel to Case Thermal Resistance | $R_{th(ch-C)}$ *4 | 1.55 | $^\circ\text{C/W}$ |
| Channel to Ambient Thermal Resistance | $R_{th(ch-A)}$ *4 | 150 | $^\circ\text{C/W}$ |

Notes: *1 $T_C = 25^\circ\text{C}$, $P_w \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

*2 Mounted on glass epoxy substrate of 40 mm \times 40 mm \times 1.6 mm with 4% Copper area (35 μm)

*3 $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

*4. Not subject of production test. Verified by design/characterization.

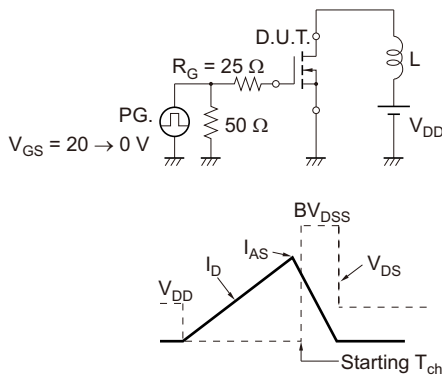
Electrical Characteristics ($T_A = 25^\circ\text{C}$)

| Item | Symbol | MIN. | TYP. | MAX. | Unit | Test Conditions |
|--|--------------|------|------|-----------|---------------|--|
| Zero Gate Voltage Drain Current | I_{DSS} | — | — | 1 | μA | $V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}$ |
| Gate Leakage Current | I_{GSS} | — | — | ± 100 | nA | $V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$ |
| Gate to Source Threshold Voltage | $V_{GS(th)}$ | 2.0 | 3.0 | 4.0 | V | $V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$ |
| Forward Transfer Admittance *1 | $ y_{fs} $ | 18 | 36 | — | S | $V_{DS} = 5\text{ V}, I_D = 18\text{ A}$ |
| Drain to Source On-state Resistance *1 | $R_{DS(on)}$ | — | 5.3 | 6.7 | m Ω | $V_{GS} = 10\text{ V}, I_D = 18\text{ A}$ |
| Input Capacitance *2 | C_{iss} | — | 2240 | 3360 | pF | $V_{DS} = 25\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$ |
| Output Capacitance *2 | C_{oss} | — | 230 | 350 | pF | |
| Reverse Transfer Capacitance *2 | C_{rss} | — | 95 | 180 | pF | |
| Turn-on Delay Time *2 | $t_{d(on)}$ | — | 19 | 38 | ns | $V_{DD} = 28\text{ V}, I_D = 18\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 0\ \Omega$ |
| Rise Time *2 | t_r | — | 9 | 22 | ns | |
| Turn-off Delay Time *2 | $t_{d(off)}$ | — | 47 | 94 | ns | |
| Fall Time *2 | t_f | — | 4 | 10 | ns | |
| Total Gate Charge *2 | Q_G | — | 38 | 57 | nC | $V_{DD} = 44\text{ V}$ |
| Gate to Source Charge | Q_{GS} | — | 10 | — | nC | $V_{GS} = 10\text{ V}$ |
| Gate to Drain Charge | Q_{GD} | — | 10 | — | nC | $I_D = 35\text{ A}$ |
| Body Diode Forward Voltage *1 | $V_{F(S-D)}$ | — | 0.9 | 1.5 | V | $I_F = 35\text{ A}, V_{GS} = 0\text{ V}$ |
| Reverse Recovery Time | t_{rr} | — | 35 | — | ns | $I_F = 35\text{ A}, V_{GS} = 0\text{ V}$ |
| Reverse Recovery Charge | Q_{rr} | — | 41 | — | nC | $di/dt = 100\text{ A}/\mu\text{s}$ |

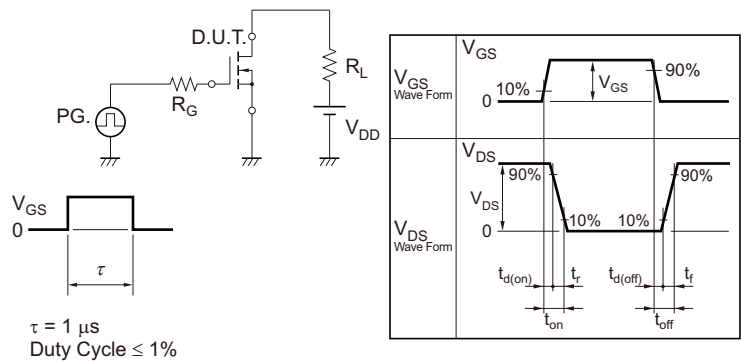
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

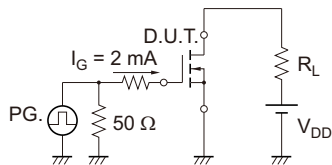
TEST CIRCUIT 1 AVALANCHE CAPABILITY



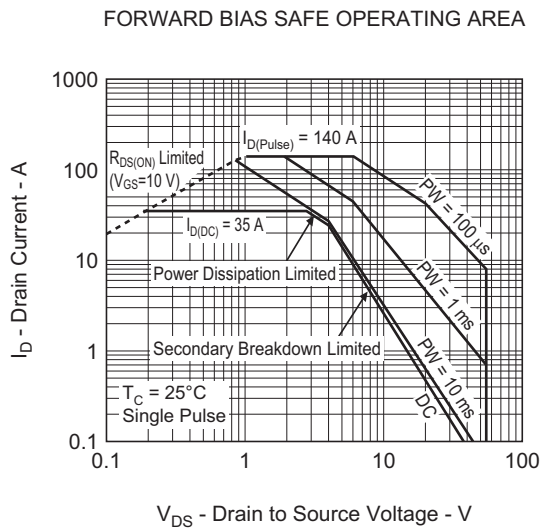
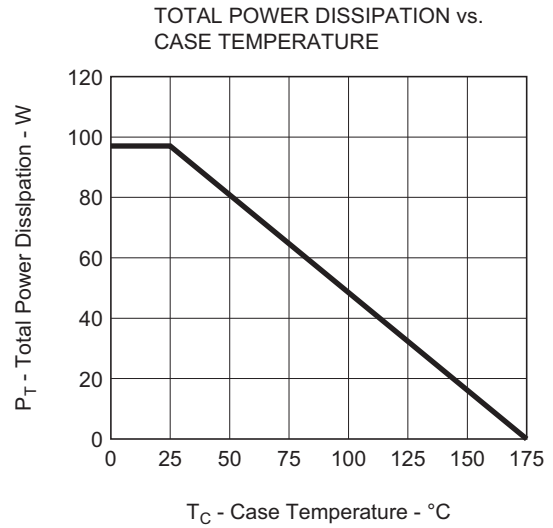
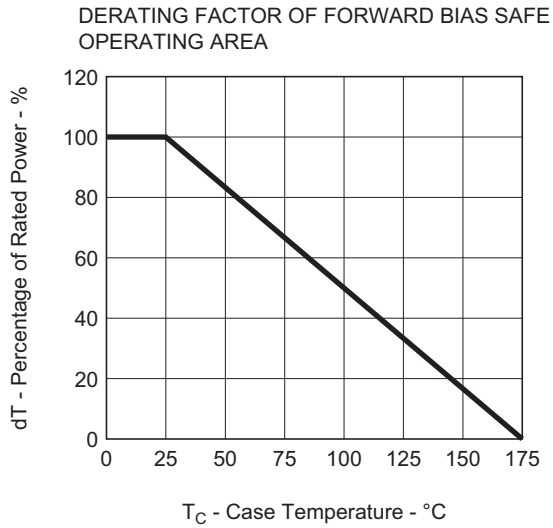
TEST CIRCUIT 2 SWITCHING TIME



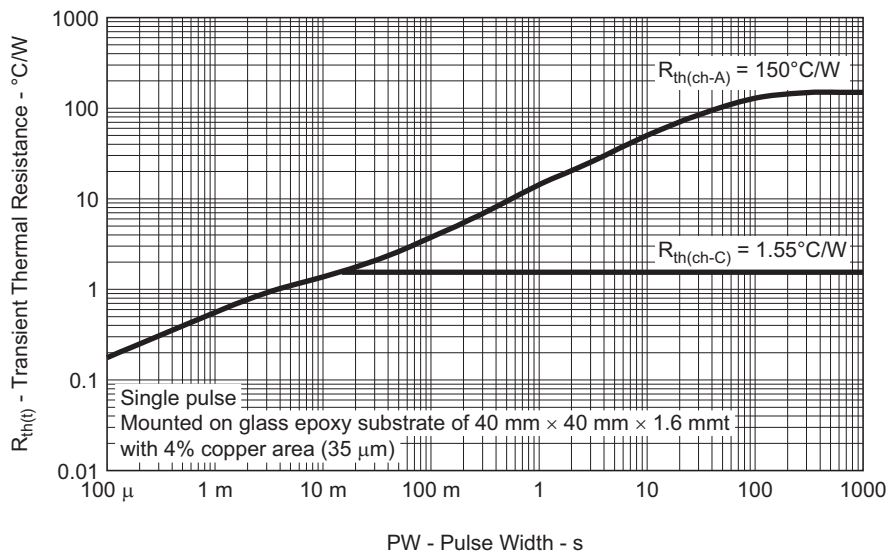
TEST CIRCUIT 3 GATE CHARGE



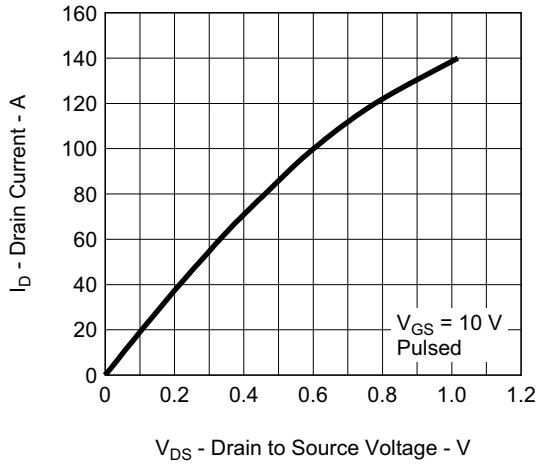
Typical Characteristics (T_A = 25°C)



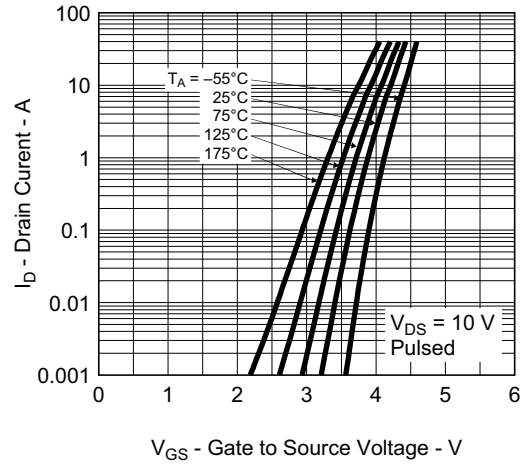
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



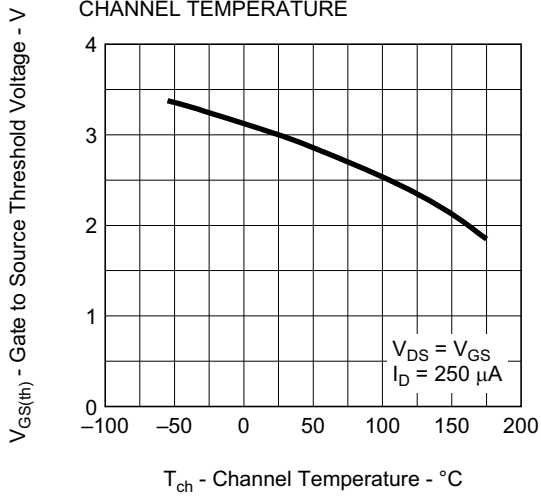
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



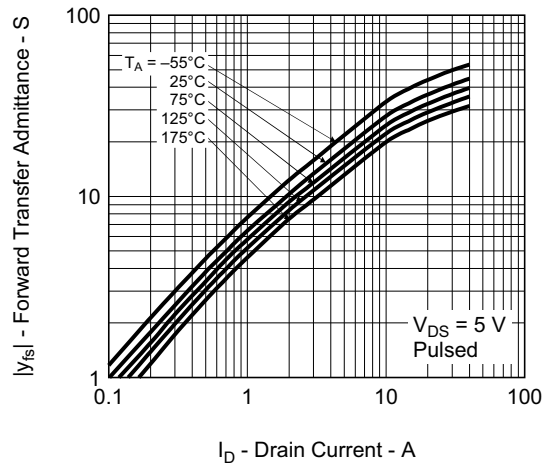
FORWARD TRANSFER CHARACTERISTICS



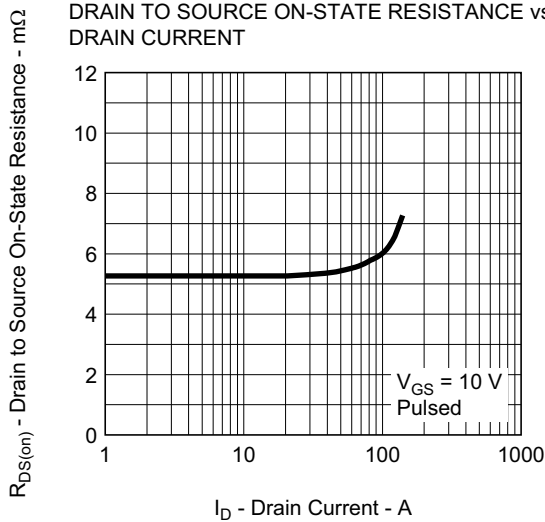
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



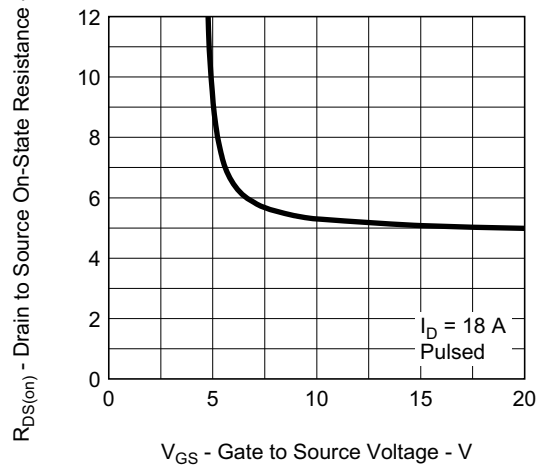
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



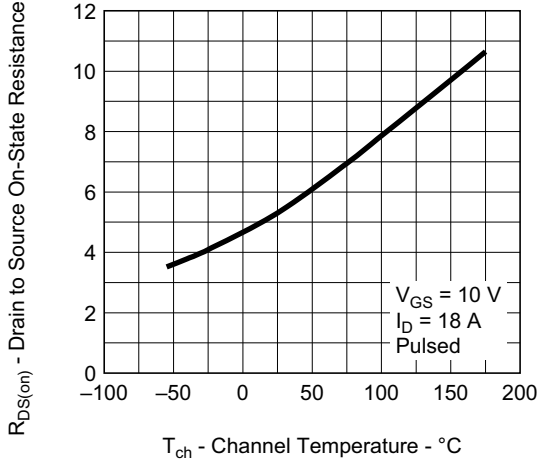
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



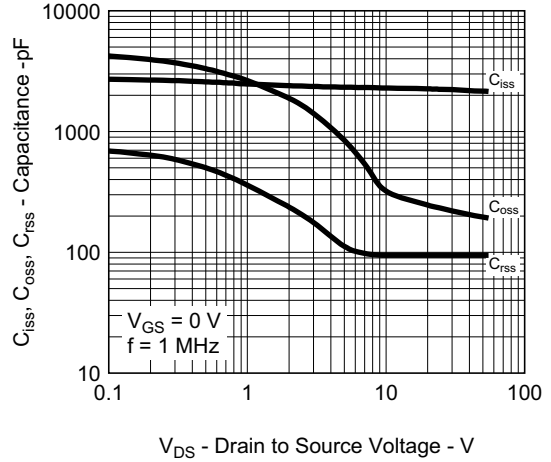
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



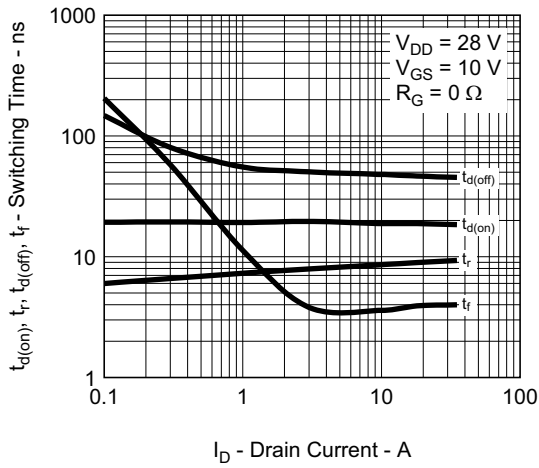
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



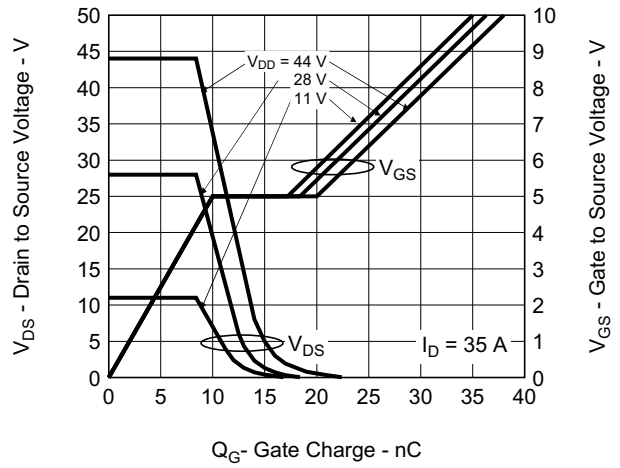
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



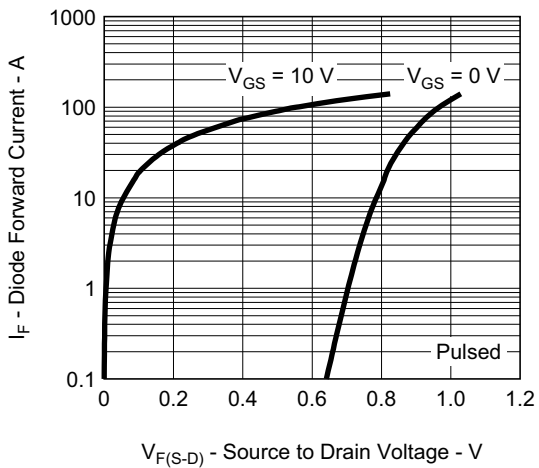
SWITCHING CHARACTERISTICS



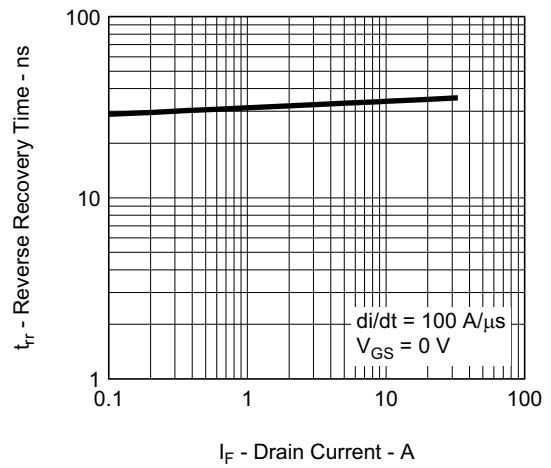
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

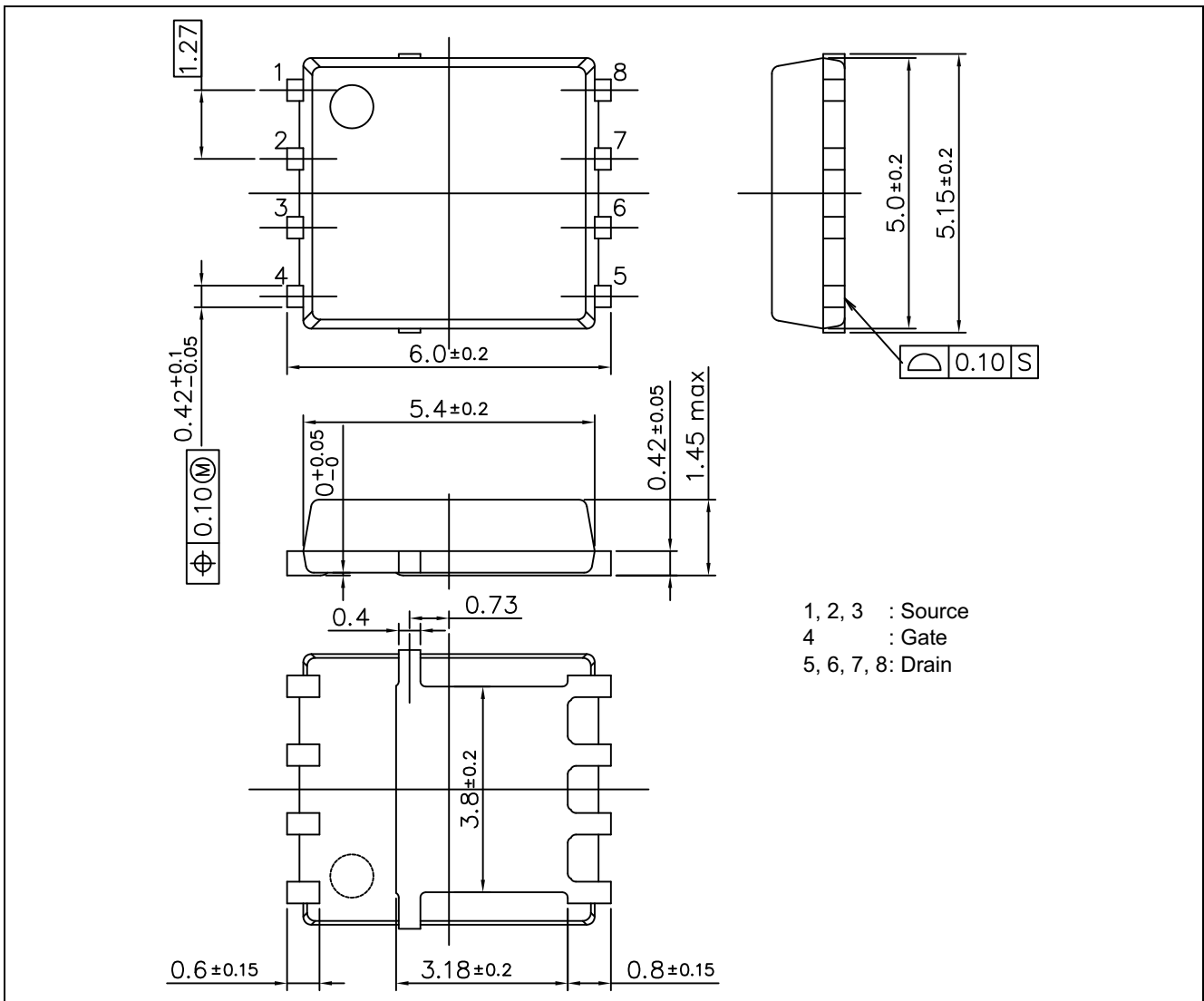


REVERSE RECOVERY TIME vs. DRAIN CURRENT

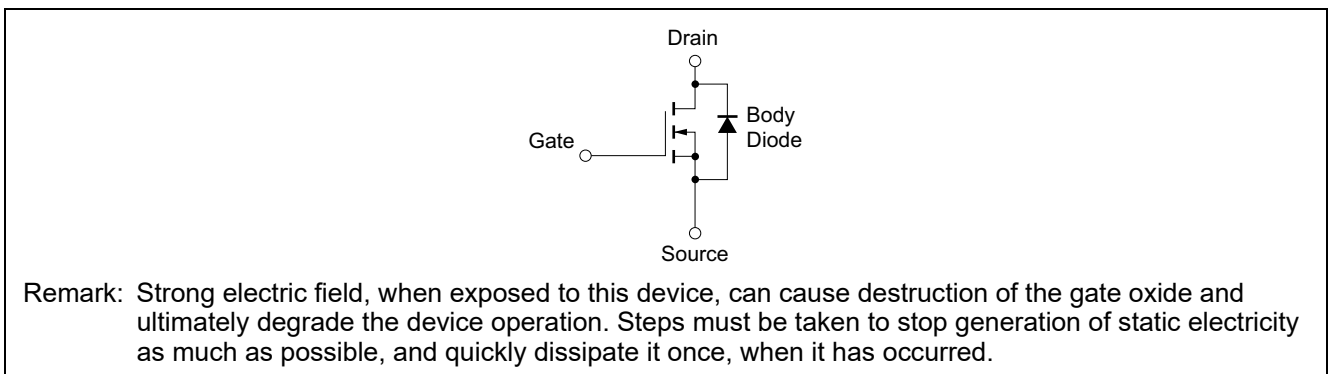


Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)



Equivalent Circuit



| | |
|-------------------------|-------------------------------|
| Revision History | NP35N055YUK Data Sheet |
|-------------------------|-------------------------------|

| Rev. | Date | Description | |
|------|--------------|-------------|----------------------|
| | | Page | Summary |
| 1.00 | Feb 08, 2013 | — | First Edition Issued |
| 2.00 | May 24 ,2018 | 1 | Note 4 was added |
| | | 2 | Note 2 was added |

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