

NP75N055YUK

55 V – 75 A – N-channel Power MOS FET
 Application: Automotive

R07DS1005EJ0200
 Rev.2.00
 May 24, 2018

Description

The NP75N055YUK is N-channel MOS Field Effect Transistors designed for high current switching applications.

Features

- Super low on-state resistance
 $R_{DS(on)} = 4.5 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 38 \text{ A)}$
- Non logic level drive type
- Designed for automotive application and AEC-Q101 qualified

Ordering Information

Part No.	Lead Plating	Packing		Package
NP75N055YUK-E1-AY *1	Pure Sn (Tin)	Tape 2500 p/reel	Taping (E1 type)	8-pin HSON
NP75N055YUK-E2-AY *1			Taping (E2 type)	

Note: *1 Pb-free (This product does not contain Pb in the external electrode)

Absolute Maximum Ratings (T_A = 25°C)

Item	Symbol	Ratings	Unit
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	55	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	±20	V
Drain Current (DC) (T _C = 25°C)	I _{D(DC)}	±75	A
Drain Current (pulse) *1, 4	I _{D(pulse)}	±225	A
Total Power Dissipation (T _C = 25°C)	P _{T1}	138	W
Total Power Dissipation (T _A = 25°C) *2	P _{T2}	1.0	W
Channel Temperature	T _{ch}	175	°C
Storage Temperature	T _{stg}	-55 to +175	°C
Repetitive Avalanche Current *3, 4	I _{AR}	32	A
Repetitive Avalanche Energy *3, 4	E _{AR}	102	mJ

Thermal Resistance

Channel to Case Thermal Resistance	R _{th(ch-C)} *4	1.09	°C/W
Channel to Ambient Thermal Resistance	R _{th(ch-A)} *4	150	°C/W

Notes: *1 T_C = 25°C, P_w ≤ 10 μs, Duty Cycle ≤ 1%

*2 Mounted on glass epoxy substrate of 40 mm × 40 mm × 1.6 mm with 4% Copper area (35 μm)

*3 R_G = 25 Ω, V_{GS} = 20 V → 0 V

*4. Not subject of production test. Verified by design/characterization.

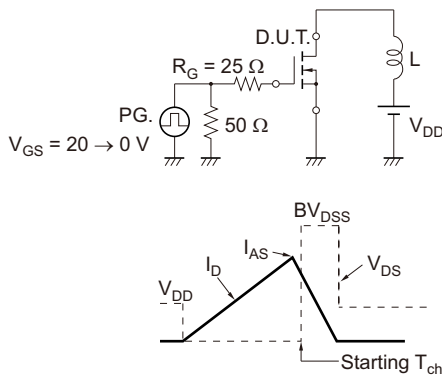
Electrical Characteristics ($T_A = 25^\circ\text{C}$)

Item	Symbol	MIN.	TYP.	MAX.	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	1	μA	$V_{DS} = 55\text{ V}, V_{GS} = 0\text{ V}$
Gate Leakage Current	I_{GSS}	—	—	± 100	nA	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	3.0	4.0	V	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$
Forward Transfer Admittance *1	$ y_{fs} $	30	60	—	S	$V_{DS} = 5\text{ V}, I_D = 38\text{ A}$
Drain to Source On-state Resistance *1	$R_{DS(on)}$	—	3.6	4.5	m Ω	$V_{GS} = 10\text{ V}, I_D = 38\text{ A}$
Input Capacitance *2	C_{iss}	—	3500	5300	pF	$V_{DS} = 25\text{ V}$ $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$
Output Capacitance *2	C_{oss}	—	360	540	pF	
Reverse Transfer Capacitance *2	C_{rss}	—	140	250	pF	
Turn-on Delay Time *2	$t_{d(on)}$	—	24	48	ns	$V_{DD} = 28\text{ V}, I_D = 38\text{ A}$ $V_{GS} = 10\text{ V}$ $R_G = 0\ \Omega$
Rise Time *2	t_r	—	7	17	ns	
Turn-off Delay Time *2	$t_{d(off)}$	—	60	120	ns	
Fall Time *2	t_f	—	5	13	ns	
Total Gate Charge *2	Q_G	—	55	83	nC	$V_{DD} = 44\text{ V}$
Gate to Source Charge	Q_{GS}	—	16	—	nC	$V_{GS} = 10\text{ V}$
Gate to Drain Charge	Q_{GD}	—	13	—	nC	$I_D = 75\text{ A}$
Body Diode Forward Voltage *1	$V_{F(S-D)}$	—	0.9	1.5	V	$I_F = 75\text{ A}, V_{GS} = 0\text{ V}$
Reverse Recovery Time	t_{rr}	—	42	—	ns	$I_F = 75\text{ A}, V_{GS} = 0\text{ V}$
Reverse Recovery Charge	Q_{rr}	—	56	—	nC	$di/dt = 100\text{ A}/\mu\text{s}$

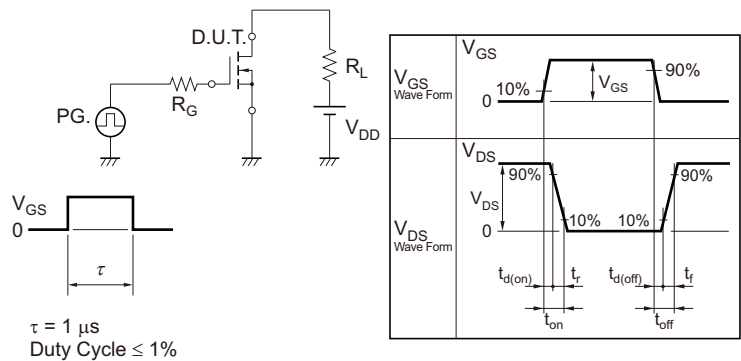
Note: *1 Pulsed test

Note: *2 Not subject of production test. Verified by design/characterization.

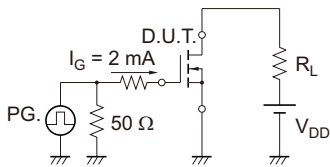
TEST CIRCUIT 1 AVALANCHE CAPABILITY



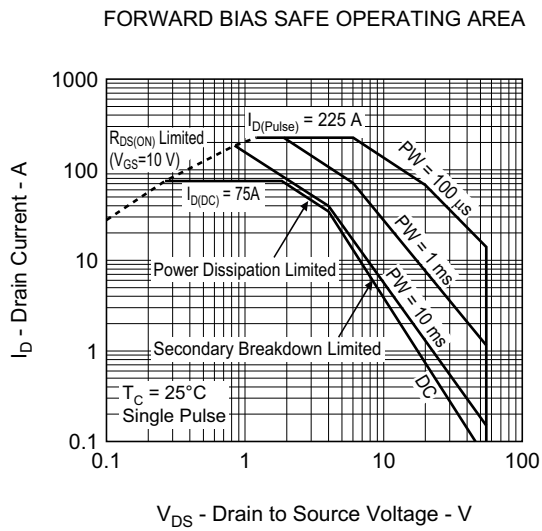
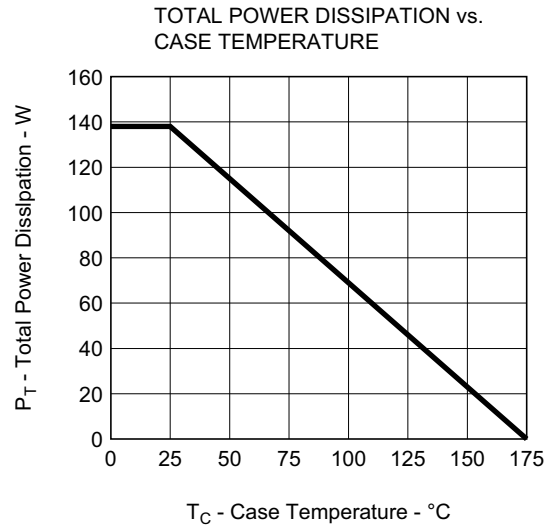
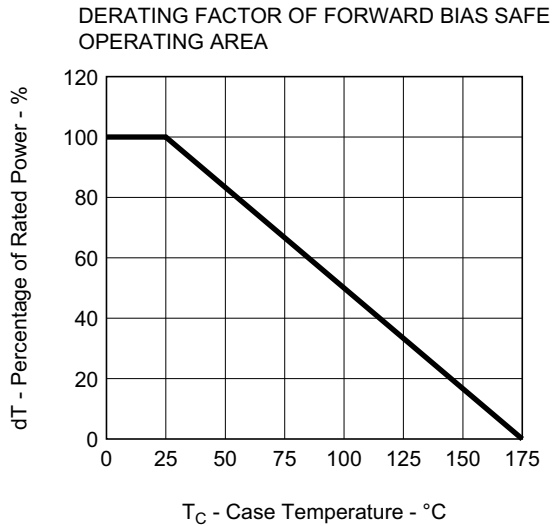
TEST CIRCUIT 2 SWITCHING TIME



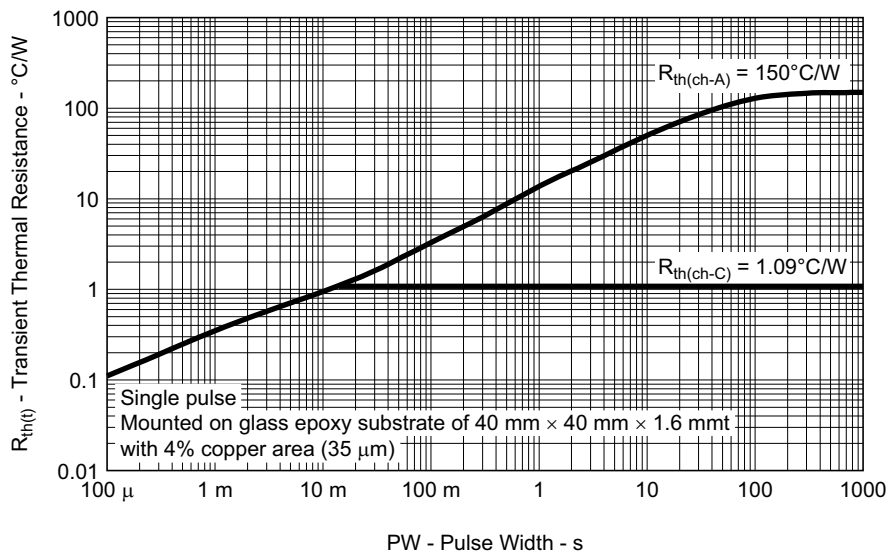
TEST CIRCUIT 3 GATE CHARGE



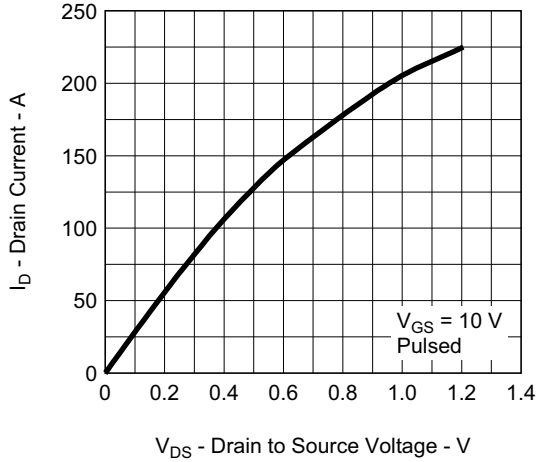
Typical Characteristics (T_A = 25°C)



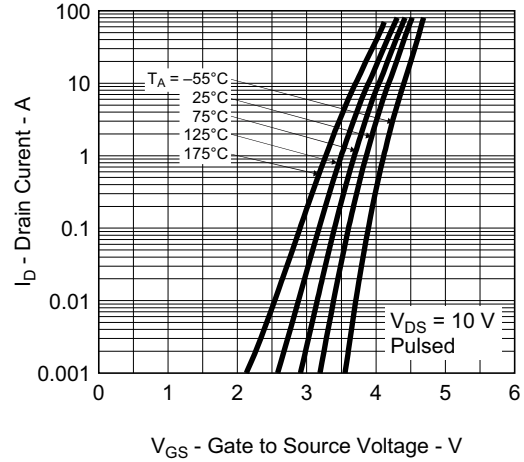
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



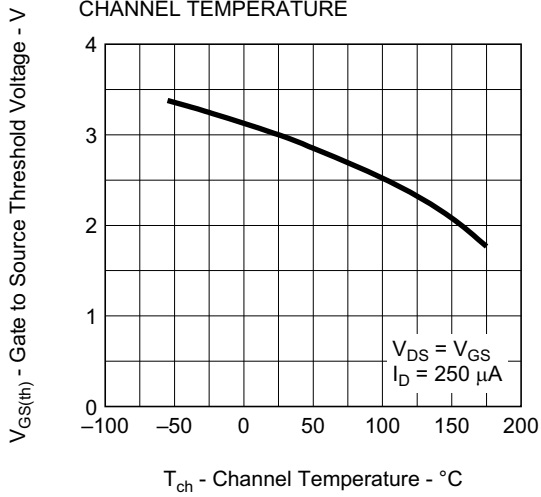
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



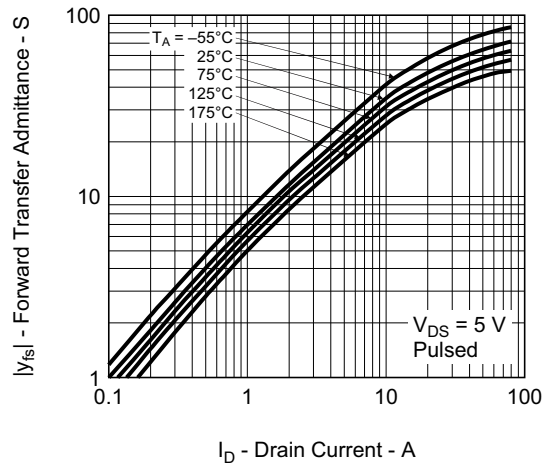
FORWARD TRANSFER CHARACTERISTICS



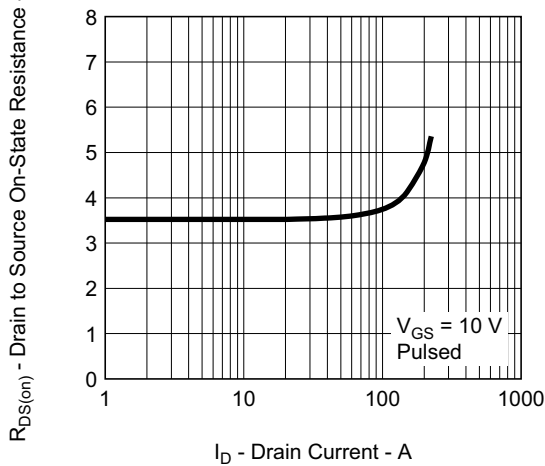
GATE TO SOURCE THRESHOLD VOLTAGE vs. CHANNEL TEMPERATURE



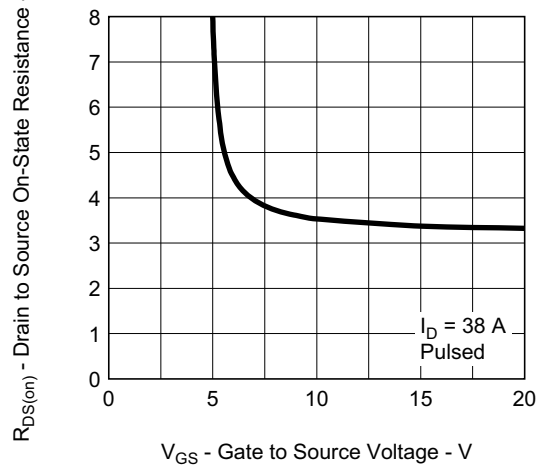
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



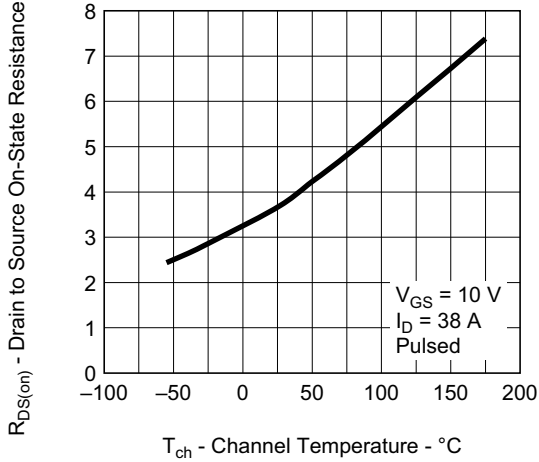
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



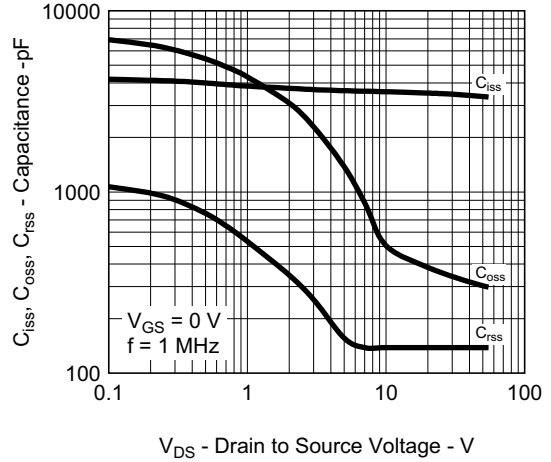
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



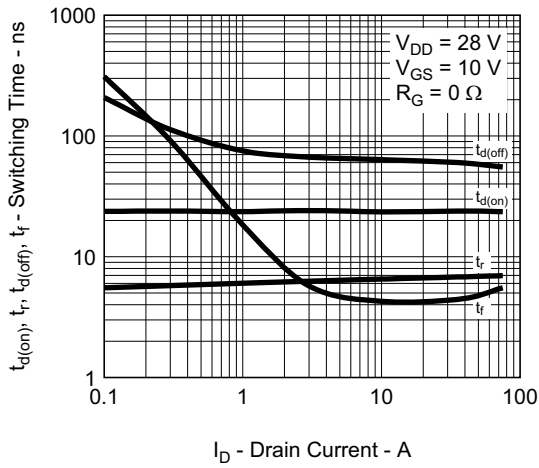
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



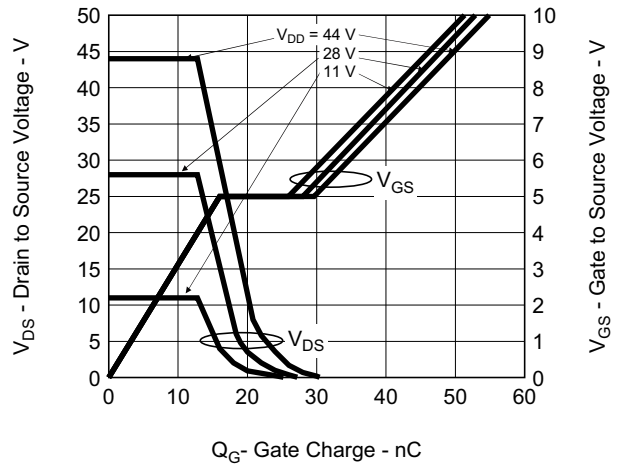
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



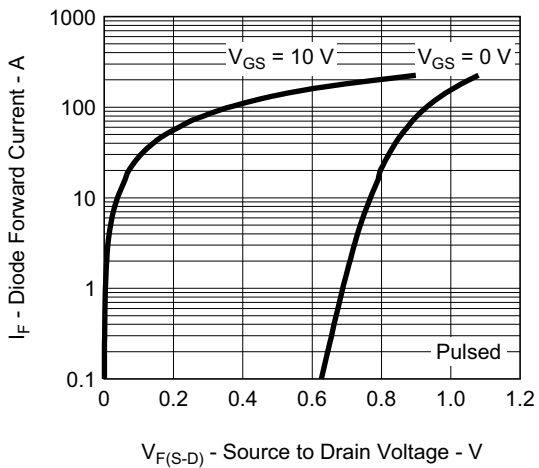
SWITCHING CHARACTERISTICS



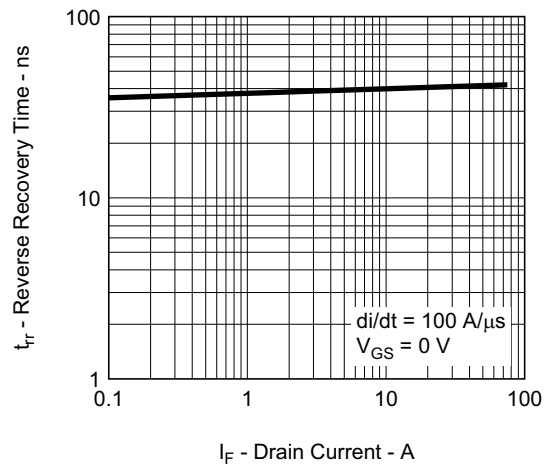
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

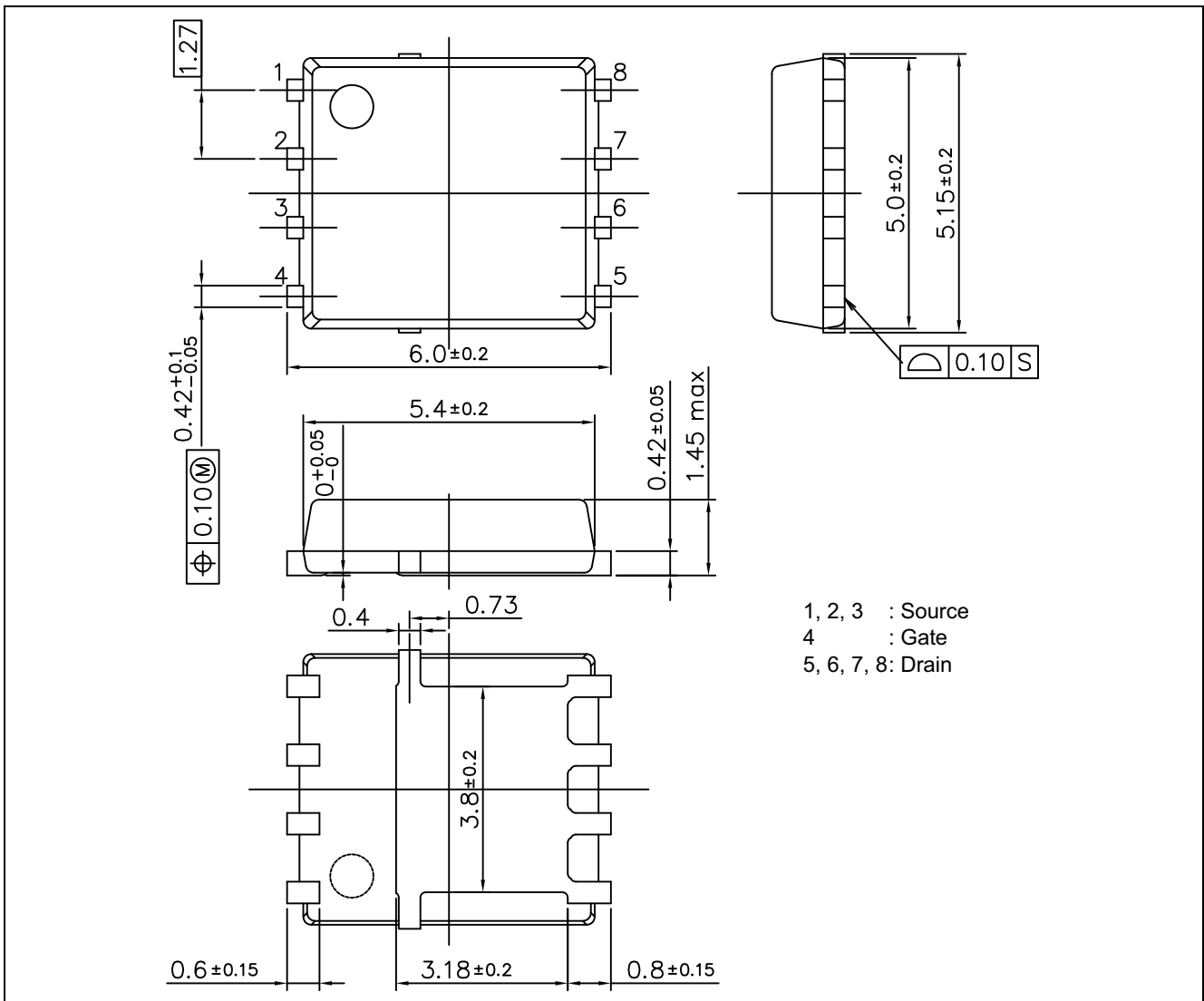


REVERSE RECOVERY TIME vs. DRAIN CURRENT

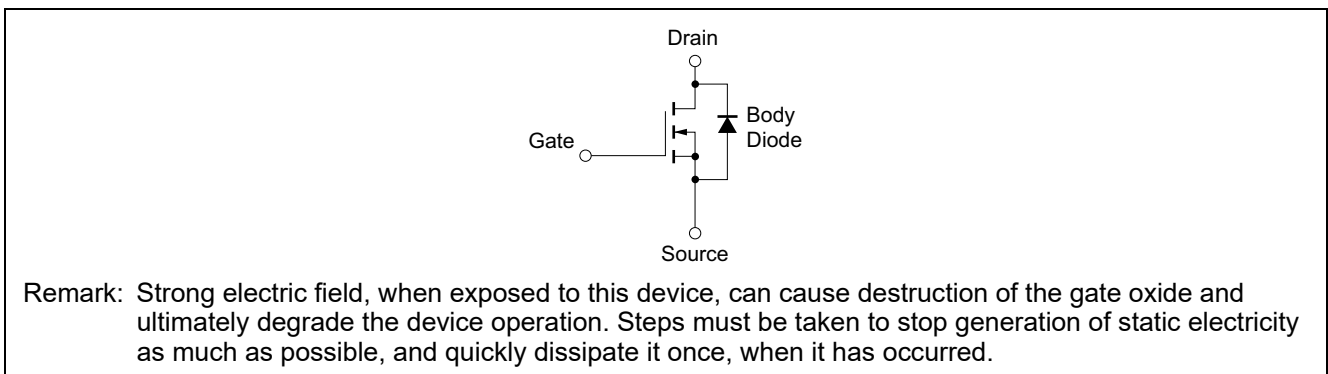


Package Drawing (Unit: mm)

8-pin HSON (Mass: 0.128 g TYP.)



Equivalent Circuit



Revision History	NP75N055YUK Data Sheet
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Rev.	Date	Description	
		Page	Summary
1.00	Feb 08, 2013	—	First Edition Issued
2.00	May 24 ,2018	1	Note 4 was added
		2	Note 2 was added

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