Single Chip Wireless Power Transmitter IC for TX-A1

Product Datasheet

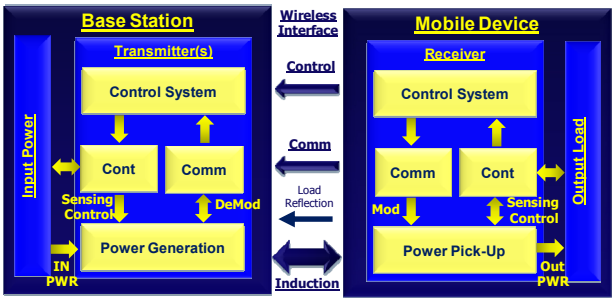
P9030

Features

- Single-Chip 5W Solution for Wireless Power Consortium (WPC)-compliant power transmitter design A1
- Conforms to WPC specification version 1.0 specifications
- 19V Operating Input Voltage
- Integrated Half-Bridge Inverter
- Closed-Loop Power Transfer Control between Base Station and Mobile Device
- Demodulates and Decodes WPC-Compliant Message Packets
- 5V Regulated DC/DC Converter
- Integrated RESET Function
- Proprietary Back –Channel Communication
- I²C Interface
- Open-Drain LED Indicator Outputs
- Over-Temperature/Voltage/Current Protection
- Security and encryption up to 64 bits
- Foreign Object Detection (FOD) for safety

Applications

- WPC-Compliant Wireless Charging Base Stations



Package: 6x6-48 TQFN (See page 27)
Ordering Information (See page 29)

Description

The P9030 is a highly-integrated single-chip WPC-compliant wireless power transmitter IC for power transmitter design A1. The device operates with a 19V (±1V) adapter, and supplies an integrated half-bridge inverter for DC/AC conversion. It controls the transferred power by modulating the switching frequency of the half-bridge inverter from 110kHz to 205kHz at a fixed 50% duty cycle specified by the WPC specification for an "A1" transmitter. It contains logic circuits required to demodulate and decode WPC-compliant message packets sent by the mobile device to adjust the transferred power.

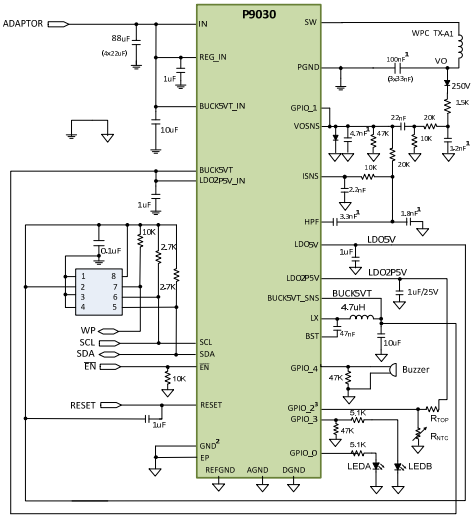
The P9030 is an intelligent device that periodically pings the area surrounding the base station to detect a mobile device for charging while minimizing idle power. Once the mobile device is detected and authenticated, the P9030 continuously monitors all communications from the mobile device, and adjusts the transmitted power accordingly by varying the switching frequency of the half-bridge inverter.

The P9030 features a proprietary back-channel communication mode which enables the device to communicate to IDT's wireless power receiver solutions (e.g. IDTP9020). This feature enables additional layers of capabilities relative to standard WPC requirements.

This device also features optional security and encryptions to securely authenticate the receiver before transferring power. This feature is available when an IDTP9020 is used for the receiver.

The device includes over-temperature/voltage/current protection and a Foreign Object Detection (FOD) method to protect the base station and mobile device from overheating in the presence of a metallic foreign object. It manages fault conditions associated with power transfer and controls status LEDs to indicate operating modes.

Typical Application Circuit



© 2019 Renesas Electronics Corporation

SIMPLIFIED APPLICATION DIAGRAM

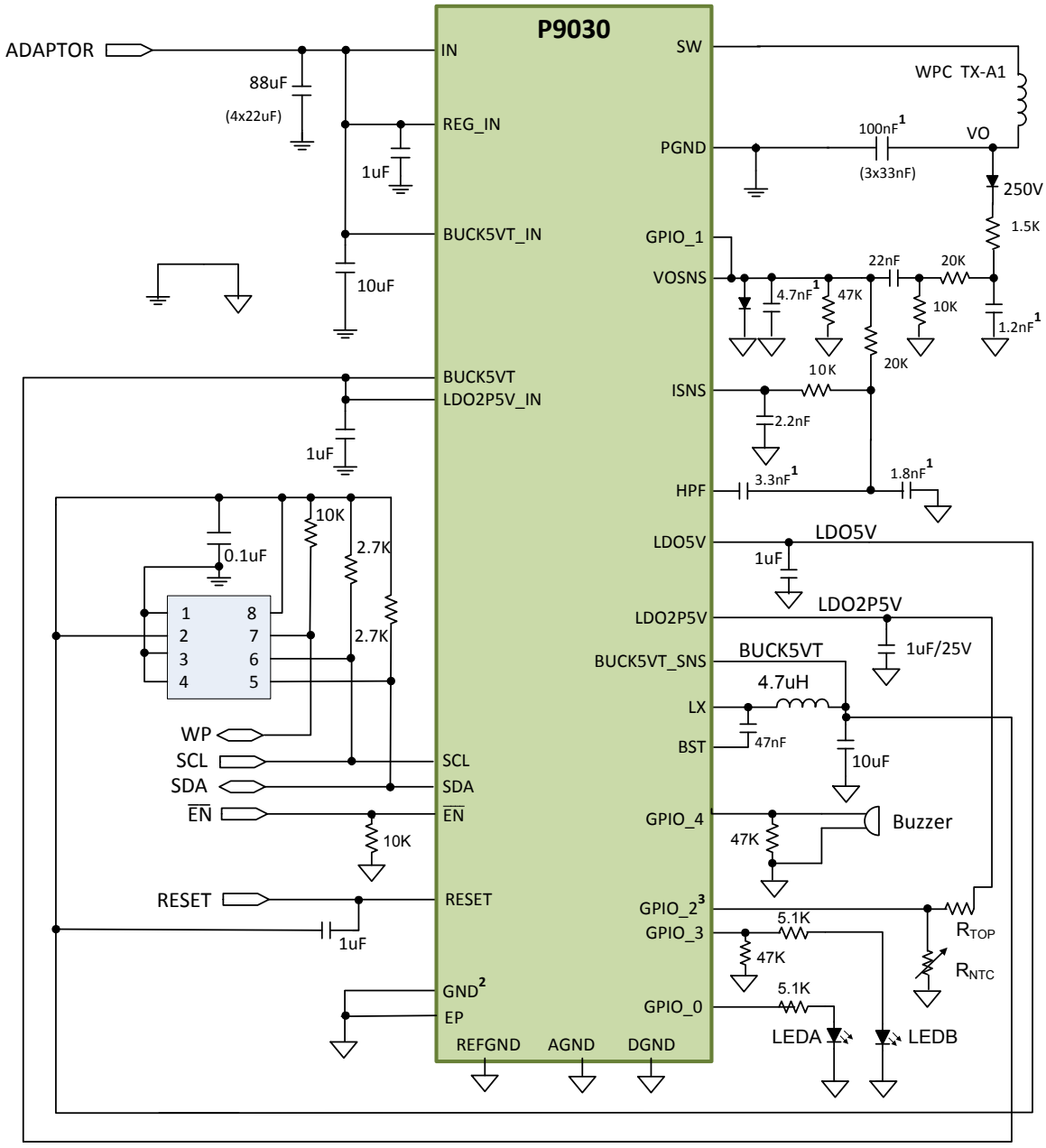


Figure 1. P9030 Simplified Application Schematic

Note 1: NPO/C0G-type ceramic capacitor.
Note 2: For PCB layout, use single-point reference ("star" ground), refer to design schematic in Figure 13).
Note 3: In circuit at GPIO_2, R_{TOP} is required to linearize the temperature range of the thermistor, R_{NTC}. Please contact IDT for a spreadsheet calculator to guide thermistor selection.

© 2019 Renesas Electronics Corporation

ABSOLUTE MAXIMUM RATINGS

These absolute maximum ratings are stress ratings only. Stresses greater than those listed below (Table 1 and Table 2) may cause permanent damage to the device. Functional operation of the P9030 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods may affect long-term reliability.

Table 1. Absolute Maximum Ratings Summary. All voltages are referred to ground, unless otherwise noted.

PINS	MAXIMUM RATING	UNITS
BUCK5VT_IN, IN, REG_IN. **THESE PINS MUST BE CONNECTED TOGETHER AT ALL TIMES.**	-0.3 to 24	V
$\overline{EN}$, LX, SW[5]	-0.3 to 24	V
BST[5]	-0.3 to 29	V
LDO2P5V, XTAL/CLK_IN, XTAL/CLK_OUT	-0.3 to 2.75	V
AGND, DGND, PGND, REFGND	-0.3 to +0.3	V
BUCK5VT_SNS, BUCK5VT, GPIO_0, GPIO_1, GPIO_2, GPIO_3, GPIO_4, GPIO_5, GPIO_6, HPF, ISNS, LDO2P5V_IN, LDO5V, RESET, SCL, SDA, VOSNS	-0.3 to +5.5	V

Table 2. Package Thermal Information

SYMBOL	DESCRIPTION	MAXIMUM RATING	UNITS
θ_{JA}	Thermal Resistance Junction to Ambient (NTG48 - TQFN)	30.8	°C/W
θ_{JC}	Thermal Resistance Junction to Case (NTG48 - TQFN)	14.6	°C/W
θ_{JB}	Thermal Resistance Junction to Board (NTG48 - TQFN)	0.75	°C/W
T_J	Junction Temperature	-40 to +150	°C
T_A	Ambient Operating Temperature	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

Note 1: The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

Note 2: This thermal rating was calculated on JEDEC 51 standard 4-layer board with dimensions 3" x 4.5" in still air conditions.

Note 3: Actual thermal resistance is affected by PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Note 4: For the NTG48 package, connecting the 4.1 mm X 4.1 mm EP to internal/external ground planes with a 5x5 matrix of PCB plated-through-hole (PTH) vias, from top to bottom sides of the PCB, is recommended for improving the overall thermal performance.

Note 5: If the voltage at VIN is less than 24V, limit the voltages on $\overline{EN}$, LX, SW to V(VIN)+0.3V and the voltage on BST to V(VIN)+5V.

© 2019 Renesas Electronics Corporation

Table 3. ESD Information

TEST MODEL	PINS	MAXIMUM RATINGS	UNITS
HBM	All, except IN	±1000	V
	Only IN (37, 38 and 39)	±800	
CDM	All	±500	V

© 2019 Renesas Electronics Corporation

BLOCK DIAGRAM

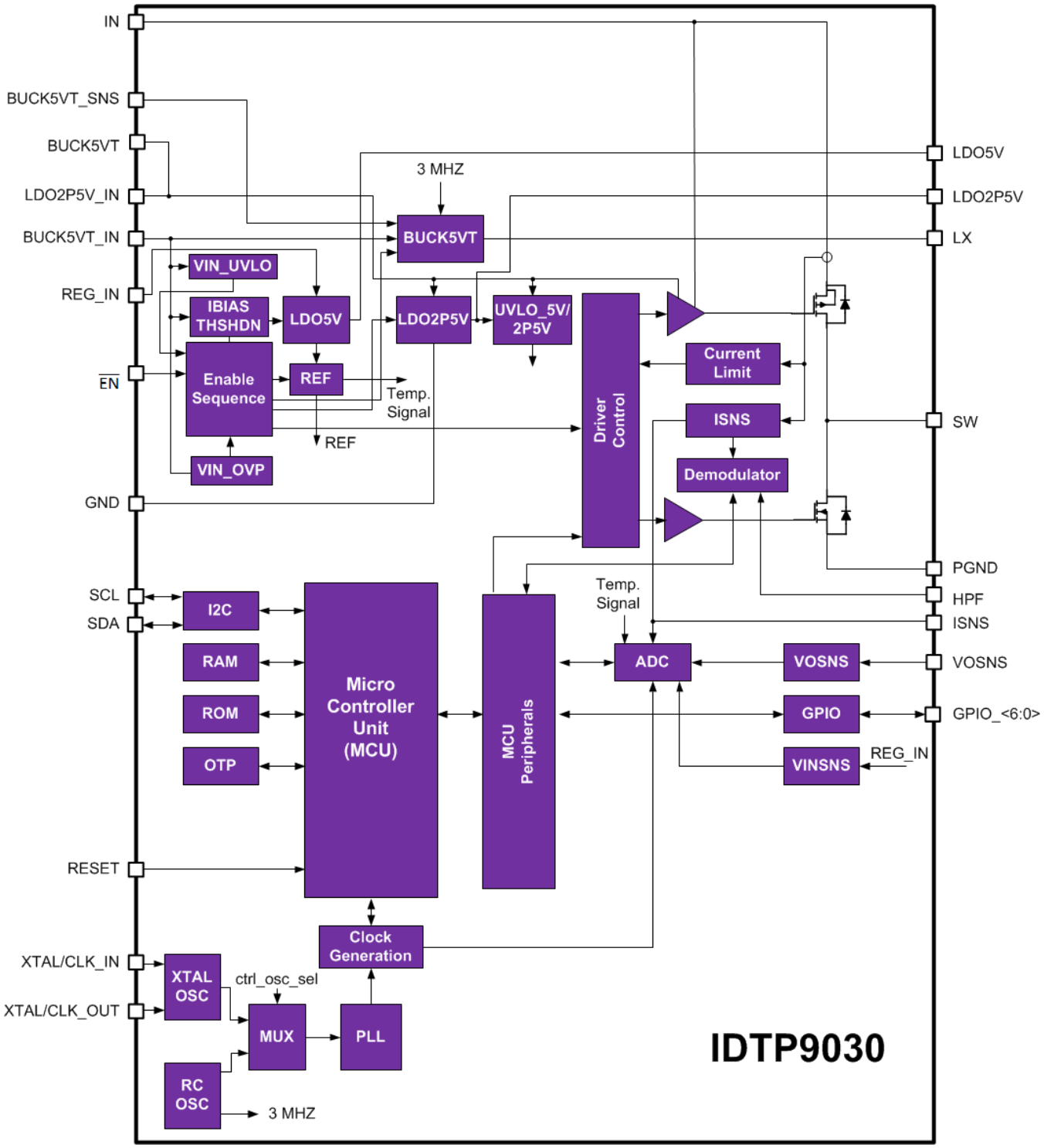


Figure 2. IDTP9030 Internal Functional Block Diagram

© 2019 Renesas Electronics Corporation

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 19V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics

SYMBOL		DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Half-Bridge Inverter							
V_{IN}		Input Supply Operating Voltage Range[1]		18		20	V
I_{IN}[2]	I_{IN_A}	Standby Input Current	After power-up sequence complete. No coil, no load at SW, LDO5V, LDO2P5V, LX. (No wireless power transfer to battery.)		8	15	mA
	I_{IN_S}	Sleep Mode Input Current	$\overline{EN}$ = 5V to V_{IN}			750	µA
F_{SW_LOW}		Switching Frequency at SW	WPC Operating Range, in compliance with WPC requirements	110			kHz
F_{SW_HIGH}						205	kHz
$R_{DS(ON)\_HS}$			Between IN and SW		175		mΩ
$R_{DS(ON)\_LS}$			Between SW and PGND		130		mΩ
UVLO and Inverter OCP							
V_{IN_UVLO}		Under-Voltage Protection Trip Point	V_{IN} rising			10.3	V
			V_{IN} falling	9.0			
			Hysteresis		625		mV
I_{IN_OCP}		Over-Current Protection Trip Point	V_{IN} = 20V, cycle-by-cycle protection.	1.8		2.4	A
DC-DC Converter (For Biasing Internal Circuitry Only)[3]							
$V_{BUCK5VT\_IN}$		Input Voltage Range[1]		18		20	V
$V_{BUCK5VT}$		Output Voltage	External I_{Load} = 25mA	4.5		5.5	V
I_{OUT}		External Load[4]			80		mA
F_{SW}		Switching Frequency at LX			3		MHz
Low Drop Out Regulators (For Biasing Internal Circuitry Only)[3]							
LDO2P5V[3]							
$V_{LDO2P5V\_IN}$		Input Voltage Range	Supplied from BUCK5VT		5		V
$V_{LDO2P5V}$		Output Voltage	I_{Load} = 2mA		2.5		V
I_{OUT}		External Load				5	mA
LDO5V[3]							
V_{REG_IN}		Input Voltage Range	See Note 1.	18		20	V
V_{LDO5V}		Output Voltage	I_{Load} = 2mA		5		V

© 2019 Renesas Electronics Corporation

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 19V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Temperature Rising Threshold		140		°C
		Temperature Falling Threshold		110		
$\overline{EN}$						
V_{IH}				900		mV
V_{IL}				550		mV
$I_{\overline{EN}}$	$\overline{EN}$ input current	$V_{\overline{EN}}$ = 5V		7.5		µA
		$V_{\overline{EN}}$ = V_{IN} = 20V		56		µA
General Purpose Inputs / Outputs (GPIO)						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
V_{OH}	Output Logic High	I_{OH}=-8mA	4			V
V_{OL}	Output Logic Low	I_{OL}=8mA			0.5	V
I_{OH}	Output Current High		-8			mA
I_{OL}	Output Current Low				8	mA
RESET						
V_{IH}	Input Threshold High		3.5			V
V_{IL}	Input Threshold Low				1.5	V
I_{LKG}	Input Leakage		-1		+1	µA
SCL, SDA (I^2C Interface)						
f_{SCL}	Clock Frequency	EEPROM loading, Step 1, P9030 as Master		100		kHz
f_{SCL}	Clock Frequency	EEPROM loading, Step 2, P9030 as Master		300		kHz
f_{SCL}	Clock Frequency	P9030 as Slave	0		400	kHz
$t_{HD;STA}$	Hold Time (Repeated) for START Condition		0.6			µs
$t_{HD;DAT}$	Data Hold Time	CBUS-compatible masters	5			µs
		I^2C-bus devices	10			ns
t_{LOW}	Clock Low Period		1.3			µs
t_{HIGH}	Clock High Period		0.6			µs
$t_{SU;STA}$	Set-up Time for Repeated START Condition		100			ns

© 2019 Renesas Electronics Corporation

ELECTRICAL CHARACTERISTICS

$\overline{EN}$ = RESET = 0V, IN = REG_IN = BUCK5VT_IN = 19V. T_A = -40 to +85°C, unless otherwise noted. Typical values are at 25°C, unless otherwise noted.

Table 4. Device Characteristics, Continued

SYMBOL	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNITS
T_{BUF}	Bus Free Time Between STOP and START Condition		1.3			µs
C_B	Capacitive Load for Each Bus Line				100	pF
C_{BIN}	SCL, SDA Input Capacitance[5]			5		pF
V_{IL}	Input Threshold Low	When powered by device 5V			1.5	V
V_{IH}	Input Threshold High		3.5			V
I_{LKG}	Leakage Current		-1.0		1.0	µA
V_{OL}	Output Logic Low (SDA)	I_{PD}= 2mA (Note 1)			0.5	V
I_{OH}	Output Current High		-2			mA
I_{OL}	Output Current Low				2	mA
Analog-to-Digital Converter						
N	ADC Conversion Resolution			12		Bit
f_{SAMPLE}	Sampling Rate			62.5		KSPS
Channel	Number of Channels at ADC MUX input			8		
ADC_{CLK}	ADC Clock Frequency			1		MHz
V_{IN_FS}	Full-Scale Input Voltage			2.5		V
Microcontroller						
F_{CLOCK}	Clock Frequency			40		MHz
V_{IN}	Input Voltage			2.5		V

Note 1: BUCK5VT_IN, IN, REG_IN. These pins must be connected together at all times.

Note 2: This current is the sum of the input currents for IN, REG_IN and BUCK5VT_IN.

Note 3: DC-DC BUCK5VT, LDO2P5V and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull up resistor loads (up to an absolute maximum of 25mA), as recommended in Figure 13 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials.

Note 4: Any external load at the output of the DC/DC converter must not inject noise onto the output node, and care must be taken with parasitic inductance and capacitance.

Note 5: Guaranteed by design.

© 2019 Renesas Electronics Corporation

PIN CONFIGURATION

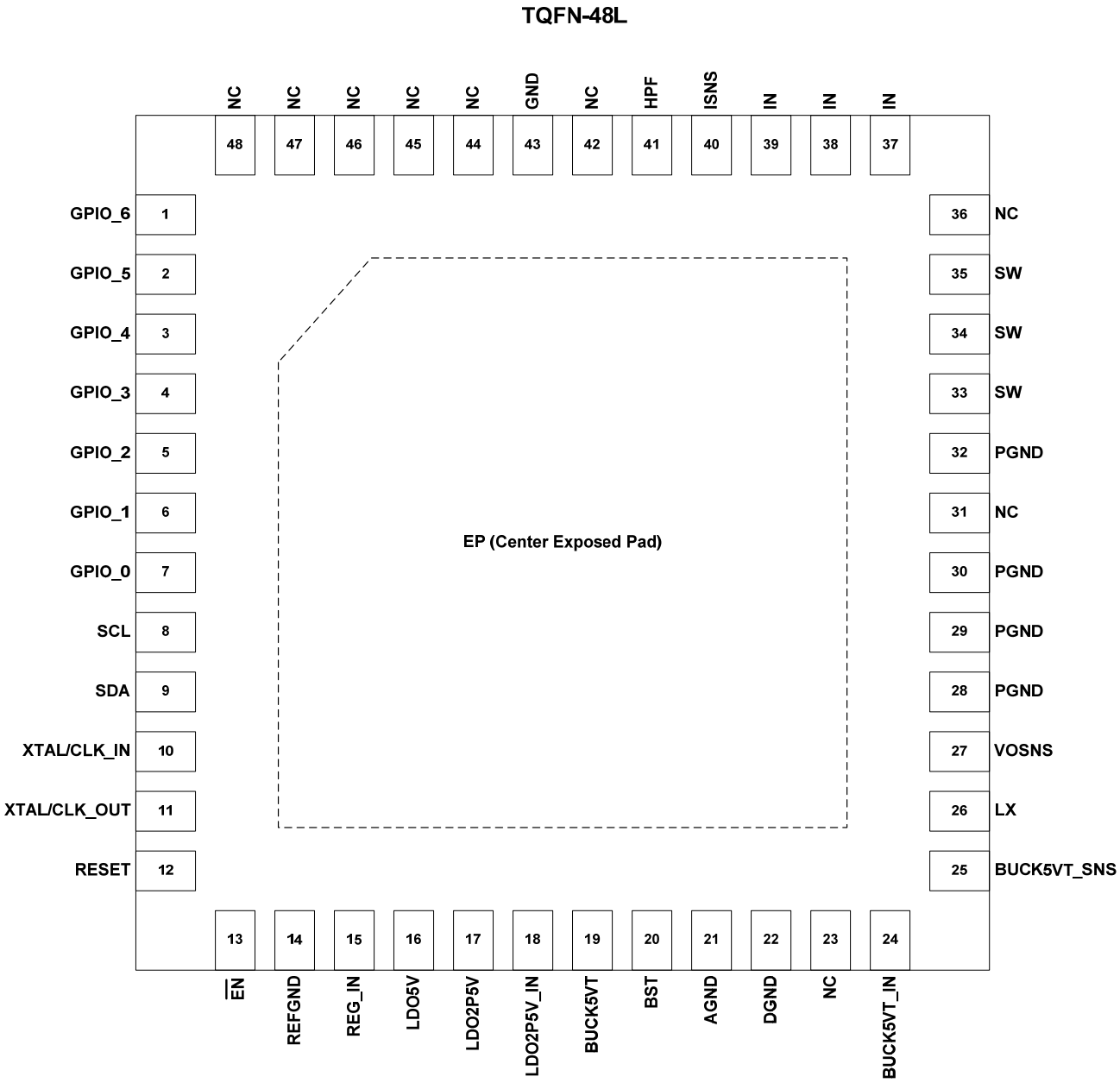


Figure 3. P9030 Pin Configuration (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm, 0.4mm pitch)

© 2019 Renesas Electronics Corporation

PIN DESCRIPTION

Table 5. P9030 NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
1	GPIO_6	I/O	General purpose input/output 6
2	GPIO_5	I/O	General purpose input/output 5
3	GPIO_4	I/O	General purpose input/output 4
4	GPIO_3	I/O	General purpose input/output 3
5	GPIO_2	I/O	General purpose input/output 2
6	GPIO_1	I/O	General purpose input/output 1
7	GPIO_0	I/O	General purpose input/output 0
8	SCL	I/O	I²C clock
9	SDA	I/O	I²C data
10	XTAL/CLK_IN	I	Crystal or clock input. If not used, must be connected to GND.
11	XTAL/CLK_OUT	O	Crystal or clock output. If not used, must be left unconnected.
12	RESET	I	Active-high chip reset pin. A 1µF ceramic capacitor must be connected between this pin and LDO5V, and a 100kΩ resistor to GND.
13	$\overline{EN}$	I	Active-low enable pin. Device is suspended and placed in low current (sleep) mode when pulled high. Tie to GND for stand-alone operation.
14	REFGND	-	Signal ground connection. Must be connected to AGND.
15	REG_IN[1]	I	A 1µF ceramic capacitor must be connected between this pin and GND. This pin must be connected to pins 37, 38, and 39.
16	LDO5V[2]	O	A 1µF ceramic capacitor must be connected between this pin and GND.
17	LDO2P5V[2]	O	2.5V LDO output. A 1µF ceramic capacitor must be connected between this pin and GND.
18	LDO2P5V_IN	I	2.5V LDO input. The LDO2P5V_IN input must be connected to BUCK5VT. A 1µF ceramic capacitor must be connected between this pin and GND.
19	BUCK5VT[2]	I	Power and digital supply input to internal circuitry.

© 2019 Renesas Electronics Corporation

Table 5. P9030 NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
20	BST	I	Bootstrap pin for BUCK converter top switch gate drive supply.
21	AGND	-	Analog ground connection. Connect to signal ground. Must be connected to REFGND.
22	DGND	-	Digital ground connection. Must be connected to GND.
23	NC	NC	Not internally connected.
24	BUCK5VT_IN[1]	I	Buck converter power supply input. Connect 0.1uF and 1µF ceramic capacitors between this pin and PGND.. This pin must be connected to pins 37, 38, and 39.
25	BUCK5VT_SNS	I	Buck regulator feedback. Connect to the high side of the buck converter output capacitor.
26	LX	O	Switch Node of BUCK converter. Connects to one of the inductor's terminals.
27	VOSNS	I	TX-A1 coil voltage sense input.
28	PGND	-	Power ground.
29	PGND	-	Power ground.
30	PGND	-	Power ground.
31	NC	NC	Not internally connected.
32	PGND	-	Power ground.
33	SW	O	Pins 33, 34, and 35 must be connected together. Inverter switch node. Must be connected to capacitor in series with TX-A1 coil.
34	SW	O	
35	SW	O	
36	NC	NC	Not internally connected.
37	IN[1]	I	Inverter power supply input. Connect at least four 22µF x 25V ceramic capacitors and a 0.1µF capacitor between this pin and ground, as close to the pin as possible. Connect all three pins (37, 38, 39) in parallel.
38	IN[1]	I	
39	IN[1]	I	
40	ISNS	O	ISNS output signal

© 2019 Renesas Electronics Corporation

Table 5. P9030 NTG48 Package Pin Functions by Pin Number ()

PIN	NAME	TYPE	DESCRIPTION
41	HPF	I	High pass filter input
42	NC		Internal connection, must be connected to GND.
43	GND	-	Ground
44	NC		Internal connection, must be connected to GND.
45	NC		Internal connection, must be connected to GND.
46	NC		Internal connection, must be connected to GND.
47	NC		Internal connection, must be connected to GND.
48	NC		Internal connection, do not connect.
EP	Center Exposed Pad	Thermal	EP is on the bottom of the package and must be electrically tied to GND. For thermal performance, solder to a large copper pad embedded with a pattern of plated through-hole vias. The die is not electrically bonded to the EP, and the EP must not be used as current-carrying electrical connection.

Note 1: IN, REG_IN, BUCK5VT_IN. These pins must be connected together at all times.

Note 2: DC-DC BUCK5VT, LDO2P5V, and LDO5V are intended only as internal device supplies and must not be loaded externally except for the EEPROM, thermistor, LED, buzzer and pull up resistor loads (up to an absolute maximum of 25mA), as recommended in Figure 13 WPC "Qi" Compliance Schematic and Table 7 WPC "Qi" Compliance Bill of Materials.

© 2019 Renesas Electronics Corporation

TYPICAL PERFORMANCE CHARACTERISTICS

$\overline{EN} = 0$, IN = BUCK5VT_IN = REG_IN = 19V, TA = 25°C. Unless otherwise noted.

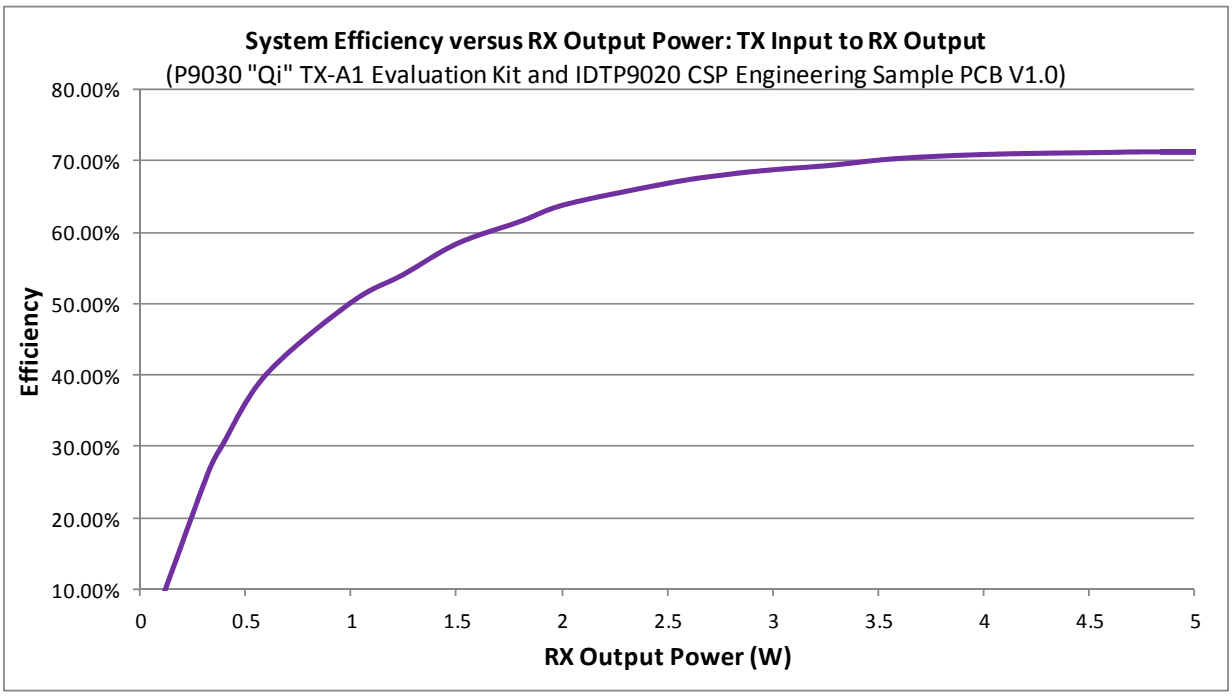


Figure 4. Efficiency vs. RX Output Power with IDTP9020 Receiver

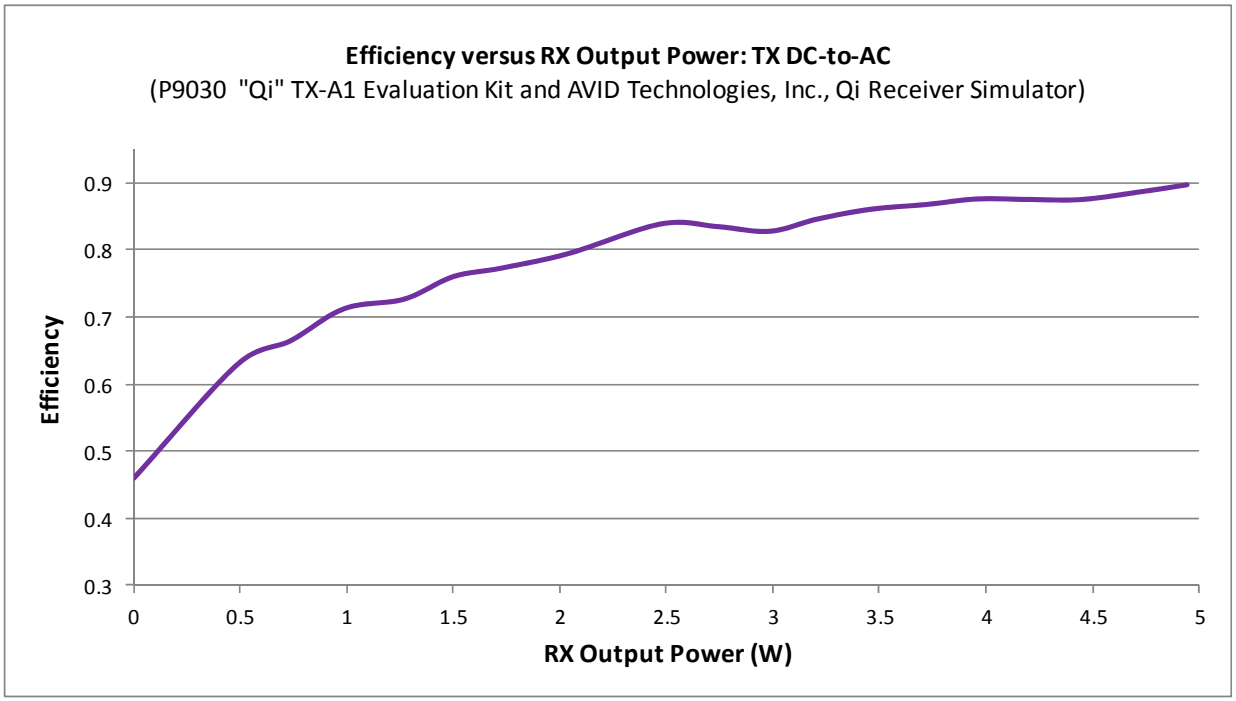


Figure 5. Spacing between TX and RX coils is 2 mm

© 2019 Renesas Electronics Corporation

SYSTEMS APPLICATIONS DIAGRAM

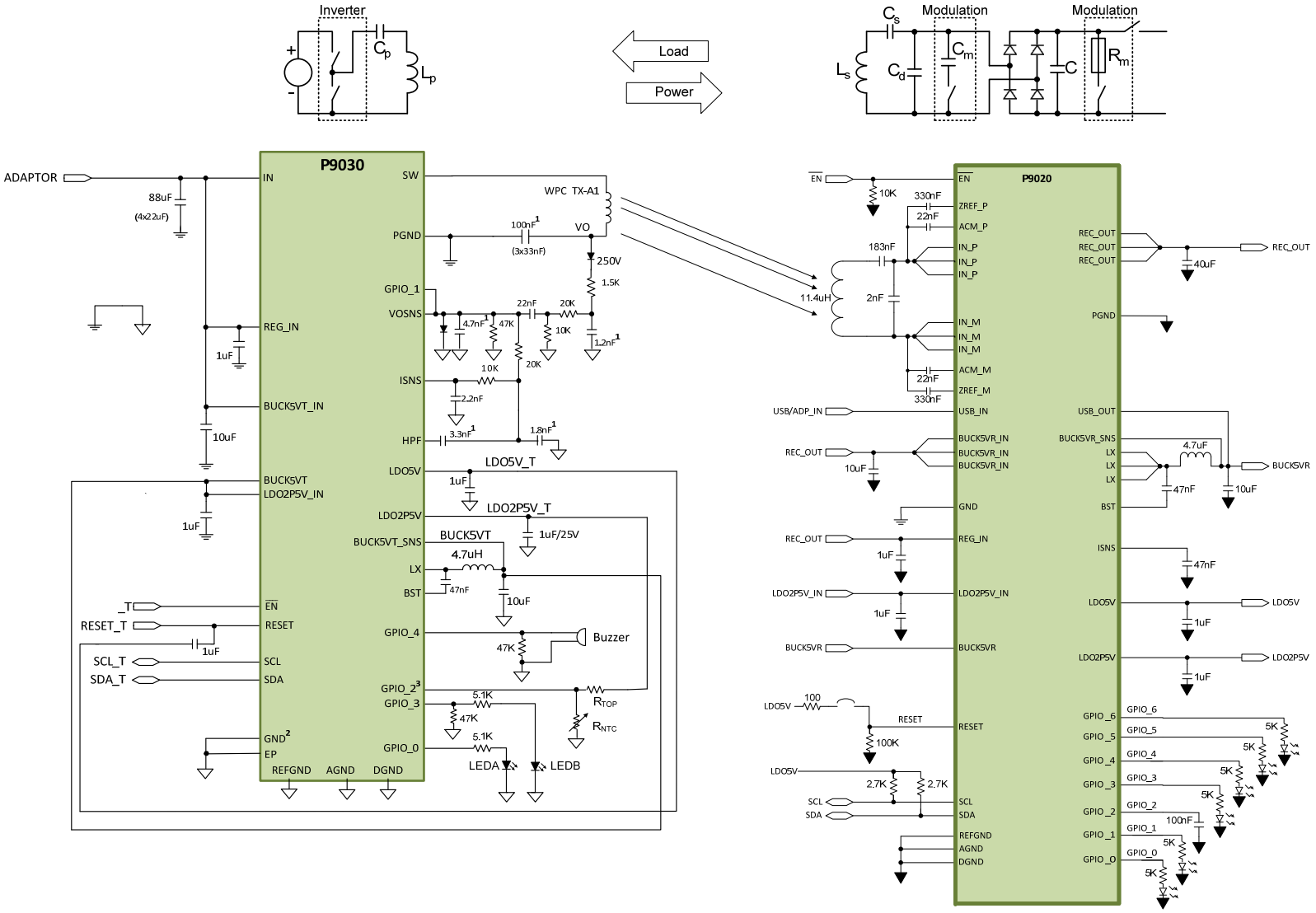


Figure 6. P9030/P9020 Simplified Systems Application Diagram

© 2019 Renesas Electronics Corporation

THEORY OF OPERATION

The P9030 is a highly-integrated WPC[1] (Wireless Power Consortium)-compliant wireless power charging IC solution for the transmitter base station. It can deliver more than 5W of power to the receiver when used with the IDTP9020 or 5W in WPC "Qi" mode using near-field magnetic induction as a means to transfer energy. It is the industry's first single-chip WPC-compliant solution designed to drive a WPC-compliant Type-A1 transmitter coil.

OVERVIEW

Figure 2 shows the block diagram of the P9030. When the VIN_UVLO block detects that the voltage at IN, REG_IN, and BUCK5VT_IN (all connected together externally) is above the Vin_rising threshold and $\overline{EN}$ is at a logic LOW, the Enable Sequence circuitry activates the voltage reference, the 5V and 2.5V LDOs, the 5V buck switching regulator, and the Driver Control for the output inverter.

The voltages at the outputs of the LDOs and the buck regulator are monitored to ensure that they remain in regulation, and the adapter voltage, coil current, and internal temperature are monitored .

The Driver Control block converts a PWM signal from the MCU to the gate drive signals required by the output inverter to drive the external resonant tank.

Communication packets from the receiver in the mobile device are recovered by the Demodulator and converted to digital signals that can be read by the MCU.

Several internal voltages and the external thermistor voltage (through GPIO2) are converted to their digital representations by the ADC and supplied to the MCU.

Five GPIO ports are available to the system designer for measuring an external temperature (ambient or inductor, for example) and driving LEDs and a buzzer.

The clock for the MCU and other circuitry is generated by either an external crystal or an internal RC oscillator.

I²C SDA and SCL pins permit communication with an external device or host.

Note 1 - Refer to the WPC specification at http://www.wirelesspowerconsortium.com/ for the most current information

UNDER VOLTAGE LOCKOUT (UVLO)

The P9030 has a built-in UVLO circuit that monitors the input voltage and enables normal operation, as shown in Figure 7.

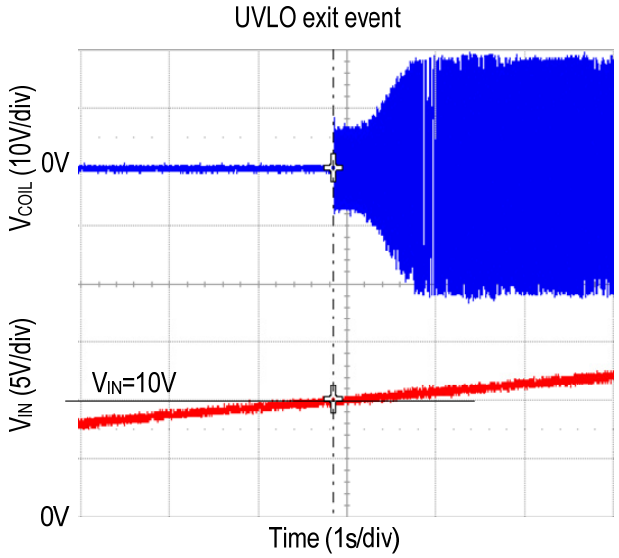


Figure 7. V_{IN} versus UVLO threshold with /EN low.

OVER-CURRENT/VOLTAGE/TEMPERATURE PROTECTION

The current in the inverter is monitored by an analog Current Limit block. If the instantaneous coil current exceeds 2A, the chip is shut down. VIN_OVP monitors the voltage applied to the P9030 by the external AC adapter and shuts the part down if the adapter voltage rises above 24V, to protect against excessive power transfer to the receiver. The internal temperature is also monitored, and the part is temporarily deactivated if the temperature exceeds 140°C and reactivated when the temperature falls below 110°C.

DRIVER CONTROL BLOCK and INVERTER

The Driver Control block contains the logic, shoot-through protection, and gate drivers for the on-chip power FETs. The FETs are configured as a very large inverter that switches the SW pin between the voltage at IN and ground at a rate set by the MCU.

© 2019 Renesas Electronics Corporation

DEMODULATOR

Power is transferred from the transmitter to the receiver through their respective coils: a loosely-coupled transformer. How much power is transferred is determined by the transmitter's switching frequency (110kHz-205kHz), and is controlled by the receiver through instructions sent back through the coils to the transmitter to change its frequency, end power transfer, or do something else. The instructions take the form of data packets, which are capacitively coupled into the P9030's Demodulator through the HPF pin. Recovering the data packets is the function of the Demodulator. Understanding the packets is up to the MCU.

OUTPUT VOLTAGE SENSE

The voltage at the junction of the external inductor and capacitor that comprise the resonant tank is monitored by the VOSNS block, digitized by the ADC, and fed to the digital control logic. The control algorithm also requires knowledge of the voltage across the inverter, so that voltage is also processed by the ADC and sent to the digital block.

MICRO-CONTROLLER UNIT (MCU)

The P9030's MCU processes the algorithm, commands, and data that control the power transferred to the reciever. The MCU is provided with RAM and ROM, and parametric trim and operational modes are set at the factory through the One-Time Programming (OTP) block, read by the MCU at power-up. Communication with external memory is performed through I^2C via the SCL and SDA pins.

APPLICATIONS INFORMATION

The recommended applications schematic diagram is shown in Figure 13. The P9030 operates with a $19V_{DC}$ (±1V) input. The switching frequency varies from 110kHz to 205kHz. At the 205kHz limit the duty cycle is also variable. The power transfer is controlled via changes in switching frequency. The base or TX-side has a series resonance circuit made of a WPC Type-A1 coil (~24µH) and a series resonant capacitor (~100nF) circuit driven by a half-bridge inverter, as shown in Figure 8.

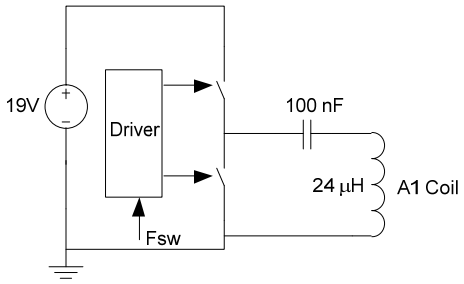


Figure 8. Half Bridge inverter TX Coil Driver.

Figure 8 shows the resonant tank configuration from the WPC specification. IDT has found that the circuit of Figure 9 is preferred for lower noise in the demodulation channel.

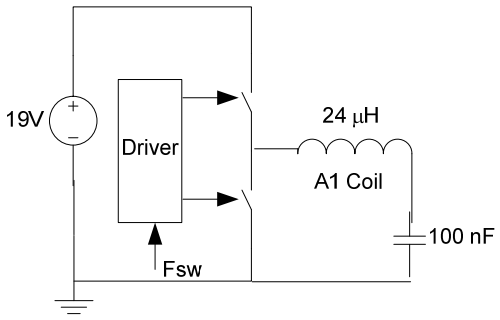


Figure 9. Half Bridge inverter TX Coil Driver.

EXTERNAL CHIP RESET and $\overline{EN}$

The P9030 can be externally reset by pulling the RESET pin to a logic high above the V_{IH} level.

The RESET pin is a dedicated high-impedance active-high digital input, and the effect is similar to the power-up reset function. Because of the internal low voltage monitoring scheme, the use of the external RESET pin is not mandatory. A manual external reset scheme can be added by connecting 5V to the RESET pin through a simple switch. When RESET is HIGH, the microcontroller's registers are set to the default configuration. When the RESET pin is released to a LOW, the microcontroller starts executing the code from the boot address. If the application is in a noisy environment, an external RC filter is recommended (see Figure 10 for reference)

© 2019 Renesas Electronics Corporation

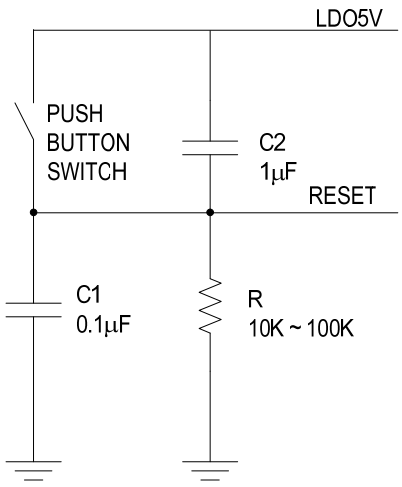


Figure 10. External Pushbutton Reset Circuit.

When the $\overline{EN}$ pin is pulled high, the device is suspended and placed in low current (sleep) mode. If pulled low, the device is active.

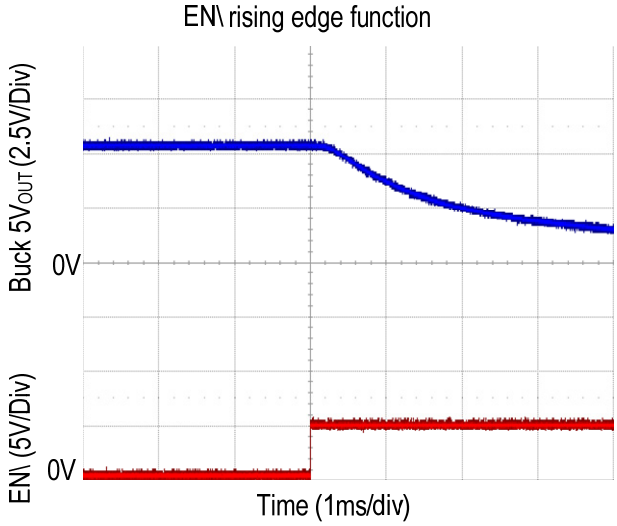


Figure 11. /EN Function.

The current into $\overline{EN}$ is about

$$I(EN) = \frac{V(EN-2V)}{300k},$$

or close to zero if V($\overline{EN}$) is less than 2V.

XTAL_CLK/IN and XTAL_CLK/OUT

A 32.768kHz crystal connected between the XTAL/CLK_IN and XTAL/CLK_OUT pins establishes a precise time base. Either that clock or the output of an on-chip RC oscillator is provided to the input of a PLL to generate the system clock. IDT recommends using the internal oscillator.

SYSTEM FEEDBACK CONTROL (WPC)

The P9030 contains logic to demodulate and decode error packets sent by the mobile device (Rx-side), and adjusts power transfer accordingly. The P9030 varies the switching frequency of the half bridge inverter between 110kHz to 205 kHz. to adjust power transfer. The mobile device controls the amount of power transferred via a communication link that exists from the mobile device to the base station. The mobile device (IDTP9020 or another WPC-compliant receiver) communicates with the P9030 via communication packets. Each packet has the following format:

Table 6 – Data Packet Format.

Preamble	Header	Message	Checksum

The overall system behavior between the transmitter and receiver follows the state machine diagram below:

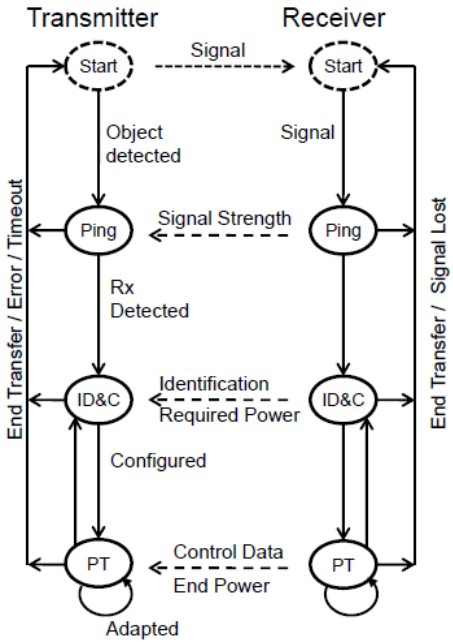


Figure 12. System state machine diagram

The P9030 performs four phases: Selection, Ping, Identification & Configuration, and Power Transfer.

START (SELECTION) PHASE

© 2019 Renesas Electronics Corporation

In this phase, the P9030 operates in a low power mode to determine if a potential receiver has been placed on the coil surface prior to the PING state. Twice a second, the P9030 applies a brief ac signal to its coil and listens for a response.

PING PHASE

In this phase, the P9030 applies a power signal at 175 kHz with a fixed 50% duty cycle and attempts to establish a communication link with a mobile device.

Required packet(s) in PING:

1. Signal strength packet (0x01)

The mobile device must send a Signal Strength Packet within a time period specified by the WPC, otherwise the power signal is terminated and the process repeats.

The mobile device calculates the Signal Strength Packet value, which is an unsigned integer value between 0-255, based on this formula:

$$Signal\ Strength\ Value = \left(\frac{U}{U_{max}}\right).256$$

where U is a monitored variable (i.e. rectified voltage/current/power) and U_{max} is a maximum value of that monitored variable expected during the digital ping phase at 175 kHz.

If the P9030 does not detect the start bit of the header byte of the Signal Strength Packet during the Ping Phase, it removes the power signal after a delay. If a signal strength packet is received, the P9030 goes to the Identification and Configuration Phase. If the P9030 does not move to the Identification and Configuration Phase after receiving the signal strength packet, or if a packet other than a signal strength packet is received, then power is terminated.

IDENTIFICATION AND CONFIGURATION (ID & Config)

In this phase, the P9030 tries to identify the mobile device and collects configuration information.

Required packet(s) in ID & Config:

1. Identification packet (0x71)
2. Extended Identification packet (0x81)*
3. Configuration packet (0x51)

* *If Ext bit of 0x71 packet is set to 1.*

Also, the P9030 must correctly receive the following sequence of packets without changing the operating point (175 kHz @ 50% duty cycle):

1. Identification Packet (0x71)
2. Extented Identification (0x81)
3. Up to 7 optional configuration Packets from the following set:
    a. Power Control Hold-Off Packet (0x06)
    b. Proprietary Packet (0x18 – 0xF2)
    c. Reserved Packet
4. Configuration Packet (0x51)

If the P9030 does not detect the start bit of the header byte of the next Packet in the sequence within a WPC-specified time after receiving the stop bit of the checksum byte of the preceding Signal Strength Packet, then the Power Signal is removed within after a delay. If a correct control packet in the above sequence is received late, or if control packets that are not in the sequence are received, the P9030 removes the Power Signal after a delay.

POWER TRANSFER PHASE

In this phase, the P9030 adapts the power transfer to the receiver based on control data it receives in control error packets.

Required packet(s) in Power Transfer:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)

For this purpose, the P9030 may receive zero or more of the following Packets:

1. Control Error Packet (0x03)
2. Rectified Power Packet (0x04)
3. Charge Status Packet (0x05)
4. End Power Transfer Packet (0x02)
5. Any Proprietary Packet
6. Any reserved Packets

If the P9030 does not correctly receive the first Control Error Packet in time, it removes the Power Signal after a delay. Because Control Error Packets come at a regular interval, the P9030 expects a new Control Error Packet after receiving the stop bit of the checksum byte of the preceding Control Error Packet. If that does not happen,

© 2019 Renesas Electronics Corporation

then the P9030 removes the Power Signal. Similary, the P9030 must receive a Rectified Power Packet within a WPC-specified time after receiving the stop bit of the checksum byte of the Configuration Packet (which was received earlier in the *identification and configuration* phase). Otherwise, it removes the Power Signal.

Upon receiving a Control Error value, the P9030 makes adjustments to its operating point after a delay to enable the Primary Coil current to stabilize again after communication.

If the P9030 correctly receives a Packet that does not comply with the sequence, then it removes the Power Signal.

FOREIGN OBJECT DETECTION (FOD)

In addition to over-temperature protection, the P9030 employs a proprietary FOD technique for safety which detects foreign objects placed on the base station. The FOD algorithm is multi-layered and issues warnings depending on the severity of the warning.

The FOD warning comes on during the *PING* phase indicating the presence of a smaller object and larger object respectively. The FOD warning is asserted during the *Power Transfer* phase, indicating presence of a foreign object. With this warning ON, the P9030 stops power transfer, goes back to the *PING* phase, and stays there until the surface is cleared and the process starts over again.

© 2019 Renesas Electronics Corporation

APPLICATIONS INFORMATION

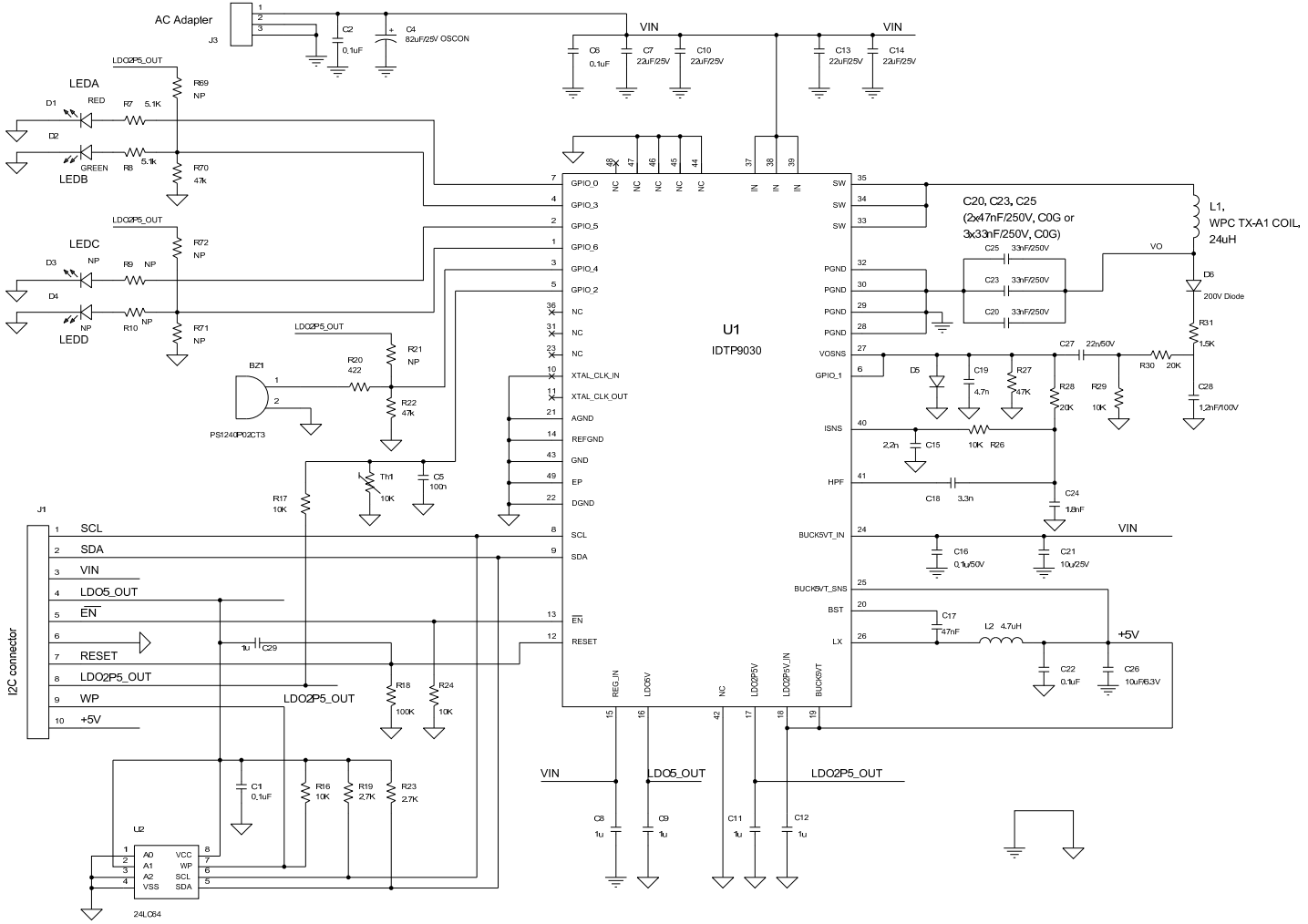


Figure 13. P9030 WPC "Qi" Compliance Schematic (See P9030 Evaluation Kit User Manual for complete details)

© 2019 Renesas Electronics Corporation

Table 7. P9030 WPC "Qi" Compliance Bill of Materials

Item #	Qty	Ref Design	Description	Manufacturer	Part #	PCB Footprint
1	3	C2,C16,C22	CAP CER 0.1UF 50V 10% X7R	TDK	C2012X7R1H104K/0.85	805
2	3	C20,C23,C25 Option 1	CAP CER 0.033UF 250V 5% NP0/C0G[1]	TDK	C4532C0G2E333JT	1812
	2	C20,C23 Option 2	CAP CER 0.047UF 250V 5% NP0/C0G[1]	TDK	C4532C0G2E473JT	1812
3	5	C8,C9,C11,C12,C29	CAP CER 1UF 25V 10% X7R	Taiyo Yuden	TMK107B7105KA-T	0603
4	4	C7, C10, C13, C14	CAP CER 22UF 25V 10% X7R	Taiyo Yuden	TMK325B7226MM-TR	1210
5	1	C4	OSCON 82UF 25V 20% 105DEGC	Panasonic	25SVPF82M	E7
5	1	C17	CAP CER 0.047UF 16V 10% X7R	Murata	GRM188R71C473KA01D	0603
6	1	C21	CAP CER 10UF 25V 10% X5R	TDK	C2012X5R1E106K	0805
7	1	C15	CAP CER 2200PF 16V 10% X7R	AVX	0603YC222KAT2A	603
8	1	C6	CAP CER 0.1UF 50V 10% X7R	Murata	GRM188R71H104KA93D	0603
9	1	C26	CAP CER 10UF 6.3V 10% X7R	Taiyo Yuden	JMK212B7106KG-T	805
10	1	C18	CAP CER 3300PF 50V 5% NP0/C0G[1]	Murata	GCM1885C1H332JA16D	0603
11	1	C24	CAP CER 1800PF 50V 5% NP0/C0G[1]	Murata	GRM1885C1H182JA01D	0603
12	1	C27	CAP CER 0.022UF 100V X7R 10%	TDK	C1608X7R2A223K	0603
12	1	C28	CAP CER 1200PF 100V 5% NP0/C0G[1]	TDK	C1608C0G2A122J	0603
13	1	C19	CAP CER 4700PF 50V 5% NP0/C0G[1]	TDK	CGJ3E2C0G1H472J	0603
14	1	D6	DIODE SWITCH 200V 250MW	Diodes Inc	BAV21W-7-F	SOD123
15	1	D5	DIODE SWITCH 75V 300mA	Micro Comm Co	1N4148W-TP	SOD123
16	1	L2	4.7uH 20% 580mA	Coilcraft	XPL2010-472ML	2ML
17	1	L1	24uH Transmitter Coil WPC TX-A1	E&E	Y31-60014F	53mmx53mm
				TDK	TTx-52-T2V	
				Toko	X1387	
18	1	R18	RES 100K OHM 1/16W 1%	Yageo	RC0402FR-07100KL	402
19	2	R28,R30	RES 20.0K OHM 1/10W 1%	Panasonic	ERJ-3EKF2002V	0603
20	1	R31	RES 1.50K OHM 1/10W 1%	Panasonic	ERJ-3EKF1501V	0603
20	1	R24	RES 10.0K OHM 1/16W 1%	Yageo	RC0402FR-0710KL	402
21	1	R29	RES 10.0K OHM 1/10W 1% 0603 SMD	Panasonic	ERJ-3EKF1002V	603
22	1	R27	RES 47K OHM 1/10W 5%	Panasonic	ERJ-2GEJ473X	402
23	1	U1	IC EEPROM 64KBIT 400KHZ	Microchip	24AA64T-I/MNY	8TDFN
24	1	U2	IC Wireless Power Transmitter	IDT	P9030	6x6x0.8-48TQFN
WPC "Qi" Compliance Components						
1	1	D1	LED SMARTLED 630NM RED	OSRAM	L29K-G1J2-1-0-2-R18-Z	0603_LED
2	1	D2	LED SMARTLED GREEN 570NM	OSRAM	LG L29K-G2J1-24-Z	0603_LED
19	2	R7, R8	RES 4.9K OHM 1/10W 5%	Panasonic	ERJ-2RKF4991X	402
20	3	R16,R17,R24	RES 10.0K OHM 1/16W 1%	Yageo	RC0402FR-0710KL	402
21	1	R20	RES 422 OHM 1/10W 1%	Panasonic	ERJ-2RKF4220X	402
22	2	R19,R23	RES 2.7K OHM 1/10W 5%	Panasonic	ERJ-2GEJ272X	402
23	2	C1,C5	CAP CER 0.1UF 50V 10% X7R	Murata	GRM188R71H104KA93D	0603
24	1	TH1	THERMISTOR NTC 10K OHM 1% RAD	TDK	B57551G0103F000	Through-hole
25	1	BZ1	BUZZER PIEZO 4KHZ PC MNT	TDK	PS1240P02CT3	12.2mmx3.5mm

Note 1: Recommended capacitor temperature/dielectric and voltage ratings: 250V capacitors are recommended because 200Vp-p voltage levels may appear on the resonance capacitors as stated in the WPC specification. C0G/NPO-type capacitor values stay relatively constant with voltage while X7R and X5R ceramic capacitor values de-rate from 40% to over 80%. The decision to use lower voltage 100V capacitors or other type temperature/dielectric capacitors is left to the end user.

External Components

The P9030 requires a minimum number of external components for proper operation (see the BOM in Table 7). A complete design schematic compliant to the WPC "Qi" standard is given in Figure 19. It includes WPC "Qi" LED signaling, buzzer, thermistor circuit, and EEPROM for loading P9030 firmware.

I²C Communication

The P9030 includes an I²C block which can support either I²C Master or I²C Slave operation. After power-on-reset (POR), the P9030 will initially become I²C Master for the purpose of uploading firmware from an external memory device, such as an EEPROM. The I²C Master mode on the P9030 does not support multi-master mode, and it is important for system designers to avoid any bus master conflict until the P9030 has finished any firmware uploading and has released control of the bus as I²C Master. After any firmware uploading from external memory is complete, and when the P9030 begins normal operation, the P9030 is normally configured by the firmware to be exclusively in I²C Slave mode.

© 2019 Renesas Electronics Corporation

For maximum flexibility, the P9030 tries to communicate with the first address on the EEPROM at 100kHz. If no ACK is received, communication is attempted at the other addresses at 300kHz.

EEPROM

The P9030 uses an external EEPROM which contains either standard or custom TX firmware. The external EEPROM memory chip is pre-programmed with a standard start-up program that is automatically loaded when 19V power is applied. The P9030 uses I²C slave address 0x52 to access the EEPROM. The P9030 slave address is 0x39. The EEPROM can be reprogrammed to suit the needs of a specific application using the P9030 software tool (see the P9030-Qi Demo Board User Manual for complete details). The IC will look initially for an external EEPROM and use the firmware built into the IC ROM only if no custom firmware is found. A serial 8Kbyte (8Kx8 64Kbits) external EEPROM is sufficient.

If the standard default/built-in firmware is not suitable for the application, custom ROM options are possible. Please contact IDT sales for more information. IDT will provide the appropriate image in the format best suited to the application.

Overview of Standard GPIO Usage

There are 7 GPIO's on the P9030 transmitter IC, of which five are available for use as follows:

- GPIO0: Red LED_A to indicate standby, fault conditions, and FOD warnings; see table 8.
- GPIO2: Temperature sensor input. Contact IDT for a spreadsheet facilitating selection and use of thermistors.
- GPIO3: Green LED_B to indicate standby, power transfer, and power complete. Table 8 lists how the red and green LEDs can be used to display information about the P9030's operating modes. The table also includes information about external resistors or internal pull up/down options to select LED modes. Eight of the ten LED modes (those associated with advanced charging modes) are currently designated as "Future" modes.
- GPIO4: AC or DC buzzer (optional) with resistor options for different buzzer configurations.
- GPIO5 LEDC and GPIO6 LEDD are for future development, and are currently not defined.

LED FUNCTIONS

Two GPIOs are used to drive LEDs which indicate, through various on/off and illumination options, the state of charging and some possible fault conditions.

A red LED indicates various Fault and FOD ("Foreign Object Detection") states. The green LED indicates Power Transfer and Charge Complete state information. Upon power up, the two LEDs together may optionally indicate the Standby State and remain in this state until another of the defined Operational States occurs

As shown in Figure 16, one or two resistors configure the defined LED option combinations. The DC voltage set in this way is read one time during power-on to determine the LED configuration. To avoid interfering with the LED operation, the useful DC voltage range must be limited to not greater than 1Vdc.

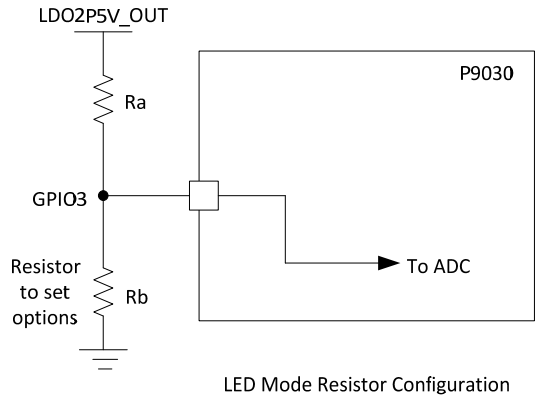


Figure 14. P9030 LED Resistor Options.

LED Pattern Operational Status Definitions:

Blink Slow: 1s ON, 1s OFF, repeat.

Blink Fast: 400ms ON, 800ms OFF, 400ms ON, 800ms OFF, repeat.

The red FOD warning LED is synchronized with the buzzer (if implemented) such that a 400ms tone corresponds with the FOD red LED illumination and 800ms of silence corresponds with the LED being off. During the 30s that the buzzer is off, the FOD LED must continue to blink.

© 2019 Renesas Electronics Corporation

Table 8 – P9030 LED Resistor Optioning (Not all options supported, shaded rows are for future development).

LED Control Option	LED Select Resistor Value	Description	LED #/ Color	Operational Status				FOD Warning
				Standby	Transfer	Complete	Condition	
1	Pull Down	Standby LEDs ON	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
2	R1	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
3	R2	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
4	R3	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
5	R4	Standby LEDs ON plus	LED1- Green	ON	BLINK SLOW	ON	OFF	OFF
			LED2- Red	ON	OFF	OFF	ON	BLINK FAST
6	Pull Up	Standby LEDs OFF	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
7	R5	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
8	R6	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
9	R7	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST
10	R8	Standby LEDs OFF plus	LED1- Green	OFF	BLINK SLOW	ON	OFF	OFF
			LED2- Red	OFF	OFF	OFF	ON	BLINK FAST

R1-R8 are created using combination of two 1% resistors.

Designates Future Option

Buzzer Function

An optional buzzer feature is supported on GPIO4. The default configuration is an "AC" buzzer. The signal is created by toggling GPIO4 active-high/active-low at a 2KHz frequency.

Buzzer Action: Power Transfer Indication

The P9030 supports audible notification when the device operation successfully reaches the Power Transfer state. The duration of the power transfer indication sound is 400ms.

The latency between reaching the Power Transfer state and sounding the buzzer does not exceed 500ms. Additionally, the buzzer sound is concurrent within ±250ms of any change to the LED configuration indicating the start of power transfer.

Buzzer Action: No Power Transfer due to Foreign Object Detected (FOD)

When a major FOD situation is detected such that, for safety reasons, power transfer is not initiated, or that power transfer is terminated, the buzzer is sounded in a repeating sequence:

For 30 seconds: 400ms ON, 800ms OFF, repeat
Next 30 seconds: Off/silence (but no change to LED on/off patterns)
The pattern is repeated while the error condition exists

The buzzer is synchronized with the FOD LED such that the 400ms on tone corresponds with the Red LED illumination and 800ms off (no sound) corresponds with Red LED being off.

Decoupling/Bulk Capacitors

As with any high-performance mixed-signal IC, the P9030 must be isolated from the system power supply noise to perform optimally. A decoupling capacitor of 0.1µF must be connected between each power supply and the PCB ground plane as close to these pins as possible. For optimum device performance, the decoupling capacitor must be mounted on the component side of the PCB. Avoid the use of vias in the decoupling circuit. Additionally, medium value capacitors in the 22µF range must be used at the VIN input to minimize ripple current and voltage droop due to the large current requirements of the resonant half Half-Bridge driver. At least four 22µF capacitors must be used close to the IN pins of the device.

© 2019 Renesas Electronics Corporation

Since the operating voltage is 18V to 20V, the value of the capacitors will decrease due to voltage derating characteristics. For example, a 22µF X7R 25V capacitor's value is actually 6µF when operating at 20V.

There must also be an 82µF to 100µF bulk capacitor connected at the node where the input voltage to the board is applied. A 25V Oscon-type or aluminum electrolytic must be connected between the input supply and ground as shown in Figure 20. Oscon capacitors have much lower ESR than aluminum electrolytic capacitors and will reduce voltage ripple.

ADC Considerations

The GPIO pins are connected internally to a successive approximation ADC with a multiplexed input. The GPIO pins that are connected to the ADC have limited input range, so attention must be paid to the maximum VIN (2.5V). 0.01µF decoupling capacitors can be added to the GPIO inputs to minimize noise.

WPC TX-A1 Coil

The SW pin connects to a series-resonance circuit comprising a WPC Type-A1 coil (~24µH) and a series resonant capacitor (~100nF), as shown in Figures 8 and 9. The inductor serves as the primary coil in a loosely-coupled transformer, the secondary of which is the inductor connected to the power receiver (IDTP9020 or another receiver).

The TX-A1 power transmitter coil is mounted on a ferrite shield to reduce EMI. The coil assembly can be mounted next to the P9030. Either ground plane or grounded copper shielding can be added beneath the ferrite shield for added reduction in radiated electrical field emissions. The coil ground plane/shield must be connected to the P9030 ground plane by a single trace.

Resonance Capacitors

The resonance capacitors must be C0G type dielectric and have a DC rating to 250V. The highest-efficiency combination is three 33nF in parallel to get the lowest ESR. Using a single 100nF or two 47nF capacitors is also an option. The part numbers are shown in Table 7.

Buck Converter

The input capacitors (C_{IN}) must be connected directly between the power V_{IN} and power PGND pins. The output capacitor (C_{OUT}) and power ground must be connected together to minimize any DC regulation errors caused by ground potential differences.

The bootstrap pin requires a small capacitor; connect a 47nF bootstrap capacitor rated above 25V between the BST pin and the LX pin.

The output-sense connection to the feedback pins must be separated from any power trace. Connect the output-sense trace as close as possible to the load point to avoid additional load regulation errors. Sensing through a high-current load trace will degrade DC load regulation.

The power traces, including PGND traces, the SW or OUT traces and the VIN trace must be kept short, direct and wide to allow large current flow. The inductor connection to the SW or OUT pins must be as short as possible. Use several via pads when routing between layers.

LDOs

Input Capacitor

The input capacitors must be located as physically close as possible to the power pin (LDO2P5V_IN) and power ground (GND). Ceramic capacitors are recommended for their higher current operation and small profile. Also, ceramic capacitors are inherently more capable than are tantalum capacitors to withstand input current surges from low impedance sources such as batteries used in portable devices. Typically, 10V- or 16V-rated capacitors are required. The recommended external components are shown in Table 7.

Output Capacitor

For proper load voltage regulation and operational stability, a capacitor is required on the output of each LDO (LDO2P5V and LDO5V). The output capacitor must be placed as close to the device and power (PGND) pins as possible. Since the LDOs have been designed to function with very low ESR capacitors, a ceramic capacitor is recommended for best performance.

PCB Layout Considerations

- For optimum device performance and lowest output phase noise, the following guidelines must be observed. Please contact IDT for Gerber files that contain the recommended board layout.
- As for all switching power supplies, especially those providing high current and using high switching frequencies, layout is an important design step. If layout is not carefully done, the regulator could show

© 2019 Renesas Electronics Corporation

instability as well as EMI problems. Therefore, use wide and short traces for high current paths.

- The 0.1µF decoupling capacitors must be mounted on the component side of the board as close to the VDD pin as possible. Do not use vias between decoupling capacitors and VDD pins. Keep PCB traces to each VDD pin and to ground vias as short as possible.
- To optimize board layout, place all components on the same side of the board and limit the use of vias. Route other signal traces away from the P9030. For example, use keepouts for signal traces routing on inner and bottom layers underneath the device.
- The NQG48 6.0 mm x 6x0 mm x 75mm 48L package has an inner thermal pad which requires blind assembly. It is recommended that a more active flux solder paste be used such as Alpha OM-350 solder paste from Cookson Electronics (http://www.cooksonsemi.com). Please contact IDT for Gerber files that contain recommended solder stencil design.
- The package center exposed pad (EP) must be reliably soldered directly to the PCB. The center land pad on the PCB (set 1:1 with EP) must also be tied to the board ground plane, primarily to maximize thermal performance in the application. The ground connection is best achieved using a matrix of PTH vias embedded in the PCB center land pad for the NTG48. The PTH vias perform as thermal conduits to the ground plane (thermally, a heat spreader) as well as to the solder side of the board. There, these thermal vias embed in a copper fill having the same dimensions as the center land pad on the component side. Recommendations for the via finished hole-size and array pitch are 0.3mm to 0.33mm and 1.3mm, respectively.
- Layout and PCB design have a significant influence on the power dissipation capabilities of power management ICs. This is due to the fact that the surface mount packages used with these devices rely heavily on thermally conductive traces or pads to transfer heat away from the package. Appropriate PC layout techniques must then be used to remove the heat due to device power dissipation. The following general guidelines will be helpful in designing a board layout for lowest thermal resistance:
    1. PC board traces with large cross sectional areas remove more heat. For optimum results, use large area PCB patterns with wide and heavy (2 oz.) copper traces, placed on the top layer of the PCB.
    2. In cases where maximum heat dissipation is required, use double-sided copper planes connected with multiple vias.
    3. Thermal vias are needed to provide a thermal path to the inner and/or bottom layers of the PCB to remove the heat generated by device power dissipation.
    4. Where possible, increase the thermally conducting surface area(s) openly exposed to moving air, so that heat can be removed by convection (or forced air flow, if available).
    5. Do not use solder mask or place silkscreen on the heat-dissipating traces/pads, as they increase the net thermal resistance of the mounted IC package.

Power Dissipation/Thermal Requirements

The P9030 is offered in a TQFN-48L package. The maximum power dissipation capability is 2W, limited by the die's specified maximum operating junction temperature, Tj, of 125°C. The junction temperature rises with the device power dissipation based on the package thermal resistance. The package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 31°C/W when the PCB layout and surrounding devices are optimized as described in the PCB Layout Considerations section. The techniques as noted in the PCB Layout section need to be followed when designing the printed circuit board layout, as well as the placement of the P9030 IC package in proximity to other heat generating devices in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attach thermal pad size, and internal package construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB itself upon which the TQFN is mounted. For example, in a still air environment, as is often the case, a significant amount of the heat that is generated (60 - 85%) sinks into the PCB. Changing the design or configuration of the PCB changes impacts the overall thermal resistivity and, thus, the board's heat sinking efficiency.

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-

© 2019 Renesas Electronics Corporation

dependant issues such as thermal coupling, airflow, added heat sinks, and convection surfaces, and the presence of other heat-generating components, affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below:

1. Improving the power dissipation capability of the PCB design
2. Improving the thermal coupling of the component to the PCB
3. Introducing airflow into the system

First, the maximum power dissipation for a given situation must be calculated:

$P_{D(MAX)} = (T_{J(MAX)} - T_A)/\theta_{JA}$

Where:

$P_{D(MAX)}$ = Maximum Power Dissipation (W)

θ_{JA} = Package Thermal Resistance (°C/W)

$T_{J(MAX)}$ = Maximum Device Junction Temperature (°C)

T_A = Ambient Temperature (°C)

The maximum recommended junction temperature ($T_{J(MAX)}$) for the P9030 device is 150°C. The thermal resistance of the 48-pin NQG package (NGQ48) is optimally θ_{JA}=30°C/W. Operation is specified to a maximum steady-state ambient temperature (T_A) of 85°C. Therefore, the maximum recommended power dissipation is:

$$P_{D(Max)} = (150°C - 85°C) / 30°C/W \cong 2 \text{ Watt}$$

Thermal Overload Protection

The P9030 integrates thermal overload shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the device if the die temperature exceeds 140°C. To allow the maximum load current on each regulator and resonant transmitter, and to prevent thermal overload, it is important to ensure that the heat generated by the P9030 is dissipated into the PCB. The package exposed paddle must be soldered to the PCB, with multiple vias evenly distributed under the exposed paddle and exiting the bottom side of the PCB. This improves heat flow away from the package and minimizes package thermal gradients.

Special Notes

NQG TQFN-48 Package Assembly

Note 1: Unopened Dry Packaged Parts have a one year shelf life.

Note 2: The HIC indicator card for newly opened Dry Packaged Parts should be checked. If there is any moisture content, the parts must be baked for minimum of 8 hours at 125˚C within 24 hours of the assembly reflow process.

© 2019 Renesas Electronics Corporation

PACKAGE OUTLINE DRAWING

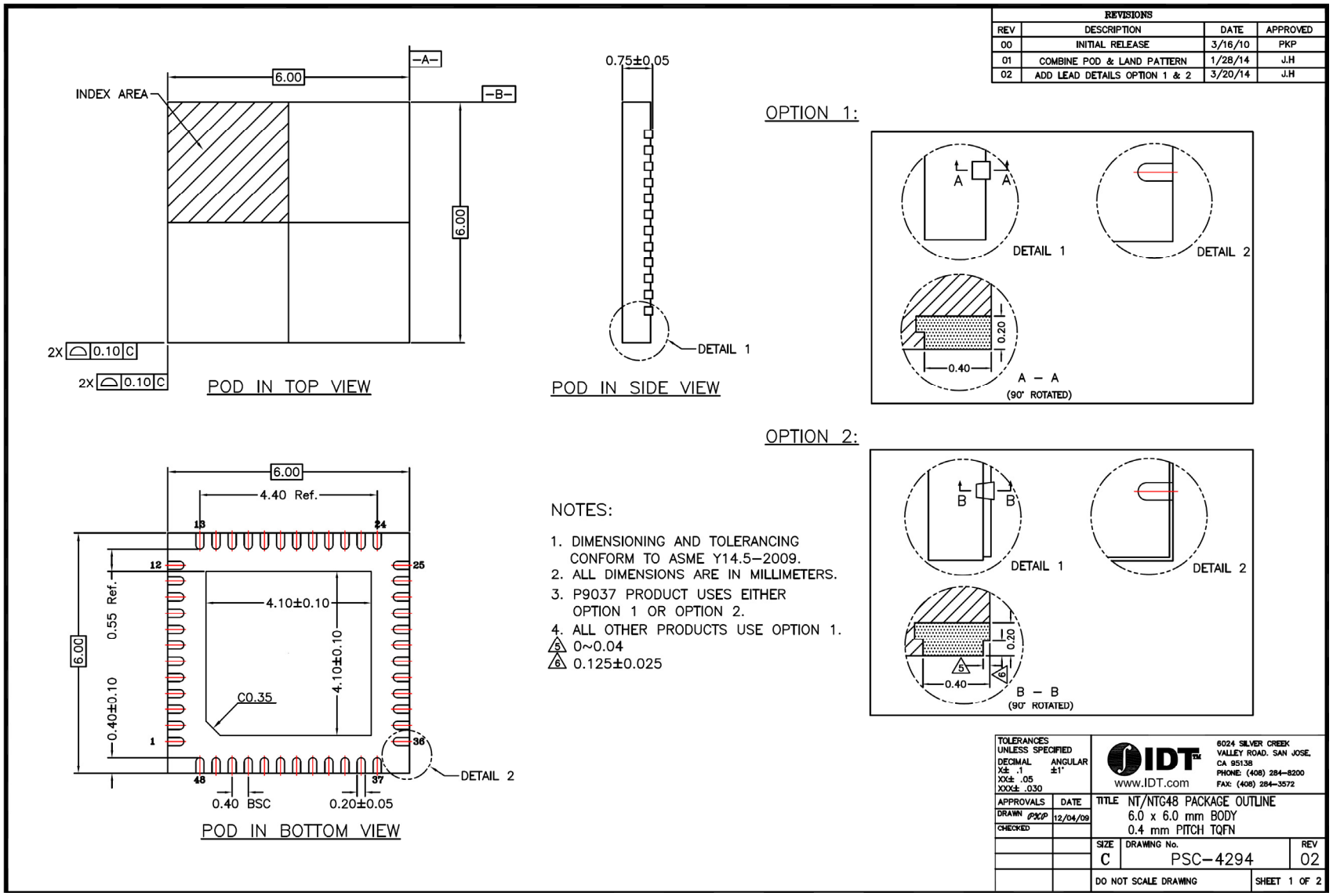


Figure 15. P9030 Package Outline Drawing (NTG48 TQFN-48L 6.0 mm x 6.0 mm x 0.75 mm48L, 0.4mm pitch)

© 2019 Renesas Electronics Corporation

LANDING PATTERN DRAWING

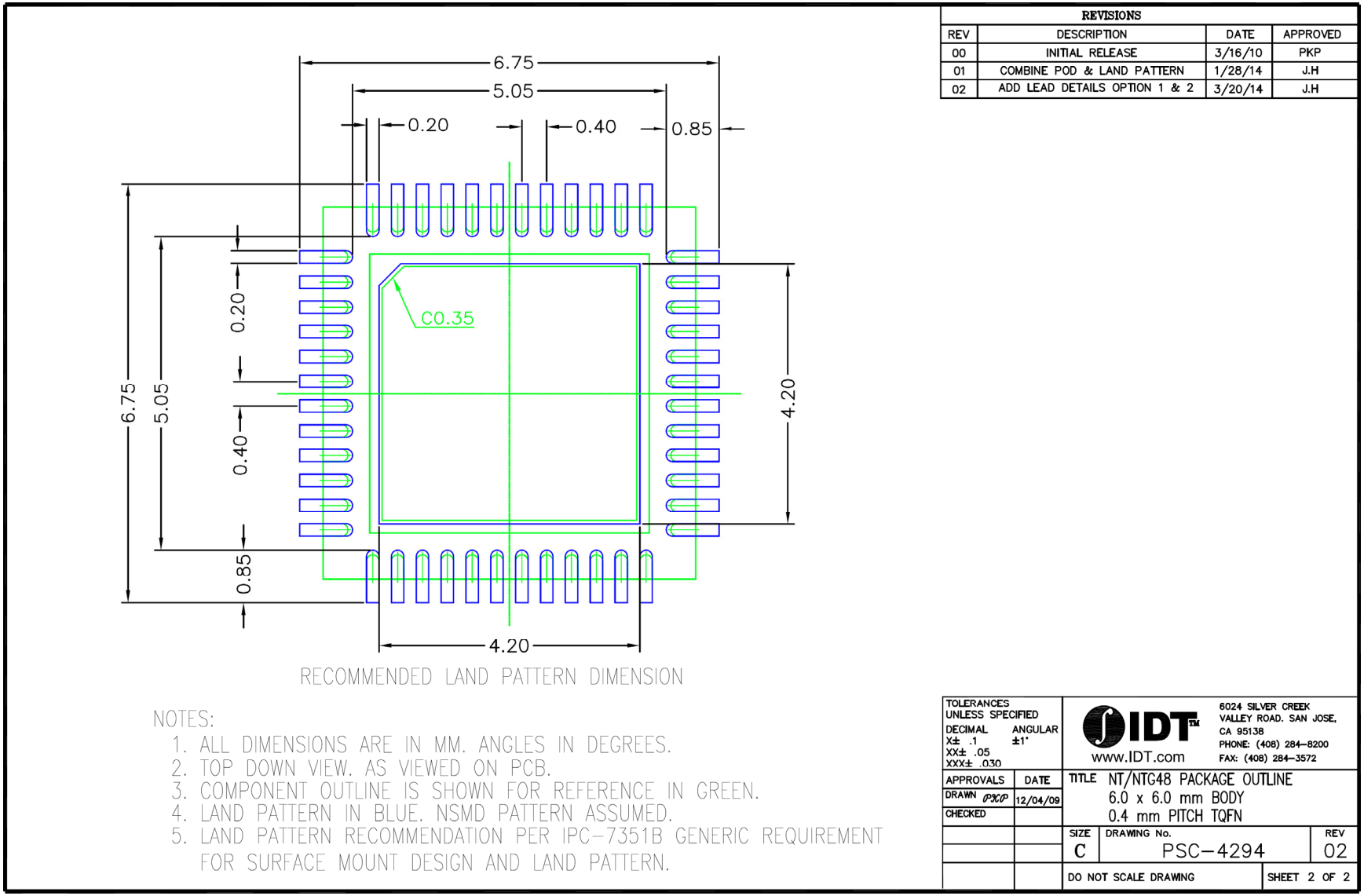


Figure 16. P9030 NTG48 TQFN landing pattern drawing.

© 2019 Renesas Electronics Corporation

ORDERING GUIDE

Table 9. Ordering Summary

PART NUMBER	MARKING	PACKAGE	AMBIENT TEMP. RANGE	SHIPPING CARRIER	QUANTITY
P9030-0NTGI	P9030NTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tray	25
P9030-0NTGI8	P9030NTG	NTG48 - TQFN-48 6x6x0.75mm	-40°C to +85°C	Tape and Reel	2,500

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2025 Renesas Electronics Corporation. All rights reserved.