R1QHA7236ABB
R1QHA7218ABB

72-Mbit DDRII+ SRAM
2-word Burst

R10DS0173EJ0203
Rev. 2.03
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Description

The R1Q#A7236 is a 2,097,152-word by 36-bit and the R1Q#A7218 is a 4,194,304-word by 18-bit synchronous double data rate static RAM fabricated with advanced CMOS technology using full CMOS six-transistor memory cell. It integrates unique synchronous peripheral circuitry and a burst counter. All input registers are controlled by an input clock pair (K and /K) and are latched on the positive edge of K and /K. These products are suitable for applications which require synchronous operation, high speed, low voltage, high density and wide bit configuration. These products are packaged in 165-pin plastic FBGA package.

= H: Latency =2.5, w/o ODT

Features

Power Supply

- 1.8 V for core (V_{DD}), 1.4 V to V_{DD} for I/O (V_{DDQ})

Clock

- Fast clock cycle time for high bandwidth
- Two input clocks (K and /K) for precise DDR timing at clock rising edges only
- Two output echo clocks (CQ and /CQ) simplify data capture in high-speed systems
- Clock-stop capability with µs restart

I/O

- Common data input/output bus
- Pipelined double data rate operation
- HSTL I/O
- User programmable output impedance
- DLL/PLL circuitry for wide output data valid window and future frequency scaling
- Data valid pin (QVLD) to indicate valid data on the output

Function

- Two-tick burst for low DDR transaction size
- Internally self-timed write control
- Simple control logic for easy depth expansion
- JTAG 1149.1 compatible test access port

Package

- 165 FBGA package (13 x 15 x 1.4 mm)
- RoHS Compliance Level = 6/6

Part Number Definition

Column No.	0	1	2	3	4	5	6	7	8	9	10	11	-	12	13	14	15	16
Example	R	1	Q	H	A	7	2	1	8	A	B	B	-	2	5	I	B	1
	The above part number is just example for 72M QDRII+ B4 x18 400MHz, 13x15mm PKG, Pb-free part.																	

No.	-	Comments	No.	-	Comments
0-1	R1	Renesas Memory Prefix	9	A	2nd Generation
2-3	Q2	QDR II B2[*1] (L15)[*2]	10-11	BB	PKG = BGA 13x15 mm
	Q3	QDR II B4 (L15)	12-13	40	Frequency = 250MHz
	Q4	DDR II B2 (L15)		33	Frequency = 300MHz
	QA	QDR II+ B4 L25		25	Frequency = 400MHz
	QB	DDR II+ B2 L25		20	Frequency = 500MHz
	QD	QDR II+ B4 L25 w/ ODT[*3]		19	Frequency = 533MHz
	QE	DDR II+ B2 L25 w/ ODT	14	I	Industrial temp. T_a range = -40°C to 85°C
	QG	QDR II+ B2 L20			
	QH	DDR II+ B2 L20	15	B	Pb-free and Tray
4	A	V_{DD} = 1.8 V	16	0 to 9, A to Z or None	Renesas internal use
5-6	72	Density = 72Mb			
7-8	09	Data width = 9bit			
	18	Data width = 18bit			
	36	Data width = 36bit			

Notes[*] 1. B=Burst length (B2: Burst length=2, B4: Burst length=4)

2. L=Read Latency (L15: Read Latency = 1.5 cycle, L20: 2.0 cycle, L25: 2.5 cycle)

3. ODT=On Die Termination

72M QDR/DDR SRAM (R1Q*A72 Series) Lineup

Renesas supports or plans to support the parts listed below.

No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation	Frequency (max) (MHz)	533	500	400	300	250
						Cycle Time (min) (ns)	1.875	2.00	2.50	3.30	4.00
1	QDRII	B2	1.5	No	x 9	R1Q2A7209ABB-yy					-40
2					x18	R1Q2A7218ABB-yy					
3					x36	R1Q2A7236ABB-yy					
4		B4			x18	R1Q3A7218ABB-yy				-33	
5					x36	R1Q3A7236ABB-yy					
6	DDRII	B2			x18	R1Q4A7218ABB-yy				-33	
7					x36	R1Q4A7236ABB-yy					
8	QDRII+	B4	2.5	No	x18	R1QAA7218ABB-yy	-19	-20			
9					x36	R1QAA7236ABB-yy					
10	DDRII+	B2			x18	R1QBA7218ABB-yy	-19	-20			
11					x36	R1QBA7236ABB-yy					
12	QDRII+	B4		Yes	x18	R1QDA7218ABB-yy	-19	-20			
13					x36	R1QDA7236ABB-yy					
14	DDRII+	B2			x18	R1QEA7218ABB-yy	-19	-20			
15					x36	R1QEA7236ABB-yy					
16	QDRII+	B4	2.0	No	x18	R1QGA7218ABB-yy			-25		
17					x36	R1QGA7236ABB-yy					
18	DDRII+	B2			x18	R1QHA7218ABB-yy			-25		
19					x36	R1QHA7236ABB-yy					

Notes 1. "yy" represents the speed bin. "R1QDA7236ABB-20" can operate at 500 MHz(max) of frequency, for example.

2. The part which is not listed above is not supported, as of the day when this datasheet was issued, in spite of the existence of the part number or datasheet.

Pin Arrangement

R1QHA7236 series

(Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	NC	SA	R-/W	/BW2	/K	/BW1	/LD	SA	SA	CQ
B	NC	DQ27	DQ18	SA	/BW3	K	/BW0	SA	NC	NC	DQ8
C	NC	NC	DQ28	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ17	DQ7
D	NC	DQ29	DQ19	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	DQ16
E	NC	NC	DQ20	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	DQ15	DQ6
F	NC	DQ30	DQ21	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	DQ31	DQ22	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ14
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	DQ32	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ13	DQ4
K	NC	NC	DQ23	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ12	DQ3
L	NC	DQ33	DQ24	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	DQ34	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ11	DQ1
N	NC	DQ35	DQ25	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	DQ10
P	NC	NC	DQ26	SA	SA	QVLD	SA	SA	NC	DQ9	DQ0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Notes 1. Address expansion order for future higher density SRAMs: 10A → 2A → 7A → 5B.

2. NC pins can be left floating or connected to 0V ～ V_{DDQ}.

R1QHA7218 series

(Top View)

	1	2	3	4	5	6	7	8	9	10	11
A	/CQ	SA	SA	R-/W	/BW1	/K	NC	/LD	SA	SA	CQ
B	NC	DQ9	NC	SA	NC	K	/BW0	SA	NC	NC	DQ8
C	NC	NC	NC	V_{SS}	SA	NC	SA	V_{SS}	NC	DQ7	NC
D	NC	NC	DQ10	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	NC	NC
E	NC	NC	DQ11	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ6
F	NC	DQ12	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ5
G	NC	NC	DQ13	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	NC
H	/DOFF	V_{REF}	V_{DDQ}	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	V_{DDQ}	V_{REF}	ZQ
J	NC	NC	NC	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	DQ4	NC
K	NC	NC	DQ14	V_{DDQ}	V_{DD}	V_{SS}	V_{DD}	V_{DDQ}	NC	NC	DQ3
L	NC	DQ15	NC	V_{DDQ}	V_{SS}	V_{SS}	V_{SS}	V_{DDQ}	NC	NC	DQ2
M	NC	NC	NC	V_{SS}	V_{SS}	V_{SS}	V_{SS}	V_{SS}	NC	DQ1	NC
N	NC	NC	DQ16	V_{SS}	SA	SA	SA	V_{SS}	NC	NC	NC
P	NC	NC	DQ17	SA	SA	QVLD	SA	SA	NC	NC	DQ0
R	TDO	TCK	SA	SA	SA	NC	SA	SA	SA	TMS	TDI

Notes 1. Address expansion order for future higher density SRAMs: 10A → 2A → 7A → 5B.

2. NC pins can be left floating or connected to 0V ～ V_{DDQ}.

Pin Description

Name	I/O type	Descriptions	Notes
SA_x	Input	Synchronous address inputs: These inputs are registered and must meet the setup and hold times around the rising edge of K. All transactions operate on a burst-of-four words (two clock periods of bus activity). SA0 and SA1 are used as the lowest two address bits for burst READ and burst WRITE operations permitting a random burst start address on ×18 and ×36 of DDR II (not II+) devices. These inputs are ignored when device is deselected or once burst operation is in progress.	
/LD	Input	Synchronous load: This input is brought low when a bus cycle sequence is to be defined. This definition includes address and READ / WRITE direction. All transactions operate on a burst-of-four data (two clock periods of bus activity).	
R-/W	Input	Synchronous read / write Input: When /LD is low, this input designates the access type (READ when R-/W is high, WRITE when R-/W is low) for the loaded address. R-/W must meet the setup and hold times around the rising edge of K.	
/BWx	Input	Synchronous byte writes: When low, these inputs cause their respective byte to be registered and written during WRITE cycles. These signals are sampled on the same edge as the corresponding data and must meet setup and hold times around the rising edges of K and /K for each of the two rising edges comprising the WRITE cycle. See Byte Write Truth Table for signal to data relationship.	
K, /K	Input	Input clock: This input clock pair registers address and control inputs on the rising edge of K, and registers data on the rising edge of K and the rising edge of /K. /K is ideally 180 degrees out of phase with K. All synchronous inputs must meet setup and hold times around the clock rising edges. These balls cannot remain V_{REF} level.	
/DOFF	Input	DLL/PLL disable: When low, this input causes the DLL/PLL to be bypassed for stable, low frequency operation.	
TMS TDI	Input	IEEE1149.1 test inputs: 1.8 V I/O levels. These balls may be left not connected if the JTAG function is not used in the circuit.	
TCK	Input	IEEE1149.1 clock input: 1.8 V I/O levels. This ball must be tied to V_{SS} if the JTAG function is not used in the circuit.	
ZQ	Input	Output impedance matching input: This input is used to tune the device outputs to the system data bus impedance. DQ and CQ output impedance are set to 0.2 × RQ, where RQ is a resistor from this ball to ground. This ball can be connected directly to V_{DDQ}, which enables the minimum impedance mode. This ball cannot be connected directly to V_{SS} or left unconnected. In ODT (On Die Termination) enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input.	
ODT	Input	ODT control: **When low**; [Option 1] Low range mode is selected. The impedance range is between 52 Ω and 105 Ω (Thevenin equivalent), which follows 0.3 x RQ for 175 Ω ≤ RQ ≤ 350 Ω. [Option 2] ODT is disabled. **When high**; High range mode is selected. The impedance range is between 105 Ω and 150 Ω (Thevenin equivalent), which follows 0.6 x RQ for 175 Ω ≤ RQ ≤ 250 Ω. **When floating**; [Option 1] High range mode is selected. [Option 2] ODT is disabled.	1

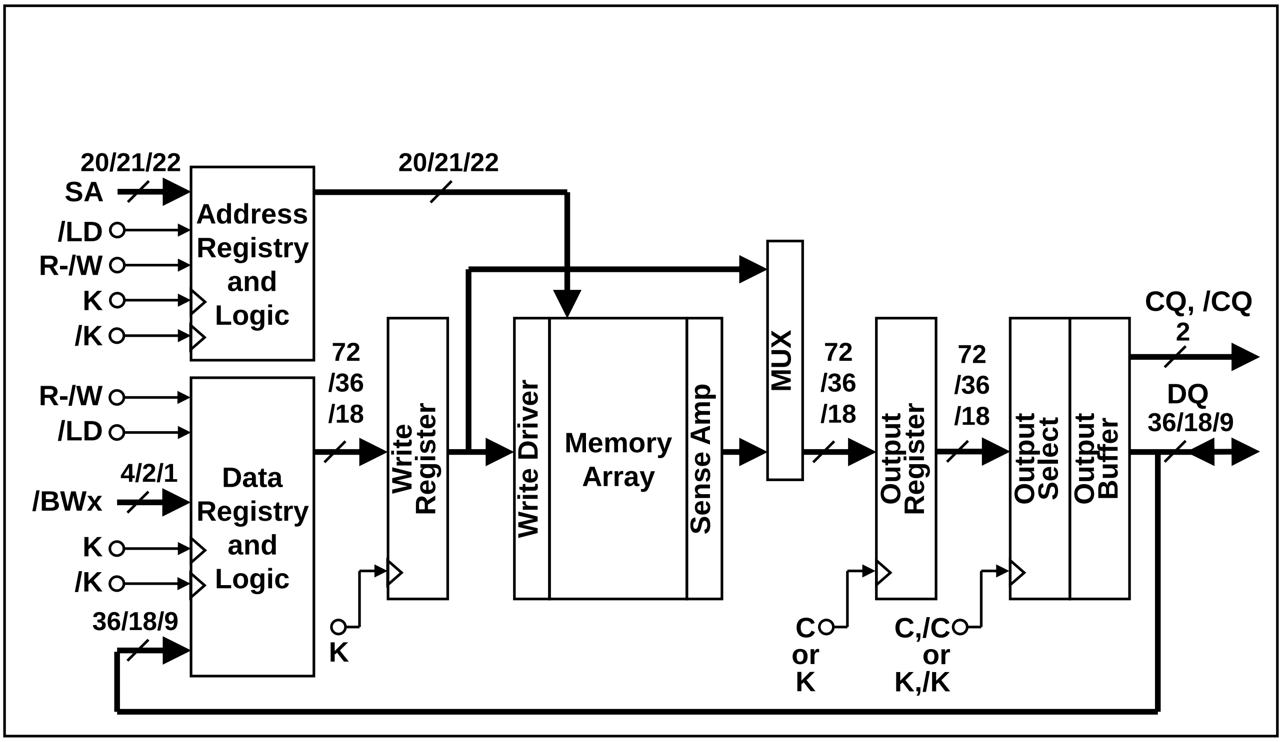
Name	I/O type	Descriptions	Notes
DQ0 to DQn	Input /Output	Synchronous data I/Os: Input data must meet setup and hold times around the rising edges of K and /K. Output data is synchronized to the respective C and /C, or to the respective K and /K if C and /C are tied high. The ×18 device uses DQ0~DQ17. DQ18~DQ35 should be treated as NC pin. The ×36 device uses DQ0~DQ35.	
CQ, /CQ	Output	Synchronous echo clock outputs: The edges of these outputs are tightly matched to the synchronous data outputs and can be used as a data valid indication. These signals run freely and do not stop when DQ tri-states.	
TDO	Output	IEEE 1149.1 test output: 1.8 V I/O level.	
QVLD	Output	Valid output indicator: The Q Valid indicates valid output data. QVLD is edge aligned with CQ and /CQ.	
V_{DD}	Supply	Power supply: 1.8 V nominal. See DC Characteristics and Operating Conditions for range.	2
V_{DDQ}	Supply	Power supply: Isolated output buffer supply. Nominally 1.5 V. See DC Characteristics and Operating Conditions for range.	2
V_{SS}	Supply	Power supply: Ground.	2
V_{REF}	-	HSTL input reference voltage: Nominally $V_{DDQ}/2$, but may be adjusted to improve system noise margin. Provides a reference voltage for the HSTL input buffers.	
NC	-	No connect: These pins can be left floating or connected to 0V ～ V_{DDQ}.	

Notes 1. Renesas status: Option 1 = Available, Option 2 = Possible.

2. All power supply and ground balls must be connected for proper operation of the device.

Block Diagram

R1QHA7236 / R1QHA7218 series



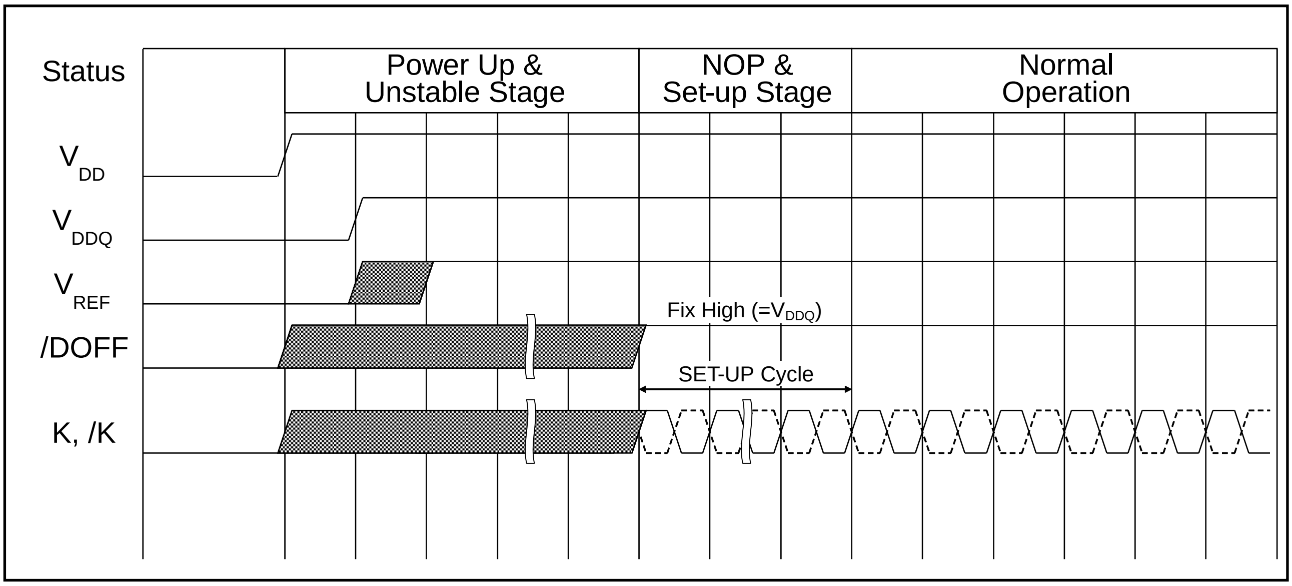
Note 1. C and /C pins do not exist in II+ series parts.

General Description

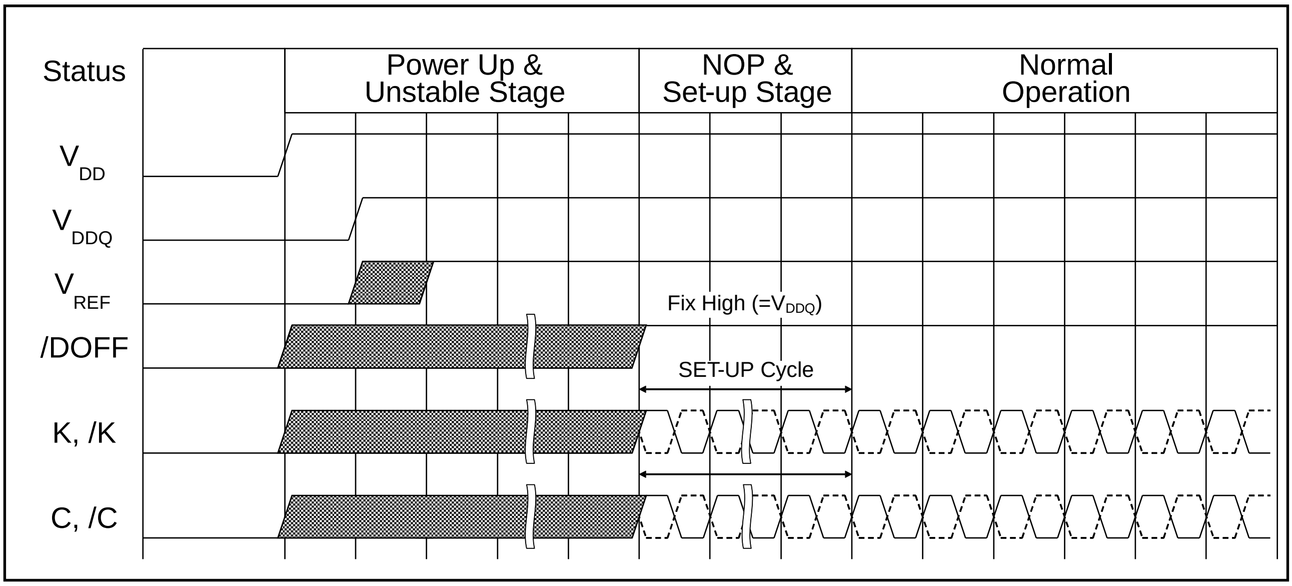
Power-up and Initialization Sequence

- V_{DD} must be stable before K, /K clocks are applied.
- Recommended voltage application sequence : $V_{SS} \rightarrow V_{DD} \rightarrow V_{DDQ}$ & $V_{REF} \rightarrow V_{IN}$. (0 V to V_{DD}, V_{DDQ} < 200 ms)
- Apply V_{REF} after V_{DDQ} or at the same time as V_{DDQ}.
- Then execute either one of the following three sequences.

1. Single Clock Mode (C and /C tied high)
   - Drive /DOFF high (/DOFF can be tied high from the start).
   - Then provide stable clocks (K, /K) for at least 1024 cycles (II series) or 20 us (II+ series).
     These meet the QDR common specification of 20 us.
     When the operating frequency is less than 180 MHz, 2048 cycles are required (II series).



2. Double Clock Mode (C and /C control outputs) **(II series only)**
- Drive /DOFF high (/DOFF can be tied high from the start)
- Then provide stable clocks (K, /K, C, /C) for at least 1024 cycles (II series).
  This meets the QDR common specification of 20 us.
  When the operating frequency is less than 180 MHz, 2048 cycles are required (II series).



3. DLL/PLL Off Mode (/DOFF tied low)
- In the "NOP and setup stage", provide stable clocks (K, /K) for at least 1024 cycles (II series) or 20 us (II+ series). These meet the QDR common specification of 20 us.

DLL/PLL Constraints

1. DLL/PLL uses K clock as its synchronizing input. The input should have low phase jitter which is specified as t_{KC} var.
2. The lower end of the frequency at which the DLL/PLL can operate is 120 MHz.
   (Please refer to AC Characteristics table for detail.)
3. When the operating frequency is changed or /DOFF level is changed, setup cycles are required again.

Programmable Output Impedance

1. Output buffer impedance can be programmed by terminating the ZQ ball to V_{SS} through a precision resistor (RQ). The value of RQ is five times the output impedance desired. The allowable range of RQ to guarantee impedance matching with a tolerance of 15% is 250 Ω typical. The total external capacitance of ZQ ball must be less than 7.5 pF.

QVLD (Valid data indicator)

1. QVLD is provided on the QDR-II+ and DDR-II+ to simplify data capture on high speed systems. The Q Valid indicates valid output data. QVLD is activated half cycle before the read data for the receiver to be ready for capturing the data. QVLD is inactivated half cycle before the read finish for the receiver to stop capturing the data. QVLD is edge aligned with CQ and /CQ.

ODT (On Die Termination)

R1QD, R1QE series

1. To reduce reflection which produces noise and lowers signal quality, the signals should be terminated, especially at high frequency. Renesas offers ODT on the input signals to QDR-II+ and DDR-II+ family of devices. (See the ODT pin table)
2. In ODT enable devices, the ODT termination values tracks the value of RQ. The ODT range is selected by ODT control input. (See the ODT range table)
3. In DDR-II+ devices having common I/O bus, ODT is automatically enabled when the device inputs data and disabled when the device outputs data.
4. There is no difference in AC timing characteristics between the SRAMs with ODT and SRAMs without ODT.
5. There is no increase in the I_{DD} of SRAMs with ODT, however, there is an increase in the I_{DDQ} (current consumption from the I/O voltage supply) with ODT.

ODT range

ODT control pin	Thevenin equivalent resistance (R_{THEV})		Unit	Notes
	Option 1	Option 2	-	6
Low	0.3 × RQ	(ODT disable)	Ω	1, 4
High	0.6 × RQ	0.6 × RQ	Ω	2, 5
Floating	0.6 × RQ	(ODT disable)	Ω	3

Notes 1. Allowable range of RQ for Option 1 to guarantee impedance matching a tolerance of ± 20 % is 175 Ω ≤ RQ ≤ 350 Ω.

2. Allowable range of RQ to guarantee impedance matching a tolerance of ± 20 % is 175 Ω ≤ RQ ≤ 250 Ω.

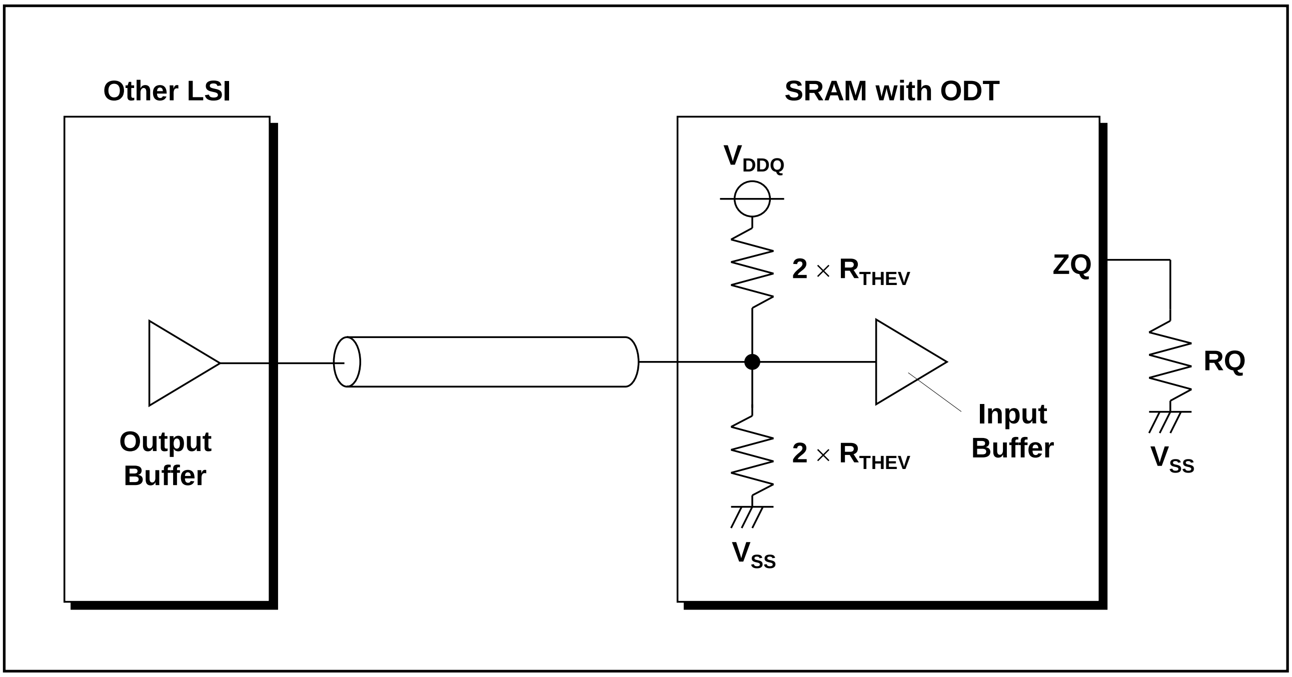
3. Allowable range of RQ for Option 1 to guarantee impedance matching a tolerance of ± 20 % is 175 Ω ≤ RQ ≤ 250 Ω.

4. At option 1, ODT control pin is connected to V_{DDQ} through 3.5 kΩ. Therefore it is recommended to connect it to V_{SS} through less than 100 Ω to make it low.

5. At option 2, ODT control pin is connected to V_{SS} through 3.5 kΩ. Therefore it is recommended to connect it to V_{DDQ} through less than 100 Ω to make it high.

6. Renesas status: Option 1 = Available, Option 2 = Possible. If you need devices with option 2, please contact Renesas sales office.

Thevenin termination



ODT pin

R1QD, R1QE series

Pin name	ODT On/Off timing			Notes
	Option 1	Option 2		3
		ODT pin = High	ODT pin = Low or Floating	
D_0 ~ D_n in separate I/O devices	Always On		Always Off	1
DQ_0 ~ DQ_n in common I/O devices	Off: First Read Command + Read Latency - 0.5 cycle On: Last Read Command + Read Latency + BL/2 cycle + 0.5 cycle (See below timing chart)		Always Off	2
$/BW_x$	Always On		Always Off	
K, /K	Always On		Always Off	

Notes 1. Separate I/O devices is R1QD series.

2. Common I/O devices is R1QE series.

3. Renesas status: Option 1 = Available, Option 2 = Possible. If you need devices with option 2, please contact Renesas sales office.

K Truth Table

<table>
<tr><th>Operation</th><th>K</th><th>/LD</th><th>R-/W</th><th colspan="4">DQ</th></tr>
<tr><td rowspan="3">Write Cycle : Load address, input write data on consecutive K and /K rising edges</td><td rowspan="3">↑</td><td rowspan="3">L</td><td rowspan="3">L</td><td colspan="4">Data in</td></tr>
<tr><td colspan="2">Input data</td><td>D(A1)</td><td>D(A2)</td></tr>
<tr><td colspan="2">Input clock</td><td>K(t+1) ↑</td><td>/K(t+1) ↑</td></tr>
<tr><td rowspan="5">Read Cycle : Load address, output read data on consecutive C and /C rising edges</td><td rowspan="5">↑</td><td rowspan="5">L</td><td rowspan="5">H</td><td colspan="4">Data out</td></tr>
<tr><td colspan="2">Output data</td><td>Q(A1)</td><td>Q(A2)</td></tr>
<tr><td rowspan="3">Input clock for Q</td><td>RL[*8] = 1.5</td><td>/C(t+1) ↑</td><td>C(t+2) ↑</td></tr>
<tr><td>RL = 2.0</td><td>C(t+2) ↑</td><td>/C(t+2) ↑</td></tr>
<tr><td>RL = 2.5</td><td>/C(t+2) ↑</td><td>C(t+3) ↑</td></tr>
<tr><td>NOP (No operation)</td><td>↑</td><td>H</td><td>×</td><td colspan="4">High-Z</td></tr>
<tr><td>Standby (Clock stopped)</td><td>Stopped</td><td>×</td><td>×</td><td colspan="4">Previous state</td></tr>
</table>

Notes 1. H: high level, L: low level, ×: don't care, ↑: rising edge.

2. Data inputs are registered at K and /K rising edges. Data outputs are delivered at C and /C rising edges, except if C and /C are high, then data outputs are delivered at K and /K rising edges.

3. /LD and R-/W must meet setup/hold times around the rising edges (low to high) of K and are registered at the rising edge of K.

4. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

5. Refer to state diagram and timing diagrams for clarification.

6. When clocks are stopped, the following cases are recommended; the case of K = low, /K = high, C = low and /C = high, or the case of K = high, /K = low, C = high and /C = low. This condition is not essential, but permits most rapid restart by overcoming transmission line charging symmetrically.

7. A1 refers to the address input during a WRITE or READ cycle. A2 refers to the next internal burst address in accordance with the linear burst sequence.

8. RL = Read Latency (unit = cycle).

Byte Write Truth Table (x36)

Operation	K	/K	/BW0	/BW1	/BW2	/BW3
Write D0 to D35	↑	-	L	L	L	L
	-	↑	L	L	L	L
Write D0 to D8	↑	-	L	H	H	H
	-	↑	L	H	H	H
Write D9 to D17	↑	-	H	L	H	H
	-	↑	H	L	H	H
Write D18 to D26	↑	-	H	H	L	H
	-	↑	H	H	L	H
Write D27 to D35	↑	-	H	H	H	L
	-	↑	H	H	H	L
Write nothing	↑	-	H	H	H	H
	-	↑	H	H	H	H

Notes 1. H: high level, L: low level, ↑: rising edge.

2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

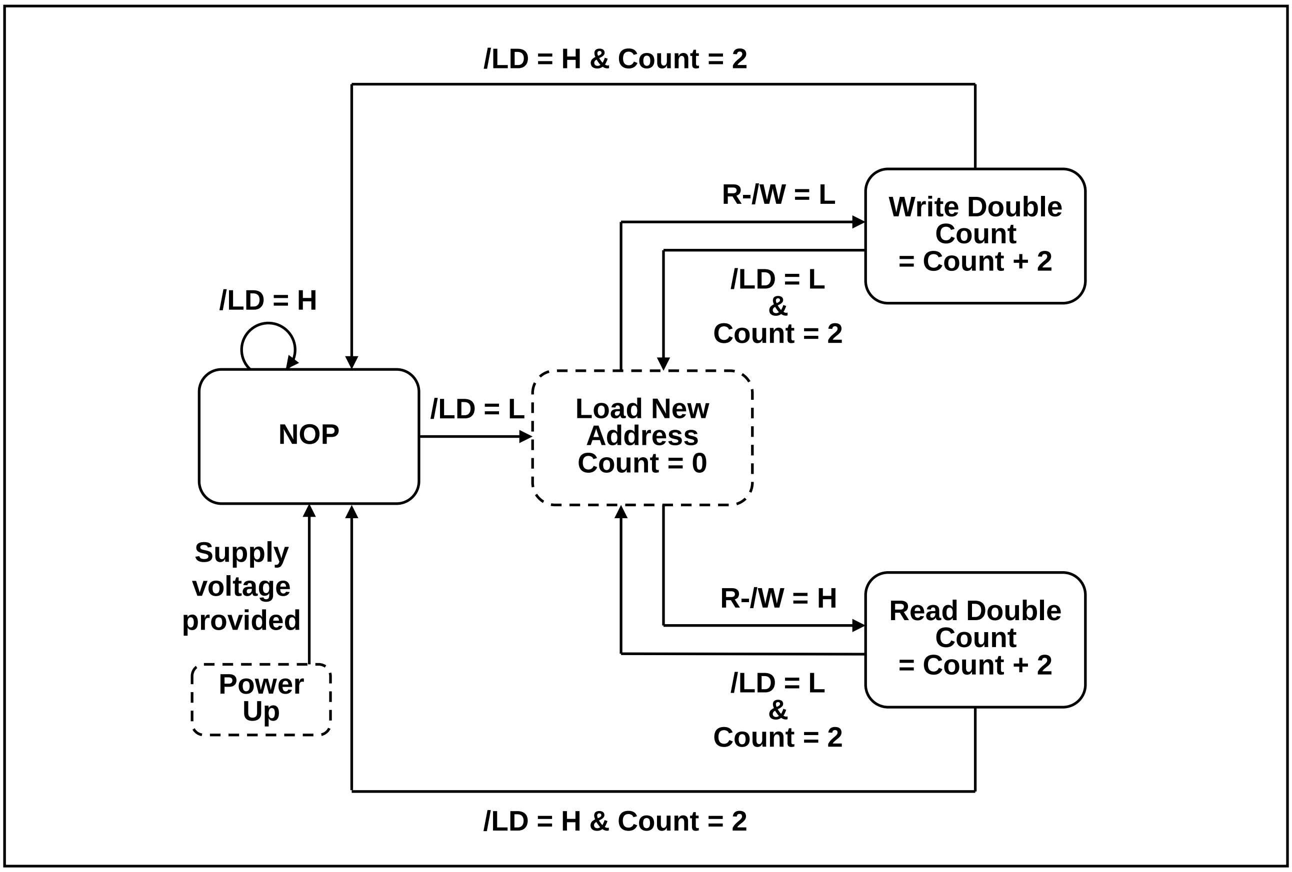
Byte Write Truth Table (x18)

Operation	K	/K	/BW0	/BW1
Write D0 to D17	↑	-	L	L
	-	↑	L	L
Write D0 to D8	↑	-	L	H
	-	↑	L	H
Write D9 to D17	↑	-	H	L
	-	↑	H	L
Write nothing	↑	-	H	H
	-	↑	H	H

Notes 1. H: high level, L: low level, ↑: rising edge.

2. Assumes a WRITE cycle was initiated. /BWx can be altered for any portion of the BURST WRITE operation provided that the setup and hold requirements are satisfied.

Bus Cycle State Diagram



Notes 1. SA0 is internally advanced in accordance with the burst order table. Bus cycle is terminated at the end of this sequence (burst count = 2).

2. State machine control timing sequence is controlled by K.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit	Notes
Input voltage on any ball	V_{IN}	-0.5 to V_{DD} + 0.5 (2.5 V max.)	V	1, 4
Input/output voltage	$V_{I/O}$	-0.5 to V_{DDQ} + 0.5 (2.5 V max.)	V	1, 4
Core supply voltage	V_{DD}	-0.5 to 2.5	V	1, 4
Output supply voltage	V_{DDQ}	-0.5 to V_{DD}	V	1, 4
Junction temperature	T_j	+125 (max)	ºC	5
Storage temperature	T_{STG}	-55 to +125	ºC	

Notes 1. All voltage is referenced to V_{SS}.

2. Permanent device damage may occur if Absolute Maximum Ratings are exceeded. Functional operation should be restricted the Operation Conditions. Exposure to higher than recommended voltages for extended periods of time could affect device reliability.

3. These CMOS memory circuits have been designed to meet the DC and AC specifications shown in the tables after thermal equilibrium has been established.

4. The following supply voltage application sequence is recommended: V_{SS}, V_{DD}, V_{DDQ}, V_{REF} then V_{IN}. Remember, according to the Absolute Maximum Ratings table, V_{DDQ} is not to exceed 2.5 V, whatever the instantaneous value of V_{DDQ}.

5. Some method of cooling or airflow should be considered in the system. (Especially for high frequency or ODT parts)

Recommended DC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Power supply voltage – core	V_{DD}	1.7	1.8	1.9	V	1
Power supply voltage – I/O	V_{DDQ}	1.4	1.5	V_{DD}	V	1, 2
Input reference voltage – I/O	V_{REF}	0.68	0.75	0.95	V	3
Input high voltage	$V_{IH(DC)}$	V_{REF} + 0.1	-	V_{DDQ} + 0.3	V	1, 4, 5
Input low voltage	$V_{IL(DC)}$	-0.3	-	V_{REF} – 0.1	V	1, 4, 5

Notes 1. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time $V_{DDQ} < V_{DD}$ and $V_{IH} < V_{DDQ}$. During normal operation, V_{DDQ} must not exceed V_{DD}.

2. Please pay attention to T_j not to exceed the temperature shown in the absolute maximum ratings table due to current from V_{DDQ}.

3. Peak to peak AC component superimposed on V_{REF} may not exceed 5% of V_{REF}.

4. These are DC test criteria. The AC V_{IH} / V_{IL} levels are defined separately to measure timing parameters.

5. Overshoot: $V_{IH(AC)} \leq V_{DDQ} + 0.5$ V for $t \leq t_{KHKH}/2$

Undershoot: $V_{IL(AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$

During normal operation, $V_{IH(DC)}$ must not exceed V_{DDQ} and $V_{IL(DC)}$ must not be lower than V_{SS}.

DC Characteristics

T_a = -40 ~ +85°C

V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V

Operating Supply Current (Write / Read)

Symbol = I_{DD}. Unit = mA.

No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation	Frequency (max) (MHz)	533	500	400	300	250	200
						Cycle Time (min) (ns)	1.875	2.00	2.50	3.30	4.00	5.00
						Speed bin	-19	-20	-25	-33	-40	
1	QDR II	B2	1.5	No	x 9	R1Q2A7209ABB-yy					760	670
2					x18	R1Q2A7218ABB-yy					890	780
3					x36	R1Q2A7236ABB-yy					950	830
4		B4			x18	R1Q3A7218ABB-yy			820	730		
5					x36	R1Q3A7236ABB-yy			850	750		
6	DDR II	B2			x18	R1Q4A7218ABB-yy			700	630		
7					x36	R1Q4A7236ABB-yy			760	680		
8	QDR II+	B4	2.0	No	x18	R1QAA7218ABB-yy	1220	1160	1070			
9					x36	R1QAA7236ABB-yy	1280	1220	1130			
10	DDR II+	B2			x18	R1QBA7218ABB-yy	1030	990	920			
11					x36	R1QBA7236ABB-yy	1110	1060	990			
12	QDR II+	B4		Yes	x18	R1QDA7218ABB-yy	1220	1160	1070			
13					x36	R1QDA7236ABB-yy	1280	1220	1130			
14	DDR II+	B2			x18	R1QEA7218ABB-yy	1030	990	920			
15					x36	R1QEA7236ABB-yy	1110	1060	990			
16	QDR II+	B4	2.5	No	x18	R1QGA7218ABB-yy			980			
17					x36	R1QGA7236ABB-yy			1060			
18	DDR II+	B2			x18	R1QHA7218ABB-yy			850			
19					x36	R1QHA7236ABB-yy			910			

Notes 1. "yy" represents the speed bin. "R1QDA7236ABB-20" can operate at 500 MHz(max) of frequency, for example.

2. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.

3. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.

4. Operating supply currents (I_{DD}) are measured at 100% bus utilization. I_{DD} of QDR family is current of device with 100% write and 100% read cycle. I_{DD} of DDR family is current of device with 100% write cycle (if I_{DD}(Write) > I_{DD}(Read)) or 100% read cycle (if I_{DD}(Write) < I_{DD}(Read)).

Standby Supply Current (NOP)

Symbol = I_{SB1}. Unit = mA.

No	Product Type	Burst Length	Latency (Cycle)	ODT	Organi-zation	Frequency (max) (MHz)	533	500	400	300	250	200
						Cycle Time (min) (ns)	1.875	2.00	2.50	3.30	4.00	5.00
						Speed bin	-19	-20	-25	-33	-40	
1	QDR II	B2	1.5	No	x 9	R1Q2A7209ABB-yy					570	510
2					x18	R1Q2A7218ABB-yy					670	600
3					x36	R1Q2A7236ABB-yy					710	630
4		B4			x18	R1Q3A7218ABB-yy			590	520		
5					x36	R1Q3A7236ABB-yy			610	540		
6	DDR II	B2			x18	R1Q4A7218ABB-yy			610	560		
7					x36	R1Q4A7236ABB-yy			670	610		
8	QDR II+	B4	2.0	No	x18	R1QAA7218ABB-yy	870	830	780			
9					x36	R1QAA7236ABB-yy	910	870	810			
10	DDR II+	B2			x18	R1QBA7218ABB-yy	870	840	780			
11					x36	R1QBA7236ABB-yy	960	920	860			
12	QDR II+	B4		Yes	x18	R1QDA7218ABB-yy	870	830	780			
13					x36	R1QDA7236ABB-yy	910	870	810			
14	DDR II+	B2			x18	R1QEA7218ABB-yy	870	840	780			
15					x36	R1QEA7236ABB-yy	960	920	860			
16	QDR II+	B4	2.5	No	x18	R1QGA7218ABB-yy			720			
17					x36	R1QGA7236ABB-yy			770			
18	DDR II+	B2			x18	R1QHA7218ABB-yy			720			
19					x36	R1QHA7236ABB-yy			790			

Notes 1. "yy" represents the speed bin. "R1QDA7236ABB-20" can operate at 500 MHz(max) of frequency, for example.

2. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.

3. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.

4. Reference value. (Condition = NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.)

Leakage Currents & Output Voltage

Parameter	Symbol	Min	Max	Unit	Test condition	Notes
Input leakage current	I_{LI}	-2	2	μA		10
Output leakage current	I_{LO}	-5	5	μA		11
Output high voltage	V_{OH} (Low)	V_{DDQ} – 0.2	V_{DDQ}	V	$\lvert I_{OH}\rvert \leq 0.1$ mA	8, 9
	V_{OH}	$V_{DDQ}/2$ – 0.12	$V_{DDQ}/2$ + 0.12	V		6, 8, 9
Output low voltage	V_{OL} (Low)	V_{SS}	0.2	V	$I_{OL} \leq 0.1$ mA	8, 9
	V_{OL}	$V_{DDQ}/2$ – 0.12	$V_{DDQ}/2$ + 0.12	V		7, 8, 9

Notes 1. All inputs (except ZQ, V_{REF}) are held at either V_{IH} or V_{IL}.

2. I_{OUT} = 0 mA. V_{DD} = V_{DD} max, t_{KHKH} = t_{KHKH} min.

3. Operating supply currents (I_{DD}) are measured at 100% bus utilization. I_{DD} of QDR family is current of device with 100% write and 100% read cycle. I_{DD} of DDR family is current of device with 100% write cycle (if I_{DD}(Write) > I_{DD}(Read)) or 100% read cycle (if I_{DD}(Write) < I_{DD}(Read)).

4. All address / data inputs are static at either $V_{IN} > V_{IH}$ or $V_{IN} < V_{IL}$.

5. Reference value. (Condition = NOP currents are valid when entering NOP after all pending READ and WRITE cycles are completed.)

6. Outputs are impedance-controlled. $\lvert I_{OH}\rvert = (V_{DDQ}/2)/(RQ/5)$ for values of $175\ \Omega \leq RQ \leq 350\ \Omega$.

7. Outputs are impedance-controlled. $I_{OL} = (V_{DDQ}/2)/(RQ/5)$ for values of $175\ \Omega \leq RQ \leq 350\ \Omega$.

8. AC load current is higher than the shown DC values. AC I/O curves are available upon request.

9. HSTL outputs meet JEDEC HSTL Class I and Class II standards.

10. $0 \leq V_{IN} \leq V_{DDQ}$ for all input balls (except V_{REF}, ZQ, TCK, TMS, TDI ball).

If R1QD and R1QE series, balls with ODT do not follow this spec.

11. $0 \leq V_{OUT} \leq V_{DDQ}$ (except TDO ball), output disabled.

Thermal Resistance

Parameter	Symbol	Airflow	Typ	Unit	Test condition	Notes
Junction to Ambient	θ_{JA}	1 m/s	11.0	°C/W	EIA/JEDEC JESD51	1
Junction to Case	θ_{JA}	-	4.4			

Notes 1. These parameters are calculated under the condition. These are reference values.

2. $T_j = T_a + \theta_{JA} \times Pd$

$T_j = T_c + \theta_{JC} \times Pd$

where

T_j : Junction temperature when the device has achieved a steady-state after application of Pd (°C)

T_a : Ambient temperature (°C)

T_c : Temperature of external surface of the package or case (°C)

θ_{JA} : Thermal resistance from junction-to-ambient (°C/W)

θ_{JC} : Thermal resistance from junction-to-case (package) (°C/W)

Pd : Power dissipation that produced change in junction temperature (W) (cf.JESD51-2A)

Capacitance

T_a = +25°C, Frequency = 1.0MHz, V_{DD} = 1.8V, V_{DDQ} = 1.5V

Parameter	Symbol	Min	Typ	Max	Unit	Test condition	Notes
Input capacitance (SA, /R, /W, /BW, $D_{(separate)}$)	C_{IN}	-	4	5	pF	V_{IN} = 0 V	1, 2
Clock input capacitance (K, /K, C, /C)	C_{CLK}	-	4	5	pF	V_{CLK} = 0 V	1, 2
Output capacitance ($Q_{(separate)}$, $DQ_{(common)}$, CQ, /CQ)	$C_{I/O}$	-	5	6	pF	$V_{I/O}$ = 0 V	1, 2

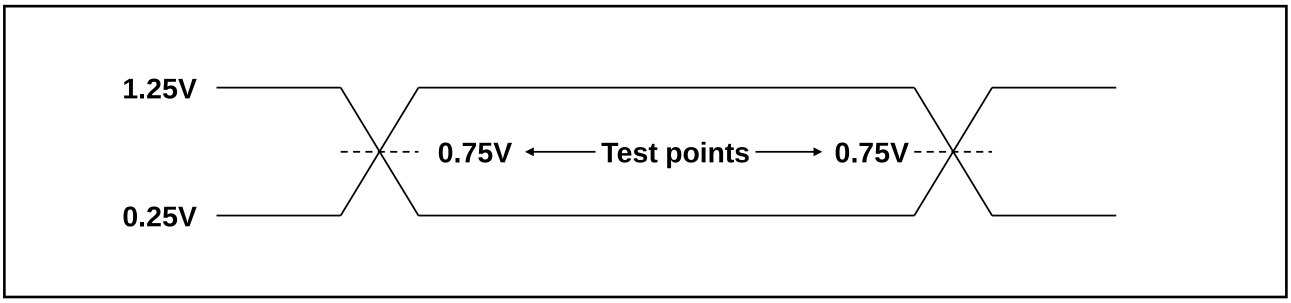
Notes 1. These parameters are sampled and not 100% tested.

2. Except JTAG (TCK, TMS, TDI, TDO) pins.

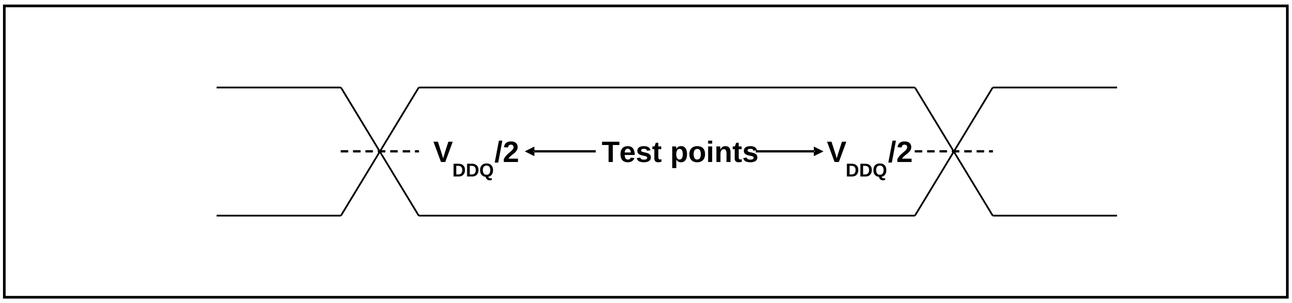
AC Test Conditions

Input waveform

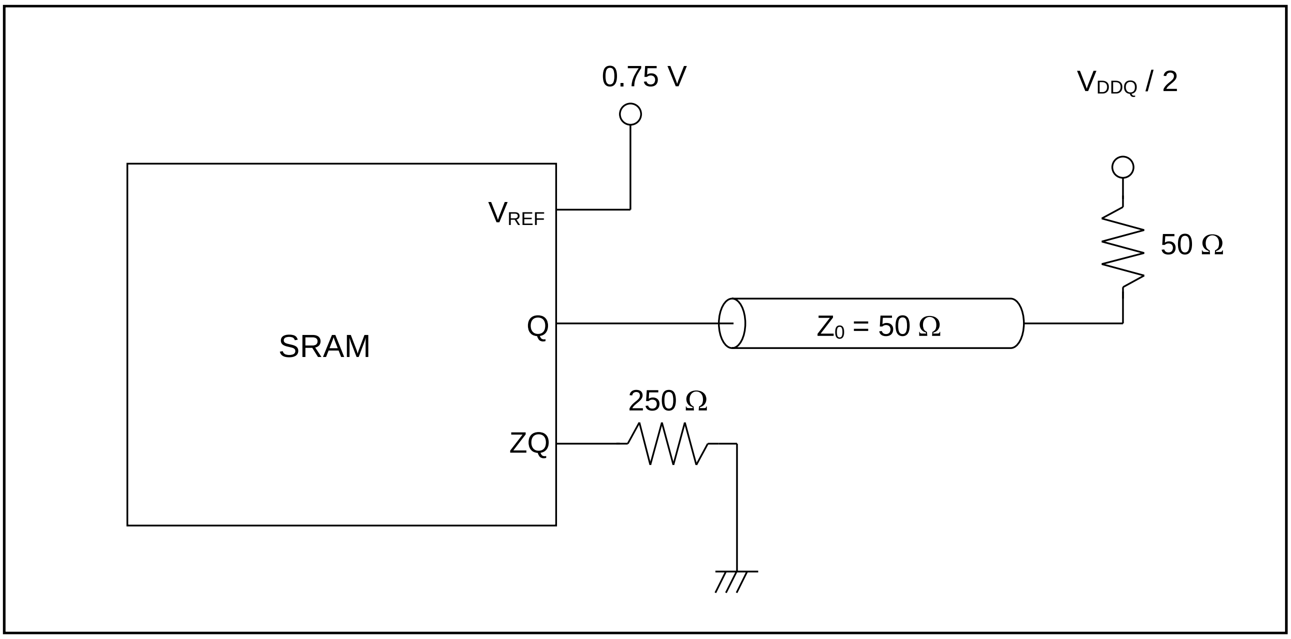
Rise/fall time ≤ 0.3 ns



Output waveform



Output load conditions



AC Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	$V_{IH(AC)}$	V_{REF} + 0.2	-	-	V	1, 2, 3, 4
Input low voltage	$V_{IL(AC)}$	-	-	V_{REF} – 0.2	V	1, 2, 3, 4

Notes 1. All voltages referenced to V_{SS} (GND).

During normal operation, V_{DDQ} must not exceed V_{DD}.

2. These conditions are for AC functions only, not for AC parameter test.

3. Overshoot: $V_{IH(AC)} \leq V_{DDQ} + 0.5$ V for $t \leq t_{KHKH}/2$

Undershoot: $V_{IL(AC)} \geq -0.5$ V for $t \leq t_{KHKH}/2$

Control input signals may not have pulse widths less than t_{KHKL}(min) or operate at cycle rates less than t_{KHKH}(min).

4. To maintain a valid level, the transitioning edge of the input must:

a. Sustain a constant slew rate from the current AC level through the target AC level, $V_{IL(AC)}$ or $V_{IH(AC)}$.

b. Reach at least the target AC level.

c. After the AC target level is reached, continue to maintain at least the target DC level, $V_{IL(DC)}$ or $V_{IH(DC)}$.

AC Characteristics (QDR-II+, DDR-II+ series, Read Latency = 2.0cycle)

Ta = -40 ~ +85°C
V_{DD} = 1.8V ±0.1V, V_{DDQ} = 1.5V, V_{REF} = 0.75V

Parameter	Symbol	-25						Unit	Notes
		400 MHz		375 MHz		333 MHz			
		Min	Max	Min	Max	Min	Max		
Clock									
Average clock cycle time (K, /K)	t_{KHKH}	2.50	4.00	2.66	4.00	3.00	4.00	ns	
Clock high time (K, /K)	t_{KHKL}	0.40	-	0.40	-	0.40	-	Cycle	
Clock low time (K, /K)	t_{KLKH}	0.40	-	0.40	-	0.40	-	Cycle	
Clock to /clock (K to /K)	$t_{KH/KH}$	0.425	-	0.425	-	0.425	-	Cycle	
/Clock to clock (/K to K)	$t_{/KHKH}$	0.425	-	0.425	-	0.425	-	Cycle	
DLL / PLL timing									
Clock phase jitter (K, /K)	t_{KC} var	-	0.20	-	0.20	-	0.20	ns	3
Lock time (K)	t_{KC} lock	20	-	20	-	20	-	us	2
K static to DLL/PLL reset	t_{KC} reset	30	-	30	-	30	-	ns	7
Output Times									
K, /K high to output valid	t_{CHQV}	-	0.55	-	0.55	-	0.55	ns	
K, /K high to output hold	t_{CHQX}	-0.35	-	-0.35	-	-0.35	-	ns	
K, /K high to echo clock valid	t_{CHCQV}	-	0.55	-	0.55	-	0.55	ns	
K, /K high to echo clock hold	t_{CHCQX}	-0.35	-	-0.35	-	-0.35	-	ns	
CQ, /CQ high to output valid	t_{CQHQV}	-	0.20	-	0.20	-	0.20	ns	4, 7
CQ, /CQ high to output hold	t_{CQHQX}	-0.20	-	-0.20	-	-0.20	-	ns	4,7
K, /K high to output high-Z	t_{CHQZ}	-	0.55	-	0.55	-	0.55	ns	5, 6
K, /K high to output low-Z	t_{CHQX1}	-0.35	-	-0.35	-	-0.35	-	ns	5
CQ high to QVLD valid	t_{QVLD}	-0.20	0.20	-0.20	0.20	-0.20	0.20	ns	7

Parameter	Symbol	-25						Unit	Notes
		400 MHz		375 MHz		333 MHz			
		Min	Max	Min	Max	Min	Max		
Setup Times									
Address valid to K rising edge	t_{AVKH}	0.40	-	0.40	-	0.40	-	ns	1, 8
Control inputs valid to K rising edge	t_{IVKH}	0.40	-	0.40	-	0.40	-	ns	1, 8
Data-in valid to K, /K rising edge	t_{DVKH}	0.28	-	0.28	-	0.28	-	ns	1, 9
Hold Times									
K rising edge to address hold	t_{KHAX}	0.40	-	0.40	-	0.40	-	ns	1, 8
K rising edge to control inputs hold	t_{KHIX}	0.40	-	0.40	-	0.40	-	ns	1, 8
K, /K rising edge to data-in hold	t_{KHDX}	0.28	-	0.28	-	0.28	-	ns	1, 9

Notes 1. This is a synchronous device. All addresses, data and control lines must meet the specified setup and hold times for all latching clock edges.

2. V_{DD} and V_{DDQ} slew rate must be less than 0.1 V DC per 50 ns for DLL/PLL lock retention. DLL/PLL lock time begins once V_{DD}, V_{DDQ} and input clock are stable.
It is recommended that the device is kept inactive during these cycles.
This specification meets the QDR common spec. of 20 us.

3. Clock phase jitter is the variance from clock rising edge to the next expected clock rising edge.

4. Echo clock is very tightly controlled to data valid / data hold. By design, there is a ±0.1 ns variation from echo clock to data. The datasheet parameters reflect tester guardbands and test setup variations.

5. Transitions are measured ±100 mV from steady-state voltage.

6. At any given voltage and temperature t_{CHQZ} is less than t_{CHQX1} and t_{CHQV}.

7. These parameters are sampled.

8. t_{AVKH}, t_{IVKH}, t_{KHAX}, t_{KHIX} spec is determined by the actual frequency regardless of Part Number (Marking Name). The following is the spec for the actual frequency.

0.30 ns for ≤533MHz & >500MHz
0.33 ns for ≤500MHz & >450MHz
0.40 ns for ≤450MHz & ≥250MHz

9. t_{DVKH}, t_{KHDX} spec is determined by the actual frequency regardless of Part Number (Marking Name). The following is the spec for the actual frequency.

0.20 ns for ≤533MHz & >500MHz
0.22 ns for ≤500MHz & >450MHz
0.25 ns for ≤450MHz & >400MHz
0.28 ns for ≤400MHz & ≥250MHz

Remarks 1. Test conditions as specified with the output loading as shown in AC Test Conditions unless otherwise noted.

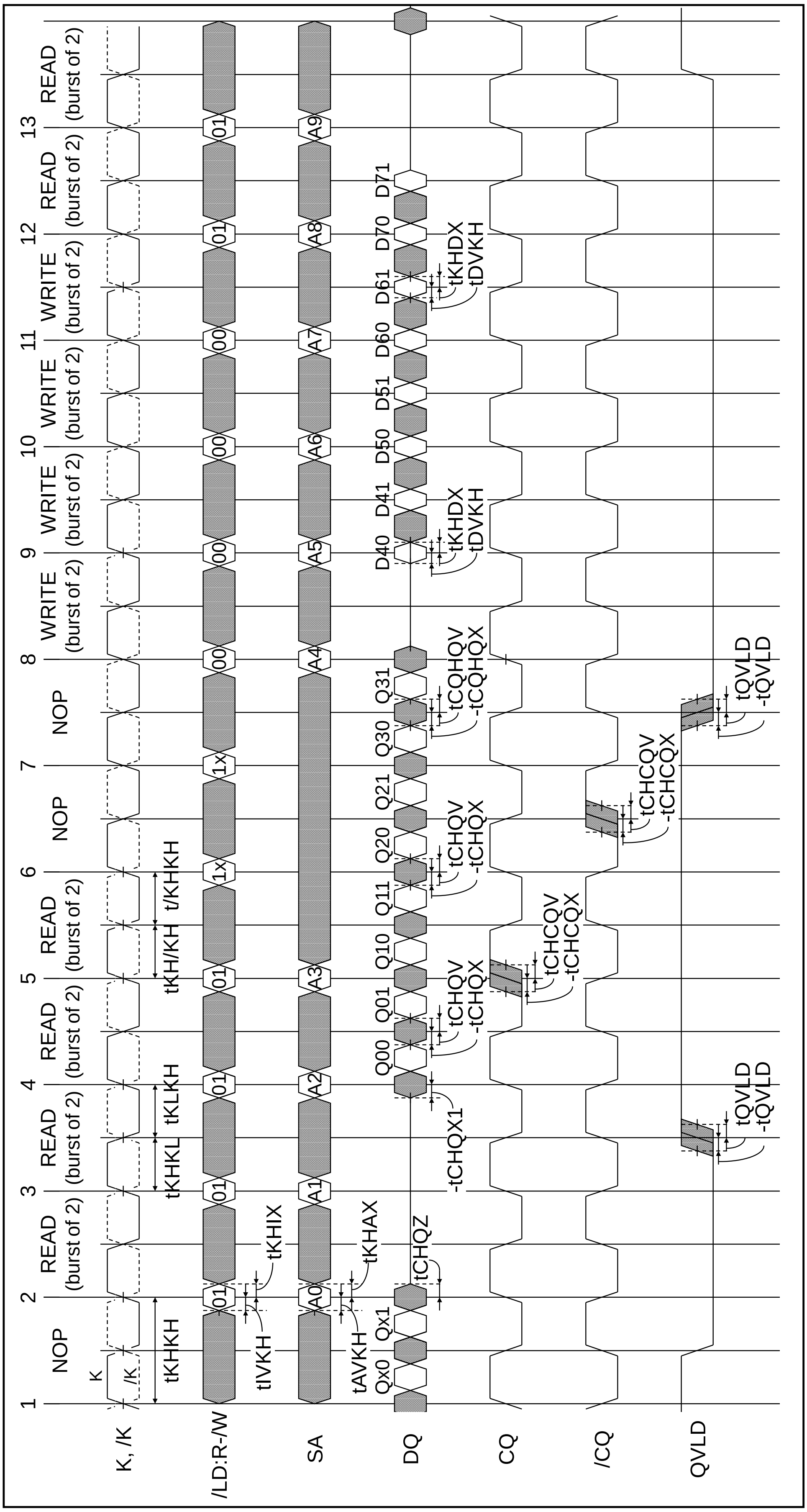
2. Control input signals may not be operated with pulse widths less than t_{KHKL} (min).

3. V_{DDQ} is +1.5 V DC. V_{REF} is +0.75 V DC.

4. Control signals are /R, /W (QDR series), /LD, R-/W (DDR series), /BW, /BW0, /BW1, /BW2 and /BW3. Setup and hold times of /BWx signals must be the same as those of Data-in signals.

Timing Waveforms

Read and Write Timing (DDRII+, B2, Read Latency = 2.0 cycle)



Notes 1. Q00 refers to output from address A0. Q01 refers to output from the next internal burst address following A0, etc.

2. Outputs are disabled (High-Z) N clock cycle after the last read cycle. Here, N = Read Latency + Burst Length × 0.5.

3. In this example, if address A8 = A7, then data Q80 = D70, Q81 = D71, etc. Write data is forwarded immediately as read results.

4. To control read and write operations, /BW signals must operate at the same timing as Data-in signals.

5. The second NOP cycle is not necessary for correct device operation; however, at high clock frequencies it may be required to prevent bus contention.

JTAG Specification

These products support a limited set of JTAG functions as in IEEE standard 1149.1.

Disabling the Test Access Port

It is possible to use this device without utilizing the TAP. To disable the TAP controller without interfering with normal operation of the device, TCK must be tied to V_{SS} to preclude mid level inputs.

TDI and TMS are internally pulled up and may be unconnected, or may be connected to V_{DD} through a pull up resistor.

TDO should be left unconnected.

Test Access Port (TAP) Pins

Symbol I/O	Pin assignments	Description	Notes
TCK	2R	Test clock input. All inputs are captured on the rising edge of TCK and all outputs propagate from the falling edge of TCK.	
TMS	10R	Test mode select. This is the command input for the TAP controller state machine.	
TDI	11R	Test data input. This is the input side of the serial registers placed between TDI and TDO. The register placed between TDI and TDO is determined by the state of the TAP controller state machine and the instruction that is currently loaded in the TAP instruction.	
TDO	1R	Test data output. Output changes in response to the falling edge of TCK. This is the output side of the serial registers placed between TDI and TDO.	

Note 1. The device does not have TRST (TAP reset). The Test-Logic Reset state is entered while TMS is held high for five rising edges of TCK. The TAP controller state is also reset on SRAM POWER-UP.

TAP DC Operating Characteristics

T_a = -40 ~ +85°C

V_{DD} = 1.8V ±0.1V

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Input high voltage	V_{IH}	+1.3	-	V_{DD} + 0.3	V	
Input low voltage	V_{IL}	-0.3	-	+0.5	V	
Input leakage current	I_{LI}	-5.0	-	+5.0	μA	0 V ≤ V_{IN} ≤ V_{DD}
Output leakage current	I_{LO}	-5.0	-	+5.0	μA	0 V ≤ V_{IN} ≤ V_{DD}, output disabled
Output low voltage	V_{OL1}	-	-	0.2	V	I_{OLC} = 100 μA
	V_{OL2}	-	-	0.4	V	I_{OLT} = 2 mA
Output high voltage	V_{OH1}	1.6	-	-	V	$\|I_{OHC}\|$ = 100 μA
	V_{OH2}	1.4	-	-	V	$\|I_{OHT}\|$ = 2 mA

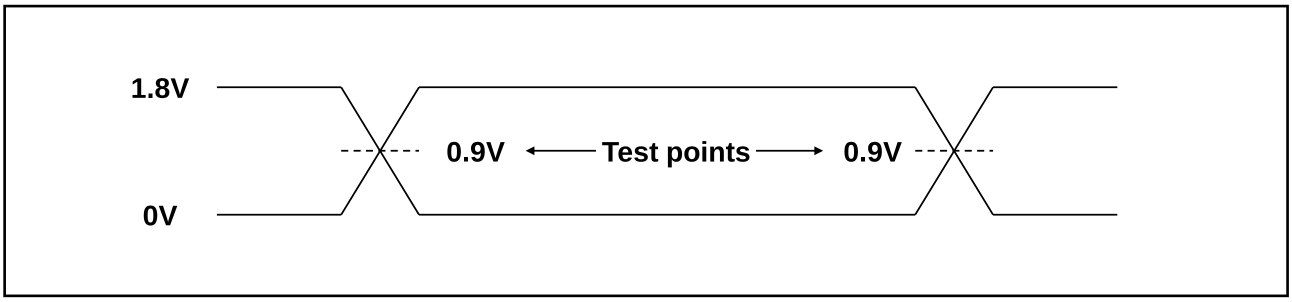
Notes 1. All voltages referenced to V_{SS} (GND).

2. At power-up, V_{DD} and V_{DDQ} are assumed to be a linear ramp from 0V to V_{DD}(min.) or V_{DDQ}(min.) within 200ms. During this time V_{DDQ} < V_{DD} and V_{IH} < V_{DDQ}. During normal operation, V_{DDQ} must not exceed V_{DD}.

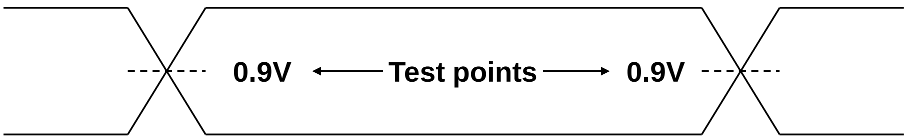
TAP AC Test Conditions

Parameter	Symbol	Conditions	Unit	Notes
Input timing measurement reference levels	V_{REF}	0.9	V	
Input pulse levels	V_{IL}, V_{IH}	0 to 1.8	V	
Input rise/fall time	tr, tf	≤ 1.0	ns	
Output timing measurement reference levels		0.9	V	
Test load termination supply voltage (V_{TT})		0.9	V	
Output load		See figures		

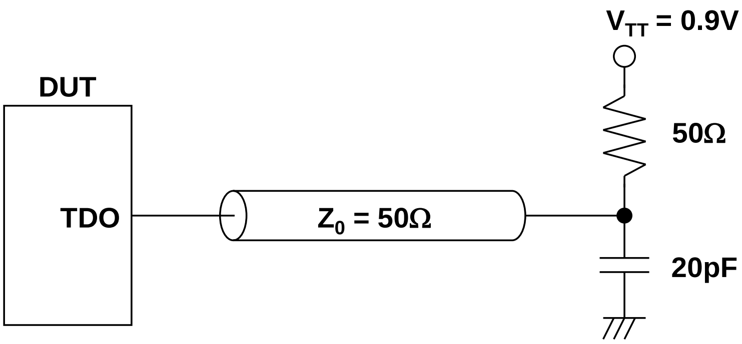
Input waveform



Output waveform



Output load condition



External Load at Test

TAP AC Operating Characteristics

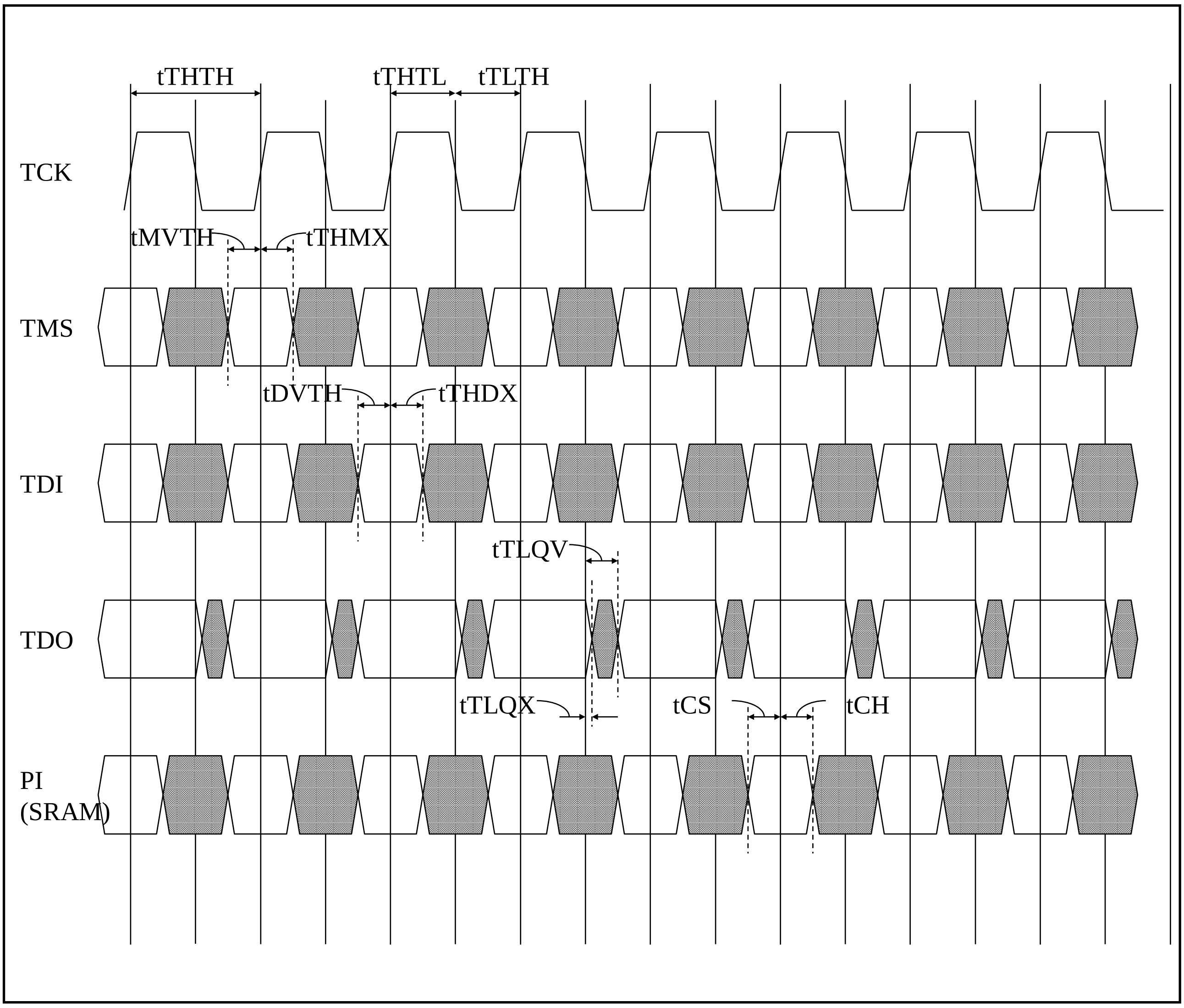
T_a = -40 ~ +85°C

V_{DD} = 1.8V ±0.1V

Parameter	Symbol	Min	Typ	Max	Unit	Notes
Test clock (TCK) cycle time	t_{THTH}	50	-	-	ns	
TCK high pulse width	t_{THTL}	20	-	-	ns	
TCK low pulse width	t_{TLTH}	20	-	-	ns	
Test mode select (TMS) setup	t_{MVTH}	5	-	-	ns	
TMS hold	t_{THMX}	5	-	-	ns	
Capture setup	t_{CS}	5	-	-	ns	1
Capture hold	t_{CH}	5	-	-	ns	1
TDI valid to TCK high	t_{DVTH}	5	-	-	ns	
TCK high to TDI invalid	t_{THDX}	5	-	-	ns	
TCK low to TDO unknown	t_{TLQX}	0	-	-	ns	
TCK low to TDO valid	t_{TLQV}	-	-	10	ns	

Note 1. t_{CS} + t_{CH} defines the minimum pause in RAM I/O pad transitions to assure pad data capture.

TAP Controller Timing Diagram



Test Access Port Registers

Register name	Length	Symbol	Notes
Instruction register	3 bits	IR [2:0]	
Bypass register	1 bit	BP	
ID register	32 bits	ID [31:0]	
Boundary scan register	109 bits	BS [109:1]	

TAP Controller Instruction Set

IR2	IR1	IR0	Instruction	Description	Notes
0	0	0	EXTEST	The EXTEST instruction allows circuitry external to the component package to be tested. Boundary scan register cells at output balls are used to apply test vectors, while those at input balls capture test results. Typically, the first test vector to be applied using the EXTEST instruction will be shifted into the boundary scan register using the PRELOAD instruction. Thus, during the Update-IR state of EXTEST, the output driver is turned on and the PRELOAD data is driven onto the output balls.	1, 2, 3, 5
0	0	1	IDCODE	The IDCODE instruction causes the ID ROM to be loaded into the ID register when the controller is in capture-DR mode and places the ID register between the TDI and TDO balls in shift-DR mode. The IDCODE instruction is the default instruction loaded in at power up and any time the controller is placed in the Test-Logic-Reset state.	
0	1	0	SAMPLE-Z	If the SAMPLE-Z instruction is loaded in the instruction register, all RAM outputs are forced to an inactive drive state (High-Z), moving the TAP controller into the capture-DR state loads the data in the RAMs input into the boundary scan register, and the boundary scan register is connected between TDI and TDO when the TAP controller is moved to the shift-DR state.	3, 4, 5
0	1	1	RESERVED	The RESERVED instructions are not implemented but are reserved for future use. Do not use these instructions.	
1	0	0	SAMPLE (/PRELOAD)	When the SAMPLE instruction is loaded in the instruction register, moving the TAP controller into the capture-DR state loads the data in the RAMs input and I/O buffers into the boundary scan register. Because the RAM clock(s) are independent from the TAP clock (TCK) it is possible for the TAP to attempt to capture the I/O ring contents while the input buffers are in transition (i.e., in a metastable state). Although allowing the TAP to SAMPLE metastable input will not harm the device, repeatable results cannot be expected. Moving the controller to shift-DR state then places the boundary scan register between the TDI and TDO balls.	3, 5
1	0	1	RESERVED	-	
1	1	0	RESERVED	-	
1	1	1	BYPASS	The BYPASS instruction is loaded in the instruction register when the bypass register is placed between TDI and TDO. This occurs when the TAP controller is moved to the shift-DR state. This allows the board level scan path to be shortened to facilitate testing of other devices in the scan path.	

Notes 1. Data in output register is not guaranteed if EXTEST instruction is loaded.

2. After performing EXTEST, power-up conditions are required in order to return part to normal operation.

3. RAM input signals must be stabilized for long enough to meet the TAPs input data capture setup plus hold time (t_{CS} plus t_{CH}). The RAMs clock inputs need not be paused for any other TAP operation except capturing the I/O ring contents into the boundary scan register.

4. Clock recovery initialization cycles are required after boundary scan.

5. For R1QD and R1QE series, ODT is disabled in EXTEST, SAMPLE-Z or SAMPLE mode.

Boundary Scan Order

Bit #	Ball ID	Signal names	
		x18	x36
1	6R	NC	NC
2	6P	QVLD	QVLD
3	6N	SA	SA
4	7P	SA	SA
5	7N	SA	SA
6	7R	SA	SA
7	8R	SA	SA
8	8P	SA	SA
9	9R	SA	SA
10	11P	DQ0	DQ0
11	10P	NC	DQ9
12	10N	NC	NC
13	9P	NC	NC
14	10M	DQ1	DQ11
15	11N	NC	DQ10
16	9M	NC	NC
17	9N	NC	NC
18	11L	DQ2	DQ2
19	11M	NC	DQ1
20	9L	NC	NC
21	10L	NC	NC
22	11K	DQ3	DQ3
23	10K	NC	DQ12
24	9J	NC	NC
25	9K	NC	NC
26	10J	DQ4	DQ13
27	11J	NC	DQ4
28	11H	ZQ	ZQ
29	10G	NC	NC
30	9G	NC	NC
31	11F	DQ5	DQ5
32	11G	NC	DQ14
33	9F	NC	NC
34	10F	NC	NC
35	11E	DQ6	DQ6

Bit #	Ball ID	Signal names	
		x18	x36
36	10E	NC	DQ15
37	10D	NC	NC
38	9E	NC	NC
39	10C	DQ7	DQ17
40	11D	NC	DQ16
41	9C	NC	NC
42	9D	NC	NC
43	11B	DQ8	DQ8
44	11C	NC	DQ7
45	9B	NC	NC
46	10B	NC	NC
47	11A	CQ	CQ
48	10A	SA	SA
49	9A	SA	SA
50	8B	SA	SA
51	7C	SA	SA
52	6C	NC	NC
53	8A	/LD	/LD
54	7A	NC	/BW1
55	7B	/BW0	/BW0
56	6B	K	K
57	6A	/K	/K
58	5B	NC	/BW3
59	5A	/BW1	/BW2
60	4A	R-/W	R-/W
61	5C	SA	SA
62	4B	SA	SA
63	3A	SA	SA
64	2A	SA	NC
65	1A	/CQ	/CQ
66	2B	DQ9	DQ27
67	3B	NC	DQ18
68	1C	NC	NC
69	1B	NC	NC
70	3D	DQ10	DQ19

Bit #	Ball ID	Signal names	
		x18	x36
71	3C	NC	DQ28
72	1D	NC	NC
73	2C	NC	NC
74	3E	DQ11	DQ20
75	2D	NC	DQ29
76	2E	NC	NC
77	1E	NC	NC
78	2F	DQ12	DQ30
79	3F	NC	DQ21
80	1G	NC	NC
81	1F	NC	NC
82	3G	DQ13	DQ22
83	2G	NC	DQ31
84	1H	/DOFF	/DOFF
85	1J	NC	NC
86	2J	NC	NC
87	3K	DQ14	DQ23
88	3J	NC	DQ32
89	2K	NC	NC
90	1K	NC	NC
91	2L	DQ15	DQ33
92	3L	NC	DQ24
93	1M	NC	NC
94	1L	NC	NC
95	3N	DQ16	DQ25
96	3M	NC	DQ34
97	1N	NC	NC
98	2M	NC	NC
99	3P	DQ17	DQ26
100	2N	NC	DQ35
101	2P	NC	NC
102	1P	NC	NC
103	3R	SA	SA
104	4R	SA	SA
105	4P	SA	SA
106	5P	SA	SA
107	5N	SA	SA
108	5R	SA	SA
109	-	Internal	Internal

Notes In boundary scan mode,

1. Clock balls (K, /K, C, /C) are referenced to each other and must be at opposite logic levels for reliable operation.
2. CQ and /CQ data are synchronized to the respective C and /C (except EXTEST, SAMPLE-Z).
3. If C and /C tied high, CQ is generated with respect to K and /CQ is generated with respect to /K (except EXTEST, SAMPLE-Z).

ID Register

-	Revision number (31 :29)			Type number (28 : 12)																	Vendor JEDEC code (11 : 1)											Start bit (0)
#	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Symbol	R	R	R	0	C	M	M	M	A	W	W	0	1	Q	Q	Q	B	O	S	0	0	1	0	0	0	1	0	0	0	1	1	1

R	R	R	
0	0	0	Revison 0
0	0	1	Revison 1
0	1	0	Revison 2
0	1	1	Revison 3
:			:

C	
0	36M&72M w/o ODT, 144M,288M
1	36M&72M w/ ODT

M	M	M	
0	1	0	Density = 36Mb
0	1	1	Density = 72Mb
1	0	1	Density = 144Mb
1	1	0	Density = 288Mb

A	
0	144M&288M w/o ODT, 36M,72M
1	144M&288M w/ ODT

W	W	
0	0	x9
1	0	x18
1	1	x36

Q	
0	II (QDR-II, DDR-II)
1	II+ (QDR-II+, DDR-II+)

Q	
0	DDR
1	QDR

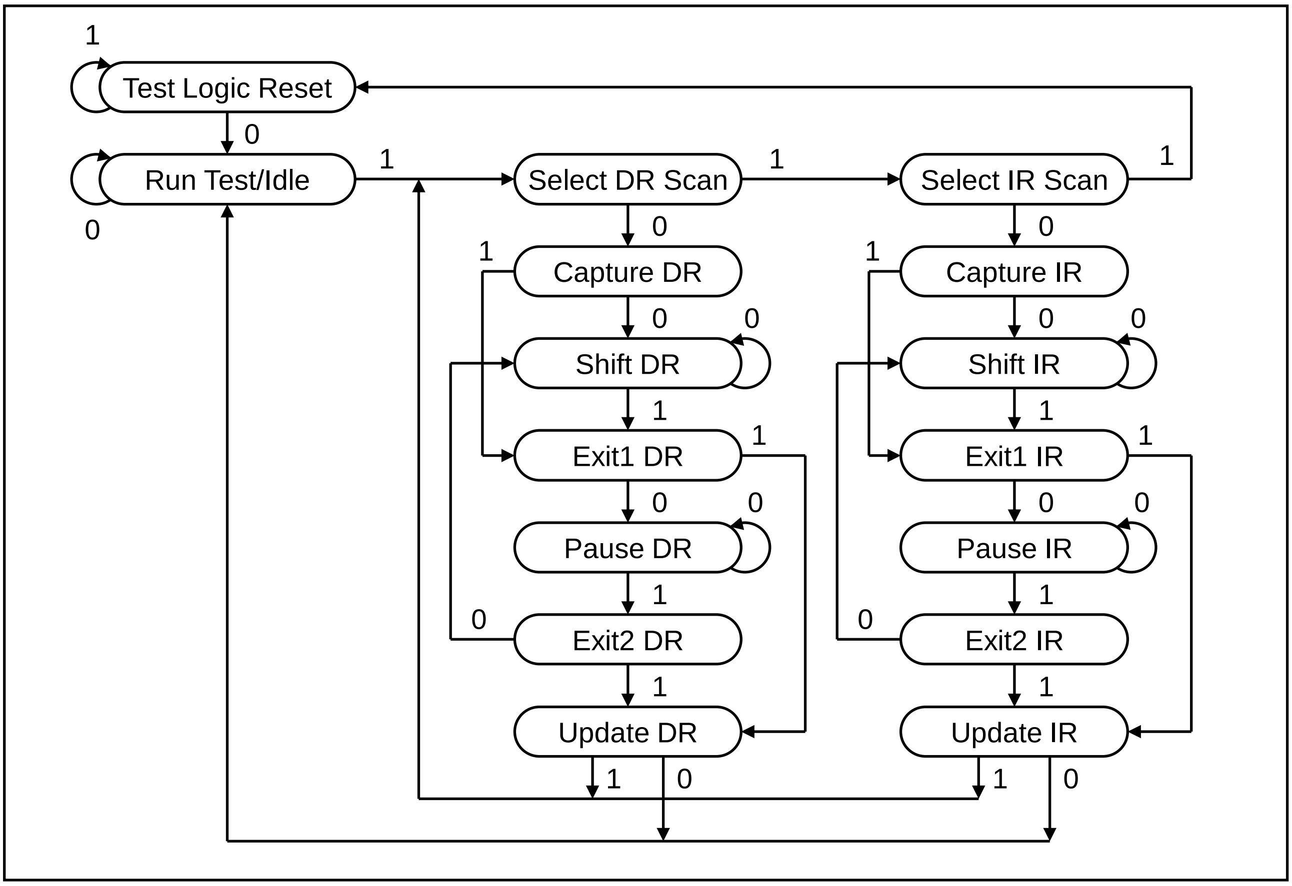
Q	
0	Latency=1.5 (@II), Latency=2.0 (@II+)
1	Latency=2.5 (@II+)

B	
0	Burst Length = 2 word burst
1	Burst Length = 4 word burst

O	
0	without ODT
1	with ODT

S	
0	Common I/O
1	Separate I/O

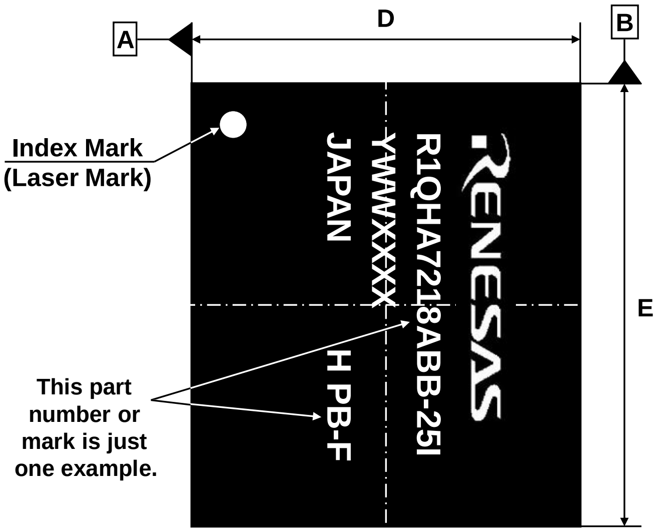
TAP Controller State Diagram



Note 1. The value adjacent to each state transition in this figure represents the signal present at TMS at the time of a rising edge at TCK. No matter what the original state of the controller, it will enter Test-Logic-Reset when TMS is held high for at least five rising edges of TCK.

Package Dimensions and Marking Information

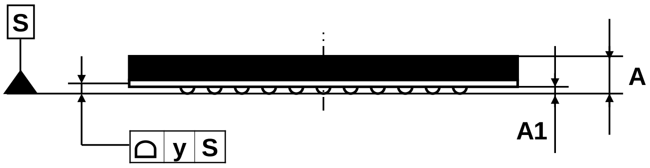
JEITA Package Code	Renesas Code	Previous Code	Mass (typ.)
P-LBGA165-13x15-1.00	PLBG0165FE-A	165FHG	0.5g



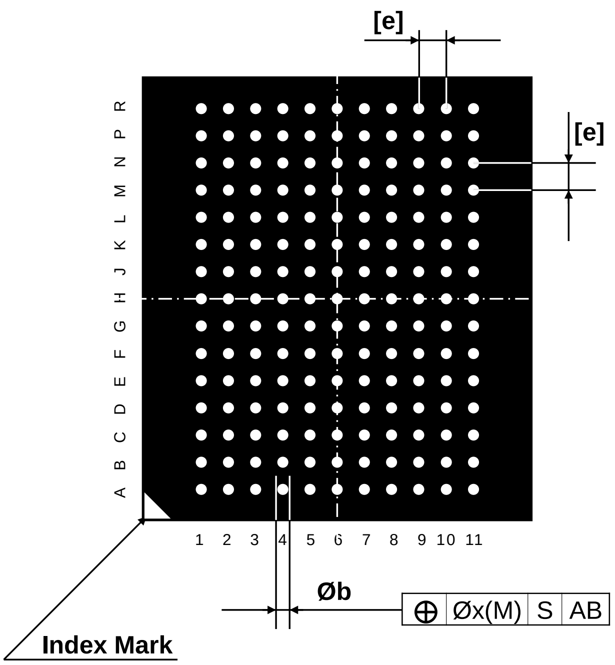
Top View

Marking Information

- 1st row : Vender name (RENESAS)
- 2nd row: Part number
- 3rd row : Y : Year code
  - WW : Week code
  - XXXX : Renesas internal use
- 4th row : Country name (JAPAN)
  - + "H" --- Non-Halogeneted
  - + "PB-F" --- Pb-free parts



Side View



Bottom View

Reference Symbol	Dimension in mm		
	Min	Nom	Max
D	12.9	13.0	13.1
E	14.9	15.0	15.1
A	-	-	1.4
A1	0.31	0.36	0.41
[e]	-	1.0	-
b	0.45	0.5	0.6
x	-	-	0.2
y	-	-	0.15

Revision History	R1QHA7236ABB, R1QHA7218ABB

Rev.	Date	Description	
		Page	Summary
1.00	-	-	Applied new document format.
2.00	’17.05.15	-	Reflected the information related change to non-halogenated package and merger some speed bin.
2.01	’17.06.09	-	Fixed some typo.
2.02	’17.08.29	P.16 P.34	Fixed K Truth Table Fixed Boundary Scan Order Table
2.03	’19.02.01	-	Deleted description other than current Renesas 72M QDR Lineup. Fixed some typo and orthographical variants.

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