RAA211250

4.5V to 30V, 5A, DC/DC Synchronous Step-Down Regulator w/ Internal Compensation and Adjustable Frequency

The RAA211250 is a DC/DC synchronous step-down (Buck) regulator that supports a 4.5V to 30V input voltage range and adjustable output voltage. It can deliver up to continuous 5A of continuous output current with premium load and line regulation performance.

The RAA211250 uses peak-current mode control architecture. Its PWM switching frequency is programmable to provide the best trade-off between transient response and efficiency. It also supports PFM operation and DEM to maximize light load efficiency, in addition to an external bias LDO input to further reduce power dissipation across the load range. The regulator also has an internal loop compensation circuit to reduce the external component count and BOM cost.

The RAA211250 provides useful functions such as internal or programmable soft-start and power good indicator. For safe operation, the RAA211250 also offers protection features such as cycle-by-cycle peak and valley current limit, input voltage UVLO, output voltage undervoltage (short-circuit) protection, and thermal shutdown.

Applications

- Industrial power systems
- Distributed power supplies and general-purpose point-of-load
- Telecommunication base station power supplies
- High-voltage single-board systems

Features

- Wide input voltage range: 4.5V to 30V
- Adjustable output voltage: 0.8V to 90% of VIN (limited by minimum off time)
- Up to 5A of continuous output current
- Default 400kHz switching frequency and programmable switching frequency range from 200kHz to 800kHz
- ±1% Load regulation accuracy from -40°C to 125°C, ±0.5% Load regulation accuracy at 25°C
- 95µA typical quiescent current
- Internal compensation
- Internal 0.5ms soft-start in QFN
- External programmable soft-start (HTSSOP)
- PFM operation and DEM at light load
- Integrated external bias LDO
- Power-good indicator
- Integrated MOSFET $r_{DS(ON)}$ (typical): 70mΩ/25mΩ (QFN); 115mΩ/40mΩ (TSSOP)
- Cycle-by-cycle peak and valley current limit
- Input voltage UVLO and output voltage undervoltage (short-circuit) protection
- Thermal Shutdown
- Available in 20 Ld QFN 4mm × 3.5mm and 16 Ld HTSSOP packages

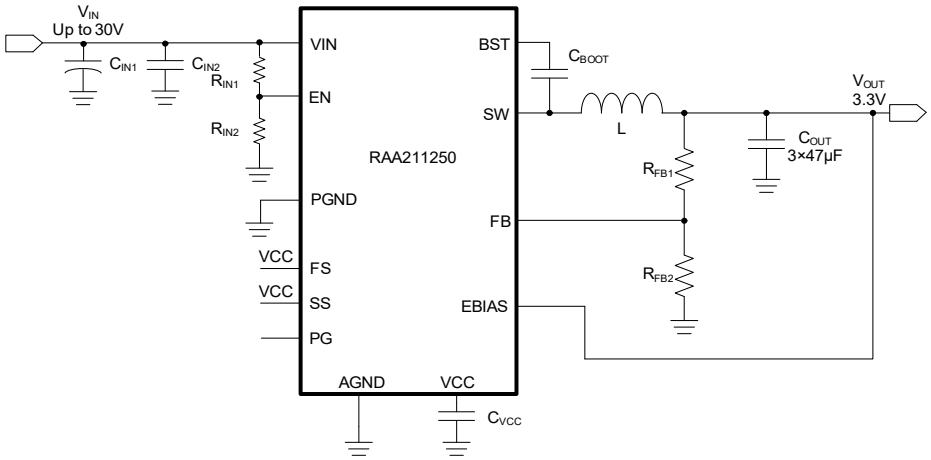


Figure 1. Typical Application Circuit

Contents

1. Overview

1.1 Block Diagram

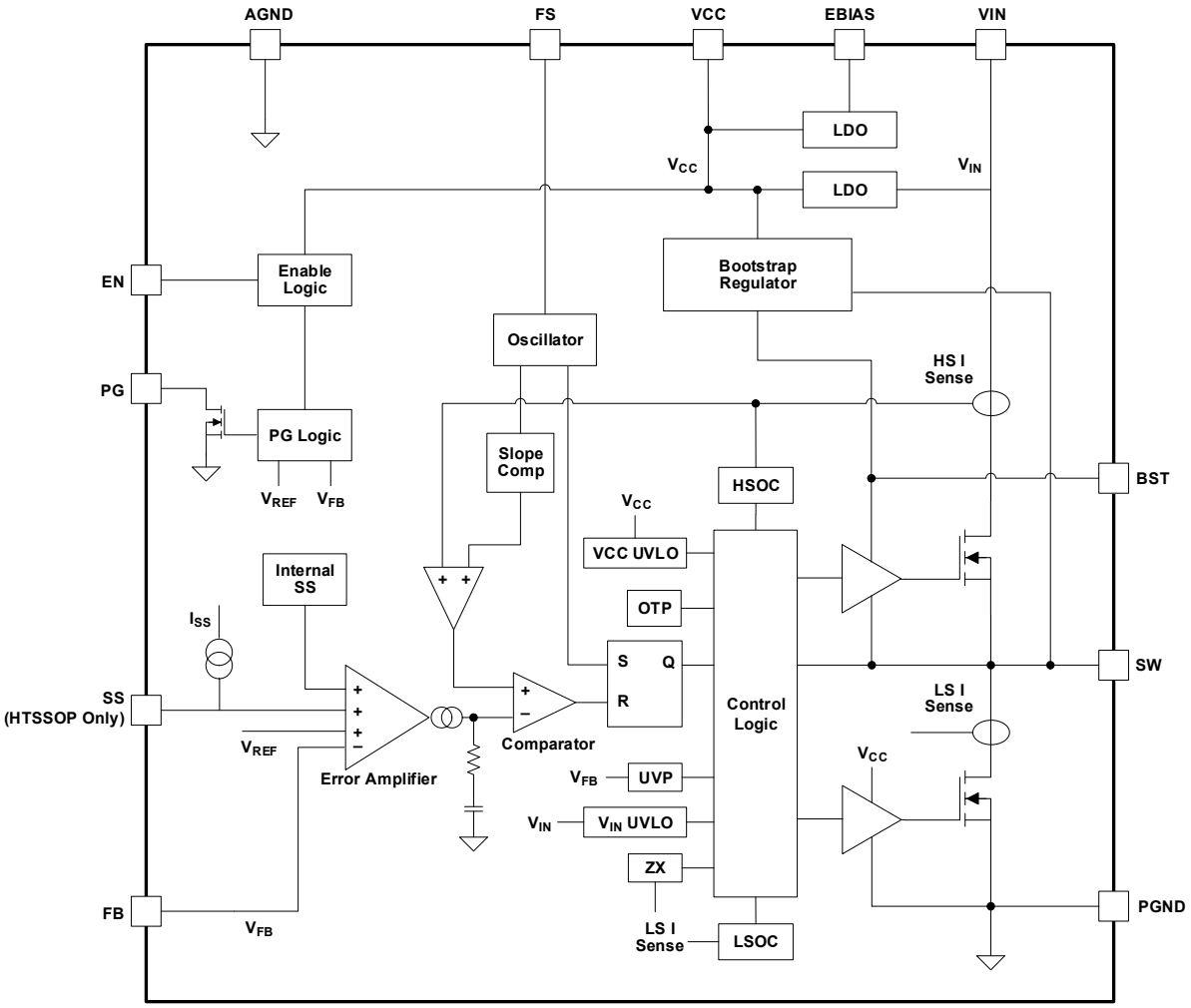
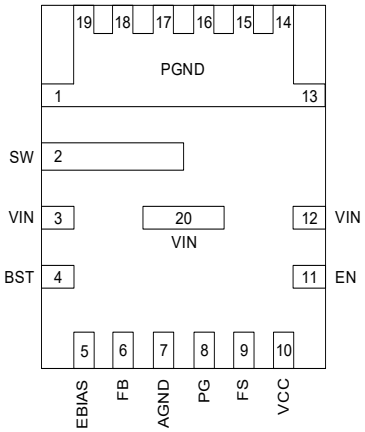


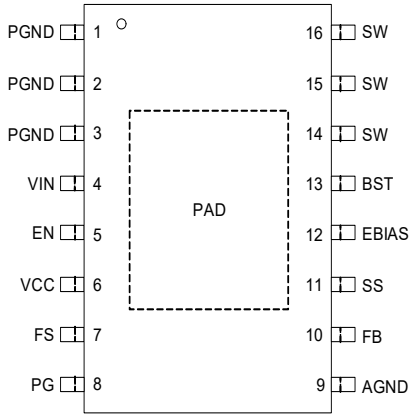
Figure 2. Functional Block Diagram

2. Pin Information

2.1 Pin Assignments



20 Ld QFN
Top View



16 Ld HTSSOP
Top View

2.2 Pin Descriptions

Pin #		Pin Name	Description
QFN	HTSSOP		
1, 13, 14, 15, 16, 17, 18, 19	1, 2, 3	PGND	These pins are connected to the source of the integrated low-side FET and are used as the power ground. Place input bypass capacitors as close as possible to the PGND pins and VIN pin(s).
2	14, 15, 16	SW	These pins are the phase node of the regulator. They are connected to the source of the high-side FET and the drain of the low-side FET. Connect these pins to the inductor and the boot capacitor.
3, 12, 20	4	VIN	This pin is connected to the drain of the integrated high-side FET. This pin is also connected to the input of internal linear regulator that provides bias for the IC. Connect this pin to the input rail and decouple to PGND with input bypass capacitors.
4	13	BST	This pin is the bootstrap circuit supply pin. Connect this pin to SW with a capacitor to provide bias voltage for the integrated high-side FET gate driver.
5	12	EBIAS	This pin is connected to the auxiliary internal linear regulator. This pin can be connected to the output of the regulator to provide bias for the IC.
N/A	11	SS	This pin configures the soft-start time. Connect a capacitor from this pin to ground to program the soft-start time. Tie this pin to VCC for default 0.5ms soft-start time.
6	10	FB	This pin is connected to the inverting input of the feedback error amplifier and should be connected to a properly selected resistor divider from VOUT to ground to set the output voltage.
7	9	AGND	This pin is connected to the analog ground of the IC. Connect this pin to the PCB ground plane.
8	8	PG	This pin is an open-drain power-good output. It can be pulled up with a resistor to VCC or another rail. The recommended pull-up voltage is 3.3V or lower.
9	7	FS	This pin sets the switching frequency. Connect a resistor from this pin to ground to set the switching frequency from 200kHz to 800kHz. Connect this pin to VCC for default 400kHz switching frequency.

10	6	VCC	This pin is connected to the output of internal linear regulators and provides bias for the IC including the gate driver. Connect this pin to ground with a ceramic decoupling capacitor.
11	5	EN	This pin is the enable pin. It is high voltage tolerant and can be directly connected to VIN. When using EN to turn the device on or off, connect this pin to GND with a 1MΩ resistor.
N/A	-	PAD	This is the bottom thermal pad. It should be connected to AGND and to the PCB ground plane with thermal vias.

2.3 Recommended Components Values for Typical Applications

f_{SW} (kHz)	V_{OUT} (V)	R_{FB1} (kΩ)	R_{FB2} (kΩ)	L (µH)	C_{OUT}
400	0.8	0	20	1.0	5 × 100µF/1210/6.3V/X7S
	1.8	24.9	20	2.2	2 × 100µF/1210/6.3V/X7S + 1 × 47µF/1210/6.3V/X7R
	3.3	61.9	20	3.3	3 × 47µF/1210/10V/X7R
	5	105	20	4.7	2 × 47µF/1210/16V/X7R
	12	280	20	10	2 × 22µF/1210/50V/X7R
	24	576	20	22	2 × 10µF/1210/50V/X7R
600	0.8	0	20	0.56	3 × 100µF/1210/6.3V/X7S
	1.8	24.9	20	1.0	1 × 100µF/1210/6.3V/X7S + 1 × 47µF/1210/6.6V/X7R
	3.3	61.9	20	2.2	2 × 47µF/1210/10V/X7R
	5	105	20	3.3	1 × 47µF/1210/16V/X7R + 1 × 10µF/1210/16V/X7R
	12	280	20	6.8	1 × 22µF/1210/50V/X7R
	24	576	20	10	1 × 10µF/1210/50V/X7R
800	0.8	0	20	0.47	2 × 100µF/1210/6.3V/X7S + 1 × 47µF/1210/6.3V/X7R
	1.8	24.9	20	1.0	1 × 100µF/1210/6.3V/X7S + 1 × 22µF/1210/6.3V/X7R
	3.3	61.9	20	1.5	1 × 47µF/1210/10V/X7R + 1 × 22µF/1210/10V/X7R
	5	105	20	2.2	1 × 47µF/1210/16V/X7R
	12	280	20	4.7	1 × 22µF/1210/50V/X7R
	24	576	20	6.8	1 × 10µF/1210/50V/X7R

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN	-0.3	35	V
EBIAS	-0.3	35	V
EN	-0.3	35	V
SW	-0.7	V_{IN}+0.3	V
SW Transient	-3 (for 15ns)	V_{IN}+2	V
BST	-0.7	SW+4	V
BST to SW	-0.3	4	V
All other pins	-0.3	4	V
Operating junction temperature	–40	150	°C
Storage temperature range	–65	150	°C

3.2 ESD Ratings

ESD Model/Test	Rating	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Package Type	Thermal Resistance (Typical)		
	θ_{JA} (°C/W)[1]	$\theta_{JA(EVB)}$ (°C/W)[2]	θ_{JC} (°C/W)[3]
QFN Package	48.3	27.3	6.0
HTSSOP Package	35.0	20.1	3.0

1. θ_{JA} is measured in free air with the component mounted on a JEDEC std. high-effective thermal conductivity test board with direct attach features, including:
   • For the QFN, 3 thermal vias under the bottom PGND area of the QFN.
   • For the HTSSOP, 9 thermal vias under the bottom EPAD of the HTSSOP.
   Note: See TB379 for general thermal metric information.
2. $\theta_{JA(EVB)}$ is measured in free air with the component mounted on a 4-layer PCB (2oz Cu outer layers and 1 oz Cu inner layers) evaluation board.
3. For θ_{JC}:
   • For the QFN, the case temperature is taken on the pin #2 SW EPAD strip near the center of the package underside.
   • For the HTSSOP, the case temperature is taken at the center of the exposed metal pad on the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature		+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	see TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage (V_{IN})	4.5	30	V
Output Voltage (V_{OUT})	0.8	90% of V_{IN}	V
EBIAS Operating Voltage (EBIAS)	3.3	30	V
Output Current (I_{OUT})	0	5	A
Junction Temperature (T_J)	-40	125	°C

3.5 Electrical Specifications

Typical Values are at T_A = +25°C, V_{IN} = 24V unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C.

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
V_{IN} Supply						
Input Voltage Range	V_{IN}		4.5		30	V
Shutdown Current				1		µA
Quiescent Current	I_q	EN = 2V, VFB = 0.825V, VIN = 24V, EBIAS = 3.3V, No Switching		90	200	µA
V_{IN} UVLO/EN						
V_{IN} UVLO Rising Threshold			3.9	4.25	4.5	V
V_{IN} UVLO Falling Hysteresis				325		mV
EN Rising Threshold			1.125	1.3	1.375	V
EN Falling Hysteresis				170		mV
EN Deglitch Filter				2.5		µs
Feedback Voltage Reference						
Feedback Voltage Reference	V_{FB}	25°C	0.796	0.8	0.804	V
		-40°C to 125°C	0.792	0.8	0.808	V
Integrated MOSFETs (QFN)						
High-Side FET On-Resistance	R_{DS_onh}			70		mΩ
Low-Side FET On-Resistance	R_{DS_onl}			25		mΩ

Typical Values are at T_A = +25°C, V_{IN} = 24V unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Integrated MOSFETs (HTSSOP)						
High-Side FET On-Resistance	R_{DS_onh}			115		mΩ
Low-Side FET On-Resistance	R_{DS_onl}			40		mΩ
Soft-Start						
Internal Soft-Start Time	t_{SS}			0.5		ms
Soft-Start Charge Current	I_{SS}		3.75	5.3	6.5	µA
Soft-Start Pull-Down Resistance	R_{SS}			1		kΩ
Soft-Start Done Threshold				1.2		V
Oscillator/PWM Comparator						
Switching Frequency	f_{SW}	V_{FB} = 0.8 V, FS = V_{CC}	360	400	440	kHz
Minimum On-Time	t_{ON_MIN}			96		ns
Minimum Off-Time	t_{OFF_MIN}				220	ns
Switching Frequency Range			200		800	kHz
Overcurrent Protection (OCP)/V_{OUT} Undervoltage Protection (UVP)						
Peak Current Limit Threshold	I_{HSOC}		7.0	8.5	9.5	A
Low-Side Current Limit Threshold	I_{LSOC}		5	6		A
VFB Undervoltage Threshold				0.4		V
Foldback Frequency		V_{FB} = 0V		50		kHz
Hiccup Time	t_{HICCUP}			23		ms
Thermal Shutdown (OTP)						
Thermal Shutdown Threshold				155		°C
Thermal Shutdown Recovery Hysteresis				20		°C
Power Good						
PG Overvoltage Threshold		% of FB Rising	109	112	115	%
PG Undervoltage Threshold		% of FB Falling	85	88	91	%
Hysteresis		% of FB		3		%
Deglitch Filter		Rising and Falling Edges		4		µs

Typical Values are at T_A = +25°C, V_{IN} = 24V unless otherwise noted. Min and Max values apply across the junction temperature range, -40°C to +125°C. (Cont.)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Pull-Down Resistance				65		Ω
V_{CC}/EBIAS						
V_{CC} Voltage			3.1	3.3	3.5	V
VCC Output Current Limit				50		mA
VCC UVLO Rising Threshold			2.75	3	3.15	V
VCC UVLO Falling Hysteresis				280		mV
EBIAS Operating Voltage			3.3		30	V
EBIAS Switchover Rising Threshold				3.0		V
EBIAS Switchover Falling Hysteresis				200		mV

4. Typical Performance Curves

Waveforms and curves were measured on RTKA211250E00000BU or RTKA211250E00010BU, unless otherwise noted.

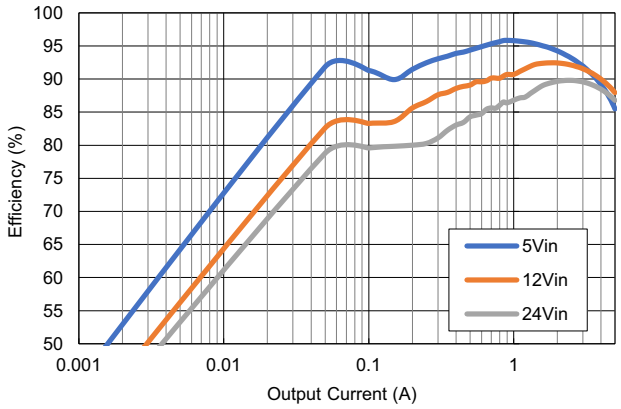


Figure 3. Efficiency vs Load, 3.3V V_{OUT}, 400kHz, QFN

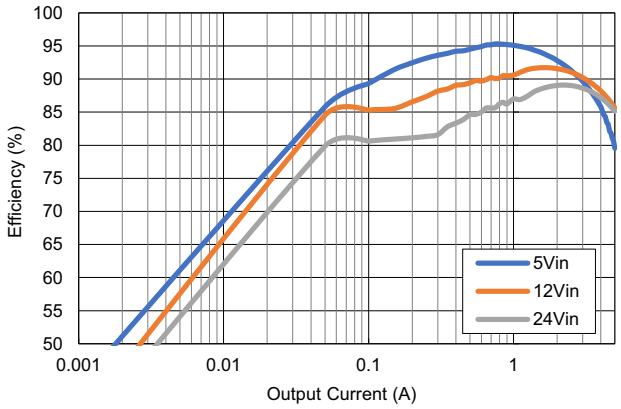


Figure 4. Efficiency vs Load, 3.3V V_{OUT}, 400kHz, HTSSOP

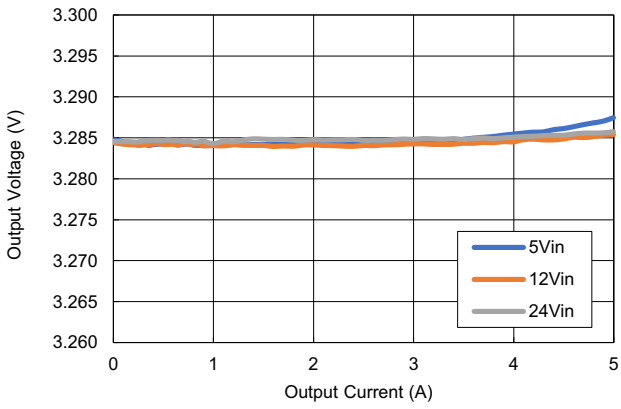


Figure 5. Load Regulation, 3.3V V_{OUT}, 400kHz, QFN

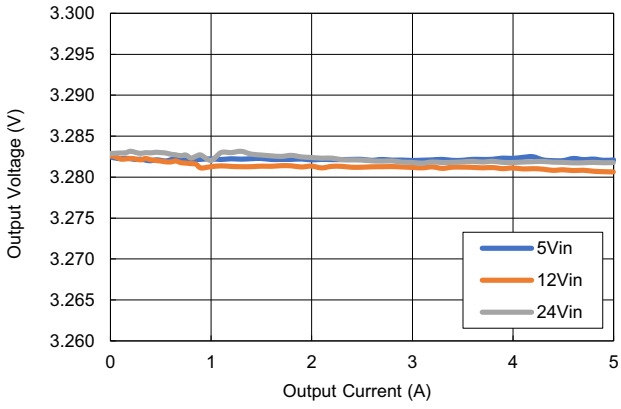


Figure 6. Load Regulation, 3.3V V_{OUT}, 400kHz, HTSSOP

Waveforms and curves were measured on RTKA211250E00000BU or RTKA211250E00010BU, unless otherwise noted. (Cont.)

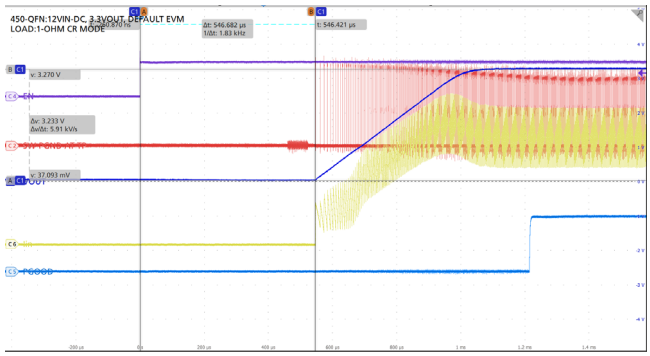


Figure 7. EN Start-Up, 12V_{IN}, 3.3V V_{OUT}, 400kHz, 1.0Ω Load, QFN

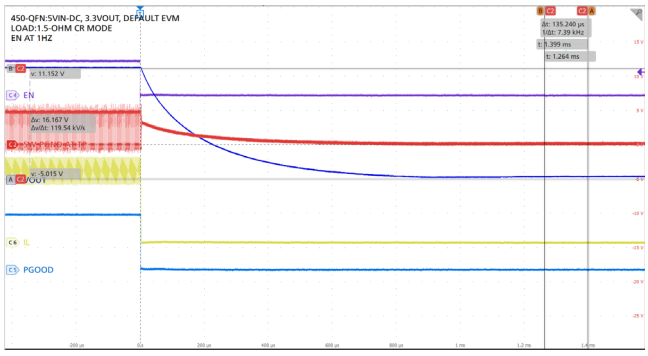


Figure 8. EN Shutdown, 5V_{IN}, 3.3V V_{OUT}, 400kHz, 1.5Ω Load, QFN

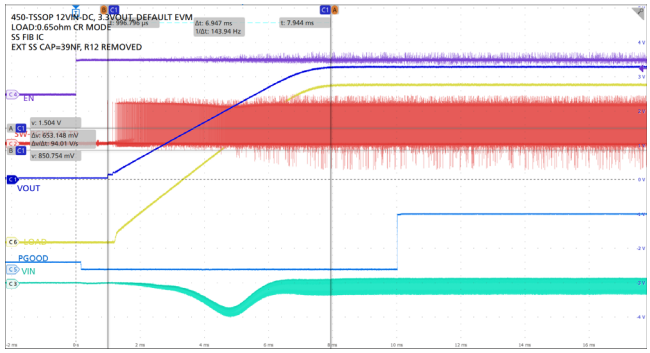


Figure 9. External SS, 12V_{IN}, 3.3V_{OUT}, 0.65Ω Load, C_{SS} = 39nF, HTSSOP

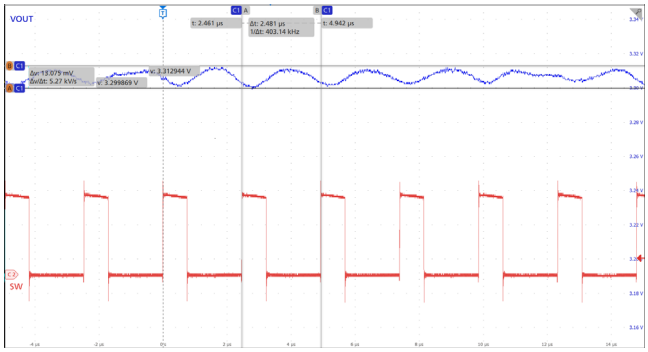


Figure 10. Steady State, 3.3V V_{OUT}, Full Load, 400kHz, QFN

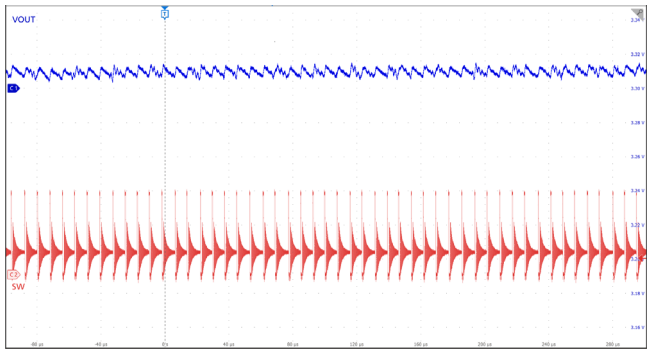


Figure 11. Steady State, 3.3V V_{OUT}, No Load, 400kHz, QFN

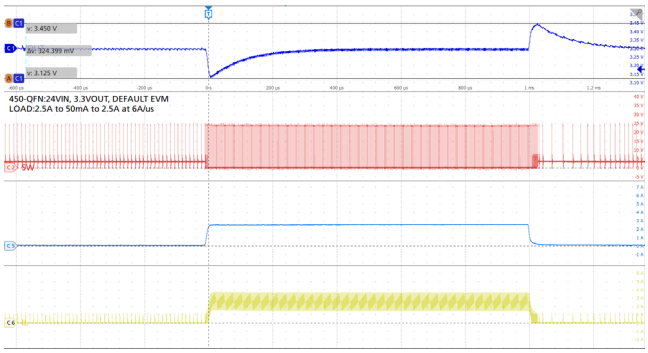


Figure 12. Load Transient, 24V_{IN}, 3.3V_{OUT}, 400kHz, 50mA to 2.5A, QFN

Waveforms and curves were measured on RTKA211250E00000BU or RTKA211250E00010BU, unless otherwise noted. (Cont.)

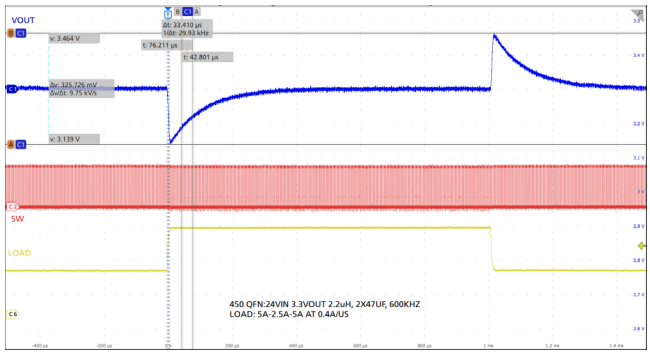


Figure 13. Load Transient, 24V_{IN}, 3.3V_{OUT}, 600kHz, 2.5A to 5A, QFN

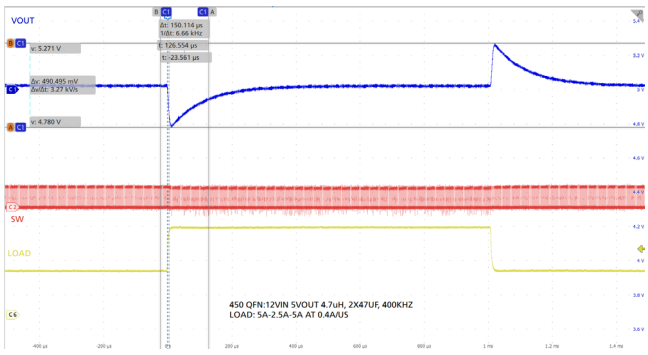


Figure 14. Load Transient, 12V_{IN}, 5V_{OUT}, 400kHz, 2.5A to 5A, QFN

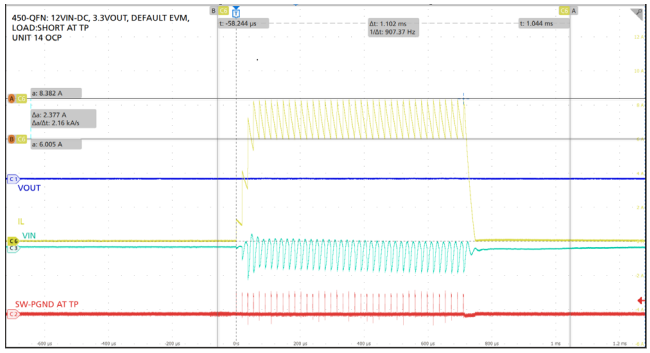


Figure 15. Output Voltage Short Protection, 12V_{IN}, 3.3V_{OUT}, QFN

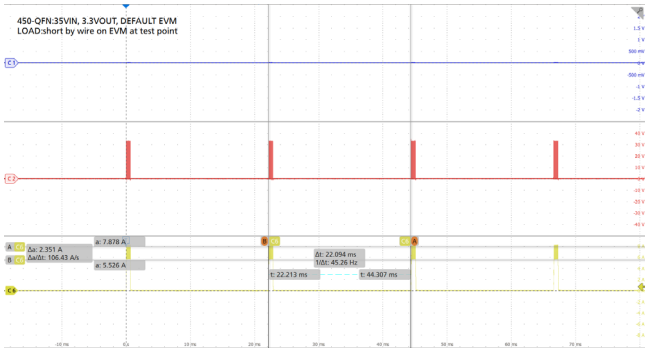


Figure 16. Output Short Protection with Hiccup, QFN

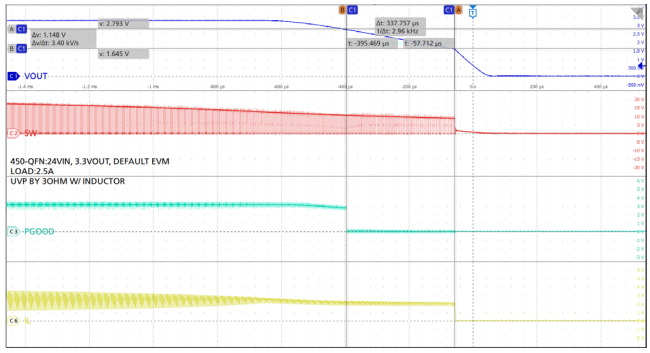


Figure 17. Undervoltage Protection, 12V_{IN}, 3.3V_{OUT}, QFN

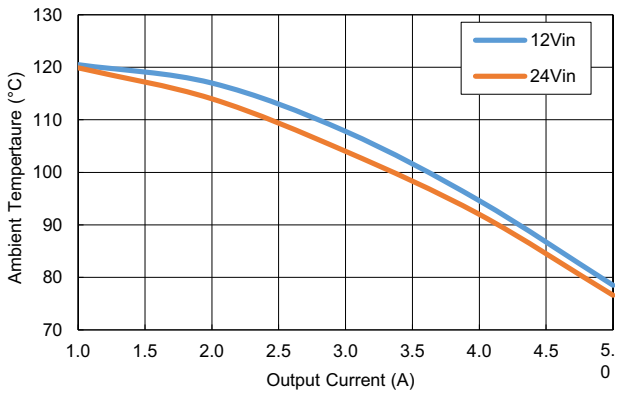


Figure 18. Safe Operating Area: 3.3Vout, 400kHz, QFN, Default EVM

Waveforms and curves were measured on RTKA211250E00000BU or RTKA211250E00010BU, unless otherwise noted. (Cont.)

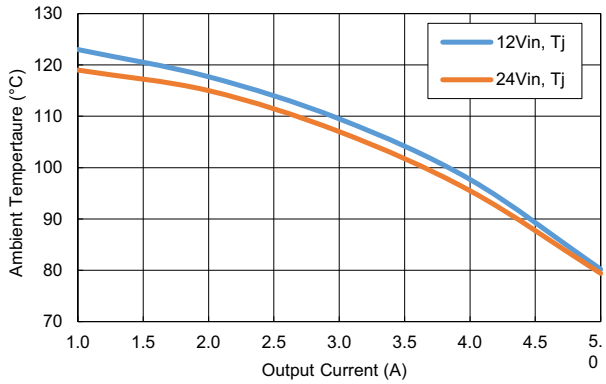


Figure 19. Safe Operating Area: 3.3Vout, 400kHz, HTSSOP, Default EVM

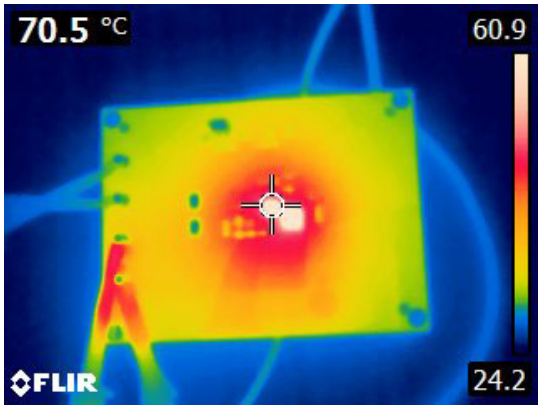


Figure 20. Thermal Image, $12V_{IN}$, $3.3V_{OUT}$, 400kHz, 5A, QFN, T_J = 70.5°C

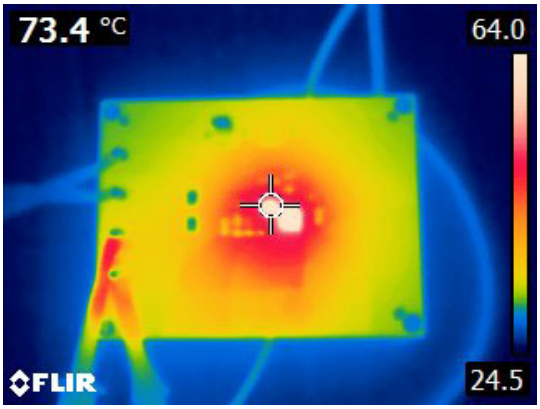


Figure 21. Thermal Image, $24V_{IN}$, $3.3V_{OUT}$, 400kHz, 5A, QFN, T_J = 73.4°C

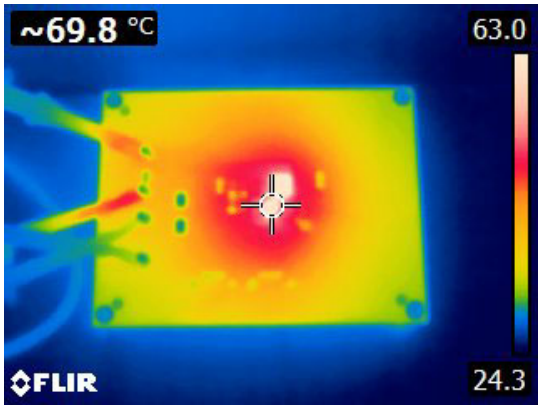


Figure 22. Thermal Image, $12V_{IN}$, $3.3V_{OUT}$, 400kHz, 5A, HTSSOP, T_J = 69.8°C

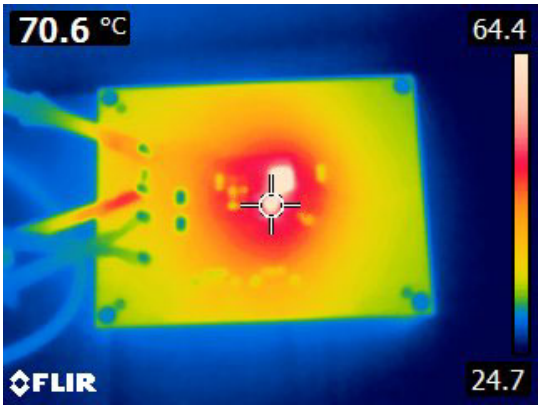


Figure 23. Thermal Image, $24V_{IN}$, $3.3V_{OUT}$, 400kHz, 5A, HTSSOP, T_J = 70.6°C

5. Functional Description

The control architecture is based on peak current mode control. The output voltage is sensed by a resistor divider from the output of the converter to the FB pin. An internal transconductance error amplifier (EA) compares the FB voltage with an internal 0.8V reference voltage and produces an amplified compensated signal (COMP) to minimize the error in V_{OUT}. The EA has internal compensation that provides stable operation across operating conditions and switching frequency range. The COMP signal is compared with the sum of sensed high-side current and the slope compensation value.

5.1 Fixed Frequency Operation Mode

In the continuous conduction mode (CCM) operation where the load current is higher one-half of inductor peak-to-peak inductor current, the RAA211250 operates at a programmed fixed frequency. At the rising edge of the PWM clock, the high-side FET turns on and the inductor current ramps up at a slew rate determined by the inductor value, input voltage, and output voltage. The high-side FET is switched off when the sum of the sampled high-side FET current and slope compensation reaches the COMP signal level or when either the maximum duty cycle or high-side overcurrent is reached. *Note:* The high-side FET must stay on for at least 96ns as the minimum on-time expires.

When the high-side FET is turned off, the low-side FET turns on after a small amount of dead time. The dead time between the two MOSFETs prevents shoot-through. When the low-side FET is turned on for the remainder of period, the inductor current ramps down at a rate determined by the output voltage and inductor value. *Note:* The low-side FET must stay on for at least 220ns as the minimum off-time expires.

5.2 Discontinuous Operation Mode

To improve efficiency at light load, RAA211250 allows operation with the switching frequency lower than programmed frequency. The switching frequency is varied and depends on the output load. RAA211250 enters the discontinuous conduction mode (DCM) when the output load is less than one-half of the peak-to-peak ripple current of the inductor. In this mode, the COMP signal value is lower than the preset DCM value. Also, the internal oscillator clock is forced to skip pulses and allows reduction of the cycle switching frequency.

When the output load is increasing, the COMP signal rises above the preset DCM value and exits the DCM.

5.3 Soft-Start Timing

Depending on which RAA211250 package you are using, there are two options to configure soft-start timing. The QFN package has a fixed soft-start time of 500µs (typical), which is not adjustable. The HTSSOP package allows soft-start time to be set to an interval longer than 500µs by placing a capacitor from the SS pin to ground. Use Equation 1 to calculate the C_{SS} value. If you want to use 500µs soft-start time with the HTSSOP package, short the SS pin to VCC.

(EQ. 1) $$t_{SS} = C_{SS} \times \frac{V_{REF}}{I_{SS}}$$

5.4 Start-Up Process

When both EN and V_{IN} UVLO meet the thresholds, RAA211250 initiates the start-up process. When the output voltage starts from 0V, RAA211250 uses the SS voltage as the reference voltage for the EA during start-up. The SS voltage starts from 0V and finishes the soft-start when the SS voltage reaches 0.8V. After soft-start, RAA211250 switches to its 0.8V reference voltage for the EA. The SS voltage continues ramping up, and when it reaches 1.2V, it asserts the PG signal.

When pre-bias is present on the output, RAA211250 does not generate any pulses until the SS voltage is greater than the FB voltage.

5.5 BOOT Refresh and Capacitor Selection

Approximately 500µs after EN is driven high and before the start-up process begins, the RAA211250 turns on the low-side FET for 250ns with a 2µs period and repeats this for 32 cycles. This action charges the boot capacitor before the start-up process begins. After the regulator has started up, if it is operating in DCM in a light load condition, the boot refresh circuitry is enabled when the cycle switching frequency is longer than 3.7ms.

A capacitor is needed between the BST pin and SW pin to provide gate voltage for the high-side internal MOSFET. Renesas recommends using a 16V X7R 0.1µF ceramic capacitor as the bootstrap capacitor for most applications.

5.6 Power-Good

The RAA211250 provides a Power-Good (PG) signal to alert the system that the output voltage is within regulation. Power-good logic is functional when VCC voltage is above UVLO.

The PG pin is the open drain of a MOSFET. Renesas recommends connecting it to a voltage source through a pull-up resistor such as 100kΩ. At the start-up, the PG signal is held low before SS is ready, and it is asserted when the SS voltage reaches 1.2V, and FB voltage is within the regulation window. When the FB voltage goes 12% below or 12% above the nominal value, PG is pulled low.

5.7 Switching Frequency Resistor Selection

The default switching frequency of 400kHz is programmed by shorting the FS pin to VCC.

Connect a resistor from the FS pin to AGND to program the switching frequency from 200kHz to 800kHz. See Figure 24 and Table 1 to select a resistor value for a specific frequency.

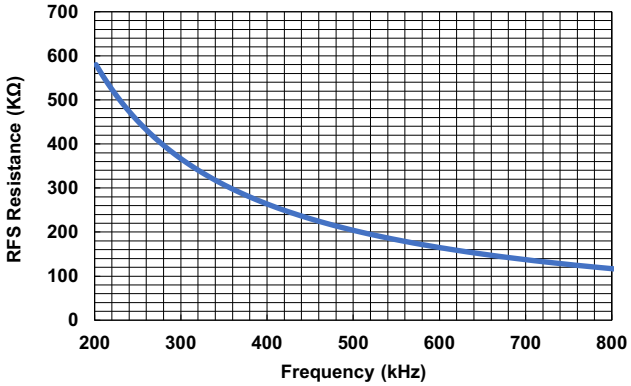


Figure 24. Switching Frequency versus FS Resistance

Table 1. Typical Switching Frequency Resistor Value

Switching Frequency (kHz)	R_{FS}(kΩ)
200	590
300	374
400	261
500	205
600	165
700	140
800	121

5.8 Input Undervoltage Lockout

The input undervoltage lockout level can be set with a resistor divider from VIN to the EN pin to GND based on Equation 2 (see Figure 1) where V_{INR} is the minimum input voltage for the part to turn on..

(EQ. 2) $$R_{IN1} = R_{IN2} \times \frac{V_{INR} - 1.25}{1.25}$$

The resulting input voltage (V_{INF}) for the part to be turned off is calculated using Equation 3 (see Figure 1).

(EQ. 3) $$V_{INF} = 1.125 \times \frac{R_{IN1} + R_{IN2}}{R_{IN2}}$$

5.9 VCC and EBIAS

RAA211250 uses the VCC voltage to bias the IC, charges the boot capacitor, and drives the low-side MOSFET. VCC is an output of two internal LDOs. One LDO is connected to VIN and the other LDO is connected to EBIAS.

The EBIAS pin allows you to connect an external bias source to the IC. The typical usage case is to connect the output voltage rail (VOUT) to EBIAS. Any other voltage source that is in the 3.3V to 30V range can also be used for this purpose. When EBIAS is connected to VOUT, RAA211250 automatically detects and switches over to the VOUT bias source when it is greater than 3.1V. Using the EBIAS pin results in higher efficiency if the external bias voltage level is lower than the input voltage. The EBIAS pin can be grounded if not used.

5.10 Overcurrent Protection (OCP)

RAA211250 detects both high-side and low-side overcurrent using a cycle-by-cycle sensing method. Overcurrent in the high-side FET is detected by sensing the voltage across the FET while it is on. After the high-side FET is on, there is a noise blanking interval before the inductor current is compared to a fixed peak current threshold value of 8.3A. The high-side FET on-time is terminated immediately when the inductor current reaches 8.3A. The low-side FET is switched on to draw down the inductor current. The low-side FET remains on until the valley inductor current falls below a fixed threshold value of 6A. Overcurrent in the low-side FET is detected by sensing the voltage across the FET while it is on. After the low-side FET is on, there is a noise blanking time before the OC comparator is enabled. When the valley inductor current is below 6A, the high-side FET can turn on. Because of this, the cycle switching frequency is lower than programmed switching frequency. The output voltage is reduced during OCP events. When the FB voltage falls to 50% of $0.8V_{REF}$, RAA211250 enters hiccup mode until the excessive load is removed.

For an application that operates near minimum on-time or if there is a hard short on the output, the COMP voltage moves higher to extend the on-time to respond to the lower output voltage. In this case, the high-side OCP dominates. When the output current ramps up gradually and the peak inductor current does not reach 8.3A, the low-side OCP dominates. Figure 25 and Figure 26 show the cases for output hard short and slowly ramping up the output current. These protections work together to prevent damage to the system such as IC, components, and the load.

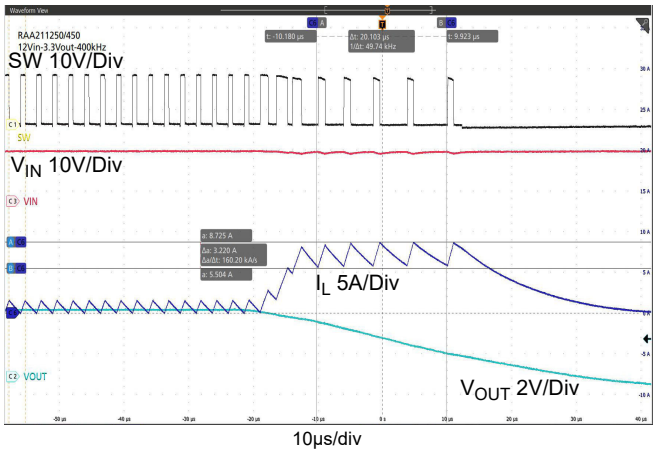


Figure 25. Short Output Protection, High-Side OC Protection

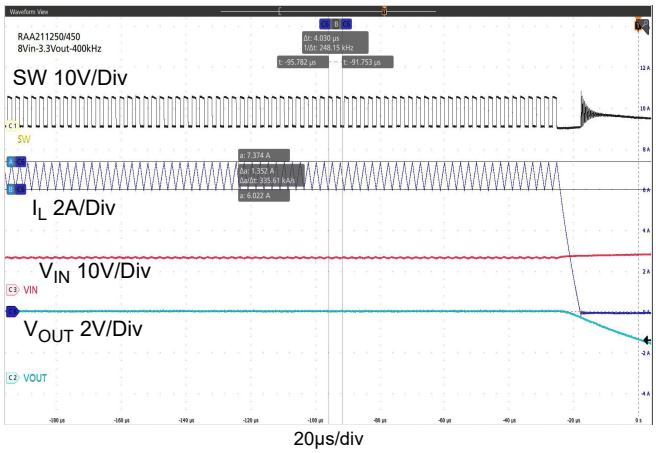


Figure 26. Output Current Ramps Up Slowly from 5A, Low-Side OC Protection

5.11 Undervoltage and Overvoltage Protection

When the RAA211250 senses that the FB voltage has dropped to 50% of V_{REF} (or lower), an undervoltage fault condition exists. Both the high-side and low-side FETs are tri-stated when this condition is detected and the RAA211250 enters a hiccup mode for a 23ms period. The converter attempts to start up after the 23ms hiccup timer expires. If the short or heavy load has been removed, it resumes normal voltage regulation. If the short or heavy load is still present, the fault condition continues, and the converter repeats the hiccup process.

5.12 Thermal Protection

If RAA211250 senses a temperature above the thermal limit (typically 150°C), the converter is disabled and remains disabled until the temperature drops down to 130°C. The PG signal is pulled low during the over-temperature event.

6. Applications Information

6.1 Output Voltage Feedback Resistor Divider

The output voltage can be programmed down to 0.8V with a resistor divider from VOUT to the FB pin to GND based on Equation 4. The recommended R_{FB2} (see Figure 1) resistance is 20kΩ. See Recommended Components Values for Typical Applications for R_{FB1} and R_{FB2} values for typical V_{OUT} applications.

(EQ. 4) $$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 0.8}{0.8}$$

6.2 Inductor Selection

Several factors need to be considered when selecting an inductor for use with the RAA211250. An inductor with lower DC resistance results in higher efficiency; however, the part may be physically larger than required. The saturation current rating needs to be high enough to accommodate DC load current and AC ripple current with additional margin for overload conditions. Selecting a higher inductance value results in lower output ripple voltage; however, transient performance is impacted. Renesas recommends starting off by assuming a range of inductor ripple current of 30% to 50% of maximum output current. Inductor ripple current is calculated using Equation 5.

(EQ. 5) $$\Delta I = \frac{V_{OUT} \times (1 - D)}{L \times f_{SW}}$$

Considering the wide operating input voltage range of the part, Renesas recommends calculating the required inductor by using Equation 6 where V_{OUT} is the output voltage in V, L is the inductance in µH, and f_{SW} is the switching frequency in kHz. Recommended Components Values for Typical Applications can be referenced for selecting the inductance for typical V_{OUT} applications.

(EQ. 6) $$L(\mu H) = \frac{1000 \times V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{\Delta I \times f_{SW}(kHz)}$$

6.3 Input Capacitor Selection

The input capacitor is used in the buck converter to maintain the input voltage by suppressing the voltage ripple induced by discontinuous switching current. The required RMS current rating $I_{IN(RMS)}$ of the input capacitor is calculated using Equation 7 where $I_{OUT(MAX)}$ is the maximum average load current and D is the duty ratio.

(EQ. 7) $$I_{IN(RMS)} = I_{OUT(MAX)} \times \sqrt{D \times (1 - D)}$$

When D equals 0.5, $I_{IN(RMS)}$ has the maximum value which is $I_{OUT(MAX)}/2$.

The voltage rating of the input capacitor should be higher than the maximum input voltage. The required capacitance C_{IN} of the input capacitor to ensure the expected peak-to-peak input voltage ripple ΔV_{IN} is calculated using Equation 8 where f_{SW} is the switching frequency.

(EQ. 8) $$C_{IN} = I_{OUT(MAX)} \times \frac{D \times (1 - D)}{f_{SW} \times \Delta V_{IN}}$$

The required capacitance also has the maximum value when D equals 0.5. Renesas recommends using low ESR/low ESL ceramic capacitors across the input of the regulator. When selecting the ceramic capacitors for power supply applications, consider that the effective capacitance reduces with DC bias voltage across it, so you need to consult the capacitor datasheets to understand the impact of this effect. Also, Renesas recommends using X7R dielectric ceramic capacitors because of their small temperature coefficient.

If the input to the regulator is fed through a high impedance path, Renesas recommends adding an electrolytic capacitor in addition to the ceramic capacitor to dampen the input voltage oscillation effects.

6.4 Output Capacitor Selection

Output capacitor selection impacts both steady-state performance and transient performance of the buck converter. Factors such as output voltage ripple, output voltage variation during transients, and control loop stability should be considered when selecting the output capacitor. Renesas recommends using X7R dielectric ceramic for the output capacitor. When selecting the ceramic capacitor, consider that the effective capacitance reduces with DC bias voltage across it.

The effective capacitance of the ceramic capacitor should be used when determining output voltage ripple. The required capacitance $C_{OUT(RIPPLE)}$ for the expected peak-to-peak output voltage ripple $\Delta V_{OUT(RIPPLE)}$ is calculated using Equation 9 where ΔI_L is the inductor peak-to-peak current ripple and f_{SW} is the switching frequency.

(EQ. 9) $$C_{OUT(RIPPLE)} = \frac{\Delta I_L}{8 \times f_{SW} \times \Delta V_{OUT(RIPPLE)}}$$

To meet the output voltage variation requirements during load step up and load step down transients, the required capacitance $C_{OUT(STEPUP)}$ is calculated using Equation 10 and $C_{OUT(STEPDOWN)}$ is calculated using Equation 11, where I_{STEP} is the transient load step and ΔV_{OUT} is the expected voltage variation during the transient.

(EQ. 10) $$C_{OUT(STEPUP)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times (V_{IN} - V_{OUT}) \times \Delta V_{OUT}}$$

(EQ. 11) $$C_{OUT(STEPDOWN)} = \frac{L \times \left(I_{STEP} + \frac{\Delta I_L}{2}\right)^2}{2 \times V_{OUT} \times \Delta V_{OUT}}$$

To have a stable control loop with adequate gain margin, phase margin, and bandwidth, the required capacitance $C_{OUT(LOOP)}$ is derived using Equation 12 where $C_{OUT(LOOP)}$ is in µF and V_{OUT} is in V.

(EQ. 12) $$C_{OUT(LOOP)(\mu F)} = \frac{150000}{f_{SW(kHz)} \times V_{OUT}}$$

The output capacitors should be selected so that the requirements are met: this means that the total output capacitance should be greater than the highest value calculated in Equation 9, Equation 10, Equation 11, or Equation 12.

See Recommended Components Values for Typical Applications for further guidance when selecting output capacitors for typical V_{OUT} applications.

7. Layout Suggestions

- Place the input ceramic capacitor(s) as close as possible to the IC VIN pin and PGND pins. Keep the power loop (input ceramic capacitor, IC VIN and PGND pins) as small as possible to minimize switch node voltage ringing caused by parasitic inductance in the PCB traces. Minimizing loop size also results in better EMI performance.
- Place an 0402 or 0603 size 0.1µF capacitor as close as possible to VIN and PGND pins. Then place a higher value capacitor such as 1µF or 10µF right next to the 0.1µF capacitor. If an aluminum electrolytic capacitor is used, place it as close as possible to the 0.1µF/1µF/10µF capacitors near the VIN pin.
- Keep the phase node copper area small to reduce parasitic capacitance, but large enough to handle the load current.
- The power ground (CIN and COUT ground) should be connected to the analog ground layer or island, which connects to GND pin, in only one spot.
- Place feedback resistors close to the FB and GND pin and away from phase and boot signals.
- Place the ceramic decoupling capacitor for VCC on the same side of the PCB as the IC, as close as possible to the pin.
- Add additional thermal vias to thermal PGND pad for better heat transfer.

Note: The thermal performance depends on the PCB area and copper layer thickness. For the evaluation board, 2oz copper for top and bottom layers and 1oz copper for two internal layers were used. Use the evaluation board manual as a reference for the PCB layout and further details.

7.1 Layout Examples

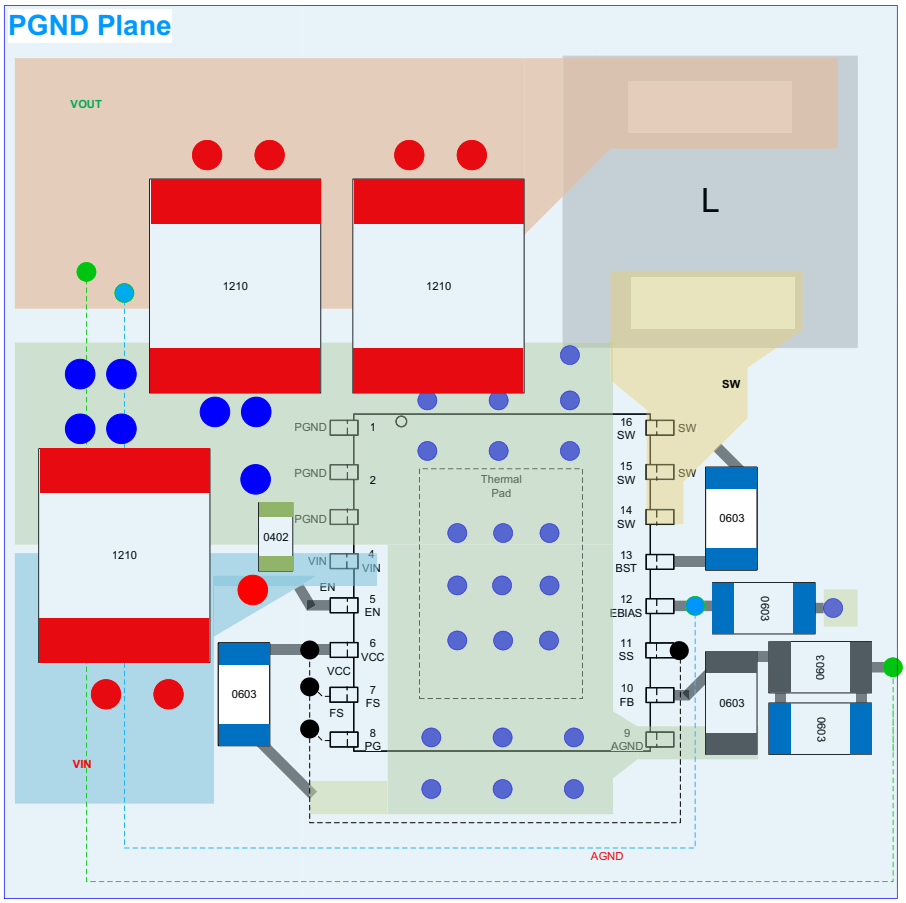


Figure 27. HTSSOP Package Layout Recommendation

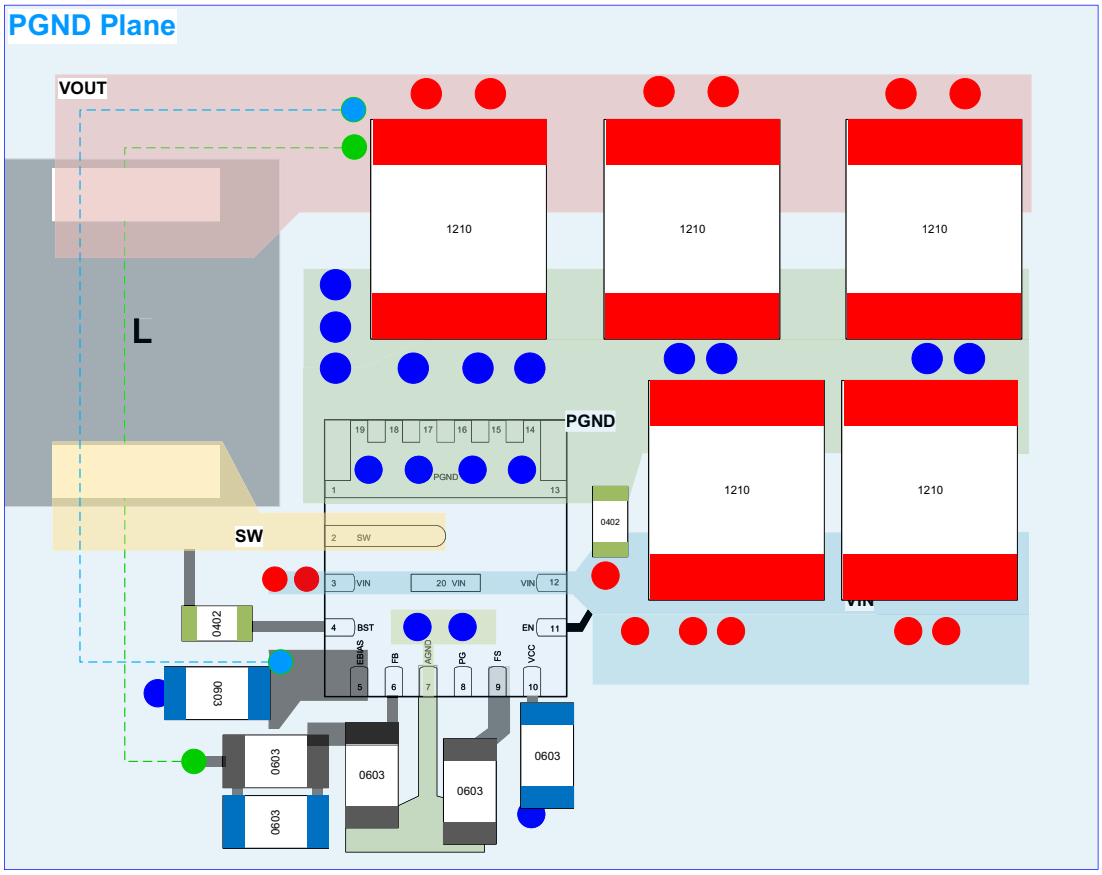


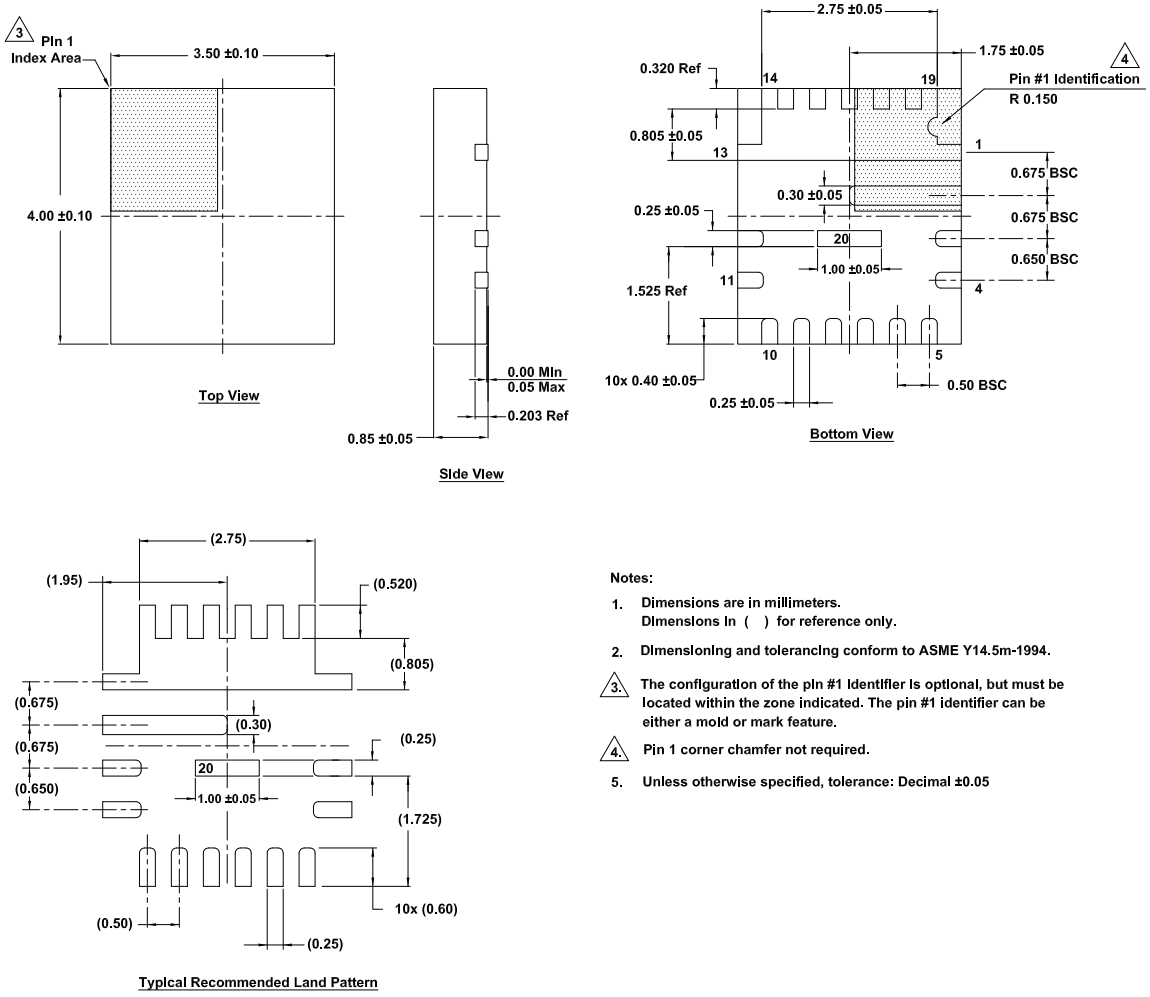
Figure 28. QFN Package Layout Recommendation

8. Package Outline Drawings

For the most recent package outline drawing, see L20.3.5x4.

L20.3.5x4

20 Lead Quad Flat No-Lead Package (QFN)
Rev 2, 8/2022



Notes:

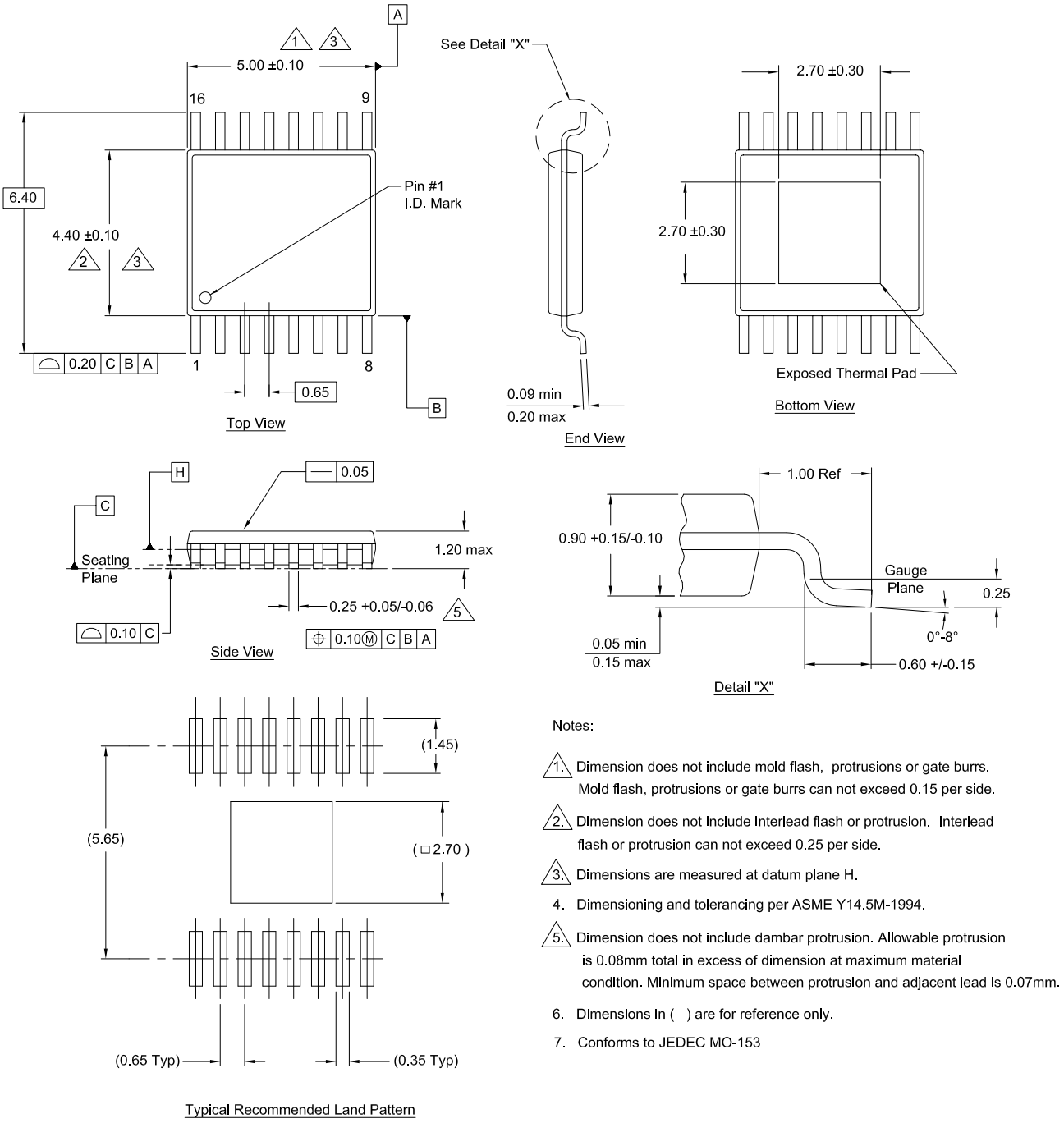
1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier can be either a mold or mark feature.
4. Pin 1 corner chamfer not required.
5. Unless otherwise specified, tolerance: Decimal ±0.05

For the most recent package outline drawing, see M16.173B.

M16.173B

16 Lead Heatsink Thin Shrink Small Outline Package (HTSSOP)

Rev 0, 9/20



Notes:

1. Dimension does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs can not exceed 0.15 per side.
2. Dimension does not include interlead flash or protrusion. Interlead flash or protrusion can not exceed 0.25 per side.
3. Dimensions are measured at datum plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.
5. Dimension does not include dambar protrusion. Allowable protrusion is 0.08mm total in excess of dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm.
6. Dimensions in ( ) are for reference only.
7. Conforms to JEDEC MO-153

9. Ordering Information

Part Number[1][2]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg #	Carrier Type[3]	Junction Temp. Range
RAA211250GNP#HA0	RAA 211250	3.5 x 4 mm QFN	L20.3.5x4	Reel, 6k	-40°C to +125°C
RAA211250GSP#HA0	RAA2 11250	16 Lead HTSSOP	M16.173B	Reel, 2.5k	

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA211250 device page. For more information about MSL, see TB363.
3. See TB347 for details about reel specifications.

10. Revision History

Revision	Date	Description
1.02	Oct 12, 2022	Updated VIN UVLO Rising Threshold minimum value from 4.05V to 3.9V. Updated EBIAS Operating Voltage maximum value from 40V to 30V. Updated EN Deglitch Filter typical value from 1µs to 2.5µs. Updated Figure 1.
1.01	Sep 1, 2022	Updated POD L20.3.5x4 to the latest revision, changes are as follows: ▪ Changed “9x” to “10x” in the bottom view to account for the correct number of leads. Updated Equation 5.
1.00	Aug 4, 2022	Initial release

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(Rev.1.0 Mar 2020)

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