CHAPTER 1. INTRODUCTION

1.1 Features

- **Fully integrated battery management solution with battery capacity measurement and programmable protection capability.**
- **Supports Single Cell Li-ion or Li-Polymer battery cell.**
- **Integrated with Renesas Ultra Low Power RL78 CPU core for multi-function process.**
- **Memory**
  Code flash memory: 64 KB
  Data flash memory (up to 100,000 erase/write cycles): 4 KB
  SRAM: 4 KB
- **Clock generator**
  High speed on-chip oscillator: up to 8 MHz
  Low speed on-chip oscillator: 15 kHz
  AFE speed on-chip oscillator: 2.097 MHz
  AFE low speed on-chip oscillator: 131.072 kHz
- **General Purpose I/O Ports**
  Total: 7 pins
  CMOS input/output: 3, CMOS input: 1
  N-ch open-drain Input/output [6V tolerance]: 3
- **Serial interface**
  I^2C: 1 channel
  UART: 1 channel
  Simplified I^2C: 1 channel
- **Timer**
  16-bit timer: 4 channels**,** 12-bit interval timer: 1 channel
  Real time clock: 1 channel, Watchdog timer: 1 channel
  AFE Timer: 2 channels
  - AFE Timer A: setting range: 125 ms to 64 s
  - AFE Timer B: setting range: 61 us to 2 s
- **Embedded A/D converter**
  AFE 18-bit resolution sigma-delta A/D converter
  - Automatic measurement mode
  - Battery cell voltage, Internal voltage and temperature (AN port voltage) detection function without controlling from F/W.
- **Current integration circuit**
  18-bit resolution sigma-delta A/D converter
- **Impedance measurement circuit**
  Simultaneous measurement of battery voltage and current
- **Overcurrent detection / wake up current detection circuit**
  Discharge short-circuit current detection
  Charge overcurrent detection
  Discharge overcurrent detection
  Charge wakeup current detection
  Discharge wakeup current detection
- **Cell voltage detection circuit**
  Overvoltage detection
  Undervoltage detection
- **Charge and Discharge MOSFET control**
  Supports Low side N-h MOSFET control
- **Charger connect detection circuit**
  Designated charger detection pin when Charge FET is off.
- **Ultra low power consumption**
  Shutdown mode current: 0.1 uA (TYP.)
  Sleep mode 1 current: 10 uA (TYP.) (Protection enable)
  Normal mode current: 2 mA (TYP.) (Protection and Gauging enable, MCU always on)
  Average current under typical operating conditions: 80 uA (TYP.) (Protection and Gauging enable)
- **Voltage and temperature condition**
  Power supply voltage: VDD = 2.0 to 5.5 V
  Operating ambient temperature T_A = -40 to +85 °C
- **Package Information**
  16 pin WLBGA
  ([Body] 1.871 mm x 2.478 mm (TYP.) , 0.5 mm pitch)

1.2 Applications

- Smartphone and other single battery applications

1.3 Description

RAA241200 is a Renesas battery fuel gauge and management device to accomplish various battery protection and management functions. This device incorporates advanced battery management features such as primary and secondary protection, voltage and current measurement, current integration, and host communication interface. Through user programmable control firmware and configuration data stored in the onboard MCU's embedded flash memory, the embedded analog and digital hardware circuits offer optimum battery management operations including high accuracy remaining capacity estimation and battery safety.

CHAPTER 2. OUTLINE

2.1 Outline of Functions

(1/2)

Item		Description
Code Flash memory		64 KB
Data Flash memory		4 KB
RAM		4 KB
Address size		1 MB
Main system clock	High speed on-chip Oscillator clock(f_{IH})	LS (low-speed main) mode: 1 to 8 MHz
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.125 us (Internal high speed oscillation clock: f_{IH} = 8 MHz)
Instruction set		• Data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8 × 8 bits, 16 × 16 bits), Division (16 ÷ 16 bits, 32 ÷ 32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS I/O	3 (P00/INTP10, P01/P02/INTP9, P40/TOOL0)
	CMOS input	1 (P137/INTP2)
	N-ch open-drain I/O (6V tolerance)	3 (P60/SCL/INTP0, P61/SDA/INTP1, P62/INTP7)
Timer	16-bit timer	4 channels (TAU: 4 channels)
	Watchdog timer	1 channel
	Real time clock	1 channel
	12-bit interval timer	1 channel
Serial interface	UART	1 channel
	Simplified I^2C	1 channel
	I^2C	1 channel
Vector interrupt source	Internal	32
	External	6
Reset		・Internal reset by watchdog timer ・Internal reset by illegal instruction execution Note ・internal reset by RAM parity error ・internal reset by illegal memory access
Power-on-reset circuit		・Power-on-reset: 1.51 ± 0.04 V ・Power-down-reset: 1.50 ± 0.04 V
Voltage detector		2.04 V to 4.06 V (10 stages)
On-chip debug function		Support

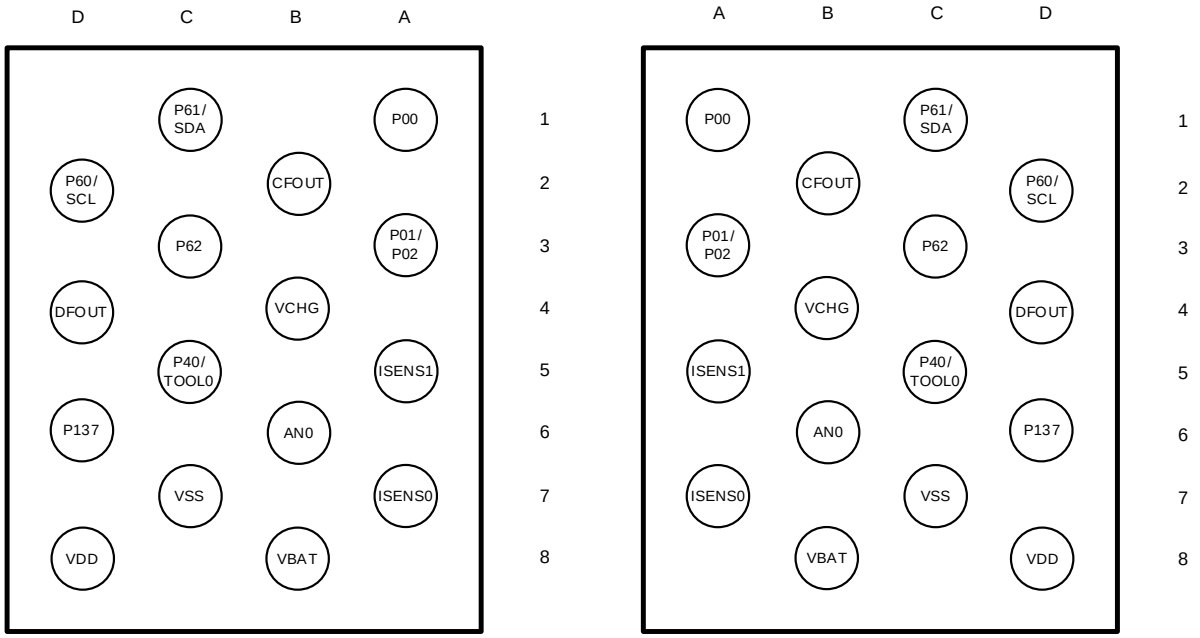
Note The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

(2/2)

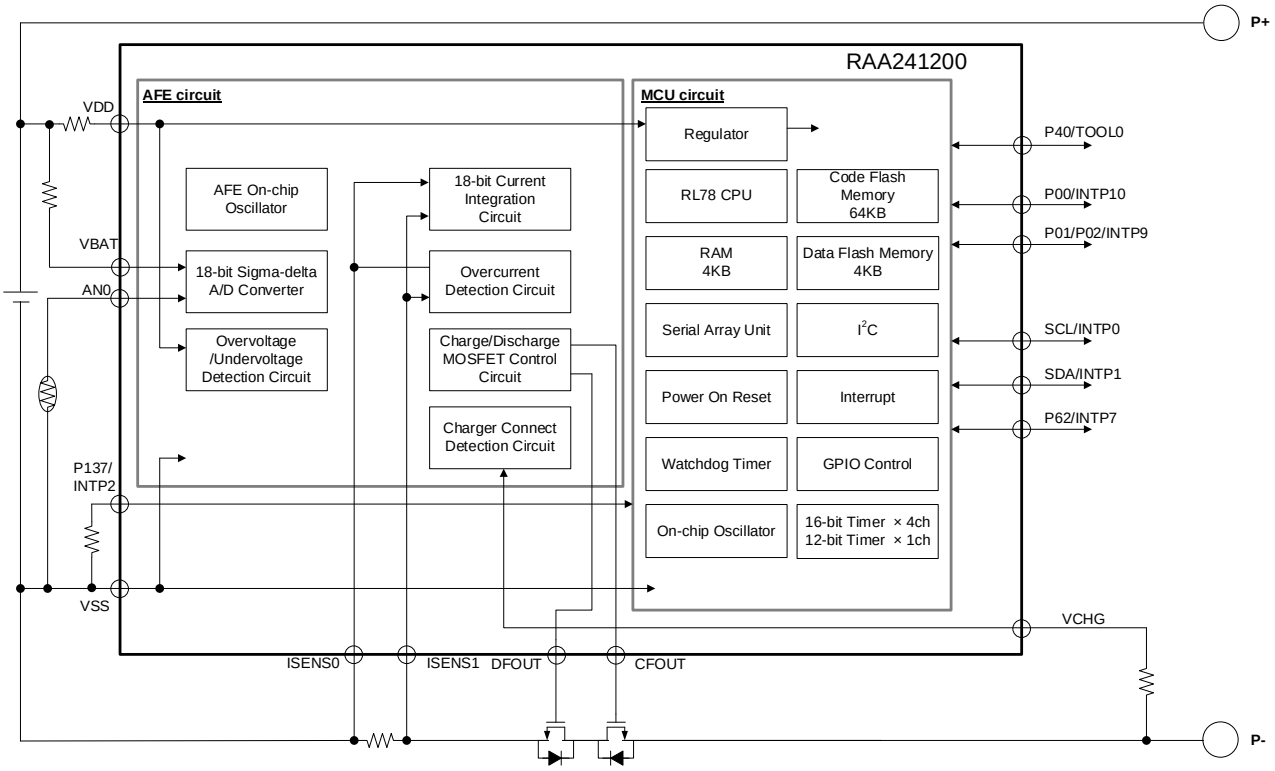
Item	Description
Sigma-delta A/D converter	18-bit resolution (sigma-delta method) • Battery Cell voltage • Thermistor sensor port with on-chip pull-up 10 kΩ resistor: 1 channel • On-chip simple temperature sensor (temperature range: -40 to 85 °C) • Internal reference and supply voltage
Battery cell voltage and temperature (AN port voltage) detection circuit	Battery Cell voltage detection • Over voltage (Overcharge voltage) • Under voltage (Overdischarge voltage) Temperature (AN port voltage) detection • Charge/Discharge Over temperature • Charge/Discharge Under temperature
Current integration circuit	1 channel:18-bit resolution
Current integration circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wakeup current detection circuit	• Discharge short-circuit current detection • Discharge overcurrent detection • Charge overcurrent detection, • Wakeup current detection (discharge and charge)
Overcurrent detection circuit and wakeup current detection circuit	Battery Cell voltage detection • Overvoltage detection • Undervoltage detection
Simple temperature sensor	1 channel
Charge/Discharge FET control circuit	Low Side N-ch MOSFET driver for charge control (C-FET) Low Side N-ch MOSFET driver for discharge control (D-FET)
Charger connect detection circuit	Charger connect detection
AFE On-chip oscillator	2.097 MHz (TYP.)
AFE low speed On-chip oscillator	131.072 kHz (TYP.)
AFE Timer	2 channels • AFE Timer A (setting range: 125 ms to 64 s) • AFE Timer B (setting range: 61 us to 2 s)
Power supply voltage	VDD = 2.0 to 5.5 V
Operation ambient temperature	-40 to 85 °C
Package	16 pin plastic WLBGA([Size] 1.871 mm x 2.478 mm (TYP.), 0.5 mm pitch)

2.2 Pin Configuration

16 pin WLBGA([Body] 1.871 mm x 2.478 mm (TYP.), 0.5 mm pitch)



2.3 Block Diagram



Caution **This example of a peripheral circuit does not guarantee the operation of this device. Evaluate the operation adequately with actual applications, and then determine the circuits and constants.**

Remark It is recommended to connect to VCHG pin to P- terminal via a 200 Ω resistor.

CHAPTER 3. PIN FUNCTIONS

3.1 Pin Identification

No.	Name	Type	Description
A-1	P00/INTP10/SCL00	DIO	Port0 / External Interrupt Input / Simplified I^2C Bus clock I/O
A-3	P01/P02/INTP9/TXD0/ RXD0/SDA00	DIO	Port0 / External Interrupt Input / Serial data of UART I/O / Simplified I^2C Bus data I/O
A-5	ISENS1	AIN	Current sense input for FET side
A-7	ISENS0	AIN	Current sense input for cell minus side
B-2	CFOUT	DOUT	CFET gate voltage output
B-4	VCHG	P	CFET source voltage(P-) input
B-6	AN0	AIN	Thermistor reference voltage output
B-8	VBAT	AIN	Battery voltage input
C-1	P61/SDA/INTP1	DIO	Port6 / I^2C Bus data I/O / External Interrupt Input
C-3	P62/INTP7	DIO	Port6 / External Interrupt Input / Interrupt output (N-ch open-drain)
C-5	P40/TOOL0	DIO	Port4 / Data I/O for flash memory programmer/debugger.
C-7	VSS	P	Ground
D-2	P60/SCL/INTP0	DIO	Port6 / I^2C Bus clock I/O / External Interrupt Input
D-4	DFOUT	DOUT	DFET gate voltage output
D-6	P137/INTP2	DIN	Port13 / External Interrupt Input
D-8	VDD	P	Power supply input

P: **power**

DIO: **digital I/O**

DIN: **digital input**

DOUT: **digital output**

AIN: **analog input**

3.2 Pin Functions

3.2.1 Pin type and alternate functions

Function name	Pin Type	I/O	After Reset Release	Alternate Function	Function
P00	7-1-7	I/O	Input port On-chip-pull-up on	INTP10/SCL00	Port 0. 3-bit I/O port. Input/output can be specified in 1-bit unit.
P01/P02	7-1-7-1	I/O		INTP9/TXD0/RXD0/SDA00	
P40	7-1-3	I/O	Input port On-chip-pull-up on	TOOL0	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
P60	12-1-2	I/O	Input port On-chip-pull-up on	INTP0/SCL	Port 6. 3-bit I/O port. Input/output can be specified in 1-bit unit. Output of P60 to P62 can be set to N-ch open-drain output (6.0 V tolerance).
P61	12-1-2			INTP1/SDA	
P62	12-1-2			INTP7	
P137	2-1-2	Input	Input port	INTP2	Port 13. 1-bit input-only port.

3.2.2 External Pin Functions

Category	Pin name	I/O	Function
Power supply	VDD	–	Power supply input Apply power supply voltage to VDD pin from a charger or battery.
	VSS	–	Ground input Connect the negative input terminal of lithium-ion battery
	VCHG	–	Ground input for CFOUT Connect the negative input terminal of battery pack
TOOL0	TOOL0 Note	Input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external 1kΩ pull-up resistor in the on-chip debug mode
I^2C-BUS interface (IICA0)	SCL	I/O	Serial clock I/O pin of serial interface IICA0
	SDA	I/O	Serial data I/O pin of serial interface IICA0
I^2C-BUS interface (IIC00)	SCL00	I/O	Serial clock I/O pin of serial interface IIC00 (Simplified I^2C)
	SDA00	I/O	Serial data I/O pin of serial interface IIC00 (Simplified I^2C)
Serial interface (UART0)	TXD0	Output	Serial data output of UART0
	RXD0	Input	Serial data input of UART0
A/D converter	AN0	Input	A/D converter analog input
Current integration circuit and overcurrent detection circuit	ISENS0, ISENS1	Input	Analog input for current integration circuit and over current detection circuit
External interrupt input	INTP0 INTP1 INTP2 INTP7 INTP9 INTP10	Input	Interrupt request input pin
Battery voltage detection circuit	VBAT	Input	The positive input terminal of lithium-ion battery
MOSFET control	CFOUT	Output	Control signal for low side charge N-ch MOSFET
	DFOUT	Output	Control signal for low side discharge N-ch MOSFET

Note After reset release, the connection between P40/TOOL0 and P01/P02 pin and the operating mode are as follows.

Table 3-3-1 Operation Mode entry after Reset Release

P40/TOOL0	P01/P02	Operation Mode
VDD	-	Normal operation mode
VSS	VDD	Flash memory programming mode
	VSS	SMBus Boot programming mode

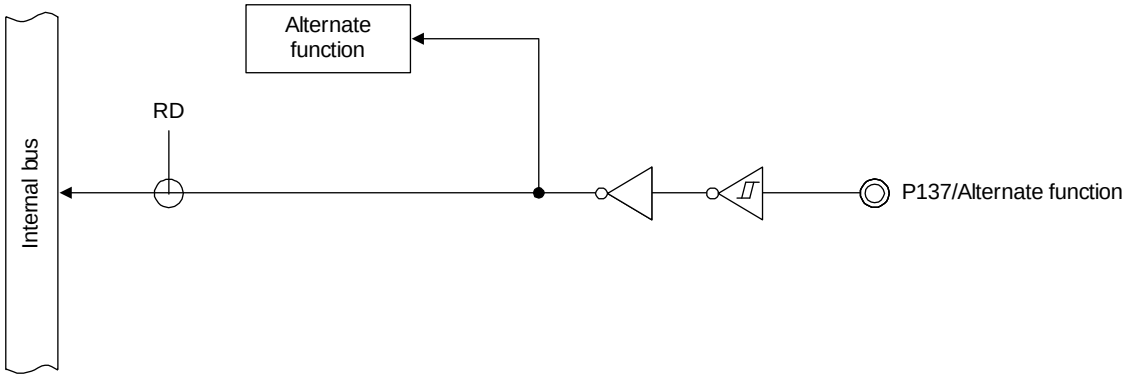
3.3 Unused Pins Connection

Table 3-2 Unused Pins connection

Pin Name	Recommended Connection of Unused Pins
P00-P02	Input: Independently connect to VDD via a resistor, or leave open. Output: Leave open.
P40/TOOL0	Input: Independently connect to VDD via a resistor, or leave open. Output: Leave open.
P60-P62	Input: Leave open. Output: Leave open.
P137	Input: Independently connect to VDD or VSS via a resistor.
AN0	Leave open.
DFOUT	Leave open.
CFOUT	Leave open.
VBAT	Connect to VDD via a resistor.
ISENS1, ISENS0	Connect to VSS.

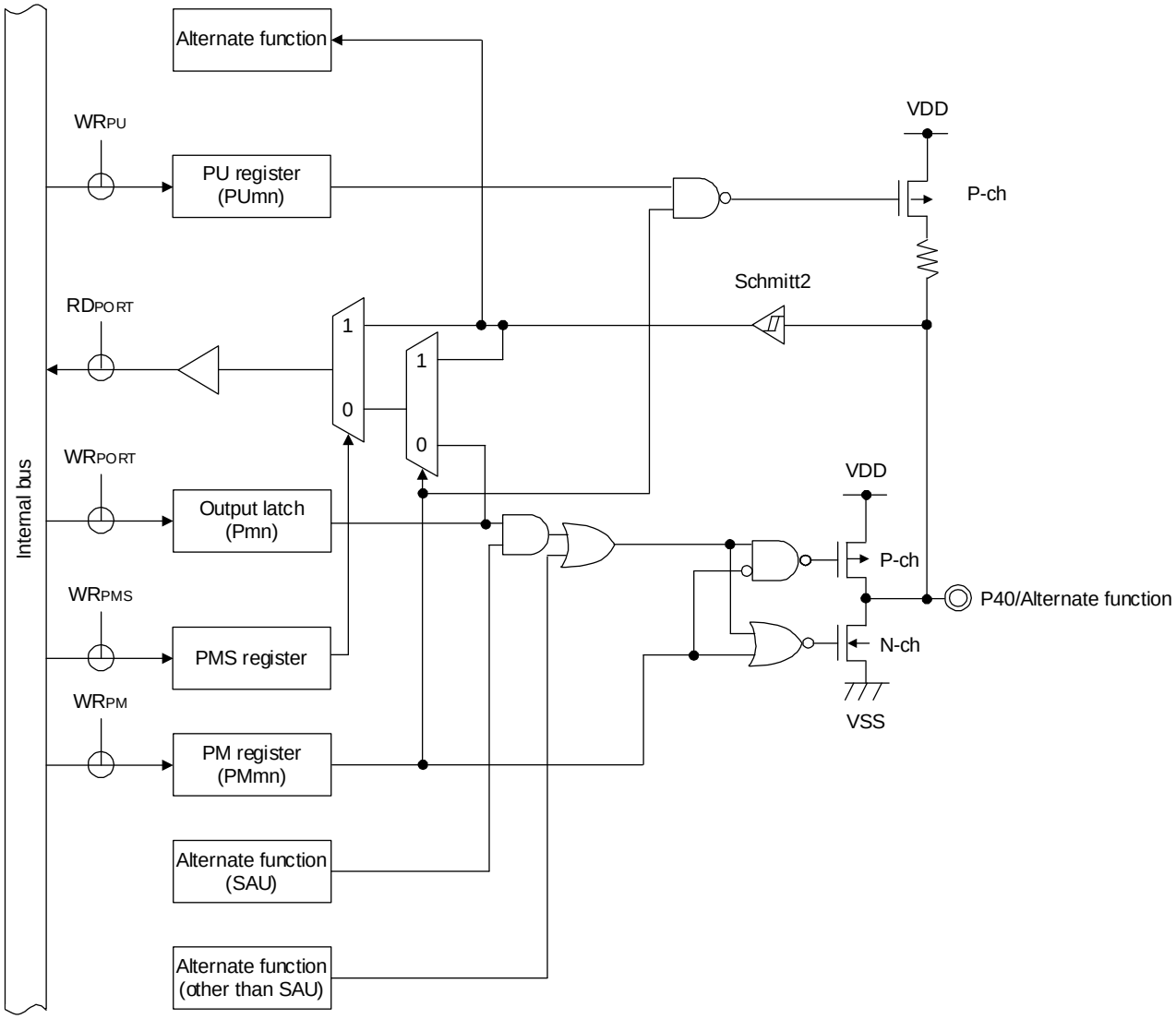
3.4 Pin Block Diagram

Figure 3-1 Pin Block Diagram of Pin type 2-1-2



Remark Refer to 3.2.1 Pin type and alternate functions.

Figure 3-2 Pin Block Diagram of Pin type 7-1-3



Remark Refer to 3.2.1 Pin type and alternate functions.

Figure 3-3 Pin Block Diagram of Pin type 7-1-7

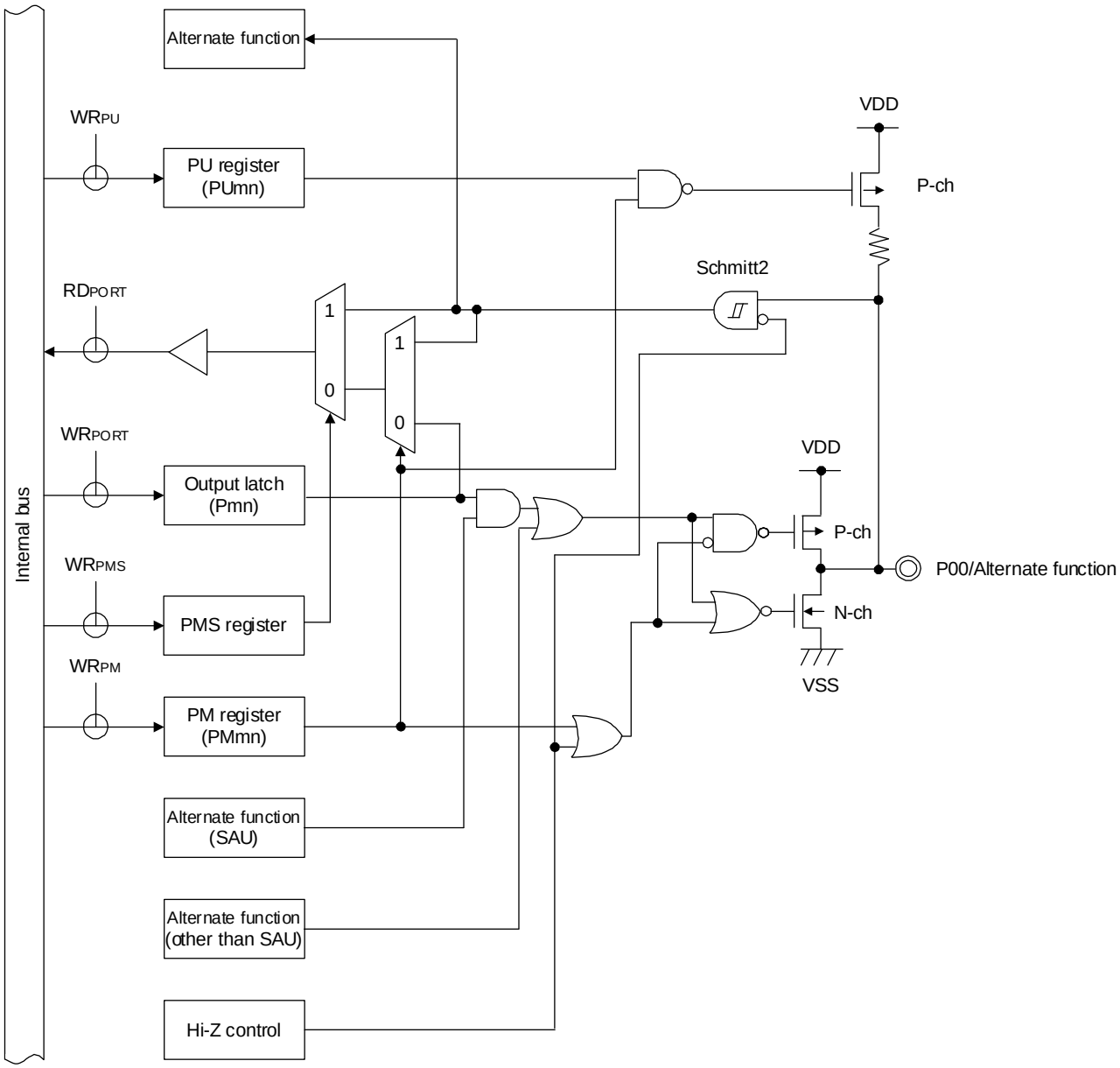


Figure 3-4 Pin Block Diagram of Pin type 7-1-7-1

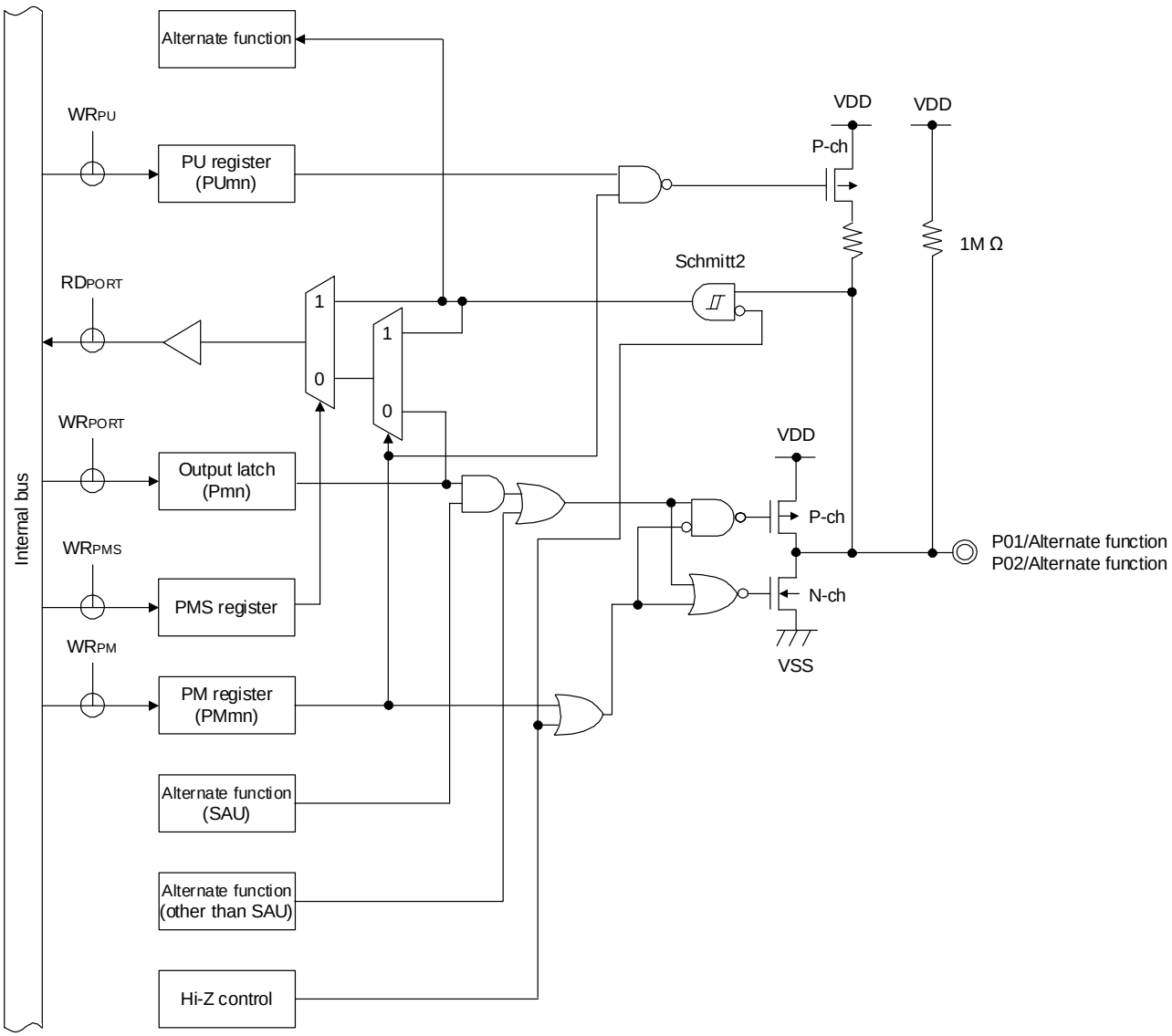
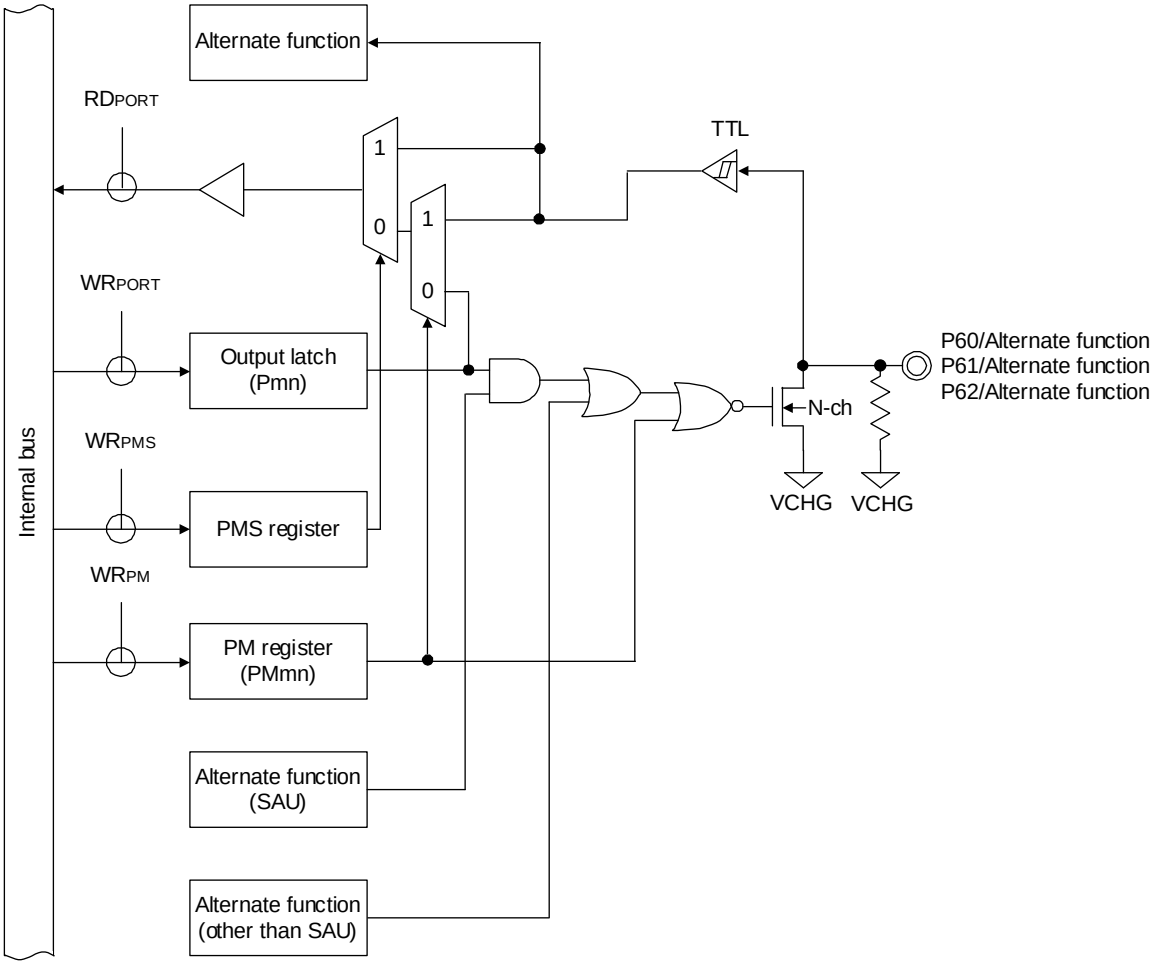


Figure 3-5 Pin Block Diagram of Pin type 12-1-2



Remark Refer to 3.2.1 Pin type and alternate functions.

Figure 3-6 Pin Block Diagram of VBAT Pin

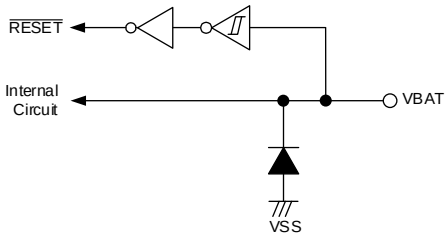


Figure 3-7 Pin Block Diagram of AN0 Pin

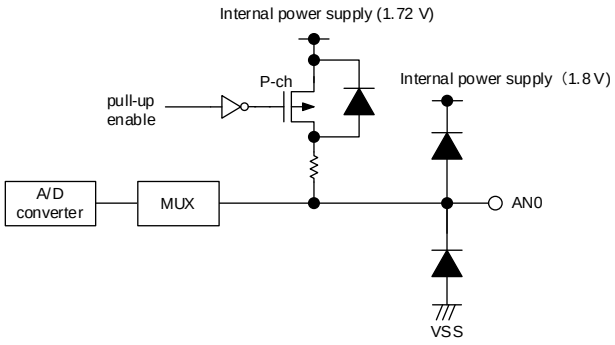


Figure 3-8 Pin Block Diagram of ISENS0 and ISENS1 Pin

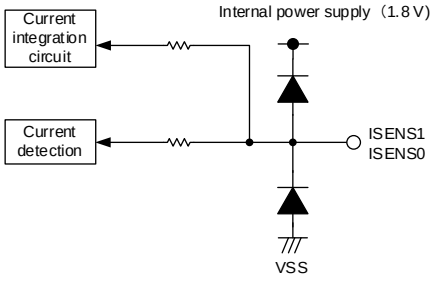


Figure 3-9 Pin Block Diagram of CFOUT Pin

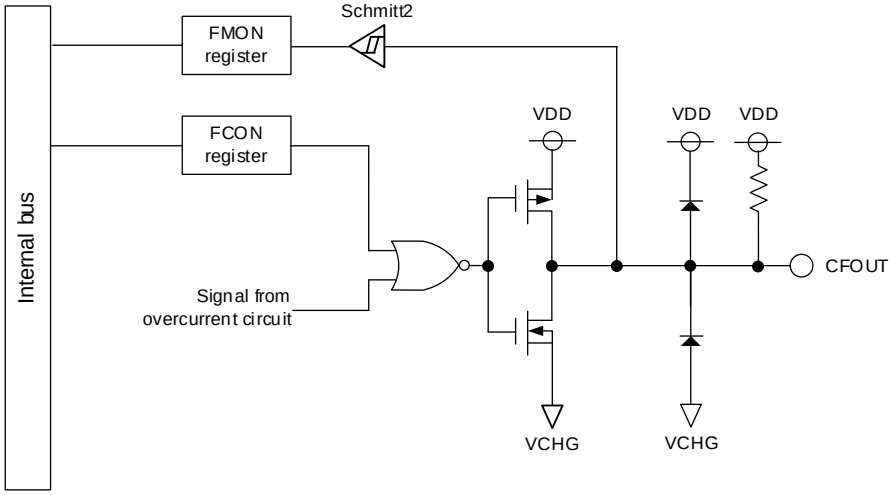


Figure 3-10 Pin Block Diagram of DFOUT Pin

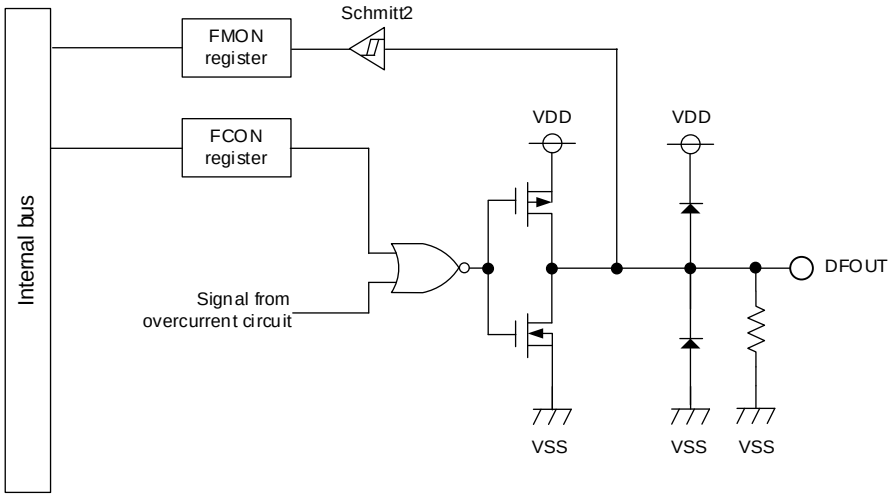
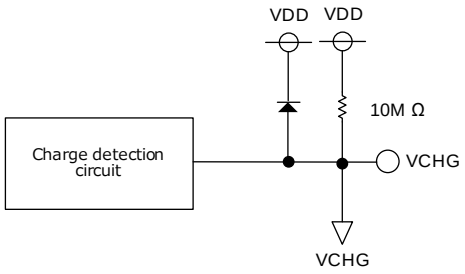


Figure 3-11 Pin Block Diagram of VCHG



CHAPTER 4. ANALOG FRONT END FUNCTIONS

4.1 Overview

Table 4-1 shows the AFE function.

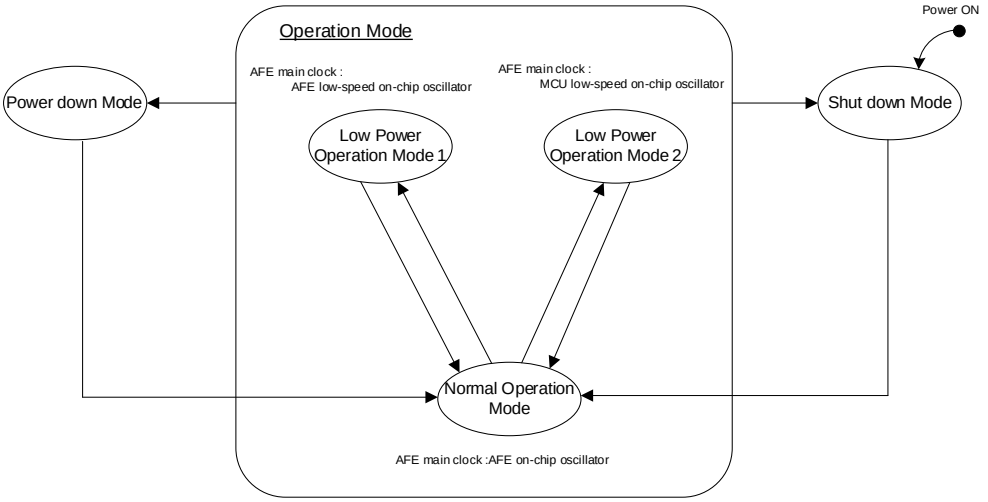
Table 4-1 AFE functions

Item	Description
Sigma-delta A/D converter	18-bit resolution (sigma-delta method) • Battery Cell voltage • Thermistor sensor port with on-chip pull-up 10kΩ resistor: 1 channel • On-chip simple temperature sensor (temperature range: -40 to 85 °C) • Internal reference and supply voltage
Battery cell voltage and temperature (AN port voltage) detection circuit	Battery Cell voltage detection • Over voltage (Overcharge voltage) • Under voltage (Overdischarge voltage) Temperature (AN port voltage) detection • Charge/Discharge Over temperature • Charge/Discharge Under temperature
Current integration circuit	1 channel:18-bit resolution
Current integration circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wakeup current detection circuit	• Discharge short-circuit current detection • Discharge overcurrent detection • Charge overcurrent detection • Wakeup current detection (discharge and charge)
Overvoltage/Undervoltage detection circuit	Battery Cell voltage detection • Overvoltage detection • Undervoltage detection
Simple temperature sensor	1 channel
Charge/Discharge MOSFET control circuit	Low Side N-ch MOSFET driver for charge control (C-FET) Low Side N-ch MOSFET driver for discharge control (D-FET)
Charger connect detection circuit	Charger connect detection
AFE On-chip oscillator	2.097 MHz (TYP.)
AFE Low speed on-chip oscillator	131.072 kHz (TYP.)
AFE Timer	2 channels • AFE Timer A (setting range: 125 ms to 64 s) • AFE Timer B (setting range: 61 us to 2 s)

4.2 AFE Operation Mode

Figure 4-1 shows AFE state transition diagram and overview of each mode is described in 4.2.1 to 4.2.6.

Figure 4-1 AFE state transition diagram



4.2.1 Power ON (MCU reset release)

AFE normal mode transition starts when MCU reset is released.

4.2.2 Normal Operation Mode

Normal Operation Mode represents the fully operational mode. ADC measurement can be performed in this mode.
Both AFE low-speed on-chip oscillator and AFE on-chip oscillator operate. The AFE on-chip oscillator is selected as the AFE main clock. This is the highest current consumption mode of AFE.

4.2.3 Low Power Operation Mode 1

In **Low Power Operation Mode 1**, power consumption is reduced by stopping AFE on-chip oscillator. In this mode, the AFE low-speed on-chip oscillator is selected as the AFE main clock.

4.2.4 Low Power Operation Mode 2

In **Low Power Operation Mode 2**, power consumption is reduced by stopping AFE on-chip oscillator and AFE low-speed on-chip oscillator. In this mode, the MCU low-speed on-chip oscillator is selected as the AFE main clock. In this mode, circuit other than the Discharge short-circuit current detection, the discharge overcurrent detection, charge wakeup current detection and undervoltage detection are prohibited.

4.2.5 Power down Mode

In this mode, all AFE circuits except charger connect detection circuits are under shutdown. AFE registers except trimming registers are initialized. MCU is working and its interrupt is operable.

4.2.6 Shutdown Mode

The lowest power mode that this device supports. All MCU and AFE circuits except charger connect detection circuits are under shutdown condition in this mode.

4.2.7 Operating Blocks of AFE

Table 4-2 shows list of blocks that can be operated in each mode.

Table 4-2 Operating Blocks of AFE

Block	Normal Operation Mode	Low Power Operation Mode 1	Low Power Operation Mode 2	Power down Mode	Shutdown Mode
Sigma delta A/D Converter	Available	Unavailable	Unavailable	Unavailable	Unavailable
Current integration circuit	Available	Available	Unavailable	Unavailable	Unavailable
Overcurrent detection circuit Wakeup current detection circuit	Available	Available	Available Note 1	Unavailable	Unavailable
Overvoltage / Undervoltage detection circuit	Available	Available	Available Note 2	Unavailable	Unavailable
AFE Timer	Available	Available	Available	Unavailable	Unavailable
Charger Detection	Available	Available	Available	Available	Available

Note 1. In Low Power Operation Mode 2, only Discharge short-circuit current detection circuit, Discharge overcurrent detection circuit, and Charge wakeup current detection circuit are available.

Note 2. In Low Power Operation Mode 2, only Undervoltage detection circuit is available.

4.3 AFE Clock Generator

The AFE clock generator generates the clock to be supplied to the AFE internal circuit.

The following three kinds of clock generators are selectable.

4.3.1 AFE On-chip Oscillator (AOCO)

This circuit oscillates a clock of f_{IAH} = 2.097 MHz (TYP.).

AFE on-chip oscillator can be controlled to enable or disable by register when it is not in use.

4.3.2 AFE Low-speed On-chip Oscillator (ALOCO)

This circuit oscillates a clock of f_{IAL} = 131.072 kHz (TYP.).

The AFE low-speed on-chip oscillator is turned on when using AFE.

4.3.3 MCU Low-speed On-chip Oscillator (LOCO)

This circuit oscillates a clock of f_{IL} = 15 kHz (TYP.).

4.4 Charge/Discharge MOSFET Control Circuit

Charge/Discharge MOSFET control circuit can drive the external charge N-ch MOSFET (charge FET) and discharge N-ch MOSFET (discharge FET). And, MOSFET status can be monitored.

4.5 Sigma-delta A/D Converter

The A/D converter comprises an 18-bit sigma-delta A/D converter.

The analog signal output by the multiplexer circuit of AFE can be selected as input channels.

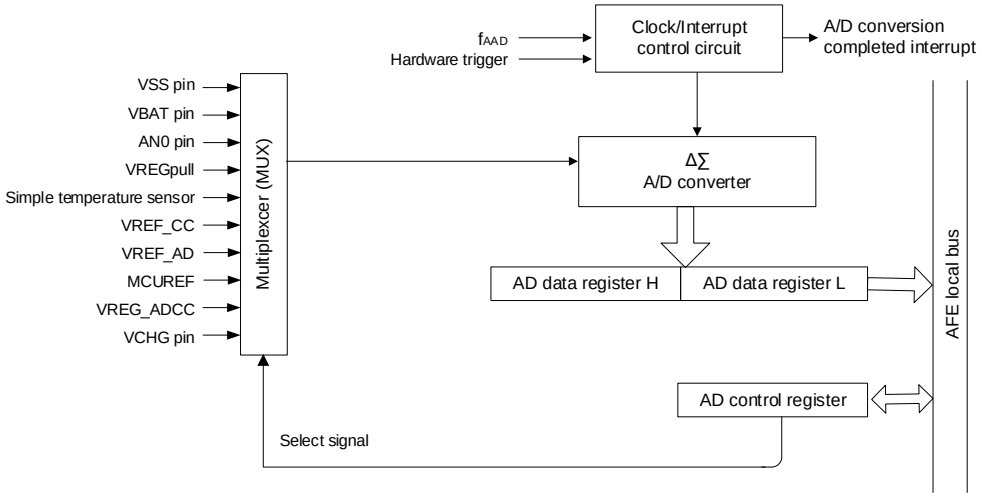
Table 4-3 A/D converter performance

Items	Performance
A/D Conversion method	Sigma-delta A/D Conversion method
Analog input voltage range	-0.1 V to 5.1 V
Operating clock	f_{AAD} : 1.049 MHz
Resolution	18 bits max
Conversion accuracy	Integral non-linearity error: ±27 LSB
Multiplexer input channel	Refer to Table 4-4 Selection of A/D converter input channel.
A/D conversion start condition	Software trigger or Hardware trigger
Conversion rate per item	256 AD cycles : 0.25 ms mode 512 AD cycles : 0.5 ms mode 1024 AD cycles : 1 ms mode 2048 AD cycles : 2 ms mode 4096 AD cycles : 4 ms mode 8192 AD cycles : 8 ms mode 16384 AD cycles : 16 ms mode 32768 AD cycles : 32 ms mode 65536 AD cycles : 64 ms mode

Table 4-4 Selection of A/D converter input channel

	Item	Input to ADC (+side)	Input to ADC (-side)
1	Offset Voltage	VSS pin	VSS pin
2	Battery Cell Voltage	VBAT pin	VSS pin
3	AN0 pin	AN0 pin	VSS pin
4	Internal Power supply for AN0 pin’s pull-up	VREGpull	VSS pin
5	Internal Simple temperature sensor	Simple temperature sensor	VSS pin
6	Reference voltage for CC	VREF_CC	VSS pin
7	Reference voltage for AD	VREF_AD	VSS pin
8	MCU internal reference voltage	MCUREF	VSS pin
9	Internal Power supply for AD/CC	VREG_ADCC	VSS pin
10	VCHG	VCHG pin	VSS pin

Figure 4-2 Block diagram of A/D converter



4.6 Current Integration Circuit

This circuit can measure current value through current sensing resistor by digital conversion of voltage potential difference between both pin ends of current sensing resistor connected to ISENS1 pin and ISENS0 pin.

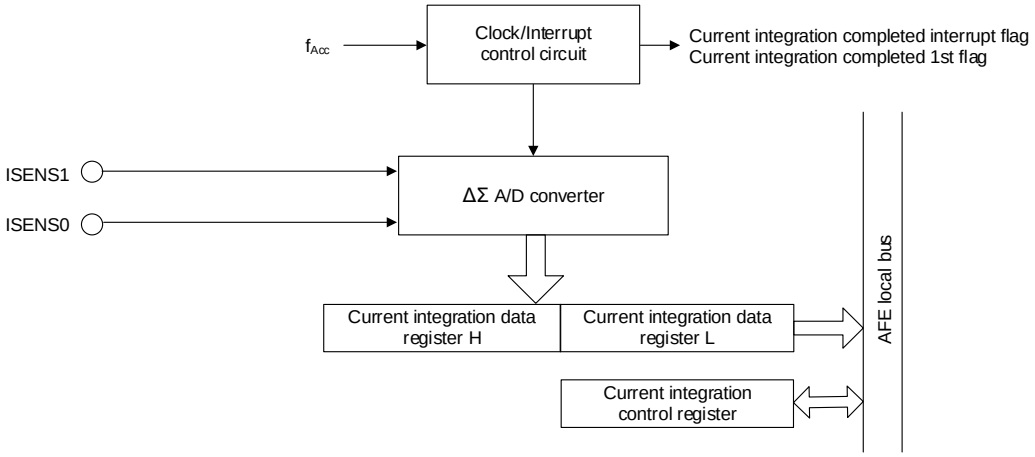
Analog signals are input from ISENS1 pin and ISENS0 pin.

Table 4-5 Current integration circuit performance

Item	Performance
Conversion method	Sigma-delta A/D Conversion method
Analog input voltage range	-0.05 V to 0.05 V
Operating clock	f_{ACC} : 131.072 kHz, 32.768 kHz, 8.192 kHz Note
Resolution	18 bits
Conversion accuracy	Integral non-linearity error: ±0.02 %FSR
Analog input pin	Potential difference between ISENS1 pin and ISENS0 pin
Conversion time per cycle	250 ms (32,768 (f_{ACC}=131.072 kHz) cycle) 1000 ms (32,768 (f_{ACC}=32.768 kHz) cycle) 4000 ms (32,768 (f_{ACC}=8.192 kHz) cycle)

Note It varies by conversion time setting.

Figure 4-3 Current integration circuit block diagram



4.7 Current Integration Circuit for Impedance Measurement

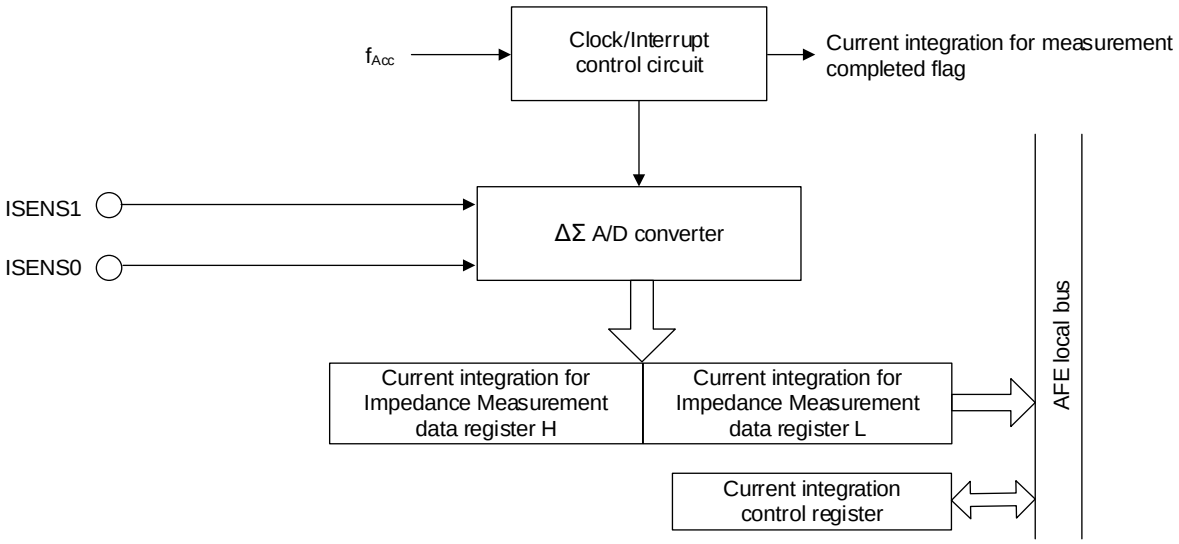
This circuit can measure current value through current sensing resistor by digital conversion of voltage potential difference between both pin ends of current sensing resistor connected to ISENS1 pin and ISENS0 pin being synchronized with A/D conversion. Impedance value can be measured from the voltage value and current value to be synchronized with A/D conversion.

Analog signals are input from ISENS1 pin and ISENS0 pin.

Table 4-6 Current integration circuit for impedance measurement performance

Item	Performance	
Conversion method	Sigma-delta A/D Conversion method	
Analog input voltage range	-0.05 V to 0.05 V	
Operating clock	f_{lack} : 131.072 kHz, 32.768 kHz	
Resolution	● First order filter Conversion time 64 ms: 13 bits Conversion time 32 ms: 12 bits Conversion time 16 ms: 11 bits Conversion time 8 ms: 10 bits Conversion time 4 ms: 9 bits Conversion time 2 ms: 8 bits Conversion time 1 ms: 7 bits Conversion time 0.5 ms: 6 bits Conversion time 0.25 ms: 5 bits	● Second order filter Conversion time 64 ms: 15 bits Conversion time 32 ms: 15 bits Conversion time 16 ms: 15 bits Conversion time 8 ms: 15 bits Conversion time 4 ms: 15 bits Conversion time 2 ms: 15 bits Conversion time 1 ms: 14 bits Conversion time 0.5 ms: 12 bits Conversion time 0.25 ms: 8 bits
Analog input pin	Potential difference between ISENS1 pin and ISENS0 pin	
Conversion time per cycle	0.25 ms, 0.5 ms, 1 ms, 2 ms, 4 ms, 8 ms, 16 ms, 32 ms, 64 ms	

Figure 4-4 Current integration circuit for impedance measurement block diagram



4.8 Overcurrent Detection and Wakeup Current Detection Circuit

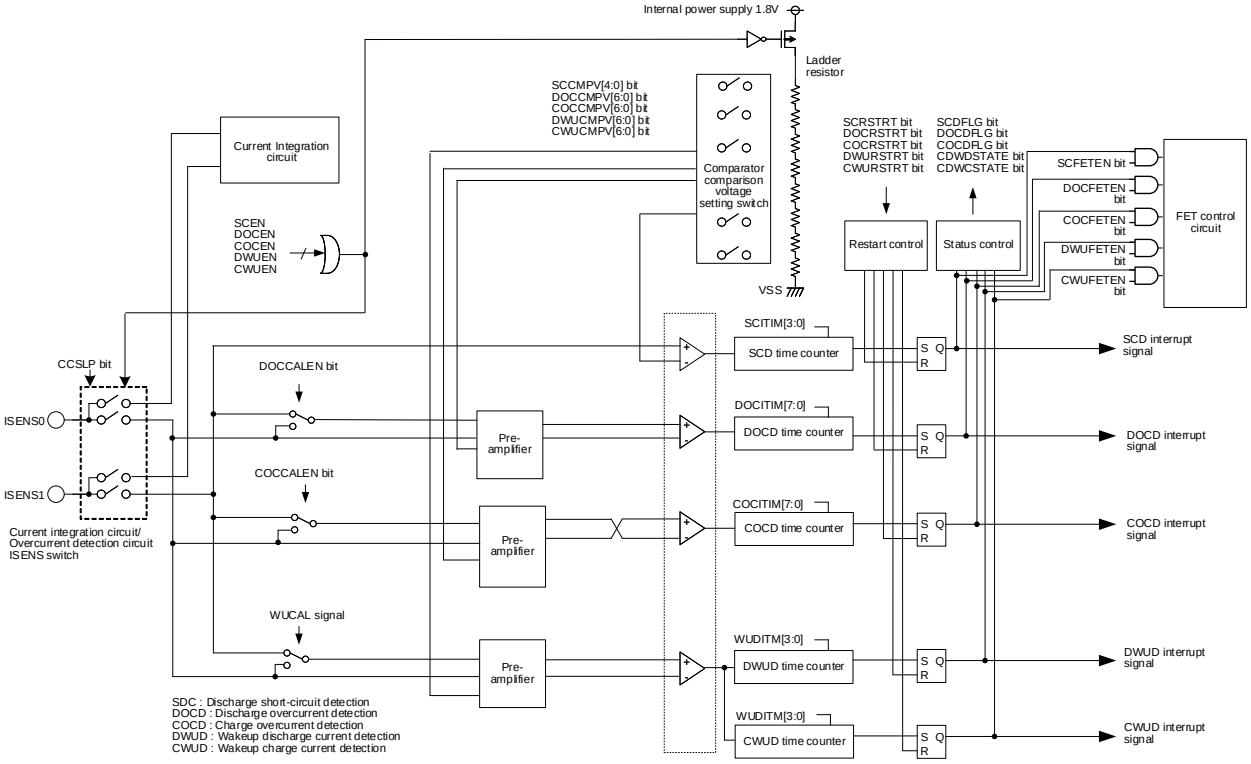
The overcurrent detection circuit detects overcurrent such as short-circuit current that flows through the detection resistor connected between pins ISENS1 and ISENS0, and turns off the battery pack charge/discharge control MOSFET to stop charging/discharging. The overcurrent detection circuit incorporates discharge short-circuit current circuit, discharge short-circuit current circuit, discharge overcurrent circuit, and charge overcurrent circuit, for which detection voltage and detection time can be set independently.

In addition, the overcurrent detection circuit also incorporates a wakeup current detection circuit to generate an interrupt in power down mode where the current integration circuit is disabled when a battery is charging or discharging.

Table 4-7 Overcurrent detection and Wakeup current detection circuit performance

item	Contents	
Analog input pin	ISENS1, VSS (Discharge short circuit) ISENS1, ISENS0 (Other than above)	
Operating clock	Discharge short-circuit current detection	f_{ACD} : 32.768 kHz f_{IL} : 15 kHz
	Discharge overcurrent detection	f_{ACD} : 32.768 kHz f_{IL} : 15 kHz
	Charge overcurrent detection	f_{ACD} : 32.768 kHz
	Discharge wakeup current detection	f_{ACD} : 32.768 kHz
	Charge wakeup current detection	f_{ACD} : 32.768 kHz f_{IL} : 15 kHz
Detection voltage Setting range (setting interval)	Discharge short-circuit current detection	24 mV to 216 mV (12 mV)
	Discharge overcurrent detection	3 mV to 31.2 mV (0.3 mV)
	Charge overcurrent detection	-25.2 mV to -3 mV (0.3 mV)
	Discharge wakeup current detection	3 mV to 31.2 mV (0.3 mV)
	Charge wakeup current detection	-31.2 mV to -3 mV (0.3 mV)
Detection time Setting range (setting interval)	Discharge short-circuit current detection	f_{ACD} : 0 us to 916 us (61 us) f_{IL} : 0 us to 1005 us (67 us)
	Discharge overcurrent detection	f_{ACD} : 0.122 ms to 31.25 ms (0.122 ms) f_{IL} : 0.133 ms to 34.1 ms (0.133 ms)
	Charge overcurrent detection	0.122 ms to 31.25 ms (0.122 ms)
	Discharge wakeup current detection	3.91 ms to 62.56 ms (3.91 ms)
	Charge wakeup current detection	3.91 ms to 62.56 ms (3.91 ms)

Figure 4-5 Overcurrent detection and Wakeup detection circuit block diagram



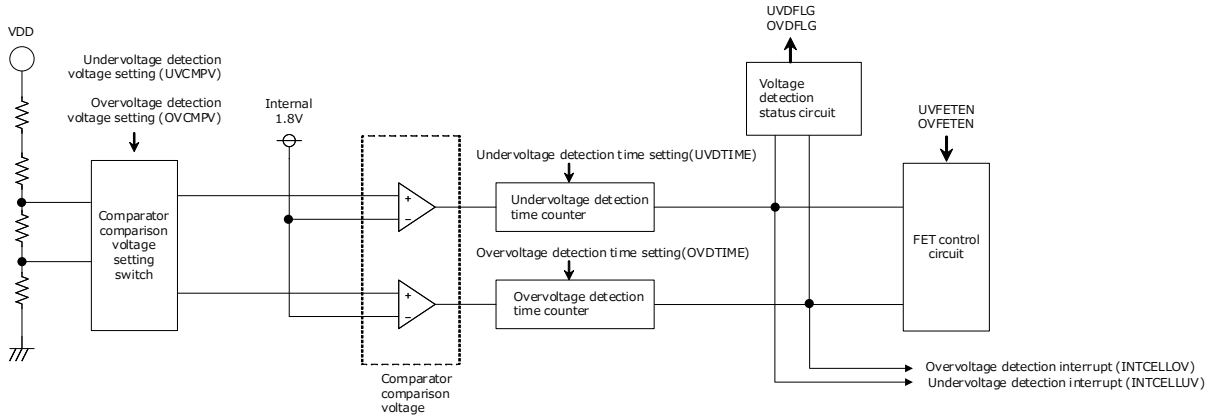
4.9 Overvoltage / Undervoltage Detection Circuit

Overvoltage detection circuit can detect voltage potential difference between VDD pin and VSS pin and control charge MOSFET. And undervoltage detection circuit can detect voltage potential difference between VDD pin and VSS pin and control discharge MOSFET.

Table 4-8 Overvoltage / Undervoltage detection circuit performance

item	Contents	
Analog input pin	VDD, VSS	
Operating clock	Overvoltage detection	f_{IAH}, f_{IAL}
	Undervoltage detection	f_{IAH}, f_{IAL}, f_{IL}
Detection voltage Setting range (setting interval)	Overvoltage detection	4300 mV to 4800 mV (5 mV)
	Undervoltage detection	2200 mV to 3000 mV (50 mV)
Detection delay time Setting range (setting interval)	Overvoltage detection	400 ms to 1000 ms (200 ms)
	Undervoltage detection	20 ms, 96 ms, 128 ms, 144 ms
Release hysteresis voltage Setting range (Setting interval)	Overvoltage detection	100 mV to 400 mV (100 mV)
	Undervoltage detection	100 mV to 500 mV (100 mV)

Figure 4-6 Overvoltage / Undervoltage detection circuit block diagram



4.10 AFE Timer

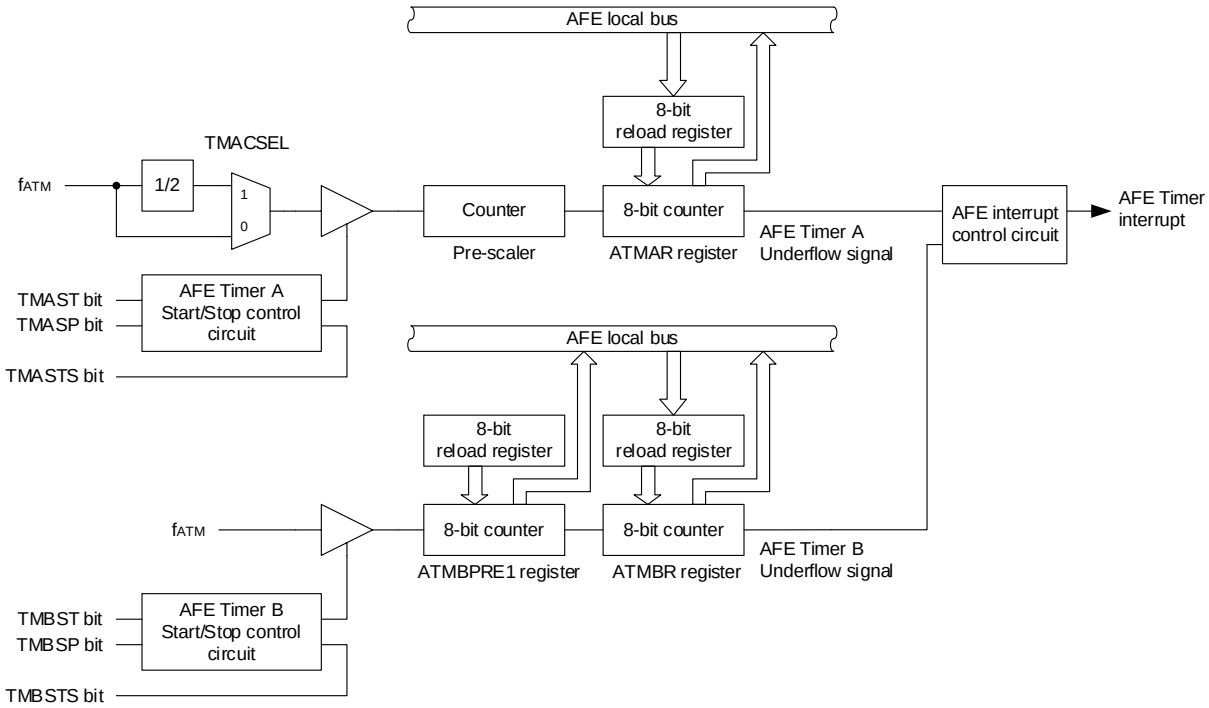
AFE Timer is a timer for time measurement with on-chip two channel timers (AFE Timer A and AFE Timer B).

These are composed of re-load register and down counter, and arranged at the same AFE address.

Table 4-9 AFE Timer performance

Item	Contents
Operation	Count a count source
Count source	f_{ATM} : 32.768 kHz or $f_{ATM/2}$
Interrupt	when counter underflows
Setting	AFE Timer A: 125 ms to 64 s AFE Timer B: 61 us to 2 s

Figure 4-7 AFE Timer block diagram



4.11 Battery cell voltage and Temperature (AN port Voltage and Simple Temperature Sensor) Detection Circuit

Battery cell voltage and temperature (AN port voltage) detection circuit detects following factors individually.

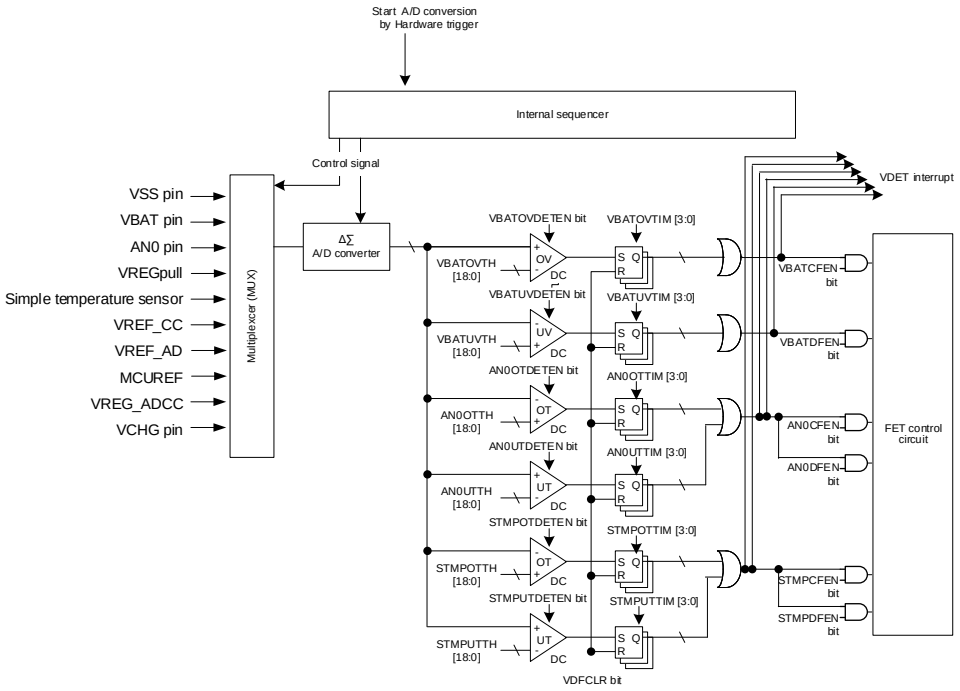
- Over/Under voltage of battery cell (Cell voltage).
- Charge/Discharge over temperature (AN port voltage and Simple temperature sensor).
- Charge/Discharge under temperature (AN port voltage and Simple temperature sensor).

Battery cell voltage, AN port voltage and Simple temperature sensor are measured by A/D converter. Then, the measurement result is compared with setting value of each register by digital comparator. When over/under voltage and over/under temperature are detected by digital comparator, interrupt signal is generated and appropriate charge/discharge MOSFET is shut off.

Table 4-10 Battery cell voltage and temperature (AN port voltage) detection circuit performance

Items	Performance
Voltage detection method	Sigma-delta A/D conversion and digital comparator method
Monitor items	Battery cell voltage input VBAT pin to VSS pin Thermistor sensor pin with on-chip pull-up 10 kΩ resistor: AN0 pin
Voltage detection items	Over voltage of battery cell voltage Under voltage of battery cell voltage Charge/discharge over temperature (Monitoring AN0 voltage and Simple temperature sensor) Charge/discharge under temperature (Monitoring AN0 voltage and Simple temperature sensor)
A/D conversion start condition	Hardware trigger
Voltage detection start condition	Hardware trigger
Voltage detection threshold range	0000H to FFFFH
Voltage detection delay time	1 to 15 time (1 time step)

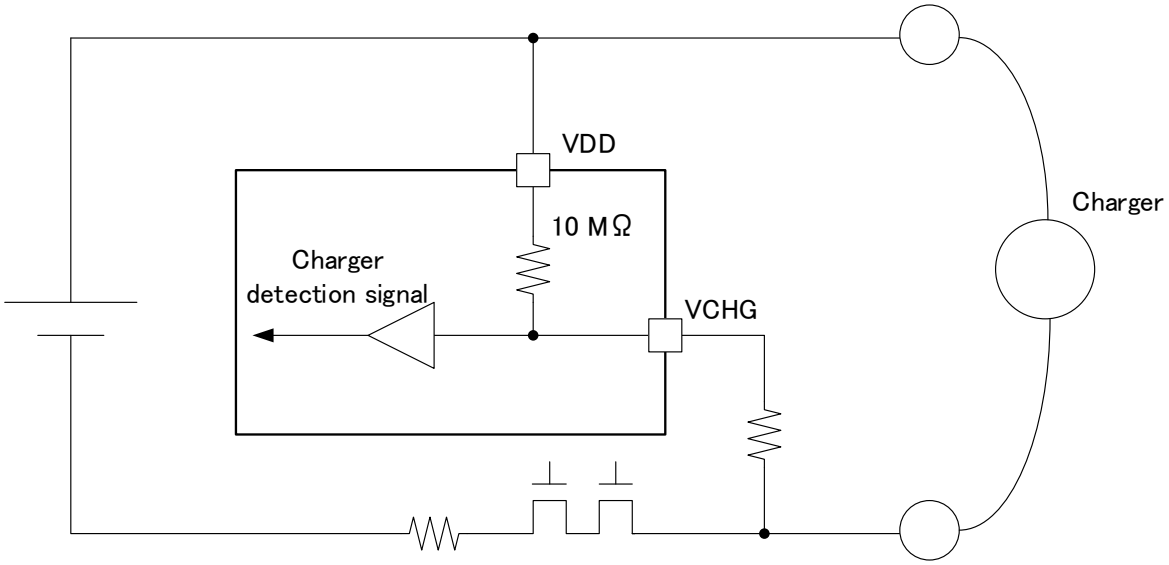
Figure 4-8 Battery cell voltage and temperature (AN port voltage) detection circuit block diagram



4.12 Charger Connect Detection Circuit

The VCHG pin detects the falling edge of the node voltage and assert the charger detection interrupt.

Figure 4-9 Charger Connect detection circuit block diagram



CHAPTER 5. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

5.1 Absolute Maximum Ratings

Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	VDD	VDD		-0.5 to +6.5	V
	GND	VSS		-0.5 to 0.3	V
Input voltage	V_{I1}	P00, P01/P02, P40 /TOOL0, P137		-0.3 to (VDD+0.3) Note 1	V
	V_{I2} Note2	P60/SCL P61/SDA P62		-0.3 to +6.5	V
	V_{I3}	VCHG		VDD-6.5 to VDD+0.3	V
	V_{IN-L}	AN0, ISENS0, ISENS1		-0.3 to +2.0	V
	V_{IN-H}	VBAT		VDD-0.3 to VDD+0.3	V
Output voltage	V_{O1}	P00, P01/P02, P40/TOOL0, DFOUT		-0.3 to (VDD +0.3) Note 1	V
	V_{O2} Note2	P60/SCL, P61/SDA, P62		-0.3 to 6.5	V
	V_{O3} Note2	CFOUT		-0.3 to (VDD +0.3) Note 1	V
High-level output current	I_{OH}	Per pin	P00, P01/P02, P40/TOOL0, CFOUT Note2, DFOUT	-40	mA
		Total of all pins	P00, P01/P02, P40/TOOL0 CFOUT Note2, DFOUT	-70	mA
Low-level output current	I_{OL}	Per pin	P00, P01/P02, P40/TOOL0, CFOUT Note2, DFOUT, P60/SCL Note2, P61/SDA Note2, P62 Note2	+40	mA
		Total of all pins	P00, P01/P02, P40/TOOL0, CFOUT Note2, DFOUT, P60/SCL Note2, P61/SDA Note2, P62 Note2	+70	mA
Operating ambient Temperature	T_A			-40 to +85	°C
Storage temperature	T_{stg}			-65 to +150	°C

Note 1. Must be 6.5 V or lower.

Note 2. GND level is VCHG pin voltage.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. VSS: Reference voltage.

5.2 Power supply voltage condition

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VDD		2.0	-	5.5	V
	GND	VSS	-	0.0	-	V

5.3 Supply current characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Shutdown mode current	I_{SDL}	VDD ≤ 2.0 V VCHG = VDD	-	0.1	1.0	uA
Sleep mode current 1	I_{SLP1}	MCU operation mode: STOP mode AFE operation mode: Low Power Operation Mode 2 (AOCO, ALOCO = OFF) CD (SCD, DOCP) = ON CD (COCP, CWU, DWU) = OFF CC = OFF AD = OFF UVP = ON OVP = OFF CFET = ON, DFET = ON	-	10.0	15.0	uA
<R> Sleep mode current 2	I_{SLP2}	MCU operation mode: STOP mode AFE operation mode: Normal Operation Mode (AOCO, ALOCO = ON) CD = ALL ON CC = ON AD = ON UVP = ON OVP = ON CFET = ON, DFET = ON	-	320	-	uA
<R> Normal mode current	I_{NOM}	MCU operation mode: LS (Low-Speed main) mode, f_{HOCO} = 8 MHz AFE operation mode: Normal Operation Mode (AOCO, ALOCO = ON) CD = ALL ON AD = ON CC = ON UVP = ON OVP = ON CFET = ON, DFET = ON	-	2.0	3.0	mA

Caution After trimming.

5.4 Oscillator Characteristics

5.4.1 On-chip oscillator characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1, 2	f_{IH}		1	-	8	MHz
High-speed on-chip oscillator clock frequency accuracy			-1.5	-	+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}		-	15	-	kHz
Low-speed on-chip oscillator clock frequency accuracy			-15	-	+15	%
AFE on-chip oscillator clock frequency	f_{IAH}		-	2.097	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	2	%
AFE on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us
AFE Low-speed on-chip oscillator clock frequency	f_{IAL}		-	131.072	-	kHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%
AFE Low-speed on-chip oscillator clock frequency stabilization wait time			-	-	(50)	us

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

Caution After trimming.

Remark Values in parentheses are design value.

5.5 Pin characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH1}	P00, P01/P02, P40/TOOL0, CFOUT Note4, DFOUT	2.0 V ≤ VDD ≤ 5.5 V	-	-	-10.0 Note 2	mA
		Total of P00, P01/P02, P40/TOOL0, CFOUT Note4, DFOUT (When duty ≤ 70 % Note 3)	4.0 V ≤ VDD ≤ 5.5 V	-	-	-55.0	mA
			2.7 V ≤ VDD < 4.0 V	-	-	-10.0	mA
			2.0 V ≤ VDD < 2.7 V	-	-	-5	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the VDD pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70 %.

The output current value that has changed to the duty factor > 70 % the duty ratio can be calculated with the following expression (when changing the duty factor from 70 % to n %).

• Total output current of pins = (I_{OH} × 0.7)/(n × 0.01)

<Example> Where n = 80 % and I_{OH} = -10.0 mA

Total output current of pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.

A current higher than the absolute maximum rating must not flow into one pin.

Note 4. GND level is VCHG.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL1}	Per pin for P00, P01/P02, P40 CFOUT Note 4, DFOUT		-	-	20.0 Note 2	mA
		Per pin for P60-P62		-	-	15.0 Note 2	mA
		Total of P00, P01/P02, P40	4.0 V ≤ VDD ≤ 5.5 V	-	-	70.0	mA
		P60/SCL Note 4	2.7 V ≤ VDD < 4.0 V	-	-	15.0	mA
		P61/SDA Note 4 P62 Note 4 CFOUT Note 4 DFOUT (When duty ≤ 70 % Note 3)	2.0 V ≤ VDD < 2.7 V	-	-	9.0	mA
		Total of all pins (When duty ≤ 70 % Note 3)		-	-	150.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification under conditions where the duty factor ≤ 70 %.
The output current value that has changed to the duty factor > 70 % the duty ratio can be calculated with the following expression (when changing the duty factor from 70 % to n %).

• Total output current of pins = (IOL × 0.7) / (n × 0.01)

<Example> Where n = 80 % and IOL = 10.0 mA
Total output current of pins = (10.0 × 0.7) / (80 × 0.01) ≈ 8.7 mA

However, the current that is allowed to flow into one pin does not vary depending on the duty factor.
A current higher than the absolute maximum rating must not flow into one pin.

Note 4. GND level is VCHG.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/5)

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P00, P01/P02, P40/TOOL0	Normal input buffer	0.8 VDD	-	VDD	V
	V_{IH2}	P60 to P62 (TTL input buffer)		1.26 Note	-	VDD	V
	V_{IH3}	P137		0.8 VDD	-	VDD	V
Input voltage, low	V_{IL1}	P00, P01/P02, P40/TOOL0	Normal input buffer	-		0.2 VDD	V
	V_{IL2}	P60 to P62 (TTL input buffer)		0	-	0.54 Note	V
	V_{IL3}	P137		0	-	0.2 VDD	V

Note GND level is VCHG.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. Values in parentheses are design value.

(4/5)

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	P00, P01/P02, P40 CFOUT Note DFOUT	4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -10.0 mA	VDD - 1.5	-	-	V
			4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA	VDD - 0.7	-	-	V
			2.0 V ≤ VDD ≤ 5.5 V, IOH1 = -1.5 mA	VDD - 0.5	-	-	V
Output voltage, low	V_{OL1}	P00, P01/P02, P40 CFOUT Note DFOUT	4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 20.0 mA	-	-	1.3	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA	-	-	0.7	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA	-	-	0.6	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA	-	-	0.4	V
			2.0 V ≤ VDD ≤ 5.5 V, IOL1 = 0.6 mA	-	-	0.4	V
	V_{OL2}	P60 to P62	4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 15.0 mA	-	-	2.0	V
			4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 5.0 mA	-	-	0.4	V
			2.7 V ≤ VDD ≤ 5.5 V, IOL2 = 3.0 mA	-	-	0.4	V
			2.0 V ≤ VDD ≤ 5.5 V, IOL2 = 2.0 mA	-	-	0.2	V

Note GND level is VCHG and VCHG external resistor is 0 Ω.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH1}	P00, P01/P02, P40	VI = VDD	-	-	1	uA
	I_{LIH2}	P137	VI = VDD	-	-	1	uA
	I_{LIH3}	P60 to P62	VI = VDD	-	-	8	uA
Input leakage current, low	I_{LIL1}	P00, P40	VI = VSS	-	-	-1	uA
	I_{LIL2}	P137	VI = VSS	-	-	-1	uA
	I_{LIL3}	P60 to P62	VI = VSS = VCHG	-	-	-1	uA
	I_{LIL4}	P01/P02	VI = VSS	-	-	-7	uA
On-chip pull-up resistance	R_{U1}	P40		10	20	100	kΩ
	R_{UA}	AN0		7.5	10	12.5	kΩ
	R_{U2}	P01/P02		0.8	1	1.2	MΩ

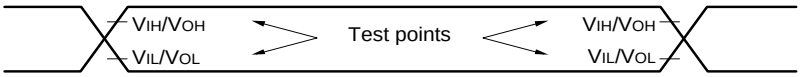
Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

5.6 AC Characteristics

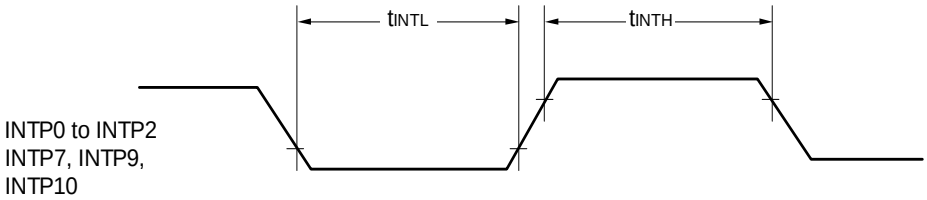
(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	LS (low-speed main) mode	0.125	-	1	us
		In the self-programming mode	LS (low-speed main) mode	0.125	-	1	us
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0 to INTP2 INTP7, INTP9, INTP10	2.0 V ≤ VDD ≤ 5.5 V	1	-	-	us

AC Timing Test Points

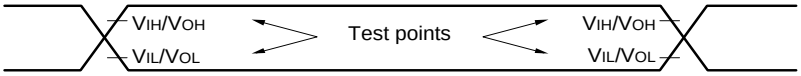


Interrupt Request Input Timing



5.7 Peripheral circuit characteristics

AC Timing Test Points



5.7.1 Serial array unit

(1) During communication at same potential (UART mode)

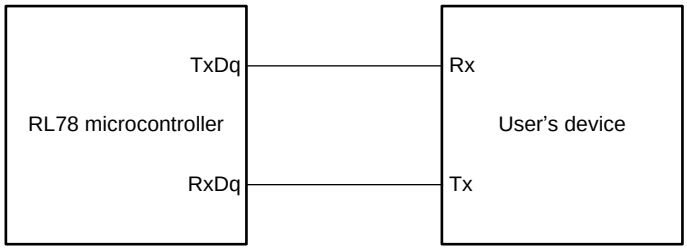
(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	LS (low-speed main) mode		Unit
			MIN.	MAX.	
Transfer rate Note			-	f_{MCK}/6	bps
		Theoretical value of the maximum transfer rate $f_{MCK} = f_{CLK}$	-	1.3	Mbps

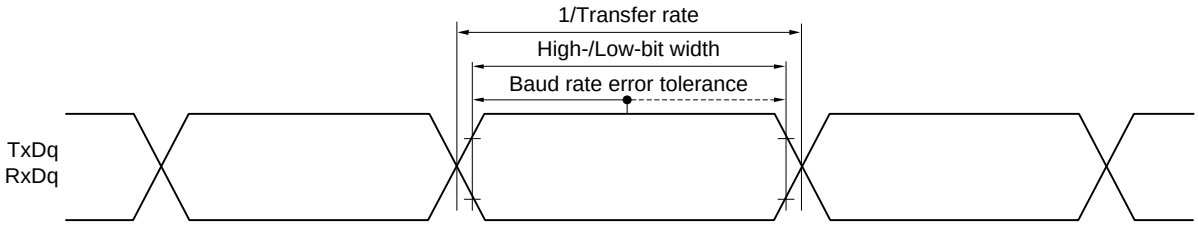
Note Transfer rate in the SNOOZE mode is only 4800 bps.

Caution Select the normal input buffer for the RXDq pin and normal output mode for the TXDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

UART mode connection diagram (during communication at same potential)



UART mode bit width (during communication at same potential) (reference)



Remark 1. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 5, 14)

Remark 2. f_{MCK}: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13))

(2) During communication at same potential (simplified I²C mode)

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

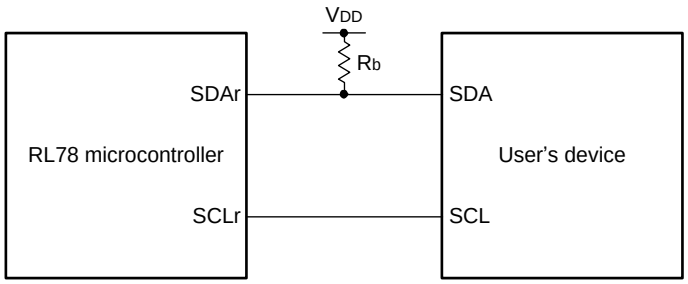
Parameter	Symbol	Conditions	LS (low-speed main) mode		Unit
			MIN.	MAX.	
SCLr clock frequency	f_{SCL}	2.0 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	-	400 Note 1	kHz
Hold time when SCLr = "L"	t_{LOW}	2.0 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1150	-	ns
Hold time when SCLr = "H"	t_{HIGH}	2.0 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	1150	-	ns
Data setup time (reception)	$t_{SU: DAT}$	2.0 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	$1/f_{MCK}$ + 145 Note 2	-	ns
Data hold time (transmission)	$t_{HD: DAT}$	2.0 V ≤ VDD ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	0	305	ns

Note 1. The value must also be equal to or less than f_{MCK}/4.

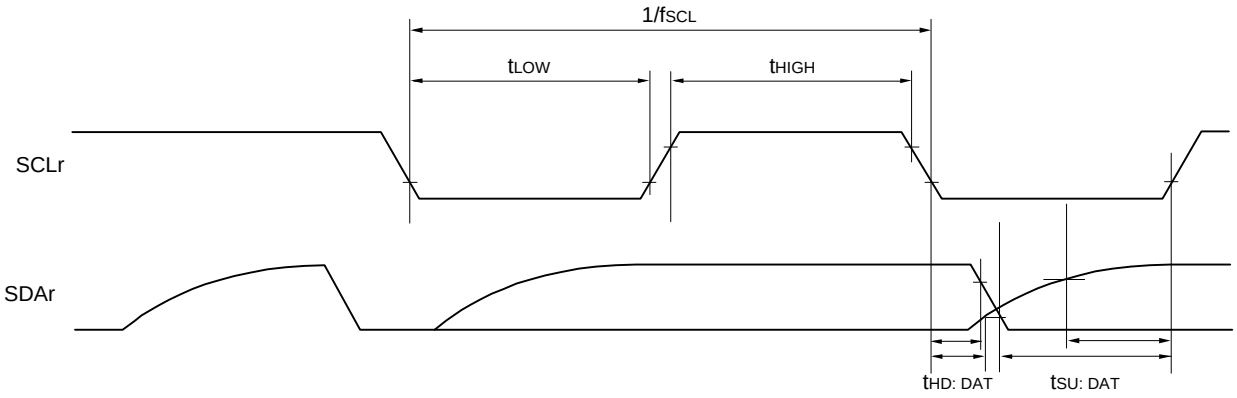
Note 2. Set the f_{MCK} value not to over the hold time of SCLr = "L" and SCLr = "H".

Caution Select the normal input buffer and the N-ch open-drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)



Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 10), g: PIM number (g = 10, 13), h: POM number (h = 11, 14)

Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), mn = 00 to 03, 10 to 13)

5.7.2 Serial interface IICA

(1) I^2C standard mode

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	LS (low-speed main) mode		Unit
			MIN.	MAX.	
SCL clock frequency	f_{SCL}	Standard mode: f_{CLK} ≥ 1 MHz	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7	-	us
Hold time Note 1	$t_{HD: STA}$		4.0	-	us
Hold time when SCL = “L”	t_{LOW}		4.7	-	us
Hold time when SCL = “H”	t_{HIGH}		4.0	-	us
Data setup time (reception)	$t_{SU: DAT}$		250	-	ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	us
Setup time of stop condition	$t_{SU: STO}$		4.0	-	us
Bus-free time	t_{BUF}		4.7	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

(2) I^2C fast mode

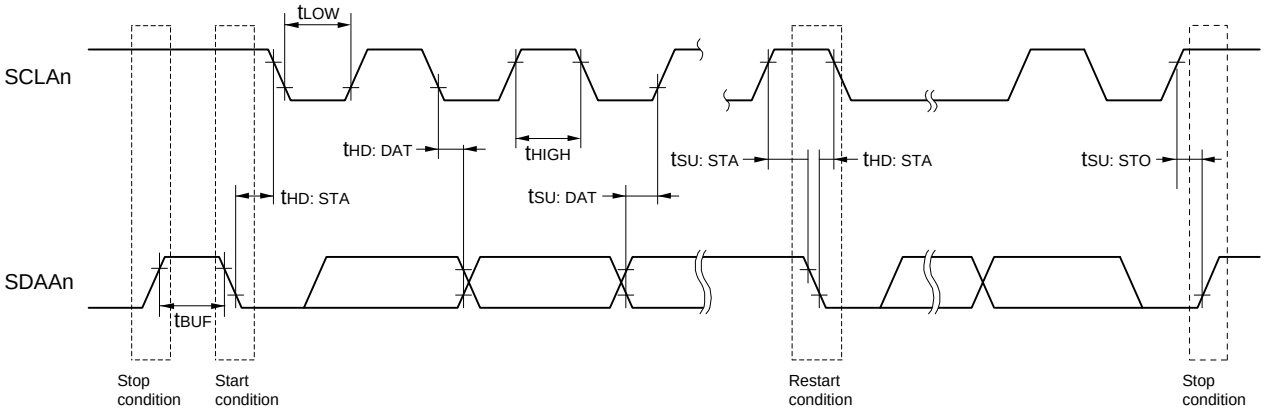
(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	LS (low-speed main) mode		Unit
			MIN.	MAX.	
SCL clock frequency	f_{SCL}	Fast mode: $f_{CLK} \geq 3.5$ MHz	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$		0.6	-	us
Hold time[Note1]	$t_{HD: STA}$		0.6	-	us
Hold time when SCL = “L”	t_{LOW}		1.3	-	us
Hold time when SCL = “H”	t_{HIGH}		0.6	-	us
Data setup time (reception)	$t_{SU: DAT}$		100	-	ns
Data hold time (transmission) [Note2]	$t_{HD: DAT}$		0	0.9	us
Setup time of stop condition	$t_{SU: STO}$		0.6	-	us
Bus-free time	t_{BUF}		1.3	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

IICA serial transfer timing



Remark n = 0

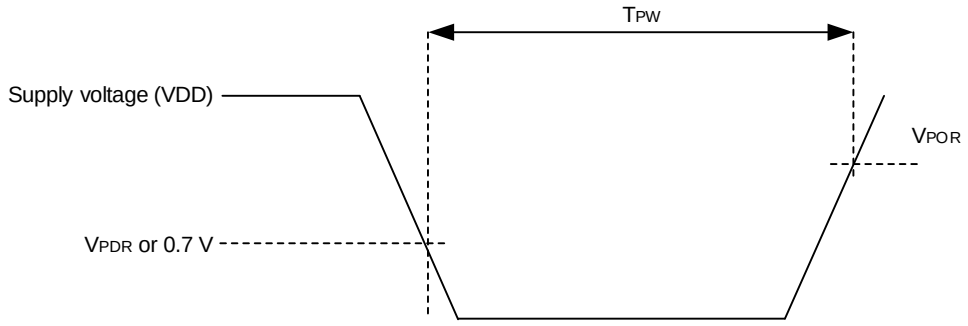
5.7.3 POR circuit characteristics

(T_A = -40 to +85 °C, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on VDD rising	1.47	1.51	1.55	V
	V_{PDR}	Voltage threshold on VDD falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW}		300	-	-	us

Note 1. However, when the operating voltage falls while the LVD is off, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in 5.6 AC Characteristics.

Note 2. Minimum time required for a POR reset when VDD is below VPDR. This is also the minimum time required for a POR reset when VDD exceeds VPOR after VDD is below 0.7 V during STOP mode or while the main system clock is stopped by setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



5.7.4 LVD circuit characteristics

Reset Mode

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter		Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Voltage detection threshold	Supply voltage level	V_{LVI0}	Power supply rise time	3.98	4.06	4.14	V
			Power supply fall time	3.90	3.98	4.06	V
		V_{LVI1}	Power supply rise time	3.68	3.75	3.82	V
			Power supply fall time	3.60	3.67	3.74	V
		V_{LVI2}	Power supply rise time	3.07	3.13	3.19	V
			Power supply fall time	3.00	3.06	3.12	V
		V_{LVI3}	Power supply rise time	2.96	3.02	3.08	V
			Power supply fall time	2.90	2.96	3.02	V
		V_{LVI4}	Power supply rise time	2.86	2.92	2.97	V
			Power supply fall time	2.80	2.86	2.91	V
		V_{LVI5}	Power supply rise time	2.76	2.81	2.87	V
			Power supply fall time	2.70	2.75	2.81	V
		V_{LVI6}	Power supply rise time	2.66	2.71	2.76	V
			Power supply fall time	2.60	2.65	2.70	V
		V_{LVI7}	Power supply rise time	2.56	2.61	2.66	V
			Power supply fall time	2.50	2.55	2.60	V
		V_{LVI8}	Power supply rise time	2.45	2.50	2.55	V
			Power supply fall time	2.40	2.45	2.50	V
		V_{LVI9}	Power supply rise time	2.05	2.09	2.13	V
			Power supply fall time	2.00	2.04	2.08	V
Minimum pulse width		t_{LW}		300	-	-	us
Detection delay time		t_{LD}		-	-	300	us

5.7.5 Sigma-delta A/D converter characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution Note1	RESAD	Conversion time = 64 ms	-	-	18	bit
		Conversion time = 32 ms	-	-	17	bit
		Conversion time = 16 ms	-	-	16	bit
		Conversion time = 8 ms	-	-	15	bit
		Conversion time = 4 ms	-	-	14	bit
		Conversion time = 2 ms	-	-	13	bit
		Conversion time = 1 ms	-	-	12	bit
		Conversion time = 0.5 ms	-	-	11	bit
		Conversion time = 0.25 ms	-	-	10	bit
Input voltage range	VINAD		-0.1	-	5.1	V
Input voltage range VBAT	VRA1		2.0	-	5.1	V
Input voltage range AN0	VRA2		0.0	-	1.72	V
Integral nonlinearity	INLAD	15-bit resolution End fit	-27	-	27	LSB
Conversion result in zero input	ADZERO	VIN = 0 V 15-bit resolution	-	3240 Note 2	-	LSB
Temperature dependency In zero input	dTADZERO	VIN = 0 V 15-bit resolution	-0.24	-	+0.24	LSB/°C
Conversion result in full-scale input	ADFS	VIN = 5.1 V 15-bit resolution	-	30964 Note 2	-	LSB
Temperature dependency in full-scale input	dTADFS	VIN = 5.1 V 15-bit resolution	-0.24	-	+0.24	LSB/°C
Input resistance	RINAD		-	(1.0)	-	MΩ
During cell voltage measurement error	ERRCELL1	T_A = +25 °C After calibration 2.5 V ≤ VDD = VBAT ≤ 5.0 V	-	-	(±5)	mV
	ERRCELL2	T_A = -25 to +85 °C After calibration 2.5 V ≤ VDD = VBAT ≤ 5.0 V	-	-	(±10)	mV

Note 1. AD conversion result is output in 18 bits.

Note 2. This value is before subtracting the offset voltage.

Caution 1. Except for During cell voltage measurement error (ERRCELL), these parameters are sigma-delta A/D converter circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in parentheses are design value.

5.7.6 On-chip simple temperature sensor

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Temperature coefficient	FVTMPS	Temperature sensor that depends on the temperature	-	-1.6	-	mV/°C

5.7.7 Current integration circuit characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC		-	18	-	bit
Conversion time	TCC		250	1000	4000	ms
Input voltage range	VINCC	ISENS1 to ISENS0	-50	-	+50	mV
Integral nonlinearity	INLCC	End fit	-	-	0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1	-	(1.0)	-	MΩ
Current measurement error	ERRCURR	After calibration -25 °C ≤ T_A ≤ 85 °C 2.5 V ≤ VDD ≤ 5.0 V	-	-	(±50)	uV

Caution 1. Except for Current measurement error (ERRCURR), these parameters are current integration circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in parentheses are design value.

5.7.8 Overcurrent detection / wakeup current detection circuit characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection setting voltage step	dSVSC	24 mV to 240 mV	-	12	-	mV
Discharge short-circuit current detection voltage error	dVSC	24 mV to 240 mV	-	-	±12	mV
Discharge overcurrent detection setting voltage step	dSVDOC	3 mV to 31.2 mV	-	0.3	-	mV
Discharge overcurrent detection voltage error Note 1	dVDOC	3 mV to 31.2 mV	-	-	±1	mV
Charge overcurrent detection setting voltage step	dSVCOC	-3 mV to -25.2 mV	-	0.3	-	mV
Charge overcurrent detection voltage error Note 1	dVCOC	-3 mV to -25.2 mV	-	-	±1	mV
Discharge wakeup current detection setting voltage step	dSVDWU	3 mV to 31.2 mV	-	0.3	-	mV
Discharge wakeup current detection voltage error Note 1	dVDWU	3 mV to 31.2 mV	-	-	±1	mV
Charge wakeup current detection setting voltage step	dSVCWU	-31.2 mV to -3 mV	-	0.3	-	mV
Charge wakeup current detection voltage error Note 1	dVCWU	-31.2 mV to -3 mV	-	-	±1	mV
Discharge short-circuit current detection time error Note 4	dTSC	AOCO, ALOCO 0 us to 916 us (61 us step)	-	-	30.5	us
		LOCO 0 us to 1005 us (67 us step)	-	-	67	us
Discharge overcurrent detection time error Note 4	dTDOC	AOCO, ALOCO 0.122 ms to 31.25 ms Note 3 (0.122 ms step)	-	-	30.5	us
		LOCO 0.266 ms to 34.1 ms (0.133 ms step)	-	-	67	us
Charge overcurrent detection time error Note 2	dTCOC	0.122 ms to 31.25 ms (0.122 ms step)	-	-	30.5	us
Discharge wakeup current detection time error Note 2	dTDWU	3.91 ms to 62.56 ms (3.91 ms step)	-	-	3.91	ms
Charge wakeup current detection time Error Note 2, 4	dTCWU	AOCO, ALOCO, LOCO 3.91 ms to 62.56 ms (3.91 ms step)	-	-	3.91	ms

Note 1. This is the specification after zero-calibration is executed.

Note 2. These values are when AOCO and ALOCO are selected.

Note 3. These ranges and steps are added 9% when using fil clock.

Note 4. The frequency error of AFE On-chip oscillator (AOCO and ALOCO) and MCU On-chip oscillator (LOCO) are excluded from these detection time error.

5.7.9 Overvoltage / Undervoltage detection circuit characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Under voltage detection range	VUVP	50 mV step	2200	2500	3000	mV
Under voltage detection accuracy	VUVP_ACC	T_A = 25 °C 2500 mV setting	-50	-	+50	mV
<R>		T_A = -40 to +85 °C	-100	-	+100	mV
Under voltage release hysteresis voltage	VUVP_HYS	100 mV step	100	-	500	mV
Under voltage detection delay	tUVP		-	20	-	ms
			-	96	-	ms
			-	128	-	ms
			-	144	-	ms
Under voltage release delay	tUVP_REL	Auto release function	-	1	-	ms
Over voltage detection range	VOVP	5 mV step	4300	4460	4800	mV
Over voltage detection accuracy	VOVP_ACC	T_A = 25 °C 4460 mV setting	-10	-	10	mV
		T_A = -40 to +85 °C	-50	-	50	mV
Over voltage release hysteresis voltage	VOVP_HYS	100 mV step	100	-	400	mV
Over voltage detection delay	tOVP		-	400	-	ms
			-	600	-	ms
			-	800	-	ms
			-	1000	-	ms
Over voltage release delay	tOVP_REL	Auto release function	-	8	-	ms

5.7.10 Charger connect detection circuit characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

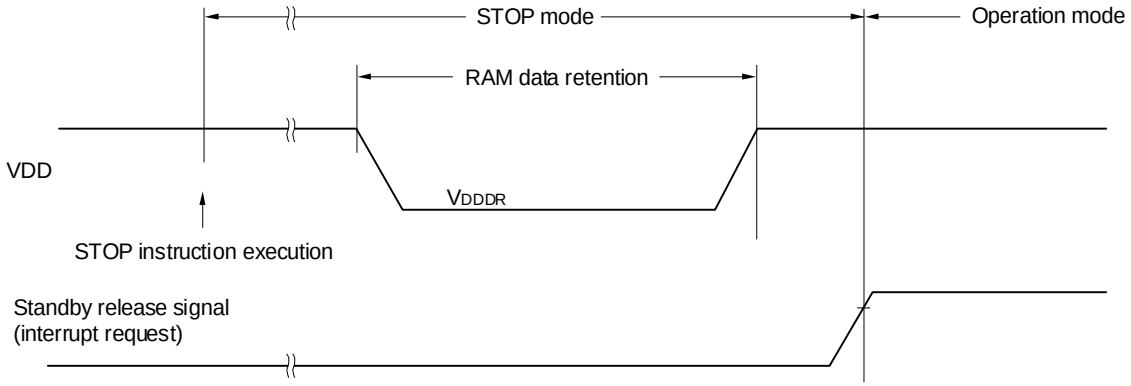
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Charger detection voltage	VCHG_DET		VDD - 1.5	VDD - 1.1	VDD -0.5	V
Internal resistance	RCHG		-	10	-	MΩ

5.8 RAM Data Retention Characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note	-	5.5	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



5.9 Flash Memory Programming Characteristics

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
System clock frequency	f_{CLK}		1	-	8	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85 °C	1,000	-	-	Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year T_A = 25 °C	-	1,000,000	-	
		Retained for 5 years T_A = 85 °C	100,000	-	-	
		Retained for 20 years T_A = 85 °C	10,000	-	-	

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

5.10 Dedicated Flash Memory Programmer Communication

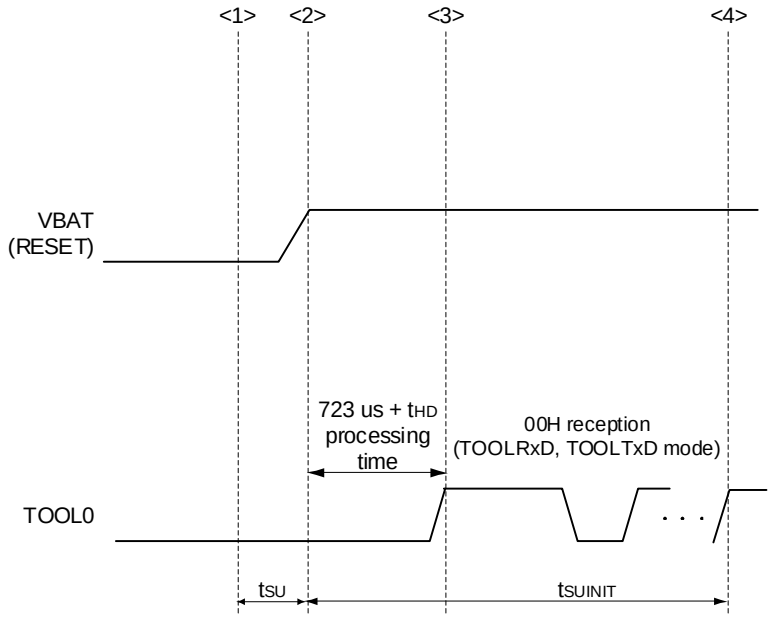
(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200	-	1,000,000	bps

5.11 Timing of Entry to Flash Memory Programming Modes

(T_A = -40 to +85 °C, 2.0 V ≤ VDD ≤ 5.5 V, VSS = VCHG = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
How long from when an external reset ends until the initial communication settings are specified	t_{SUINIT}	POR and LVD reset must end before the external reset ends.	-	-	100	ms
How long from when the TOOL0 pin is placed at the low level until an external reset end	t_{SU}	POR and LVD reset must end before the external reset ends.	10	-	-	us
How long the TOOL0 pin must be kept at the low level after an external reset end (excluding the processing time of the firmware to control the flash memory)	t_{HD}	POR and LVD reset must end before the external reset ends.	1	-	-	ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by TOOL0 pin and complete the baud rate setting.

Remark tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tSU: How long from when the TOOL0 pin is placed at the low level until a pin reset ends

tHD: How long to keep the TOOL0 pin at the low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

CHAPTER 6. PACKAGE OUTLINE

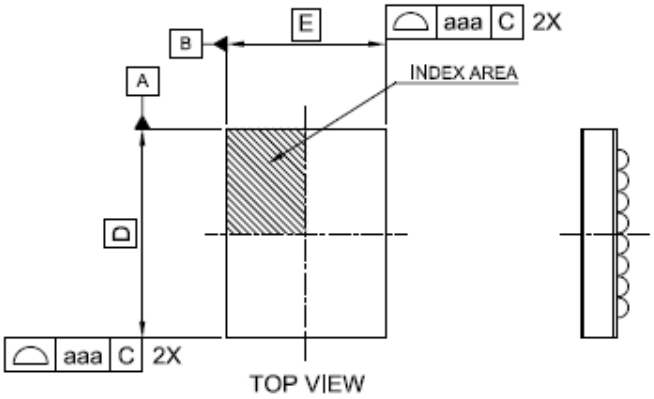
6.1 PACKAGE OUTLINE

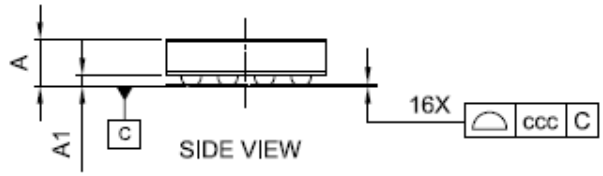
Caution This product has some assembly sites.

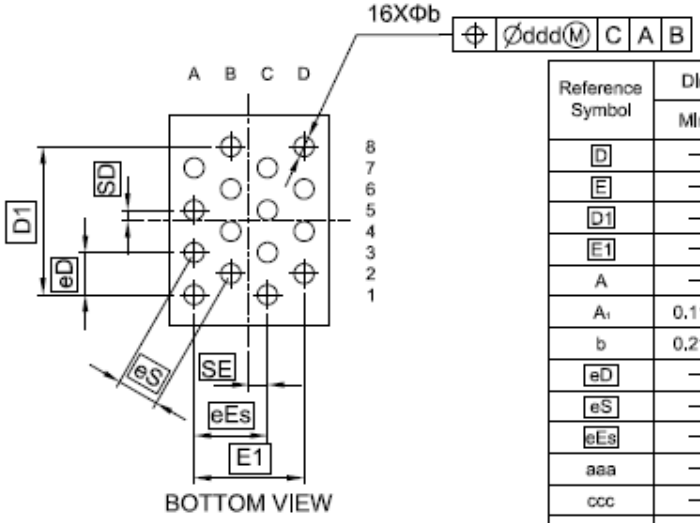
[FAB A]

外形図 Outline drawing Renesasコード SUBG0016KB-A	RDK-G-001504 1/1 ルネサスエレクトロニクス株式会社 Renesas Electronics Corporation

JEITA Package code	RENESAS code	MASS(TYP.)[g]
S-UFBGA16-1.871x2.478-0.50	SUBG0016KB-A	0.01





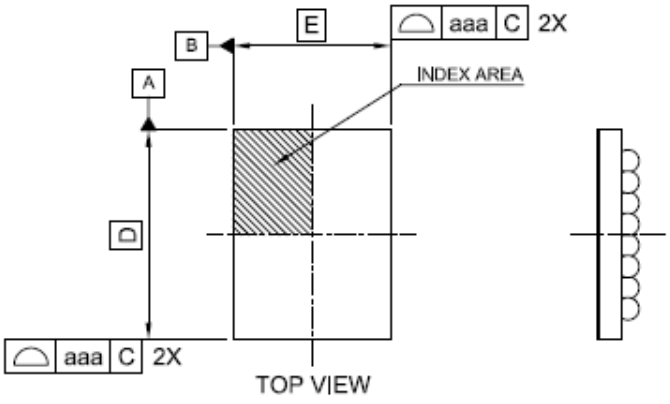


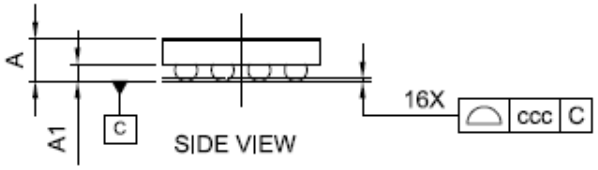
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	2.478	—
E	—	1.871	—
D1	—	1.750	—
E1	—	1.299	—
A	—	—	0.600
A_1	0.115	0.135	0.155
b	0.210	0.235	0.260
eD	—	0.500	—
eS	—	0.500	—
eEs	—	0.866	—
aaa	—	—	0.050
ccc	—	—	0.050
ddd	—	—	0.050
SD	—	0.125	—
SE	—	0.217	—

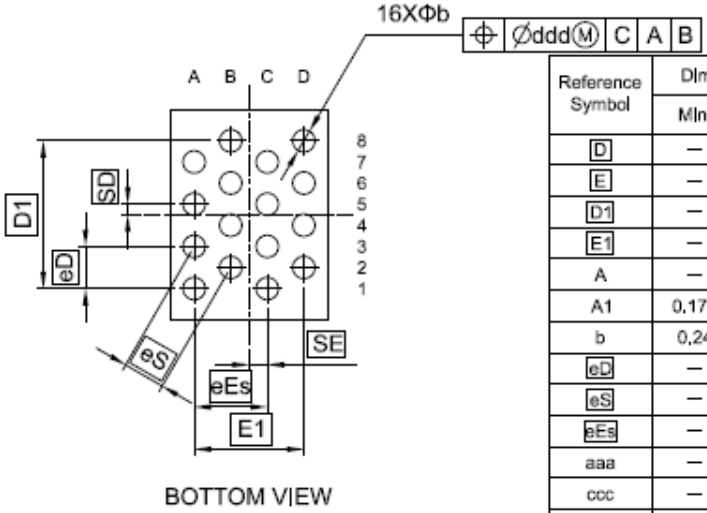
[FAB B]

外形図 Outline drawing Renesasコード SUBG0016KC-A	RDK-G-001610 1/1 ルネサスエレクトロニクス株式会社 Renesas Electronics Corporation

JEITA Package code	RENESAS code	MASS(TYP.)[g]
S-UFBGA16-1.871x2.478-0.50	SUBG0016KC-A	0.01



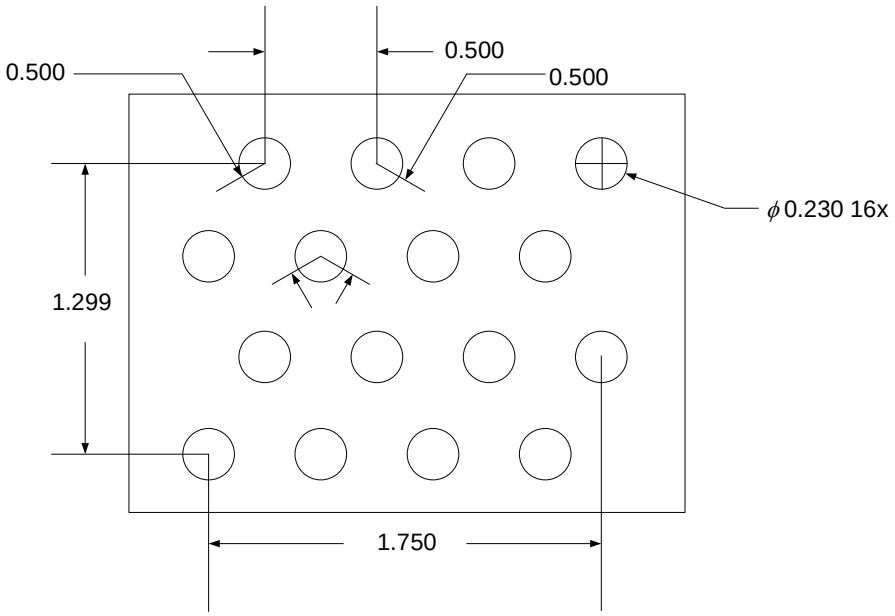




Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	2.478	—
E	—	1.871	—
D1	—	1.750	—
E1	—	1.299	—
A	—	—	0.55
A1	0.175	0.20	0.225
b	0.24	0.265	0.29
eD	—	0.50	—
eS	—	0.50	—
eEs	—	0.866	—
aaa	—	—	0.05
ccc	—	—	0.05
ddd	—	—	0.05
SD	—	0.125	—
SE	—	0.217	—

6.2 Recommended Land Pattern Dimension

[FAB A] [FAB B]



Note 1. All dimensions are in mm, angle in degrees.

Note 2. Top down view, as view on PCB.

REVISION HISTORY

Rev.	Date	Page	Description
1.00	Jun. 15, 2021		First release
1.01	Jul. 08, 2021	Chapter 5. ELECTRICAL SPECIFICATION	
		p.32	Updated description for 5.5 Pin characteristics
		p.41	Updated condition for 5.7.5 Sigma-delta A/D converter characteristics
		p.42	Updated condition for 5.7.7 Current integration circuit characteristics
1.02	Aug. 23, 2022	Chapter 5. ELECTRICAL SPECIFICATION	
		p.28	Updated condition for 5.3 Supply current characteristics (Sleep mode current 2)
		p.28	Updated condition for 5.3 Supply current characteristics (Normal mode current)
		p.44	Added condition of VUVP_ACC for 5.7.9 Overvoltage / Undervoltage detection circuit characteristics

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact information

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