RAA271000

General-Purpose Power Management IC for Automotive Applications

The RAA271000 is a general-purpose Power Management Integrated Circuit (PMIC) suitable for the Renesas R-Car SoC series.

RAA271000 contains five high efficiency DC/DC synchronous buck regulators and two low-dropout linear regulators (LDO).

RAA271000 can support ASIL D system safety goals. It includes independent reference for monitoring of the output voltages, dual internal temperature monitors, challenge-response watchdog timer, SoC error pin monitors, reset generator, a dedicated safety-control state machine, and a safety shutdown path. An integrated 12-bit ADC monitors all input rails, output rails, internal temperature, and includes additional inputs to monitor external analog sources.

RAA271000 is available in a 5.71×8.46, 0.8mm pitch, FCCSP package. The device is offered as AEC-Q100 Grade 1 operation supporting an ambient temperature range of -40°C to 125°C.

Applications

- Automotive vision systems
- Automotive LIDAR systems
- Ideal power supply for the Renesas V3H SoC

Features

- Input range: 2.7V to 5.5V
- Five switching regulators with adjustable output
- V_{OUT} from 0.3V ~ 3.3V at:
  - 15A (Buck 1)
  - 2A (Buck 2-3)
  - 4A (Buck 4-5)
- Two linear regulators
  - Output 0.6V to 3.6V at 300mA (LDO1-2)
- 12-bit analog-to-digital converter for monitoring
- Configurable through I^2C or SPI interface
- Programmable power sequence
- Supports R-Car SoC sequence of activation
- Challenge-response watchdog timer
- Dual thermal protection system
- 60 ball FCCSP package, 0.8mm pitch
- ASIL-D ISO26262 Development Process
- AEC-Q100 qualified (grade 1)

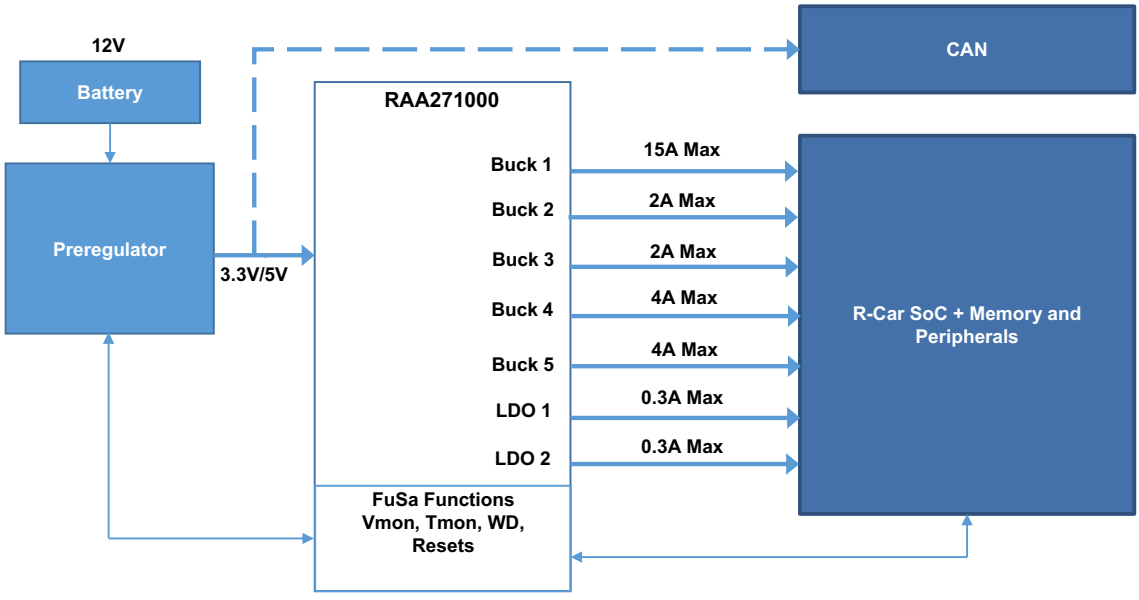


Figure 1. Typical Application Block Diagram

Contents

1. Overview

1.1 Typical Application Diagram

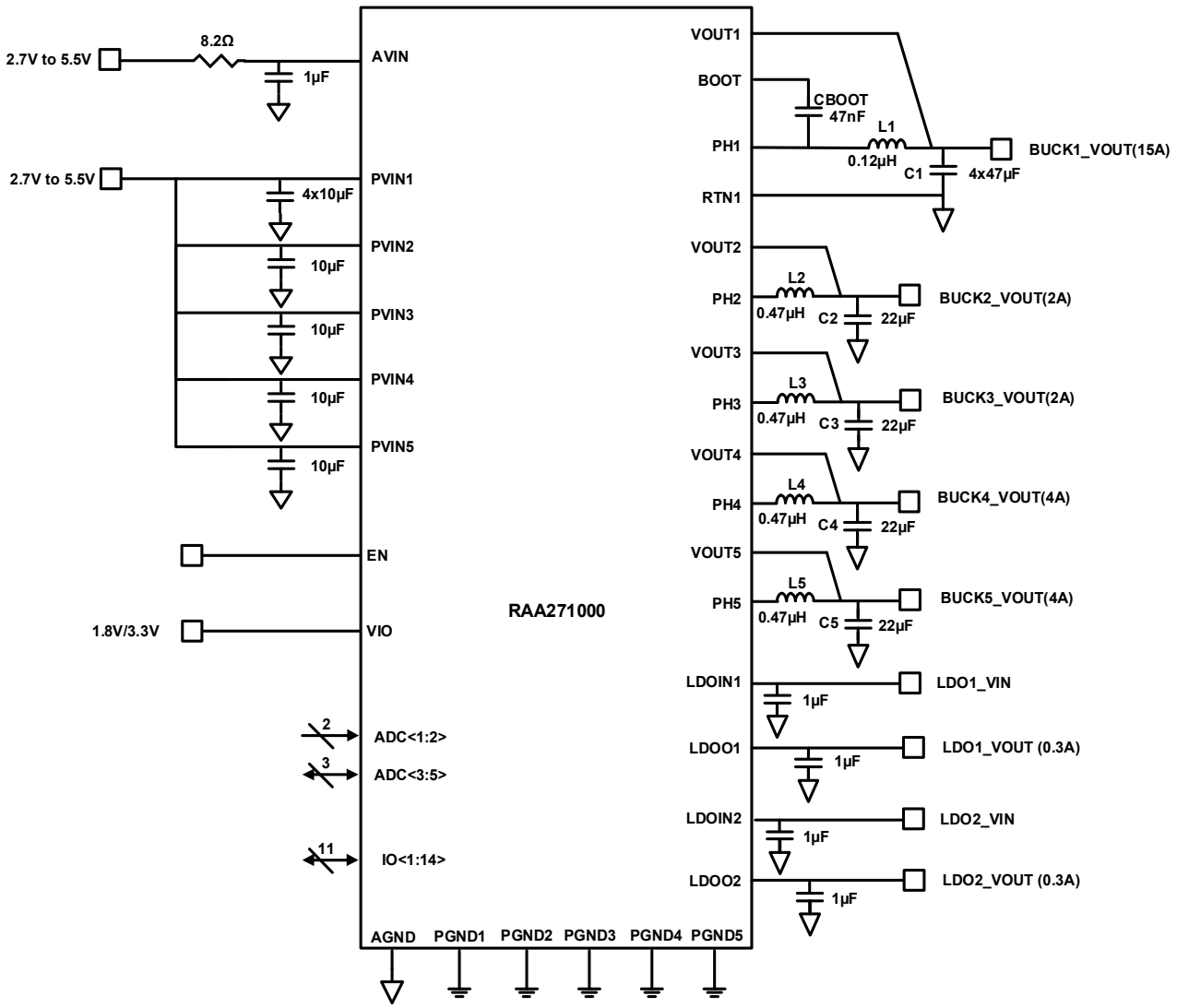


Figure 2. Typical Application Diagram

1.2 Block Diagram

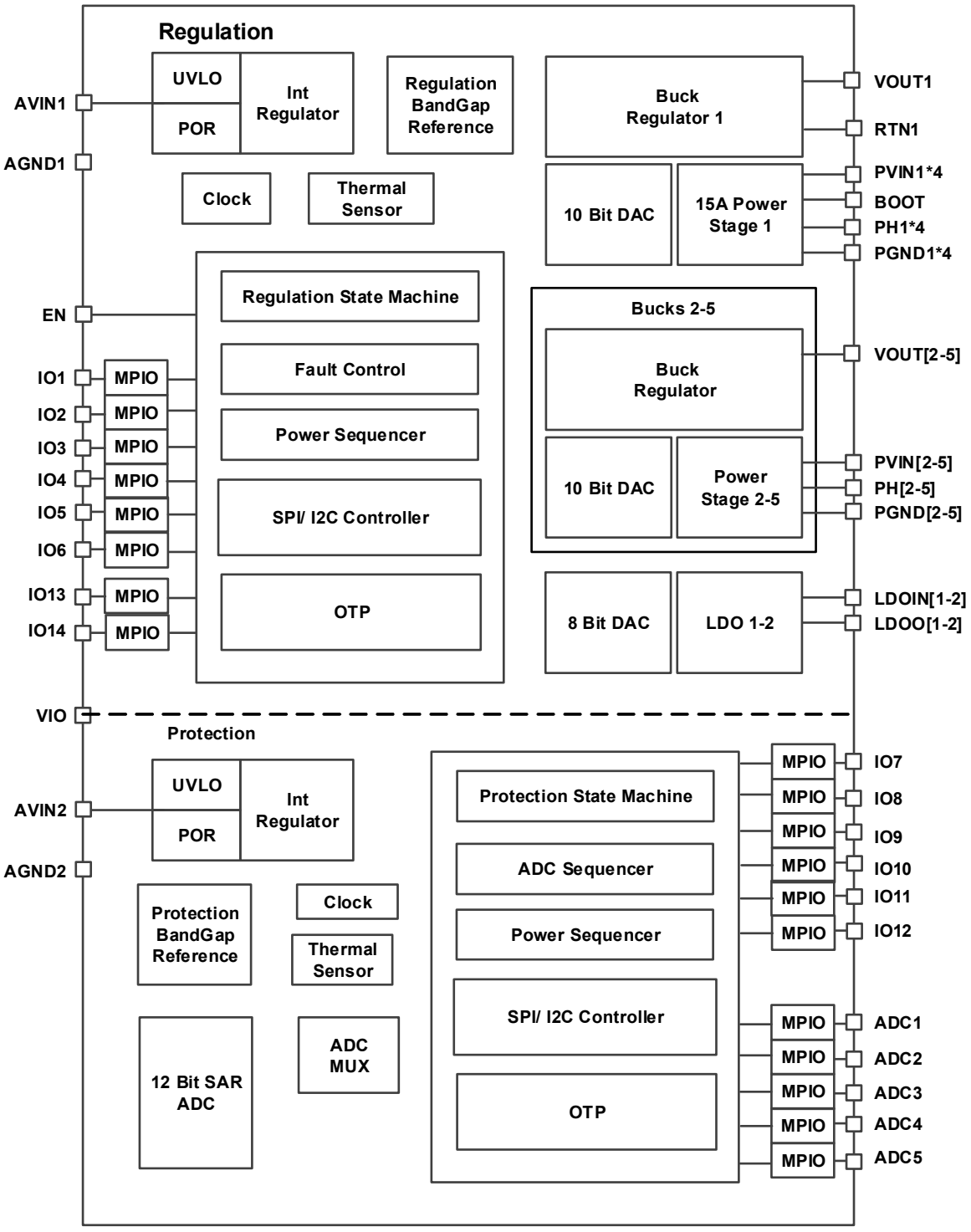
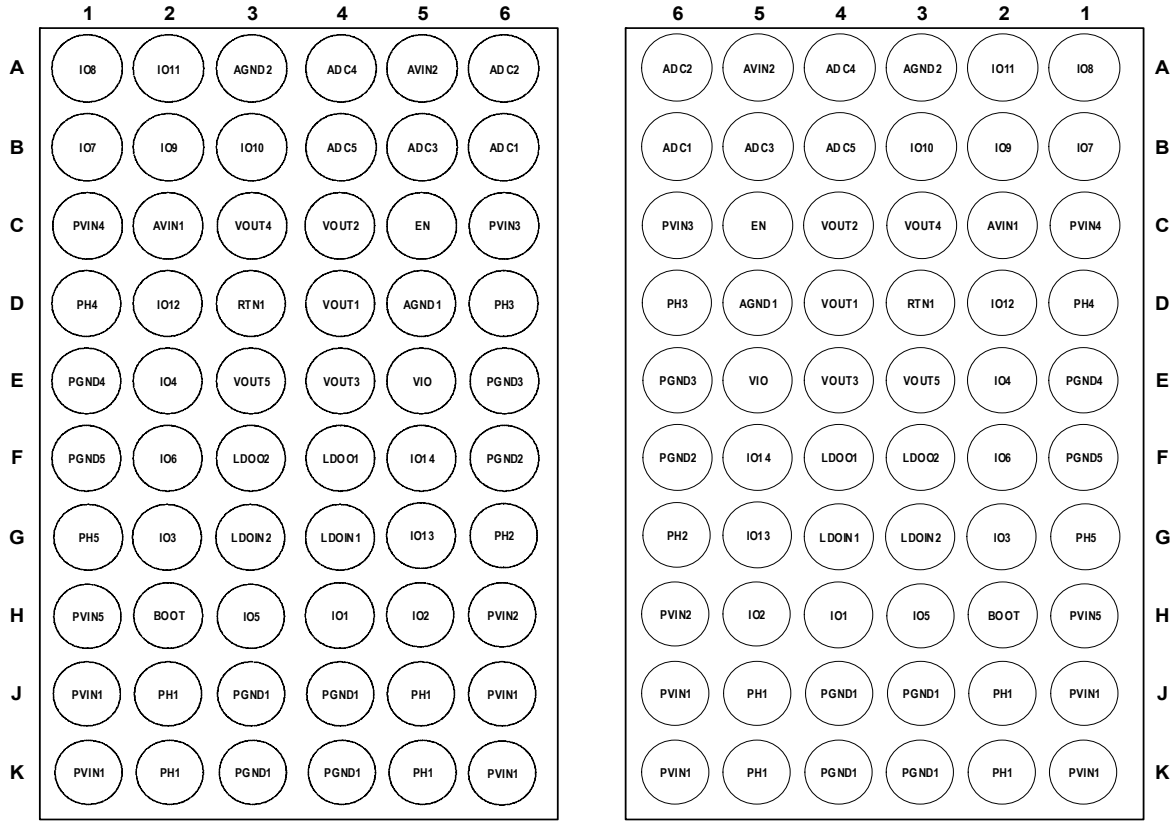


Figure 3. Simplified Block Diagram

2. Pin Information

2.1 Pin Assignments



Device pin out with balls down (left) and balls up (right)

2.2 Pin Descriptions

Pin Number	Pin Name	Type	Description
A1	IO8/PRESET#	Output	Protection state dependent output. Generally starts or resets an SoC.
A2	IO11/PRESET_OUT	Input	Protection interrupt input. Generally checks the status of an SoC.
A3	AGND2	Input	Analog ground 2. Internally connected to AGND1.
A4	ADC4	Input/Output	ADC input or ADC decoder output
A5	AVIN2	Input	Analog supply voltage 2, 2.7V ~ 5.5V. Connect this pin to AVIN1 on the PCB.
A6	ADC2	Input	External ADC input
B1	IO7/FSCLKST#	Input	Protection interrupt input. Generally checks the status of an SoC.
B2	IO9/SDO1	Output	Protection state dependent output 1
B3	IO10/SSP	Output	Protection state dependent output
B4	ADC5	Input/Output	ADC input or ADC decoder output
B5	ADC3	Input/Output	ADC input or ADC decoder output
B6	ADC1	Input	External ADC input
C1	PVIN4	Input	Power supply for Buck 4 power stage

Pin Number	Pin Name	Type	Description
C2	AVIN1	Input	Analog supply voltage 1, 2.7V ~ 5.5V. Connect this pin to AVIN2 on the PCB.
C3	VOUT4	Input	Remote sense of the output voltage of Buck 4
C4	VOUT2	Input	Remote sense of the output voltage of Buck 2
C5	EN	Input	Chip enable
C6	PVIN3	Input	Power supply for Buck 3 power stage
D1	PH4	Output	Switching node for Buck 4 power stage
D2	IO12/SDO2	Output	Protection state dependent output 2
D3	RTN1	Input	Remote ground sense at the load for Buck 1
D4	VOUT1	Input	Remote sense of the output voltage for Buck 1
D5	AGND1	Input	Analog ground 1. Internally connected to AGND2
D6	PH3	Output	Switching node for Buck 3 power stage
E1	PGND4	Input	Ground connection for Buck 4 power stage
E2	IO4	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
E3	VOUT5	Input	Remote sense of the output voltage of Buck 5
E4	VOUT3	Input	Remote sense of the output voltage of Buck 3
E5	VIO	Input	I/O voltage
E6	PGND3	Input	Ground connection for Buck 3 power stage
F1	PGND5	Input	Ground connection for Buck 5 power stage
F2	IO6	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
F3	LDOO2	Output	LDO 2 power output
F4	LDOO1	Output	LDO 1 power output
F5	IO14/FLT#	Output	Fault indication output signal
F6	PGND2	Input	Ground connection for Buck 2 power stage
G1	PH5	Output	Switching node for Buck 5 power stage
G2	IO3	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
G3	LDOIN2	Input	LDO 2 power input
G4	LDOIN1	Input	LDO 1 power input
G5	IO13	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
G6	PH2	Output	Switching node for Buck 2 power stage
H1	PVIN5	Input	Power supply for Buck 5 power stage
H2	BOOT	Input	Supply for boosted gate drive for Buck 1
H3	IO5	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
H4	IO1	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).

Pin Number	Pin Name	Type	Description
H5	IO2	Input/Output	Multi-purpose I/O. The function of this pin depends on the pin mode selected (Table 1).
H6	PVIN2	Input	Power supply for Buck 2 power stage
J1	PVIN1_A	Input	Power supply for Buck 1 power stage
J2	PH1_A	Output	Switching node for Buck 1 power stage
J3	PGND1_A	Input	Ground connection for Buck 1 power stage
J4	PGND1_C	Input	Ground connection for Buck 1 power stage
J5	PH1_C	Output	Switching node for Buck 1 power stage
J6	PVIN1_C	Input	Power supply for Buck 1 power stage
K1	PVIN1_B	Input	Power supply for Buck 1 power stage
K2	PH1_B	Output	Switching node for Buck 1 power stage
K3	PGND1_B	Input	Ground connection for Buck 1 power stage
K4	PGND1_D	Input	Ground connection for Buck 1 power stage
K5	PH1_D	Output	Switching node for Buck 1 power stage
K6	PVIN1_D	Input	Power supply for Buck 1 power stage

2.2.1 I/O Pin Configurations

RAA271000 supports a number of different pin configurations to address different application requirements. The pin mode value is factory programmed.

Table 1. I/O Pin Configurations

Pin Mode	IO1	IO2	IO3	IO4	IO5	IO6	IO7	IO8	IO9	IO10	IO11	IO12	IO13	IO14
0[1]	SSP2	SS_B2	SCK	SS_B	MOSI	MISO	FSCLKST#	PRESET#	SDO1	SSP	PRESET OUT	SDO2	GPIO1	INTb
1[2]	SCL	SDA	DVFS	FSO_CFE_0	FSO_CFE_1	FSO_TOE	FSCLKST#	PRESET#	SDO1	SSP	PRESET OUT	SDO2	GPIO1	INTb
2[3]	SCL	SDA	GPIO1	GPIO2	GPIO3	GPIO4	FSCLKST#	PRESET#	SDO1	SSP	PRESET OUT	SDO2	GPIO5	INTb
3[4]	SCL	SDA	DVFS	GPIO1	INT_REGU	GPIO2	FSCLKST#	PRESET#	SDO1	SSP	PRESET OUT	SDO2	GPIO3	INTb
4[5]	INT_REGU	SS_B2	SCK	SS_B	MOSI	MISO	FSCLKST#	PRESET#	SDO1	SSP	PRESET OUT	SDO2	GPIO1	INTb
5[6]	SCL	SDA	SCK	SS_B	MOSI	MISO	FSCLKST#	PRESET#	SS_B2	SSP	PRESET OUT	SDO2	GPIO1	INTb
6[7]														
7[7]														

1. Application 1: SPI, no FSO pins
2. Application 2: I^2C, FSO pins, DVFS
3. Application 3: I^2C with 4 GPIOs
4. Application 4: I^2C, no FSO pins, DVFS, SSPT, interrupt
5. Application 5: SPI, no FSO pins, DVFS, interrupt
6. Application 6: I^2C and SPI, no FSO pins
7. Not used

2.2.2 I/O Pin Descriptions

Table 2. I/O Descriptions

I/O Name	Type	Description
DVFS	Input	Buck1 Dynamic Voltage Scaling selection pin. This pin selects between 2 voltage levels set for Buck1.
FSCLKST#	Input	SoC error notification signal. FSCLKST is asserted when a fault is detected in the R-Car SoC.
FSO_CFE_0	Input	SoC failure self-detection output pin. This pin is configured using software to react to certain faults in the R-Car SoC. The function of this pin is similar to FSCLKST#.
FSO_CFE_1	Input	SoC failure self-detection output pin. This pin is configured using software to react to certain faults in the R-Car SoC. The function of this pin is similar to FSCLKST#.
FSO_TOE	Input	SoC error notification signal. FSO_TOE is asserted when a time-out condition occurs. The function of this pin is similar to FSCLKST#.
GPIO[1-6]	Input/Output	General purpose IO. If configured as an output, the state of this pin can be set by a register. If configured as an input, the value of this pin can be read by a register.
INTb	Output	Maskable interrupt signal indicating a fault in the protection side of the device
MISO	Output	SPI master input, slave output signal
MOSI	Input	SPI master output, slave input signal
PRESET#	Output	Reset signal sent to R-Car SoC. During startup, this pin is LO until LBIST and self checks pass, then transitions HI after a fixed (but adjustable) timer has expired. If there is any fault in the protection portion of RAA271000, this pin transitions LO to reset the SoC.
PRESETOUT	Input	Reset notification signal from R-Car SoC. This is expected to be the same state as PRESET# but with a delay in processing from the SoC.
INT_REGU	Output	Maskable interrupt signal indicating a fault in the regulation side of the device
SCK	Input	SPI clock signal
SCL	Input	I^2C clock signal
SDA	Input/Output	I^2C data signal
SDO1	Safety Defined Output	Output signal defined by the protection state machine. As an example, this can set the standby control signal for a CAN transceiver.
SDO2	Safety Defined Output	Output signal defined by the protection state machine. As an example, this can enable an external CAN transceiver.
SS_B	Input	SPI slave select signal for regulation digital
SS_B2	Input	SPI slave select signal for protection digital
SSP, SSP2	Safety Defined Output	Output signal defined by the protection state machine. As an example, these can control a secondary safety path in the system.

3. Specifications

3.1 Absolute Maximum Ratings

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
PVIN[1-5], AVIN[1-2], LDOIN[1-2] pins to PGND[1-5]	-0.3	6	V
VOUT[1-5] (V_{OUT_PROG} ≤ 1.8V)	-0.3	2.1	V
VOUT[1-5] (V_{OUT_PROG} > 1.8V)	-0.3	V_{OUT_PROG} + 0.3V	V
VIO, EN to AGND[1-2]	-0.3	AVIN + 0.3	V
PH[1-5] to PGND[1-5]	-0.3	PVIN + 0.3	V
ADC[1-5] to AGND	-0.3	AVIN2 + 0.3	V
GPIO[1-14] pins to AGND	-0.3	VIO + 0.3	V
RTN1, AGND[1-2] to PGND[1-5]	-0.3	0.3	V
LDOIN[1-2] to AVIN[1-2]	-0.3	0.3	V

3.2 ESD Ratings

ESD Rating	Value	Unit
Human Body Model (Tested per JS-001-2017)	2	kV
Charged Device Model (Tested per JS-002-2018)	500	V
Charged Device Model Corner Pins (Tested per JS-002-2018)	750	V
Latch-Up (Tested per JESD78E; Class 2, Level A)	100	mA

3.3 Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)[1]	θ_{JC} (°C/W)[2]
60 Ball FCCSP Package	30.2	7.2

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is taken at the package top center.

Parameter	Minimum	Maximum	Unit
Maximum Storage Temperature Range	-65	+150	°C
Pb-Free Reflow Profile	See TB493		

3.4 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Supply Voltage (AVIN to GND)	2.7	5.5	V
Supply Voltage (PVIN to GND)	2.7	5.5	V
Ambient Temperature	-40	+125	°C
VIO Voltage (VIO to PGND)	1.7	5.5	V
Buck 1 Operating Current		15	A
Buck [2-3] Operating Current		2	A
Buck [4-5] Operating Current		4	A

3.5 Electrical Specifications

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C unless otherwise noted.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Input Supply						
Supply Voltage	AVIN		**2.7**		**5.5**	V
	PVIN		**2.7**		**5.5**	V
I/O Supply Voltage	VIO		**1.7**		**AVIN**	V
Operating Current at AVIN	Iq	EN = 0V		1		µA
		I_{OUT} = 0A, AV_{IN} = 5V, Forced CCM Operation, 1 buck enabled		13		mA
UVLO Rising Threshold	V_{UVLOR}	AVIN1, AVIN2, PVIN4 only	**2.7**		**2.9**	V
UVLO Falling Threshold	V_{UVLOF}	AVIN1, AVIN2, PVIN4 only	**2.5**		**2.7**	V
UVLO Hysteresis	$V_{UVLOhys}$			200		mV
AVIN1 OVP Rising Threshold	V_{OVPR}		**5.7**	5.8	**5.96**	V
AVIN1 OVP Hysteresis	V_{OVPhys}			200		mV
Power-On Self Test Time	T_{POST}			6		ms
Buck Regulators						
Regulation						
DC Output Voltage Accuracy		V_{OUT} > 0.8V	**-1.5**		**1.5**	%
		V_{OUT} ≤ 0.8V	**-13**		**13**	mV
Pull-Down Resistance of Buck Output	R_{dis_B1}	EN = 0, Buck 1		8		Ω
	R_{dis_B25}	EN = 0, Buck 2, Buck 3, Buck 4, Buck 5		40		Ω
Hysteretic Frequency						
Hysteretic CCM Frequency Tolerance	$f_{SW\_H\_TOL}$	Steady-state operation	**-20**		**20**	%
Fixed Switching Frequency						
Fixed Frequency Tolerance	$f_{SW\_F\_TOL}$		**-10**		**10**	%

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C unless otherwise noted. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Linear Regulators						
LDO 1-2						
Input Voltage Range for LDO	V_{IN_LDO}		**1.8**	3.6	**5.5**	V
DC Output Voltage Accuracy		V_{LDOOUT} = 2.5V to 3.6V, $V_{LDOOUT} < V_{LDOIN} - V_{DO}$, I_{OUT} = 0 mA	**-1.5**		**1.5**	%
		V_{LDOOUT} = 1.8V to 2.5V, $V_{LDOOUT} < V_{LDOIN} - V_{DO}$, I_{OUT} = 0 mA	**-2**		**2**	%
		V_{LDOOUT} = 0.6V to 1.8V, $V_{LDOOUT} < V_{LDOIN} - V_{DO}$, I_{OUT} = 0 mA	**-36**		**36**	mV
Rated Output Current	I_{OUTMAX}	V_{IN} > 3V	300			mA
		V_{IN} < 3V	200			mA
Output Current Limit	I_{OUT_LIM}		300	430	550	mA
Dropout Voltage	V_{DO}	V_{LDOIN} = 3V, $V_{DO} = V_{LDOIN} - V_{LDOOUT}$, I_{OUT} = 200mA			200	mV
DC Load Regulation		I_{OUT} from 0 to I_{OUTMAX}		20		mV/A
DC Line Regulation		V_{LDOIN} = VINmin to VINmax, I_{OUT} = 200mA		2		mV/V
Power Supply Ripple Rejection	PSRR	f = 10kHz, $I_{OUT} = I_{OUTMAX}/2$		40		dB
		f = 2.2MHz, $I_{OUT} = I_{OUTMAX}/2$		10		dB
Pull-Down Resistance and the Output of the LDO	R_{dis_LDO}	EN = 0		100		Ω
GPIO						
Chip Enable Logic Threshold Level						
EN Pin Low Level Input Voltage Range	V_{IL}				0.5	V
EN Pin High Level Input Voltage Range	V_{IH}		1.35			V
GPIO Logic Threshold Levels						
Low Level Input Voltage Range	V_{IL}				**0.25*VIO**	V
High Level Input Voltage Range	V_{IH}		**0.75*VIO**			V
Input Hysteresis	V_{HYS}		**0.1*VIO**			V
Low Level Output	V_{OL}	1mA			**0.4**	V
High Level Output	V_{OH}	1mA	**VIO-0.4**			V
Serial Interfaces						
I^2C Frequency Capability	f_{I2C}		**0.4**		**3.4**	MHz
SPI Frequency Capability	f_{SPI}				**26**	MHz

Unless otherwise noted, all external components are as shown in Figure 2 and PVIN = AVIN = 5V, T_A = +25°C. **Boldface limits apply across the operating temperature range, -40°C to +125°C unless otherwise noted. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Protection						
Buck 1 Positive Current Limit	$I_{PLIMIT1}$	2.5V < V_{IN} < 5.5V, OC = 20A	**-25**		**25**	%
Buck 1 Negative Current Limit	$I_{NLIMIT1}$	2.5V < V_{IN} < 5.5V, NOC = 9A	**-25**		**25**	%
Buck 2-3 Positive Current Limit	$I_{PLIMIT23}$	2.5V < V_{IN} < 5.5V, OC = 3A	**-25**		**25**	%
Buck 2-3 Negative Current Limit	$I_{NLIMIT23}$	2.5V < V_{IN} < 5.5V, NOC = 2A	**-25**		**25**	%
Buck 4-5 Positive Current Limit	$I_{PLIMIT45}$	2.5V < V_{IN} < 5.5V, OC = 6A	**-25**		**25**	%
Buck 4-5 Negative Current Limit	$I_{NLIMIT45}$	2.5V < V_{IN} < 5.5V, NOC = 3A	**-25**		**25**	%
Buck Output UVP Threshold Accuracy	V_{UVP}	BUCKx_VOUTFBDIV[1:0] = 0b00 programmable thresholds: ±100mV, ±150mV, ±200mV, ±250mV	**-35**		**35**	mV
Buck Output OVP Threshold Accuracy	V_{OVP}	BUCKx_VOUTFBDIV[1:0] = 0b00 programmable thresholds: ±100mV, ±150mV, ±200mV, ±250mV	**-35**		**35**	mV
Over-Temperature Rising Threshold	OT_R	Over-temperature threshold programmable from 135°C to 170°C in 5°C increments		150		°C
Over-Temperature Falling Threshold	OT_F	Over-temperature threshold programmable from 90°C to 125°C in 5°C increments		90		°C
Analog-to-Digital Converter						
Resolution				12		Bits
Reference Voltage				1.222		V
Reference Error					12	mV
Sample Period		Internal measurements		40		µs
		External measurements without external MUX		100		µs
		External measurements with external MUX		320		µs
Monitoring Accuracy						
Temperature Accuracy		PGA Gain = 8.0, IIR = 1/16		4		°C
Accuracy 0.6V		PGA Gain = 1.4, IIR = 1/16		1.5		%
Accuracy 0.82V		PGA Gain = 1.4, IIR = 1/16		1.5		%
Accuracy 1.1V		PGA Gain = 0.5, IIR = 1/16		1.5		%
Accuracy 1.2V		PGA Gain = 0.5, IIR = 1/16		1.5		%
Accuracy 1.8V		PGA Gain = 0.333, IIR = 1/16		1.5		%
Accuracy 2.5V		PGA Gain = 0.333, IIR = 1/16		1.5		%
Accuracy 3.3V		PGA Gain = 0.125, IIR = 1/16		1.5		%
Accuracy 4.0V		PGA Gain = 0.125, IIR = 1/16		1.5		%
Accuracy 5.0V		PGA Gain = 0.125, IIR = 1/16		1.5		%

1. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.

4. Typical Performance Curves

Unless otherwise specified, the operating condition is: V_{IN} = 5V, T_A = 25°C.

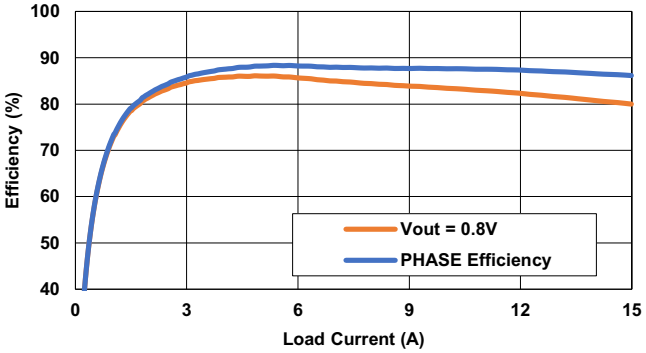


Figure 4. Efficiency of Buck1 at V_{IN} = 5V

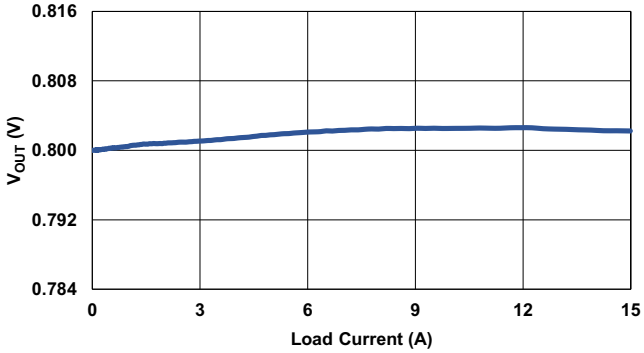


Figure 5. Load Regulation of Buck1 at V_{IN} = 5V

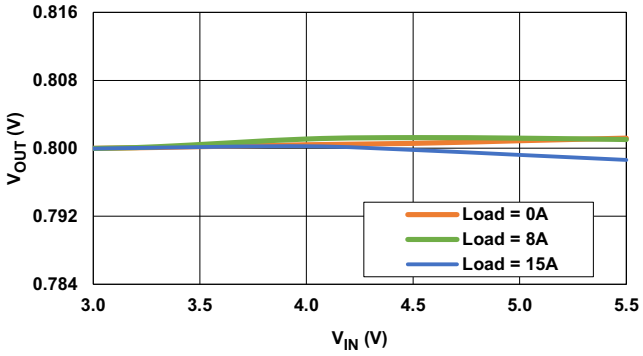


Figure 6. Line Regulation of Buck1

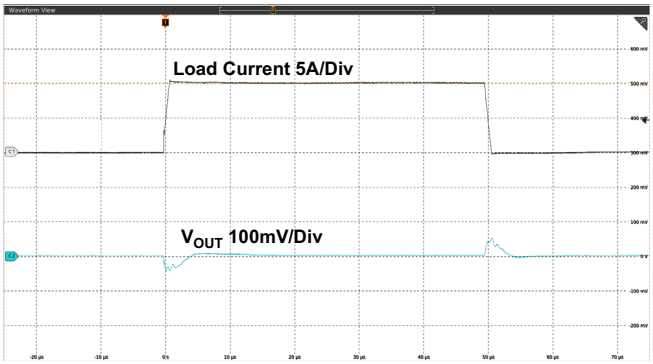


Figure 7. Load Transient of Buck1 at V_{IN} = 5V
V_{OUT} = 0.8V, C_{OUT} = 4x47µF, L= 0.12µH
Load Current Stepping from 1A - 11A

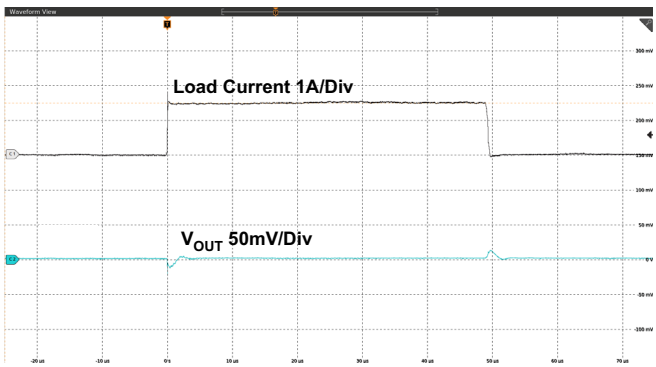


Figure 8. Load Transient of Buck2 at V_{IN} = 5V
V_{OUT} = 1.1V, C_{OUT} = 1x22µF, L= 0.47µH
Load Current Stepping from 0.5A - 2A

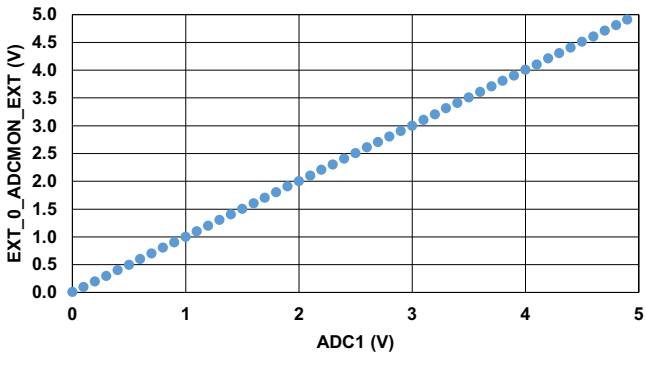


Figure 9. ADC Monitoring Ramp Test

5. Function Descriptions

5.1 Power Sequencing

Both the startup and shutdown sequencing of RAA271000 are user programmable.

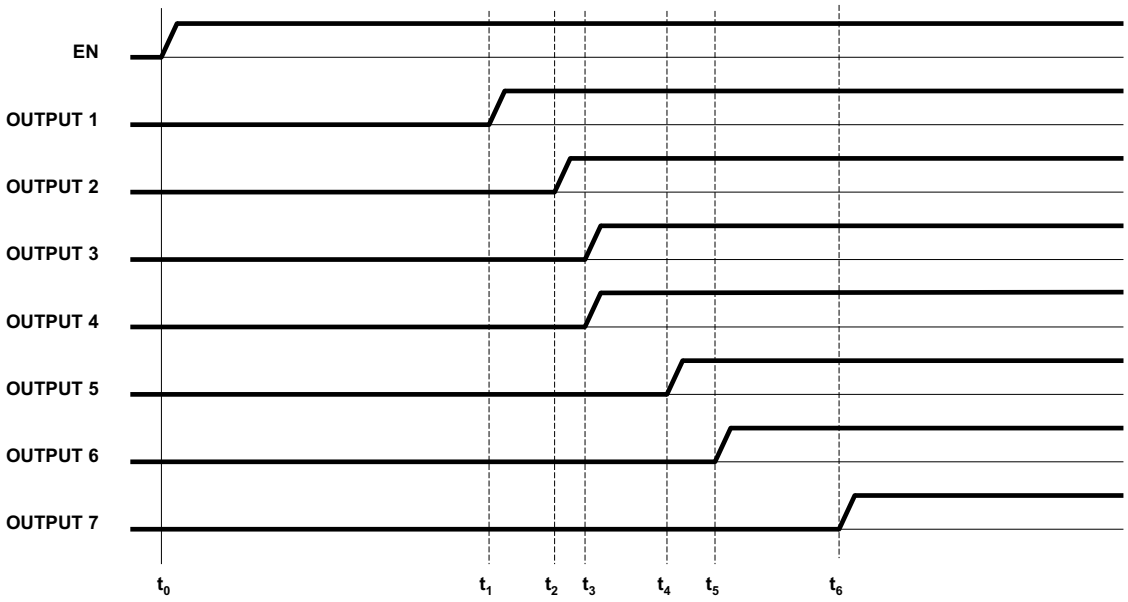


Figure 10. Startup Sequencing Example

For each output of RAA271000 (Buck 1-5 and LDO 1-2), the startup delay can be programmed from a value of 0ms to 67ms in 1.07ms steps. This sequence can be set in registers *_EN_DLY, where * is one of BUCK1, BUCK2, BUCK3, BUCK4, BUCK5, LDO1, or LDO2. In the example startup sequence shown in Figure 10, OUTPUT1 has a 0ms delay from EN, and the other outputs have an integer delay between 1.07ms and 67ms. **Note:** In this example, OUTPUT3 and OUTPUT4 have the same delay value. For a value of 0 for *_EN_DLY, there is a fixed wait time while the chip starts up and completes LBIST. This additional delay time is 6ms (typical).

While the EN_DLY value specifies when an output begins to startup, each output also starts up with a factory programmed ramp rate, which is specified in Buck Regulator Startup Ramp Rate and LDO Startup Ramp Rate.

An example of shutdown sequencing is shown in Figure 11.

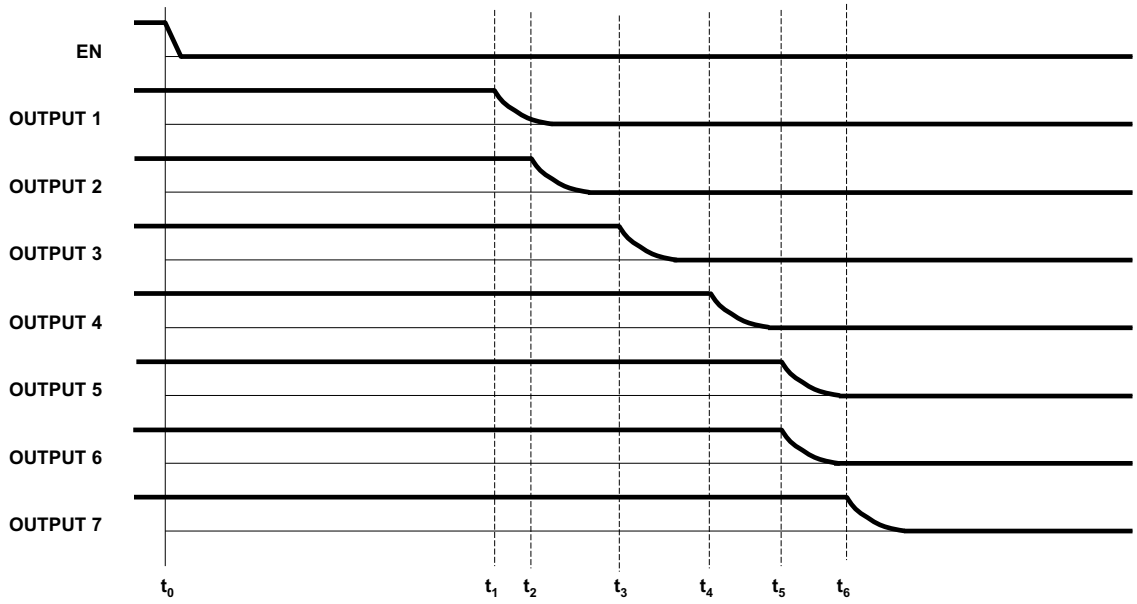


Figure 11. Shutdown Sequencing Example

Similar to the startup sequencing setting, each output can delay shutdown by between 0 to 67ms, which is specified in register *_SHUTDN_DLY. In Figure 11, the value of t_1 - t_0 can be 0ms. During shutdown, the sequencer gives the command to shut down a specific channel, which causes that output to go high impedance (both switches Hi-Z for buck regulators and the LDO output PMOS Hi-Z for LDO regulators) and pull down through a resistance. For buck regulators, this pull-down resistance is 8Ω for Buck 1 and 40Ω for Buck 2-5 (typical), and for the LDOs, the pull-down resistance is 100Ω (typical).

5.2 Functional Safety

Functional safety for RAA271000 is described fully in the Safety Application Note.

6. Serial Communication Interface

The RAA271000 has two serial interface protocols to read/write the registers.

- SPI
  - Regulation digital accessed with slave pin SS_B
  - Protection digital accessed with slave pin SS_B2
- I^2C
  - Regulation digital accessed by read/write to regulation slave
  - Protection digital accessed by read/write to protection slave

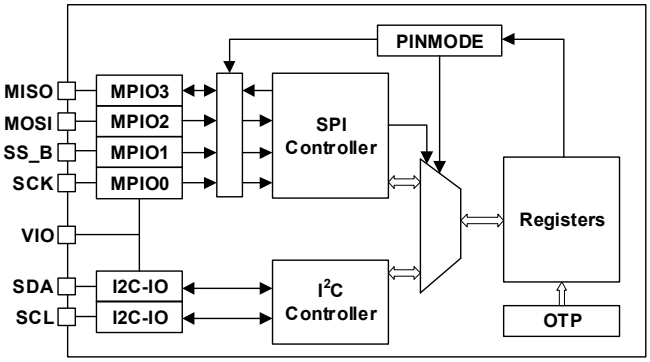


Figure 12. SPI and I^2C Interface Block Diagram

The arbitration of the register access bus between SPI and I^2C is determined by the pad MPIO1 when using IO_PINMODE = 0x5, as shown in Table 3:

Table 3. SPI/I^2C Register Access

Register IO_PINMODE	Pad MPIO_1 (SS_B)	Register Access
5	0	SPI (Read/Write Access[1]
	1	I^2C[2]

1. When the device is configured for SPI access, the I^2C should not be addressed with the device ID.
2. When the device is configured for I^2C access, in PINMODE 5, the SS_B line must be held high.

After switching from SPI to I^2C or from I^2C to SPI, there is a minimum of 50ns wait time is required before starting a transaction.

For the communication interfaces, the following parameters are factory programmable:

Table 4. Communication Interface Fuse Programmable Options

Design Parameter	Description	Recommended Value
IO_I2CADDR_PROT	Protection I^2C Slave	0x1D
IO_I2CADDR_REGU	Regulation I^2C Slave	0x1E
IO_SPIMODE	SPI Packet Length Mode	1
IO_SPICPOL	SPI Clock Polarity	0
IO_SPICPHA	SPI Clock Phase	0

6.1 SPI Serial Interface

The SPI interface is a general specification 4-wire slave interface capable of operating at a clock speed of up to 26MHz. It is based on byte transfers.

6.1.1 SPI Data Protocol

Both Read and Write SPI transactions begin when SS_B goes low and end when SS_B goes high.

6.1.1.1 Write Operation

To write to the RAA271000, the master (controller) must drive SS_B low, send the Control Byte, the register address, and the packet length (if IO_SPIMODE = 1), and finally as the data bytes are written, SS_B high is driven high to terminate the transaction (see Figure 13). The MSB of the Control byte is the R/W bit that must be set to write operation. Bit [1] and bit [0] of the Control byte indicate the page number of the register location that must be written (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address must be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the master must send the data bytes. When all eight bits of data are received, they are written to the specified register address.

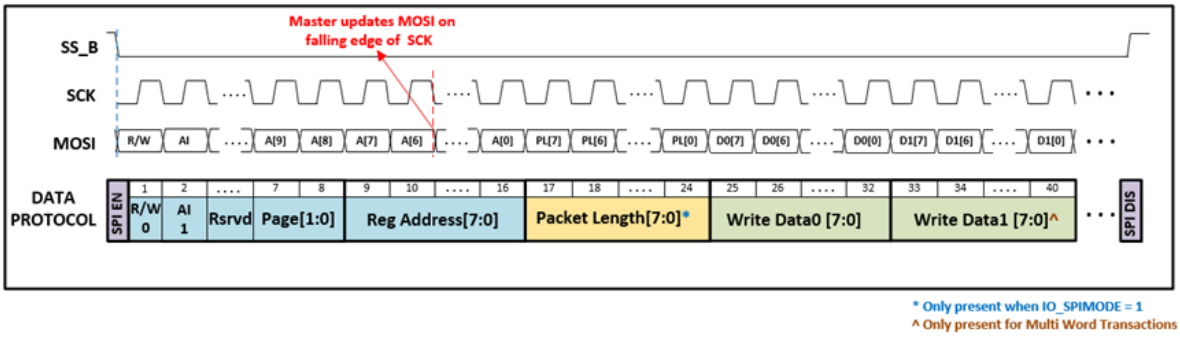


Figure 13. SPI Write Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

In single byte transactions (AI = 0 or Packet length = 1), the RAA271000 goes into a wait state and waits for SS_B to go high.

6.1.1.2 Read Operation

To read from the RAA271000, the master (controller) needs to drive SS_B low and then send the Control Byte, followed by register address, packet length (if IO_SPIMODE = 1). Next, the RAA271000 sends the data bytes from the requested registers and finally the master drives SS_B high to terminate the transaction. The MSB of the Control byte is the R/W bit that needs to be set to the read operation (see Table 5). Bits [1] and [0] of the Control byte indicate the page number of the register location be read (MSBs of the register address). The register address byte is the 8-bit address of the register within the page specified by Page[1:0] bits. If IO_SPIMODE = 1, the register address needs to be followed by an 8-bit packet length, which indicates the number of bytes to be written. Following the packet length field, the RAA271000 sends the data from the requested register.

In a single-byte transaction, (AI = 0 or Packet length = 1), the RAA271000 goes into a wait state and waits for SS_B to go high.

Note: The MISO pin is pulled low while SS_B is high.

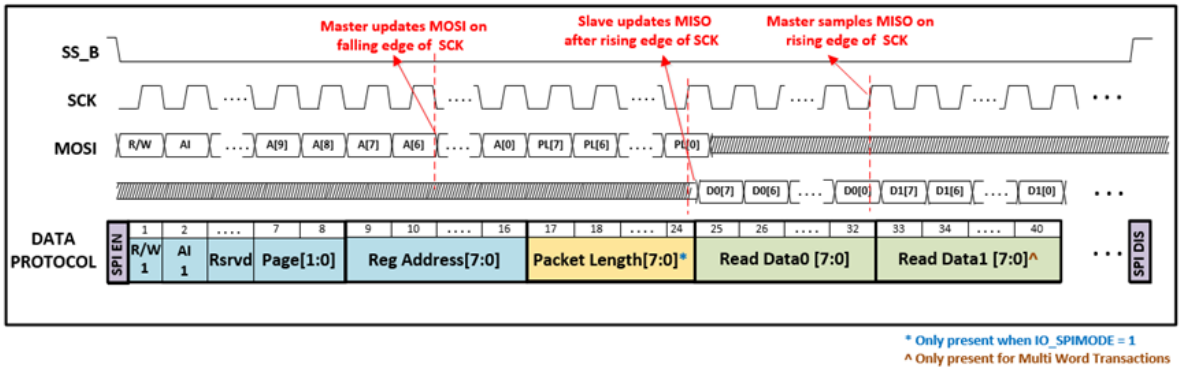


Figure 14. SPI Read Transaction with IO_SPIMODE = 1; IO_SPICPOL = 0; IO_SPICPHA = 0

R/W	Read/Write Bit Indicating Read or Write Operation
Page	2-bit page address of the register to be written/read
Address	8-bit register address of the register to be written/read
Packet Length	8-bit packet length indicating number of data bytes to be transferred. Overrides AI when IO_SPIMODE = 1
Read Data	Data in the register at address, Address [7:0] + n
Write Data	Data to be written to the register at address, Address [7:0] + n

6.1.2 SPI Configuration

The following register bits configure the SPI operation:

- **IO_SPICPOL:** SPI clock polarity, RAA271000 is configured as active high, IO_SPICPOL = 0.
- **IO_SPICPHA:** SPI clock phase, RAA271000 samples data on rising edge of SPI clock, IO_SPICPHA = 0.

The four possible modes of clocking are shown in Figure 15.

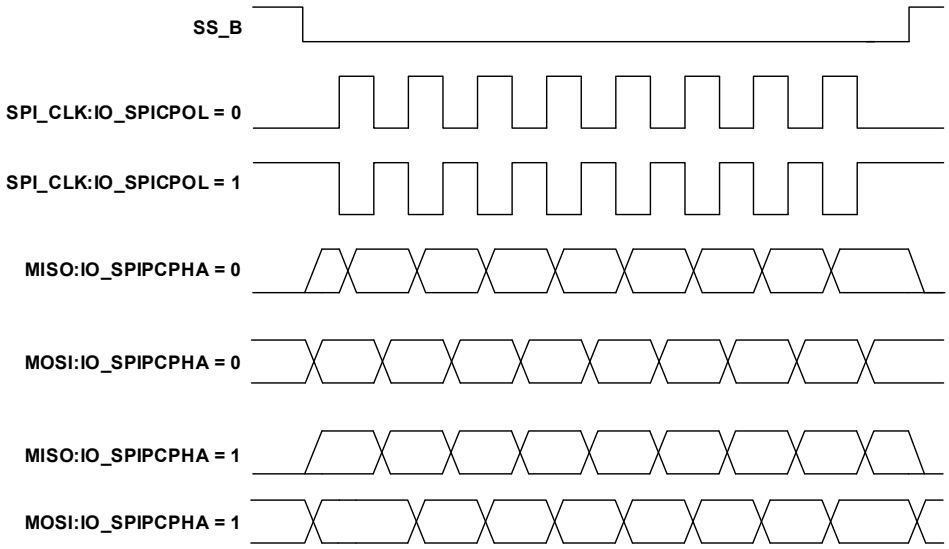


Figure 15. Four Possible Clocking Modes

- **IO_SPIRWPOL:** R/W bit polarity, RAA271000 SPI_RWPOL is set to 0, 1: Read, 0: Write.

Table 5. SPI_RWPOL R/W Bit Settings

SPI_RWPOL	R/W	Operation
0	0	Write
0	1	Read

- **IO_SPIMODE:** Packet length enable. The RAA271000 uses packet length mode by default, which means, the third data byte from master is the packet length and indicates the total number of data words to be sent/received in a transaction.

6.1.3 RAA271000 SPI Timing

Figure 16 shows SPI timing for IO_SPICPOL = 0; IO_SPICPHA = 0. The timing values in Table 6 hold true for other values of IO_SPICPOL, and IO_SPICHPA.

Table 6. Timing Values

Parameter	Symbol	Min	Max	Units
Clock Period	t_1	38.4		ns
Enable Lead Time	t_2	12		ns
Enable Lag Time	t_3	12		ns
Clock High or Low Time	t_4	15		ns
Data Setup Time (Input)	t_5	12		ns
Data Hold Time (Input)	t_6	10		ns
Time MISO is Stable before the Next Rising Edge of CLK	t_7	5		ns
Data Held after Clock Edge (Output)	t_8	5		ns
Load Capacitance	C_L		10	pF

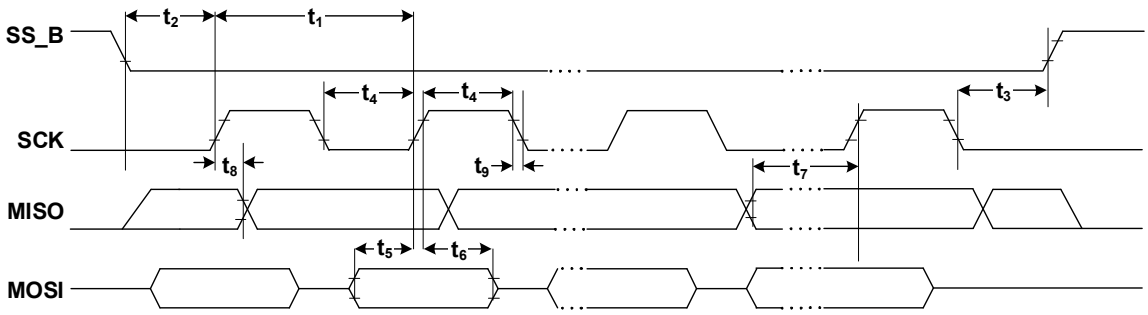


Figure 16. SPI Timing for IO_SPICPHA = 0, IO_SPICPOL = 0

6.2 I²C Interface

The I²C interface is a simple, bidirectional 2-wire bus protocol, consisting of the Serial Clock Control (SCL/I2C_CLK) and the Serial Data Signal (SDA/I2C_SDA). The RAA271000 hosts a slave I²C interface that supports data speeds up to 3.4Mbps. SCL is an input to the RAA271000 and is supplied by the controller, whereas SDA is bidirectional. The RAA271000 has an open-drain output to transmit data on SDA. **Note:** An external pull-up resistor must be placed on the serial data line to pull the drain output high during data transmission.

The RAA271000 uses a 7-bit hardware address scheme. The default address is set to 0x1D by a one-time programmable fuse.

6.2.1 I²C Bus Operation

The chip supports 7-bit addressing. The RAA271000 I²C device address is reconfigurable through the OTP.

All communication over the I²C interface is conducted by sending the MSB of each byte of data first. Data states on the SDA line can change only during SCL LOW periods. SDA state changes during SCL HIGH are reserved for indicating START and STOP conditions (see Figure 19).

All I²C interface operations must begin with a START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The RAA271000 continuously monitors the SDA and SCL lines for the START condition and does

not respond to any command until this condition is met. **Note:** All I²C interface operations must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH.

An Acknowledge (or ACK), is a software convention that indicates a successful data transfer. The transmitting device, either master or slave, releases the SDA bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data (Figure 19). The RAA271000 responds with an ACK after recognition of a START condition, followed by a valid Identification (also known as I²C Address) Byte. The RAA271000 also responds with an ACK after receiving a Data Byte of a write operation. The master must respond with an ACK after receiving a Data Byte of a read operation.

6.2.1.1 Write Operation

A Write operation requires a START condition, followed by an RAA271000 I²C Address byte with the R/W bit set to 0, a Register Address Byte, Data Bytes, and a STOP condition. After each byte, the RAA271000 responds with an ACK. **Note:** A STOP condition that terminates the write operation must be sent by the master after sending at least one full data byte and its associated ACK signal. If a STOP byte is issued in the middle of a data byte, the write is not performed.

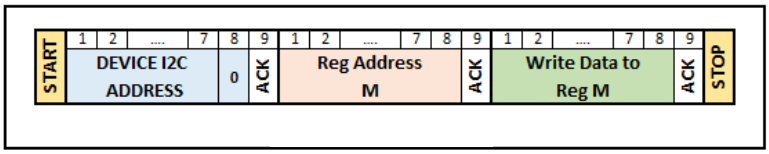


Figure 17. 1-Byte Write to Register M

6.2.1.2 Read Operation

A Read operation consists of a 3-byte dummy write instruction to send the register address to begin reading from, followed by a Current Address Read operation. The master initiates the operation, issuing the following sequence: a START condition, followed by an RAA271000 I²C Address byte with the R/W bit set to 0, a Register Address Byte, a second START, and a second RAA271000 I²C Address byte with the R/W bit set to 1. After each of the three bytes, the RAA271000 responds with an ACK. Next, the RAA271000 transmits the data bytes. The master terminates the Read operation from the RAA271000 by issuing a STOP condition following the last bit of the last data byte.

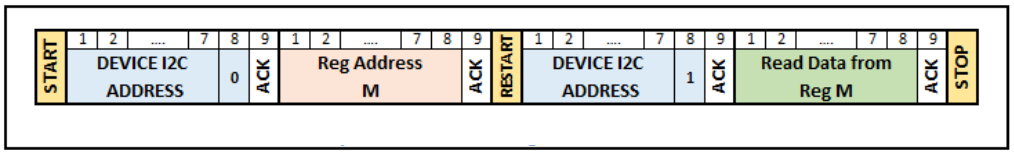


Figure 18. 1-Byte Data Read from Register M

6.2.2 I²C Timing

The timing specifications of the I²C I/O from the I²C spec are shown in Figure 19 and Table 7. The I²C controller provides a slave I²C transceiver capable of interpreting I²C protocol in Standard, Fast, Fast+, and High Speed modes.

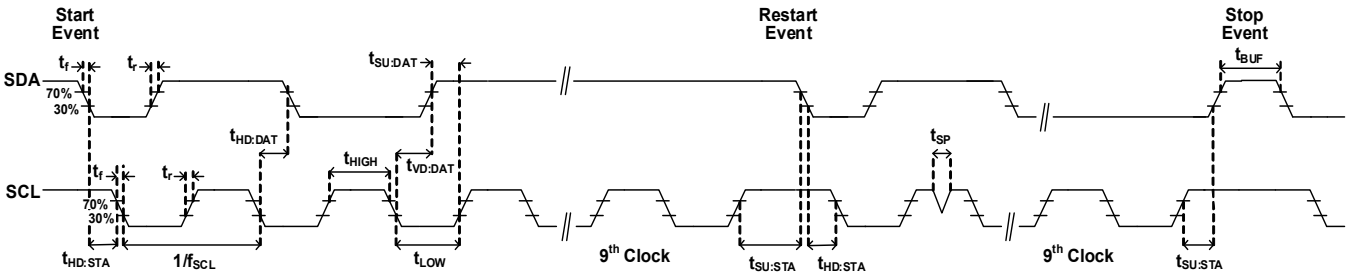


Figure 19. I²C Timing

Table 7. I²C Specification

Parameter[1]	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Frequency	f_{SCL}	0	100	0	400	0	1000	0	3400	kHz
Hold Time (repeated) START Condition. (After this period, the first clock pulse is generated.)	t_{HD};STA	4000	-	600	-	260	-	160	-	ns
LOW Period of the SCL Clock	t_{LOW}	4700	-	1300	-	500	-	160	-	ns
HIGH Period of the SCL Clock	t_{HIGH}	4000	-	600	-	260	-	60	-	ns
Setup Time for a Repeated START Condition	$t_{SU;STA}$	4700	-	600	-	260	-	160	-	ns
Data Hold Time	$t_{HD;DAT}$	15	-	15	-	15	-	15	70	ns
Data Setup Time	$t_{SU;DAT}$	250	-	100	-	50	-	10	-	ns
Rise Time of SCL	t_{rCL}	-	1000	-	300	-	120	-	40	ns
Fall Time of SCL	t_{fCL}	-	300	-	300	-	120	-	40	ns
Rise Time of SDA	t_{rDA}	-	1000	20	300	-	120	10[2]	80	ns
Fall Time of SDA	t_{fDA}	-	300	20 × (V_{DD}/5.5V)[3]	300	20 × (V_{DD}/5.5V)[2]	120	10[2]	80	ns
Setup Time for STOP Condition	$t_{SU;STO}$	4000	-	600	-	260	-	160	-	ns
Bus Free Time between a STOP and START Condition	t_{BUF}	4700	-	1300	-	500	-	-	-	ns
Capacitive Load for each Bus Line	C_b	-	400	-	400	-	400		100	pF

Table 7. I²C Specification (Cont.)

Parameter[1]	Symbol	Standard Mode		Fast Mode		Fast Mode Plus		High Speed Mode		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
Output Fall Time from VIHmin to VILmax	t_{of}	-	250[5]	20 × (V_{DD} /5.5V)[6]	250[5]	20 × (V_{DD}/5.5V)[6]	120[7]	10[2]	80	ns
Pulse Width of Spikes Suppressed by the Input Filter	t_{SP}	-	-	0	50	0	50	0	10	ns

1. V_{DD} is the pull-up source to the I²C lines (GPIO0, GPIO1).
2. Valid only for V_{DD} < 1.9V.
3. Valid only for V_{DD} < 4V.

6.3 Communication Cyclic Redundancy Check (CRC)

As a fuse option, each write and read transaction from the master to RAA271000 can be implemented with an additional byte of Cyclic Redundancy (CRC-8). CRC can be used for both I²C and SPI communication using the following polynomial:

(EQ. 1) $$x^8 + x^2 + x^1 + 1$$

During a WRITE transaction, this extra byte is added after the write data. For a READ transaction, a second byte of CRC is sent to the master after the data byte. For each new transaction, the CRC value is reset to 0x00.

6.3.1 Example CRC calculation (C)

Below is a sample 1-byte CRC calculation in C language:

```
uint8_t calculate_i2c_crc(uint8_t last_crc, uint8_t new_data)
          {

             crc_result = 0;

// Extract bits of last_crc
for(i=0;i<8;i++)
   {
   crc_c[i] = (last_crc >> i) & 1;
   }

// Extract bits of new_data
for(i=0;i<8;i++)
   {
   crc_d[i] = (new_data >> i) & 1;
   }

crc_newcrc[7] = crc_d[7]^crc_d[6]^crc_d[5]^crc_c[5]^crc_c[6]^crc_c[7];
crc_newcrc[6] = crc_d[6]^crc_d[5]^crc_d[4]^crc_c[4]^crc_c[5]^crc_c[6];
crc_newcrc[5] = crc_d[5]^crc_d[4]^crc_d[3]^crc_c[3]^crc_c[4]^crc_c[5];
crc_newcrc[4] = crc_d[4]^crc_d[3]^crc_d[2]^crc_c[2]^crc_c[3]^crc_c[4];
crc_newcrc[3] =
crc_d[7]^crc_d[3]^crc_d[2]^crc_d[1]^crc_c[1]^crc_c[2]^crc_c[3]^crc_c[7];
crc_newcrc[2] =
crc_d[6]^crc_d[2]^crc_d[1]^crc_d[0]^crc_c[0]^crc_c[1]^crc_c[2]^crc_c[6];
crc_newcrc[1] = crc_d[6]^crc_d[1]^crc_d[0]^crc_c[0]^crc_c[1]^crc_c[6];
crc_newcrc[0] = crc_d[7]^crc_d[6]^crc_d[0]^crc_c[0]^crc_c[6]^crc_c[7];

// restore bits back to unsigned short
for(i=0;i<8;i++)
   {
   crc_result |= crc_newcrc[i] << i;
   }

return crc_result;
}
```

7. Power Management Features

7.1 Buck Regulators (Buck 1-5)

RAA271000 includes five DC/DC buck step-down regulators. Each regulator has an output voltage adjustable by using a 10-bit DAC and a feedback divider. The frequency of each buck can be set to hysteretic (varying frequency), fixed frequency, or pseudo-random spread spectrum frequency. Of these three options, hysteretic mode offers the best transient performance.

7.1.1 Buck Output Voltage Selection

The output voltage for each buck regulator is set by a feedback divider and a 10-bit DAC. While the feedback divider ratio is factory programmed, the DAC value can be changed by adjusting the values of BUCKx_DVS0VOUT92 and BUCKx_DVS0VOUT10. These values are the top eight bits and lower two bits of the 10-bit DAC, respectively. For the output voltage to change, the value of BUCKx_DVS0VOUT10 must be written. For Buck 1 only, there is a value for the second DVS code in BUCK1_DVS1VOUT. More details on Buck1 DVS are described in Dynamic Voltage Scaling (DVS).

The output voltage for each buck based on the FB divider setting used is shown in Equation 2. **Note:** To ensure proper regulation, the buck output voltage must be set to a value between 0.3V and 3.3V.

(EQ. 2) $$V_{BUCK} = 1.2125 \bullet \frac{(DAC/1023)}{FBDIV}$$

DAC is the 10-bit Buck DAC code and FBDIV is the feedback divider value. **Note:** FBDIV can be factory programmed to a value of 1, 0.75, 0.5, or 0.25.

7.1.1.1 Buck DAC Step Size

The step size for each DAC code in () can also be rewritten as mV/bit as shown in Table 8.

Table 8. Buck DAC Step Size

VOUTFBDIV Value	DAC Step Size (mV/bit)
1.0	1.19
0.75	1.58
0.5	2.37
0.25	4.74

7.1.2 Buck Regulator Startup Ramp Rate

The rate at which the buck regulators ramp up during startup can be factory programmed to different options. This ramp rate depends on the voltage range used for the buck regulator and therefore, the value of VOUTFBDIV. Table 9 shows the factory programmable startup ramp rate options.

Table 9. Buck Regulator Ramp Rate Options

VOUTFBDIV Value	Option Number	Buck 1 Ramp Rate (mV/µs)	Buck 2-5 Ramp Rate (mV/µs)
1.0 Options			
1.0	0	3	1.2
1.0	1	6	3
1.0	2	14.4	7.2
1.0	4	12	6
0.75 Options			
0.75	0	1.6	1.6
0.75	1	3.2	3.2
0.75	2	6.4	6.4
0.5 Options			
0.5	0	1.2	1.2
0.5	1	2.4	2.4
0.5	2	6	6
0.25 Options			
0.25	0	1.2	1.2
0.25	1	2.4	2.4
0.25	2	6	6

7.1.3 Buck 1 Additional Features

In addition to the specifications previously mentioned that are common to all buck channels, Buck 1 contains some additional features. Buck 1 includes Dynamic Voltage Scaling (DVS) to quickly change between two predetermined voltage levels. Buck 1 also uses an internal high-side NMOS device, so a bootstrap capacitor is required and ties between pins BOOT and PH1.

7.1.4 Dynamic Voltage Scaling (DVS)

While all buck regulators can change output voltage by changing the DAC value, Buck 1 has several options to achieve DVS. There are two independently programmable voltage settings for the Buck 1 controller, which can set the output voltage. These settings are DVS0 and DVS1. By changing the DVS number selected, the corresponding output voltage is selected. There are two methods to select the DVS output voltage.

- **Method 1**: Use internal registers to select DVS by writing to the BUCK1_DVSSELECT bit in the BUCK1_DVSSEL register using SPI or I^2C. To use this method, the BUCK1_DVSCTRL bit has to be set to 0b0 for the corresponding buck. The BUCK1DVSSELECT bit allows you to switch between the two different DVS settings, each corresponding to a set of DVS registers holding the DVS information.
  For example, DVS0 corresponds to BUCK1_DVS0VOUT92[7:0] and BUCK1_DVS0VOUT10[1:0]. The two register values combined represent the complete 10-bit DAC code for DVS0.
- **Method 2**: Using the GPIO3 pin to achieve DVS, there are five variations depending on the IO_PINMODE register setting. See Table 1.
  Note: To use DVS using the GPIO/MPIO pins requires IO_PINMODE to be OTP programmed before a start-up

boot sequence is initiated. **Note:** On-the-fly programming is not recommended for the following configurations.
(i) IO_PINMODE = 1 or 3: DVFS pin available

7.1.5 Fixed Frequency Operation

The buck regulators can be forced to operate in a fixed frequency mode. In this mode, each regulator can be factory programmed to one of the three frequencies shown in Table 10.

Table 10. Fixed Frequency Options

Frequency (MHz)	Option Number
2.29	0
2.91	1
4.00	2

If two or more buck outputs are programmed with the same fixed frequency option, a selectable phase shift of 0º or 180º, measured relative to the phase of Buck 1.

7.1.6 Spread Spectrum Operation

The buck regulators support quasi-random spread spectrum operation to reduce emissions. This mode is implemented using a divided version of the internal oscillator while modulating control bits to rapidly adjust the oscillator center frequency. **Note:** The center frequency used in spread spectrum mode is factory programmable with the same values in Table 8.

The frequency deviation in fixed frequency mode can be factory programmed between ±3.5% to ±1%. There is also a dwell (or pause) time that keeps the oscillation to a fixed frequency for a certain period of time. The dwell time can be fixed or random in time.

The full list of factory programmable options in spread spectrum mode are listed in Table 11 through Table 13.

Table 11. Spread Spectrum Amplitude Options

Maximum Frequency Deviation (%)	Option Number
1	0
2	1
3	2
3.5	3

Table 12. Spread Spectrum Direction Options

Direction	Option Number
Spread spectrum disabled	0
Downwards only (-)	1
Centered (+ and -)	2
Upwards only (+)	3

Table 13. Spread Spectrum Frequency Dwell Settings

Dwell Setting	Option Number
Random dwell for 0 - 1.75ms	0
Random dwell for 0 - 3.75ms	1

Table 13. Spread Spectrum Frequency Dwell Settings (Cont.)

Dwell Setting	Option Number
Random dwell for 0.75 - 7.75ms	2
Random dwell for 0 - 15.75ms	3
Fixed dwell for 1.75ms	4
Fixed dwell for 3.25ms	5
Fixed dwell for 7.75ms	6
Fixed dwell for 14.25ms	7

7.1.7 Recommended Buck External Components

Based on the operating option, the buck regulators can be used with a different minimum amount of output capacitance to maintain their load transient specifications. Capacitance values lower than recommended can be used, but the transient performance suffers.

Table 14. Recommended Buck Output Capacitance Based on Operating Mode

Output	Hysteretic (µF)	Fixed Frequency (µF)	Spread Spectrum (µF)
Buck 1	4 x 47	8 x 47	8 x 47
Buck 2	1 x 22	3 x 47	3 x 47
Buck 3	1 x 22	3 x 47	3 x 47
Buck 4	1 x 22	3 x 47	3 x 47
Buck 5	1 x 22	3 x 47	3 x 47

Table 15. Recommended Inductors for Each Buck Output

Output	Inductor Value (nH)
Buck 1	80 ~ 150
Buck 2	220 ~ 470
Buck 3	220 ~ 470
Buck 4	220 ~ 470
Buck 5	220 ~ 470

7.2 LDO regulators (LDO 1-2)

RAA271000 includes two LDOs. The output of each LDO is programmed by an 8-bit DAC and each output is independent. LDO1 and LDO2 have separate power inputs at pints LDOIN1 and LDOIN2, respectively. The output of each LDO should be connected to a 1µF filtering capacitor.

Renesas does not recommended to operate the LDOs with a large dropout voltage (LDOO - LDOIN) and a high current. The power dissipated by each LDO must be less than 600mW. This power is calculated using Equation 3.

(EQ. 3) $$Pdiss = (V_{LDOIN} - V_{LDOO}) \bullet I_{OUT}$$

7.2.1 LDO Output Voltage

Both LDOs can be set to an output voltage of 0.6V to 3.6V in 15.2mV steps. This output voltage is set by the 8-bit DAC value in registers LDO1_VOUT_CORE and LDO2_VOUT_CORE for LDO1 and LDO2, respectively. The LDO output voltage follows Equation 4.

Note: The output voltage of the LDO must be set above 0.6V to ensure proper operation.

(EQ. 4) $$V_{LDO} = 3.2 \bullet 1.2125 \bullet \frac{DAC}{255}$$

7.2.2 LDO Startup Ramp Rate

Similar to the buck regulators, LDO1-2 starts up with a factory-programmed ramp rate based on Table 16.

Table 16. LDO Ramp Rate Options

Option Number	LDO Ramp Rate (mV/µs)
0	15.4
1	7.7
2	3.9
3	2.0
4	1.0
5	0.5
6	0.2

7.3 Digital Features

7.3.1 Fault Reactions

The Buck and LDO regulators have a number of faults for which they can report and react. Figure 21 summarizes the faults and how the regulators can be configured to react:

Table 17. Faults and Reactions

Fault Name	Regulator Type	Reaction	Description
Overvoltage	Buck only	Do nothing	Ignore the fault
		Stops switching this buck	Stop the buck switching
		Stops switching for a few cycles then shutdown this buck	Stop the buck switching for a few cycles then shutdown
		Shuts down this buck	Force the buck to disable
		Shuts down all bucks	Force all buck regulators to disable
		Shuts down all regulators	Force all regulators to disable
Undervoltage	Buck and LDO	Do nothing	Ignore the fault
		Shuts down this regulator	Force the regulator to disable
		Shuts down all bucks	Force all buck/LDOs to disable
		Shuts down all regulators	Force all regulators to disable
High-Side Positive Current Limit	Buck only	Do nothing	Ignore the fault
		Shuts down this regulator	Force the buck to disable
		Shuts down all bucks	Force all buck regulators to disable
		Shuts down all regulators	Force all regulators to disable

Table 17. (Cont.)Faults and Reactions

Fault Name	Regulator Type	Reaction	Description
Low-Side Negative Current Limit	Buck only	Do nothing	Ignore the fault
		Shuts down this regulator	Force the buck to disable
		Shuts down all bucks	Force all buck regulators to disable
		Shuts down all regulators	Force all regulators to disable
Regulation Over-Temperature Protection	Buck and LDO	Shuts down this regulator	Force the regulator to disable
		Do Nothing	Ignore the fault

7.3.2 Regulation Interrupt (REGU_INT) Pin

In pin mode 0x3 and pin mode 0x4, there is an interrupt pin (REGU_INT) that alerts the SoC to faults inside the regulation block of the PMIC. These faults can be individually masked by changing the bits in the FLT_MASK* registers and faults can be read through the FLT_RECORD* registers. **Note:** Both registers exist in the regulation register map, listed in Regulation Register Map. Table 18 shows a list of the individual faults that can trigger the REGU_INT pin.

Table 18. INT Pin Fault Signals

Description	Register Map Name	Maskable?	Notes
OTP Program Warning	OTPPROGWARN	Y	Not used by user
OTP Programming Addr fault	OTPPROGADDR	Y	Not used by user
OTP Programming fault	OTPPTOG	Y	Not used by user
OTP Init failure	OTPINIT	Y	OTP download engine failed to complete
OTP CRC Failure 2	OTPCRCPAGE2	Y	CRC failure bit [2]
OTP CRC Failure 1	OTPCRCPAGE01	Y	CRC failure bit [1]
OTP Read Duration Fault	OTPTIMEOUT	Y	OTP Read duration > ~8ms
OTP Not Programmed Fault	OTPNOTPGMD	Y	
Boot Occurred	BOOT	Y	Indicates that boot process has occurred
Over-Temperature Rising	TEMPSDR	Y	Indicates that the over-temperature block in the regulation area is over its threshold value (rising threshold)
Over-Temperature Falling	TEMPSDF	Y	Indicates that the over-temperature block in the regulation area has fallen below the threshold (falling threshold, Shutdown - Hysteresis)
Buck1 Boot Undervoltage	BOOTUV	Y	Indicates an undervoltage fault on Buck 1
Buck1 Low-Side Way Undercurrent	BUCK1_LSWUC	Y	
Buck1 Low-Side Way Overcurrent	BUCK1_LSWOC	Y	
Buck1 High-Side Way Overcurrent	BUCK1_HSWOC	Y	
Buck1 Overvoltage	BUCK1_OV	Y	Factory programmable threshold of +150mV, +200mV, +250mV, or +300mV
Buck1 Undervoltage	BUCK1_UV	Y	Factory programmable threshold of -150mV, -200mV, -250mV, or -300mV

Table 18. INT Pin Fault Signals (Cont.)

Description	Register Map Name	Maskable?	Notes
Buck2 Low-Side Way Undercurrent	BUCK2_LSWUC	Y	
Buck2 Low-Side Way Overcurrent	BUCK2_LSWOC	Y	
Buck2 High-Side Way Overcurrent	BUCK2_HSWOC	Y	
Buck2 Overvoltage	BUCK2_OV	Y	Factory programmable threshold of +150mV, +200mV, +250mV, or +300mV
Buck2 Undervoltage	BUCK2_UV	Y	Factory programmable threshold of -150mV, -200mV, -250mV, or -300mV
Buck3 Low-Side Way Undercurrent	BUCK3_LSWUC	Y	
Buck3 Low-Side Way Overcurrent	BUCK3_LSWOC	Y	
Buck3 High-Side Way Overcurrent	BUCK3_HSWOC	Y	
Buck3 Overvoltage	BUCK3_OV	Y	Factory programmable threshold of +150mV, +200mV, +250mV, or +300mV
Buck3 Undervoltage	BUCK3_UV	Y	Factory programmable threshold of -150mV, -200mV, -250mV, or -300mV
Buck4 PVIN OK	BUCK4_PVIN_OK	Y	Indicates whether there is a fault on PVIN4
Buck4 Low-Side Way Undercurrent	BUCK4_LSWUC	Y	
Buck4 Low-Side Way Overcurrent	BUCK4_LSWOC	Y	
Buck4 High-Side Way Overcurrent	BUCK4_HSWOC	Y	
Buck4 Overvoltage	BUCK4_OV	Y	Factory programmable threshold of +150mV, +200mV, +250mV, or +300mV
Buck4 Undervoltage	BUCK4_UV	Y	Factory programmable threshold of -150mV, -200mV, -250mV, or -300mV
Buck5 Low-Side Way Undercurrent	BUCK5_LSWUC	Y	
Buck5 Low-Side Way Overcurrent	BUCK5_LSWOC	Y	
Buck5 High-Side Way Overcurrent	BUCK5_HSWOC	Y	
Buck5 Overvoltage	BUCK5_OV	Y	Factory programmable threshold of +150mV, +200mV, +250mV, or +300mV
Buck5 Undervoltage	BUCK5_UV	Y	Factory programmable threshold of -150mV, -200mV, -250mV, or -300mV
LDO2 Undervoltage	LDO2_UV	Y	Undervoltage detection for LDO2. Indicates a short-circuit and the threshold is about 70% of the target LDO output voltage.

Table 18. INT Pin Fault Signals (Cont.)

Description	Register Map Name	Maskable?	Notes
LDO1 Undervoltage	LDO1_UV	Y	Undervoltage detection for LDO1. Indicate a short-circuit and the threshold is about 70% of the target LDO output voltage.
VBAT Overvoltage	VBAT_OV	Y	Overvoltage fault on AVIN1
SPI CRC Error	FLT_SPI	Y	Indicates a fault during a SPI transaction while CRC for SPI communication is enabled
I^2C CRC Error	FLT_I2C	Y	Indicates a fault during an I2C transaction while CRC for I^2C communication is enabled

8. Protection Features

While the Regulation side of the chip handles the power management functions and delivers stable power to all outputs, the Protection side of the chip monitors all output and internal signals for faults.

8.1 Monitoring ADC

The RAA271000 uses a sophisticated multi-channel 12-bit SAR ADC to continuously monitor all output rails, critical internal signals and the chip temperature. ADC samples are processed by a digital averaging filter to reduce noise and increase accuracy.

The monitoring system also measures up to 16 external signals by using 5 dedicated ADC pins. These ADC pins can be configured either as all analog inputs (ADC 1-5), or they can be configured to use external multiplexers. If external multiplexers are used, pins ADC1 and ADC2 are analog inputs, and pins ADC3, ADC4, and ADC5 are digital outputs to control the digital multiplexers with fixed timing. When external multiplexers are used, the channels are interleaved between each MUX with ADC1 connecting to even channels and ADC2 connecting to odd channels. A block diagram of the monitoring system is shown in Figure 20.

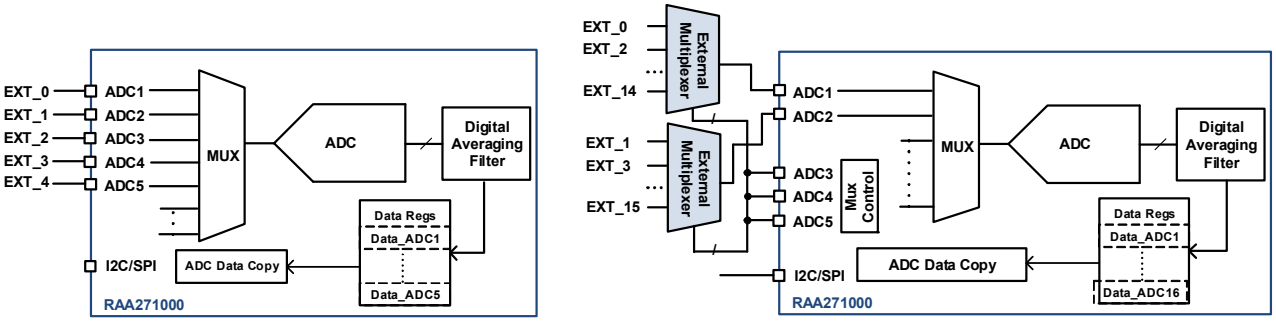


Figure 20. Monitoring ADC Block Diagram without (Left) and with (Right) External MUX

ADC High/low thresholds, averaging filter coefficient (IIR) and full-scale range (PGA gain) are all independently programmable for external measurements 1 to 8. When using external MUXes, this corresponds to the first four input signals on each MUX.

8.1.1 Monitoring ADC Inputs

The monitoring system monitors the outputs of each of the ADC inputs shown in Table 19. Monitoring is performed by comparing the current ADC Data with a High Limit and Low Limit value that is set in the same format as the ADC readings.

Table 19. All Monitoring ADC Inputs

ADC Input Description	Register Map Name	Scaling Factor	Unit
ADC Internal Offset	ADCMON_Offset	1	Codes
Temperature	ADCMON_Temp	4	°C
Temperature (redundant copy)	ADCMON_Temp_Delta	4	°C
Regulation Bandgap	ADCMON_BGRegu	4000	V
Regulation PGND	ADCMON_PGNDRegu	4000	V
Regulation Internal LDO #1	IntLDORegu_0_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #2	IntLDORegu_1_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #3	IntLDORegu_2_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #4	IntLDORegu_3_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #5	IntLDORegu_4_ADCMON_IntLDORegu	3000	V
Regulation Internal LDO #6	IntLDORegu_5_ADCMON_IntLDORegu	3000	V
Protection Internal LDO #1	IntLDOProt_0_ADCMON_IntLDOProt	3000	V
Protection Internal LDO #2	IntLDOProt_1_ADCMON_IntLDOProt	3000	V
AVIN1 Voltage	ADCMON_AVIN1	4000	V
AVIN2 Voltage	ADCMON_AVIN2	4000	V
LDO1 Voltage	extLDO_0_ADCMON_ExtLDO	4000	V
LDO2 Voltage	extLDO_1_ADCMON_ExtLDO	4000	V
PVIN1 Voltage	PVIN_0_ADCMON_PVIN	533	V
PVIN2 Voltage	PVIN_1_ADCMON_PVIN	533	V
PVIN3 Voltage	PVIN_2_ADCMON_PVIN	533	V
PVIN4 Voltage	PVIN_3_ADCMON_PVIN	533	V
PVIN5 Voltage	PVIN_4_ADCMON_PVIN	533	V
Buck1 (VOUT1) Voltage	VOUT_0_ADCMON_VOUT	4000	V
Buck1 (VOUT1) Voltage	VOUT_1_ADCMON_VOUT	4000	V
Buck1 (VOUT1) Voltage	VOUT_2_ADCMON_VOUT	4000	V
Buck1 (VOUT1) Voltage	VOUT_3_ADCMON_VOUT	4000	V
Buck1 (VOUT1) Voltage	VOUT_4_ADCMON_VOUT	4000	V
ADC1 / External ADC Mux Channel 0	EXT_0_ADCMON_EXT	4000	V
ADC2 / External ADC Mux Channel 1	EXT_1_ADCMON_EXT	4000	V
ADC3 / External ADC Mux Channel 2	EXT_2_ADCMON_EXT	4000	V
ADC4 / External ADC Mux Channel 3	EXT_3_ADCMON_EXT	4000	V
ADC5 / External ADC Mux Channel 4	EXT_4_ADCMON_EXT	4000	V
External ADC Mux Channel 5	EXT_5_ADCMON_EXT	4000	V
External ADC Mux Channel 6	EXT_6_ADCMON_EXT	4000	V
External ADC Mux Channel 7	EXT_7_ADCMON_EXT	4000	V
External ADC Mux Channel 8	EXT_8_ADCMON_EXT	4000	V
External ADC Mux Channel 9	EXT_9_ADCMON_EXT	4000	V

Table 19. All Monitoring ADC Inputs (Cont.)

ADC Input Description	Register Map Name	Scaling Factor	Unit
External ADC Mux Channel 10	EXT_10_ADCMON_EXT	4000	V
External ADC Mux Channel 11	EXT_11_ADCMON_EXT	4000	V
External ADC Mux Channel 12	EXT_12_ADCMON_EXT	4000	V
External ADC Mux Channel 13	EXT_13_ADCMON_EXT	4000	V
External ADC Mux Channel 14	EXT_14_ADCMON_EXT	4000	V
External ADC Mux Channel 15	EXT_15_ADCMON_EXT	4000	V

8.1.2 Programmable Gain Amplifier

The monitoring ADC includes a Programmable Gain Amplifier (PGA) to precondition analog inputs. The output of the PGA is connected to the ADC. The ADC itself has an input voltage range of ±980mV.

RAA271000 has 8 PGA gain settings that set the effective input voltage range of the input to the ADC. The PGA gain for each ADC channel can be set independently. All PGA gains are shown in Table 20.

Table 20. PGA Gain settings

Option Number	PGA Gain	Input Voltage Range
0	0.125	±7.84 V
1	0.5	±1.96 V
2	2	±490 mV
3	8	±123 mV
4	0.333	±2.94V
5	0.8	±1.25V
6	N/A	N/A (internal use only)
7	1.4	±700mV

8.1.3 Monitoring System IIR Filter

The monitoring ADC includes an Infinite Impulse Response (IIR) filter to reduce noise and improve accuracy. The IIR filter has the following transfer function:

(EQ. 5)
$$Average = \frac{NewSample - z^{-1} \times Average}{2^{-m}} + z^{-1} \times Average$$

The value of m can be independently set from 0 to 7 for each monitored rail, so the IIR can have the following values:

Table 21. IIR Coefficient Options

Option	IIR Averaging Value
0	1
1	1/2
2	1/4
3	1/8
4	1/16

Table 21. IIR Coefficient Options

Option	IIR Averaging Value
5	1/32
6	1/64
7	1/128

8.1.4 Sampling Rate

The sampling rates for different ADC channels are shown in Table 22.

Table 22. ADC Sampling Rate of Different Inputs

PMIC Outputs (Buck1-5, LDO1-2)	PMIC Internal	ADC 1-5 Pins without MUX	ADC 1-5 Pins with MUX
40µs	40µs	100µs	320µs

8.1.5 ADC Data Format

The data in all ADC registers follow the S13.2 data format, for example, this is a 16-bit signed number with an LSB of 0.25mV (or 0.25°C for temperature readings). Some of the ADC inputs have an attenuation before the PGA, so the scaling factor in Table 19 is not the same for all channels.

To convert an ADC value to a real number, perform the following calculation:

1. Convert digital value to a signed number
2. Divide by the scaling factor specified in Table 19

Examples:

Channel VOUT_1_ADCMON_VOUT = 0x13E8 (decimal 5096)

- Value / Scaling_factor = 5096 / 4000 = 1.274V

Channel ADCMON_Temp = 0xFFAD (decimal -83)

- Value / Scaling_factor = -83/4 = -20.75°C

Channel PVIN_2_ADCMON_PVIN = 0x0A5E (decimal 2654)

- Value / Scaling_factor = 2654/533 = 4.98V

8.2 Overvoltage (OV) and Undervoltage (UV) Monitoring

Using the SAR ADC, all internal and external voltages of RAA271000 are continuously monitored and compared against a digital Overvoltage (OV) and Undervoltage (UV) value. If any of these signals is outside of the OV and UV levels, a protection fault is triggered.

The OV and UV levels for all internal and external regulators are factory programmed in one-time programmable memory, but can be specified by the customer for each application.

The full list of regulators that are monitored for OV and UV conditions is show in Table 19.

8.3 Over-Temperature Warning and Shutdown

Similar to OV and UV protection for voltages, the protection side temperature sensor is monitored by the ADC and temperature thresholds can be set, namely a Warning threshold and a Shutdown threshold. Both of these thresholds can be specified by the customer, are factory programmed in one-time programmable memory and can be any temperature value with a resolution of 0.25°C.

8.4 Watchdog Timer (WDT)

RAA271000 contains a watchdog timer that can be used in several ways to ensure that the PMIC is still alive and able to respond to serial commands. The following are the three watchdog options available in RAA271000:

- A 16-question watchdog
- A 4-question watchdog
- A windowed watchdog function

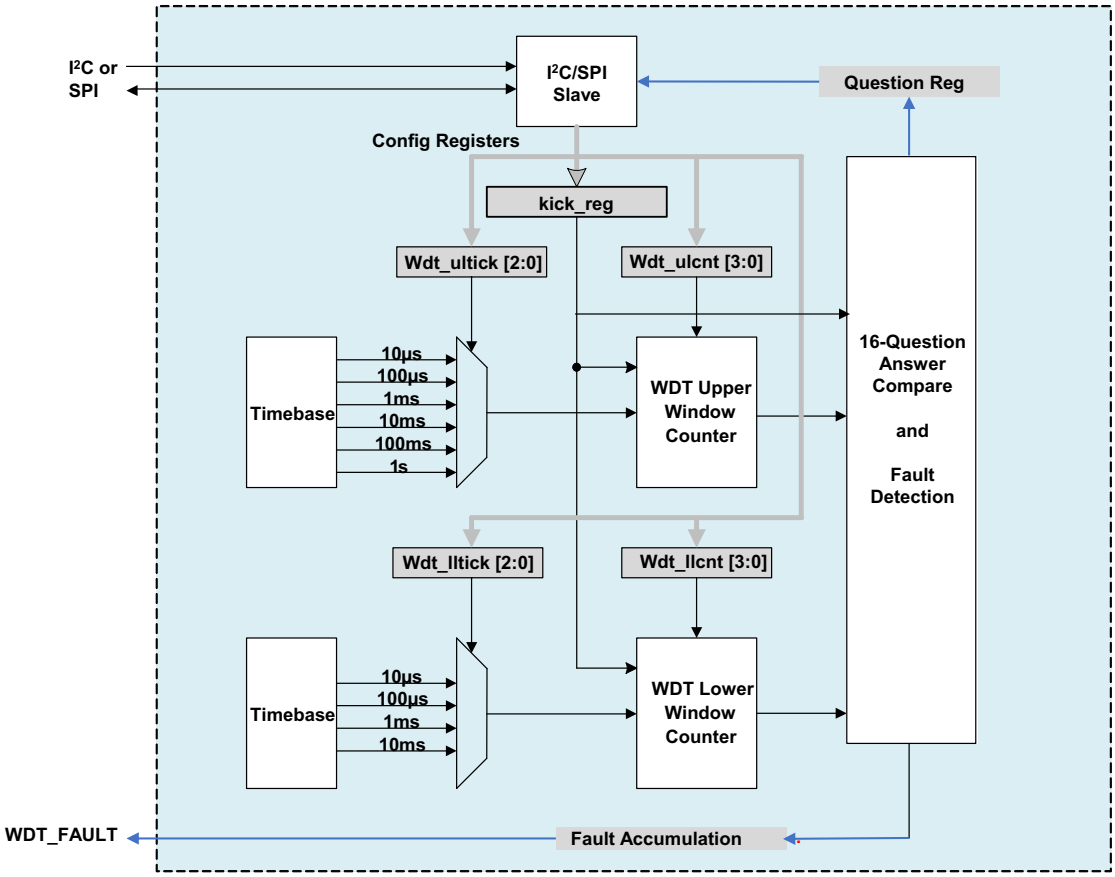


Figure 21. 16-Question Watchdog Timer

8.4.1 16-Question Watchdog Timer (QA16WDT)

In the 16-Q&A watchdog mode, RAA271000 provides a Token value by reading the top four bits of register 0xC9 - WDT_LFSR. After sending the token, RAA271000 expects the four answer bytes to be written to register 0xC8 - WDT_KICK_REG in the order Answer-0, Answer-1, Answer-2, and Answer-3 with the values shown in Table 23.

Table 23. QA16WDT Questions and Answers

Token	Watchdog Answer			
	Answer-3	Answer-2	Answer-1	Answer-0
0x0	0xFF	0x0F	0xF0	0x00
0x1	0xB0	0x40	0xBF	0x4F
0x2	0xE9	0x19	0xE6	0x16
0x3	0xA6	0x56	0xA9	0x59
0x4	0x75	0x85	0x7A	0x8A
0x5	0x3A	0xCA	0x35	0xC5

Table 23. QA16WDT Questions and Answers (Cont.)

Token	Watchdog Answer			
	Answer-3	Answer-2	Answer-1	Answer-0
0x6	0x63	0x93	0x6C	0x9C
0x7	0x2C	0xDC	0x23	0xD3
0x8	0xD2	0x22	0xDD	0x2D
0x9	0x9D	0x6D	0x92	0x62
0xA	0xC4	0x34	0xCB	0x3B
0xB	0x8B	0x7B	0x84	0x74
0xC	0x58	0xA8	0x57	0xA7
0xD	0x17	0xE7	0x18	0xE8
0xE	0x4E	0xBE	0x41	0xB1
0xF	0x01	0xF1	0x0E	0xFE

Note: It is possible to simplify the table slightly by noticing that some of the answers have just the MSB, LSB, or full value of Answer-0 flipped. Using C syntax:

- Answer-1 = Answer-0 ^ 0xF0
- Answer-2 = Answer-0 ^ 0x0F
- Answer-3 = Answer-0 ^ 0xFF

8.4.2 4-Question Watchdog Timer (QA4WDT)

The 4-Q&A watchdog mode is similar to the 16-Q&A watchdog, but the number of questions is reduced to four and there is only one answer. In QA4WDT mode, bits [7:6] of register 0xC9 - WDT_LFSR read the Token, and bits [5:0] compute the WD answer. As with the QA16WDT, the answer is written back to register 0xC8 - WDT_KICK_REG.

Table 24. QA4WDT Questions and Answers

Token Read From WDT_LFSR		WD Answer To be written to WDT_KICK_REG
WDT_LFSR <7>	WDT_LFSR <6>	
0	0	WDT_LFSR <5:0>
0	1	WDT_LFSR <5:0> shifted one bit to the left
1	0	WDT_LFSR <5:0> shifted one bit to the right
1	1	Inverse of WDT_LFSR <5:0>

8.4.3 Windowed Watchdog Timer (WWDT)

The watchdog function can also be used in a basic Windowed Kick mode. When configured this way, the PMIC expects the value 0x2A to be continuously written to register 0xC8 - WDT_KICK_REG within the configured time window.

8.5 Protection Interrupt Pin (INTb)

RAA271000 contains an interrupt pin (INTb) that reacts to faults in the protection digital. This pin is a push-pull output that is powered by the VIO supply and asserts LO when a fault is recorded.

INTb reacts to the following:

- Protection digital internal logic faults (such as self test, clock monitor)
- Watchdog faults
- CRC communication faults
- AVIN/GND OV/UV faults
- Internal reference OV/UV faults
- Internal LDO OV/UV faults
- Buck regulator OV/UV faults
- LDO regulator OV/UV faults
- External ADC channel OV/UV faults
- Faults related to OTP (one-time programmable memory)

Note: A full list of faults and their reactions is located in the RAA271000 Safety Application Note.

8.6 Monitoring Configuration Lock Bit

RAA271000 includes a lock bit for the monitoring hardware. While this bit is asserted, all registers that change the configuration of the monitoring block are locked and cannot be written by you (including fault masking). When this bit is de-asserted, the registers can be written as normal.

8.7 Debug Mode and Fault Lockout Fuse

RAA271000 includes a fault lockout bit implemented using a polyfuse. Before the fuse is blown, all fault modes in the protection block are masked to help with initial setup of the device. After the polyfuse is electrically blown, the device returns to normal operation and all faults in the protection block work as normal.

9. Register Maps

The RAA271000 contains two separate register spaces: one to control the power management functions (the Regulation register map), and one to control protection related functions (the Protection register map). If the RAA271000 is configured with I^2C communication (pin modes 1, 2, 3, or 5), Regulation and Protection can be accessed individually by communicating to different I^2C slave addresses. These slave addresses are set in one time-programmable memory.

If RAA271000 is configured with SPI communication (pin modes 0, 4, or 5), the Regulation registers can be accessed by asserting SS_B, and the Protection registers can be accessed by asserting SS_B2 while communicating over the MOSI, MISO, and SCLK pins.

9.1 Regulation Register Map

9.1.1 0x00 - RESERVED

Bit	Name	R/W	Description	Default
7:4	Reserved	RO		0x0
3:0	Reserved	RW		0x0

9.1.2 0x01 - IO_CHIPNAME_REGU

Bit	Name	R/W	Description	Default
7:0	IO_CHIPNAME	RO	Chip Name, Set by Renesas in metal 0x01: RAA271000	0x01

9.1.3 0x02 - IO_CHIPVERSION_REGU

Bit	Name	R/W	Description	Default
7:0	IO_CHIPVERSION	RO	Chip Version, Set by Renesas in metal 0x01: RAA271000	0x01

9.1.4 0x03 - IO_DIEID3_REGU

Bit	Name	R/W	Description	Default
7:0	IO_DIEID3	RO	Byte 3 of Die ID set by Renesas	0xFE

9.1.5 0x04 - IO_DIEID2_REGU

Bit	Name	R/W	Description	Default
7:0	IO_DIEID2	RO	Byte 2 of Die ID set by Renesas	0xDC

9.1.6 0x05 - IO_DIEID1_REGU

Bit	Name	R/W	Description	Default
7:0	IO_DIEID1	RO	Byte 1 of Die ID set by Renesas	0xBA

9.1.7 0x06 - IO_DIEID0_REGU

Bit	Name	R/W	Description	Default
7:0	IO_DIEID0	RO	Byte 0 of Die ID set by Renesas	0x98

9.1.8 0x0A - OTP_VERSION_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_VERSION	RO	OTP version for registers	0x01

9.1.9 0x0B - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RO		0x00

9.1.10 0x0C - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.11 0x0D - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RO		0x00

9.1.12 0x0E - OTP_CALCCRCMSB_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_CALCCRCMSB	RO	Upper byte of calculated CRC	0x00

9.1.13 0x0F - OTP_CALCCRCLSB_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_CALCCRCLSB	RO	Lower byte of calculated CRC	0x00

9.1.14 0x10 - OTP_RWADDR_REGU

Bit	Name	R/W	Description	Default
7	OTP_CRC_FAULT	RO	OTP download CRC fail 0x1: CRC fail on OTP download 0x0: CRC pass on OTP download	0x0
6	Reserved	RO		0x0
5:4	Reserved	RW		0x0
3:0	Reserved	RW		0x0

9.1.15 0x11 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.16 0x12 - OTP_CRCMSB_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_CRCMSB	RO		0x00

9.1.17 0x13 - OTP_CRCLSB_REGU

Bit	Name	R/W	Description	Default
7:0	OTP_CRCLSB	RO		0x00

9.1.18 0x22 - IO_MODECTRL_REGU

Bit	Name	R/W	Description	Default
7	IO_BUCK1_EN	RW	Enable for BUCK1 0x0: Buck1 Disabled 0x1: Buck1 Enabled	0x1
6	IO_BUCK2_EN	RW	Enable for BUCK2 0x0: Buck2 Disabled 0x1: Buck2 Enabled	0x1
5	IO_BUCK3_EN	RW	Enable for BUCK3 0x0: Buck3 Disabled 0x1: Buck3 Enabled	0x1
4	IO_BUCK4_EN	RW	Enable for BUCK4 0x0: Buck4 Disabled 0x1: Buck4 Enabled	0x1
3	IO_BUCK5_EN	RW	Enable for BUCK5 0x0: Buck5 Disabled 0x1: Buck5 Enabled	0x1
2	IO_LDO1_EN	RW	Enable for LDO1 0x0: LDO1 Disabled 0x1: LDO1 Enabled	0x1
1	IO_LDO2_EN	RW	Enable for LDO1 0x0: LDO1 Disabled 0x1: LDO1 Enabled	0x1
0	IO_REGVALID	RW	0x0: OTP not programmed or OTP read failed CRC All Registers set to POR values Buck is not allowed to power up even if BUCK[5:1]_EN[0] = 1 0x1: OTP read successful Registers set to OTP values Buck is allowed to power up if BUCK[5:1]_EN = 1	0x0

9.1.19 0x23 - CHIPSTATUS

Bit	Name	R/W	Description	Default
7	BG_BANDGAPOK	RO	Bandgap State 0x0: Bandgap outside of range 0x1: Bandgap operating in proper range	0x0
6	INTLDO_VDDOK	RO	VDD State (for both Analog and Digital LDO's and VBAT) 0x0: VBAT or Internal LDOs (Analog or Digital) outside of range 0x1: VBAT and Internal LDOs (Analog and Digital) operating properly	0x0
5:0	READONLY_RSVD	RO		0x00

9.1.20 0x24 - CHIPTSTATE_DCM

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK1_DCMSTATE	RO		0x0
3	BUCK2_DCMSTATE	RO		0x0
2	BUCK3_DCMSTATE	RO		0x0
1	BUCK4_DCMSTATE	RO		0x0
0	BUCK5_DCMSTATE	RO		0x0

9.1.21 0x25 - CHIPTSTATE_PGOOD

Bit	Name	R/W	Description	Default
7	Reserved	RO		0x0
6	LDO1_PGOODSTATE	RO	LDO1 Power-Good State 0x1: LDO1 is not undervoltage after soft start completes	0x0
5	LDO2_PGOODSTATE	RO	LDO2 Power-Good State 0x1: LDO2 is not undervoltage after soft start completes	0x0
4	BUCK1_PGOODSTATE	RO	BUCK1 Power-Good State 0x1: Buck1 has completed ramping to its target voltage	0x0
3	BUCK2_PGOODSTATE	RO	BUCK2 Power-Good State 0x1: Buck2 has completed ramping to its target voltage	0x0
2	BUCK3_PGOODSTATE	RO	BUCK3 Power-Good State 0x1: Buck3 has completed ramping to its target voltage	0x0
1	BUCK4_PGOODSTATE	RO	BUCK4 Power-Good State 0x1: Buck4 has completed ramping to its target voltage	0x0
0	BUCK5_PGOODSTATE	RO	BUCK5 Power-Good State 0x1: Buck5 has completed ramping to its target voltage	0x0

9.1.22 0x30 - FLT_MASK_OTP

Bit	Name	R/W	Description	Default
7	Reserved	RW	Mask INT for OTP PROG WARN (1 out of 4 bit failed) 0x0: Passed to output pin 0x1: Masked from output pin	0x0
6	Reserved	RW	Mask INT for OTP PROG ADDR failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
5	Reserved	RW	Mask INT for OTP PROG failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASKOTPINIT	RW	Mask INT for OTP INIT failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASKOTPCRCPAGE2	RW	Mask INT for OTP CRC Page 2 failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
2	FLT_MASKOTPCRCPAGE01	RW	Mask INT for OTP CRC Page 0 failure 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASKOTPTIMEOUT	RW	Mask INT for FLT_OTPTIMEOUT[0] Fault 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASKOTPNOTPGMD	RW	Mask INT for FLT_OTPNOTPGMD[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.23 0x31 - FLT_MASK_TEMP

Bit	Name	R/W	Description	Default
7	FLT_MASKBOOT	RW	Mask INT for FLT_BOOT[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
6:2	Reserved	RO		0x00
1	FLT_MASKTEMPSDR	RW	Mask INT for FLT_TEMPSDR[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASKTEMPSDF	RW	Mask INT for FLT_TEMPSDF[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.24 0x32 - FLT_MASK_BUCK1

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5	FLT_MASK_BUCK1_BOOTUV	RW	Mask INT for FLT_BUCK1_BOOTUV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASK_BUCK1_LSWUC	RW	Mask INT for FLT_BUCK1_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_BUCK1_LSWOC	RW	Mask INT for FLT_BUCK1_LSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x1
2	FLT_MASK_BUCK1_HSWOC	RW	Mask INT for FLT_BUCK1_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK1_OV	RW	Mask INT for FLT_BUCK1_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK1_UV	RW	Mask INT for FLT_BUCK1_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.25 0x33 - FLT_MASK_BUCK2

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_MASK_BUCK2_LSWUC	RW	Mask INT for FLT_BUCK2_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_BUCK2_LSWOC	RW	Mask INT for FLT_BUCK2_LSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x1
2	FLT_MASK_BUCK2_HSWOC	RW	Mask INT for FLT_BUCK2_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK2_OV	RW	Mask INT for FLT_BUCK2_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK2_UV	RW	Mask INT for FLT_BUCK2_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.26 0x34 - FLT_MASK_BUCK3

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_MASK_BUCK3_LSWUC	RW	Mask INT for FLT_BUCK3_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_BUCK3_LSWOC	RW	Mask INT for FLT_BUCK3_LSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x1
2	FLT_MASK_BUCK3_HSWOC	RW	Mask INT for FLT_BUCK3_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK3_OV	RW	Mask INT for FLT_BUCK3_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK3_UV	RW	Mask INT for FLT_BUCK3_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.27 0x35 - FLT_MASK_BUCK4

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5	FLT_MASK_BUCK4_PVIN_OK	RW	Mask INT for FLT_BUCK4_PVIN_OK[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
4	FLT_MASK_BUCK4_LSWUC	RW	Mask INT for FLT_BUCK4_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_BUCK4_LSWOC	RW	Mask INT for FLT_BUCK4_LSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x1
2	FLT_MASK_BUCK4_HSWOC	RW	Mask INT for FLT_BUCK4_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK4_OV	RW	Mask INT for FLT_BUCK4_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK4_UV	RW	Mask INT for FLT_BUCK4_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.28 0x36 - FLT_MASK_BUCK5

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_MASK_BUCK5_LSWUC	RW	Mask INT for FLT_BUCK5_LSWUC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
3	FLT_MASK_BUCK5_LSWOC	RW	Mask INT for FLT_BUCK5_LSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x1
2	FLT_MASK_BUCK5_HSWOC	RW	Mask INT for FLT_BUCK5_HSWOC[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_BUCK5_OV	RW	Mask INT for FLT_BUCK5_OV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_BUCK5_UV	RW	Mask INT for FLT_BUCK5_UV[0] 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.29 0x37 - FLT_MASK_LDO

Bit	Name	R/W	Description	Default
7:2	Reserved	RO		0x00
1	FLT_MASK_LDO2_UV	RW	Mask INT for FLT_LDO2_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_LDO1_UV	RW	Mask INT for FLT_LDO1_UV 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.30 0x38 - FLT_MASK_IF

Bit	Name	R/W	Description	Default
7:3	Reserved	RO		0x00
2	FLT_MASK_VBAT_OV	RW	Mask INT for FLT_VBAT_OV 0x0: Passed to output pin 0x1: Masked from output pin	0x0
1	FLT_MASK_SPI	RW	Mask INT for FLT_SPI 0x0: Passed to output pin 0x1: Masked from output pin	0x0
0	FLT_MASK_I2C	RW	Mask INT for FLT_I2C 0x0: Passed to output pin 0x1: Masked from output pin	0x0

9.1.31 0x040 - FLT_RECORD_OTP

Bit	Name	R/W	Description	Default
7	FLT_OTPPROGWARN	RW	OTP Program Warning that one of the four bits in different/redundant programming mode failed 0x0: All four bits programmed correctly 0x1: One out of four bits programmed incorrectly but overall bit is correct Read returns status. Write 0 to clear.	0x0
6	FLT_OTPPROGADDR	RW	OTP PROG ADDR failure 0x0: Programming address is in the correct range 0x1: Programming address is out of acceptable range Read returns status. Write 0 to clear.	0x0
5	FLT_OTPPROG	RW	OTP PROG failure 0x0: Programming passed 0x1: Programming failed Read returns status. Write 0 to clear.	0x0
4	FLT_OTPINIT	RW	OTP INIT failure 0x0: Read Initialization passed 0x1: Read Initialization failed Read returns status. Write 0 to clear.	0x0
3	FLT_OTPCRCPAGE2	RW	OTP CRC failure 0x0: No OTP Failure 0x1: OTP CRC Failure Read returns status. Write 0 to clear.	0x0
2	FLT_OTPCRCPAGE01	RW	OTP CRC failure 0x0: No OTP Failure 0x1: OTP CRC Failure Read returns status. Write 0 to clear.	0x0
1	FLT_OTPTIMEOUT	RW	OTP Read Duration Fault 0x0: No OTP Read Duration Fault 0x1: OTP Read Duration >= 256*Low Freq Clock Periods (~8ms) Read returns status. Write 0 to clear.	0x0
0	FLT_OTPNOTPGMD	RW	Read of OTP to see if OTP has been programmed 0x0: No fault 0x1: Fault Read returns status. Write 0 to clear.	0x0

9.1.32 0x41 - FLT_RECORD_TEMP

Bit	Name	R/W	Description	Default
7	FLT_BOOT	RW	BOOT occurred 0x0: No boot process has occurred since the last time this register was read 0x1: Boot process has occurred (set high after OTP Read is finished) Read returns status. Write 0 to clear.	0x0
6:2	Reserved	RO		0x00
1	FLT_TEMPSDR	RW	Over-Temperature (OT) Shutdown (rising threshold) 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_TEMPSDF	RW	Over-Temperature (OT) Shutdown (falling edge) (Shutdown – Hysteresis) 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0

9.1.33 0x42 - FLT_RECORD_BUCK1

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5	FLT_BUCK1_BOOTUV	RW	Boot Undervoltage (BOOTUV) for BUCK1 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
4	FLT_BUCK1_LSWUC	RW	LS Way Undercurrent (WOC) for BUCK1 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
3	Reserved	RW		0x0
2	FLT_BUCK1_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK1 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_BUCK1_OV	RW	Overvoltage (OV) for BUCK1 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_BUCK1_UV	RW	Undervoltage (UV) for BUCK1 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.34 0x43 - FLT_RECORD_BUCK2

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_BUCK2_LSWUC	RW	LS Way Undercurrent (WOC) for BUCK2 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
3	Reserved	RW		0x0
2	FLT_BUCK2_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK2 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_BUCK2_OV	RW	Overvoltage (OV) for BUCK2 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_BUCK2_UV	RW	Undervoltage (UV) for BUCK2 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.35 0x44 - FLT_RECORD_BUCK3

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_BUCK3_LSWUC	RW	LS Way Undercurrent (WOC) for BUCK3 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
3	Reserved	RW		0x0
2	FLT_BUCK3_HSWOC	RW	HS Way Overcurrent (WOC) for BUCK3 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_BUCK3_OV	RW	Overvoltage (OV) for BUCK3 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_BUCK3_UV	RW	Undervoltage (UV) for BUCK3 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.36 0x45 - FLT_RECORD_BUCK4

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5	FLT_BUCK4_PVIN4_OK	RW	PVIN4_OK for BUCK4 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0
4	FLT_BUCK4_LSWUC	RW	LS Way Undercurrent (WOC) for BUCK4 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
3	Reserved	RW		0x0
2	FLT_BUCK4_HSWOC	RW	Way Overcurrent (WOC) for BUCK4 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_BUCK4_OV	RW	Overvoltage (OV) for BUCK4 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_BUCK4_UV	RW	Undervoltage (UV) for BUCK4 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.37 0x46 - FLT_RECORD_BUCK5

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FLT_BUCK5_LSWUC	RW	LS Way Undercurrent (WOC) for BUCK5 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
3	Reserved	RW		0x0
2	FLT_BUCK5_HSWOC	RW	Way Overcurrent (WOC) for BUCK5 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_BUCK5_OV	RW	Overvoltage (OV) for BUCK5 0x0: No fault, Less than threshold 0x1: Fault, greater than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_BUCK5_UV	RW	Undervoltage (UV) for BUCK5 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.38 0x47 - FLT_RECORD_LDO

Bit	Name	R/W	Description	Default
7:2	Reserved	RO		0x00
1	FLT_LDO2_UV	RW	Undervoltage (UV) for LDO2 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0
0	FLT_LDO1_UV	RW	Undervoltage (UV) for LDO1 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0

9.1.39 0x48 - FLT_RECORD_IF

Bit	Name	R/W	Description	Default
7:3	Reserved	RO		0x00
2	FLT_VBAT_OV	RW	VBAT Overvoltage 0x0: No fault, greater than threshold 0x1: Fault, less than threshold Read returns status. Write 0 to clear.	0x0
1	FLT_SPI	RW	SPI CRC error 0x0: No fault detected 0x1: Fault detected Read returns status. Write 0 to clear.	0x0
0	FLT_I2C	RW	I2C CRC error 0x0: No fault detected 0x1: Fault detected Read returns status. Write 0 to clear.	0x0

9.1.40 0x50 - IO_GP2CFGMSB

Bit	Name	R/W	Description	Default
7:5	Reserved	RW		0x0
4	Reserved	RW		0x0
3:2	IO_GP2PULLUPDOWN	RW	Selects the pull up on Pin GPIO13 0x0: No pull up or pull down 0x1: Pull Down of 10µA/180kΩ 0x2: Pull Up of 30µA/60kΩ 0x3: Pull Up of 1µA/1.8MΩ	0x0
1:0	IO_GP2DRIVE	RW	Selects output drive strength of Pin GPIO13 The peak current level depends on the supply 0x0: Min (20% of Max) 0x1: 50% of Max 0x2: 80% of Max 0x3: Max	0x0

9.1.41 0x51 - IO_GP2CFGLSB

Bit	Name	R/W	Description	Default
7	IO_GP2DIGDIRECTION	RW	Digital Data Direction of GPIO13 0x0: Output I/O acts like an output pad 0x1: Input Output devices are turned off and pin functions as an input	0x1
6	IO_GP2OPENDRAIN	RW	Modifies Digital Output Mode of GPIO13 0x0: Configure as a CMOS output buffer 0x1: Configure as an open-drain output with any pull-up or pull-down set by IO_GP2PullUpDown[1:0]	0x0
5	IO_GP2INVERT	RW	Polarity Control for input and Output of GPIO13 0x0: Noninverting buffers are used on both the input and the output 0x1: Inverting buffers are used on both the input and the output	0x0
4	Reserved	RW		0x0
3	Reserved	RW		0x0
2	SSP2_LOCK	RW		0x1
1	SSP2_ASSERT	RW		0x0
0	Reserved	RO		0x0

9.1.42 0x52 - IO_GP3CFGMSB

Bit	Name	R/W	Description	Default
7:5	Reserved	RW		0x0
4	Reserved	RW		0x0
3:2	IO_GP3PULLUPDOWN	RW	Selects the pull up on Pin GPIO14 0x0: No pull-up or pull-down 0x1: Pull-down of 10µA/180kΩ 0x2: Pull-up of 30µA/60kΩ 0x3: Pull-up of 1µA/1.8MΩ	0x0
1:0	IO_GP3DRIVE	RW	Selects output drive strength of Pin GPIO14 The peak current level depends on the supply 0x0: Min (20% of Max) 0x1: 50% of Max 0x2: 80% of Max 0x3: Max	0x0

9.1.43 0x53 - IO_GP3CFGLSB

Bit	Name	R/W	Description	Default
7	IO_GP3DIGDIRECTION	RW	Digital Data Direction for GPIO14 0x0: Output I/O acts like an output pad 0x1: Input Output devices are turned off and pin functions as an input	0x1
6	IO_GP3OPENDRAIN	RW	Modifies Digital Output Mode of GPIO14 0x0: Configure as a CMOS output buffer 0x1: Configure as an open-drain output with any pull-up or pull-down set by IO_GP3PullUpDown[1:0]	0x0
5	IO_GP3INVERT	RW	Polarity Control for input and Output of GPIO14 0x0: Noninverting buffers are used on both the input and the output 0x1: Inverting buffers are used on both the input and the output	0x0
4	Reserved	RW		0x0
3	Reserved	RW		0x0
2:0	Reserved	RO		0x0

9.1.44 0x54 - IO_GPIO_DATA

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:4	IO_GPIO_DATAIN	RO	2-bit GPIO data inputs written through the GPIO and stored in register for Software Read The IO_GPxCFGxSB need to be configured accordingly. IO_GPxDIGDIRECTION should be set to input (0x1)	0x0
3:2	Reserved	RO		0x0
1:0	IO_GPIO_DATAOUT	RW	2-bit GPIO data outputs for software to control devices in the system. The IO_GPxCFGxSB need to be configured accordingly. IO_GPxDIGDIRECTION should be set to Output (0x0)	0x0

9.1.45 0x58 - LOCK_OUT_CFG

Bit	Name	R/W	Description	Default
7:0	LOCK_OUT_CFG	RW		0x00

9.1.46 0x60 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.47 0x61 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.48 0x62 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.49 0x63 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.50 0x68 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.51 0x69 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.52 0x6A - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.53 0x6B - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.1.54 0x70 - BUCK1_DVS0CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK1_DVS0VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck1 V_{OUT} for DVS configuration 0 V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xD7

9.1.55 0x71 - BUCK1_DVS0CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK1_DVS0VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck1 V_{OUT} for DVS config 0 For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK1_DVS0DECAY	RW	Buck1 DECAY setting 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.56 0x72 - BUCK1_DVS1CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK1_DVS1VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck1 V_{OUT} for DVS configuration 1 V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xAD

9.1.57 0x73 - BUCK1_DVS1CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK1_DVS1VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck1 V_{OUT} for DVS configuration 1 For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK1_DVS1DECAY	RW	Buck DECAY for DVS Config 1 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.58 0x74 - BUCK1_DVSCFG

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK1_PGOODDAC0V	RW	Power-Good State when BUCK1 DAC is set to 0V 0x0: BUCK1_PGOOD is set low when DAC is set to 0V 0x1: BUCK1_PGOOD is allowed to stay high when DAC is set to 0V	0x0
3:2	BUCK1_PGOODDELAY	RW	Delay before PGOOD signal is set (no delay when cleared) Delay = BUCK1_PGOODDELAY[1:0] (32kHz # of Clocks) 0x0: 0µs (0) 0x1: 125µs (4) 0x2: 375µs (12) 0x3: 1000µs (32)	0x0
1:0	Reserved	RO		0x0

9.1.59 0x75 - BUCK1_DVSSEL

Bit	Name	R/W	Description	Default
7:2	Reserved	RO		0x00
1	BUCK1_DVSCTRL	RW	BUCK1 DVS Control 0x0: Use BUCK_DVSSELECT[0] to select active DVS configuration 0x1: Use DVS Pin to control DVS selection	0x0
0	BUCK1_DVSSELECT	RW	BUCK DVS Selection 0x0: Use DVS Config 0 in BUCK_DVS0CFG and BUCK_DVS0VOUT 0x1: Use DVS Config 1 in BUCK_DVS1CFG and BUCK_DVS1VOUT **Note:** When BUCK_DVSCTRL[0] = 0x0 any write to the register BUCK_DVSSEL causes a DVS ramping event to occur	0x0

9.1.60 0x76 - BUCK1_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK1_EN_DLY	RW	Delay time from EN pin and IO_REGVAID go high to internal BUCK_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.61 0x77 - BUCK1_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK1_SHUTDN_DLY	RW	Delay time from EN pin or IO_REGVAID go low to internal BUCK_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.62 0x80 - BUCK2_DVS0CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK2_DVS0VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck2 V_{OUT} V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xFF

9.1.63 0x81 - BUCK2_DVS0CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK2_DVS0VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck2 V_{OUT}. For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK2_DVS0DECAY	RW	Buck2 DECAY 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.64 0x82 - BUCK2_DVSCFG

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK2_PGOODDAC0V	RW	Power-Good State when BUCK2 DAC is set to 0V 0x0: BUCK_PGOOD is set low when DAC is set to 0V 0x1: BUCK_PGOOD is allowed to stay high when DAC is set to 0V	0x0
3:2	BUCK2_PGOODDELAY	RW	Delay before PGOOD signal is set (no delay when cleared) Delay = BUCK_PGOODDELAY[1:0] (32kHz # of Clocks) 0x0: 0µs (0) 0x1: 125µs (4) 0x2: 375µs (12) 0x3: 1000µs (32)	0x0
1:0	Reserved	RO		0x0

9.1.65 0x86 - BUCK2_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK2_EN_DLY	RW	Delay time from EN pin and IO_REGVAID go high to internal BUCK_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.66 0x87 - BUCK2_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK2_SHUTDN_DLY	RW	Delay time from BUCK_EN pin or IO_REGVAID go low to internal BUCK_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.67 0x90 - BUCK3_DVS0CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK3_DVS0VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck3 V_{OUT} V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xFF

9.1.68 0x91 - BUCK3_DVS0CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK3_DVS0VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck3 V_{OUT}. For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK3_DVS0DECAY	RW	Buck3 DECAY 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.69 0x92 - BUCK3_DVSCFG

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK3_PGOODDAC0V	RW	Power-Good State when BUCK3 DAC is set to 0V 0x0: BUCK_PGOOD is set low when DAC is set to 0V 0x1: BUCK_PGOOD is allowed to stay high when DAC is set to 0V	0x0
3:2	BUCK3_PGOODDELAY	RW	Delay before PGOOD signal is set (no delay when cleared) Delay = BUCK_PGOODDELAY[1:0] (32kHz # of Clocks) 0x0: 0µs (0) 0x1: 125µs (4) 0x2: 375µs (12) 0x3: 1000µs (32)	0x0
1:0	Reserved	RO		0x0

9.1.70 0x96 - BUCK3_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK3_EN_DLY	RW	Delay time from BUCK_EN pin and IO_REGVAID go high to BUCK_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.71 0x97 - BUCK3_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK3_SHUTDN_DLY	RW	Delay time from BUCK_EN pin or IO_REGVAID go low to BUCK_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.72 0xA0 - BUCK4_DVS0CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK4_DVS0VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck3 V_{OUT} V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xFF

9.1.73 0xA1 - BUCK4_DVS0CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK4_DVS0VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck4 V_{OUT} For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK4_DVS0DECAY	RW	Buck4 DECAY 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.74 0xA2 - BUCK4_DVSCFG

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK4_PGOODDAC0V	RW	Power-Good State when BUCK4 DAC is set to 0V 0x0: BUCK_PGOOD is set low when DAC is set to 0V 0x1: BUCK_PGOOD is allowed to stay high when DAC is set to 0V	0x0
3:2	BUCK4_PGOODDELAY	RW	Delay before PGOOD signal is set (no delay when cleared) Delay = BUCK_PGOODDELAY[1:0] (32kHz # of Clocks) 0x0: 0µs (0) 0x1: 125µs (4) 0x2: 375µs (12) 0x3: 1000µs (32)	0x0
1:0	Reserved	RO		0x0

9.1.75 0xA6 - BUCK4_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK4_EN_DLY	RW	Delay time from BUCK_EN pin and IO_REGVAID go high to internal BUCK_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.76 0xA7 - BUCK4_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK4_SHUTDN_DLY	RW	Delay time from BUCK_EN pin or IO_REGVAID go low to internal BUCK_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.77 0xB0 - BUCK5_DVS0CFG1

Bit	Name	R/W	Description	Default
7:0	BUCK5_DVS0VOUT92	RW	Upper eight bits of 10-bit DAC[9:0] value to generate Buck5 V_{OUT} V_{OUT} (V) = (1.2V / FBDIV) * (DAC[9:0] / 210) FBDIV is from BUCK_VOUTFBDIV[1:0] = (1.0, 0.8, 0.6, 0.5) **Note:** V_{OUT} must be programmed between 0.3V and 3.3V For more details on output voltage selection, see Buck Output Voltage Selection	0xFF

9.1.78 0xB1 - BUCK5_DVS0CFG0

Bit	Name	R/W	Description	Default
7:6	BUCK5_DVS0VOUT10	RW	Lower two bits of 10-bit DAC[9:0] value to generate Buck5 V_{OUT} For more details on output voltage selection, see Buck Output Voltage Selection	0x3
5	BUCK5_DVS0DECAY	RW	Buck5 DECAY 0x0: Active pull-down, decay determined by selected slew rate 0x1: Decay Mode (load determines slew rate)	0x0
4:1	Reserved	RO		0x0
0	Reserved	RW		0x0

9.1.79 0xB2 - BUCK5_DVSCFG

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	BUCK5_PGOODDAC0V	RW	Power-Good State when in BUCK DAC is set to 0V 0x0: BUCK_PGOOD is set low when DAC is set to 0V 0x1: BUCK_PGOOD is allowed to stay high when DAC is set to 0V	0x0
3:2	BUCK5_PGOODDELAY	RW	Delay before PGOOD signal is set (no delay when cleared) Delay = BUCK_PGOODDELAY[1:0] /32kHz # of Clocks 0x0: 0µs 0 0x1: 125µs 4 0x2: 375µs 12 0x3: 1000µs 32	0x0
1:0	Reserved	RO		0x0

9.1.80 0xB6 - BUCK5_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK5_EN_DLY	RW	Delay time from BUCK_EN pin and IO_REGVAID go high to internal BUCK_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.81 0xB7 - BUCK5_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	BUCK5_SHUTDN_DLY	RW	Delay time from BUCK_EN pin or IO_REGVAID go low to internal BUCK_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.82 0xC0 - LDO1_VOUT_CORE

Bit	Name	R/W	Description	Default
7:0	LDO1_VOUT_CORE	RW	8-bit DAC value for LDO1 output voltage selection. 1LSB = 15.4mV. For more information on LDO output voltage selection, see LDO Output Voltage	0x4E

9.1.83 0xC1 - LDO2_VOUT_CORE

Bit	Name	R/W	Description	Default
7:0	LDO2_VOUT_CORE	RW	8-bit DAC value for LDO2 output voltage selection. 1LSB = 15.4mV. For more information on LDO output voltage selection, see LDO Output Voltage	0x4E

9.1.84 0xC2 - LDO_EN

Bit	Name	R/W	Description	Default
7	EN_LDO1_OC	RW	Overcurrent protection setting for LDO1 0x0: LDO1 overcurrent protection disabled 0x1: LDO1 overcurrent protection enabled	0x1
6	EN_LDO2_OC	RW	Overcurrent protection setting for LDO2 0x0: LDO2 overcurrent protection disabled 0x1: LDO2 overcurrent protection enabled	0x1
5:0	Reserved	RO		0x00

9.1.85 0xC3 - LDO1_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	LDO1_EN_DLY	RW	Delay time from LDO_EN pin and IO_REGVALID go high to internal LDO_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.86 0xC4 - LDO1_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	LDO1_SHUTDN_DLY	RW	Delay time from LDO_EN pin or IO_REGVAID go low to internal LDO_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.87 0xC5 - LDO2_EN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	LDO2_EN_DLY	RW	Delay time from LDO_EN pin and IO_REGVALID go high to internal LDO_en control asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.88 0xC6 - LDO2_SHUTDN_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	LDO2_SHUTDN_DLY	RW	Delay time from LDO_EN pin or IO_REGVAID go low to internal LDO_en control de-asserted. Delay = (integer value of register) ms [1.07ms/LSB]	0x00

9.1.89 0xC7 - HICCUP_RESTRT_DLY

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5:0	HICCUP_RESTRT_DLY	RW	Restart delay time for LDO after faulting when hiccup is enabled. Delay = (integer value of register) ms (1.07ms/LSB) Value is used for LDO1 and LDO2.	0x00

9.2 Protection Register Map

9.2.1 0x00 - RESERVED

Bit	Name	R/W	Description	Default
7:4	Reserved	RO		0x0
3:0	Reserved	RW		0x0

9.2.2 0x01 - IO_CHIPNAME

Bit	Name	R/W	Description	Default
7:0	IO_CHIPNAME	RO	Chip name, set by Renesas in metal 0x01: RAA271000	0x01

9.2.3 0x02 - IO_CHIPVERSION

Bit	Name	R/W	Description	Default
7:0	IO_CHIPVERSION	RO	Chip version, set by Renesas in metal 0x01: RAA271000	0x01

9.2.4 0x03 - IO_DIEID3

Bit	Name	R/W	Description	Default
7:0	IO_DIEID3	RO	Byte 3 of Die ID set by Renesas	0xFE

9.2.5 0x04 - IO_DIEID2

Bit	Name	R/W	Description	Default
7:0	IO_DIEID2	RO	Byte 2 of Die ID set by Renesas	0xDC

9.2.6 0x05 - IO_DIEID1

Bit	Name	R/W	Description	Default
7:0	IO_DIEID1	RO	Byte 1 of Die ID set by Renesas	0xBA

9.2.7 0x06 - IO_DIEID0

Bit	Name	R/W	Description	Default
7:0	IO_DIEID0	RO	Byte 0 of Die ID set by Renesas	0x98

9.2.8 0x07 - IO_CHIPSTATE

Bit	Name	R/W	Description	Default
7	BG_BANDGAPOK	RO	Bandgap State 0x0 Bandgap outside range 0x1 Bandgap within range	0x0
6	INTLDO_VDDOK	RO	Analog and digital LDOs and VBAT state 0x0 VBAT and internal LDOs outside range 0x1 VBAT and internal LDOs with in range	0x0
5	INTERRUPT	RO	Analog and digital LDOs and VBAT state 0x0 VBAT and internal LDOs outside range 0x1 VBAT and internal LDOs with in range	0x0
4:0	READONLY_RSVD	RO	Reserved	0x00

9.2.9 0x10 - FUSA_CTRL_1_A

See the Safety Application Note for details on this register.

9.2.10 0x11 - FUSA_CTRL_2

See the Safety Application Note for details on this register.

9.2.11 0x12 - FUSA_CTRL_3

See the Safety Application Note for details on this register.

9.2.12 0x13 - FUSA_CTRL_4

See the Safety Application Note for details on this register.

9.2.13 0x14 - FUSA_CTRL_5

See the Safety Application Note for details on this register.

9.2.14 0x15 - FUSA_CHK_CVM1

See the Safety Application Note for details on this register.

9.2.15 0x16 - FUSA_STATUS_CVM1

See the Safety Application Note for details on this register.

9.2.16 0x17 - FUSA_STATUS_CVM2

See the Safety Application Note for details on this register.

9.2.17 0x18 - FUSA_STATUS_CVM3

See the Safety Application Note for details on this register.

9.2.18 0x19 - FUSA_STATUS_CVM4

See the Safety Application Note for details on this register.

9.2.19 0x1A - FUSA_STATUS_CVM5

See the Safety Application Note for details on this register.

9.2.20 0x1B - FUSA_STATUS_1

See the Safety Application Note for details on this register.

9.2.21 0x1C - FUSA_STATUS_2

See the Safety Application Note for details on this register.

9.2.22 0x1D - FUSA_STATUS_3

See the Safety Application Note for details on this register.

9.2.23 0x1E - FUSA_STATUS_4

See the Safety Application Note for details on this register.

9.2.24 0x1F - FUSA_SOC_CHK_1

See the Safety Application Note for details on this register.

9.2.25 0x20 - IO_HOST_MSGCNT

See the Safety Application Note for details on this register.

9.2.26 0x21 - CLK_CNT_1

Bit	Name	R/W	Description	Default
7:0	FREERUN_CNT_UPPER	RO	Upper byte of free running counter (32MHz)	0x00

9.2.27 0x22 - CLK_CNT_2

Bit	Name	R/W	Description	Default
7:0	FREERUN_CNT_LOWER	RO	Lower byte of free running counter (32MHz)	0x00

9.2.28 0x30 - FLT_RECORD_A

See the Safety Application Note for details on this register.

9.2.29 0x31 - FLT_RECORD_B

See the Safety Application Note for details on this register.

9.2.30 0x32 - FLT_RECORD_GND_AVIN

Bit	Name	R/W	Description	Default
7:4	Reserved	RO		0x0
3	FaultStatus_AVIN2_Prot	RO	AVIN2 power supply (Protection) 0x0: AVIN2 monitoring is in range 0x1: AVIN2 monitoring is out of range	0x0
2	FaultStatus_AVIN1_Regu	RO	AVIN1 power supply (Regulation) 0x0: AVIN1 monitoring is in range 0x1: AVIN1 monitoring is out of range	0x0
1	FaultStatus_PGND_Regu	RO	Monitoring result for PGND (Regulation) 0x0: monitoring is in range 0x1: monitoring is out of range	0x0
0	FaultStatus_Offset	RO	Monitoring result for GND Protection 0x0: monitoring is in range 0x1: monitoring is out of range	0x0

9.2.31 0x33 - FLT_RECORD_BG_Temp

Bit	Name	R/W	Description	Default
7:6	Reserved	RO		0x0
5	FaultStatus_BG_REGU	RO	Bandgap (Regulation) status 0x0: Bandgap (Regulation) is in range 0x1: Bandgap (Regulation) is outside range	0x0
4	FaultStatus_TempShdn	RO	Temperature sensor severity status 0x0: Temperature is below critical shutdown temperature limit 0x1: Temperature is above critical shutdown temperature limit	0x0
3	FaultStatus_TempWarn	RO	Temperature sensor warning status 0x0: Temperature is below warning temperature limit 0x1: Temperature is above warning temperature limit	0x0
2:1	Reserved	RO		0x0
0	FaultStatus_TEMP2_SENSOR	RO	Temperature sensor health status 0x0: Val(Ref. TEMP Sensor) = Val(Temp Sensor) 0x1: Val(Ref. TEMP Sensor) ≠ Val(Temp Sensor)	0x0

9.2.32 0x34 - FLT_RECORD_IntLDOs

Bit	Name	R/W	Description	Default
7	FaultStatus_IntLDOProt_1	RO	Internal LDO 1 (Protection) Status 0x0: Internal LDO 1 (Protection) is in range 0x1: Internal LDO 1 (Protection) is outside range	0x0
6	FaultStatus_IntLDOProt_0	RO	Internal LDO 0 (Protection) Status 0x0: Internal LDO 0 (Protection) is in range 0x1: Internal LDO 0 (Protection) is outside range	0x0
5	FaultStatus_IntLDORegu_5	RO	Internal LDO 5 (Regulation) Status 0x0: Internal LDO 5 (Regulation) is in range 0x1: Internal LDO 5 (Regulation) is outside range	0x0
4	FaultStatus_IntLDORegu_4	RO	Internal LDO 4 (Protection) Status 0x0: Internal LDO 4 (Protection) is in range 0x1: Internal LDO 4 (Protection) is outside range	0x0
3	FaultStatus_IntLDORegu_3	RO	Internal LDO 3 (Regulation) Status 0x0: Internal LDO 3 (Regulation) is in range 0x1: Internal LDO 3 (Regulation) is outside range	0x0
2	FaultStatus_IntLDORegu_2	RO	Internal LDO 2 (Protection) Status 0x0: Internal LDO 2 (Protection) is in range 0x1: Internal LDO 2 (Protection) is outside range	0x0
1	FaultStatus_IntLDORegu_1	RO	Internal LDO 1 (Regulation) Status 0x0: Internal LDO 1 (Regulation) is in range 0x1: Internal LDO 1 (Regulation) is outside range	0x0
0	FaultStatus_IntLDORegu_0	RO	Internal LDO 0 (Protection) Status 0x0: Internal LDO 0 (Protection) is in range 0x1: Internal LDO 0 (Protection) is outside range	0x0

9.2.33 0x35 - FLT_RECORD_ExtLDOs

Bit	Name	R/W	Description	Default
7:5	Reserved	RO		0x0
4	FaultStatus_SPARE0	RO	VIO Status 0x0: Limit high > V(VIO) > limit low 0x1 V(VIO) > limit high or < limit low	0x0
3	FaultStatus_ExtLDORegu_3	RO	External LDO 3 Status 0x0: Limit high > V(ExtLDO_3) > limit low 0x1 V(ExtLDO_3) > limit high or < limit low	0x0
2	FaultStatus_ExtLDORegu_2	RO	External LDO 2 Status 0x0: Limit high > V(ExtLDO_2) > limit low 0x1 V(ExtLDO_2) > limit high or < limit low	0x0
1	FaultStatus_ExtLDORegu_1	RO	External LDO 1 Status 0x0: Limit high > V(ExtLDO_1) > limit low 0x1 V(ExtLDO_1) > limit high or < limit low	0x0
0	FaultStatus_ExtLDORegu_0	RO	External LDO 0 Status 0x0: Limit high > V(ExtLDO_0) > limit low 0x1 V(ExtLDO_0) > limit high or < limit low	0x0

9.2.34 0x36 - FLT_RECORD_BUCK15A

Bit	Name	R/W	Description	Default
7:3	Reserved	RO		0x00
2	FaultStatus_VOUT0_Buck15A	RO	VOUT1 (Remote voltage sense pin of 15A Buck1) Status 0x0: Limit high > VOUT1 > limit low 0x1 VOUT1 > limit high or < limit low	0x0
1	FaultStatus_PVIN0_Buck15A	RO	PVIN1 (power stage supply pin of 15A Buck1) Status 0x0: Limit high > PVIN1 > limit low 0x1 PVIN1 > limit high or < limit low	0x0
0	FaultStatus_PGND0_Buck15A	RO	PGND1 (power stage ground pin of 15A Buck1) Status 0x0: Limit high > PGND1 > limit low 0x1 PGND1 > limit high or < limit low	0x0

9.2.35 0x37 - FLT_RECORD_BUCKS

Bit	Name	R/W	Description	Default
7	FaultStatus_VOUT4_Buck1A	RO	VOUT5 (Remote voltage sense pin of Buck5) Status 0x0: Limit high > VOUT5 > limit low 0x1 VOUT5 > limit high or < limit low	0x0
6	FaultStatus_PVIN4_Buck1A	RO	PVIN5 (power stage supply pin of Buck5) Status 0x0: Limit high > PVIN5 > limit low 0x1 PVIN5 > limit high or < limit low	0x0
5	FaultStatus_VOUT3_Buck1A	RO	VOUT4 (Remote voltage sense pin of Buck4) Status 0x0: Limit high > VOUT4) > limit low 0x1 VOUT4 > limit high or < limit low	0x0
4	FaultStatus_PVIN3_Buck1A	RO	PVIN4 (power stage supply pin of 1A Buck 4) Status 0x0: Limit high > PVIN4 > limit low 0x1 PVIN4 > limit high or < limit low	0x0
3	FaultStatus_VOUT2_Buck1A	RO	VOUT3 (Remote voltage sense pin of 1A Buck3) Status 0x0: Limit high > VOUT3 > limit low 0x1 VOUT3 > limit high or < limit low	0x0
2	FaultStatus_PVIN2_Buck1A	RO	PVIN3 (power stage supply pin of 1A Buck3) Status 0x0: Limit high > PVIN3 > limit low 0x1 PVIN3 > limit high or < limit low	0x0
1	FaultStatus_VOUT1_Buck1A	RO	VOUT2 (Remote voltage sense pin of 1A Buck2) Status 0x0: Limit high > VOUT2 > limit low 0x1 VOUT2 > limit high or < limit low	0x0
0	FaultStatus_PVIN1_Buck1A	RO	PVIN2 (power stage supply pin of 1A Buck2) Status 0x0: Limit high > PVIN2 > limit low 0x1 PVIN2 > limit high or < limit low	0x0

9.2.36 0x38 - FLT_RECORD_ExtINPs_7_0

Bit	Name	R/W	Description	Default
7	FaultStatus_EXT_7_Prot	RO	EXT 7 pin (Protection) Status 0x0: Limit high > V(EXT_7) > limit low 0x1 V(EXT_7) > limit high or < limit low	0x0
6	FaultStatus_EXT_6_Prot	RO	EXT 6 pin (Protection) Status 0x0: Limit high > V(EXT_6) > limit low 0x1 V(EXT_6) > limit high or < limit low	0x0
5	FaultStatus_EXT_5_Prot	RO	EXT 5 pin (Protection) Status 0x0: Limit high > V(EXT_5) > limit low 0x1 V(EXT_5) > limit high or < limit low	0x0
4	FaultStatus_EXT_4_Prot	RO	EXT 4 pin (Protection) Status 0x0: Limit high > V(EXT_4) > limit low 0x1 V(EXT_4) > limit high or < limit low	0x0
3	FaultStatus_EXT_3_Prot	RO	EXT 3 pin (Protection) Status 0x0: Limit high > V(EXT_3) > limit low 0x1 V(EXT_3) > limit high or < limit low	0x0
2	FaultStatus_EXT_2_Prot	RO	EXT 2 pin (Protection) Status 0x0: Limit high > V(EXT_2) > limit low 0x1 V(EXT_2) > limit high or < limit low	0x0
1	FaultStatus_EXT_1_Prot	RO	EXT 1 pin (Protection) Status 0x0: Limit high > V(EXT_1) > limit low 0x1 V(EXT_1) > limit high or < limit low	0x0
0	FaultStatus_EXT_0_Prot	RO	EXT 0 pin (Protection) Status 0x0: Limit high > V(EXT_0) > limit low 0x1 V(EXT_0) > limit high or < limit low	0x0

9.2.37 0x40 - OTP_VERSION

Bit	Name	R/W	Description	Default
7:0	OTP_VERSION	RO	Protection OTP version	0x01

9.2.38 0x41 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RO		0x00

9.2.39 0x42 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RO		0x00

9.2.40 0x43 - OTP_CALCCRCMSB

Bit	Name	R/W	Description	Default
7:0	OTP_CALCCRCMSB	RO	Upper byte of calculated CRC	0x00

9.2.41 0x44 - OTP_CALCCRCLSB

Bit	Name	R/W	Description	Default
7:0	OTP_CALCCRCLSB	RO	Lower byte of calculated CRC	0x00

9.2.42 0x45 - OTP_WRITEDATA

Bit	Name	R/W	Description	Default
7:0	OTP_WRITEDATA	RW	Data byte to be written (programmed) to OTP	0x00

9.2.43 0x46 - OTP_RWADDR

Bit	Name	R/W	Description	Default
7	OTP_CRC_FAULT	RO	OTP download CRC fail 0x1: CRC fail on OTP download 0x0: CRC pass on OTP download	0x0
6	Reserved	RO		0x0
5:4	Reserved	RW		0x0
3:0	Reserved	RW		0x0

9.2.44 0x47 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.2.45 0x48 - OTP_FLT_RECORD

Bit	Name	R/W	Description	Default
7	OTP_FLT_DLOAD_Timeout	RO	OTP Read Duration Fault 0x0: No OTP Read Duration Fault 0x1: OTP Read Duration ≥ 256*Low Freq Clock Periods (~8ms)	0x0
6	OTP_FLT_INIT_Fail	RO	OTP INIT failure 0x0: Read Initialization passed 0x1: Read Initialization failed	0x0
5	OTP_FLT_CRC_FailPage0	RO	OTP CRC failure 0x0: No OTP Failure 0x1: OTP CRC Failure	0x0
4	OTP_FLT_CRC_FailPage2	RO	OTP CRC failure 0x0: No OTP Failure 0x1: OTP CRC Failure	0x0
3	OTP_FLT_PGM_NotPGMD	RO	Read of OTP to see if OTP has been programmed 0x0: No fault 0x1: Fault	0x0
2	OTP_FLT_PGM_Warn	RO	OTP Program Warning that one of the four bits in different/redundant programming mode failed 0x0: All four bits programmed correctly 0x1: One out of four bits programmed incorrectly but overall bit is correct	0x0
1	OTP_FLT_PGM_WrongAddr	RO	OTP PROG ADDR failure 0x0: Programming address is in the correct range 0x1: Programming address is out of acceptable range	0x0
0	OTP_FLT_PGM_Error	RO	OTP PROG failure 0x0: Programming passed 0x1: Programming failed	0x0

9.2.46 0x49 - OTP_CRCMSB

Bit	Name	R/W	Description	Default
7:0	OTP_CRCMSB	RW	Upper byte of 16-bit OTP_CRC value	0x00

9.2.47 0x4A - OTP_CRCLSB

Bit	Name	R/W	Description	Default
7:0	OTP_CRCLSB	RW	Lower byte of 16-bit OTP_CRC value	0x00

9.2.48 0x60 - ADCMON_COPY_SAMPLE

Bit	Name	R/W	Description	Default
7	ADCMON_COPY_SAMPLE_RDY	RO	ADC_DATA_READY goes low when ADC_DATACOPY is written and then goes high when the data is copied over to ADC_DATA_[MSB,LSB] 0x1: Copied Sample Ready 0x0: Copied Sample Not Ready	0x0
6:0	ADCMON_COPY_SAMPLE	RW	Selection of which value to copy to the ADCMON_COPY_DATA registers. When this value is written a sample is copied to ADCMON_COPY_DATA 0x00: ADCMON_Offset (Offset) 0x01: ADCMON_Temp (Die temperature) 0x02: ADCMON_Temp_Delta (Copy of die temperature) 0x03: ADCMON_BGRegu (Regulation bandgap) 0x04: ADCMON_PGNDRegu (Regulation PGND) 0x05: IntLDORegu_0_ADCMON_IntLDORegu (Internal Regulation LDO #1) 0x06: IntLDORegu_1_ADCMON_IntLDORegu (Internal Regulation LDO #2) 0x07: IntLDORegu_2_ADCMON_IntLDORegu (Internal Regulation LDO #3) 0x08: IntLDORegu_3_ADCMON_IntLDORegu (Internal Regulation LDO #4) 0x09: IntLDORegu_4_ADCMON_IntLDORegu (Internal Regulation LDO #5) 0x0A: IntLDORegu_5_ADCMON_IntLDORegu (Internal Regulation LDO #6) 0x0B: IntLDOProt_0_ADCMON_IntLDOProt (Internal Protection LDO #1) 0x0C: IntLDOProt_1_ADCMON_IntLDOProt (Internal Protection LDO #2) 0x10: ADCMON_AVIN1 0x0E: ADCMON_AVIN2 0x11: extLDO_0_ADCMON_ExtLDO (LDO1 voltage) 0x12: extLDO_1_ADCMON_ExtLDO (LDO2 voltage) 0x15: PVIN_0_ADCMON_PVIN (PVIN1 voltage) 0x17: PVIN_1_ADCMON_PVIN (PVIN2 voltage) 0x19: PVIN_2_ADCMON_PVIN (PVIN3 voltage) 0x1B: PVIN_3_ADCMON_PVIN (PVIN4 voltage) 0x1D: PVIN_4_ADCMON_PVIN (PVIN5 voltage) 0x16: VOUT_0_ADCMON_VOUT (VOUT1 voltage) 0x18: VOUT_1_ADCMON_VOUT (VOUT2 voltage) 0x1A: VOUT_2_ADCMON_VOUT (VOUT3 voltage) 0x1C: VOUT_3_ADCMON_VOUT (VOUT4 voltage) 0x1E: VOUT_4_ADCMON_VOUT (VOUT5 voltage) 0x0D: ADCMON_SPARE_0 (VIO voltage) 0x40: EXT_0_ADCMON_EXT 0x41: EXT_1_ADCMON_EXT 0x42: EXT_2_ADCMON_EXT 0x43: EXT_3_ADCMON_EXT 0x44: EXT_4_ADCMON_EXT 0x45: EXT_5_ADCMON_EXT 0x46: EXT_6_ADCMON_EXT 0x47: EXT_7_ADCMON_EXT 0x48: EXT_8_ADCMON_EXT 0x49: EXT_9_ADCMON_EXT 0x4A: EXT_10_ADCMON_EXT 0x4B: EXT_11_ADCMON_EXT 0x4C: EXT_12_ADCMON_EXT 0x4D: EXT_13_ADCMON_EXT 0x4E: EXT_14_ADCMON_EXT 0x4F: EXT_15_ADCMON_EXT	0x00

9.2.49 0x61 - ADCMON_COPY_DATA_MSB

Bit	Name	R/W	Description	Default
7:0	ADCMON_COPY_DATA_MSB	RO	Upper Byte of 16-bit ADC result for copied ADC data. See available channels in register 0x60 - ADCMON_COPY_SAMPLE.	0x00

9.2.50 0x62 - ADCMON_COPY_DATA_LSB

Bit	Name	R/W	Description	Default
7:0	ADCMON_COPY_DATA_LSB	RO	Lower Byte of 16-bit ADC result for copied ADC data. See available channels in register 0x60 - ADCMON_COPY_SAMPLE.	0x00

9.2.51 0x65 - ADCMON_DATAMSB_Offset

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Offset	RO	Upper byte of 16-bit ADC result for GND (Protection) measurement	0x00

9.2.52 0x66 - ADCMON_DATALSB_Offset

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Offset	RO	Lower byte of 16-bit ADC result for GND (Protection) measurement	0x00

9.2.53 0x67 - ADCMON_DATAMSB_Temp2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Temp3	RO	Upper byte of 16-bit ADC result for reference temperature sensor TEMP2 (Protection) measurement	0x00

9.2.54 0x68 - ADCMON_DATALSB_Temp2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Temp3	RO	Lower byte of 16-bit ADC result for reference temperature sensor TEMP2 (Protection) measurement	0x00

9.2.55 0x69 - ADCMON_DATAMSB_Temp3

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_Temp2	RO	Upper byte of 16-bit ADC result for temperature sensor TEMP3 (Protection) measurement	0x00

9.2.56 0x6A - ADCMON_DATALSB_Temp3

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_Temp2	RO	Lower byte of 16-bit ADC result for temperature sensor TEMP3 (Protection) measurement	0x00

9.2.57 0x6B - ADCMON_DATAMSB_BGRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_BGRegu	RO	Upper byte of 16-bit ADC result for Bandgap (Regulation) measurement	0x00

9.2.58 0x6C - ADCMON_DATALSB_BGRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_BGRegu	RO	Lower byte of 16-bit ADC result for Bandgap (Regulation) measurement	0x00

9.2.59 0x6D - ADCMON_DATAMSB_PGNDRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PGNDRegu	RO	Upper byte of 16-bit ADC result for PGND 0 (Regulation) measurement	0x00

9.2.60 0x6E - ADCMON_DATALSB_PGNDRegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PGNDRegu	RO	Lower byte of 16-bit ADC result for PGND 0 (Regulation) measurement	0x00

9.2.61 0x6F - IntLDORegu_0_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.62 0x70 - IntLDORegu_0_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.63 0x71 - IntLDORegu_1_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.64 0x72 - IntLDORegu_1_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.65 0x73 - IntLDORegu_2_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.66 0x74 - IntLDORegu_2_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.67 0x75 - IntLDORegu_3_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.68 0x76 - IntLDORegu_3_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.69 0x77 - IntLDORegu_4_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.70 0x78 - IntLDORegu_4_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.71 0x79 - IntLDORegu_5_ADCMON_DATAMSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDORegu	RO	Upper byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.72 0x7A - IntLDORegu_5_ADCMON_DATALSB_IntLDORegu

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDORegu	RO	Lower byte of 16-bit ADC result for Internal LDO (Regulation) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.73 0x7B - IntLDOProt_0_ADCMON_DATAMSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDOProt	RO	Upper byte of 16-bit ADC result for Internal LDO (Protection) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.74 0x7C - IntLDOProt_0_ADCMON_DATALSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDOProt	RO	Lower byte of 16-bit ADC result for Internal LDO (Protection) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.75 0x7D - IntLDOProt_1_ADCMON_DATAMSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_IntLDOProt	RO	Upper byte of 16-bit ADC result for Internal LDO (Protection) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.76 0x7E - IntLDOProt_1_ADCMON_DATALSB_IntLDOProt

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_IntLDOProt	RO	Lower byte of 16-bit ADC result for Internal LDO (Protection) measurement. **Note:** The value in this register is scaled by a factor of 3/4.	0x00

9.2.77 0x7F - ADCMON_DATAMSB_AVIN1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_AVIN1	RO	Upper byte of 16-bit ADC result for AVIN1 power supply (Regulation) measurement.	0x00

9.2.78 0x80 - ADCMON_DATALSB_AVIN1

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_AVIN1	RO	Lower byte of 16-bit ADC result for AVIN1 power supply (Regulation) measurement.	0x00

9.2.79 0x81 - ADCMON_DATAMSB_AVIN2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_AVIN2	RO	Upper byte of 16-bit ADC result for AVIN2 power supply (Protection) measurement.	0x00

9.2.80 0x82 - ADCMON_DATALSB_AVIN2

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_AVIN2	RO	Lower byte of 16-bit ADC result for AVIN2 power supply (Protection) measurement.	0x00

9.2.81 0x83 - extLDO_0_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16-bit ADC result for LDO1 measurement.	0x00

9.2.82 0x84 - extLDO_0_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16-bit ADC result for LDO1 measurement.	0x00

9.2.83 0x85 - extLDO_1_ADCMON_DATAMSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_ExtLDO	RO	Upper byte of 16-bit ADC result for LDO2 measurement.	0x00

9.2.84 0x86 - extLDO_1_ADCMON_DATALSB_ExtLDO

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_ExtLDO	RO	Lower byte of 16-bit ADC result for LDO2 measurement.	0x00

9.2.85 0x87 - PVIN_0_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16-bit ADC result for PVIN1 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.86 0x88 - PVIN_0_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16-bit ADC result for PVIN1 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.87 0x89 - PVIN_1_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16-bit ADC result for PVIN2 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.88 0x8A - PVIN_1_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16-bit ADC result for PVIN2 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.89 0x8B - PVIN_2_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16-bit ADC result for PVIN3 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.90 0x8C - PVIN_2_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16-bit ADC result for PVIN3 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.91 0x8D - PVIN_3_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16-bit ADC result for PVIN4 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.92 0x8E - PVIN_3_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16-bit ADC result for PVIN4 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.93 0x8F - PVIN_4_ADCMON_DATAMSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_PVIN	RO	Upper byte of 16-bit ADC result for PVIN5 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.94 0x90 - PVIN_4_ADCMON_DATALSB_PVIN

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_PVIN	RO	Lower byte of 16-bit ADC result for PVIN5 measurement. **Note:** The value in this register is scaled by a factor of 1/2.	0x00

9.2.95 0x91 - VOUT_0_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16-bit ADC result for VOUT1 measurement	0x00

9.2.96 0x92 - VOUT_0_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16-bit ADC result for VOUT1 measurement	0x00

9.2.97 0x93 - VOUT_1_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16-bit ADC result for VOUT2 measurement	0x00

9.2.98 0x94 - VOUT_1_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16-bit ADC result for VOUT2 measurement	0x00

9.2.99 0x95 - VOUT_2_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16-bit ADC result for VOUT3 measurement	0x00

9.2.100 0x96 - VOUT_2_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16-bit ADC result for VOUT3 measurement	0x00

9.2.101 0x97 - VOUT_3_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16-bit ADC result for VOUT4 measurement	0x00

9.2.102 0x98 - VOUT_3_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16-bit ADC result for VOUT4 measurement	0x00

9.2.103 0x99 - VOUT_4_ADCMON_DATAMSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_VOUT	RO	Upper byte of 16-bit ADC result for VOUT5 measurement	0x00

9.2.104 0x9A - VOUT_4_ADCMON_DATALSB_VOUT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_VOUT	RO	Lower byte of 16-bit ADC result for VOUT5 measurement	0x00

9.2.105 0x9B - ADCMON_DATAMSB_SPARE_0

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_SPARE_0	RO	Upper byte of 16-bit ADC result for VIO monitoring ADC channel	0x00

9.2.106 0x9C - ADCMON_DATALSB_SPARE_0

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_SPARE_0	RO	Lower byte of 16-bit ADC result for VIO monitoring ADC channel	0x00

9.2.107 0x9D - EXT_0_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for ADC1 (no external MUX) or external channel 0 (with external MUX)	0x00

9.2.108 0x9E - EXT_0_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for ADC1 (no external MUX) or external channel 0 (with external MUX)	0x00

9.2.109 0x9F - EXT_1_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for ADC2 (no external MUX) or external channel 1 (with external MUX)	0x00

9.2.110 0xA0 - EXT_1_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for ADC2 (no external MUX) or external channel 1 (with external MUX)	0x00

9.2.111 0xA1 - EXT_2_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for ADC3 (no external MUX) or external channel 2 (with external MUX)	0x00

9.2.112 0xA2 - EXT_2_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for ADC3 (no external MUX) or external channel 2 (with external MUX)	0x00

9.2.113 0xA3 - EXT_3_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for ADC4 (no external MUX) or external channel 3 (with external MUX)	0x00

9.2.114 0xA4 - EXT_3_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for ADC4 (no external MUX) or external channel 3 (with external MUX)	0x00

9.2.115 0xA5 - EXT_4_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for ADC5 (no external MUX) or external channel 4 (with external MUX)	0x00

9.2.116 0xA6 - EXT_4_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for ADC5 (no external MUX) or external channel 4 (with external MUX)	0x00

9.2.117 0xA7 - EXT_5_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 5 (with external MUX)	0x00

9.2.118 0xA8 - EXT_5_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 5 (with external MUX)	0x00

9.2.119 0xA9 - EXT_6_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 6 (with external MUX)	0x00

9.2.120 0xAA - EXT_6_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 6 (with external MUX)	0x00

9.2.121 0xAB - EXT_7_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 7 (with external MUX)	0x00

9.2.122 0xAC - EXT_7_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 7 (with external MUX)	0x00

9.2.123 0xAD - EXT_8_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 8 (with external MUX)	0x00

9.2.124 0xAE - EXT_8_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 8 (with external MUX)	0x00

9.2.125 0xAF - EXT_9_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 9 (with external MUX)	0x00

9.2.126 0xB0 - EXT_9_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 9 (with external MUX)	0x00

9.2.127 0xB1 - EXT_10_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 10 (with external MUX)	0x00

9.2.128 0xB2 - EXT_10_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 10 (with external MUX)	0x00

9.2.129 0xB3 - EXT_11_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 11 (with external MUX)	0x00

9.2.130 0xB4 - EXT_11_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 11 (with external MUX)	0x00

9.2.131 0xB5 - EXT_12_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 12 (with external MUX)	0x00

9.2.132 0xB6 - EXT_12_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 12 (with external MUX)	0x00

9.2.133 0xB7 - EXT_13_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 13 (with external MUX)	0x00

9.2.134 0xB8 - EXT_13_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 13 (with external MUX)	0x00

9.2.135 0xB9 - EXT_14_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 14 (with external MUX)	0x00

9.2.136 0xBA - EXT_14_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 14 (with external MUX)	0x00

9.2.137 0xBB - EXT_15_ADCMON_DATAMSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATAMSB_EXT	RO	Upper byte of 16-bit ADC result for external channel 15 (with external MUX)	0x00

9.2.138 0xBC - EXT_15_ADCMON_DATALSB_EXT

Bit	Name	R/W	Description	Default
7:0	ADCMON_DATALSB_EXT	RO	Lower byte of 16-bit ADC result for external channel 15 (with external MUX)	0x00

9.2.139 0xC0 - MTE_CFG_CTRL_A

Bit	Name	R/W	Description	Default
7:1	Reserved	RO		0x00
0	MTE_BURN	RW	0x1: Writing a 1 to this register makes bypass self-diagnosis state. 0x0: Writing a 1 to this register burns the MTE fuses.	0x0

9.2.140 0xC8 - WDT_KICK_REG

Bit	Name	R/W	Description	Default
7:0	WDT_KICK_REG	RW	Kick data register for WatchDog Timer	0x00

9.2.141 0xC9 - WDT_LFSR

Bit	Name	R/W	Description	Default
7:0	WDT_LFSR	RO	Question output for Q&A Watchdog functions	0x00

9.2.142 0xD0 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.2.143 0xD1 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.2.144 0xD2 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.2.145 0xD3 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

9.2.146 0xE0 - RESERVED

Bit	Name	R/W	Description	Default
7:0	Reserved	RW		0x00

10. Layout Guidelines

The RAA271000 is a highly programmable, multiple-channel power management integrated circuit (PMIC) designed for Renesas R-Car SoC to meet the high-performance requirements in addition to providing a high level of integration to minimize system board area and BOM cost. It includes 5 Buck switching regulators and 2 LDOs, a 12-bit ADC and 14 GPIOs, in a 0.8mm pitch 60 ball FCCSP package. **Note:** Proper PCB layout is an important design practice to ensure a satisfactory electrical and thermal performance.

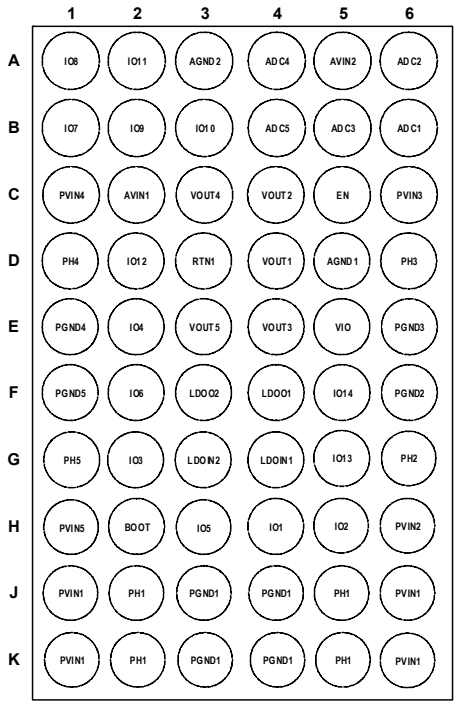


Figure 22. RAA271000 Pinout (Top View)

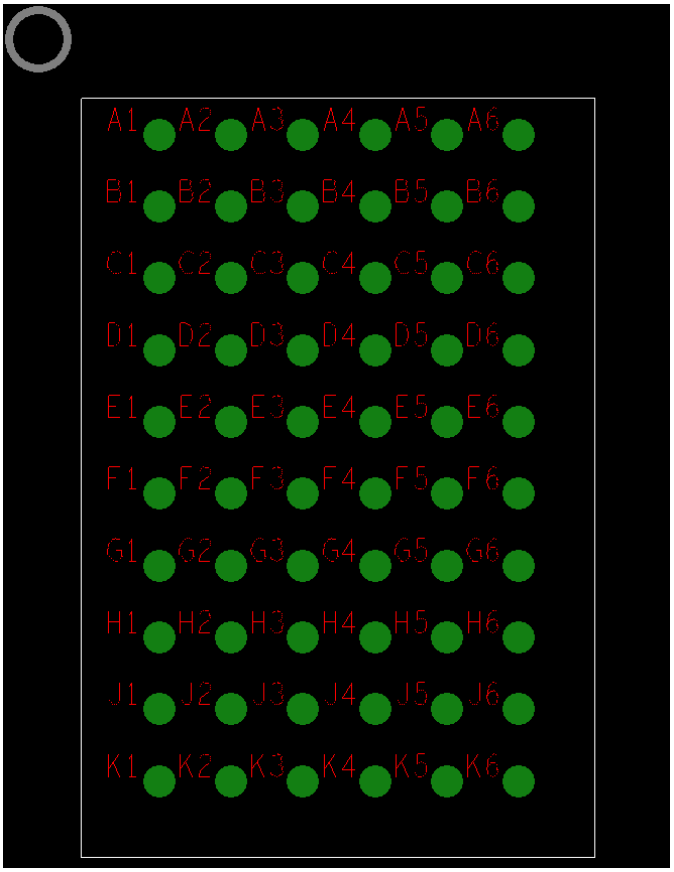


Figure 23. RAA271000 PCB Footprint (Top View)

Note: Row A is closer to the PMIC package boundary; Row K is further to the PMIC package boundary.

Each Buck regulator power delivery loop consists of the output inductor L, the output capacitor C_{OUT}, the PH switching node pin, and the PGND pin.

Important: Make the power delivery or current flow loop as small as possible. The PCB connecting traces among those components and pins should be direct, short, and wide. Apply the same practice to the connections of the PVIN pin, the input capacitor C_{IN}, and PGND.

The input voltage (V_{IN}) and the output voltage (V_{OUT}) PCB copper should be wide enough to minimize the current conduction loss.

Multiple solid ground layer is helpful to reduce the current flow resistance, have better thermal dissipation and for a good EMI performance. Use enough vias to connect all the GND layers.

10.1 Buck-1 Components Placement and PCB Routing

In Figure 24 through Figure 26, the signal/copper net name is labeled in red text and the component is labeled in yellow text. The RAA271000 is placed on the PCB top component layer.

1. Place the input capacitors C_{IN1} as close as possible to Buck-1 PVIN and PGND pins.
2. Connect all the Buck-1 PGND pins together through a GND copper plane and use multiple vias connecting to the inner and other GND layers.
3. Connect the Buck-1 PH1 pins together through a PH1 copper plane on the PMIC component layer.
4. Place the inductor L1 as close as possible to the PMIC.
5. Place the output bulk capacitor C_{OUT1} close to the inductor L1 output terminal.
   a. Minimize the GND distance of the input capacitor C_{IN1} and the output capacitor C_{OUT1}. If C_{IN1} GND plane and C_{IN2} GND plane cannot be connected directly with copper, use enough vias connecting them to the inner or other GND plane respectively, such as the two GND planes can be connected through the other GND layers with minimized resistance.
   b. Solid ground plane is helpful for a good EMI performance, current conduction, and thermal dissipation.
6. If possible, use two or multiple layer or wide enough PCB copper trace for the output voltage V_{OUT1} to minimize the conduction loss, since Buck-1 output carries high current.

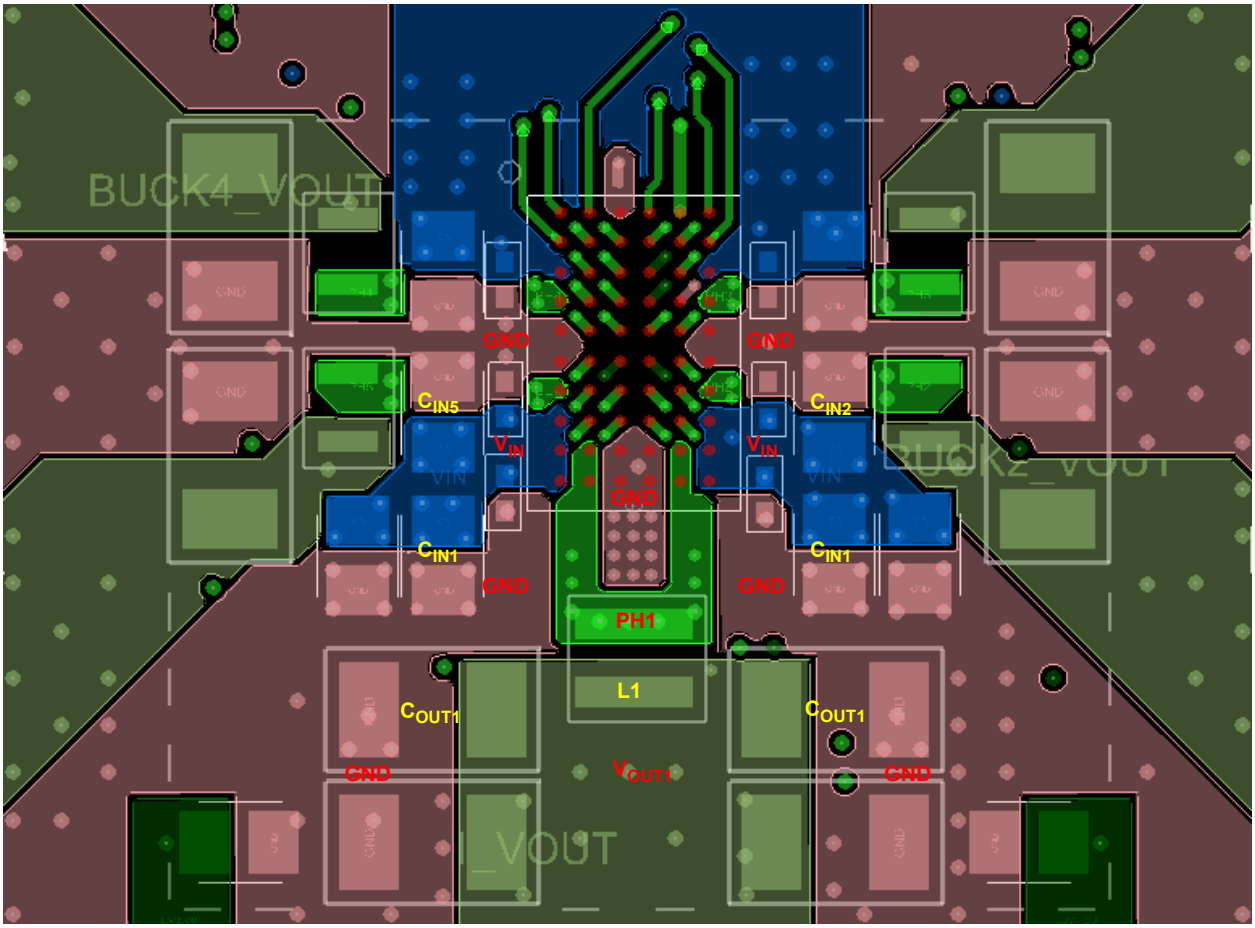


Figure 24. Top Layer

7. For the Buck-1 bootstrap cap C_{BOOT}, place it on the PCB bottom component layer.
   a. Use a via connecting BOOT pin to the bottom layer; use a via connecting PH1 net to the bottom layer.
   b. Minimize the loop and PCB trace of “Boot pin→Boot trace→Cboot→PH1 trace”.
   c. Use at least 10 mil width trace for the Boot trace and PH1 trace to conduct the Buck-1 high side FET driver current.
   d. Keep all other smaller signals away from BOOT and PH1 via/trace/copper.

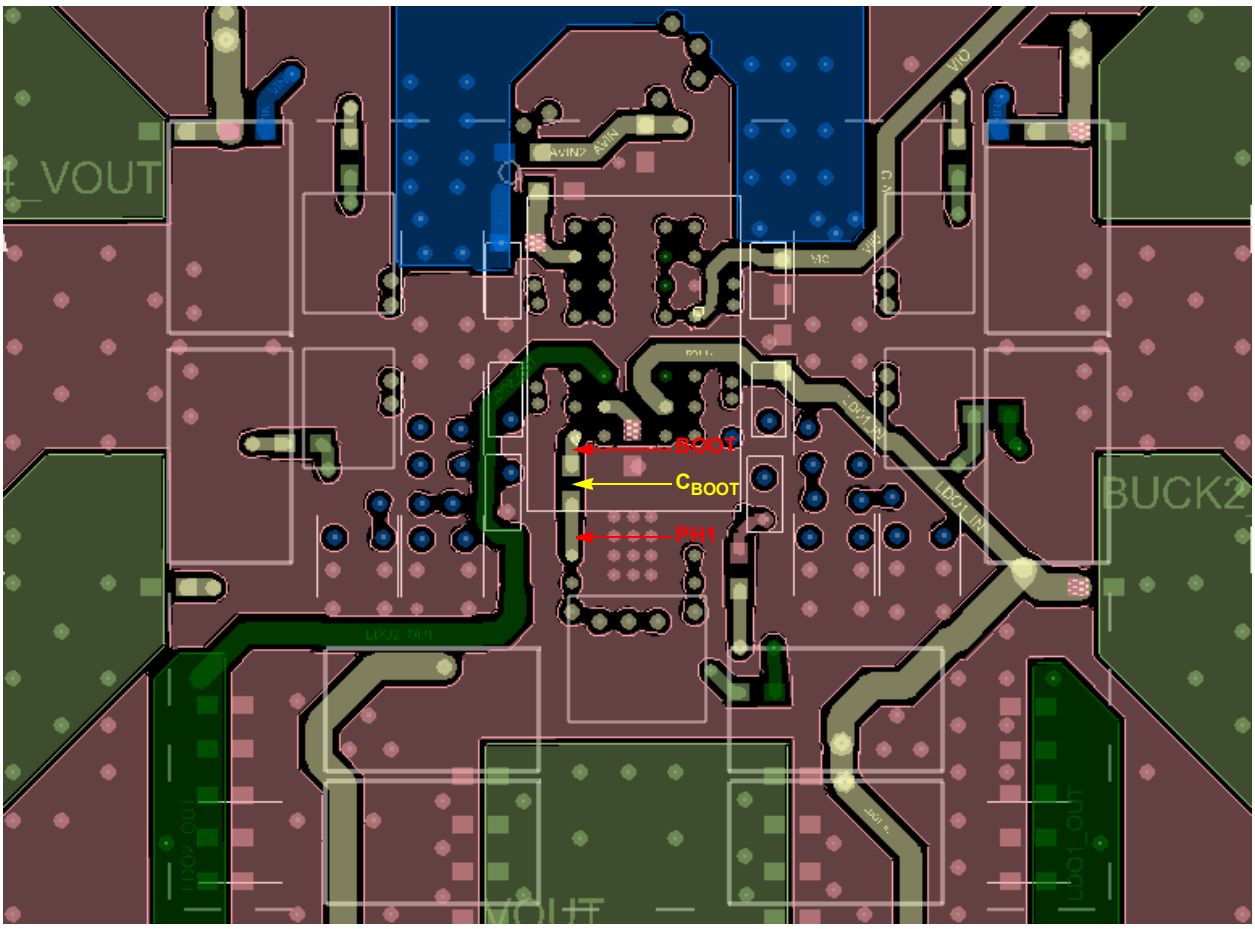


Figure 25. PCB Bottom Component Layer

8. Run the V_{OUT1} and RTN1 output voltage feedback differential trace in parallel, staying away from the PH1, PH, PH2, PH3, PH4, PH5, and BOOT, the noisy signal via/trace/copper, and away from any high-speed digital signals. Shield the V_{OUT1} and RTN1 differential parallel traces with GND copper.
9. Connect the V_{OUT1} and RTN1 differential sensing point to the V_{OUT1} output high frequency ceramic cap bank to minimize the feedback ripple and noise.

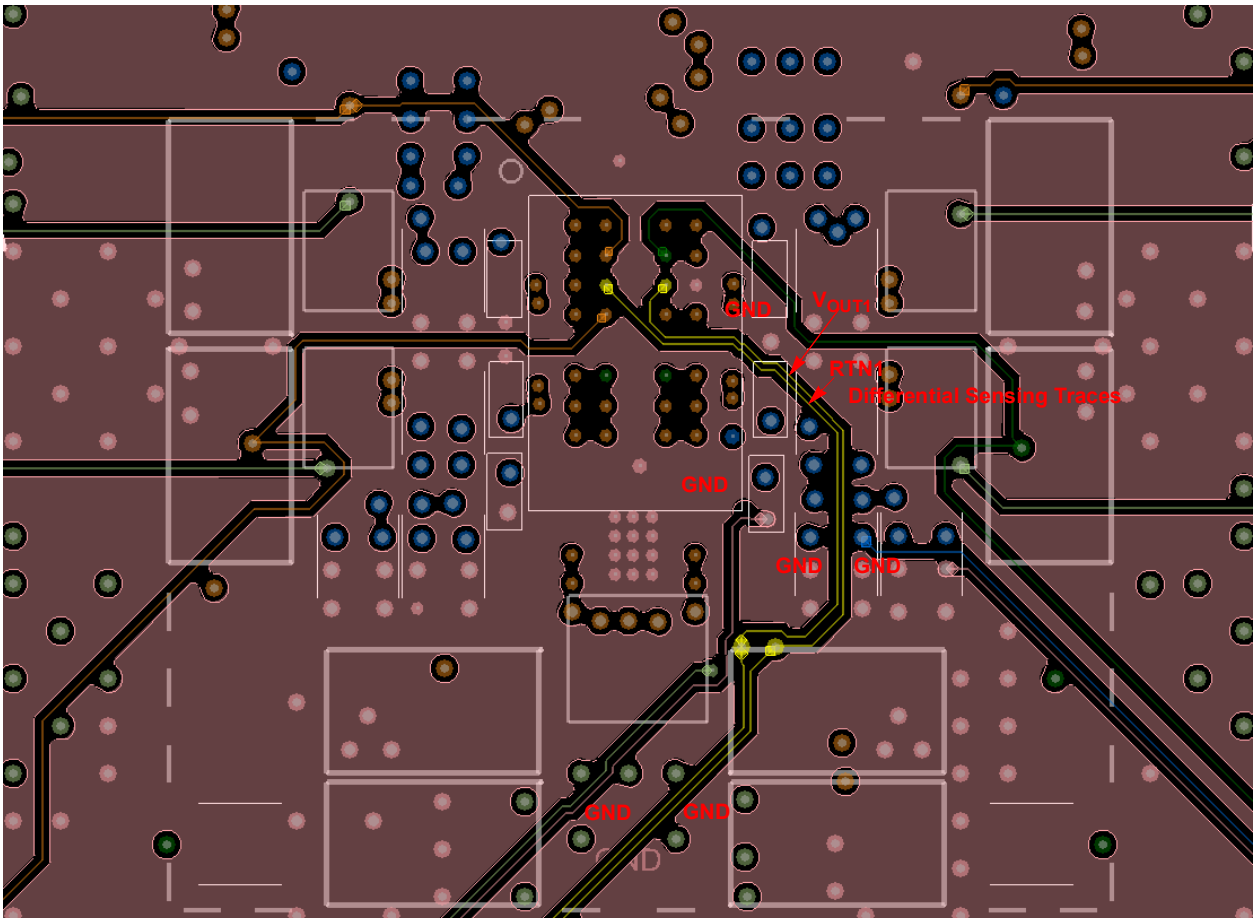


Figure 26. PCB V_{OUT} and RTN Routing

10.2 Buck-2, Buck-3, Buck-4, and Buck-5 Component Placement and PCB Routing

Take Buck-2 and Buck-3 as the example; the Buck-4 and Buck-5 follow the same layout practices. In Figure 27, the signal/copper net name is labeled in red text and the component is labeled in yellow text.

1. Place the input capacitor C_{IN2} as close as possible to Buck-2 PVIN and PGND pins and C_{IN3} to Buck-3 PVIN and PGND pins.
2. Connect the Buck-2 PH2 pins through a PH2 copper trace to the inductor L2 PH2 terminal and pad.
3. Connect the Buck-3 PH3 pins through a PH3 copper trace to the inductor L3 PH3 terminal and pad.
4. Place the inductor L2 and L3 as close as possible to the PMIC.
5. Place the output bulk capacitor C_{OUT2} close to the inductor L2 and C_{OUT3} close to the L3 output terminal.
6. Connect the C_{IN2} and C_{IN3} GND copper plane to the C_{OUT2} and C_{OUT3} GND copper plane through copper directly or connect them through the other GND layers with multiple vias. Minimize the resistance between the input capacitor GND plane and the output capacitor GND plane.
7. If possible, use two or multiple layer or wide enough PCB copper trace for the output of V_{OUT2} and V_{OUT3}.

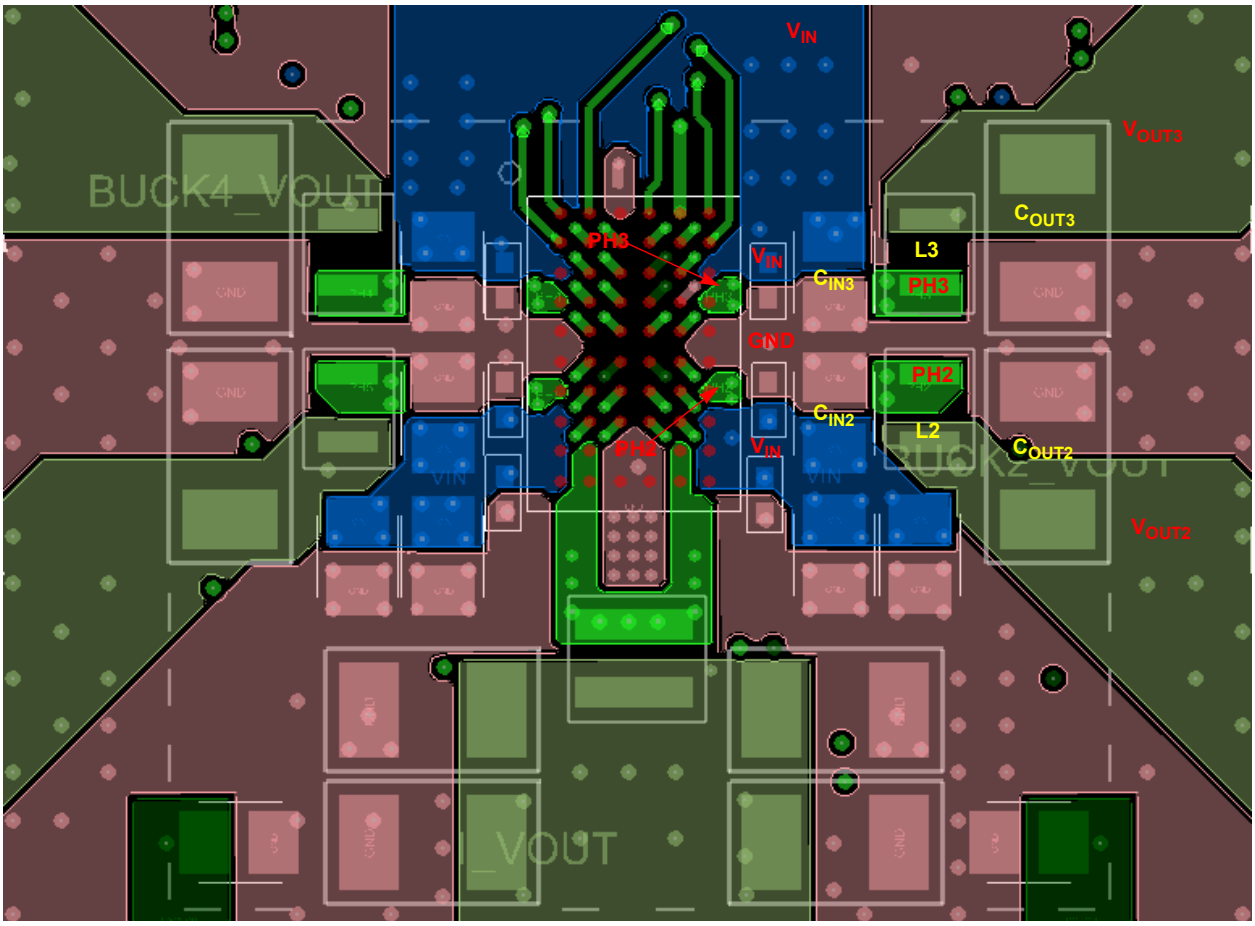


Figure 27. PCB Top Layer Buck Component Placement

8. Use inner layer or bottom layer to run the PH2 trace, connect to PH2 pin and L2 inductor pad through multiple vias.
   a. The PH2 trace should be wide because it carries the Buck-2 output current.
   b. Avoid any sensitive signal close to the PH2 trace and via.

9. Use inner layer or bottom layer to run the PH3 trace, connect to PH3 pin and L3 inductor pad through multiple vias.
   a. The PH3 trace should be wide because it carries the Buck-3 output current.
   b. Avoid any sensitive signal close to the PH3 trace and via.

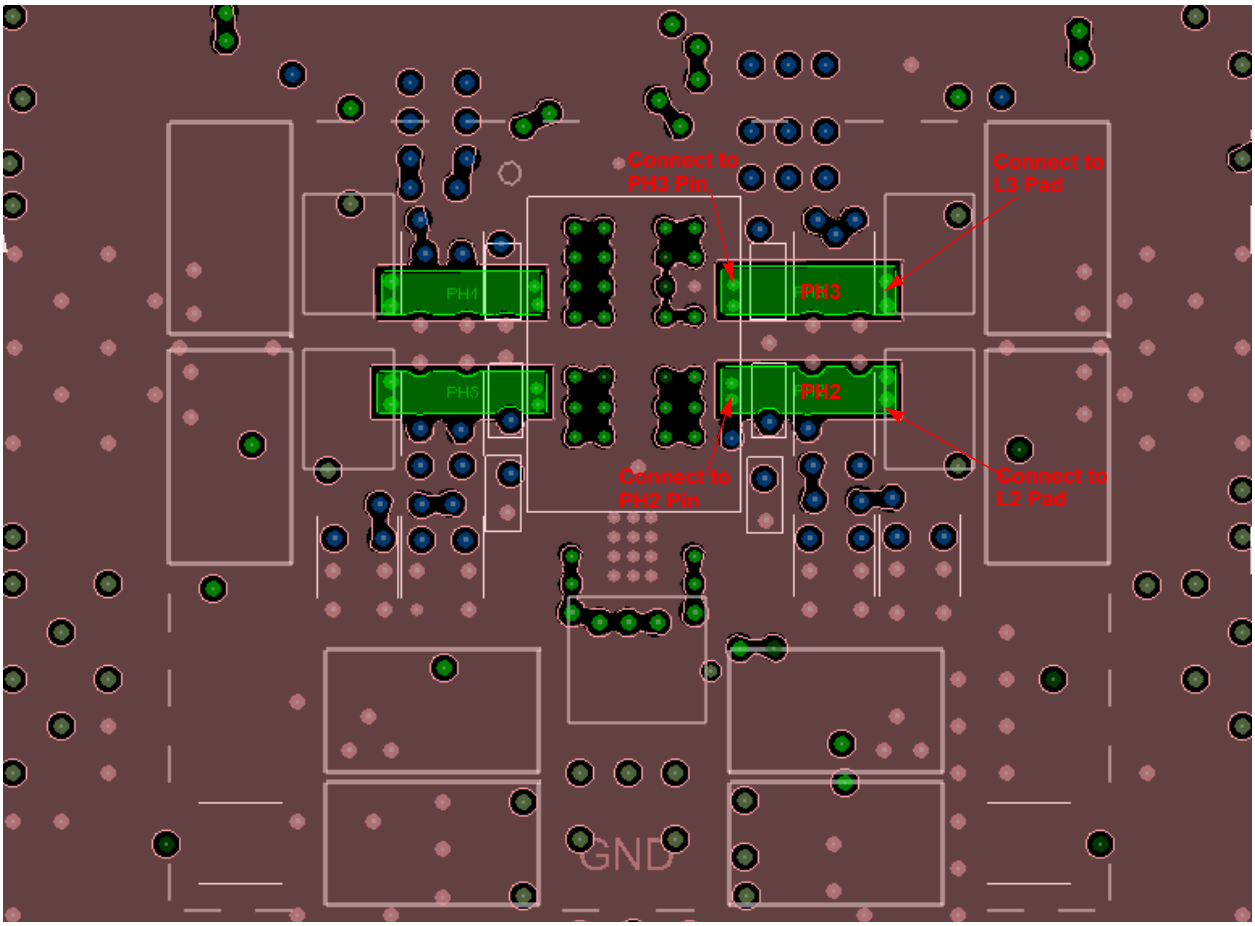


Figure 28. PCB Buck2-4 PH Trace Example

10. Run the V_{OUT2} and V_{OUT3} output voltage sensing trace, avoid any PH1/2/3/4/5 switching via/trace/copper, and shield the feedback sensing trace with GND copper.
11. Connect the V_{OUT2} feedback sensing point to Buck-2 and the V_{OUT3} to the Buck-3 output high frequency ceramic cap bank to minimize the feedback ripple and noise.

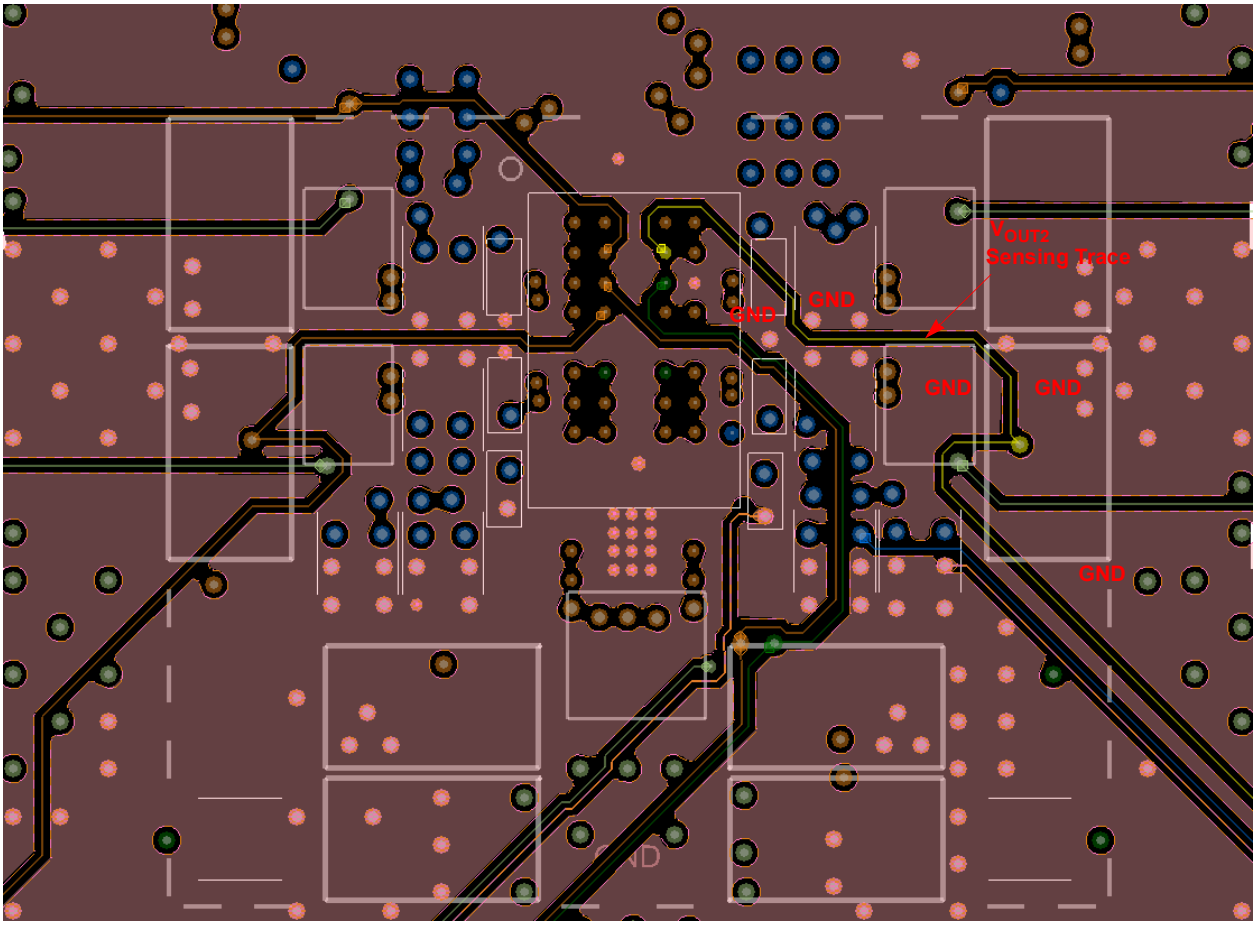


Figure 29. PCB V_{OUT2} Trace Example

10.3 All Other Components Placement and PCB Routing

1. Place the LDO1 and LDO2 input capacitors as close as possible to the LDOIN1 and LDOIN2 pins, respectively.
2. Place the LDO1 and LDO2 output capacitors as close as possible to the LDO1 and LDO2 output pins, respectively.
3. Place the AVIN1 pin and AVIN2 pin R-C filter capacitor as close as possible to the AVIN1 and AVIN2 pins, respectively. Always reference the decoupling capacitor GND pad to a quiet GND plane.
4. Run the ADCs and GPIOs digital traces away from the PH1/2/3/4/5 and BOOT the noisy signal via/trace/copper.

10.4 Other Recommendations

10.4.1 PCB Via Options

The RAA271000 PCB layout can use the plated through-holes via or the staggered micro-via to connect the pins to the inner layers and the bottom component layer.

10.4.2 8-Layer PCB Stackup Example

Table 25. PCB Layer Recommendation

Layer Level	Routed Connections
Top Layer	RAA271000, components, power (V_{IN}, V_{OUT}, GND)
Layer-2	GND
Layer-3	Power, PH2, PH3, PH4, PH5
Layer-4	GND
Layer-5	Signal, output voltage sensing traces
Layer-6	Signal
Layer-7	GND
Bottom Layer	Component, Signal, GND

10.4.3 Summary of the PCB Layout Practice

1. Place the input capacitors as close as possible to their respective PVIN and PGND pins.
2. Route the Buck switching phase nodes with short, wide traces, and avoid any sensitive signals.
3. Route output voltage sensing traces to the load point and the high frequency ceramic bank to minimize the feedback noise.
4. Run the output voltage sensing traces away from the switching phase via/trace/copper and high-speed digital signals, shield with GND copper.
5. Minimize the input capacitor GND and the output capacitor GND distance and resistance.
6. Use enough vias and PCB trace width for the current flow capacity.

10.5 RAA271000 PCB Layout Example 1 (Top view) - Through Hole via

Figure 30 shows the RAA271000 footprint, the components placement, the V_{IN}, V_{OUT}, and GND copper planes.

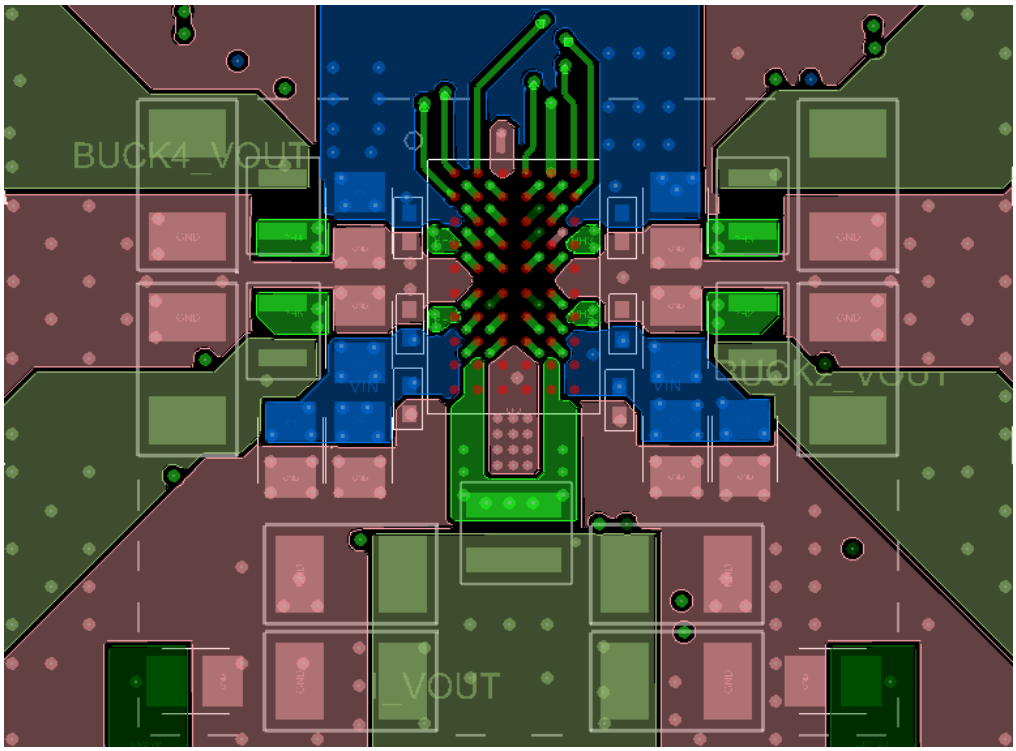


Figure 30. PCB Top Layer with All Components

Figure 31 is the inner Layer showing PH2, PH3, PH4, and PH5 traces.

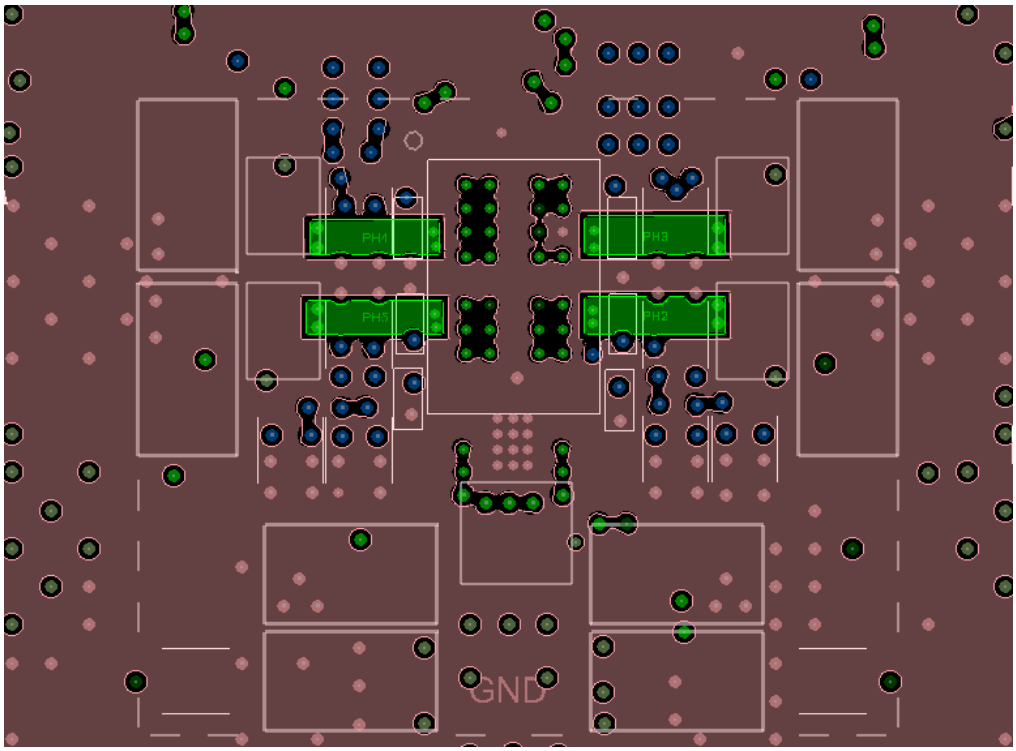


Figure 31. PCB Inner Layer Showing PH2-5 Traces

Figure 32 is the inner Layer showing V_{IN} copper and digital traces.

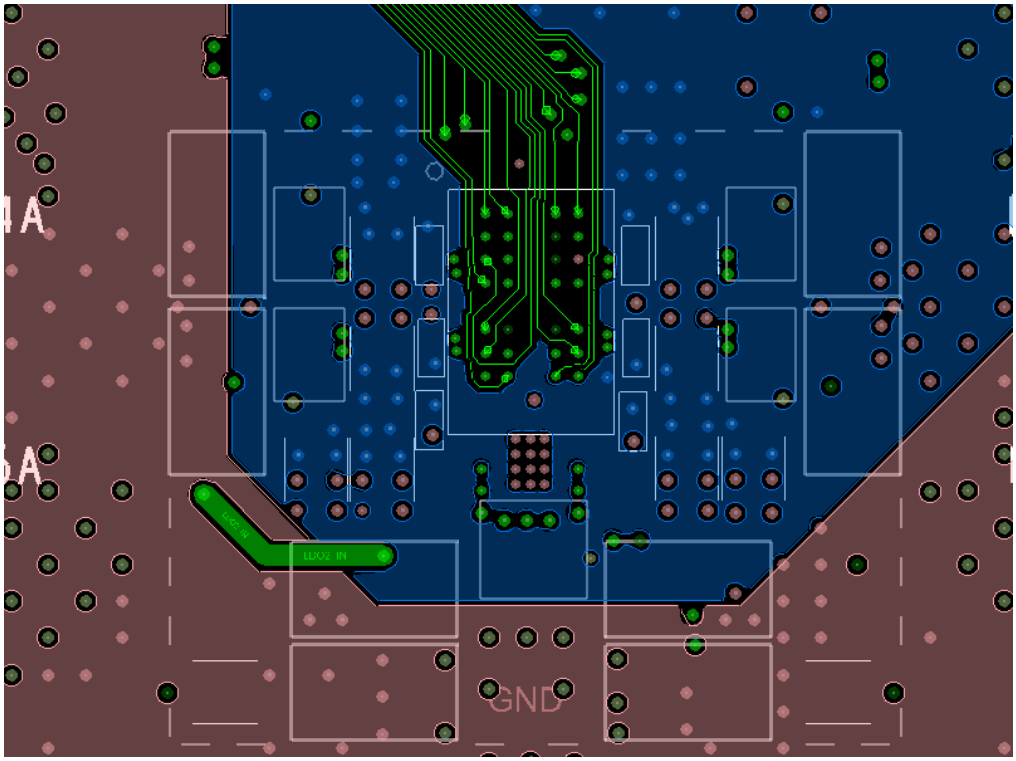


Figure 32. PCB Inner Copper and Digital Traces

Figure 33 shows Buck-1 bootstrap cap connection, V_{IN} copper.

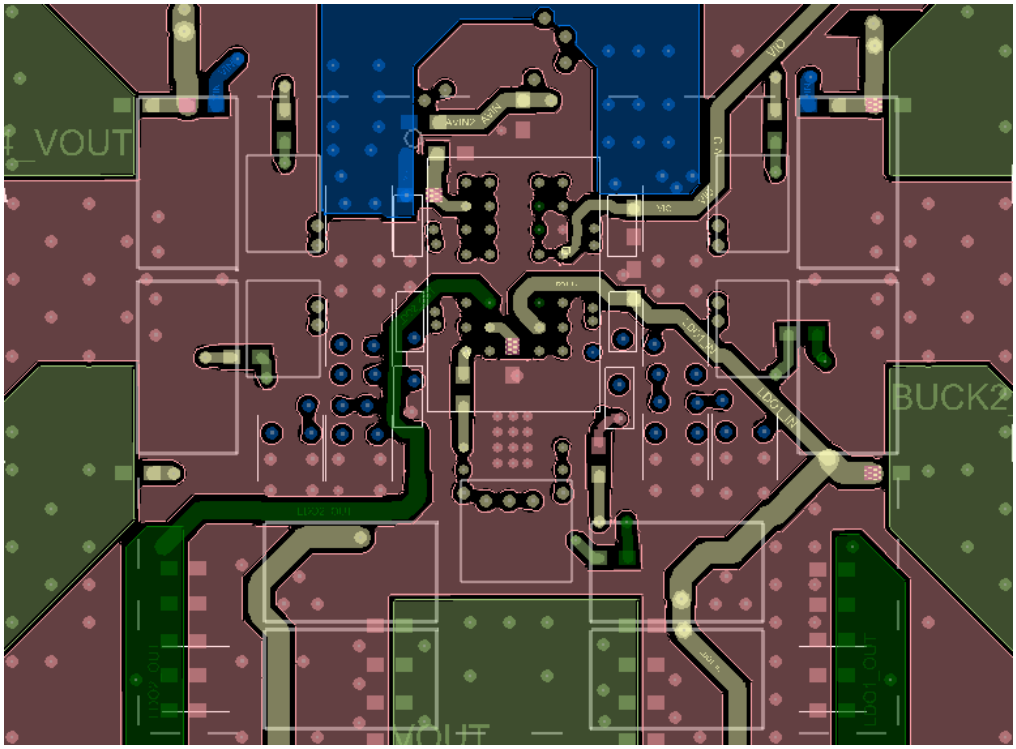


Figure 33. PCB Bottom Layer and Bootstrap Capacitor Connection

10.6 RAA271000 PCB Layout Example 2 (Top view) - Stagger Via

Figure 34 shows the RAA271000 footprint, the components placement, the V_{IN}, V_{OUT}, GND copper planes, and digital signals traces

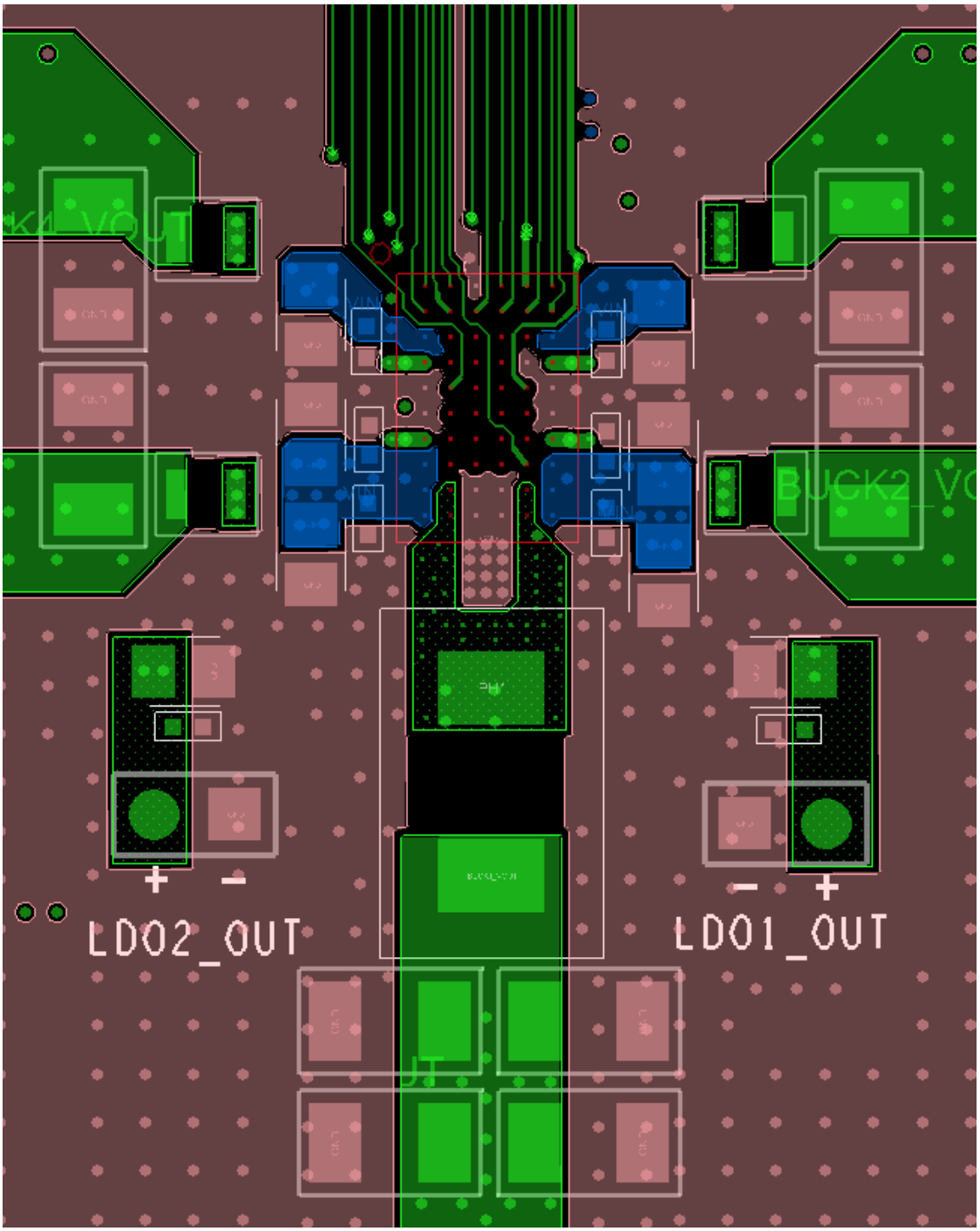


Figure 34. PCB Example 2, Top Layer with Staggered Vias

Figure 35 shows PH2, PH3, PH4, and PH5 traces, V_{IN} and GND copper.

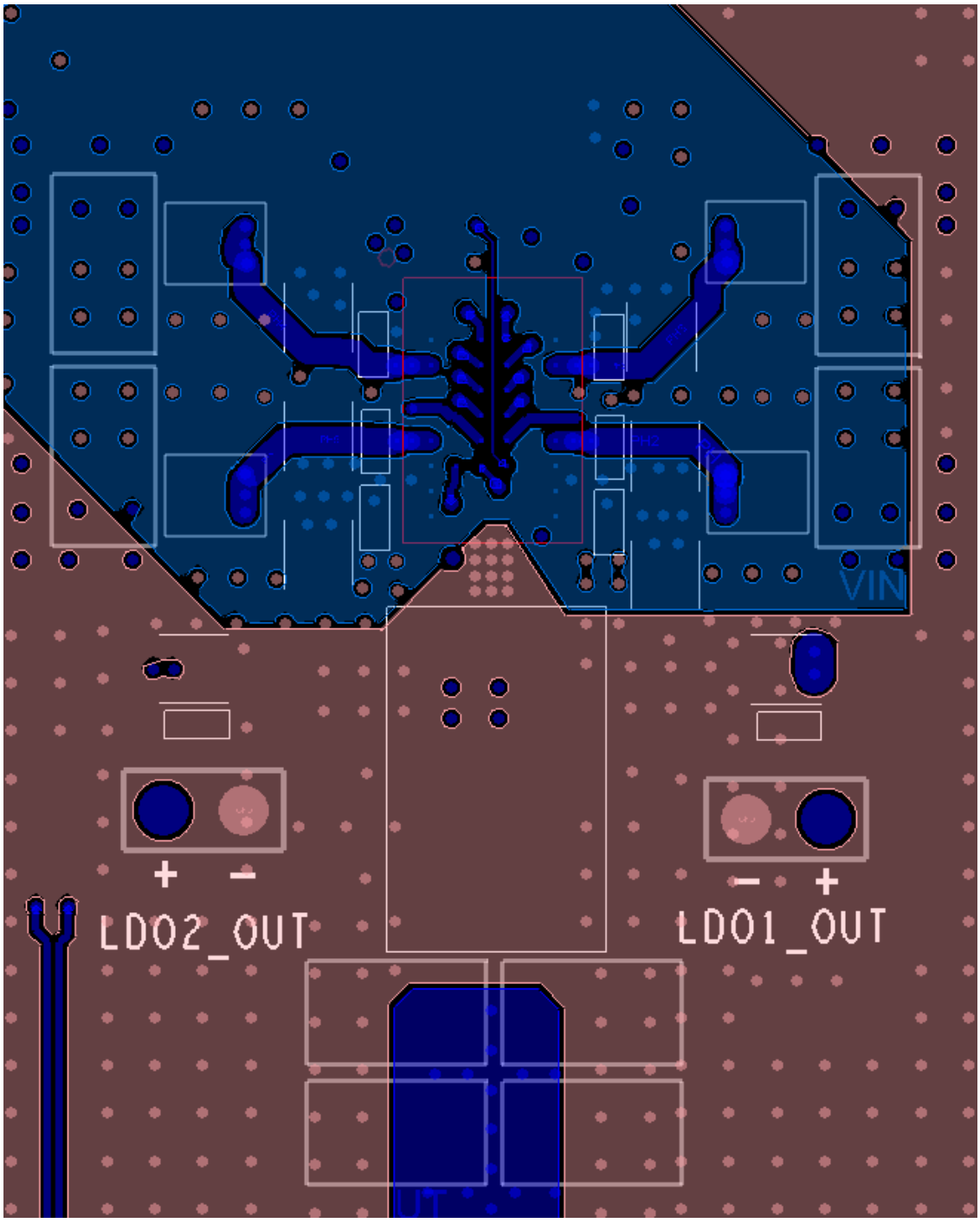


Figure 35. PCB Example 2, Inner Layer Showing PH2-5, VIN and GND Copper

Figure 36 shows V_{IN} and GND copper

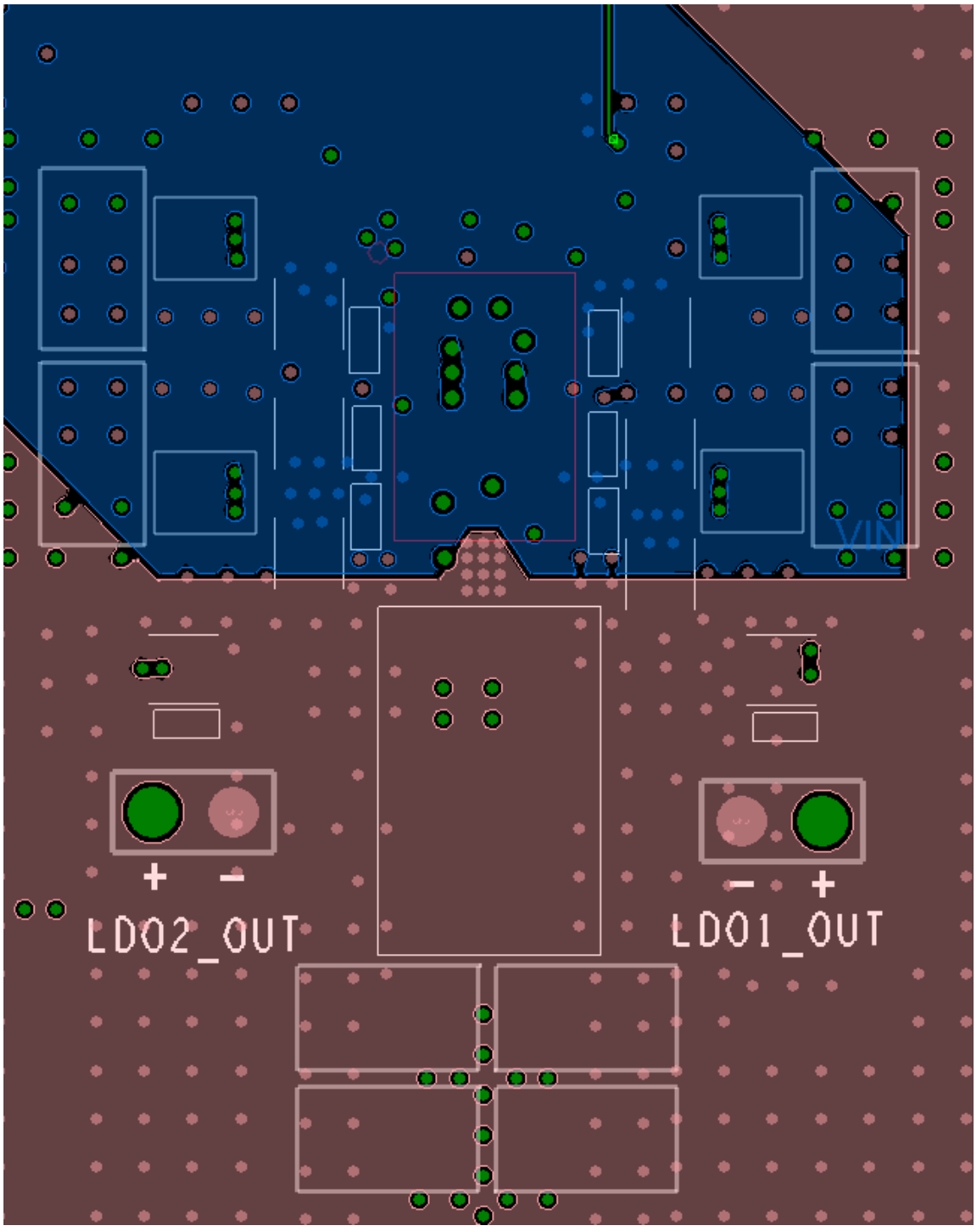


Figure 36. PCB Example 2, Inner Layer VIN and GND Copper

Figure 37 shows LDO1 and LDO2 traces and V_{OUT} sensing traces.

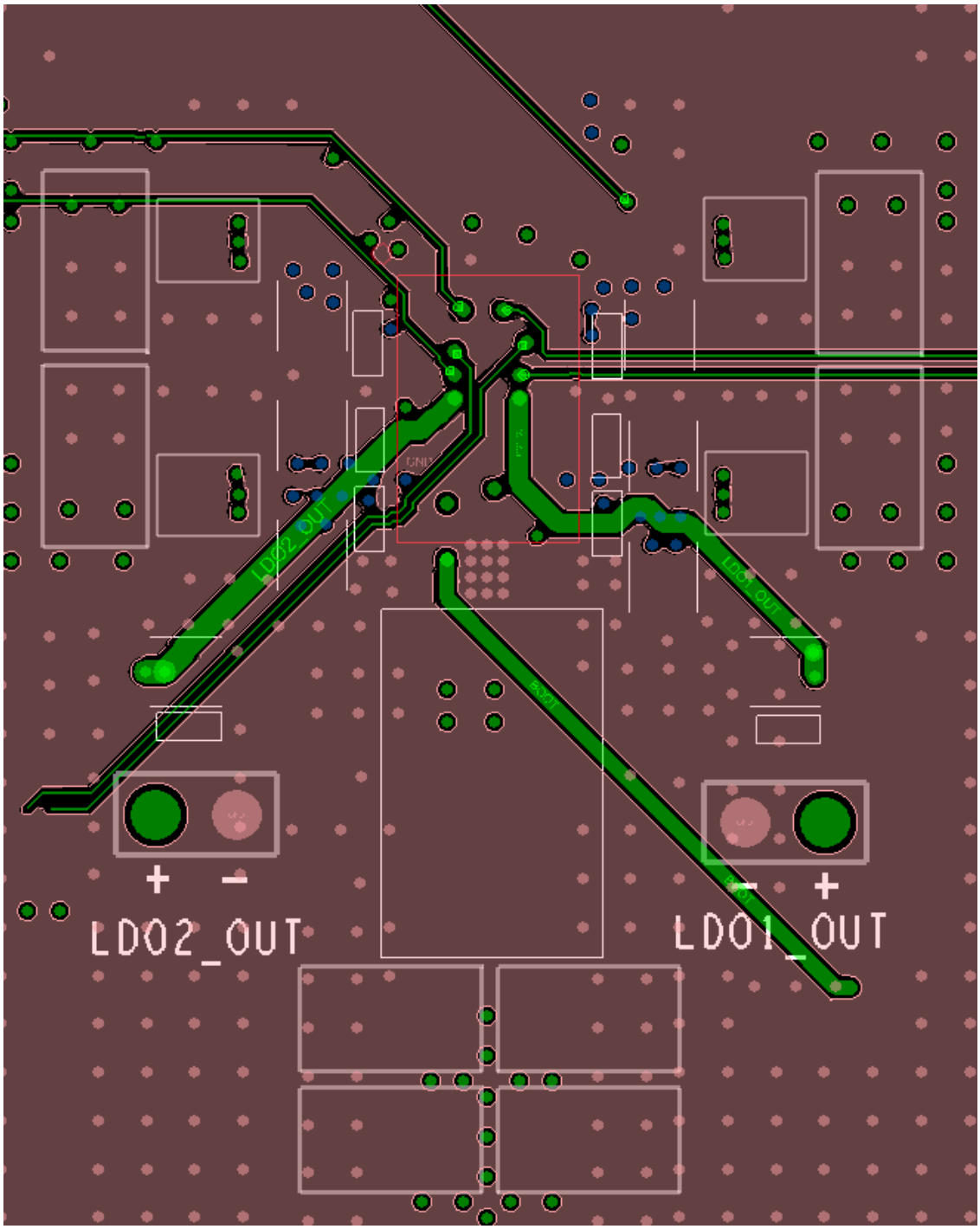


Figure 37. PCB Example 2, Inner Layer Showing LDO1-2 and V_{OUT} Sensing Traces

Figure 38 shows the Buck-1 bootstrap capacitor and two Buck-1 input capacitors placed on bottom.

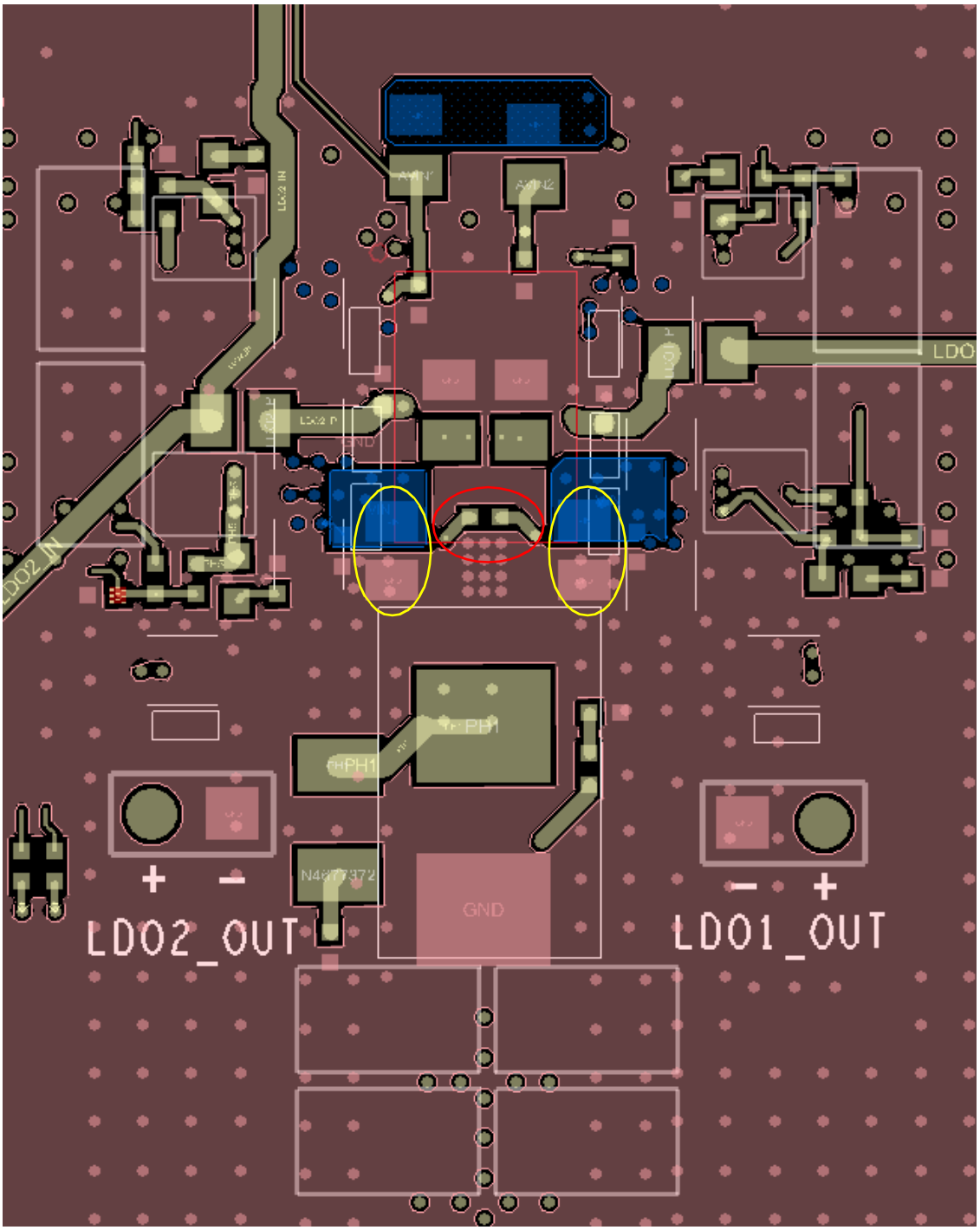


Figure 38. PCB Example 2, Bottom Layer Showing Bootstrap Capacitor and Buck1 Input Capacitors

11. Package Outline Drawing

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

12. Ordering Information

Part Number[1][2][3]	Part Marking	Package Description (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[3]	Temp Range
RAA271000A4HBG#AC0	RA271000 A4HBG	60 Ball FCCSP	V60.5.71x8.46	Tray	-40 to +125°C
RTKA271000E00000BU	Comprehensive Evaluation Board				
RTKA271000DE0000BU	Compact Reference Board				

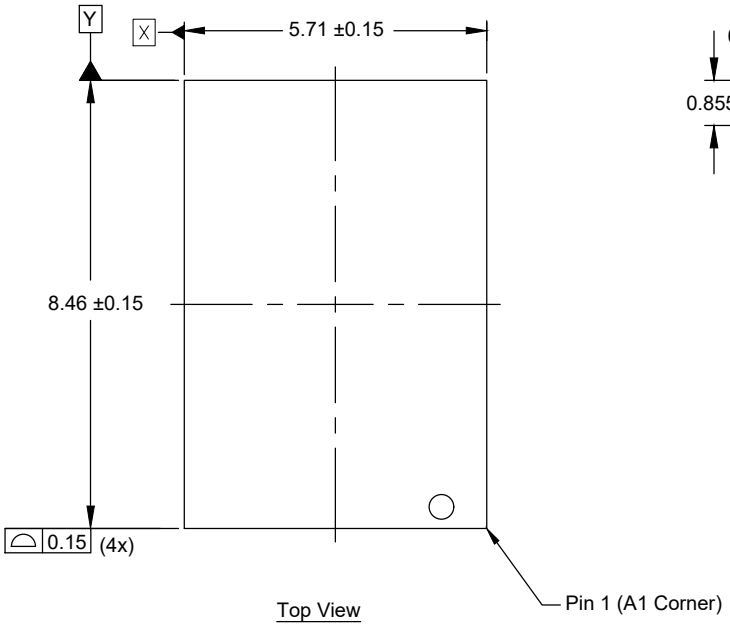
1. These Pb-free WLCSP packaged products employ special Pb-free material sets; molding compounds/die attach materials and SnAgCu - e6 solder ball terminals, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Pb-free WLCSP packaged products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA271000 product page. For more information about MSL, see TB363.
3. For additional part OTP options and carrier type, contact your local sales office.

13. Revision History

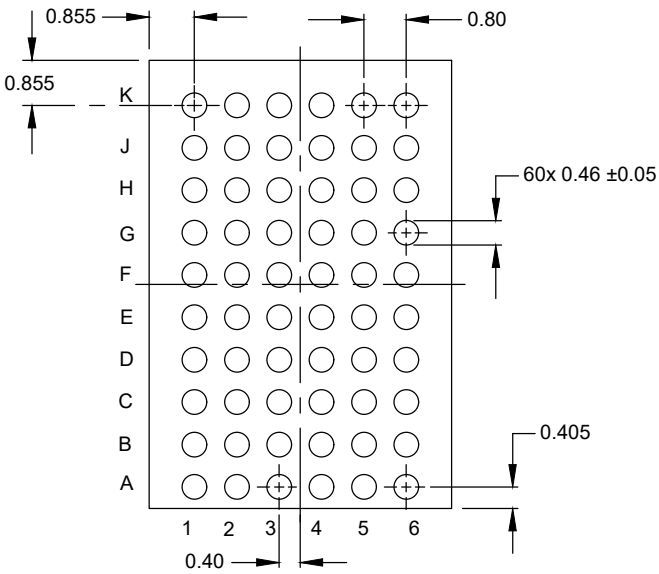
Rev.	Date	Description
2.01	Nov 26, 2024	Removed Feature: “Programmable current limits for all bucks”. 3.5, Electrical Specifications: updated Test Conditions, Min, and Max for the Protection parameters. 5.1, Power Sequencing, updated “0ms to 63ms in 1ms steps” to “0ms to 67ms in 1.07ms steps”. 6.1.1.1, Write Operation, updated first paragraph, Removed second paragraph. 6.1.1.2, Read Operation, updated text. Removed last paragraph. 6.1.2, SPI Configuration, updated IO_SPIMODE. 6.2.1.1, Write Operation, updated text. 6.2.1.2, Read Operation, updated text. 7.3.2, Table 18, updated Notes for Buck1 to Buck5. For the following Registers, updated the Default for Bit 3: ▪ 0x32 - FLT_MASK_BUCK1 ▪ 0x33 - FLT_MASK_BUCK2 ▪ 0x34 - FLT_MASK_BUCK3 ▪ 0x35 - FLT_MASK_BUCK4 ▪ 0x36 - FLT_MASK_BUCK5 For the following Registers, updated Bit 3 to Reserved: ▪ 0x42 - FLT_RECORD_BUCK1 ▪ 0x43 - FLT_RECORD_BUCK2 ▪ 0x44 - FLT_RECORD_BUCK3 ▪ 0x45 - FLT_RECORD_BUCK4 ▪ 0x46 - FLT_RECORD_BUCK5 In the Description for the following Registers, updated the Delay for Bit [5:0], from 1ms/LSB to 1.07ms/LSB: ▪ 0x76 - BUCK1_EN_DLY ▪ 0x77 - BUCK1_SHUTDN_DLY ▪ 0x86 - BUCK2_EN_DLY ▪ 0x87 - BUCK2_SHUTDN_DLY ▪ 0x96 - BUCK3_EN_DLY ▪ 0x97 - BUCK3_SHUTDN_DLY ▪ 0xA6 - BUCK4_EN_DLY ▪ 0xA7 - BUCK4_SHUTDN_DLY ▪ 0xB6 - BUCK5_EN_DLY ▪ 0xB7 - BUCK5_SHUTDN_DLY ▪ 0xC3 - LDO1_EN_DLY ▪ 0xC4 - LDO1_SHUTDN_DLY ▪ 0xC5 - LDO2_EN_DLY ▪ 0xC6 - LDO2_SHUTDN_DLY ▪ 0xC7 - HICCUP_RESTRT_DLY
1.01	May 23, 2022	Updated POD V60.5.71x8.46 to the latest version, changes are as follows: ▪ On Bottom View: Corrected typo, changed ball qty from 35x to 60x. ▪ Revised Title from Low Profile Ball Grid Array Package (LFBGA) to Flip Chip - Chip Scale Package (FCCSP). ▪ Updated Typical land pattern circles so they are easily distinguished from one another. No dimension changes were made to the POD. Updated Note 1 in the Ordering Information table.
1.00	Oct 4, 2021	Initial release

Package Outline Drawing

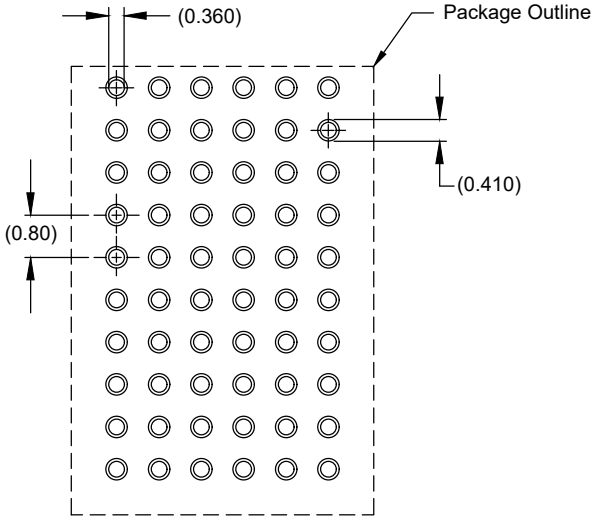
60 Flip Chip Chip Scale Package (FCCSP) Plastic Package
POD Number: V60.5.71x8.46, Revision: 05, Date Created: Apr 15, 2024



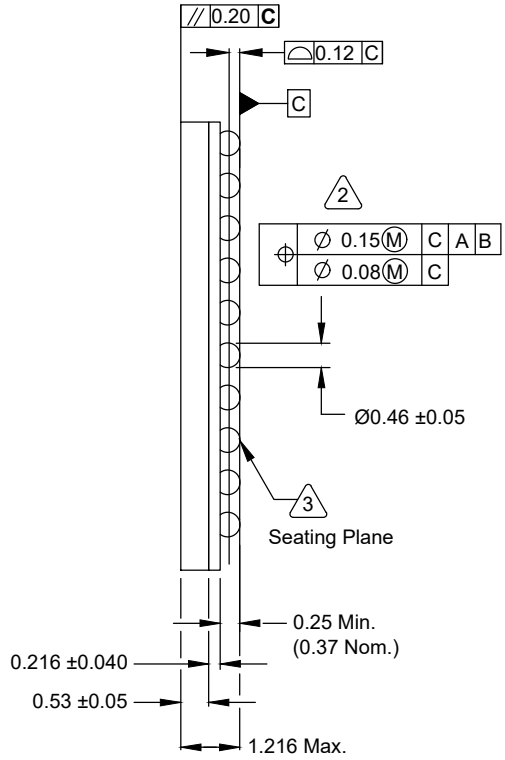
Top View



Bottom View



Typical Recommended Land Pattern



Side View

Notes:

1. All dimensions and tolerances conform to ASME Y14.5 - 2009.
2. Dimension is measured at the maximum solder ball diameter, parallel to primary datum C.
3. Primary datum C and seating plane are defined by the spherical crowns of the solder balls.
4. Unless otherwise specified, dimensions are in millimeters.

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