RAA271041

Cold Crank Boost and Buck Controller with Drivers for ASIL-D Automotive Applications

Description

The RAA271041 is a controller for a dual regulator system capable of supporting ASIL-D automotive systems which must operate during battery dropout conditions. The Channel 2 boost regulator maintains the voltage rail which supplies the downstream Channel 1 buck regulator, allowing the buck output to maintain regulation during a battery dropout event such as cold cranking.

For Cold Crank applications, the Channel 2 Boost has an adjustable output and is active when the V_{BAT} input voltage falls below a user-programmable threshold. The boost channel can also be configured as an independent boost with separate Enable (WAKE2) control.

The boost output from Channel 2 supplies the input for Channel 1 buck. The buck output can be configured either as 3.3V, 5V, or as an adjustable voltage from 0.8V to 12V using a resistor divider.

The RAA271041 requires a typical input voltage of 5.5V at the VIN pin for start-up. The Channel 2 Boost has an input range from 2.1V to 42V while the Channel 1 Buck has an input range from 3.5V to 42V.

The RAA271041 buck channel can operate in Energy Conservation Mode (ECM) to reduce quiescent current draw to 8µA typical when no external load is applied. The buck switching frequency is factory programmable to 440kHz or 2.2MHz. The boost switching frequency is also factory programmable to 440kHz, or 2.2MHz if the buck channel is also set to 2.2MHz. Optional spread spectrum operation is available to reduce EMI and noise levels.

Features

- ASIL-D Functional Safety
- 40V boost and buck integrated driver controller
- FET drivers support source/sink current of 2A/3A
- Low I_Q with ECM mode of 8µA typical (buck Channel 1 only)
- Separate or Combined Wake (Enable) inputs for each channel
- Minimized FET ON and OFF times (25ns and 45ns)
- High-efficiency buck exceeding 80% at 10mA
- Buck frequency options 440kHz or 2.2MHz
- Boost frequency options 440kHz or 2.2MHz (2.2MHz Boost requires 2.2MHz Buck frequency)
- VBATS sense for Boost Enable during Cold Crank
- Optional pseudo-random spread spectrum clocking
- External synchronization using SYNC pin
- Dual Over-temperature protection monitors
- Extensive protection mechanisms for OV/UV/OC/OT
- 6x6mm 36Ld SC-QFN package
- AEC-Q100 grade 1 qualified
- Functional Safety Features
  - Built-in Self Test (LBIST and ABIST) at power up
  - Recurring Checks: Internal References, PWM clock, System Clock, PGND/AGND connection, Dual Over-Temperature monitor, VCC supply, Logic Pin Stuck Low.
  - Independent References and feedback sense paths for Buck and Boost OV/UV detection
  - Independent Fault Indicators for Buck and Boost
  - Fail-Safe Output, logic high indicates a trusted device state and all safety monitors are active.

Applications

- Automotive battery supplied applications
- In cabin systems
- ADAS: Advanced Driver Assist Systems
- Start-stop protected systems (such as head unit, cluster, e-Mirror)

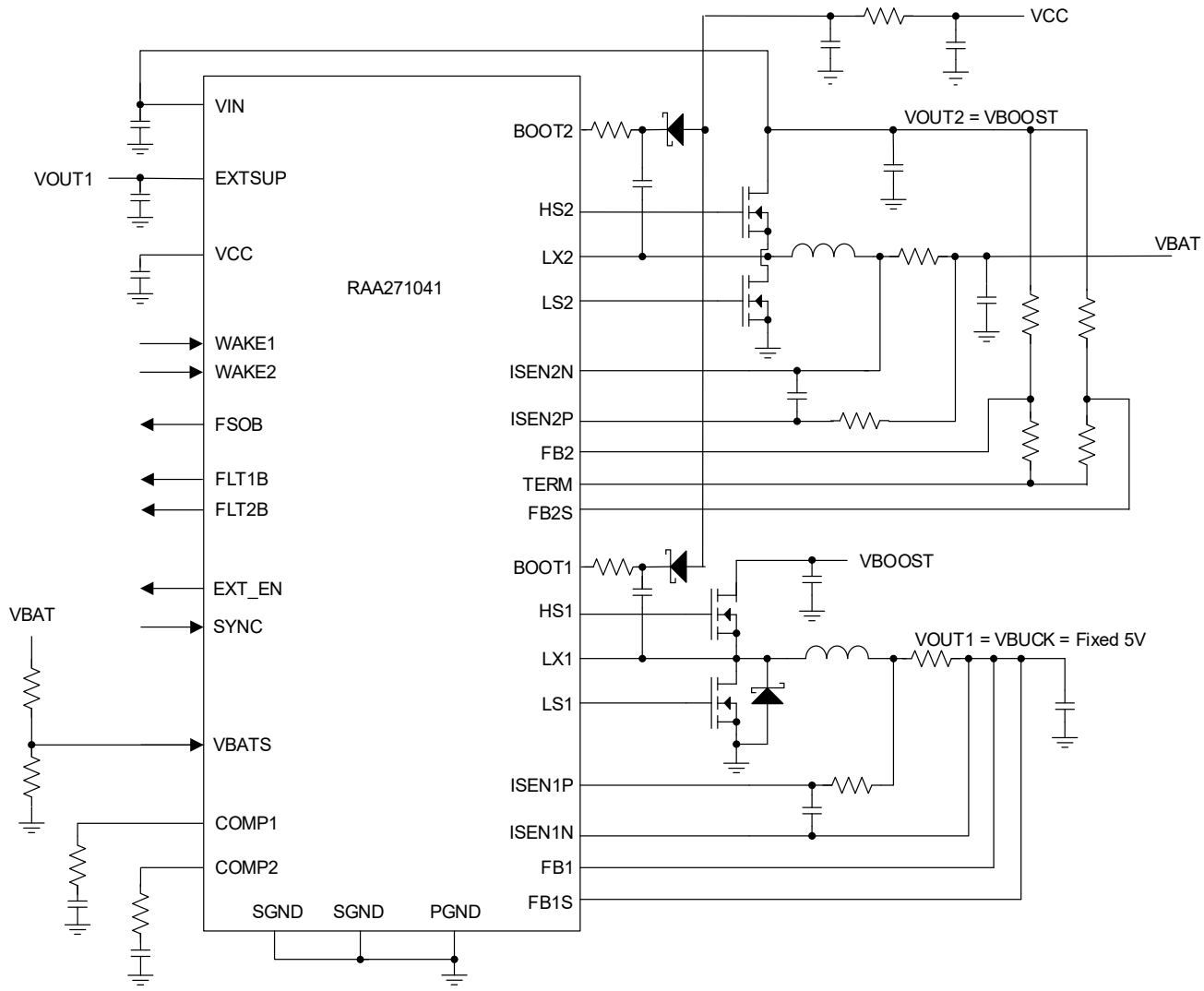


Figure 1. Typical Application Schematic

Contents

1. Overview

1.1 Typical Application Schematics

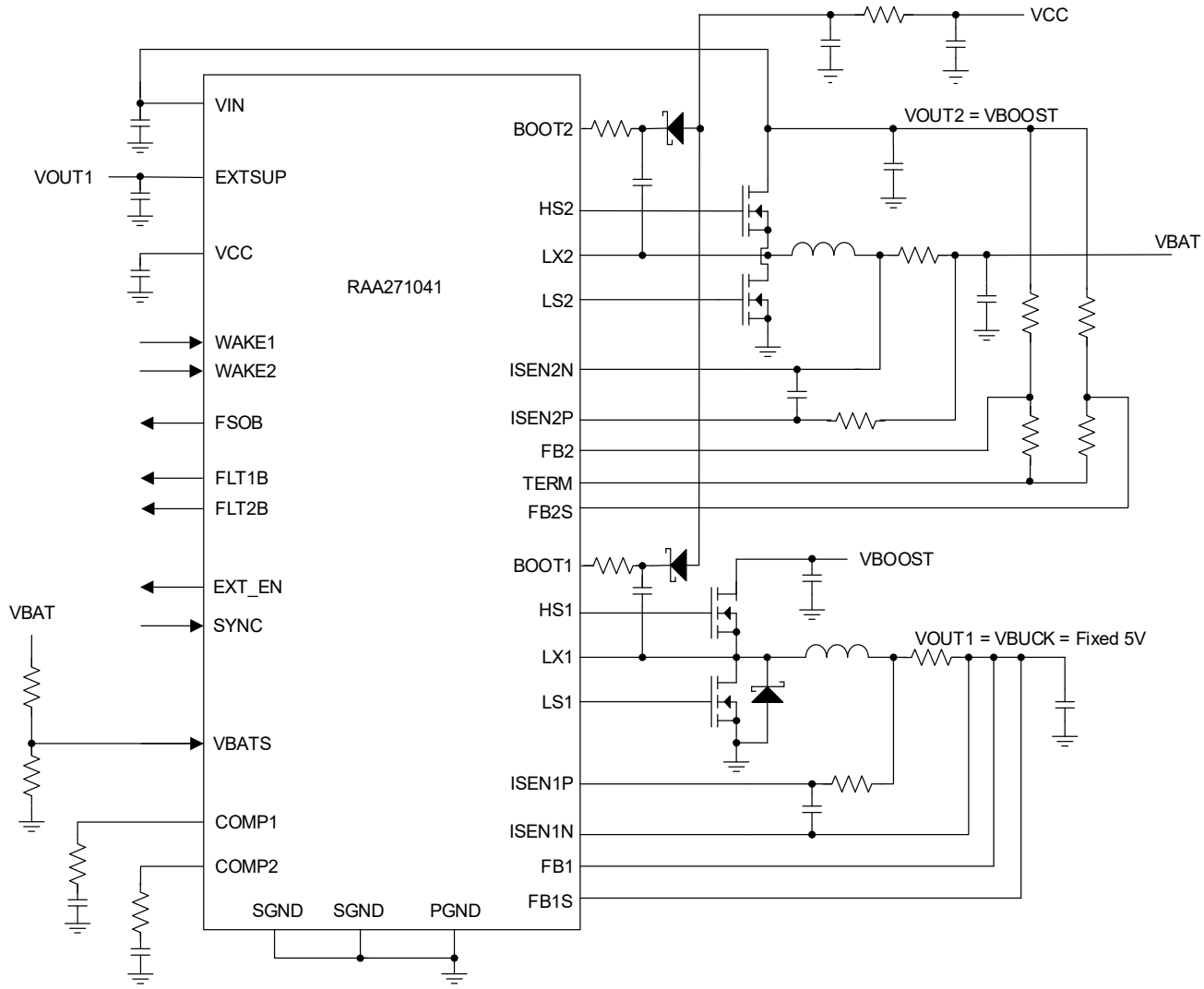


Figure 2. Typical Cold Crank Applications Schematic (VOUT1 Fixed 5V, EXTSUP connected to VOUT1)

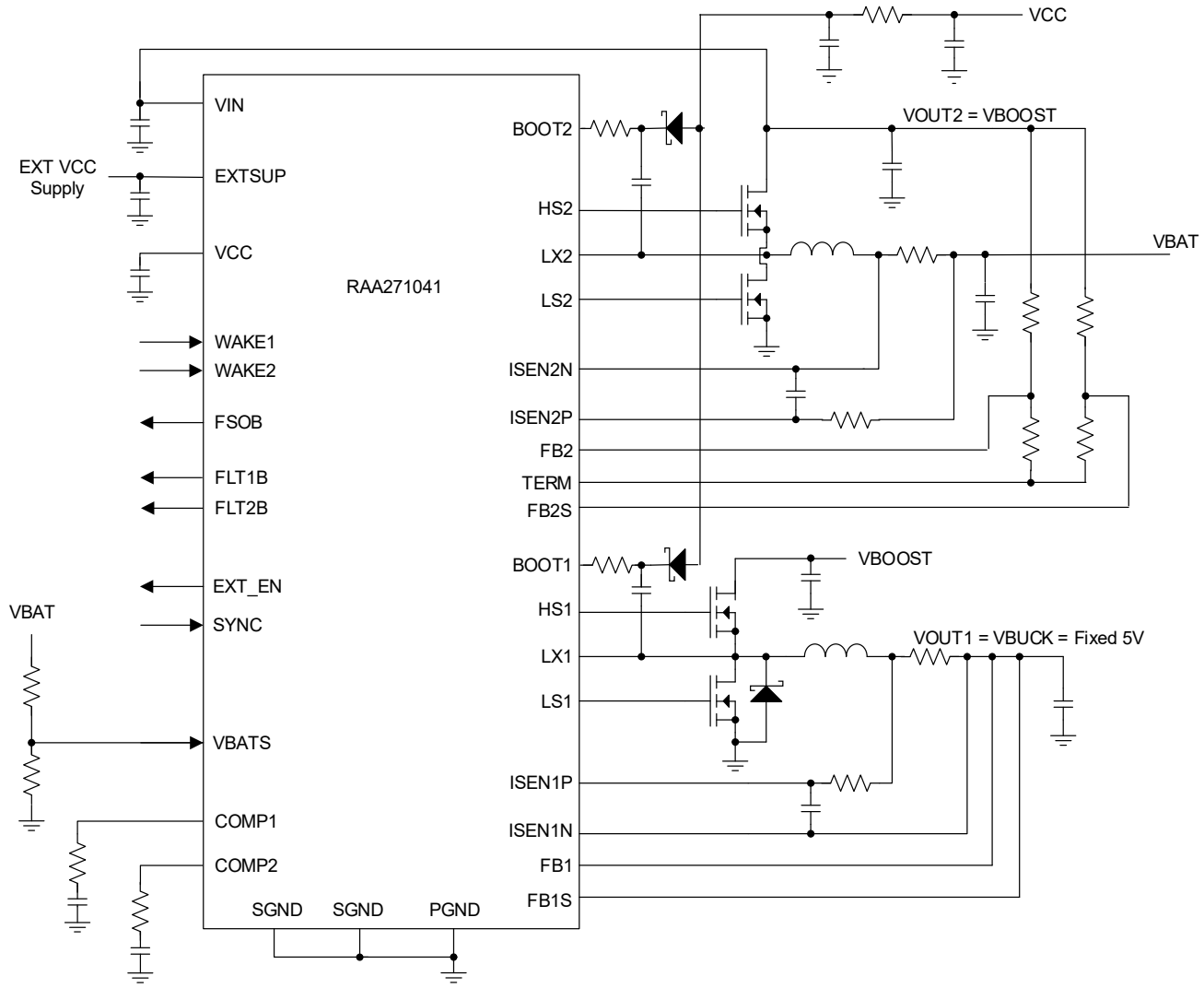


Figure 3. Typical Cold Crank Applications Schematic - EXT VCC Supplied, VOUT1 Fixed 5V)

1.2 Block Diagram

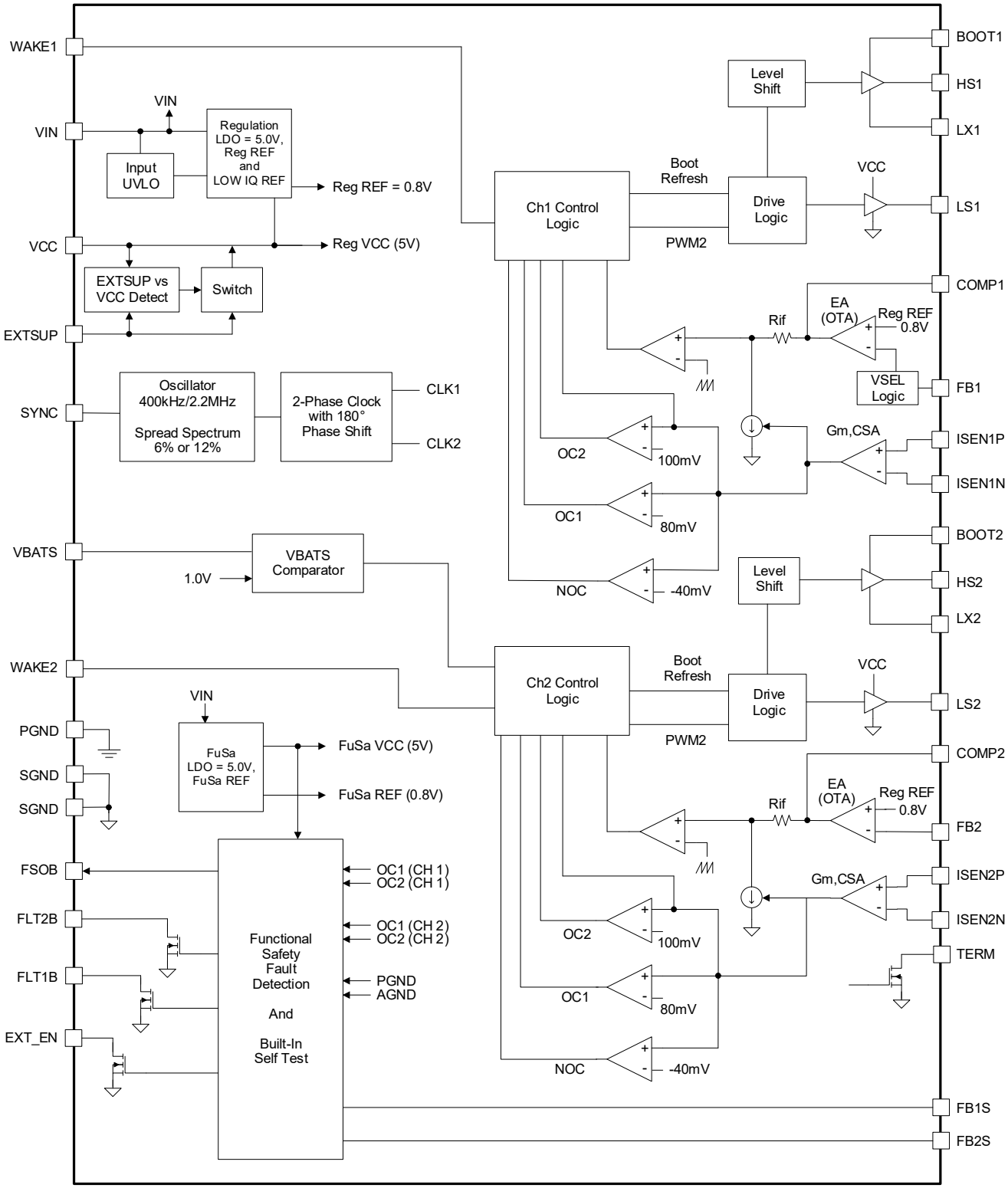


Figure 4. Block Diagram

2. Pin Information

2.1 Pin Assignments

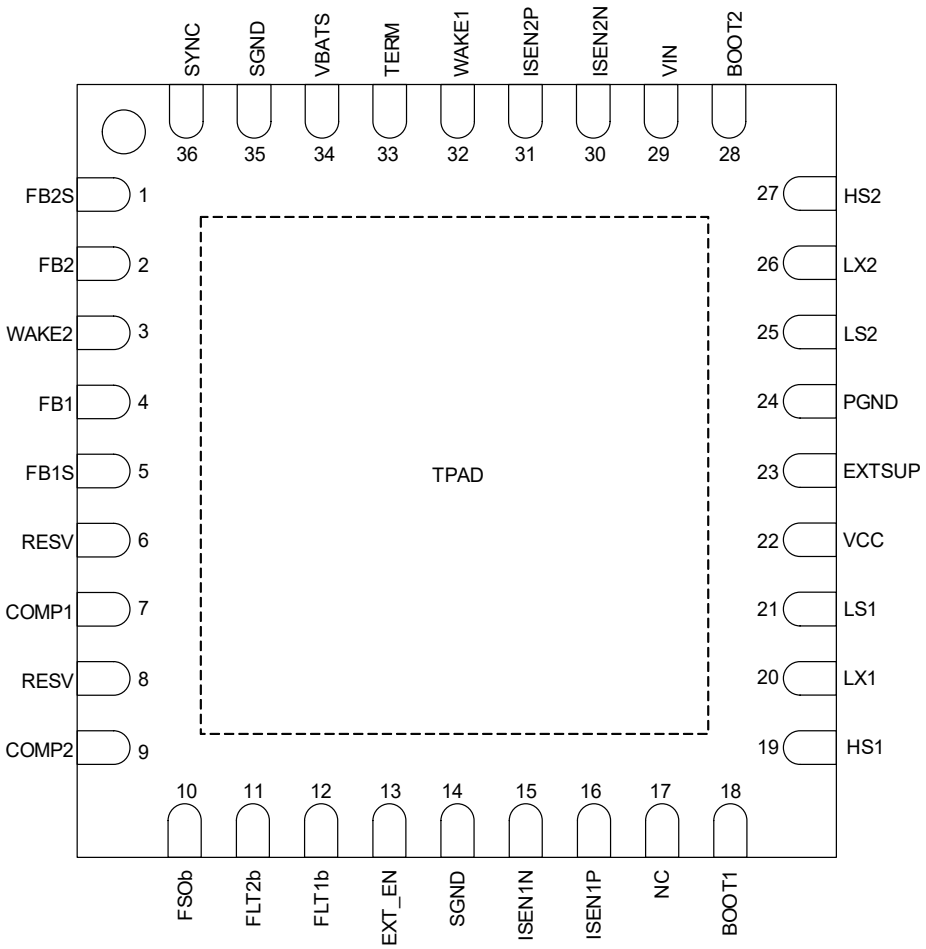


Figure 5. Pin Assignments - Top View

2.2 Pin Descriptions

Pin Number	Pin Names	Description
1	FB2S	OV/UV sense input for Channel 2 boost regulator. Connect to a resistor divider from Channel 2 Boost output to the TERM pin. For ASIL protection, this resistor divider must be a separate copy of the divider used for pin FB2.
2	FB2	Feedback input for Channel 2 adjustable-output boost regulator. Connect to a resistor divider from Channel 2 Boost output to the TERM pin. FB2 is regulated to 0.8V.
3	WAKE2	Enable input for both channels for Enable Fuse option 1. Enable input for Channel 2 only for Enable Fuse option 2. Logic high activates the enable.
4	FB1	Feedback input for Channel 1 buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly to the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground, and the FB1 voltage is regulated to 0.8V.
5	FB1S	OV/UV sense input for Channel 1 buck regulator. For fixed output voltages of 5.0V or 3.3V, this pin connects directly to the output of Channel 1 buck. For adjustable output, this pin connects to a resistive divider from Channel 1 output to ground. For ASIL protection, this resistor divider must be a separate copy of the divider used for pin FB1.
6, 8	RESV	Reserved, connect to SGND.
7	COMP1	Loop compensation pin for Channel 1 with a resistor/capacitor/capacitor network connected to ground, to provide control loop compensation for Channel 1 buck regulator.
9	COMP2	Loop compensation pin for Channel 2 with a resistor/capacitor/capacitor network connected to ground, to provide control loop compensation for Channel 2 boost regulator.
10	FSOb	Fail Safe Output (Indicator). Asserted high indicates the device is not in a Fail State and all safety monitors are active.
11	FLT2b	Open drain Fault Indicator for Channel 2 (boost). Output low state indicates a Channel 2 fault.
12	FLT1b	Open drain Fault indicator for Channel 1 (buck). Output low state indicates a Channel 1 fault.
13	EXT_EN	Open drain indicator for Channel 1. Open state indicates that Channel 1 buck is enabled and is operating in regulation.
14, 35	SGND	Analog ground, connect to PGND pin in the top copper trace under the IC.
15	ISEN1N	Negative input to Channel 1 buck output current sense. Connect to the output voltage of Channel 1.
16	ISEN1P	Positive input to Channel 1 buck output current sense. Connect through an R-C filter to the positive (inductor) side of the Channel 1 output current sense resistor.
17	NC	Leave this pin unconnected to allow proper node clearance.
18	BOOT1	Floating supply voltage for Channel 1 high-side MOSFET gate driver. Connect to a 0.1uF ceramic capacitor which connects from BOOT1 to LX1. The capacitor is charged using an external diode connected to VCC through an R-C filter.
19	HS1	Output of Channel 1 high-side MOSFET gate driver.
20	LX1	Channel 1 switch node, and return path for the high-side MOSFET gate driver between BOOT1 and LX1.
21	LS1	Output of Channel 1 low-side MOSFET gate driver; switches between VCC and GND.
22	VCC	Bias supply (5V typical) for the IC and the MOSFET gate drivers. Decouple with a 10µF ceramic capacitor. This pin is supplied by the internal LDO during start-up. After initial start-up, the bias voltage can be supplied from either the buck 5V output or an external supply, using the automatic switchover feature of the EXTSUP pin.
23	EXTSUP	Input to the automatic switchover circuit for the VCC bias supply. EXTSUP accepts an external 5V supply derived from either a Channel 1 output of 5V or an independent 5V supply. Do Not apply External bias to EXTSUP until VIN has exceeded initial start-up voltage; however, a voltage such that EXTSUP - VIN ≤ 0.5V can be tolerated.
24	PGND	Connection point for power ground of the switching circuits for Channel 1 and Channel 2, and is the return path for the low-side MOSFET gate drivers.
25	LS2	Output of Channel 2 low-side MOSFET gate driver, switches between VCC and GND.
26	LX2	Channel 2 switch node, also is the return path for the high-side MOSFET gate driver between BOOT2 and LX2.
27	HS2	Output of Channel 2 high-side MOSFET gate driver.
28	BOOT2	Floating supply voltage for Channel 2 high-side MOSFET gate driver. Connect to a 0.1µF ceramic capacitor which connects from BOOT2 to LX2. The capacitor is charged using an external diode connected to VCC through an R-C filter.

Pin Number	Pin Names	Description
29	VIN	For Cold Crank (CC) applications, connect this pin to the output of the Boost Channel 2. For Individual Buck/Boost (IBB) applications, connect this pin to the VBAT power input. This pin is decoupled using a 0.1µF or larger ceramic capacitor.
30	ISEN2N	Negative input to Channel 2 boost input current sense. Connect through an R-C filter to the negative (inductor) side of the Channel 2 input current sense resistor.
31	ISEN2P	Positive input to Channel 2 boost input current sense. Connect to the positive side of the Channel 2 input current sense resistor, typically connected to VBAT which is the DC input voltage.
32	WAKE1	Enable input for Channel 1 buck.
33	TERM	Open drain pull-down for the bottom side of the FB2 and FB2S resistor dividers. This pin becomes open (float) when the boost channel is disabled, to eliminate power loss in the FB2 and FB2S resistor dividers.
34	VBATS	VBAT sense input which sets the boost turn-on threshold for when the battery input falls below normal, such as during Cold Crank. Connect to a resistor divider to set the voltage threshold which enables the boost channel. VBATS threshold is 1.0V. *Note*: The VBATS turn on/off function for the boost channel is disabled when Individual Buck/Boost operation is selected using factory OTP.
36	SYNC	The SYNC pin selects modes of operation including FCCM (SYNC = logic high), ECM and DCM (SYNC = logic low), and synchronization to an external oscillator in FCCM. Please refer to the SYNC section in applications information for details.
-	TPAD	Bottom pad, used for thermal heat dissipation. Connect to PCB GND layers, using multiple vias to conduct heat away from the device.

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
VIN, WAKE1, FB2, FB2S, ISEN2N, ISEN2P, TERM, VBATS, LX1, LX2	-0.3	45	V
HS1, HS2, BOOT1, BOOT2	-0.3	51.5	V
WAKE2, COMP1, COMP2, SYNC	-0.3	6.5	V
LS1, LS2, VCC, EXTSUP, FLT1b, FLT2b, FSOb, EXT_EN	-0.3	6.5	V
ISEN1N, ISEN1P, FB1, FB1S	-0.3	42[1]	V
SGND to PGND	-0.3	0.3	V
All Other Pins	-0.3	6.5	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per AEC-Q100-002)	-	2	kV
Charged Device Model (Tested per AEC-Q100-001)	-	750	V
Latch-Up (Tested per AEC-Q100-004)	-	100	mA

1. In case of a high-side FET short, FB1 can tolerate 42V. Long term exposure to voltage exceeding 14V can adversely impact product reliability and result in failures not covered by warranty.

3.2 Recommended Operating Condition

Parameter[1] [2]	Minimum	Maximum	Unit
Ambient Temperature Range	-40	+125	°C
Junction Operating Temperature Range	-40	+150	°C
Startup Voltage Range V_{IN}	6.0	42	V
Battery Voltage Range V_{BAT} (Cold Crank)	2.1	42	V
Buck Channel 1 V_{OUT} Fixed options	3.3	5.0	V
Buck Channel 1 V_{OUT} Adjustable Range	0.8	12	V
Boost Channel 2 V_{OUT} Adjustable Range	5.0	40	V

1. The device can handle load dump voltage up to maximum voltage and should not exceed the Absolute Maximum Ratings. 42V continuous input voltage is possible but not recommended.
2. Higher input voltage can result in higher thermal dissipation within the device. For such applications improved thermal performance might be required. Consult section 3.3 for Thermal Information.

3.3 Thermal Information

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	36-SCQFN part 6.0× 6.0 mm	θ_{JA}[1]	Junction to ambient	27	°C/W
		θ_{JC}[2]	Junction to case	0.9	°C/W

1. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with direct attach features. See TB379.
2. For θ_{JC}, the case temperature location is the center of the exposed metal pad on the package underside.

3.4 Electrical Specifications

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.**

Parameter	Symbol	Test Conditions	Min[1]	Typ[2])	Max([1])	Unit
Power Supply						
V_{IN} Undervoltage Lockout Threshold	$V_{IN,UVLO}$	Rising voltage sensed at VIN pin	**5.35**	5.5	**5.65**	V
Boost On/Off Threshold (V_{IN} Monitor, sensed at ISEN2P pin)	V_{INL}	Turn-on threshold rising, measured at ISEN2P	**2.7**	2.8	**2.9**	V
		Turn-off threshold falling, measured at ISEN2P	**2.0**	2.1	**2.2**	V
VBATS Threshold (VBATS Monitor)	V_{VBATS}	VBATS turn-on threshold, falling	**0.9**	1.0	**1.1**	V
		VBATS turn-off threshold, rising	**0.97**	1.07	**1.17**	V
		VBATS hysteresis	-	70	-	mV
$V_{IN+EXTSUP}$ Supply Current in ECM	I_{QECM}	ECM mode, no external load on V_{OUT}[3]	-	8	**30**	µA
$V_{IN+EXTSUP}$ Supply Current during Normal Switching	I_Q	PWM mode, no external load on V_{OUT1}, WAKE1 = WAKE2 = HIGH, f_{SW} = 440kHz, No Load, Channel 2 off (sum of current into VIN and EXTSUP pins, excluding gate driver currents)	-	15	**25**	mA
		PWM mode, no external load on V_{OUT}, WAKE1 = WAKE2 = HIGH, f_{SW} = 2.2MHz, No Load, Channel 2 off (sum of current into VIN and EXTSUP pins, excluding gate driver currents)	-	20	**30**	mA
V_{IN} Overvoltage Threshold	$V_{IN,OV}$	VIN pin or VBATS pin (per factory programming)	**40**	43	**45**	V
V_{IN} Supply Current, Shutdown	I_{SD}	WAKE1 = WAKE2 = SGND	-	0.5	**10**	µA
LDO and EXTSUP						
Output Voltage of Internal LDO	V_{VCC}	V_{IN} = 6.0V to 42V, I_{OUT} = 130mA	**4.75**	5.00	**5.25**	V
Output Current of Internal LDO	I_{VCC}	V_{IN} = 6.0 to 42V	-	-	**0.13**	A
Dropout Voltage of Internal LDO	D_{VCC}	V_{IN} = 5.1V, I_{LDO} = 130mA	-	0.55	**1.2**	V
Low (Min) VIN LDO Reset	-	I_{LDO} = 130mA and V_{CC} drops to VCC UVLO falling threshold	**4.75**	4.4	-	V
LDO Current Limit	I_{LMTLDO}	V_{CC} = 4.5V	**120**	180	**250**	mA
		V_{CC} = 0V	**110**	300	**450**	mA
VCC Undervoltage Lockout Threshold	$V_{VCCUVLO}$	Falling	**3.85**	4.0	**4.15**	V
External Bias Voltage Range	V_{EXTSUP}	For VOUT1 buck = 5V ±5%	**4.75**	5.00	**5.25**	V
External Bias Voltage Switchover Threshold	VTH_{EXTSUP}	Rising	-	4.55	**4.7**	V
		Falling	**4.2**	4.33	-	V
		Hysteresis	-	0.22	-	V
Oscillator, Spread Spectrum						
Internal Switching Range - Low	f_{SWIR1}	Range 1	**400**	440	**480**	MHz
Internal Switching Range - High	f_{SWIR2}	Range 2	**2.0**	2.2	**2.4**	MHz
Frequency Tolerance	F_{reqTol}	Internal 440kHz or 2.2MHz	-10	-	+10	%
External Switching Frequency	f_{SWEXR1}	Range 1; applied to SYNC pin	**400**	-	**480**	MHz
	f_{SWEXR2}	Range 2; applied to SYNC pin	**2.0**	-	**2.4**	MHz
Spread Spectrum Narrow Mode	F_{SSNAR}	Spread Spectrum ON, narrow mode	-	+6	-	%

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2])	Max([1])	Unit
Spread Spectrum Wide Mode	F_{SSWID}	Spread Spectrum ON, wide mode	-	+12	-	%
Controller 1 Specification (Buck)						
Output Voltage during normal operation	V_{OUT1_3}	Fixed 3.3V selected; SYNC = VCC	**-1.5%**	3.3	**+1.5%**	V
	V_{OUT1_5}	Fixed 5.0V selected; SYNC = VCC.	**-1.5%**	5.0	**+1.5%**	V
FB1 Pin Voltage Regulation (Adj)	V_{FB1}	Adjustable output selected; SYNC = VCC	**-1.5%**	0.8	**+1.5%**	V
V_{OUT1} Comparator Threshold at ECM	V_{ECMTH1}	V_{OUT} = Fixed 3.3V; SYNC = GND	**-2%**	3.3	**+2%**	V
		V_{OUT} = Fixed 5.0V; SYNC = GND	**-2%**	5.0	**-+2%**	V
		V_{FB} = 0.8V (adjustable V_{OUT1}); SYNC = GND	**-2%**	0.80	**+2%**	V
FB1/FB1S Pin Leakage Current	I_{FBCH1}	-	-	0.2	**1.5**	µA
Forward CH1 Cycle-by-Cycle Current Limit	$I_{LMT1CH1+}$	ISEN1P-ISEN1N	**60**	80	**100**	mV
Forward CH1 Hiccup Current Limit	$I_{LMT2CH1+}$	ISEN1P-ISEN1N	**75**	100	**125**	mV
Negative CH1 Current Limit (NOC)	$I_{LMTCH1-}$	ISEN1P-ISEN1N	**-55**	-40	**-25**	mV
CH1 Zero Cross	V_{ZCD1}	-	**-7**	0	**7**	mV
CH1 Dead Time	T_{DTLH1S}	Low-side low to high-side high	**15**	25	**45**	ns
	T_{DTHL1S}	High-side low to low-side high	**20**	45	**70**	ns
	T_{DTLH1L}	Low-side low to high-side high	**70**	95	**120**	ns
	T_{DTHL1L}	High-side low to low-side high	**70**	95	**120**	ns
CH1 Maximum Duty	T_{DTMAX1}	-	-	98.5	-	%
CH1 Minimum On-time	T_{ONMIN1}	-	**10**	25	**50**	ns
CH1 Minimum Off-time	$T_{OFFMIN1}$	-	**30**	45	**60**	ns
CH1 Soft-Start Time	T_{SSCH1}	FB1 from 0V to regulation point	-	630	-	µs
CH1 Buck Error Amp (OTA) GM	$CH1_{EAOTA}$	-	-	1.7	-	mS
BOOT1 Refresh Threshold	$V_{B1RFRESH}$	Rising	**3.35**	3.5	**3.65**	V
		Falling	**3.25**	3.4	**3.55**	V
		Hysteresis	-	0.1	-	V
CH1 Warning Overvoltage Threshold	OV_{THCH1}	Rising Threshold (options = +6%, +8%, +12%)	**-2**	-	**+2**	%
CH1 Severe Overvoltage Threshold	SOV_{THCH1}	Rising Threshold (options = +12%, +15%)	**-2**	-	**+2**	%
CH1 Warning Undervoltage Threshold	UV_{THCH1}	Falling Threshold (options = -5%, -8%, -12%)	**-2**	-	**+2**	%
CH1 Severe Undervoltage Threshold	SUV_{THCH1}	Falling Threshold (options = -12%, -15%)	**-2**	-	**+2**	%
CH1 V_{IN} ECM Lockout Threshold	VTH_{ECMLO}	Rising	**17**	18.5	**20**	V
		Falling	**16.5**	18	**19.5**	V
		Hysteresis	-	0.5	-	V
CH 1 ECM Entry Threshold	VTH_{ECMENT}	Rising	**5.4**	5.55	**5.7**	V
		Falling	**5.1**	5.25	**5.4**	V
		Hysteresis	-	0.3	-	V

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2])	Max([1])	Unit
Controller 2 Specification (Boost)						
FB2 Pin Voltage Regulation	V_{FBCH2}	V_{OUT} adjustable	**0.788**	0.8	**0.812**	V
FB2/FB2S Pin Leakage Current	I_{FBCH2}	-	-	0.1	**0.25**	µA
Forward CH2 Cycle-by-Cycle current limit	$I_{LMT1CH2+}$	ISEN2P-ISEN2N	**60**	80	**100**	mV
Forward CH2 Hiccup Current Limit	$I_{LMT2CH2+}$	ISEN2P-ISEN2N	**75**	100	**125**	mV
Negative CH2 Current Limit (NOC)	$I_{LMTCH2-}$	ISEN2P-ISEN2N	**-55**	-40	**-25**	mV
CH2 Zero Cross	V_{ZCD2}	-	**-7**	0	**7**	mV
CH2 Dead Time	T_{DTLH2S}	Low-side low to high-side high	**10**	25	**45**	ns
	T_{DTHL2S}	High-side low to low-side high	**20**	45	**70**	ns
	T_{DTLH2L}	Low-side low to high-side high	**70**	95	**120**	ns
	T_{DTHL2L}	High-side low to low-side high	**70**	95	**120**	ns
CH2 Maximum Duty	D_{MAX2}	-	-	95	-	%
CH2 Minimum On-time	T_{ONMIN2}	-	**10**	25	**50**	ns
CH2 Minimum Off-time	$T_{OFFMIN2}$	-	**25**	45	**55**	ns
CH2 Soft-Start Time	T_{SSCH2}	Not applicable to Boost Cold Crank startup. Applies to Independent Buck/Boost mode only.	-	630	-	µs
Boost Error Amp (OTA) GM	$CH2EA_{OTA}$	-	-	1.7	-	mS
BOOT2 Refresh	$V_{B2RFRESH}$	Falling	**3.35**	3.5	**3.65**	V
		Rising	**3.25**	3.4	**3.55**	V
		Hysteresis	-	0.1	-	V
CH2 Warning Overvoltage Threshold	OV_{THCH2}	Rising Threshold (options = +6%, +8%, +12%)	**-2**	-	**+2**	%
CH2 Severe Overvoltage Threshold	SOV_{THCH2}	Rising Threshold (options = +12%, +15%)	**-2**	-	**+2**	%
CH2 Warning Undervoltage Threshold	UV_{THCH2}	Falling Threshold (options = -5%, -8%, -12%)	**-2**	-	**+2**	%
CH2 Severe Undervoltage Threshold	SUV_{THCH2}	Falling Threshold (options = -12%, -15%)	**-2**	-	**+2**	%
Output Drivers						
High-Side Drive Source Current	$I_{HS,SRC}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V	-	1	-	A
High-Side Drive Source Resistance	$R_{HS,SRC}$	100mA source current, V_{BOOT} - V_{LX} = 4.4V	-	2	-	Ω
High-Side Drive Sink Current	$I_{HS,SNK}$	V_{HS} - V_{LX} = 2.5V, V_{BOOT} - V_{LX} = 4.4V	-	1	-	A
Hide-Side Drive Sink Resistance	$R_{HS,SNK}$	100mA sink current, V_{BOOT} - V_{LX} = 4.4V	-	1.5	-	Ω
Low-Side Drive Source Current	$I_{LS,SRC}$	V_{LS} - V_{PGND} = 2.5V, VCC = 5V	-	1	-	A
Low-Side Drive Source Resistance	$R_{LS,SRC}$	100mA source current, VCC = 5V	-	2	-	Ω
Low-Side Drive Sink Current	$I_{LS,SNK}$	V_{LS} - V_{PGND} = 2.5V, V_{CC} = 5V	-	1.5	-	A
Low-Side Drive Sink Resistance	$R_{LS,SNK}$	100mA sink current, V_{CC} = 5V	-	1.5	-	Ω

V_{IN} = 12V, T_A = +25°C. **Boldface limits apply across the operating junction temperature range, -40°C to +125°C and input voltage range (4.5V to 42V) unless specified otherwise.** (Cont.)

Parameter	Symbol	Test Conditions	Min[1]	Typ[2])	Max([1])	Unit
Input Pins						
WAKE1 Input Low Voltage threshold	VIL_{WAKE1}	WAKE1 = CH1 = buck turned OFF; CH2 can be ON/OFF	**0.4**	0.85	-	V
WAKE1 Input High Voltage threshold	VIH_{WAKE1}	WAKE1 = CH1 = buck turned ON; CH2 can be ON/OFF	-	1.25	**1.6**	V
WAKE1 Leakage Current	ILK_{WAKE1}	WAKE1 = 12V	**-0.5**	-	**0.5**	µA
WAKE2 Input Low Voltage threshold	VIL_{WAKE2}	WAKE2 = CH2 = Boost turned OFF; CH1 can be ON/OFF	**0.4**	0.85	-	V
WAKE2 Input High Voltage threshold	VIH_{WAKE2}	WAKE2 = CH2 = Boost turned ON; CH1 can be ON/OFF	-	1.25	**1.6**	V
WAKE2 Leakage Current	ILK_{WAKE2}	WAKE2 = VCC	**-0.5**	-	**0.5**	µA
SYNC Input Low Voltage	VIL_{SYNC}	-	-	-	**0.3×VCC**	V
SYNC Input High Voltage	VIH_{SYNC}	-	**0.7×VCC**	-	-	V
SYNC Pulse Width High	$T_{SYNCMINH}$	-	**50**	-	-	ns
SYNC Pulse Width Low	$T_{SYNCMINL}$	-	**50**	-	-	ns
Switching Frequency SYNC Range	f_{SYNC}	-	**-10**	-	**10**	%
Output Pins						
FLT1b Pin Voltage	VOL_{FLT1b}	V_{OUTCH1} = OFF; Sink Current = 3mA	-	0.1	**0.4**	V
FLT2b Pin Voltage	VOL_{FLT2b}	V_{OUTCH2} = OFF; Sink Current = 3mA	-	0.1	**0.4**	V
FLT1b Pin Leakage Current	ILK_{FLT1b}	$V_{PULL-UP}$ = 5V	-	0.01	**1**	µA
FLT2b Pin Leakage Current	ILK_{FLT2b}	$V_{PULL-UP}$ = 5V	-	0.01	**1**	µA
EXT_EN Pin Voltage	VOL_{EXT_EN}	EXT_EN = low; sink Current = 3mA	-	0.1	**0.4**	V
EXT_EN Pin Leakage Current	ILK_{EXT_EN}	$V_{PULL-UP}$ = 5V	-	0.01	**1**	µA
FSOb Output High Voltage	$FSOb_{VH}$	With respect to VCC; FSO Source Current = 3mA	**-0.6**	-0.3	-	V
FSOb Output Low Voltage	$FSOb_{VL}$	FSOb Sink Current = 3mA	-	0.3	**0.6**	V
TERM Pin Resistance	R_{TERM}	-	**10**	30	**70**	Ω
TERM Leakage Current	ILK_{TERM}	-	-	0.01	**1**	µA
Thermal Shutdown[4]	T_{OTP}	Rising	151	160	175	°C
Thermal Shutdown LDO	T_{TSL}	Rising	160	170	180	°C

1. Parameters with MIN and/or MAX limits are 100% tested at +50°C, unless otherwise specified. Temperature limits established by characterization and are not production tested.
2. Typical values are for T_A = +25°C and V_{IN} = 12V.
3. Quiescent current measurements are taken when the output is not switching. (Condition VIN = 12V, VOUT1 = 5V, EXTSUP = VOUT1).
4. MIN and MAX based on Design Spec or Simulations. Not tested on ATE.

4. Typical Perfomance Curves

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation.

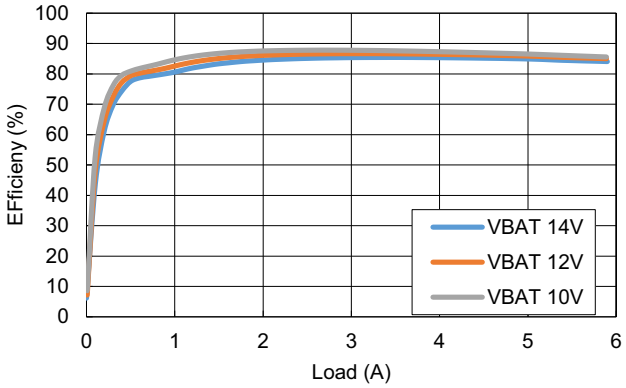


Figure 6. CCM Efficiency (Buck) VOUT1 = 5V, 2.2MHz, EXTSUP = GND

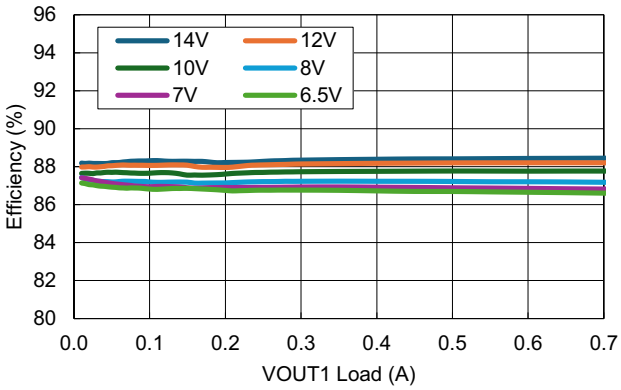


Figure 7. ECM Efficiency (Buck) VOUT1 = 5V, 2.2MHz, EXTSUP = VOUT1

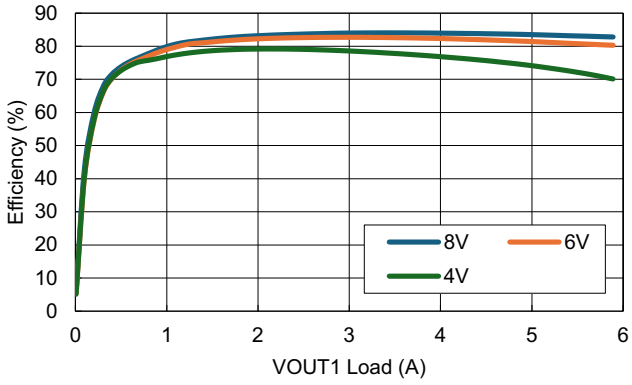


Figure 8. CCM Efficiency (Boost) VOUT2 = 12V, 2.2MHz

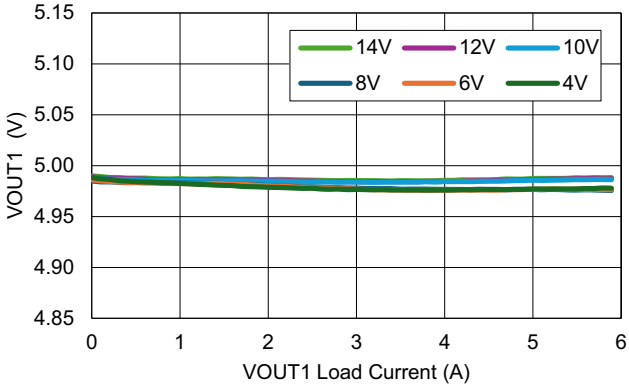


Figure 9. CCM VOUT1 Load Regulation, VOUT1 = 5V, 2.2MHz

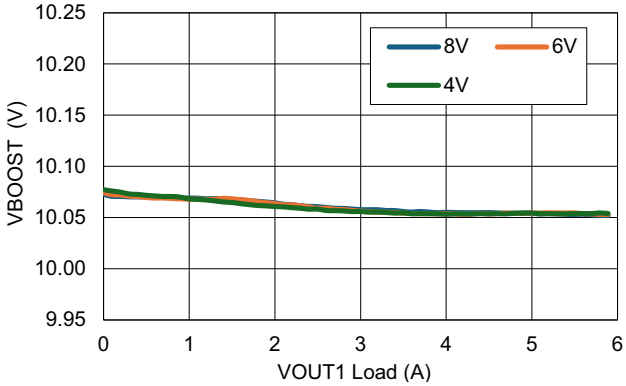


Figure 10. CCM VOUT2 Load Regulation, VOUT2 = 10V, 2.2MHz

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. (Cont.)

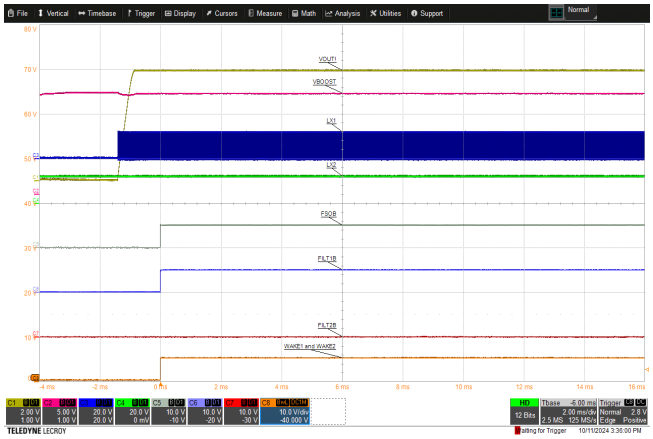


Figure 11. Startup, VBAT = 12V, WAKE1 = VBAT

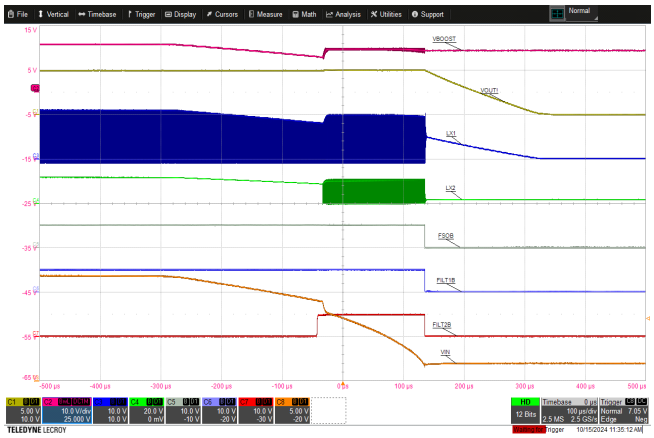


Figure 12. Shutdown using VBAT Ramp Down, VBAT = 12V, WAKE1 = VBAT

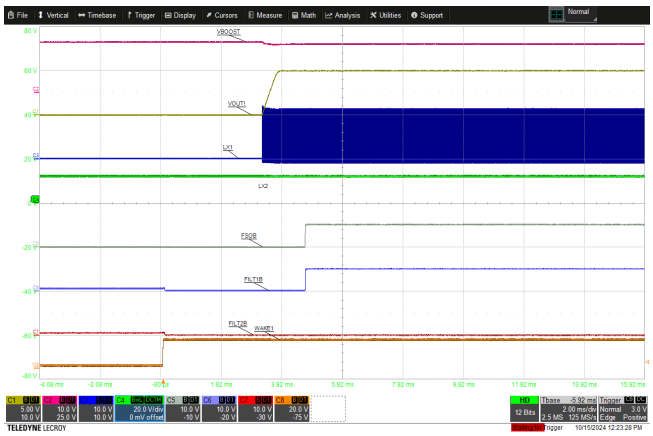


Figure 13. Startup using WAKE1 Toggle, VBAT = 12V

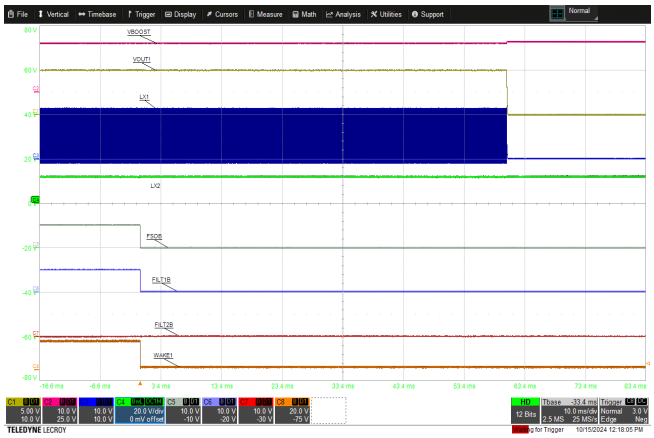


Figure 14. Shutdown using WAKE1 toggle, VBAT = 12V

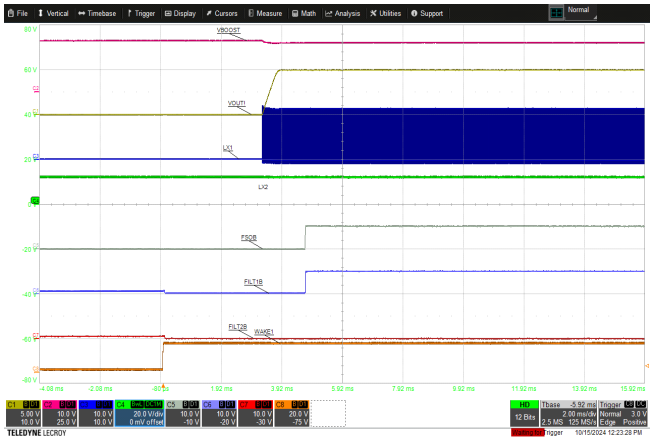


Figure 15. Startup at 12V with WAKE1 Switched to VIN

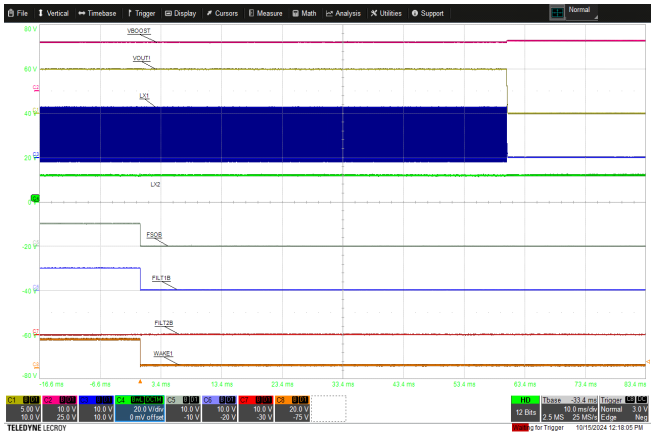


Figure 16. Shutdown at 12V with WAKE1 Switched to GND, No load

Unless otherwise noted, operating conditions are: T_A = +25°C, V_{IN} = 6V, VOUT1 = 5V, VOUT2 = 10V in cold crank operation. (Cont.)

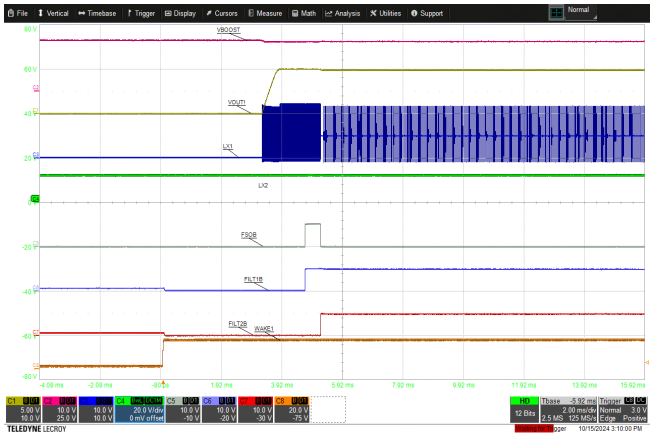


Figure 17. BUCK1 Startup with Wake1 Switched High with SYNC Low

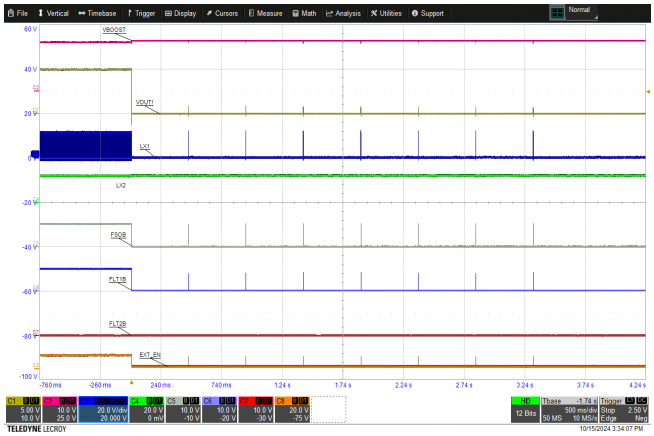


Figure 18. BUCK1 Output Shorted with Latch Off

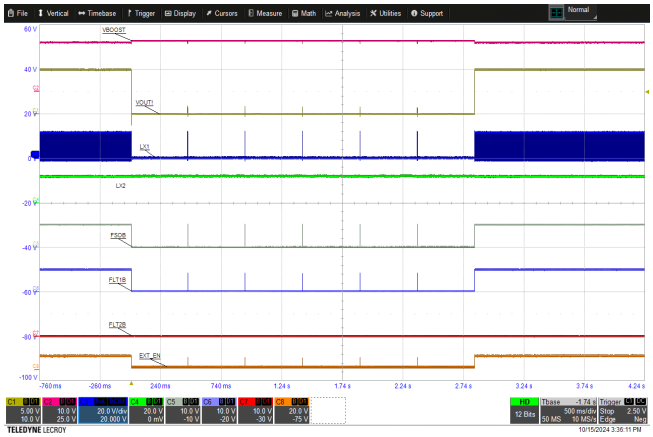


Figure 19. BUCK1 Output Shorted and Short Removed Allowing for Recovery

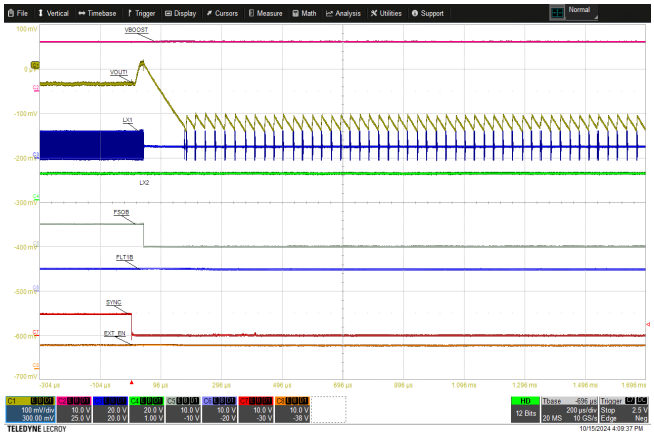


Figure 20. Buck1 ECM Entry with SYNC Driven Low

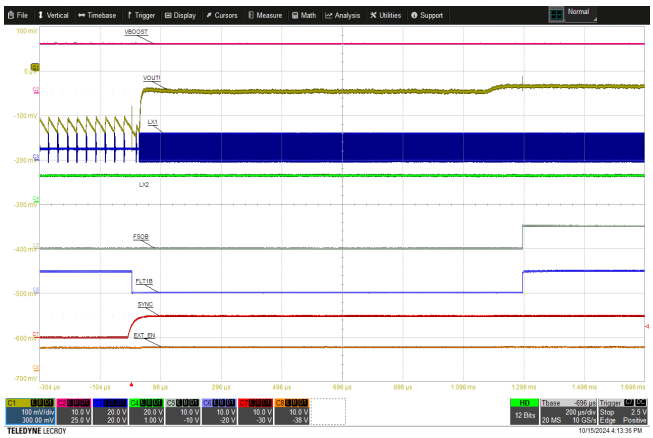


Figure 21. Buck1 ECM Exit with SYNC Driven High

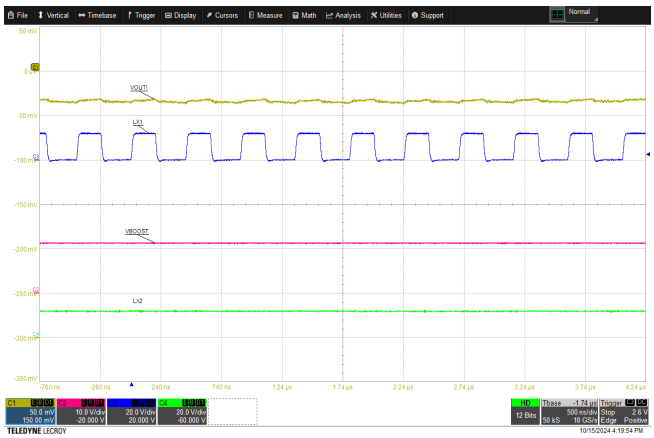


Figure 22. Buck1 FCCM Switching Operation, Buck1 at 75mA Load

5. Functional Description

The RAA271041 contains controllers to support two DC/DC channels, Buck and Boost, which are configurable in various modes and operate across a V_{IN} range of 2.1V to 40V. Buck Channel 1 can be configured as a fixed 3.3V, fixed 5.0V, or as an adjustable output voltage from 0.8V to 12.0V.

Boost Channel 2 is an adjustable output with an output voltage range from 5V to 40V. The RAA271041 can be configured such that the Boost output operates as an input for the Buck, often referred to as Cold Crank configuration (CC mode). Alternatively, the RAA271041 can be configured such that the Buck and Boost channels operate independently (IBB mode).

5.1 Synchronous Buck and Boost

To improve efficiency, the RAA271041 employs both a synchronous buck and synchronous boost architecture. In the synchronous buck, the LS1 output drives the synchronous low-side MOSFET, which replaces the freewheeling diode and improves efficiency. The HS1 signal provides the buck controller PWM information and is complementary to the LS1 signal. HS1 is powered from a boot supply voltage, which is generated using an external diode from VCC to BOOT1 to charge an external capacitor between BOOT1 and LX1 when LS1 is high and LX1 is low.

In the synchronous boost, the operation of the high-side MOSFET(s) and low-side MOSFET(s) are interchanged. The HS2 output drives the synchronous high-side MOSFET, which acts as the blocking/freewheeling diode to improve efficiency. The LS2 signal is complementary to the HS2 signal and provides boost controller PWM information to the low-side MOSFET(s). The HS2 signal is powered from a boot supply voltage (from BOOT2 to LX2), which is generated using an external diode from VCC to BOOT2 to charge an external capacitor between BOOT2 and LX2 when LS2 is high and LX2 is low.

When the Cold Crank configuration is used, the boost channel powers up only when the VBAT voltage drops below a user-programmable threshold, while under normal conditions the boost is not switching.

5.2 Start-Up Operation in Cold Crank Configuration (CC Mode)

For the Cold Crank configuration, the VBAT supply is the input to the Boost channel. Under normal operation, the Boost channel is off, and the Boost output is powered from VBAT using the body diode of the boost high-side MOSFET. If VBAT falls below a user-programmable threshold, the Boost channel turns on and regulates the Boost output to a programmed voltage. In the Cold Crank configuration, the VIN pin of the RAA271041 is connected to the boost output. This arrangement allows the device to be powered from the boost output during Cold Crank events in which the VBAT supply might fall too low to provide sufficient operating voltage. The RAA271041 does not start until the VIN pin exceeds the undervoltage lockout rising threshold of 5.5V typical.

In cold crank applications, Buck Channel 1 is typically enabled first using WAKE1, which might be connected to VBAT or driven by an external signal. This configuration allows the internal LDO regulator to supply V_{CC} bias, enabling the device to begin switching and proceed through the soft-start sequence. The boost controller does not need to switch for the buck controller to power up.

In the typical cold crank application, the WAKE1 and WAKE2 pins are internally joined (OR'd) using factory programming. Boost Channel 2 is typically off when V_{BAT} is at the nominal level of 12V. As V_{BAT} decreases, such as during Cold Cranking, the VBATS pin voltage also decreases. When the VBATS pin falls below 1.0V, the Boost output quickly powers up and maintains the Boost output voltage, which feeds the downstream Buck channel. This allows the Buck output to continue operating, until VBAT drops to the boost turn-off falling threshold of 2.1V (typical). If V_{BAT} rises such that the VBATS pin exceeds the rising edge threshold of 1.07V (typical), the boost channel turns off and the boost output is supplied from VBAT using the body diode of the boost high-side MOSFET.

The FLT2b pin is in an open-drain state when both the boost channel is on, and the boost output voltage is within the programmed range. The FLT2b pin is in a logic low state when the boost channel is off. The boost channel can be off due to either not enabled by a WAKE input or because the VBATS pin is above 1V.

5.3 Start-Up Operation with Individual Buck and Boost (IBB Mode)

For Individual Buck and Boost (IBB) operation, the VIN pin of the device is typically connected to VBAT. The RAA271041 remains off until the VIN pin voltage exceeds the undervoltage lockout rising threshold (5.5V typical). After this condition is met, startup is initiated when either WAKE1 or WAKE2 is set to logic high. This activates the internal VCC regulator which supplies bias power for the device and gate drivers.

Buck Channel 1 operation is controlled by the WAKE1 input. After WAKE1 transitions to logic high, the Buck output goes through a soft-start interval to increase the output voltage to the programmed level. After the buck output reaches regulation, the FLT1b pin remains at logic low for 800µs and then transitions to an open-drain state.

For use in individual boost configuration, the Channel 2 Boost operation is typically controlled by the WAKE2 input only and ignores the VBATS pin. Before the boost is enabled, the output V_{BOOST} is charged to a voltage one diode drop below V_{IN} through the body diode of the high-side MOSFET. After being enabled, the boost channel goes through an initial soft-start interval and ramps the boost output voltage to the programmed level. After the boost output reaches regulation, the FLT2b pin remains at logic low for 800µs and then transitions to an open-drain state.

5.4 WAKE1 and WAKE2 Operation

The WAKE1 pin can withstand up to 42V and can connect to VBAT through a resistor for initial start-up.

The WAKE2 pin is a low voltage (5V) pin and should not be connected to VIN or VBAT. WAKE2 can be enabled using a pull-up resistor to VCC after WAKE1 is high, or connected to an external signal, which does not exceed 5V. For simultaneous start-up of Buck and Boost, the enable pins (WAKE1 and WAKE2) can be resistively pulled to respective logic levels when V_{IN} is applied.

If the WAKE pins are OR'd with either WAKE pin high, the IC continues operation until the VCC voltage decreases below the VCC UVLO falling threshold (4.2V typical), or when VBAT falls below 2.1V (typical).

5.5 VCC Regulator and EXTSUP

The VCC regulator (internal LDO) derives power from the VIN pin and provides VCC 5V bias during startup, which can also be used in continuous operation. In this state, VCC provides bias power for both the IC supply and gate drivers, which can produce high power dissipation in the VCC regulator. To minimize IC dissipation and increase system efficiency, in some applications the EXTSUP pin can supply 5V from an external voltage source. The IC monitors the EXTSUP voltage; if the EXTSUP voltage exceeds 4.5V, the IC connects the EXTSUP pin to the VCC pin and turns off the VCC regulator. This reduces IC power loss and system power loss. If the EXTSUP feature is not used, ground the EXTSUP pin and the VCC regulator powers the IC.

In some applications with VOUT1 set to 5V, VOUT1 can be connected to the EXTSUP pin so that after startup, VOUT1 can supply VCC bias power and eliminate the LDO dissipation in normal operation.

There might be applications where EXTSUP is not used. When the RAA271041 is used in an ASIL system, consult the Safety Application Note (SAN) for application information. During restarts, the internal EXTSUP switch is turned OFF, and this power handover between LDO to EXTSUP pin takes place during each power up. If Channel 1 is not set to 5V, the EXTSUP input can accept 5V from an independent source, such as a small 3.3V to 5V boost converter. If the external bias is applied before VIN is applied, power the enable circuit from the external bias source (and not VIN).

5.6 Oscillator

The buck switching frequency is factory-programmable with options for 440kHz and 2.2MHz. The boost switching frequency is also factory-programmable for either 440kHz or 2.2MHz, however, the boost frequency cannot exceed the Channel 1 buck frequency. External synchronization can be implemented by connecting an external signal source of 440kHz or 2.2MHz (±10%) to the SYNC pin.

5.7 Phase Shift and Spread Spectrum

The Buck Channel 1 and Boost Channel 2 switching are 180° out of phase, which helps lower overall noise by reducing peak currents during switching. The 180° phase shift is between the buck high-side MOSFET on-time and the boost low-side MOSFET on-time.

The Spread Spectrum is derived from an internal triangular 3kHz wave oscillator with a modulation depth of 6% or 12% in a pseudo-random manner. Spread spectrum is configured by factory OTP, which selects spread spectrum ON/OFF and modulation depth, with 5-bit resolution to create 32 discrete frequencies.

5.8 FLTb Signals

The Fault Indicators FLT1b and FLT2b are provided for fault monitoring on the respective buck and boost channels. The pins provide an open-drain output to indicate that the soft-start cycle has completed, and the output voltage is within regulation. An external pull-up resistor is required for each pin, pulled up to VCC or to an external DC supply (5.5V maximum). These pins are pulled low during startup or when the respective output is off.

5.9 EXT_EN Signal

The EXT_EN output is an open-drain indicator that can enable external devices or circuits. The EXT_EN pin can be factory-programmed to monitor Channel 1 only, or Channel 2 only, or both channels. A high (open) state indicates that the selected channel(s) is enabled and is not shut down. During power-up, the EXT_EN pin is low until soft-start is completed and the selected channel(s) are operating in regulation.

5.10 Fail-Safe Output (FSOb)

The RAA271041 provides a Fail-Safe Output (FSOb). The FSOb indicator is an active-high/active-low output that is in the high state when the device is in a trusted state. A number of faults can cause the FSOb to go active-low, indicating that the device has detected a fault.

Note: When the FSOb output is in the active-high state (normal operation), the FSOb pin is connected internally to the VCC supply, typically 5V. Logic devices which connect to FSOb should be able to tolerate 5V signals.

5.11 Fault Protection Overview

The RAA271041 provides multiple fault detection features, including:

- Warning Undervoltage and Overvoltage detection for channels 1 and 2.
- Severe Undervoltage/Overvoltage detection and shutdown for channels 1 and 2.
- Separate internal voltage references for UV/OV detection versus output regulation for channels 1 and 2.
- Separate feedback paths for UV/OV detection versus output regulation for channels 1 and 2.
- FLT1b and FLT2b outputs for indicating faults on channels 1 and 2, respectively.
- Separate internal regulator to provide bias power for functional safety references, circuits, and logic.
- Monitor that compares the output regulation reference to the separate UV/OV reference.
- Redundant logic state machines with separate input skewing to prevent spurious noise corruption.
- Built-In Self Test (BIST) at startup and at ECM exit:
  - UV/OV comparators test
  - Fault Indication stuck-high test (FLT1b, FLT2b, EXT_EN)
  - VCC LDO over-temperature monitor
  - FuSa internal LDO supply over-temperature monitor
  - PGND/SGND connection monitor
  - System and PWM clock monitors
  - VCC UV/OV monitors
  - State machine comparison monitor
  - CRC check on internal registers after initialization

- In addition to BIST at startup, the device provides continual functional safety checking for the following:
  - CRC check of internal registers
  - State machine comparison

When the device is placed in ECM (Energy Conservation Mode, ultra-low power mode), all non-essential circuits are powered off and alternate ultra-low power circuits are activated. During this time, the device is less accurate at detecting faults and as such is not in a trusted state, and the Fail-Safe Output (FSOb) is logic low. When the device exits ECM by setting the SYNC input to logic high, the device immediately begins BIST and rechecks protective functions. After the device has successfully completed BIST, protective functions are re-enabled, the controller exits ECM operation, and the FSOb output transitions to logic high.

5.12 Pin Fault Detection

The device can detect a stuck-high condition on each of the four logic indicators: FSOb, FLT1b, FLT2b, and EXT_EN. A stuck-high fault is a condition in which the device expects a logic low level on the signal pin but detects a logic high level, indicating a fault related to the pin or the external pull-up circuitry.

When a stuck-high pin fault is detected, there is a 500µs delay on fault response. If the pin fault persists longer than 500µs, the device immediately shuts off both Channel 1 Buck and Channel 2 Boost. The outputs then either enter a hiccup/restart cycle or latch off, depending on factory programming.

5.13 Output Voltage Selection

The Channel 1 buck stage operates with an input voltage range of 3.75V to 42V and is offered in fixed output voltage options of 5.0V, 3.3V, or adjustable. In adjustable mode, the Buck output can be set in the range V_{OUT1} = 0.8V to 12V using an external resistive voltage divider from VOUT1 to SGND, with the midpoint connected to FB1.

Note: An identical resistive divider must be used with the midpoint connected to FB1S (OV/UV sense input), to provide robust OV/UV detection if the feedback path to FB1 is interrupted.

Use Equation 1 to derive the R_{UPPER1} and R_{LOWER1} resistor values, where R_{UPPER1} is the resistor between VOUT1 and FB1, and R_{LOWER1} is the resistor between FB1 and GND.

(EQ. 1) $$V_{OUT1} = 0.8V \times (1 + (R_{UPPER1}) / (R_{LOWER1}))$$

The V_{OUT} accuracy is ±1% in normal mode and is ±3% in the Energy Conservation Mode (ECM), which is a low power mode. Error amplifier compensation is achieved by connecting a Type 2 RsCs + Cp network to COMP1.

5.14 Bootstrap for High-side NMOS Drive

To provide high-side gate voltage, the RAA271041 employs a bootstrap circuit using an external boot capacitor (C_{BOOT1}) and external diode. The capacitor charges from the VCC supply when the buck low-side MOSFET is on.

5.14.1 Boot Refresh for Buck Channel in ECM

If the Buck channel is in Pulse Skip mode or in ECM mode, the long time between LX1 pulses can result in the BOOT1 voltage falling. The BOOT1 to LX1 voltage is constantly monitored and if it falls lower than 3.4V (typical), the device inserts a 180ns (or optional 360ns) pulse to the Buck low-side gate, which recharges the BOOT1 capacitor.

5.14.2 Current Limit and Overcurrent Protection

For Buck Channel 1, an external current sense resistor and internal current sense amplifier provide overcurrent protection. The current sense resistor is in series with the inductor, with a resistance value selected to provide 50mV at full load. Inductor DCR current sensing can also be used. If the load increases such that the voltage across the current sense resistor rises to 80mV (OC1 threshold), the PWM controller terminates the high-side pulse, on a cycle-by-cycle basis. If the load continues to increase and the current sense resistor signal reaches

100mV (OC2 threshold), the OC2 protection limit is reached; switching operation ceases and the output is shut down and either enters a hiccup/restart cycle or latches off.

5.14.3 Undervoltage and Overvoltage (UV and OV) Protection

The RAA271041 channels 1 and 2 have factory-programmable options for the following:

- Warning overvoltage at +6%, +8%, and +12%,
- Warning undervoltage options of -5%, -8%, and -12%.
- Severe overvoltage at +12% and +15%
- Severe undervoltage at -12% and -15%.
- Channel 1 and Channel 2 provide separate selections for Warning UV, Warning OV, Severe UV, and Severe OV.

A Warning UV or OV detection causes the corresponding FLT1b or FLT2b indicator to pull low. However, the output continues switching. If the output voltage returns to normal, the FLT1b or FLT2b pin also returns to its high (open drain) state.

A Severe UV or OV detection causes the output to shut down, and the corresponding FLT1b or FLT2b pin also drives low (if not already low due to Warning UV or OV).

Note: All UV and OV conditions are detected at the FB1S and FB2S pins, not the FB1 or FB2 pins, which are used to regulate the outputs. The separate paths for OV/UV detection versus feedback regulation protect against single-point failures in the output feedback path.

5.14.4 Boost Input Overvoltage (VBAT OV)

The RAA271041 detects overvoltage at the VBAT input. When the VBAT voltage reaches 44V, the device detects an input OV condition and immediately shuts down both channels. *Note*: The input OV condition is sensed at the VIN pin for Cold Crank options (see Current Limit and Overcurrent Protection). For Individual Buck/Boost applications, (Current Limit and Overcurrent Protection) the input OV condition is sensed at the VBATS pin.

5.15 Boost Channel 2

5.15.1 Boost Operating Range

The synchronous boost stage operates across a V_{BAT} input voltage range of 2.1V to 42V and has an adjustable V_{BOOST} output voltage range of 5V to 40V. The V_{BOOST} output voltage is set using two resistor dividers: one divider connects to the FB2 pin, and a second identical divider connects to the FB2S pin. For most applications, the purpose of the boost channel is to maintain an input supply for the Buck channel during low-battery events such as cold cranking, allowing the Buck channel to continue normal operation.

5.15.2 Boost Operation Options

The boost channel is factory-programmed to operate in one of four options:

- Option 0 (Cold Crank 0) – This option is for applications where the boost channel runs directly from the battery input, and the buck channel runs directly from the boost output. The boost output powers the buck input but does not power any other external loads.

  Under normal VBAT conditions, the boost channel is off and the VBAT voltage passes directly to the boost output through the body diode of the boost high-side MOSFET. When the VBAT input decreases to a user-programmable threshold, set by the VBATS pin threshold of 1.0V, the boost channel quickly powers up and brings the boost output up to the programmed voltage. The boost channel remains on until the VBATS pin voltage rises above the VBATS rising threshold of 1.03V, at which point the boost channel turns off.

  Note: The boost output voltage might be below the programmed voltage setting, caused by VBAT being below normal levels but not low enough to reach the VBATS falling threshold. In this condition, the boost channel is still off, and the boost output decreases as the VBAT input decreases.

  In this operation option, the boost output undervoltage and overvoltage fault detections are disabled. Undervoltage detection is disabled because the boost output might be lower than normal while the VBAT input

is below the user-programmed boost output voltage yet is not low enough to turn on the boost channel using the VBATS pin. Overvoltage detection is also disabled because the VBAT input might be much higher than normal during a Load Dump event, which can force the V_{BOOST} output voltage far above the user-programmed boost output voltage.

- Option 1 (Cold Crank 1) – This option is like Cold Crank 0, however in this case, the boost output feeds both the buck channel input and an external load. The overall operation is the same as Cold Crank 0.
- Option 2 (Individual Buck/Boost 0) – This option allows for separate operation of the Boost and Buck channels. In this mode, the Boost channel operates as controlled by the WAKE2 pin (or using OR'd WAKE pins) and ignores the VBATS pin. This mode is intended for applications in which the Boost channel must also tolerate Load Dump (high VBAT) events. During a Load Dump event it is possible for the Boost output voltage to exceed the normal regulation voltage, therefore the OV fault detection is disabled. However, the UV fault detection and response is enabled and is active whenever the Boost is on (using WAKE input).
- Option 3 (Individual Buck/Boost 1) – This option allows for the separate operation of the Boost and Buck channels when powered from regulated power input. In this mode, the Boost channel operates as controlled by the WAKE2 pin (or using OR'd WAKE pins) and ignores the VBATS pin. This mode is intended for applications in which the Boost channel does not need to tolerate Load Dump (high VBAT) events, and therefore the Boost channel has enabled fault detection and response for Warning UV/OV and for Severe UV/OV conditions.

The system architecture assumptions for each Boost operating option are listed in Table 1.

Table 1. System Architecture Assumptions

Option	Name	System Architecture
0	Cold Crank 0 CC_0	The Boost channel is active (switching) only when VBAT drops during Cold Crank, to ensure that Buck operation continues. System requires tolerance of Load Dump and Cold Crank. Boost OV faults are ignored due to possible Load Dump event causing V_{BOOST} to exceed normal levels. Boost UV faults are ignored due to possible low VBAT causing V_{BOOST} to fall below normal levels. If VBAT falls low enough to force the VBATS pin to 1V, the boost turns on and supports the Buck input. VBAT feeds the boost input. The boost output powers only the buck input, no other loads on boost.
1	Cold Crank 1 CC_1	The Boost channel is active (switching) only when VBAT drops during Cold Crank, to ensure that Buck operation continues. System requires tolerance of Load Dump and Cold Crank. Boost OV faults are ignored due to possible Load Dump event causing V_{BOOST} to exceed normal levels. Boost UV faults are ignored due to possible low VBAT causing V_{BOOST} to fall below normal levels. If VBAT falls low enough to force the VBATS pin to 1V, the boost turns on and supports the Buck input. VBAT feeds the boost input. The boost output powers the buck input and/or other external loads.
2	Individual Buck/Boost 0 IBB_0	System might require that the boost channel is always on. System requires tolerance of Load Dump and Cold Crank. Boost OV faults are ignored due to possible Load Dump event causing V_{BOOST} to exceed normal levels. Boost UV fault response is enabled when the boost is active. VBAT feeds the boost input. The buck channel can be powered from the boost output, or from VBAT, or from a separate input supply.
3	Individual Buck/Boost 1 IBB_1	System might require that the boost channel is always on. System does not require tolerance of Load Dump and Cold Crank (VBAT supply is pre-regulated). Boost OV fault response is enabled when the boost is active. Boost UV fault response is enabled when the boost is active. VBAT feeds the boost input. The buck channel can be powered from the boost output, or from VBAT, or from a separate input supply.

The device response for each of the operating options is shown in Table 2.

Table 2. Device Response versus Boost Operating Option

Option Number	Option Name	Cold Crank Tolerant	Load Dump Tolerant	Boost Enable	Boost Output OV Faults	Boost Output UV Faults	Boost Input OV Fault (VBAT OV)
0	Cold Crank 0 CC_0	Yes	Yes	Wake = High and VBATS ≤ 1V	No response	No response	Response enabled sensed at VIN pin
1	Cold Crank 1 CC_1	Yes	Yes	Wake = High and VBATS ≤ 1V	No response	No response	Response enabled sensed at VIN pin
2	Individual Buck/Boost 0 IBB_0	Yes	Yes	Wake = High VBATS ignored	No response	Response enabled when boost is active	Response enabled sensed at VBATS pin
3	Individual Buck/Boost 1 IBB_1	Yes	No	Wake = High VBATS ignored	Response enabled when boost is active	Response enabled when boost is active	Response enabled sensed at VBATS pin

5.15.3 Boost Output Voltage Programming

To program the Boost output voltage, connect a resistor divider from V_{BOOST} to the TERM pin, with the midpoint connected to the FB2 pin. Use Equation 2 to calculate the required resistor values, where R_1 is the resistor between VOUT2 and FB2, and R_2 is the resistor between FB2 and TERM.

(EQ. 2) $$V_{OUT} = 0.8V \times \left(1 + \frac{R_1}{R_2}\right)$$

Note: Place an identical resistor divider from V_{BOOST} to the TERM pin, with the midpoint connected to the FB2s pin.

When designing the PCB, include a GND guard band around the feedback resistor networks to reduce noise and improve accuracy and stability. Place resistors R_1 and R_2 close to the FB pin.

5.15.4 Current Limit and Overcurrent Protection (OC1 and OC2)

For the Boost channel, an external current sense resistor provides overcurrent protection. The current sense resistor is in series with the V_{BAT} input, with a resistance value that produces a 50mV signal between ISEN2P and ISEN2N when the full load current is applied to the output in CCM. Inductor DCR current sensing can also be used. If the load increases such that the voltage across the current sense resistor reaches 80mV, the PWM circuit begins limiting current on a cycle-by-cycle basis (OC1). If the load continues to increase and the current sense resistor signal reaches 100mV, the OC2 protection limit is reached and the output shuts down, and then enters a hiccup/restart cycle or latches off, based on factory programming.

Note: If the boost output falls below VBAT, current is free to flow from VBAT to the boost output through the high-side MOSFET body diode, even if the MOSFETs are not switching.

Also, the current sensing is done at the boost input. The input current of a boost channel is inversely proportional to the input voltage. When selecting the sense resistor value, the lowest expected operating input voltage (V_{BAT}) gives the highest expected input current and use this value to select the resistor value.

The RAA271041 boost Channel 2 also has reverse (negative) current limiting at -40mV typical.

5.15.5 Boost Turn-On Threshold in Cold Crank (VBATS Threshold)

For Cold Crank applications, the Boost channel is typically not switching until the VBAT input decreases (such as during a Cold Crank event), at which point the Boost channel turns on to provide a regulated input to the downstream Buck channel. The RAA271041 provides a VBATS pin (Pin 34) which allows the user to program the VBAT voltage at which the Boost channel turns on. To program the VBAT voltage which enables the Boost channel, connect a voltage divider from VBAT to the TERM pin (Pin 33), with the midpoint connected to VBATS (pin 34). When the VBATS pin falls below 1.0V, the boost turns on and brings the V_{BOOST} output voltage to the programmed voltage, allowing the Buck channel to continue operation.

To prevent the VBATS input from triggering on switching noise, Renesas recommends placing a 220pF capacitor connected from VBATS to GND.

5.15.6 Over-Temperature Shutdown

The RAA271041 has an over-temperature shutdown threshold of 160°C with 15°C hysteresis. When crossing the threshold, the device shuts down for 100ms and then attempts to restart the device. The device resumes operation when the over-temperature fault is cleared.

5.16 SYNC Pin

The SYNC pin allows users to select Channel to operate in Continuous Conduction Mode (CCM) switching, Diode Emulation Mode (DEM) switching, or Energy Conservation Mode (ECM) switching. ECM is available only for Buck Channel 1 and provides extremely low power consumption at light loads. Entry and exit into ECM mode is enabled by the SYNC pin (Pin 36).

With the SYNC pin set to logic high, Buck and Boost operation is always CCM, regardless of load on either output.

When the SYNC pin is driven to logic low, the Buck regulator, depending on load, operates in one of three modes:

- For loads where the voltage across the Buck RSNS resistor is 10mV or greater, the device continues to operate in FCCM. In FCCM operation, both high-side and low-side MOSFETs are switched on and off on every switching cycle.
- For loads where the voltage across the Buck RSNS resistor is between 2mV and 10mV at the moment when SYNC is set to GND, the device operates in DEM. DEM uses variable frequency to reduce switching losses and improve light-load efficiency, but unlike ECM operation protective functions are still active.
- For loads where the voltage across the Buck RSNS resistor is 2mV or less, the device enters ECM operation. *Note*: When the device enters ECM, the controller can remain in ECM operation even if the load increases and Buck RSNS voltage increases to 10mV. To enter ECM operation, the voltage on the VIN pin (Pin 29) must be in the range from 6V to 18.5V and the SYNC pin must be logic low. *Note*: In ECM operation, the device operates in an extremely low power state, which does not provide full FuSa support.

The RAA271041 can be configured to allow the Buck Controller to enter ECM to reduce power consumption. ECM allows the buck channel to provide a 5V output (with no load) while the device draws typically 8µA from the VCC supply. During ECM operation, the RAA271041 buck channel delivers power pulses to the output filter and loads at a frequency much lower than the normal switching frequency. Each power pulse supplies sufficient energy to supply small load currents with no requirement for a high-frequency multi-pulse burst operation. In the time interval between consecutive ECM power pulses, the RAA271041 drastically reduces its current consumption to minimize average standby current drawn from the input supply.

To enter ECM operation, the voltage on VIN (Pin 26) must be in a range from 6V to 18.5V and the SYNC pin must be logic low. If SYNC is directly connected to VCC, the circuit always operates in CCM. SYNC can be held low to command ECM operation when the load is small, and then SYNC can be driven high before a larger load is supplied, to force mode change to CCM and support the higher load. Alternatively, beginning with SYNC low at light load, SYNC can be driven by an external clock for synchronized operation, which forces ECM exit and CCM operation.

Note: During ECM operation, the device disables many FuSa functions to achieve an extremely low power state. Therefore, the Fail-Safe Output (FSOb) is driven low during ECM operation. When the device exits ECM operation, the Functional Safety BIST is performed. After all BIST functions are verified, the FSOb is driven high.

Also, the Boost controller must be off when Controller 1 is in ECM operation. If the boost controller is active using WAKE2, the buck controller does not enter EVM operation. If the buck controller is in ECM operation, the boost channel remains off until the Buck controlled exits ECM from either a large load increase or the SYNC pin driven high to force ECM exit.

Note: This also means that if Buck is operating in ECM, the boost channel does not automatically turn on even if the VBATS voltage falls below 1V. This is because in ECM, most fault detection functions including the VBATS detection are disabled, to reduce operating current to an ultra-low state.

Note: There is no ECM operation available for the Boost Channel 2.

5.16.1 Overview of ECM Setup and Operation

If Channel 1 (buck) is configured to allow ECM at light loads, the channel enters ECM operation if the following conditions are present:

- SYNC pin is set to logic low.
- VIN is between 6V to 18.5V.
- Buck load causes the voltage across the Buck RSEN resistor to be less than 2mV.
- Boost Channel 2 is off. For Cold Crank applications, the boost is typically off when the input voltage is at normal levels (VBATS pin is above 1V).

During ECM operation, the buck channel uses a voltage comparator in conjunction with an accurate current sense resistor and amplifier to detect load current. In between switching pulses, most of the device is off or in a very low-power state, resulting in extremely low operating current, and the load is supplied by the output capacitors. The output falls until the comparator detects the lower voltage threshold, at which point the IC energizes enough circuitry to generate a power pulse, which replenishes the output capacitors. Each ECM power pulse is terminated by one of two methods:

- Inductor current reaching the ECM peak current threshold.
- Output voltage reaching the overvoltage threshold.

Individual ECM power pulses are generated by the following procedure. First, the high-side MOSFET is turned ON (HS1 signal drives high) to apply V_{BOOST} (for Cold Crank) or V_{IN} (for IBB operation) to the output inductor. The inductor current ramps up from zero at a rate determined by the inductance and voltage from LX1 to VOUT1.

The current sense amplifier monitors the voltage level across the current sense resistor until the voltage reaches 13mV. When the 13mV threshold is attained, the high-side MOSFET is turned off and the low-side MOSFET is turned on. This forces the inductor current to ramp down to approximately 0A at which time an internal zero current comparator turns the low-side MOSFET off. After the low-side MOSFET is turned off, the IC returns to ultra-low quiescent current consumption.

Alternatively, if the output rises to approximately 3% of V_{OUT} before the peak current is detected, the high-side pulse is terminated followed by the low-side MOSFET turning on.

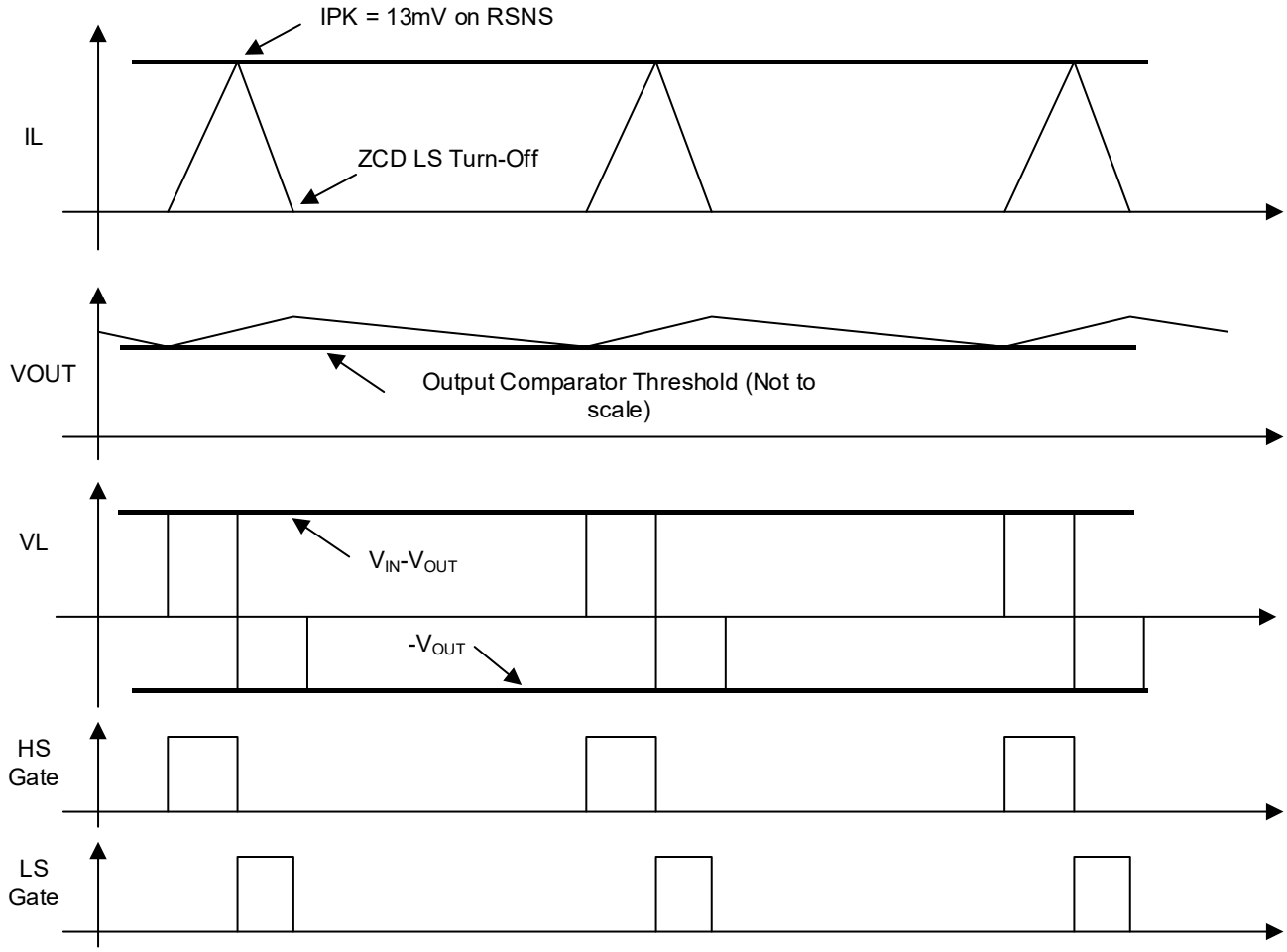


Figure 23. Energy Conservation Mode (ECM) Operational Waveforms

5.16.2 ECM Entry and Exit

The current sense resistor and amplifier set thresholds that allow ECM entry and control power pulse generation. To understand ECM power pulse operation, the current sense resistor (in series with the power inductor) is selected to produce a 50mV signal between ISEN1P and ISEN1N when the full load current is applied to the output. If ECM is allowed (SYNC = GND) and the load reduces to a level at which the signal across the current sense resistor is 2mV (typical), the circuit enters ECM. The circuit remains in ECM as the load is further reduced to minimal or no load.

If the load increases, the circuit remains in ECM operation, but it cannot support load currents in which the RSNS signal exceeds approximately 6.5mV.

6. Application Information

Several factors should be considered when selecting components for buck and boost regulators. This section discusses some examples of how to decide the parameters of the external components based on the typical application schematic shown in Figure 2. In the actual application, the parameters might need to be adjusted and also a few more additional components might need to be added for the application-specific noise, physical sizes, thermal, testing, and other requirements.

6.1 Buck Channel Components

6.1.1 Buck Inductor Selection

While the buck channel is operating in a stable Continuous Conduction Mode (CCM), the output voltage and on-time of the high-side transistor is determined by Equation 3, where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the on-duty of the high-side transistor.

(EQ. 3) $$V_{OUT} = V_{IN} \times \frac{t_{ON}}{T} = V_{IN} D$$

Under this CCM condition, the inductor ripple current can be defined as Equation 4:

(EQ. 4) $$I_{L,p\text{-}p} = t_{ON} \times \frac{V_{IN} - V_{OUT}}{L} = t_{OFF} \times \frac{V_{OUT}}{L}$$

From the previous equations, use Equation 5 to determine the inductor value.

(EQ. 5) $$L = \frac{V_{IN} - V_{OUT}}{f_{SW}} \times \frac{V_{OUT}}{V_{IN}}$$

In general, when the inductor value is determined, the ripple current varies by the input voltage. At the maximum input voltage, the on-duty becomes the minimum and the ripple current becomes the maximum. Therefore, use Equation 6 to estimate the minimum inductor value.

(EQ. 6) $$L_{min} = \frac{V_{IN} - V_{OUT}}{f_{SW} \times \Delta I_{L,\,max}} \times \frac{V_{OUT}}{V_{IN,\,max}}$$

In a Buck regulator, this ripple current is normally selected to be between 20% and 50% of the maximum DC output current. A typical starting point is to set the ripple current to 30% of the maximum DC output current. Larger inductor values reduce the ripple current and ripple voltage. However, larger inductor values can slow the response time of the channel to load transients. Also, the larger inductance reduces the RSNS current ramp signal and can result in noise sensitivity.

Under stable operation, the peak current flow in the inductor is the sum of output current and 1/2 of ripple current.

(EQ. 7) $$I_{L,pk} = \frac{I_{L,p\text{-}p}}{2} + I_{OUT}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the startup or heavy load transient. Therefore, the size of the inductor should be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the saturation current rating of the inductor.

Note: The OC1 signal is fixed at 80mV (1.6x of full load) and the OC2 hiccup threshold is fixed at 100mV (2x of full load); therefore, the inductor should have a saturation value exceeding 2x full load current.

ECM operation is based on a fixed peak signal of 13mV, which is well below the OC1 level, therefore, there are no special considerations for inductor selection for ECM.

6.1.2 Buck Output Capacitor

To filter the inductor current ripples and to have sufficient transient response, output capacitors are required. The current mode control loop allows the usage of low ESR ceramic capacitors for smallest size, and/or electrolytic and polymer capacitors that offer larger capacitance values but with higher ESR and increased physical size. While the ceramic capacitor offers excellent overall performance and reliability, the actual capacitance can be

reduced considerably when operated with significant DC bias voltage. Carefully review the capacitor manufacturer's information when selecting output capacitors.

The following are equations for the required capacitance value to meet the required ripple voltage level. Additional capacitance can lower the ripple voltage and to improve transient response.

For the ceramic capacitor (low ESR):

(EQ. 8) $$V_{OUT,rip} = \frac{\Delta I_L}{8 \times f_{SW} \times C_{OUT}}$$

where ΔI_L is the inductor's peak-to-peak ripple current, f_{SW} is the switching frequency and C_{OUT} is the output capacitor.

Required minimum output capacitance based on ripple current is:

(EQ. 9) $$C_{OUT,min} = \frac{\Delta I_L}{8 \times f_{SW} \times V_{OUT,rip}}$$

If using electrolytic capacitors, the ESR is the dominant portion of the ripple voltage.

(EQ. 10) $$V_{OUT,rip,ESR} = \Delta I_L \times ESR$$

Therefore, to reduce the ripple voltage, select the electrolytic capacitor based on maximum ESR, use multiple capacitors in parallel to reduce the ESR, or increase inductor value to reduce the ripple current.

The output capacitor value selected for CCM might require adjustment for ECM operation depending on the magnitude of ripple voltage allowed on VOUT. In standard ECM operation when there is no external loading, the output capacitor must absorb the complete pulse of energy from the output inductor peak current of 120% of full load current. Both the capacitance value and ESR should be considered for ECM operation. The capacitance should be large enough to absorb the energy with acceptable voltage rise and the ESR must be small enough to control the potentially large step in voltage equal to Ipk, ECM × ESR.

In addition to output voltage ripple requirements, select the buck output capacitor value in conjunction with the inductor to meet output deviation requirements during normal CCM operation, ECM, and load transients.

Equation 11 calculates the value of C_{OUT} required during load reduction and the output voltage overshoots the nominal level.

(EQ. 11) $$C_{OUT\_MIN\_STEP\_DOWN} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2V_{OUT}\Delta V}$$

When the load is increased, the output undershoots the nominal value and the value of C_{OUT} required is calculated using Equation 12.

(EQ. 12) $$C_{OUT\_MIN\_STEP\_UP} = \frac{L\left(I_{STEP} + \frac{I_{RIPPLE}}{2}\right)^2}{2(V_{IN} - V_{OUT})\Delta V}$$

6.1.3 Buck Input Capacitor

The Buck input power rail can incorporate a combination of electrolytic and ceramic capacitors to provide a stable input voltage while supplying pulse currents at the buck switching frequency. The voltage rating of the capacitors should exceed the maximum input voltage, a 20% margin is typically a good starting point.

The minimum value of the Buck input capacitors can be estimated by limiting the drop in VIN (ΔV_{IN} below) to approximately 1% when delivering the full load current during the on-time of the high-side MOSFET:

(EQ. 13) $$C_{IN,MIN} = \frac{I_{LOAD,MAX} \times D \times (1 - D)}{f_{SW} \times \Delta VIN}$$

The specific capacitor(s) used should be selected with an RMS current capability exceeding the value estimated by the relation shown in Equation 14.

(EQ. 14) $$I_{CIN,RMS} \cong I_{LOAD,MAX} \times \sqrt{D \times (1 - D)}$$

6.1.4 Buck MOSFET Selection

The external MOSFETs that are driven by the RAA271041 controller need to be carefully selected to optimize the design of the synchronous buck regulator. The input voltage is typically the automotive range for battery supply, so the MOSFETs are normally rated at 40V BVdss. As the high-side and low-side gate drivers are a 5V output, the MOSFET VGS needs to be specified in this range. The MOSFET should have a low total gate charge (Qgd) and low specified ON-resistance ($r_{DS(ON)}$) at VGS = 4.5V or 5V. Renesas recommends ensuring the minimum VGS threshold is higher than 1.2V, but not exceeding 2.5V to ensure the MOSFETs can be switched off reliably throughout the complete V_{CC} range.

6.1.5 Control Loop Compensation Components for the Buck Channel

Several components selected for the power, filtering, and current sense circuits play a role in the determination of the compensating components.

- R_{SENSE} = 50mV/I_{OUT} = 5mΩ (with I_{OUT} = 10A)
- Ramp slope = 38.1mV per volt of V_{IN}
- Ramp valley = 1V
- Current sense amplifier transconductance = $G_{m,CSA}$ = 91.25µS
- Current feedback resistor value = R_{IFB} = 60kΩ
- Reference voltage V_{REF} = 0.8V
- G_{mea} = 1.7mS

Use Equation 15 to calculate the current loop pole frequency

(EQ. 15) $$f_{cp} = \frac{R_{sns}}{2\pi \times L_{OUT}}$$

Use Equation 16 to determine PWM_{gain}

(EQ. 16) $$PWM_{gain} = \frac{1}{\text{ramp slope}} = \frac{1}{38.1mV} = 26.2$$

Use Equation 17 to calculate current loop unity gain frequency

(EQ. 17) $$f_{tc} = PWM_{gain} \times g_{csa} \times R_{ifb} \times f_{cp}$$

Use Equation 18 to calculate the command voltage (+1V for ramp valley voltage) for the specific conditions.

(EQ. 18) $$V_{cmd} = R_{sns} \times I_{max} \times g_{csa} \times R_{ifb}$$

Use Equation 19 to determine the equivalent transconductance of the modulator (I_{OUT}/V_{cmd}).

(EQ. 19) $$GM = \frac{1}{R_{sns} \times g_{csa} \times R_{ifb}}$$

Use Equation 20 to calculate the unity gain frequency of the modulator.

(EQ. 20) $$f_{tm} = \frac{GM}{2\pi \times C_{OUT}}$$

Constrain the voltage loop f_t to be less than current loop f_{tc}.

(EQ. 21) $$\frac{f_t}{f_{tc}} = 0.5$$

Use Equation 22 to calculate the compensation resistor R_{COMP}.

(EQ. 22) $$R_{COMP} = \frac{f_{tc} \times V_{OUT} \times 0.5}{f_{tm} \times g_{m,ea} \times V_{REF}}$$

Use Equation 23 to calculate compensation capacitor C_{COMP}.

(EQ. 23) $$C_{COMP} = \frac{15}{2\pi \times R_{COMP} \times f_{tc}}$$

6.2 Boost Channel Components

6.2.1 Bootstrap Resistor Circuit

In an application board, it is common to have ringing noise when the LX and BOOT nodes swing with high dv/dt. This is a result of parasitic inductance and capacitance in the LX node and Boot capacitor routing on the printed circuit board and in the MOSFET structure. The generated noise can disrupt portions of the control circuit analog sense lines and might require some suppression. A simple method to reduce the noise involves placing a resistor of small value (typically from 1Ω to 10Ω) between the BOOT pin and the junction of the boot diode and boot capacitor. This slows down the high-side MOSFET turn-on to reduce the dv/dt of the LX rising edge.

6.2.2 Boost Inductor Selection

While the boost channel is operating in stable Continuous Conduction Mode (CCM), the output voltage and the low-side transistor on-time is determined by Equation 24, where T is the switching cycle ($1/f_{SW}$) and $D = t_{ON}/T$ is the high-side on-duty of the transistor.

(EQ. 24) $$V_{OUT} = \frac{V_{IN}}{1 - \frac{t_{ON}}{T}} = \frac{V_{IN}}{1 - D}$$

Under this CCM condition, the inductor ripple current can be defined using Equation 25.

(EQ. 25) $$I_{L,p\text{-}p} = D \times T \times \frac{V_{IN}}{L}$$

The previous equations can be rearranged to determine the inductor value using Equation 26.

(EQ. 26) $$L = \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \times \left(\frac{V_{IN}}{I_{L,p\text{-}p} \times f_{SW}}\right)$$

In all the previous equations, the Boost minimum input voltage must be considered. *Note*: If a boost regulator is maintaining a fixed output voltage and a fixed load current, the Boost output power is constant. The boost input power must also remain relatively constant. Due to this constraint, as the input voltage falls, the boost input current must rise to maintain constant power. Therefore, the boost input current is maximum at the lowest input

voltage and the maximum boost load. This relationship can significantly affect the selection of both the inductor and the power MOSFETs.

Therefore, as the boost input voltage falls, the inductor and MOSFET current-handling capacity must increase proportionally. Renesas recommends setting the minimum input voltage as high as possible in accordance with the input voltage requirements to minimize the size and cost of the inductor and MOSFETs.

In a Boost regulator, the inductor ripple current is normally selected to be between 20% and 50% of the maximum DC output current. A typical starting point is to set the ripple current to 30% of the maximum DC output current. Larger inductor values reduce the ripple current and ripple voltage. However, larger inductor values can slow the response time of the channel to load transients. Also, the larger inductance reduces the RSNS current ramp signal and can result in noise sensitivity.

Under stable operation, the peak current flow in the inductor is the sum of maximum input current (full load and minimum V_{IN}) and 1/2 of ripple current.

(EQ. 27) $$I_{L,pk} = \frac{I_{L,p\text{-}p}}{2} + I_{IN}$$

This peak current at maximum load condition must be lower than the saturation current rating of the inductor with enough margin. In the actual design, the largest peak current can be observed at the startup, heavy load transient, and minimum input voltage. Therefore, the inductor's size must be determined with the consideration of these conditions. Also, to avoid exceeding the saturation rating of the inductor, Renesas recommends setting the OCP trip point between the maximum peak current and the inductor's saturation current rating.

Note: The OC1 signal is fixed at 80mV (160% of full load) and the OC2 hiccup threshold is fixed at 100mV; therefore, the inductor should have a saturation value exceeding 2x full load current.

6.2.3 Boost Output Capacitor

Output capacitors are required to filter the inductor current ripple and to provide energy storage to support transient load conditions, and a combination of electrolytic and ceramic capacitors is normally used. The ceramic capacitors filter the high-frequency spikes of the main switching devices and absorb the highest frequency components of the trapezoidal output current flowing through the output rectifier of a boost channel. In layout, place these output ceramic capacitors as close as possible to the main switching devices to maintain the smallest switching loop. To maintain capacitance over the biased voltage and temperature range, Renesas recommends using high-quality capacitors such as X7R or X5R. The electrolytic capacitors handle the load transient and output ripples.

Use Equation 28 to estimate the minimum output capacitor.

(EQ. 28) $$C_{OUT,min} = \frac{100 \times I_{OUT} \times T_{ON}}{V_{OUT}}$$

The boost output ripple at the switching frequency is mainly determined by the trapezoidal rectifier current and output capacitance value. For the boost channel, the maximum output voltage ripple can be estimated using Equation 29, where $I_{OUT,max}$ is the load current at output, C is the total capacitance at output, and D_{MIN} is the minimum duty cycle at $V_{IN,max}$ and $V_{OUT,min}$.

(EQ. 29) $$V_{OUT,rip} = \frac{I_{OUT,max} \times (1 - D_{MIN})}{8C \times 2 \times f_{SW}}$$

6.2.4 Control Loop Compensation Components for the Boost Channel

- R_{SENSE} = 3mΩ
- Ramp amplitude = V_{ramp} = 0.8V
- Current sense amplifier transconductance = $G_{m,CSA}$ = 91.25µS
- Current feedback resistor value = R_{IFB} = 144kΩ

- Selected C_{OUT} = result calculated in Equation 28
- Reference voltage V_{REF} = 0.8V
- G_{mea} = 1.7mS

Use Equation 30 to calculate the current loop pole frequency.

(EQ. 30) $$f_p = \frac{R_s}{2\pi L}$$

Use Equation 31 to calculate modulator gain.

(EQ. 31) $$A_m = \frac{V_{OUT}}{V_{RAMP}}$$

Use Equation 32 to determine the unity gain frequency of the current loop.

(EQ. 32) $$f_{tc} = A_m \times g_{m\_csa} \times R_{ifb} \times f_p$$

Use Equation 33 to calculate the command signal that provides I_{OUT}.

(EQ. 33) $$V_{cmd} = I_{IN} \times R_s \times g_{m\_csa} \times R_{ifb}$$

Use Equation 34 to determine the transconductance of the closed-loop current gain block.

(EQ. 34) $$GM = \frac{I_{OUT}}{V_{cmd}}$$

Incorporating selected output capacitance, use Equation 35 to calculate the unity gain frequency of the closed current loop.

(EQ. 35) $$f_{cc} = \frac{GM}{2\pi C_{OUT}}$$

Use Equation 36 to calculate the right half-plane zero frequency.

(EQ. 36) $$f_{rhpz} = \frac{V_{IN}^2}{2\pi L P_{OUT}}$$

Select a unity gain frequency less half of the right half-plane zero frequency.

(EQ. 37) $$f_t \leq 0.5 f_{rhpz}$$

Use Equation 38 to calculate the compensation resistor.

(EQ. 38) $$R_{COMP} = \frac{f_{tc} V_{OUT}}{V_{REF} \times g_{m\_csa} \times f_{cc}}$$

Use Equation 39 to calculate the unity gain frequency of the voltage loop.

(EQ. 39) $$f_t = \frac{g_{m\_ea} R_{COMP}}{V_{OUT} f_{cc}}$$

The compensation capacitor can be calculated using Equation 40.

(EQ. 40) $$C_{COMP} = \frac{5}{2\pi R_{COMP} f_t}$$

6.3 Recommended PCB Layout

TO BE UPDATED: Correct PCB layout is critical for proper operation of the RAA271041. Each channel requires specific attention to minimize the power loop area for highly efficient, stable operation. It is also important to consider routing the shared common areas between the two channels. Route the primary paths in a single layer copper if possible to reduce parasitic inductance in the power current paths.

The following layout instructions see Figure 24 and Figure 25 as noted.

- In Figure 24, connect the common connection between input capacitors, output capacitors, and the low-side FET for each channel through the central ground (gray) area.
- When the high-side MOSFET is switched ON and OFF the power current alternates flowing through the input capacitor and high-side MOSFET, or the low-side MOSFET. Minimize the loop area between CIN, high-side MOSFET, and low-side MOSFET to reduce interference from the high di/dt intervals as the current alternates between the MOSFETs.
- The first inner layer below the top copper layer with power components should be a ground layer that is as complete as possible, as indicated in Figure 25 using the light green fill. This provides a tightly coupled ground return path for the power circuitry. This layer is also used in conjunction with many vias to create a low-impedance connection from the common power GND region to the RAA271041 controller, and the thermal pad is connected to this plane using multiple vias.
- Connect the signal ground (Pin 14) to the thermal pad ground directly under the IC. For best noise immunity, signal pins such as COMP, RT, and configuration resistors can be connected in a small SGND pour that connects to Pin 14, which connects to PGND in a single point connection under the IC.
- Each channel has ISNS connections that should be routed as shown in Figure 25. The ISNS traces are routed on the second inner layer, which is shielded from power switching currents by the ground area on the inner layer 1. Begin the ISNS traces as a kelvin connection through a via in the center of the sense resistor in each channel.
- Minimize the trace lengths on the feedback loop and route around switching power circuits to minimize noise pick-up.
- Place the capacitors on VIN and VCC close to respective pins and ground connection.

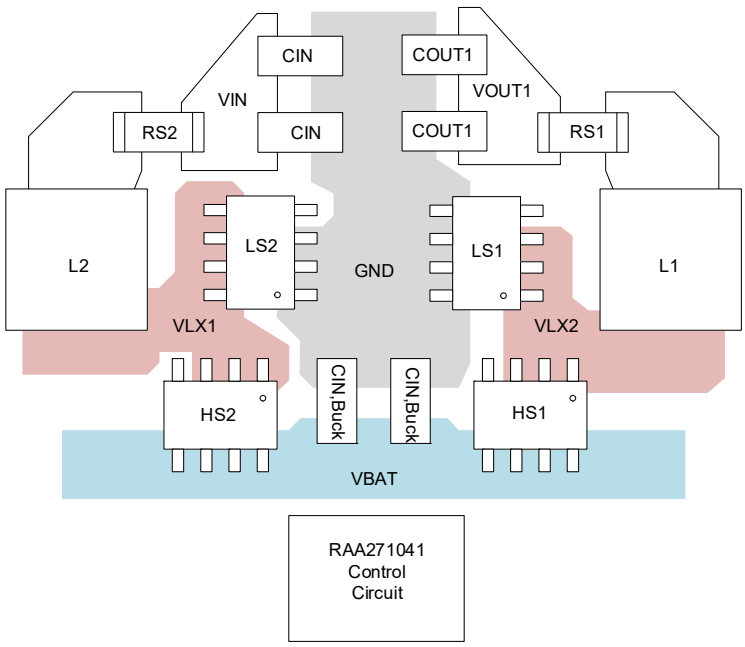


Figure 24. PCB Layout Illustrating Power Component Placement

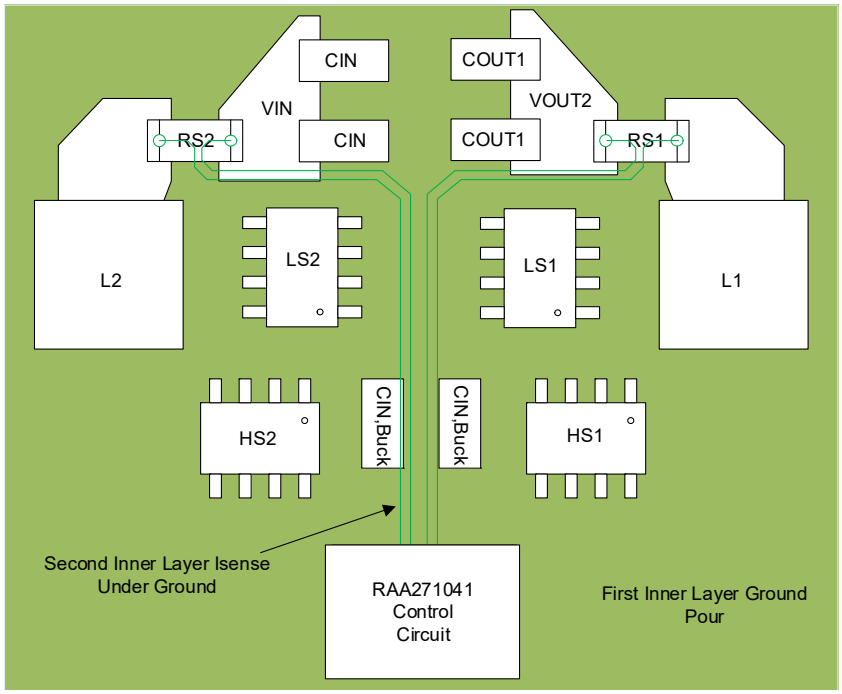
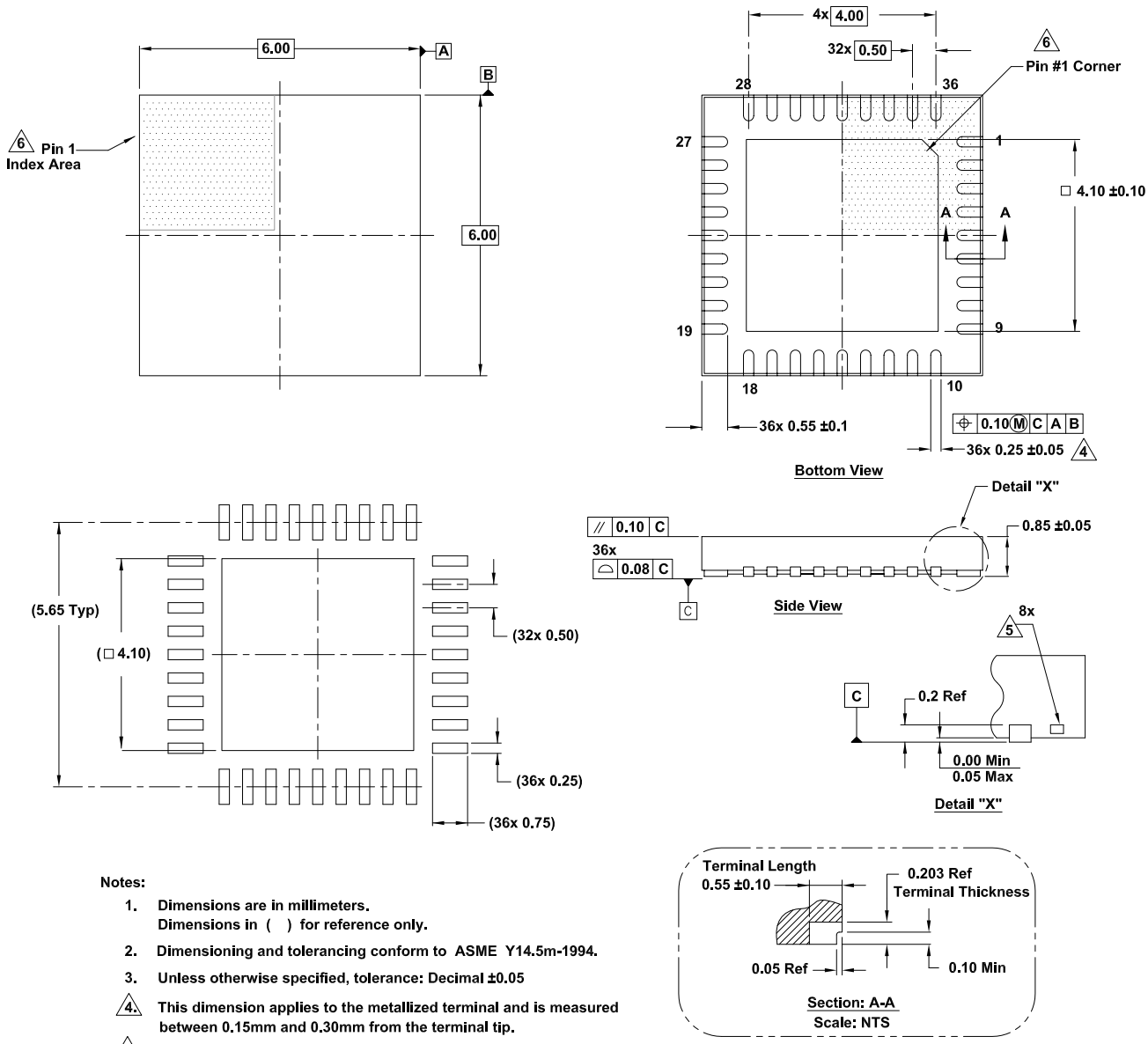


Figure 25. PCB Layout Illustrating Current Sense Routing

7. Package Outline Drawing

For the most recent package outline drawing, see L36.6x6D.

L36.6x6D
36 Lead Step Cut Quad Flat No-Lead Plastic Package (SCQFN)
Rev 0, 12/20



Notes:

1. Dimensions are in millimeters.
   Dimensions in ( ) for reference only.
2. Dimensioning and tolerancing conform to ASME Y14.5m-1994.
3. Unless otherwise specified, tolerance: Decimal ±0.05
4. This dimension applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier is either a mold or mark feature.

8. Ordering Information

Part Number[1][2]	Part Marking	Package Description[3] (RoHS Compliant)	Pkg. Dwg. #	Carrier Type[4]	Temperature Range
RAA271041A4HNP#AA0	271041 A4HNP	36 Ld 6x6 QFN	L36.6x6D	Tube	-40 to +125°C
RAA271041A4HNP#HA0				Reel, 4k	
RTKA271041DE0000BU	RAA271041 Evaluation Board				

1. These Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J-STD-020.
2. For Moisture Sensitivity Level (MSL), see the RAA271041 device page. For more information about MSL see TB363.
3. For the Pb-Free Reflow Profile, see TB493.
4. See TB347 for details about reel specifications.

Table 3. Key Differences Between Family of Parts

Part #	Channel 1	Channel 2	Channel 1 Output Range	Channel 2 Output Range
RAA271041	Buck	Boost	3.3V, 5V, 0.8V to 12V Adjustable	5V to 40V Adjustable
RAA271040	Buck	Buck	3.3V, 5V, 0.8V to 12V Adjustable	0.8V to 40V Adjustable

9. Revision History

Revision	Date	Description
1.00	Dec 16, 2024	Initial release.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: “Standard” and “High Quality”. The intended applications for each Renesas Electronics product depends on the product’s quality grade, as indicated below.

   "Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

   "High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

   Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user’s manual or other Renesas Electronics document.
7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION (“Vulnerability Issues”). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user’s manuals, application notes, “General Notes for Handling and Using Semiconductor Devices” in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) “Renesas Electronics” as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) “Renesas Electronics product(s)” means any product developed or manufactured by or for Renesas Electronics.

(Disclaimer Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.