RAA305315GBM

General purpose OIS Driver IC

Rev.1.06
2020.12.09

1 Over View

RAA305315GBM is general-purpose OIS driver IC .This is a small size single chip IC constituted by the control block built in 32 bits RISC microcomputer and DSP, and by the driver block built in hall signal processing circuit and VCM driver.

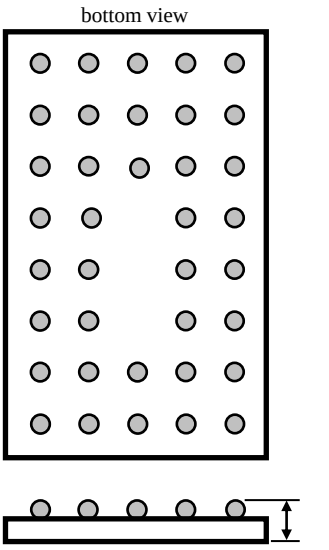
Supports open/closed loop AF control.

2 Features

Applications

Smart phone, Tablet

Pin alignment image
(37pin 2.17mm x 3.36mm
0.4mm pitch square grid array)



WLBGA

Driver Block

[IS]

(1)Built-in 2 channels H-bridge drivers
Composition : ISX, ISY
(2)Built-in 2 channels Hall signal processing circuits
Composition :
Constant Current Bias --- 2 channels
Gain Amp --- 2 channels (with gain resistor)
(3)Built-in 12bit-ADC with 6 channels input selector
(4)Configurable for VCM/Piezo/SMA drive
(5)PWM/Linear drive

[AF]

(1)Built-in H-bridge AF driver for Bi-direction setting
(2)Built-in 1 channels Hall signal processing circuits
Supports open/closed loop AF control
(3)Configurable for VCM drive
(4) Linear drive

Controller

(1)Built-in 32bit RISC CPU : Arm® Cortex®-M0+
Manufactured by Renesas Technology Corp. under license from ARM Limited
(2)Built-in Code Flash ROM(32KB)
(3)Built-in RAM(4KB) for program
(4)Built-in DSP(GREEN_DSP_V2)
(5)Built-in SPI for gyro sensor
(6)Built-in Timer (16bit) 4 channels
(7)Built-in IIC serial interface 1 channel
(8)Built-in General purpose I/O 8lines (with interruption function)
(9)Clock frequency : Built-in PLL (x4, x6, x8, x12, x16)
For system clock ---------- 32.4MHz(Max)
For PWM clock of motor control ------- 162MHz(Max)
For SPI serial clock ---------- 4MHz(Max)
For IIC serial clock ---------- 1MHz(Max, Fast Mode+)

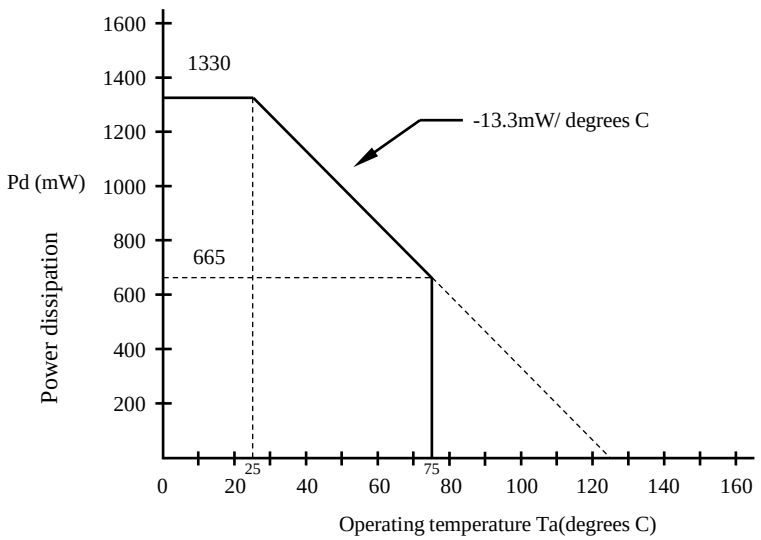
Others

(1)Built in POR(power on reset), TSD(thermal shut down)
(2)Built in Power save mode
(3)Built in IS/AF Driver control synchronized signal from Image Sensor

ABSOLUTE MAXIMUM RATING (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power dissipation	Pd	1330	mW	note1 (Ta=25 degrees C)
Thermal derating	Kθ	-13.3	mW/degrees C	note1 (Ta=25 degrees C)
Maximum junction temperature	Tj	125	degrees C	
Storage temperature	Tstg	-40 to 125	degrees C	
Power supply 1	VDD	4.6	V	note2
Power supply 2	VCC	4.6	V	note2
Power supply 3	VM	4.6	V	note2
Input voltage of terminals	Vin	-0.3 to VDD + 0.3	V	note3
DC output current	Iout	+/- 600	mA	note4
Peak output current	Iop	+/- 800	mA	note4 pulse width<10ms,Duty<=20%

Notes note1 : Glass epoxy board: 76mm × 114mm × 1.6mm 4layers board(Cu cover rate:1-layer 20%,2-layer 100%,3-layer 100%,4-layer 20%)
note2 : Don't impress a power supply conversely in principle.
note3 : Don't impress more than power supply voltage and below GND voltage in principle.
note4 : Don't exceed the specification of output current, when more than one CH use them, turning on at the same time.



Notes The power consumption of this IC has the dominant electric power which each output transistor consumes.

Output transistor power consumption formula
(Output current)^2 x Ron (ex.) (400mA)^2 x 3.3 ohm=528mW

When ambient air temperature is 25 degrees C or more, please install a heat sink with reference to the above figure if needed.

RECOMMENDED OPERATING CONDITIONS (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power supply 1	VDD	1.7 to 3.3	V	
Power supply 2	VCC	2.7 to 3.3	V	note1
Power supply 3	VM	2.7 to 3.3	V	note1

note1 : VCC and VM are designed on the assumption that it is used on the same voltage except the reset mode.
However, there is no problem if the voltage difference is less than 0.2V.

RATED POWER SUPPLY VOLTAGE (Ta=25 degrees C)

ITEM	SYMBOL	RATING	UNIT	NOTES
Power supply 1	VDD	1.8	V	
Power supply 2	VCC	2.8	V	
Power supply 3	VM	2.8	V	

OPERATING TEMPERATURE

ITEM	SYMBOL	RATING	UNIT	NOTES
Operating temperature	Topr	-20 to 75	degrees C	note1

note1 : Flash write / erase : -10 to 50 degrees C

PIN LOCATION

Bottom View

	5	4	3	2	1
A	RESET_N	VDD	SPI_CS	SPI_MOSI	SPI_MISO
B	TEST2	EXCLK	SWCLK	SPI_SCK	IMGHD
C	SCL	VSS	MON (analog monitor)	SWDIO	TEST1
D	SDA	VCC		HAISX_INN	HDISX_OUT
E	AD2	HAAF _INN		HDISY_OUT	HAISX_INP
F	TEST3	HAAF _INP		HAISY_INN	HAISY_INP
G	RSENS	OUTAF_A	OUTISX_B	PGND	HDAF_OUT
H	VM	OUTAF_B	OUTISX_A	OUTISY_A	OUTISY_B

Power Supply

GND

Driver

Sensing circuit

Controller

RENESAS TEST (Don't Connect)

TopView

	1	2	3	4	5
A	SPI_MISO	SPI_MOSI	SPI_CS	VDD	RESET_N
B	IMGHD	SPI_SCK	SWCLK	EXCLK	TEST2
C	TEST1	SWDIO	MON (analog monitor)	VSS	SCL
D	HDISX_OUT	HAISX_INN		VCC	SDA
E	HAISX_INP	HDISY_OUT		HAAF _INN	AD2
F	HAISY_INP	HAISY_INN		HAAF _INP	TEST3
G	HDAF_OUT	PGND	OUTISX_B	OUTAF_A	RSENS
H	OUTISY_B	OUTISY_A	OUTISX_A	OUTAF_B	VM

Pin Functions

No.	Land Address	Pin	Sub Function GPIO	I/O Level	IN/OUT Power/GND	Initial Condition *4	Function	Termination of unused pin
1	D4	VCC	-	-	Power supply	-	Power supply for analog block and flash	-
2	A4	VDD					Power supply for I/O and digital block	-
3	H5	VM					Power supply for IS/AF driver	-
4	G2	PGND	-	-	GND	-	Power system GND	-
5	C4	VSS					Digital and analog GND	-
6	H3	OUTISX_A	-	VM	OUT	Z	ISXch driver outpput A	*1
7	G3	OUTISX_B	-		OUT	Z	ISXch driver outpput B	*1
8	H2	OUTISY_A	-		OUT	Z	ISYch driver outpput A	*1
9	H1	OUTISY_B	-		OUT	Z	ISYch driver outpput B	*1
10	G4	OUTAF_A	-		OUT	Z	AFch driver output A	*1
11	H4	OUTAF_B	-		OUT	Z	AFch driver output B	*1
12	G5	RSENS	-		OUT	Z	AF current monitor	*1
13	C3	MON	-	VCC	OUT	Z	To Monitor Loop Gain	*1
14	D1	HDISX_OUT	-		OUT	Z	Hall ISXch constant current output	*1
15	E1	HAISX_INP	-		IN	Z	Hall amplifier ISX non-inverting input	*2
16	D2	HAISX_INN	-		IN	Z	Hall amplifier ISX inverting input	
17	E2	HDISY_OUT	-		OUT	Z	Hall ISYch constant current output	*1
18	F1	HAISY_INP	-		IN	Z	Hall amplifier ISY non-inverting input	*2
19	F2	HAISY_INN	-		IN	Z	Hall amplifier ISY inverting input	
20	G1	HDAF_OUT	-		OUT	Z	AF constant current output	*1
21	F4	HAAF_INP	-		IN	Z	Hall amplifire AF non-inverting input	*2
22	E4	HAAF_INN	-		IN	Z	Hall amplifire AF inverting input	
23	E5	AD2	-		IN	Z	ADC input	*2
24	A5	RESET_N	-	VDD	IN	Z	Reset	-
25	C5	SCL	GPIO00		IN/OUT	Z	SCL for I2C Interface / GPIO port GPIO00 / UART RXD00 / CPU INTIN0 / DSP IN0	*3
26	D5	SDA	GPIO01		IN/OUT	Z	SDA for I2C Interface / GPIO port GPIO01 / UART TXD00 / CPU INITIN1 / DSP IN1	*3
27	B2	SPI_SCK	GPIO02		IN/OUT	Z	CLOCK input or output for SPI (SCK) / GPIO port GPIO02 / CPU INTIN2 / DSP IN2	*3
28	A2	SPI_MOSI	GPIO03		IN/OUT	Z	Data inout for SPI (DAT) / Data output for SPI (MOSI) / GPIO port GPIO03 / CPU INTIN3 / DSP IN3	*3
29	A1	SPI_MISO	GPIO07		IN/OUT	Z	Data input for SPI (MISO) / GPIO port GPIO07 / CPU INTIN7	*3
30	A3	SPI_CS	GPIO04		IN/OUT	Z	Chip select input or output for SPI (CS) / GPIO port GPIO04 / TAU TO0, TO1, TO2 / CPU INTIN4	*3
31	B4	EXCLK	-		IN	Z	External CLOCK input	-
32	B3	SWCLK	GPIO05		IN/OUT	Z (Pull-up)	Clock input for Debugger / GPIO port GPIO05 / UART RXD00 / TAU TI2 / CPU INTIN5	*3
33	C2	SWDIO	GPIO06		IN/OUT	Z (Pull-up)	Data input/output for Debugger / GPIO port GPIO06 / UART TXD00 / TAU TI1 / CPU INTIN6	*3
34	B1	IMGHD	-		IN	Z	Image Sencor Sync signal	*2
35	C1	TEST1	-	-	IN	Pull-up	TEST for RENESAS	*1
36	B5	TEST2	-	-	OUT	-	TEST for RENESAS	*1
37	F5	TEST3	-	-	IN	Z	TEST for RENESAS	*1

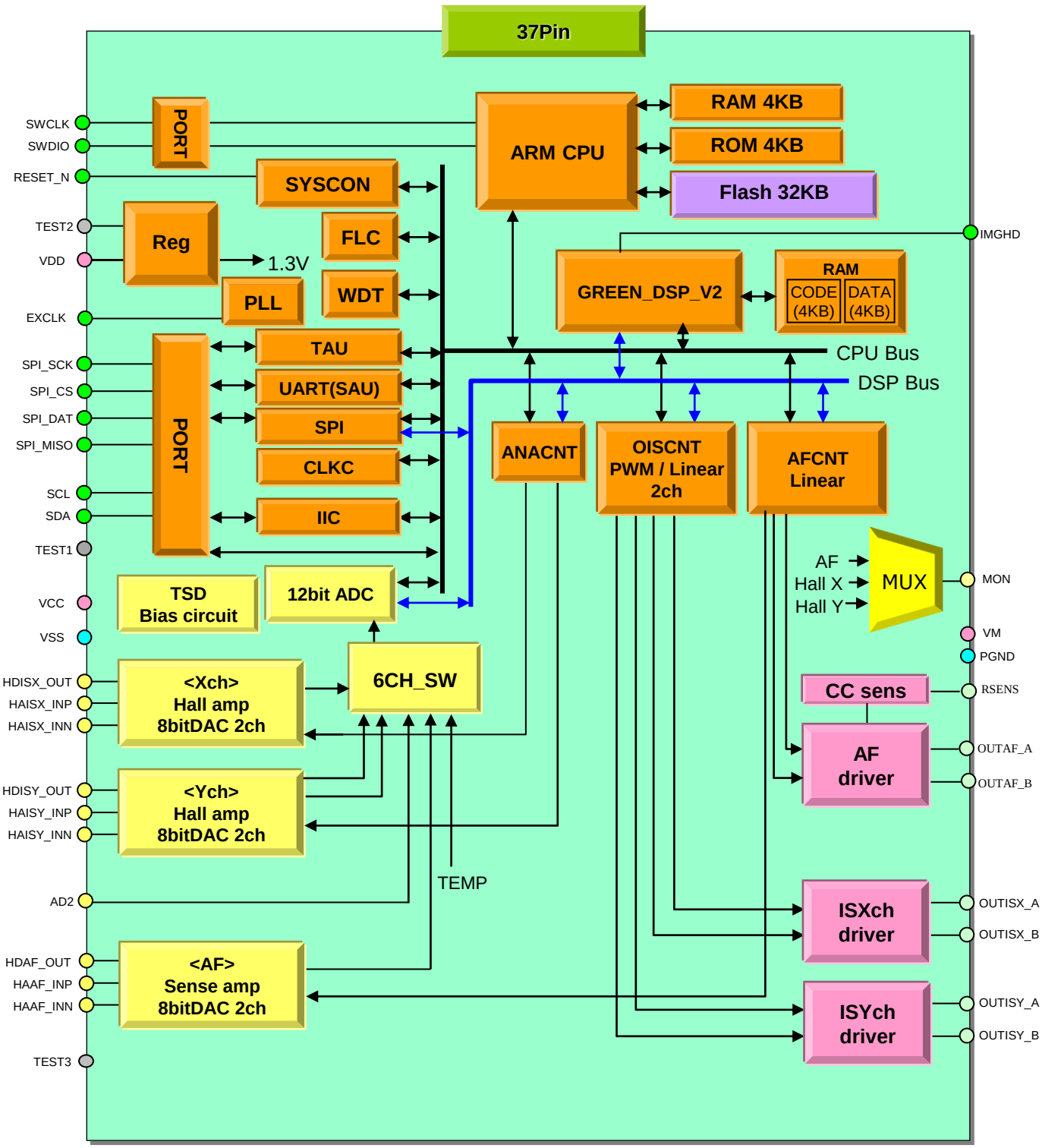
*1 Open

*2 Connect to VSS

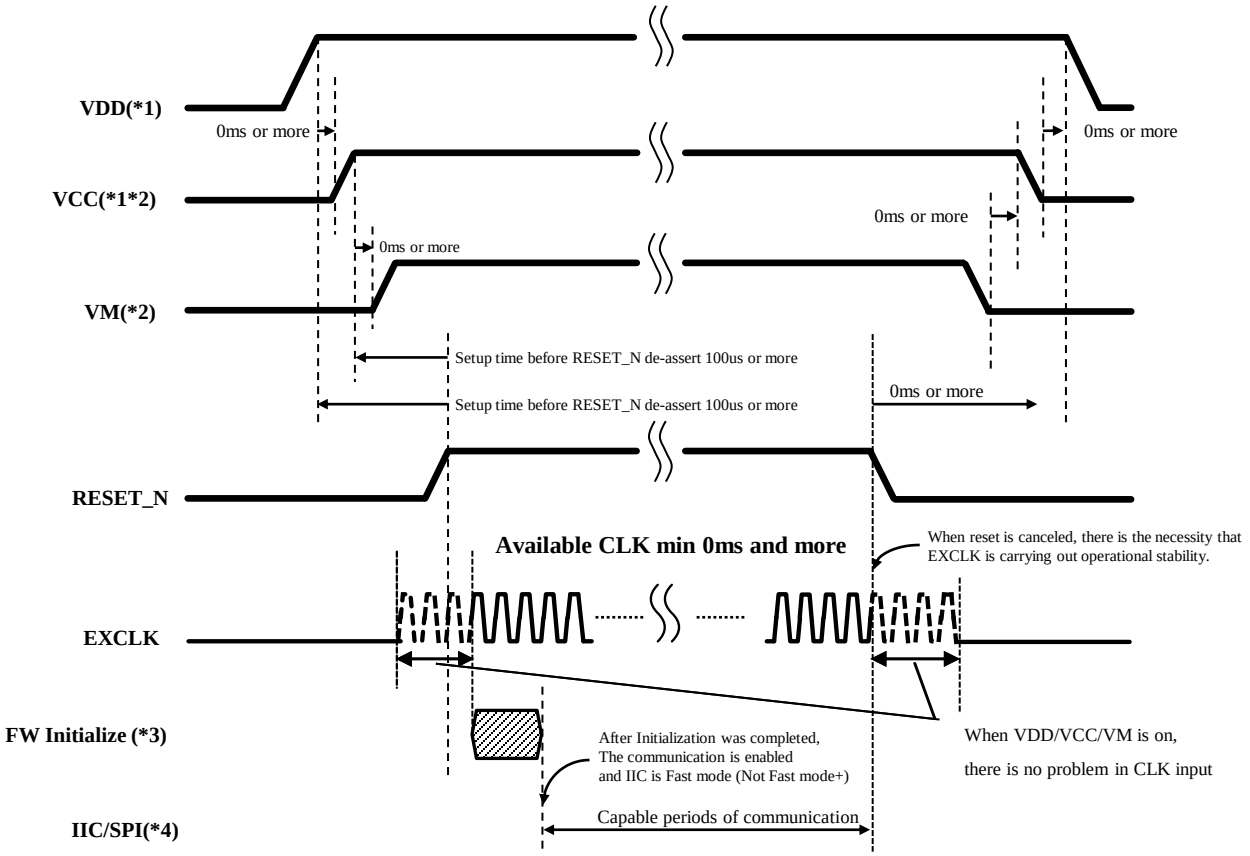
*3 'Connect to VSS' or
'Pin is Open
,Pin enbled in PORTSEL register
,Switch to GPIO in PNMOD register
,Output Enable in GPIO0OE register
and output data fixed to '0' in GPIO0DT register.'

*4 An initial value is not influenced by the RESET_N terminal.

TOTAL BLOCK


37Pin
SWCLK
SWDIO
RESET_N
TEST2
VDD
EXCLK
SPI_SCK
SPI_CS
SPI_DAT
SPI_MISO
SCL
SDA
TEST1
VCC
VSS
HDISX_OUT
HAISX_INP
HAISX_INN
HDISY_OUT
HAISY_INP
HAISY_INN
AD2
HDAF_OUT
HAAF_INP
HAAF_INN
TEST3
PORT
PORT
SYSCON
Reg
1.3V
PLL
FLC
WDT
TAU
UART(SAU)
SPI
CLKC
IIC
TSD
Bias circuit
12bit ADC
6CH_SW
<Xch>
Hall amp
8bitDAC 2ch
<Ych>
Hall amp
8bitDAC 2ch
<AF>
Sense amp
8bitDAC 2ch
TEMP
ARM CPU
RAM 4KB
ROM 4KB
Flash 32KB
GREEN_DSP_V2
RAM
CODE (4KB)
DATA (4KB)
IMGHD
CPU Bus
DSP Bus
ANACNT
OISCNT
PWM / Linear
2ch
AFCNT
Linear
AF
Hall X
Hall Y
MUX
MON
VM
PGND
RSENS
CC sens
AF
driver
OUTAF_A
OUTAF_B
ISXch
driver
OUTISX_A
OUTISX_B
ISYch
driver
OUTISY_A
OUTISY_B

POWER SUPPLY SEQUENCE



Notes at the time of power-on

*1 Please apply VDD before VCC.

*2 Please apply VCC before VM.

Notes at the time of power-down

*1 Please power down VCC after VM

*2 Please power down VDD after VCC.

Notes at the time of FW Initialization

*3 The periods of FW Initialization is depend on FW.

CPU initialize the registers of IIC during the periods of FW Initialization.

Notes at the time of Actuator drive

*4 If the clock stops while driving the actuator, the drive current will flow continuously and the actuator may be damaged. Please do not stop the clock while driving.

Consumption current

If not specified, VDD=1.8V,VCC=VM=2.8V Ta=25degreeC

Item	Symbol	Condition	Standard Value			Unit	Remarks
			min	typ	max		
VDD current	IVDln	EXCLK=27MHz PLL=162MHz,System Clock=32.4MHz Linear mode	-	10	14	mA	*1
VCC current	IVCln	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h,BTL_IS*DAC & AF_BTL setting Defult.	-	4.5	6.75	mA	
VM current	IVMpw	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h PWM mode	-	0.8	1.2	mA	*2
VM current	IVMln	All output function without load.HA* DAC setting code 80h,HB*DAC setting code 00h,BTL_IS*DAC & AF_BTL setting Defult.	-	7.6	11.4	mA	

Note *1:These are reference data. These are depend on FW processing.
*2: These are reference , not guaranteed.

Electrical characteristics (POR threshold)

If not specified, Ta=25degreeC

Item	Symbol	Condition	Standard Value			Unit	Remarks
			min	typ	max		
UVP (Under Voltage Protect)							
PVO detect level	PVO	Check on VCC >Vcore	1.30	1.55	1.67	V	
LVI detect level 2	LVI2	Check on VCC level, LVITH=set at "low level"	2.10	2.40	2.70	V	*1
LVI detect level 3	LVI3	Check on VCC level, LVITH=set at "high level"	2.30	2.60	2.90	V	*1,*2
POR detect level	POR	Check on VDD	1.30	1.60	1.68	V	

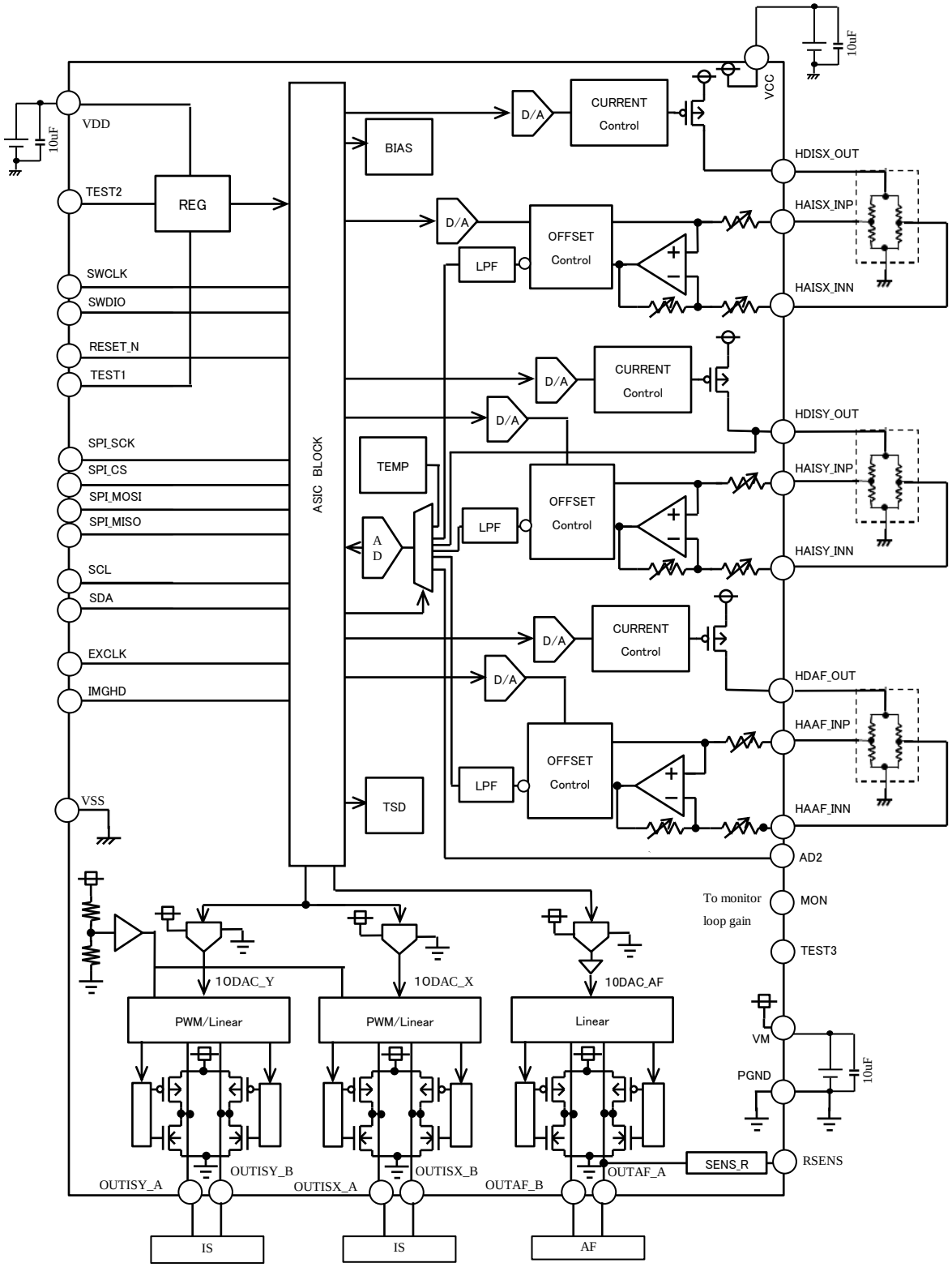
Note *1: These are reference , not guaranteed.
Note *2: Use this with VCC=3.0V or more.

OIS controller

RAA305315GBM

(Driver Block)

Example for circuit of Driver Block (Analog & Driver)



Electrical specification (Analog block) Ta=25 degrees C

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
12bit ADC	Resolution	RES	684uV/LSB @VCC=2.8V	—	12	—	bit	
	Liniearity minimum code	DRLAD	about 0.1V	—	—	080h	CODE	
	Liniearity maximum code	DRHAD	about VCC-0.1V	F7Fh	—	—	CODE	
	Zero scale input voltage	VINLAD		—	0	—	V	
	Full scale input voltage	VINHAD		—	VCC	—	V	
	Conversion time	TCAD		3.375	—	—	us	
	clock frequency	FCLK		—	—	16	MHz	
Hall Amplifier	Lo output voltage	VOLMN		—	—	0.10	V	
	Hi output voltage	VOHMN		VCC-0.1	—	—	V	
	Differential Gain accuracy	GHS	x20, x30, x40, x50, x80 x120, x160, x100, x150	-12	0	12	%	
	Output LPF cut-off frequency	BWHA	-3dB	—	10	—	kHz	*1
Hall Amplifier offset adjusting 8bit DAC	Resolution	RES	10.9mV/LSB @VCC=2.8V	—	8	—	bit	
	Differential Nonlinearity	DNLDA8	guaranteed monotonic, IO=0mA DAC setting code DRLDA8～DRHDA8	-1	—	1	LSB	*1
	Integral Nonlinearity	INLDA8	IO=0mA DAC setting code DRLDA8～DRHDA8	(Reference value) -2	—	(Reference value) 2	LSB	*1
	Liniearity minimum code	DRLDA8	about 0.25V IO=0mA	—	—	15h	CODE	
	Liniearity maximum code	DRHDA8	about 2.75V IO=0mA	EBh	—	—	CODE	
	Zero scale output voltage	VOZSDA8	DAC setting code 00h, IO=0mA	—	—	0.1	V	
	Full scale output voltage	VOFSDA8	DAC setting code FFh, IO=0mA	VCC-0.1	—	—	V	
	Output response time	TCDA8	DRLDA8～DRHDA8	—	—	(Reference value) 5	us	*1
Constant Current Amplifier (OIS)	FET Tr minimum current	IIBMINIC	DAC setting code 00h VIN=0V, ISET[1:0]=01b	—	—	10	uA	
	FET Tr maximum current 1	IIBMAXIC1	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=00b	1.0	—	—	mA	
	FET Tr maximum current 2	IIBMAXIC2	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=01b	2.0	—	—	mA	
	Internal DAC linearity minimum code	DRLIDA8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	—	—	11h	CODE	
	Internal DAC linearity maximum code	DRHIDA8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	D6h	—	—	CODE	

Note *1: These are reference , not guaranteed.

Electrical specification (Analog block) Ta=25 degrees C

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
AF Amplifier	Lo output voltage	VOLAF		—	—	0.10	V	
	Hi output voltage	VOHAF		VCC-0.1	—	—	V	
	Differential Gain accuracy	GHS	x7,x20,x45,x80	-12	0	12	%	
	Reference voltage setting 1	VRFINN1	HAAF_INN setting Low	0.2	0.3	0.4	V	
	Reference voltage setting 2	VRFINN2	HAAF_INN setting Mid1	0.7	0.8	0.9	V	
	Reference voltage setting 3	VRFINN3	HAAF_INN setting Mid2	1.3	1.4	1.5	V	
	Reference voltage setting 4	VRFINN4	HAAF_INN setting High	1.9	2.0	2.1	V	
	Output LPF cut-off frequency	BWHAAF	-3dB	—	10	—	kHz	*1
Constant Current (AF)	FET Tr minimum current	IIBMINICAF	DAC setting code 00h VIN=0V, ISET[1:0]=01b	—	—	10	uA	
	FET Tr maximum current 1	IIBMAXICAF1	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=00b	1.0	—	—	mA	
	FET Tr maximum current 2	IIBMAXICAF2	DAC setting code D6h VIN=VCC-0.5V, ISET[1:0]=01b	2.0	—	—	mA	
	Internal DAC linearity minimum code	DRLIDAAF8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	—	—	11h	CODE	
	Internal DAC linearity maximum code	DRHIDAAF8	RL=0.75kohm, Vb=0, ISET[1:0]=01b	D6h	—	—	CODE	

Note *1: These are reference , not guaranteed.

Electrical specification (Driver block) Ta=25 degrees C

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
Linear Driver (ISX, ISY, AF)	IS DAC Resolution	RESIS		-	10	-	bit	
	IS internal DAC linieariy minimum code	DRLIDA10IS	RL=28ohm	—	—	C0h	CODE	*1
	IS internal DAC linieariy maximum code	DRHIDA10IS	RL=28ohm	340h	—	—	CODE	*1

Note *1: These are reference , not guaranteed.

If not specified, VCC=VM=2.8V, VDD=1.8V, Ta=25 degrees C

	Item	Symbol	Condition	Standard Value			Unit	Remarks
				min	typ	max		
IS* PWM driver	On resistance IS	RONIS	Io=100mA, VM=2.8V Total of top and bottom resistance	-	3.6	5.8	ohm	*1
	Turn on time 1	TON1	Threshold 50%, Io=100mA IS slew rate setting=000b	-	0.3	0.45	µs	
	Turn off time 1	TOFF1	Threshold 50%, Io=100mA IS slew rate setting=000b	-	0.12	0.24	µs	
	Rise up time 1	Tr1	From 10% to 90%, Io=100mA IS slew rate setting=000b	-	0.13	0.52	µs	
	Fall downtime 1	Tf1	From 90% to 10%, Io=100mA IS slew rate setting=000b	-	0.05	0.10	µs	
	Turn on time 2	TON2	Threshold 50%, Io=100mA IS slew rate setting=110b	-	0.26	0.39	µs	
	Turn off time 2	TOFF2	Threshold 50%, Io=100mA IS slew rate setting=110b	-	0.12	0.24	µs	
	Rise up time 2	Tr2	From 10% to 90%, Io=100mA IS slew rate setting=110b	-	0.11	0.44	µs	
	Fall downtime 2	Tf2	From 90% to 10%, Io=100mA IS slew rate setting=110b	-	0.05	0.10	µs	
	Turn on time 3	TON3	Threshold 50%, Io=100mA IS slew rate setting=101b	-	0.24	0.36	µs	
	Turn off time 3	TOFF3	Threshold 50%, Io=100mA IS slew rate setting=101b	-	0.12	0.24	µs	
	Rise up time 3	Tr3	From 10% to 90%, Io=100mA IS slew rate setting=101b	-	0.08	0.32	µs	
	Fall downtime 3	Tf3	From 90% to 10%, Io=100mA IS slew rate setting=101b	-	0.05	0.10	µs	

Note *1: These are reference , not guaranteed.

OIS controller

RAA305315GBM
(Controller Block)

Controller Block outline

Block diagram

Block diagram is shown in below.

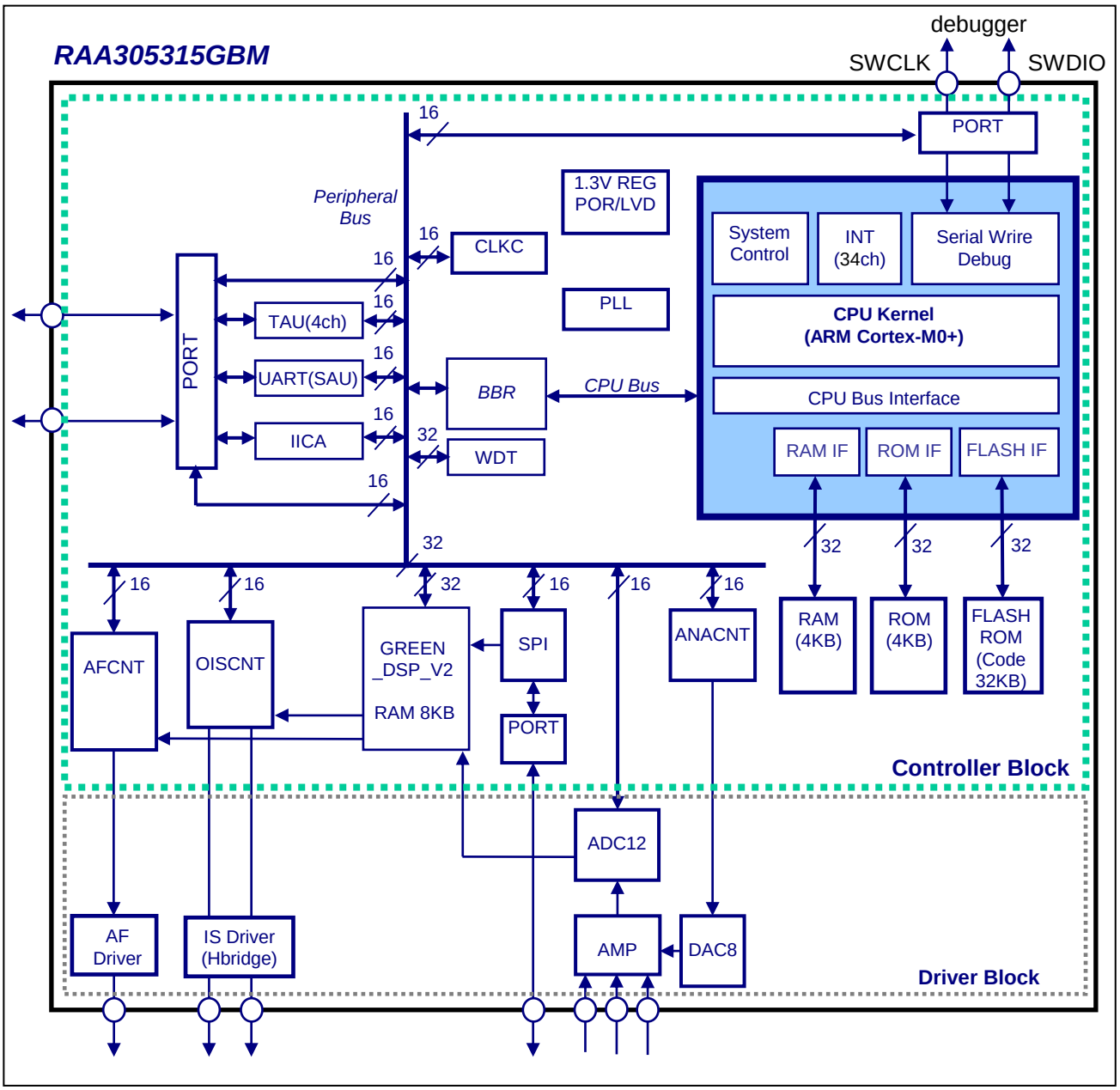


Figure 1.1 RAA305315GBM Block diagram

BBR:Bus BRidge
TAU:Timer Array Unit

Controller Features

RAA305315GBM controller peripheral I/O Features shown in Table (1)

Function block	Features	
Interrupt controller (INT)	· Internal Interrupts	: 26 sources
	· External interrupts	: 8 sources
	· ICUIN input sense	: Edge sense (rise edge, fall edge, both edges)
	· Priority	: Programable
TIMER ARRAY UNIT(TAU)	· Channels	: 4ch
	· Count bit	: 16 bits counter, down counting
	· Timer scale	: $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
General purpose I/O & Pin control (PORT)	· GPIO number of lines	: 8 lines (GPIO)
	· I/O pins	: Can be set to each I/O pin using the corresponds input and output control register bits. : Can be select to each I/O from GPIO and peripheral module Pin mode register 0/1/2/3.
	· I/O pins control	: Each pins can be changed GPIO and other peripheral functions with setting the operation mode register.
	· I/O pins pull-up	: Enables and disables the pull-up resistors.
Serial Peripheral Interface (SPI)	· Number of channels	: 1 channel
	· Character length	: 8 bits
	· Order of transfer	: MSB first or LSB first
	· Shift clock	: Internal shift clock
	· Internal shift clock source	: $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
	· Baud rate count	: 2-256
	· Transmit interrupt factor	: Transmit buffer empty or Transmit end
	· Receive error detection	: Overrun
	· Chip Select	: Chip select signal
	· DSP register access	: Registers are accessible from CPU

RAA305315GBM controller peripheral I/O Features shown in Table (2)

Function block	Features	
Universal asynchronous Receiver Transmitter (UART)	·Channels	: 1 channel
	·Character length	: 7/8/9 -bit length can be selected
	·Transfer order	: MSB and LSB first can be selected
	·Stop bit length	: 1 or 2 bit can be selected
	·Parity check	: Can be enabled or disabled
	·Attribute of parity check	: Even or Odd parity can be selected
	·Internal clock source	: Dividable range = : $f_{CLK}/2^0$ to $f_{CLK}/2^{15}$
	·Baud rate counter	: Maximum 2-256
	·Transmit interrupt factor	: Transmit buffer empty or Transmit end can be selected. Error interrupt also.
	·Error detection	: Framing error, Parity error, Overrun error.
Clock /PLL/ System control	·Clock source	: External Input (EXCLK)
	·SYSTEM/DSP clocks	: 32.4MHz max
	·PWM clocks	: 162MHz max
	·Standby Function	: SLEEP, DEEP-SLEEP
	·PLL clock(=PWM clocks)	: MAX : 162MHz
	·PLL control	: PLL can be stop.
	·OIS module clock control	: OIS module clock control can be stop
Multi Master & Slave SERIAL INTERFACE IICA (IICA)	·Channels	: 1 channel
	·Clock frequency	: Standard mode (fastest transfer rate: 100 kbps) : Fast mode (fastest transfer rate: 400 kbps) : Fast mode+ (fastest transfer rate: 1 Mbps)
	·Transmit interrupt factor	: Transfer end interrupt
	·Error detection	: Overrun error Parity error (ACK error)
OIS Control (OISCNT)	·Image stabilizer drive function	: 2 channel PWM or Linear (H-bridge)
	·DSP register access	: Registers are accessible through CPU Bus.
AF Control (AFCNT)	·Auto focus drive function	: 1 channel Linear (H-bridge)
	·DSP register access	: Registers are accessible through CPU Bus.

RAA305315GBM controller peripheral I/O Features shown in Table (3)

Function block	Features	
DSP (GREEN_DSP_V2)	· Arithmetic operation	: Multiplication Signed 32 bits * Signed 32 bits = Signed 32 bits Multiplication results (64 bits) can be shifted right any number of bits : Addition/ Substruct Signed 32 bits + Signed 32 bits = Signed 32 bits Signed 32 bits - Signed 32 bits = Signed 32 bits Internally calculated with 33bits precision. : Limit calculation Upper-/lower-limits can be set. : Capable to generate an interrupt to the CPU at program halt.
	· Interrupt requests	: When program halts: Executes the STOP, break, and undefined instructions.
Analog Control (ANACNT)	· AMP,DAC8 control	: Control register
	· DSP register access	: Registers are accessible through CPU Bus.
12bit ADC Control (ADC12)	· Resolution	: 12bits
	· Channels	: 6ch
	· Conversion mode	: Single mode, Scan mode
	· DSP register access	: Registers are accessible through CPU Bus.
POR (Power-on-reset circuit)	· Power-on-reset: 1.60V (VDD)	

Electrical characteristics (Controller block) Ta=25 degrees C

DC characteristics

If not specified VDD=1.8V, VCC=VM=2.8V, Ta=25 degrees C

Item	Symbol	Conditions	Limit			Unit	Remarks
			Min	Typ	Max		
'H' output voltage	VOH	IOH=-2mA	VDD*0.8	-	VDD	V	note1
'L' output voltage	VOL	IOL=2mA	0		VDD*0.2	V	note1
'H' input current	IIH	VI=VDD	-	-	1	uA	note2
'L' input current	IIL	VI=0V	-	-	-1	uA	note2
Pull-up resistance	Rup		10	-	150	Kohm	note3
'H' input voltage	VIH		VDD*0.7	-	VDD	V	-
'L' input voltage	VIL		0	-	VDD*0.3	V	-

note1. correspondence terminal: SCL, SDA, SPI_SCK, SPI_DAT, SPI_MISO, SPI_CS, SWCLK, SWDIO
note2. in condition that pull-up resistance is not connected. (The built-in pull-up resistor is disabled by the F/W.)
note3. correspondence terminal: SPI_SCK, SPI_DAT, SPI_MISO, SPI_CS, SWCLK, SWDIO

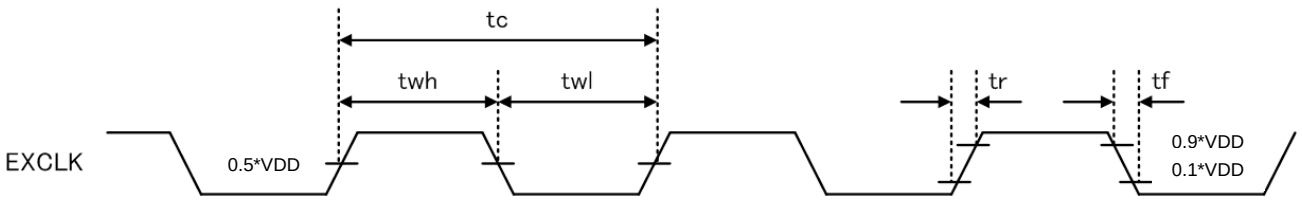
Electrical characteristics (Controller block)　Ta=25 degrees C

AC characteristics

(1) EXTERNAL CLOCK (CLOCK)

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
Input Frequency	fclk	-	6	29	MHz	-
Input 'H' pulse width	twh	＞ 0.5*VDD	14	-	ns	-
Input 'L' pulse width	twl	＜ 0.5*VDD	14	-	ns	-
Input rise time	Tr	VDD voltage 10% to 90%	-	2	ns	-
Input fall time	Tf	VDD voltage 10% to 90%	-	2	ns	-
Cycle-to-cycle period jitter	tjit(CC)	-	-	2	%	-
Period Jitter	tjit(per)	-	-4	4	%	-



Electrical characteristics (Controller block)　Ta=25 degrees C

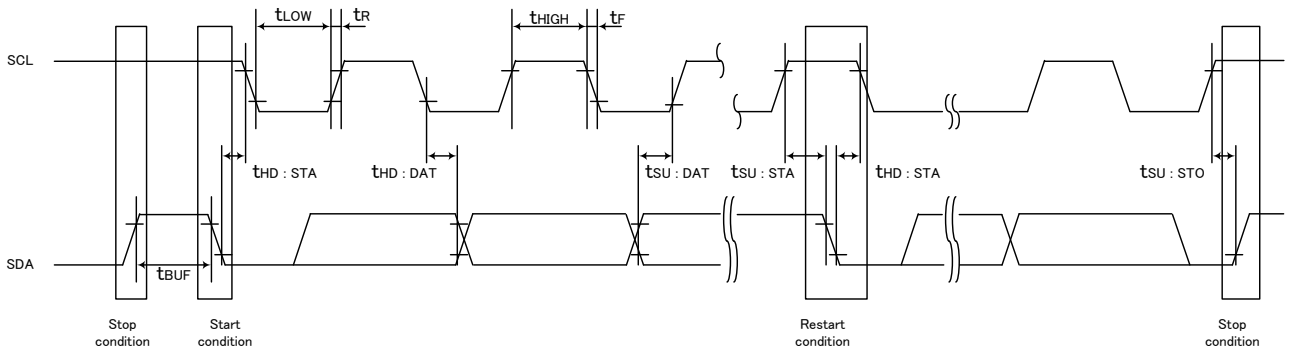
AC characteristics

(2) IIC input timing

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Standard Mode		Fast Mode		Fast Mode Pulus		Unit	Remarks
			Min	Max	Min	Max	Min	Max		
SCL clock frequency	f_{SCL}	-	0	100	0	400	0	1000	kHz	-
Setup time of restart condition *1	$t_{SU:STA}$	-	4.7	-	0.6	-	0.26	-	us	-
Hold time	$t_{HD:STA}$	-	4.0	-	0.6	-	0.26	-	us	-
Hold time when SCL = "L"	t_{LOW}	-	4.7	-	1.3	-	0.5	-	us	-
Hold time when SCL = "H"	t_{HIGH}	-	4.0	-	0.6	-	0.26	-	us	-
Data setup time (receive)	$t_{SU:DAT}$	-	250	-	100	-	50	-	ns	-
Data hold time (transmission) *2	$t_{HD:DAT}$	-	0	3.45	0	0.9	0	-	us	-
Setup time of stop condition	$t_{SU:STO}$	-	4.0	-	0.6	-	0.26	-	us	-
Bus-free time	t_{BUF}	-	4.7	-	1.3	-	0.5	-	us	-

*1 The first clock pulse is generated after this period when the start/restart condition is detected.
*2 tHD:DAT at maximum is a specification in normal output timing, a wait state is inserted in the ACK (acknowledge) timing.



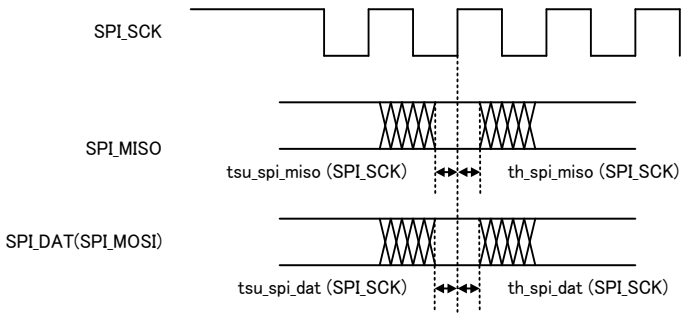
Electrical characteristics (Controller block) Ta=25 degrees C

(3) SPI timing (Master Mode)

(a) input timing

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
input setup time SPI_MISO	tsu_spi_miso (SPI_SCK)	-	110	-	ns	-
input hold time SPI_MISO	th_spi_miso (SPI_SCK)	-	19	-	ns	-
input setup time SPI_DAT (SPI_MOSI)	tsu_spi_dat (SPI_SCK)	-	110	-	ns	-
input hold time SPI_DAT (SPI_MOSI)	th_spi_dat (SPI_SCK)	-	19	-	ns	-

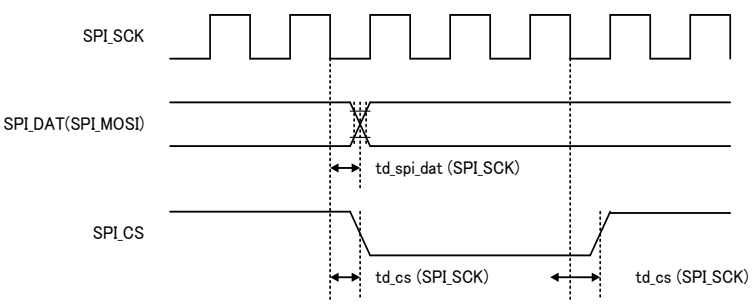


(b) output timing

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
data output delay SPI_DAT (SPI_MOSI)	td_spi_dat (SPI_SCK)	-	-	10	ns	(1)
CS output delay SPI_CS	td_spi_cs (SPI_SCK)	-	-	10	ns	(1)

Note(1): This specification is Design assurance value.



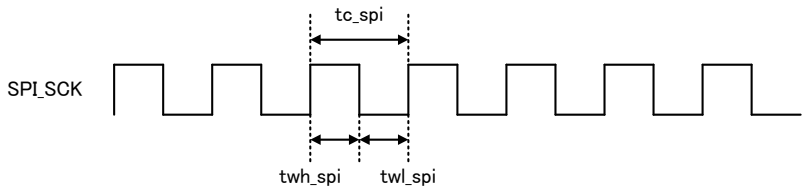
Electrical characteristics (Controller block) Ta=25 degrees C

(4) SPI timing (Slave Mode)

(a) SPI CLOCK (SPI_SCK)

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

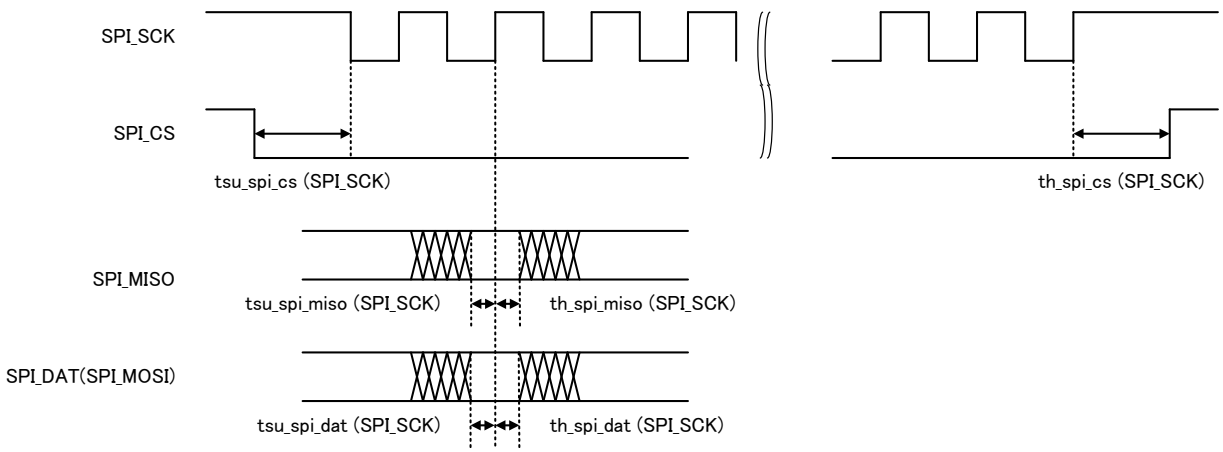
Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
SPI Clock input cycle time	tc_spi	-	250	-	ns	-
SPI Clock input 'H' pulse width	twh_spi	-	120	-	ns	-
SPI Clock input 'L' pulse width	twl_spi	-	120	-	ns	-



(b) input timing

If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
input setup time SPI_CS	tsu_spi_cs (SPI_SCK)	-	200	-	ns	-
input hold time SPI_CS	th_spi_cs (SPI_SCK)	-	232	-	ns	-
input setup time SPI_MISO	tsu_spi_miso (SPI_SCK)	-	62	-	ns	-
input hold time SPI_MISO	th_spi_miso (SPI_SCK)	-	63	-	ns	-
input setup time SPI_DAT (SPI_MOSI)	tsu_spi_dat (SPI_SCK)	-	62	-	ns	-
input hold time SPI_DAT (SPI_MOSI)	th_spi_dat (SPI_SCK)	-	63	-	ns	-



Electrical characteristics (Controller block) Ta=25 degrees C

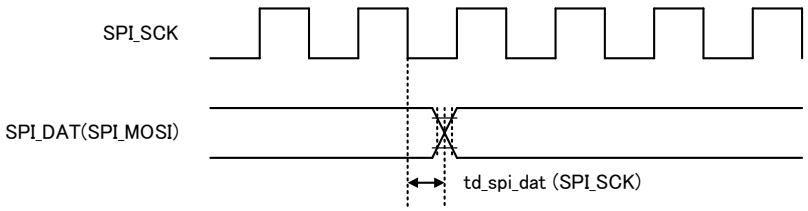
(4) SPI timing (Slave Mode)

(c) output timing

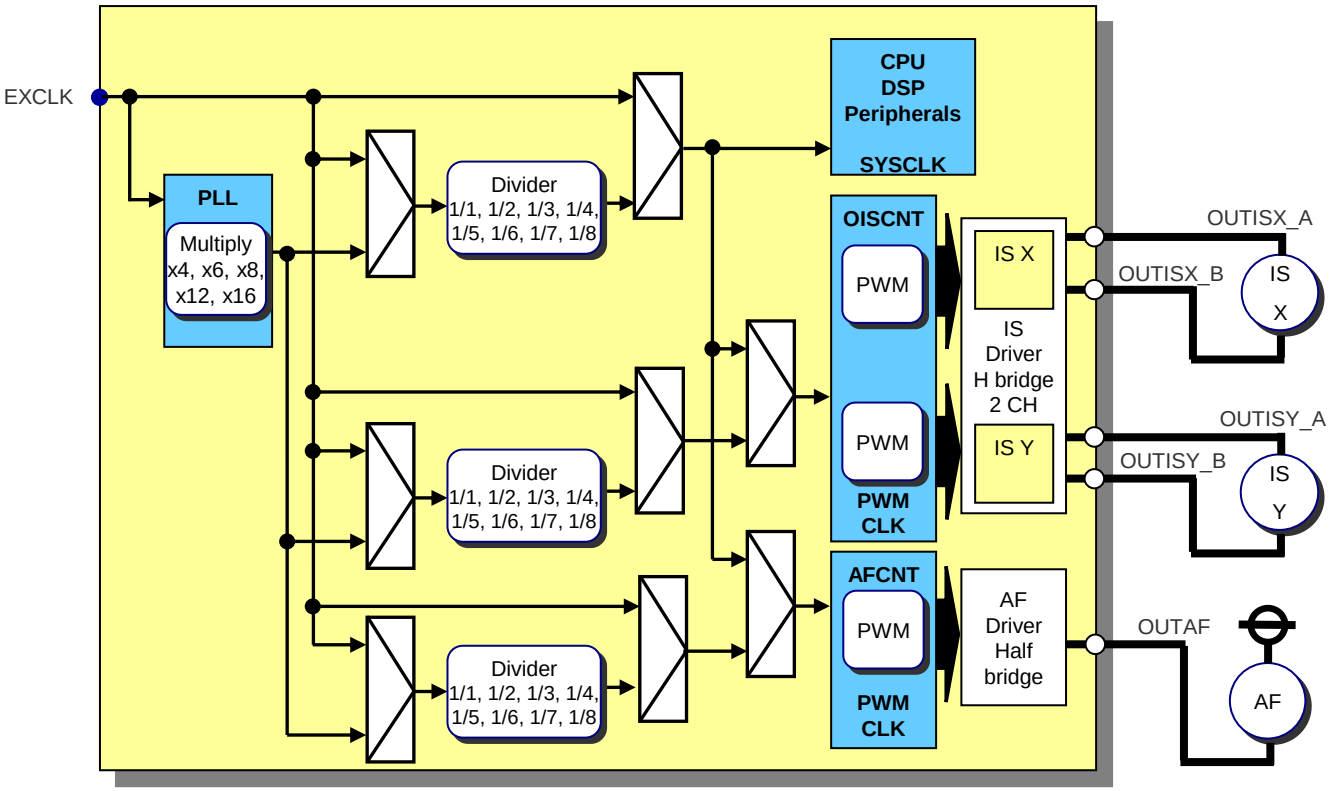
If not specified, VDD=1.8V VCC=VM=2.8V Ta=25 degrees C

Items	Symbol	Conditions	Limit		Unit	Remarks
			Min	Max		
data output delay SPI_DAT (SPI_MOSI)	td_spi_dat (SPI_SCK)	-	-	100	ns	(1)

Note(1): This specification is Design assurance value.



Clock Mode



Example of frequency setting (SYSCLK/PWMCLK)

EXCLK	PLL		Clock Divider							
Frequency[MHz]	Multiply	Frequency[MHz]	1	1/2	1/3	1/4	1/5	1/6	1/7	1/8
6	1	6	6.00	3.00	2.00	1.50	1.20	1.00	0.86	0.75
6	4	24	24.00	12.00	8.00	6.00	4.80	4.00	3.43	3.00
6	6	36	36.00	18.00	12.00	9.00	7.20	6.00	5.14	4.50
6	8	48	48.00	24.00	16.00	12.00	9.60	8.00	6.86	6.00
6	12	72	72.00	36.00	24.00	18.00	14.40	12.00	10.29	9.00
6	16	96	96.00	48.00	32.00	24.00	19.20	16.00	13.71	12.00
24	1	24	24.00	12.00	8.00	6.00	4.80	4.00	3.43	3.00
24	4	96	96.00	48.00	32.00	24.00	19.20	16.00	13.71	12.00
24	6	144	144.00	72.00	48.00	36.00	28.80	24.00	20.57	18.00
27	1	27	27.00	13.50	9.00	6.75	5.40	4.50	3.86	3.38
27	4	108	108.00	54.00	36.00	27.00	21.60	18.00	15.43	13.50
27	6	162	162.00	81.00	54.00	40.50	32.40	27.00	23.14	20.25
29	1	29	29.00	14.50	9.67	7.25	5.80	4.83	4.14	3.63
29	4	116	116.00	58.00	38.67	29.00	23.20	19.33	16.57	14.50

SYSCLK/PWMCLK supported. [MHz]

PWMCLK supported. [MHz]

Note ; PLL Lock in time = 500uS (max)

Example of PWM carrier frequency *1

(1) VCM mode carrier frequency [kHz] (PWM period=10bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162	158.4	316.7	633.4	1266.9	2533.7
144	140.8	281.5	563.0	1126.1	2252.2
116	113.4	226.8	453.6	907.1	1814.3
106	103.6	207.2	414.5	828.9	1657.9
96	93.8	187.7	375.4	750.7	1501.5

(2) VCM mode carrier frequency [kHz] (PWM period=11bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162	79.1	158.3	316.6	633.1	1266.2
144	70.3	140.7	281.4	562.8	1125.5
116	56.7	113.3	226.7	453.3	906.7
106	51.8	103.6	207.1	414.3	828.5
96	46.9	93.8	187.6	375.2	750.4

(3) VCM mode carrier frequency [kHz] (PWM period=12bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162	39.6	79.1	158.2	316.5	633.0
144	35.2	70.3	140.7	281.3	562.6
116	28.3	56.7	113.3	226.6	453.2
106	25.9	51.8	103.5	207.1	414.2
96	23.4	46.9	93.8	187.5	375.1

(4) PIEZO mode carrier frequency [kHz] (PWM period=10bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162	158.4	316.7	633.4	1266.9	2533.7
144	140.8	281.5	563.0	1126.1	2252.2
116	113.4	226.8	453.6	907.1	1814.3
106	103.6	207.2	414.5	828.9	1657.9
96	93.8	187.7	375.4	750.7	1501.5

(5) PIEZO mode carrier frequency [kHz] (PWM period=11bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162		158.3	316.6	633.1	1266.2
144		140.7	281.4	562.8	1125.5
116		113.3	226.7	453.3	906.7
106		103.6	207.1	414.3	828.5
96		93.8	187.6	375.2	750.4

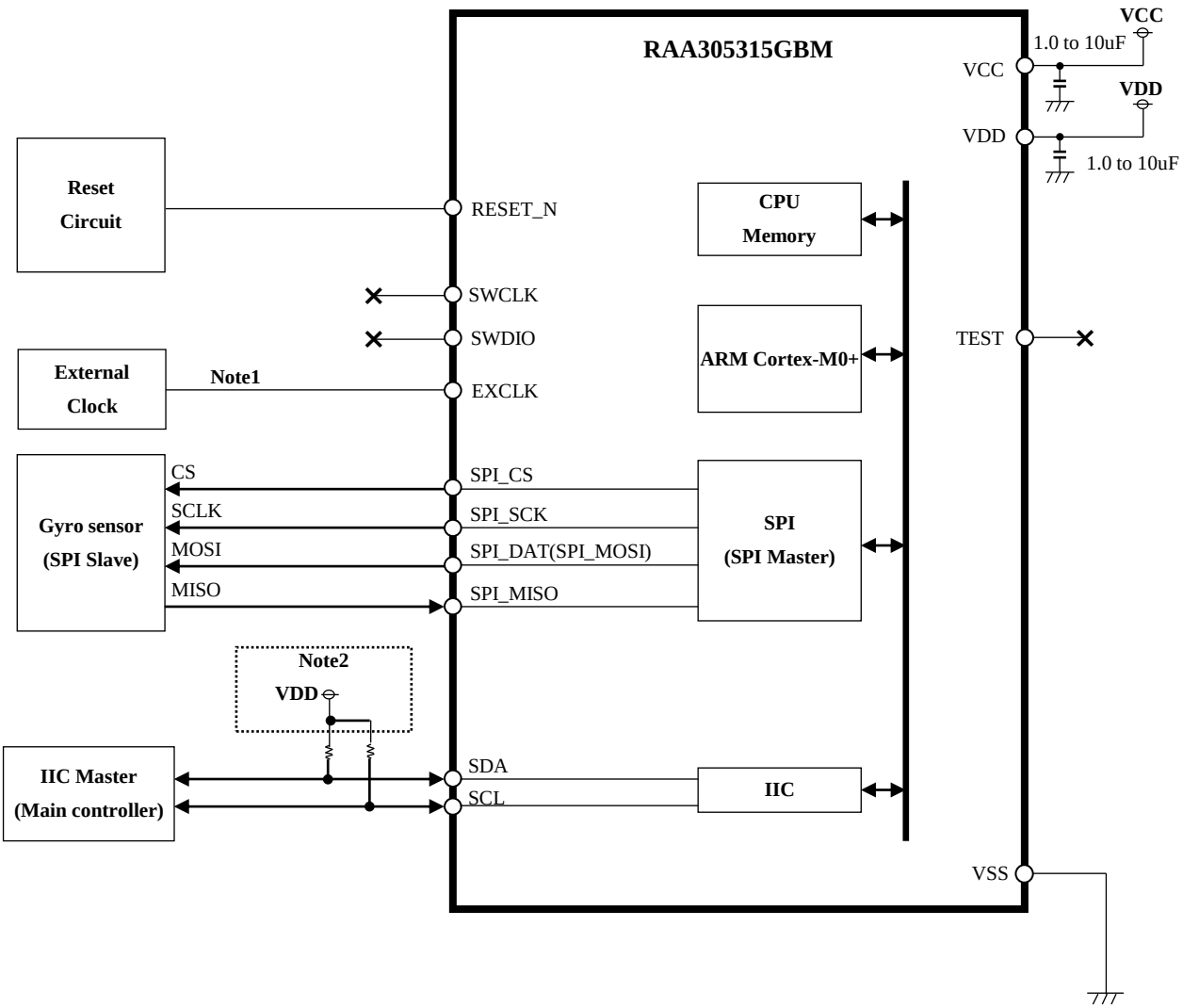
(6) PIEZO mode carrier frequency [kHz] (PWM period=12bit)

PWMCLK Frequency[MHz]	High-resolution bit number				
	0	1	2	3	4
162			158.2	316.5	633.0
144			140.7	281.3	562.6
116			113.3	226.6	453.2
106			103.5	207.1	414.2
96			93.8	187.5	375.1

*1 Since the value of PWM carrier frequency is a simple calculated value of a PWM circuit, it is necessary to take the driver characteristic into consideration at the time of use.

Example circuit for Controller block

Recommended circuit connection with normal mode

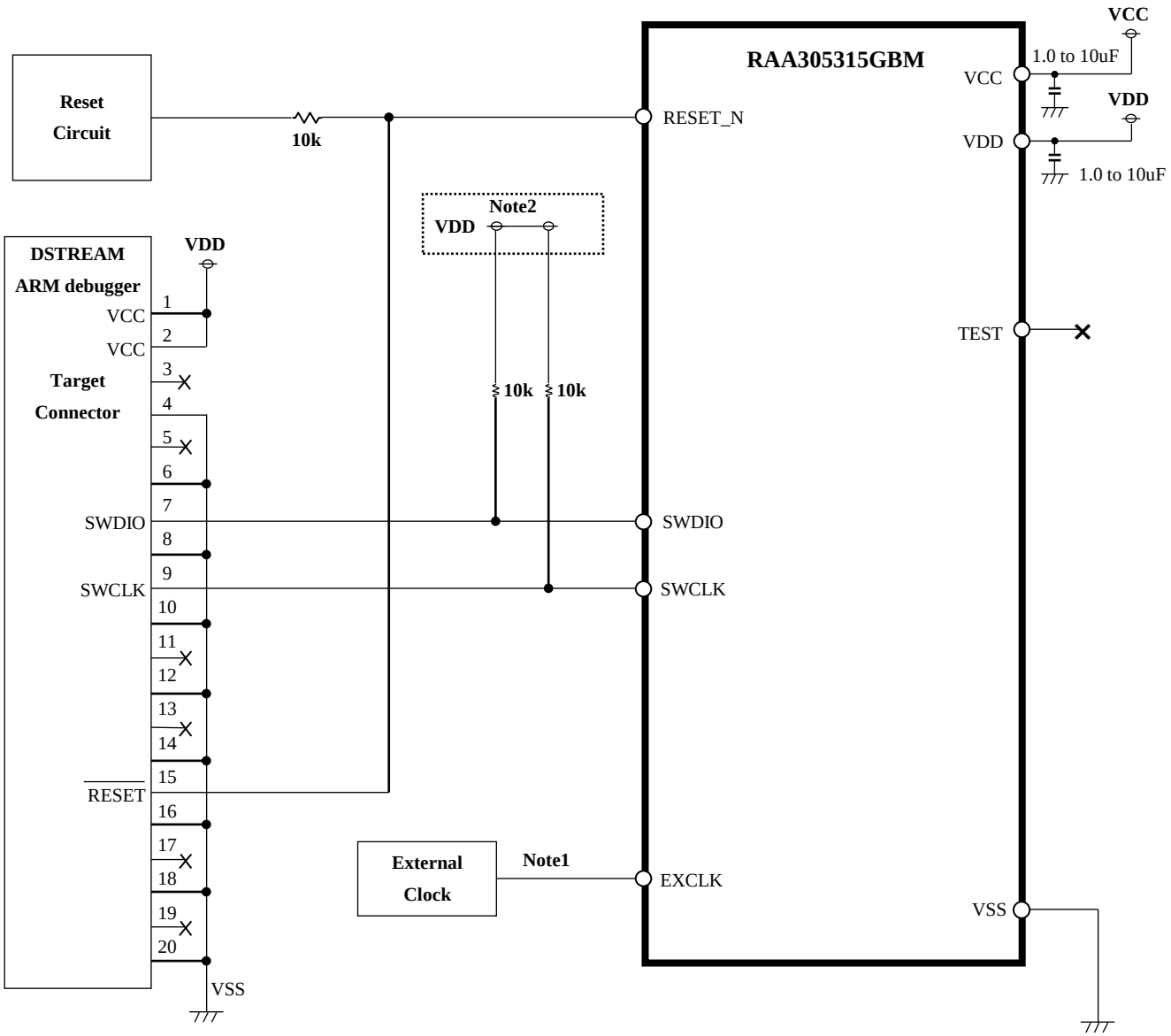


Note1. When IS driver using PWM mode, EXCLK clock source must use base clock of Image sensor.
If not use PWM mode, not need use base clock of Image sensor.

2. It is necessary to make the same the power supply (VDD) for IIC lines(SDA, SCL),
and the power supply(VDD) for RAA305315GBM.

Example circuit for Controller block (Debug mode)

Recommended circuit connection to DSTREAM(ARM debugger) with debug mode



Note1. When IS driver using PWM mode, EXCLK clock source must use base clock of Image sensor.
If not use PWM mode, not need use base clock of Image sensor.

2. It is necessary to make the same the power supply (VDD) for debugger lines(SWDIO, SWCLK), and the power supply(VDD) for RAA305315GBM.

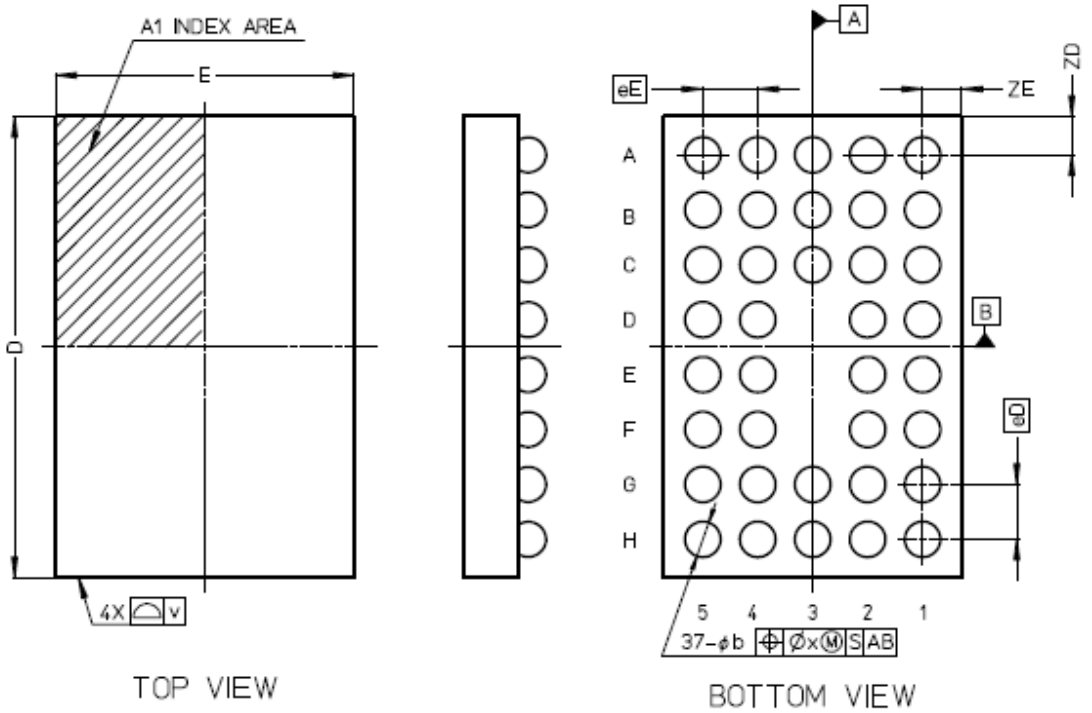
外形図　Outline Drawing (SWBG0037LA-A)

RDK-G-001024-1　1/1

ルネサス エレクトロニクス株式会社
Renesas Electronics Corporation

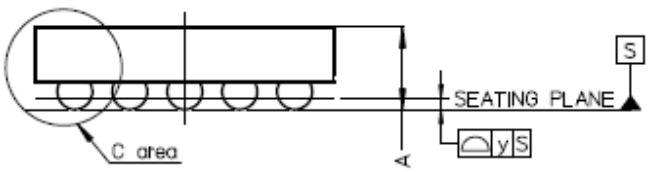
JEITA Package code	RENESAS Code	Previous Code	MASS(TYP.)[g]
S-WFBGA37-2.17x3.36-0.40	SWBG0037LA-A	—	0.01

Unit : mm

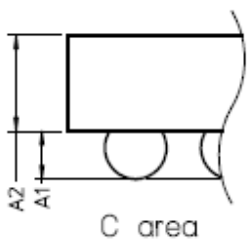


TOP VIEW

BOTTOM VIEW



SIDE VIEW

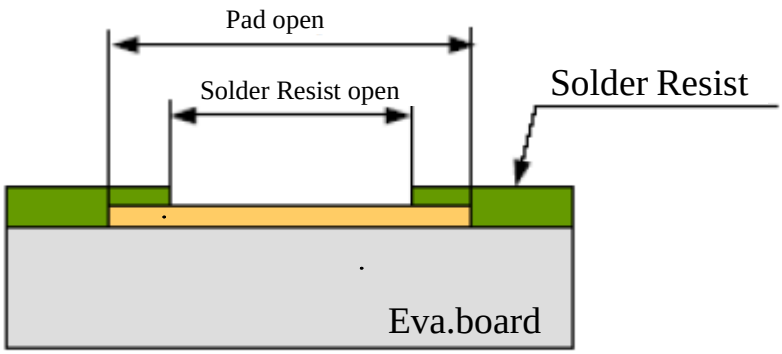


C area

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	3.31	3.36	3.41
E	2.12	2.17	2.22
ZD	0.23	0.28	0.33
ZE	0.235	0.285	0.335
A	—	—	0.70
A1	0.16	0.20	0.24
A2	0.36	0.40	0.44
b	0.21	0.26	0.31
eD	—	0.4	—
eE	—	0.4	—
v	—	—	0.05
x	—	—	0.05
y	—	—	0.08

Recommended Land Pattern(WLBGA)

Solder Resist open size: Φ0.22mm
Pad open size: Φ0.32mm



SMD type

Revision History

Rev	Date	Description	
		Page	Summary
Rev 1.06	9th. Dec. 2020	-	New

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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