1. INTRODUCTION

1.1 Features

- **Common**
  - 3-series to 10-series Cell Fuel Gauge IC (FGIC)
  - RL78 Ultra Low Power MCU (S3 core)
- **Memory**
  - Code flash memory: 64KB
  - Data flash memory (up to 100,000 erase/write cycles): 4KB
  - SRAM / 4KB
- **Clock generator**
  - High speed on-chip oscillator: up to 32 MHz
  - Low speed on-chip oscillator: 15 KHz
  - AFE on-chip oscillator: 4.19 MHz
  - AFE low speed on-chip oscillator: 131.072 KHz
- **General Purpose I/O Ports**
  - Total: 15 pins
  - CMOS input/output: 6
  - CMOS input: 2
  - N-ch open drain input/output [6.5V tolerance]: 2
  - N-ch open drain input/output [VREG2 tolerance]: 2
  - High voltage input/output [VCC tolerance]: 3
- **Serial Interface**
  - CSI (SPI): 1 channel
  - I2C: 1 channel
  - UART: 2 channels
  - Simplified I2C: 1 channel
- **Timer**
  - MCU 16-bit timer: 5 channels
  - MCU 12-bit interval timer: 1 channel
  - AFE timer: 2 channels
    - AFE timer A: setting range: 125 msec to 64 sec
    - AFE timer B: setting range: 30.52 usec to 2 sec
- **Embedded A/D converter**
  - AFE 15-bit resolution delta-sigma A/D converter
- **Current measurement circuit**
  - AFE 18-bit resolution delta-sigma A/D converter
- **Battery cell voltage and temperature (AN port voltage) detection circuit**
  - Monitoring over/under voltage and temperature by sigma-delta A/D converter (AFE) without controlling from MCU
- **Impedance measurement circuit**
  - Simultaneous measurement of battery voltage and current
- **Over current detection circuit**
  - Short circuit: 1 filter
  - Discharge over current: 4 filters
  - Charge over current: 1 filter
  - Charge wakeup: 1 filter
  - Discharge wakeup: 1 filter
- **Series regulator**
  - 3.3 V output (> 20mA)
- **Charge and Discharge MOSFETs control**
  - Low side N-ch Dual MOSFETs drive circuit embedded
  - Support individual FET control
- **Ultra Low Power consumption mode**
  - Power down mode: 1uA
  - Power down mode with PON timer: 2uA
  - Sleep mode 1: 25uA (DFET and CFET off)
  - Sleep mode 2: 40uA (DFET and CFET on)
  - In Sleep mode 2, enable all H/W protection function
- **Additional features**
  - Internal Cell Balancing Circuit (>10mA)
  - Internal Watchdog Timer (MCU)
  - MCU Runaway Detection Circuit (AFE)
  - 4 Thermistor Sensor Ports with On-chip Pull-up Resistors
  - Integrated Hardware Diagnostics function
  - Load detection circuit
  - Random cell connection tolerant
- **Voltage and temperature condition**
  - Power supply voltage: VCC = 8.0 to 50V
  - Operating Ambient Temperature: Ta = -40°C to 85°C
- **Package information**
  - 40pin QFN Package ([Body] 5 mm x 5 mm, 0.4 mm pitch)

1.2 Applications

- Vacuum cleaner, Handheld equipment, Power Tool, E-bike, UPS, Power bank

1.3 Description

RAJ240310 is Renesas Li-ion battery fuel gauge IC (FGIC) which consists of a MCU device and an AFE device in a single package. Pack with a variety of battery management features and Renesas RL78 CPU core which has multiple low power modes and capable of achieving high performance in ultra-low power operation.
The RAJ240310 has embedded flash memory on an MCU (same as other RL78 family) and use it to store program instructions (code) as well as data on to perform battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

Table of Contents

2. OUTLINE

2.1 Outline of Functions

(1/2)

Item		Description
Code flash memory		64 KB
Data Flash memory		4 KB
RAM		4 KB
Address size		1MB
Main system clock	High speed on-chip Oscillator clock(fIH)	HS (high-speed main) mode: 1 to 32 MHz LS (low-speed main) mode: 1 to 8 MHz,
Low speed on-chip oscillator clock		15 kHz (TYP.)
General purpose register		8 bits × 32 registers (8 bits × 8 registers × 4 banks)
Minimum instruction execution time		0.03125 usec (Internal high-speed oscillation clock: fIH = 32 MHz)
Instruction set		• Data transmission (8/16 bits) • Addition and subtraction/logical operations (8/16 bits) • Multiplication (8×8 bits,16×16 bits), Division (16÷16 bits,32÷32 bits) • Multiplication and Accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, bit manipulation (set, reset, test, Boolean operation) etc.
I/O Port	CMOS I/O	6
	CMOS input	2
	N-ch open-drain I/O [6.5V tolerance]	2
	N-ch open-drain I/O [VREG2 tolerance]	2
	High voltage I/O	3
Timer	16-bit timer	5 channels (TAU: 4 channels, Timer RD：1 channels)
	Watchdog timer	1 channel
	12-bit interval timer	1 channel
	Timer output	Timer outputs: 3 channels PWM outputs: 3 channels
Serial interface		• CSI: 1 channel/UART: 2 channel/simplified I2C: 1 channel
	I^2C bus	1 channel
Vector interrupt source	Internal	16
	External	9 (7 sources are connected to AFE in the chip)
Reset		・Reset by RESET pin (reset circuit output of AFE connected to RESETOUT) ・Internal reset by watchdog timer ・Internal reset by illegal instruction execution Note ・internal reset by RAM parity error ・internal reset by illegal memory access
On-chip debug function		Support

Note The illegal instruction execution is generated when instruction code FFH is executed. Reset by the illegal instruction execution is not issued by emulation with the in-circuit emulator or on-chip debug emulator.

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Item	Description
Sigma-delta A/D converter	15-bit resolution (sigma-delta method) • Battery Cell voltage • Battery Cell total voltage (VIN10 or VIN9 pin) • PONL pin input voltage • Thermistor sensor port with on-chip pull-up 15 KΩ resistor: 4 channels • On-chip simple temperature sensor (temperature range: -40 to 85C) • Internal reference and supply voltage (AFE)
Battery cell voltage and temperature (AN port voltage) detection circuit	Battery Cell voltage detection • Over voltage (Overcharge voltage) • Under voltage (Overdischarge voltage) Temperature (AN port voltage) detection • Charge/Discharge Over temperature • Charge/Discharge Under temperature
Current integrating circuit	1 channel:18-bit resolution
Current integrating circuit for impedance measurement	1 channel:15-bit resolution
Overcurrent detection circuit and wake up current detection circuit	• Discharge short-circuit current detection • Discharge overcurrent detection • Charge overcurrent detection, • Wake up current detection (discharge and charge)
Simple temperature sensor	1 channel
Charge/Discharge Low side FET control circuit	N-ch FET driver for charge control: 2 channels N-ch FET driver for discharge control: 2 channels
Power on reset	Return from power down mode by either of following factors 1. PONL low edge 2. Internal timer (Pon timer) overflow
Series regulator	VREG2: power supply for MCU (3.3 V)
Reset circuit	Series regulator output monitoring (VREG2)
Cell balancing circuit	Support 10 series cells (On-resistor: 200 Ω TYP)
MCU runaway detection circuit	20 bits×1(2 / 4 / 8 / 16 / 32 / 64 [s] to be selected)
AFE On-chip oscillator	4.194 MHz (TYP)
AFE low speed On-chip oscillator	131.072KHz (TYP)
AFE timer	2 channels • AFE timer A (setting range：125 ms to 64 s) • AFE timer B (setting range：30.52 usec to 2 s)
Load detection	Detect load presence
MCU-AFE communication interface(C2C)	AFE to MCU communication (Chip to Chip Interface)
Power supply voltage	VCC = 8.0 to 50 V
Operation ambient temperature	-40 to 85°C
Package	40 pin plastic mold QFN ([Body] 5.0mm x 5.0mm, 0.4 mm pitch, 0.95 mm thickness)

2.2 Pin Configuration

40 pin plastic mold QFN ([Body] 5 mm x 5 mm, 0.4 mm pitch)

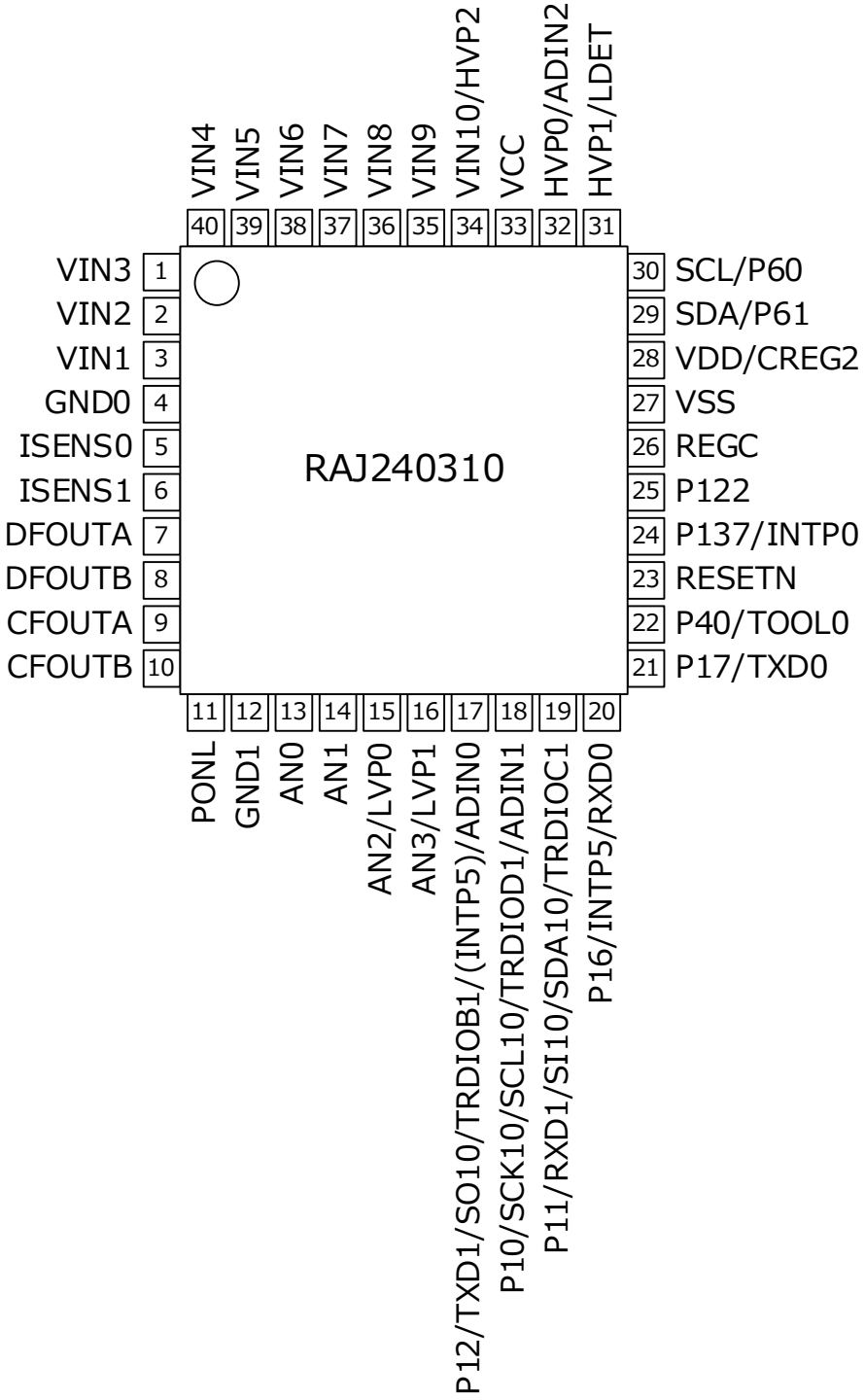

Figure 1 Pin configuration

Caution 1. **REGC pin connects to VSS pin through a capacitor (0.47 to 1.0 uF).**

Caution 2. **CREG2 pin connects to GND0/1 pin through a capacitor (1.0 to 4.7 uF).**

Remark Pin name refer to 3.1 Pin Identification.

3. PIN FUNCTIONS

3.1 Pin Identification

Table 1 Pin identification

No.	Name	Type	Description
1	VIN3	AIN	Battery voltage input
2	VIN2	AIN	Battery voltage input
3	VIN1	AIN	Battery voltage input
4	GND0	P	Device ground input. Connect the negative input pin of Lithium-ion battery 1 to GND0, GND1, and VSS
5	ISENS0	AIN	Analog input for current integration circuit
6	ISENS1	AIN	Analog input for current integration circuit
7	DFOUTA	HVO	Discharge MOS FET control channel A
8	DFOUTB	HVO	Discharge MOS FET control channel B
9	CFOUTA	HVO	Charge MOS FET control channel A
10	CFOUTB	HVO	Charge MOS FET control channel B
11	PONL	HVIN	High voltage port for power on, L=power on
12	GND1	P	Device ground input. Connect the negative input pin of Lithium-ion battery 1 to GND0, GND1, and VSS
13	AN0	AIN	Analog input for Thermistor (Primary)
14	AN1	AIN	Analog input for Thermistor (Secondary)
15	AN2 / LVP0	AIN	Analog input for Thermistor / GPIO (AFE)
16	AN3 / LVP1	AIN	Analog input for Thermistor / GPIO (AFE)
17	P12 / SO10 / TRDIOB1 / (INTP5) / TxD1 / ADIN0	DIO	Port1 / Serial Data Output / Timer Output / UART Transmit Data 1 / AD input
18	P10 / SCK10 / SCL10 / TRDIOD1 / ADIN1	DIO	Port1 / Serial Clock I/O / Simplified I2C clock I/O / Timer Output / AD input
19	P11 / SI10 / SDA10 / TRDIOC1 / RxD1	DIO	Port1 / Serial Data Input / Simplified I2C data I/O / Timer Output / UART Receive Data 1
20	P16 / RXD0 / INTP5	DIO	Port1 / UART Receive Data 0
21	P17 / TXD0	DIO	Port1 / UART Transmit Data 0
22	P40 / TOOL0	DIO	Port4 / Data input/output for Tool
23	RESETN	DIN	Reset input
24	P137 / INTP0	DIN	Port13 / External Interrupt Input
25	P122	DIN	Port12
26	REGC	P	Regulator Capacitance
27	VSS	P	Ground input for MCU. Connect the negative input pin of Lithium-ion battery 1 to GND0, GND1, and VSS
28	VDD/CREG2	P	Power Supply for MCU / Regulator output
29	SDA/P61	DIO	I2C Bus data I/O / Port61
30	SCL/P60	DIO	I2C Bus clock I/O / Port60
31	HVP1 / LDET	HVIO	High voltage I/O port / Load detection (High voltage AD input)
32	HVP0 / ADIN2	HVIO	High voltage I/O port / AD input
33	VCC	P	Power supply
34	VIN10 / HVP2	AIN	Battery voltage input / High voltage I/O port / High voltage AD input
35	VIN9	AIN	Battery voltage input
36	VIN8	AIN	Battery voltage input

37	VIN7	AIN	Battery voltage input
38	VIN6	AIN	Battery voltage input
39	VIN5	AIN	Battery voltage input
40	VIN4	AIN	Battery voltage input

HVO:	**High Voltage Output**	**DIO:**	**Digital I/O**
HVIN:	High Voltage Input	DIN:	Digital Input
HVIO:	High Voltage I/O	AIN:	Analog Input
P:	Power/Ground	AO:	Analog Output

3.2 Pin Functions

3.2.1 Pin type and alternate functions

Category	Pin Type	Function Name	I/O	After Reset Release	Alternate Function	Function
Internal Pin	7-1-3	P05	I/O	Input port	INTP10	Port 0. Note 1. 2-bit I/O port Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
	7-1-3	P06			INTP11	
External Pin	8-6-8-1 Note 3	P10	I/O	Input port	SCK10/SCL10/TRDIOD1	Port 1. 5-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. An input of P10, P16, P17 can be set to TTL input buffer. Output of P10, P11, P17 can be set to N-ch open-drain output (VREG2 tolerance).
	7-1-4	P11			SI10/SDA10/TRDIOC1/RxD1	
	7-3-3-1 Note 3	P12			SO10/TRDIOB1/(INTP5)/TxD1	
	8-6-6-1	P16			INTP5/RxD0	
	8-6-8-1	P17			TxD0	
Internal Pin	8-6-8-2	P30	I/O	Input port	INTP3	Port 3. Note 1. 2-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
	7-1-3	P31			INTP4	
External Pin	7-1-3	P40	I/O	Input port	TOOL0	Port 4. 1-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port. P40 also can be used for I/O of programmer and debugger.
External Pin	12-1-2	P60	I/O	Input port	SCLA0	Port 6. 2-bit I/O port. Input/output can be specified in 1-bit unit. Output of P60 to P61 can be set to N-ch open-drain output (6.5V tolerance).
	12-1-2	P61			SDAA0	
Internal Pin	7-1-3	P70	I/O	Input port	SCK21	Port 7. Note 1. 7-bit I/O port. Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
	7-1-4	P71			SI21	
	7-1-3	P72			SO21	
	7-1-3	P73			-	
	7-1-4	P74			INTP8	
	7-1-3	P75			INTP9	
	7-1-3	P76	I/O		INTP1	
External Pin	2-2-2	P122	input	Input port	-	Port 12. 1-bit input-only port.
External Pin	2-1-2	P137	input	Input port	INTP0	Port 13. 1-bit input-only port.
External Pin	2-1-1	RESETN	input	-	-	Input-only pin for external reset.
External Pin	AN2/LVP0 Note 2	LVP0	I/O	Input port	AN0	Port A 2-bit I/O port Input/output can be specified in 1-bit unit. Use of an on-chip pull-up resistor can be specified by a software setting at input port.
	AN3/LVP1 Note 2	LVP1	I/O	Input port	AN1	

Note 1. These are connected to AFE in the package.

Note 2. AN2 pin and AN3 pin are analog input pin. Refer to section 3.5.6.

Note 3. These pins also have analog function. Refer to section 3.5.9

3.2.2 External Pin Functions

(1/2)

Category	Pin name	I/O	Function
Power supply	VCC	–	Power supply input Apply power supply voltage to VCC pin from a charger or battery.
	GND0, GND1	–	Device ground input. Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	CREG2	–	Series regulator output
	VSS	–	Ground input for MCU Connect the negative input terminal of lithium-ion battery 1 to the GND0 pin
	REGC Note 1.	–	Pin for connecting regulator output stabilization capacitance for internal operation. Connect this pin to VSS via a capacitor (0.47 to 1 uF). Also, use a capacitor with good characteristics, since it is used to stabilize internal voltage.
RESET	RESETN	Input	This is the active-low system reset input pin for MCU.
TOOL0	TOOL0 Note 2	input	Data I/O for flash memory programmer/debugger. Connect to the VDD via an external pull-up resistor in the on-chip debug mode
Serial interface (UART0, UART1)	RxD0, RxD1	input	Serial data input pins of serial interface UART0 and UART1
	TxD0, TxD1	output	Serial data output pins of serial interface UART0 and UART1
Serial interface (CSI10)	SCK10	I/O	Serial clock I/O pins of serial interface CSI10
	SI10	input	Serial data input pins of serial interface CSI10
	SO10	output	Serial data output pins of serial interface CSI10
Serial interface (IIC10)	SCL10	output	Serial clock output pins of serial interface IIC10
	SDA10	I/O	Serial data I/O pins of serial interface IIC10
Serial interface (IICA0)	SCL (SCLA0)	I/O	Serial clock I/O pins of serial interface IICA0
	SDA (SDAA0)	I/O	Serial data I/O pins of serial interface IICA0,
A/D converter	AN0 to AN3 ADIN0 to ADIN2	input	AFE A/D converter analog input
Current integration circuit and overcurrent detection circuit	ISENS0, ISENS1	input	Analog input for current integration circuit and over current detection circuit
Timer	TRDIOB1 TRDIOC1 TRDIOD1	I/O	Timer RD input/output
High voltage I/O port	HVP0, HVP1, HVP2	I/O	High voltage I/O in correspondence with VCC tolerance HVP1 has load detection function HVP0 can be used as AD input HVP1 and HVP2 can be used as high voltage AD inputs
External interrupt input	INTP0, INTP1, INTP3 to INTP5 INTP8 to INTP11	input	Interrupt request input pin. Only INTP0 and INTP5 pins are connected to the external pin. INTP1, INTP3, INTP4, and INTP8 to INTP11 connect interrupt request signal of AFE in the package and do not connect to any pin
Power on circuit	PONL	input	Power on input for release from power down state (Detect low edge)
Cell voltage input	VIN10	input	The positive input terminal of lithium-ion battery 10.
	VIN9	Input	The negative input terminal of lithium-ion battery 10 and the positive input terminal of lithium-ion battery 9
	VIN8	Input	The negative input terminal of lithium-ion battery 9 and the positive input terminal of lithium-ion battery 8
	VIN7	Input	The negative input terminal of lithium-ion battery 8 and the positive input terminal of lithium-ion battery 7
	VIN6	Input	The negative input terminal of lithium-ion battery 7 and the positive input terminal of lithium-ion battery 6
	VIN5	Input	The negative input terminal of lithium-ion battery 6 and the positive input terminal of lithium-ion battery 5
	VIN4	Input	The negative input terminal of lithium-ion battery 5 and the positive input terminal of lithium-ion battery 4
	VIN3	Input	The negative input terminal of lithium-ion battery 4 and the positive input terminal of lithium-ion battery 3
	VIN2	Input	The negative input terminal of lithium-ion battery 3 and the positive input terminal of lithium-ion battery 2
	VIN1	Input	The negative input terminal of lithium-ion battery 2 and the positive input terminal of lithium-ion battery 1

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Category	Pin name	I/O	Function
FET control output	DFOUT A	Output	ON/OFF signal output pin for discharge FET channel A
	DFOUT B	Output	ON/OFF signal output pin for discharge FET channel B
	CFOUT A	Output	ON/OFF signal output pin for charge FET channel A
	CFOUT B	Output	ON/OFF signal output pin for charge FET channel B
Communication between AFE and MCU	P73	Input	Control signal of communication between AFE and MCU
	SCK21	Output	Clock signal of communication between AFE and MCU
	SI21	Output	Data signal (From MCU to AFE) communication between AFE and MCU
	SO21	Input	Data signal (From AFE to MCU) communication between AFE and MCU

Note 1. REGC is not external power supply pin. (Do not draw current from REGC.)

Note 2. After reset release, the connection between P40/TOOL0 and the operating mode are as follows.

Table 3-2 TOOL0 Pin Operation Mode after Reset Release

P40/TOOL0	Operation Mode
VDD	Normal operation mode
0V	Flash memory programming mode

3.3 Unused Pins Connection

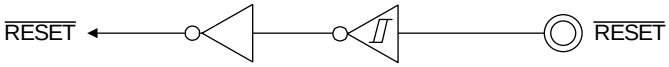
Table 3-3 Unused Pins connection

Pin Name	Recommended Connection of Unused Pins
P10-P12, P16, P17	Input: Independently connect to CREG2 or VSS via a resistor. Output: Leave open.
P40/TOOL0	Input: Independently connect to CREG2 or VSS via a resistor. Output: Leave open.
P122	Input: Independently connect to CREG2 or VSS via a resistor.
P137	Input: Independently connect to CREG2 or VSS via a resistor.
HVP0-2	Leave open.
AN0-AN3	Leave open.
DFOUTA, DFOUTB	Leave open
CFOUTA, CFOUTB	Leave open.
VIN10-VIN4	Connect input pin to positive terminal of top cell.
ISENS1, ISENS0	Connect to GND 0 or GND1.

3.4 MCU Pin Block Diagram

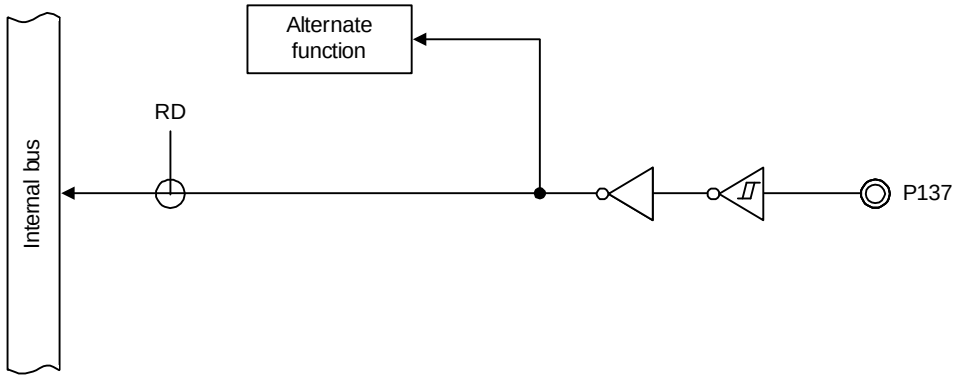
3.4.1 Type 2-1-1

Figure 3-1 Pin Block Diagram of Pin type 2-1-1



3.4.2 Type 2-1-2

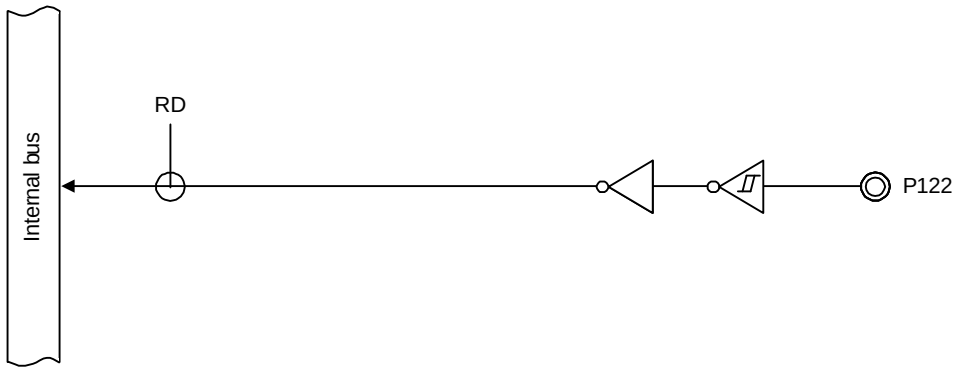
Figure 3-2 Pin Block Diagram of Pin type 2-1-2



Remark Refer to section 3.2.1for alternate functions.

3.4.3 Type 2-2-2

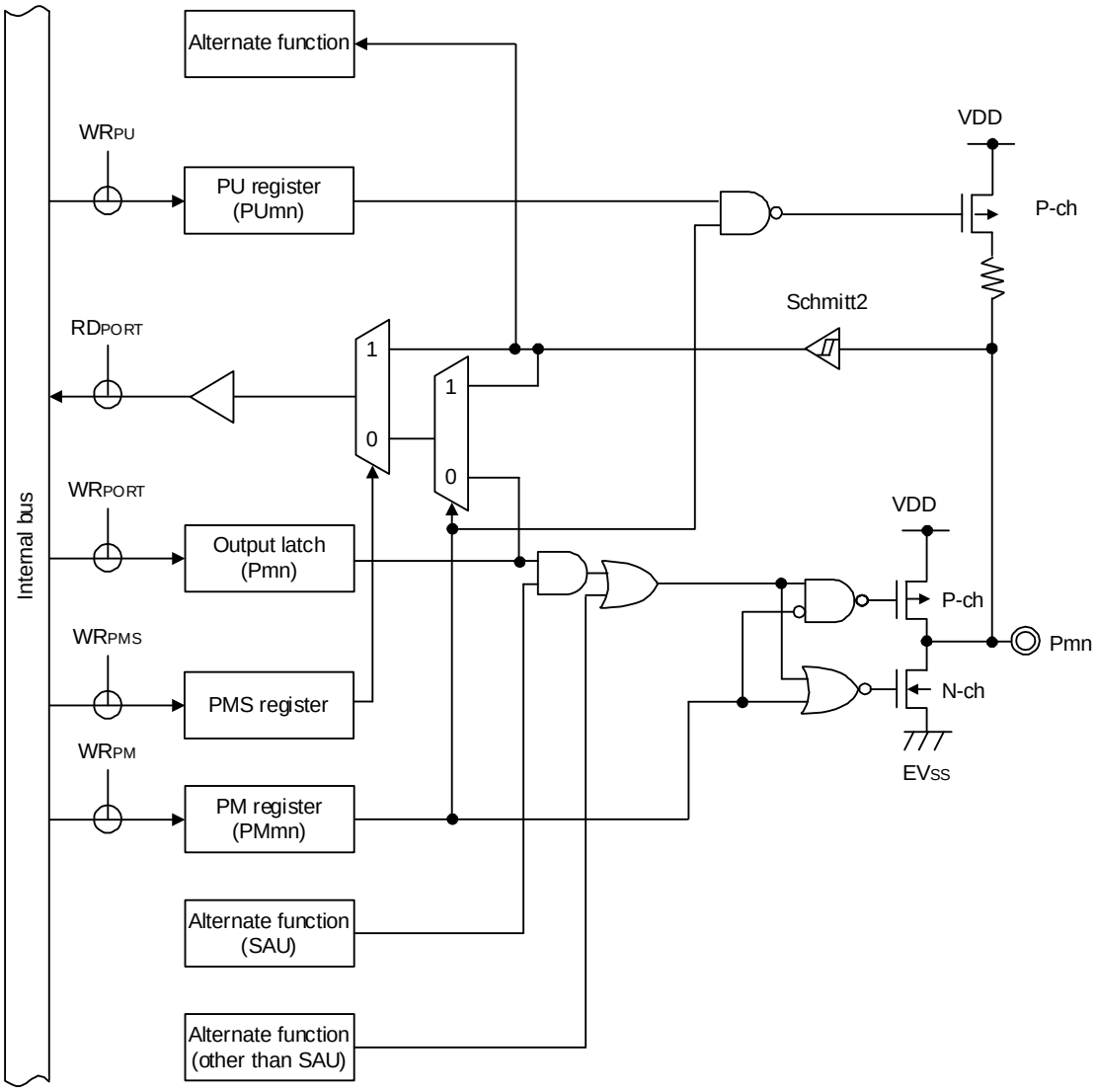
Figure 3-3 Pin Block Diagram of Pin type 2-2-2



Remark Refer to section 3.2.1for alternate functions.

3.4.4 Type 7-1-3

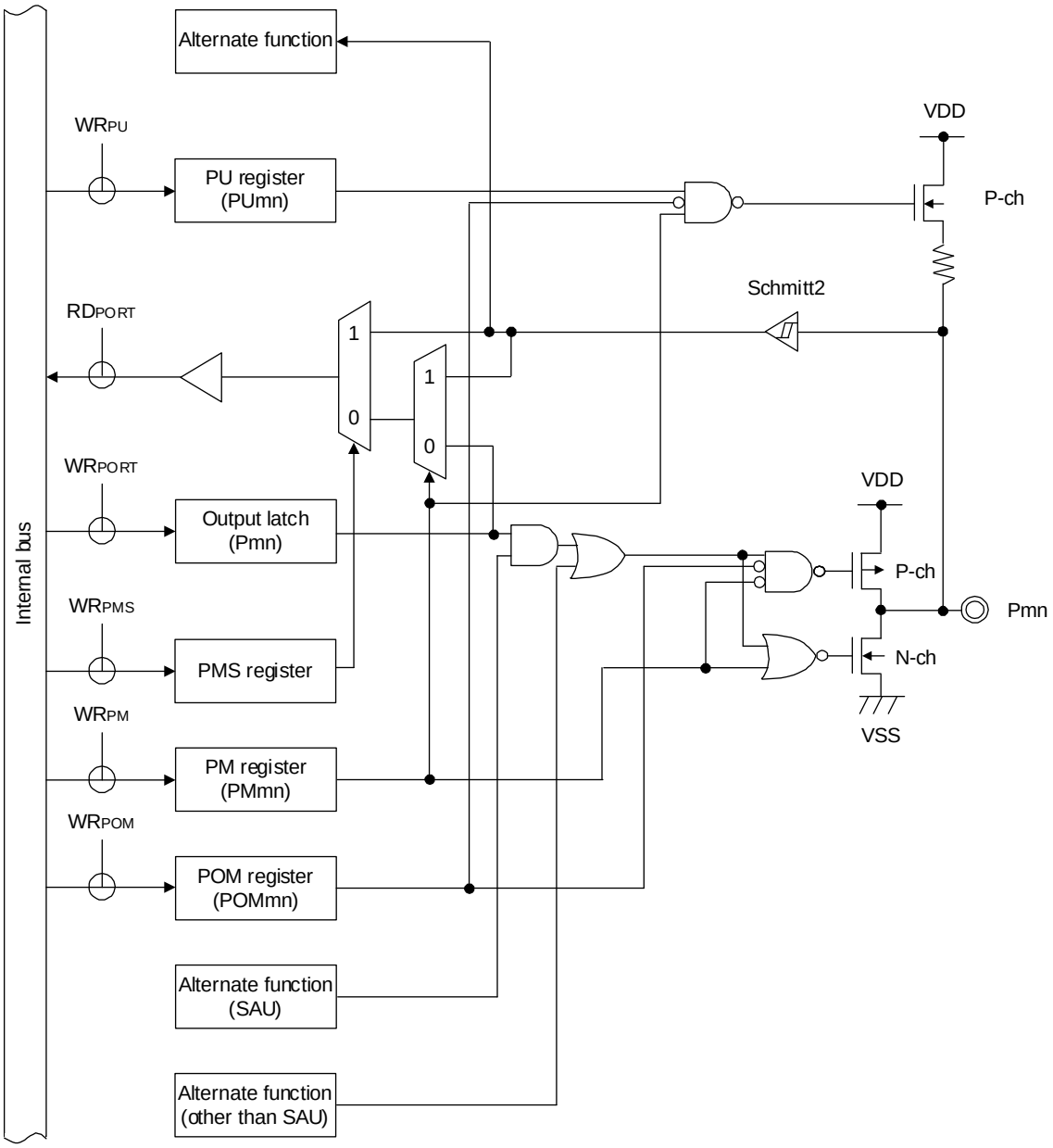
Figure 3-4 Pin Block Diagram of Pin type 7-1-3



Remark Refer to section 3.2.1for alternate functions.

3.4.5 Type 7-1-4

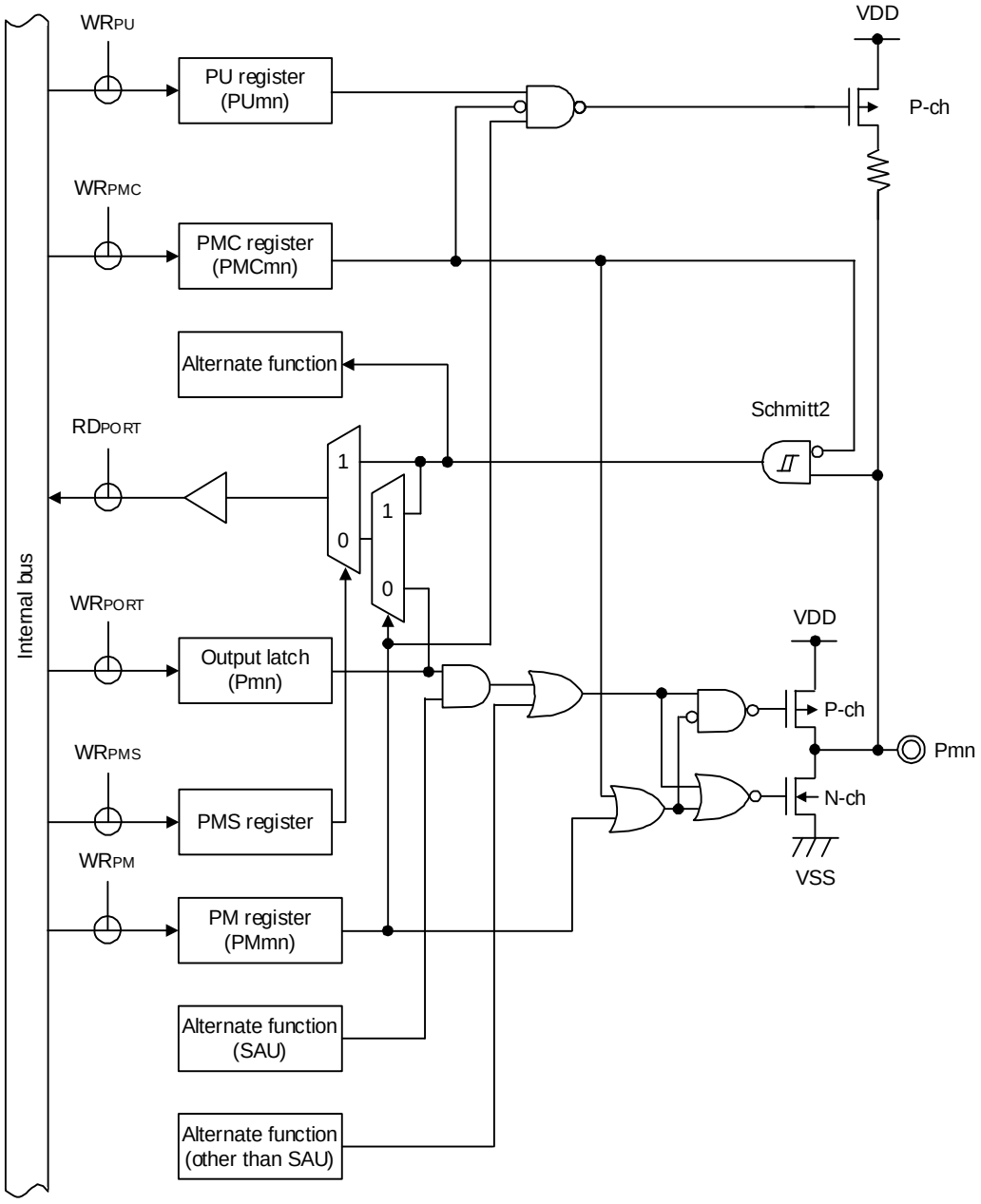
Figure 3-5 Pin Block Diagram of Pin type 7-1-4



Remark Refer to section 3.2.1for alternate functions.

3.4.6 Type 7-3-3-1

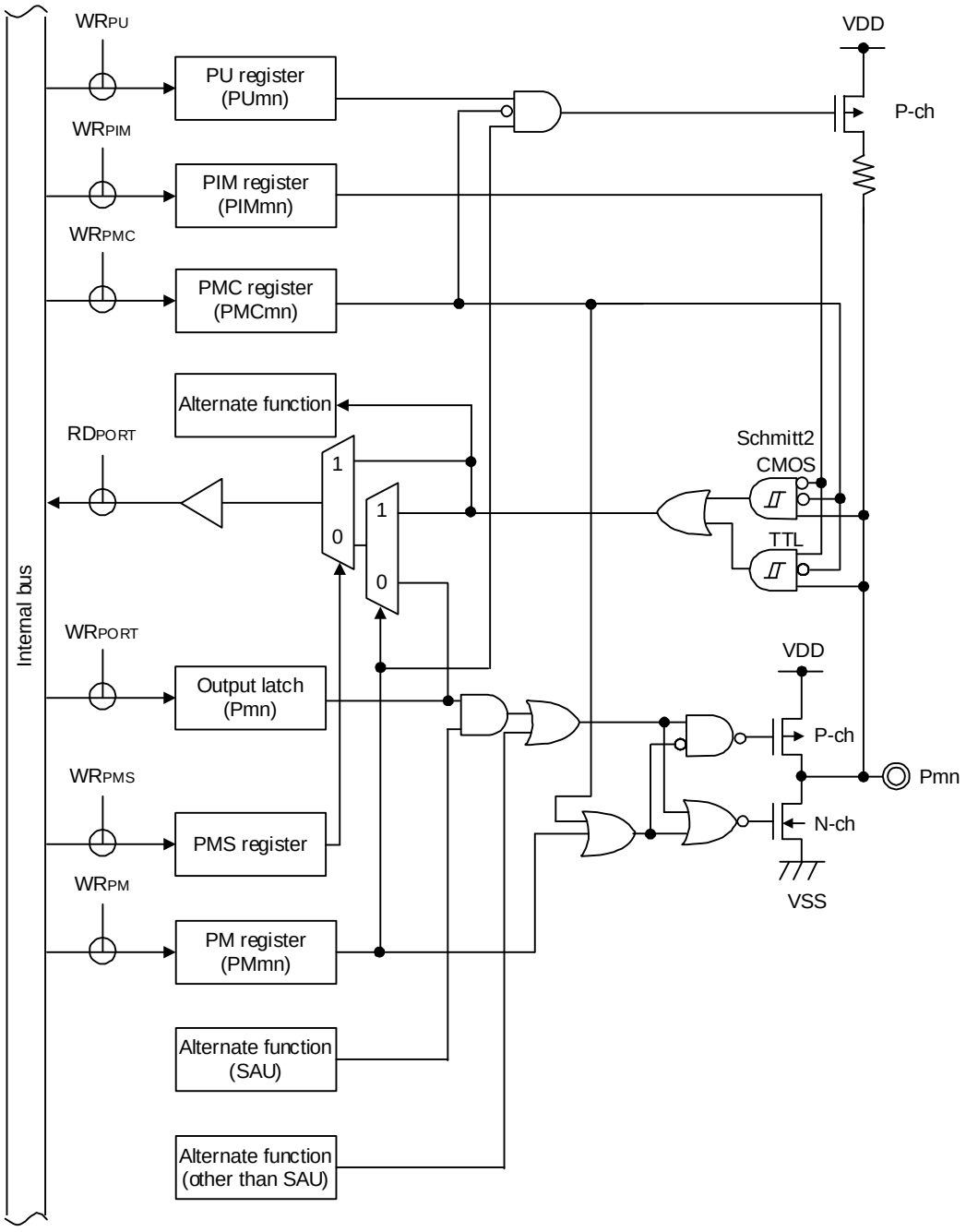
Figure 3-6 Pin Block Diagram of Pin type 7-3-3-1



Remark Refer to section 3.2.1for alternate functions.

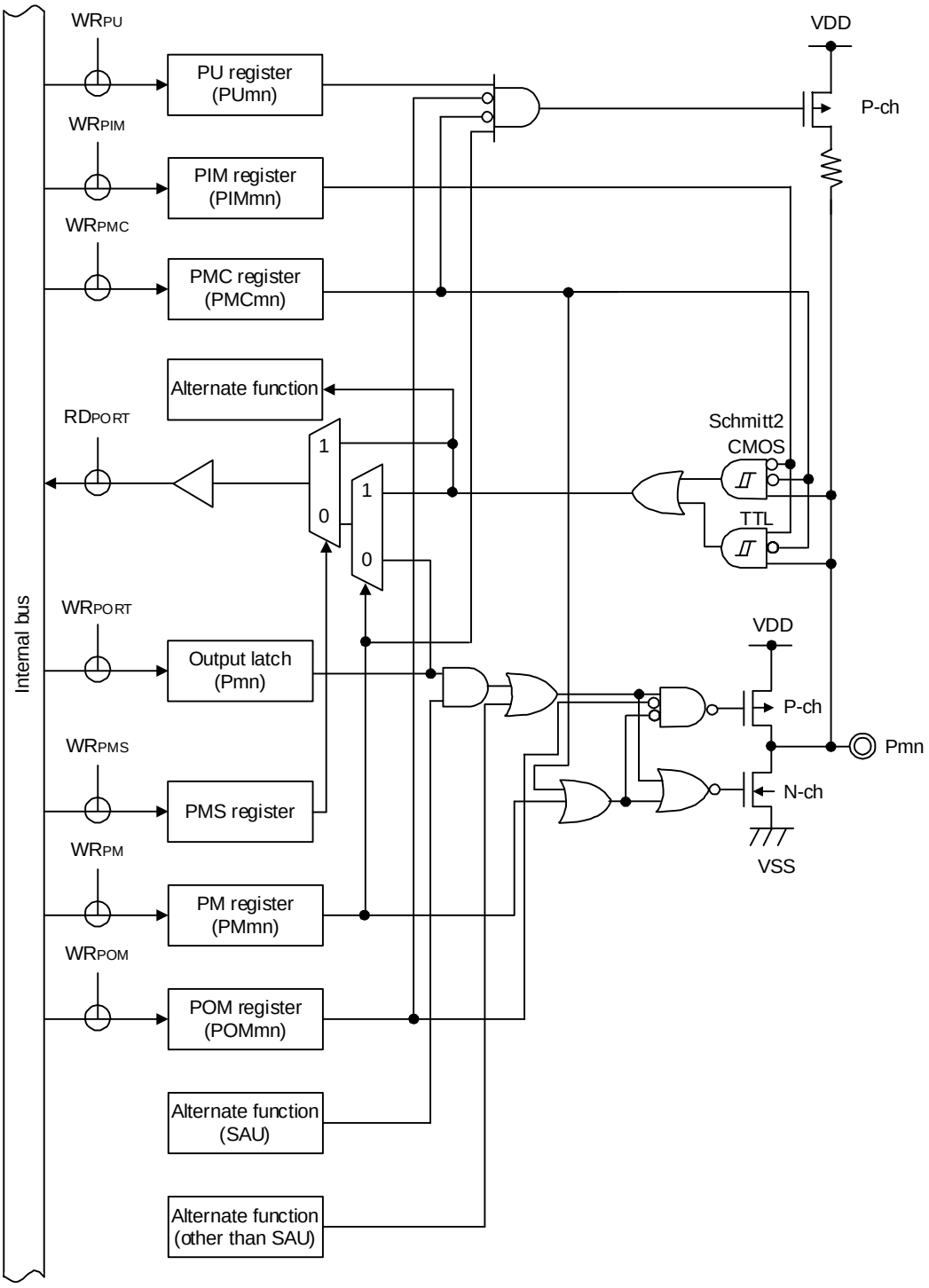
3.4.7 Type 8-6-6-1

Figure 3-7 Pin Block Diagram of Pin type 8-6-6-1



3.4.8 Type 8-6-8-1

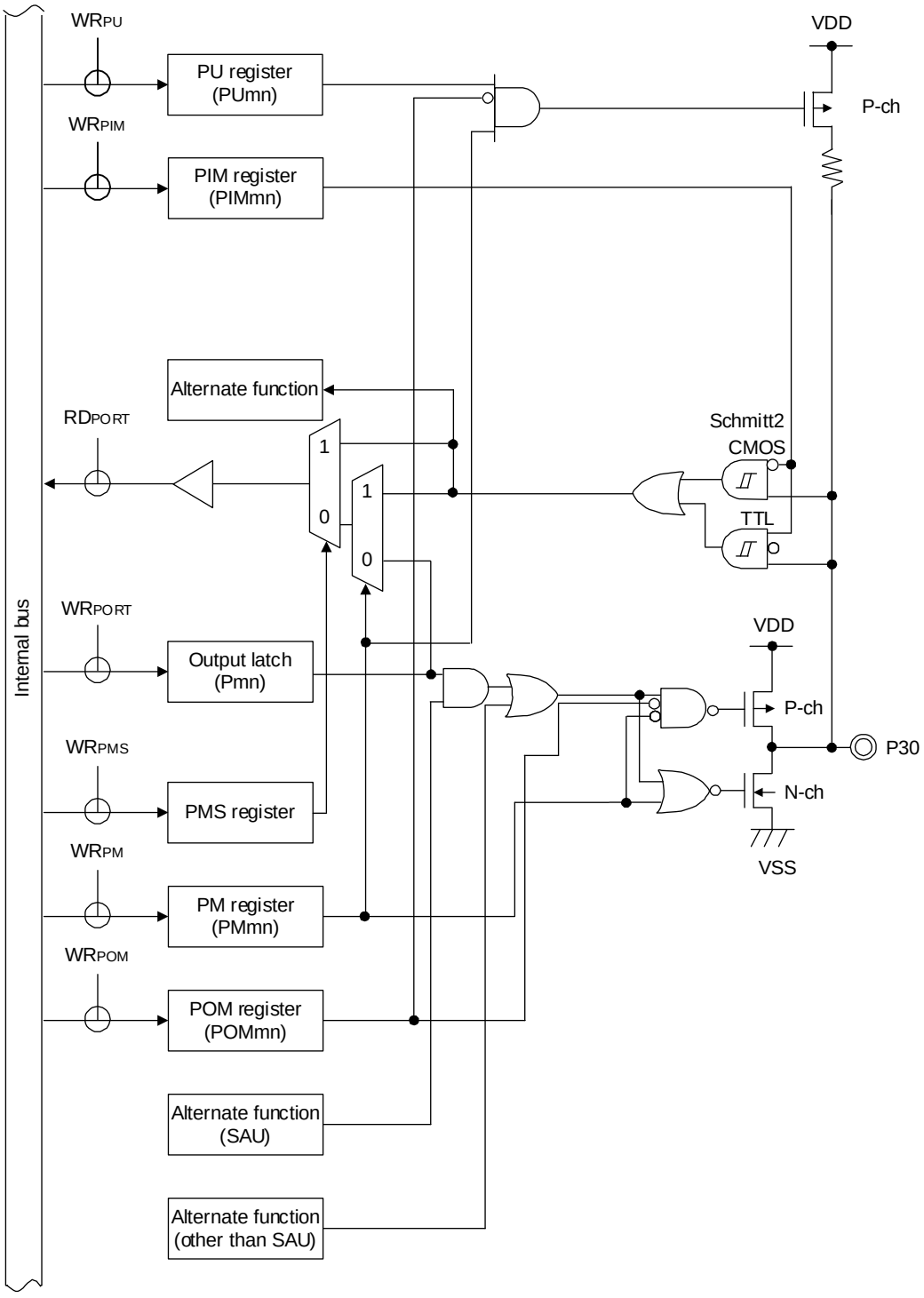
Figure 3-8 Pin Block Diagram of Pin type 8-6-8-1



Remark Refer to section 3.2.1for alternate functions.

3.4.9 Type 8-6-8-2

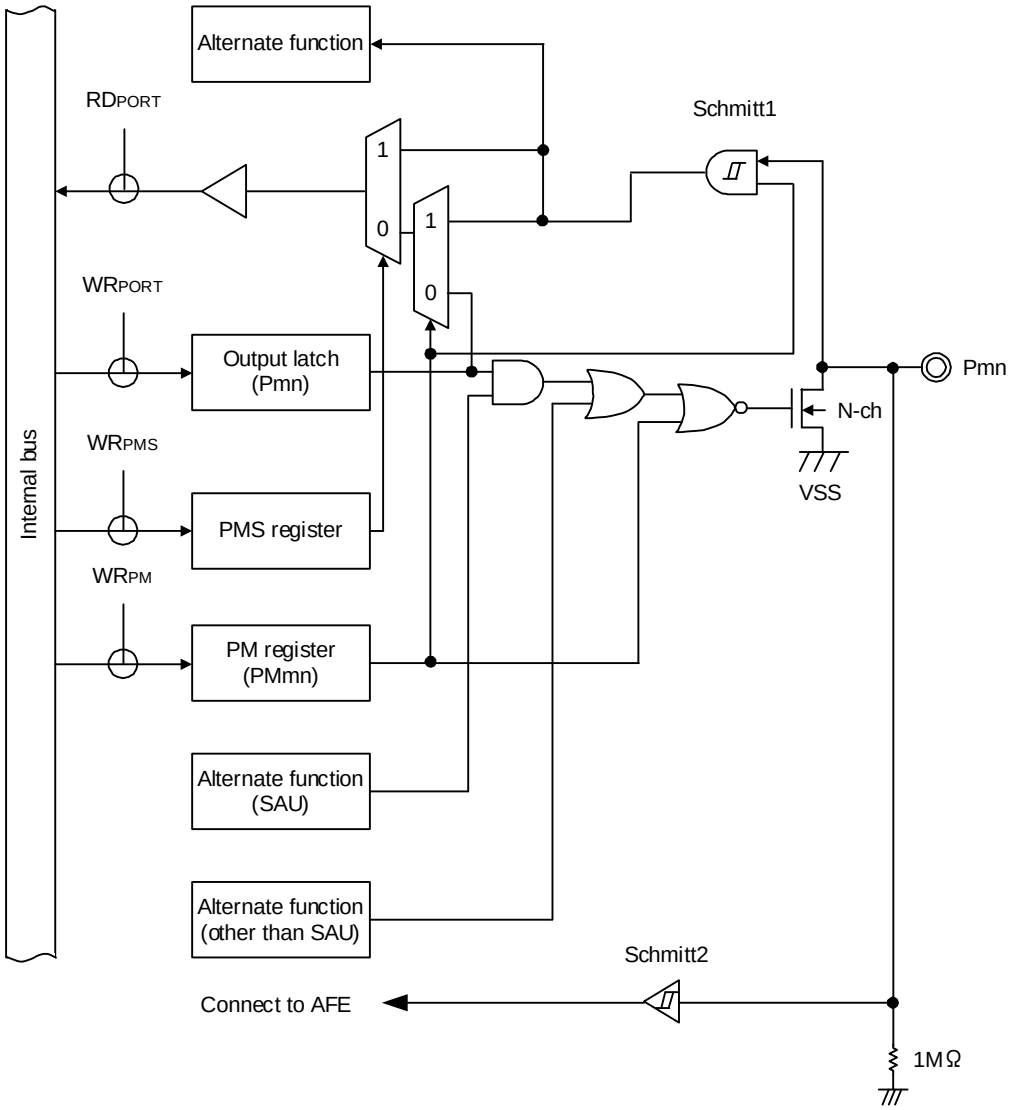
Figure 3-9 Pin Block Diagram of Pin type 8-6-8-2



Remark Refer to section 3.2.1for alternate functions.

3.4.10 Type 12-1-2

Figure 3-10 Pin Block Diagram of Pin type 12-1-2

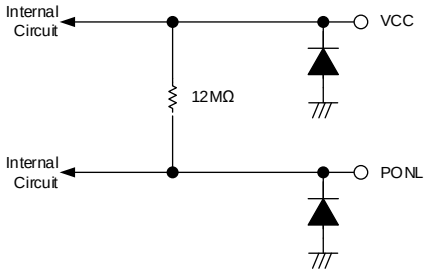


Remark Refer to section 3.2.1for alternate functions.

3.5 AFE Pin Block Diagram

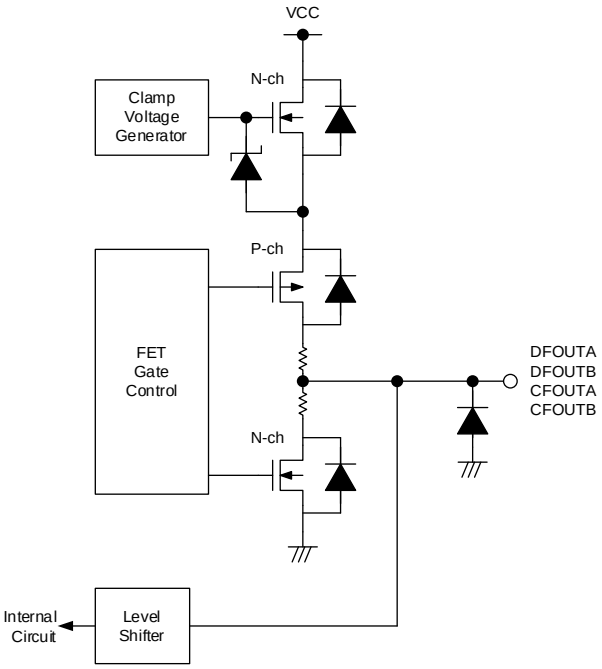
3.5.1 VCC and PONL Pin

Figure 3-11 Pin Block Diagram of VCC and PONL Pin



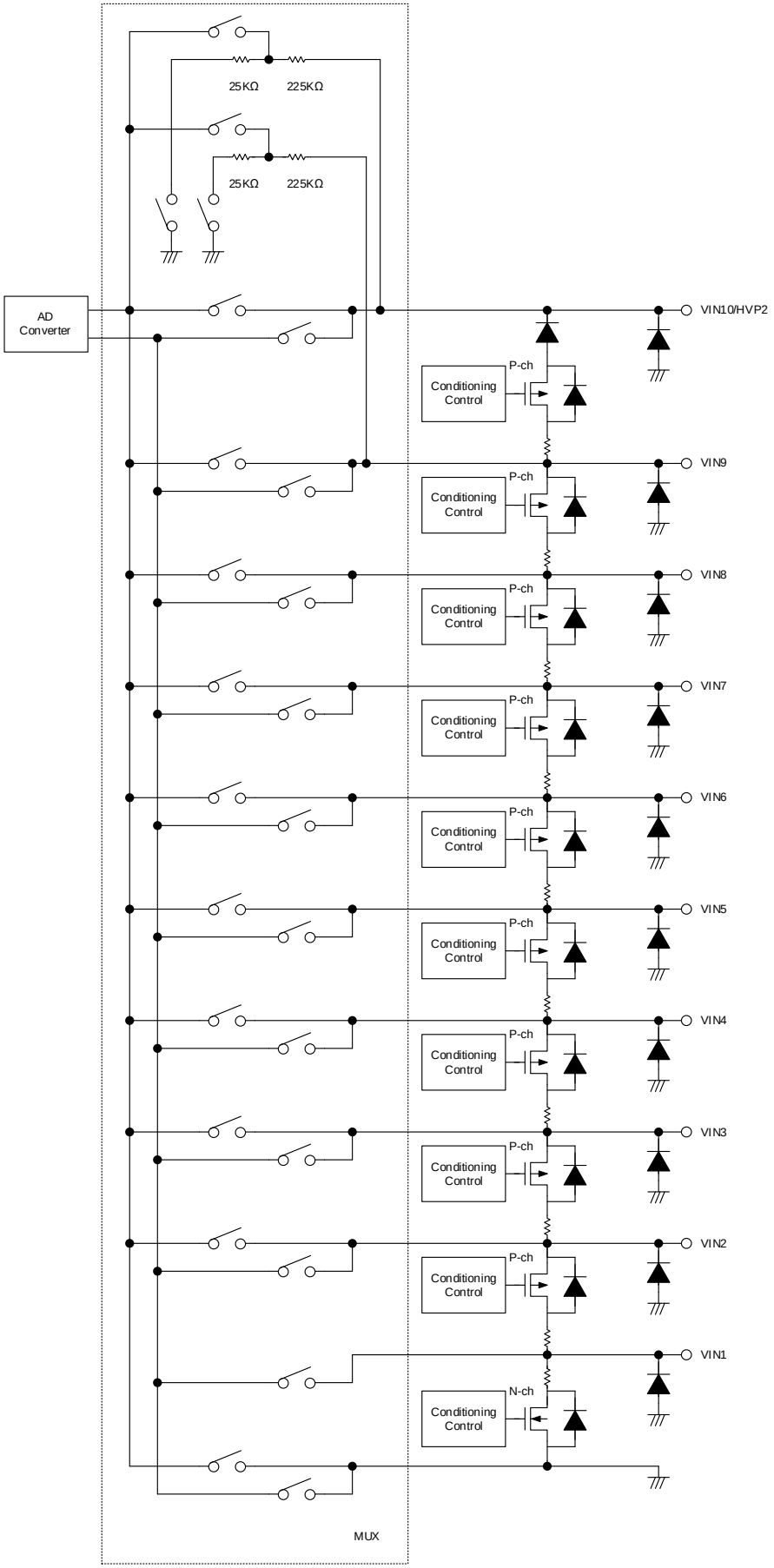
3.5.2 DFOUTA, DFOUTB, CFOUTA, and CFOUTB Pin

Figure 3-12 Pin Block Diagram of DFOUTA, DFOUTB, CFOUTA, and CFOUTB Pin



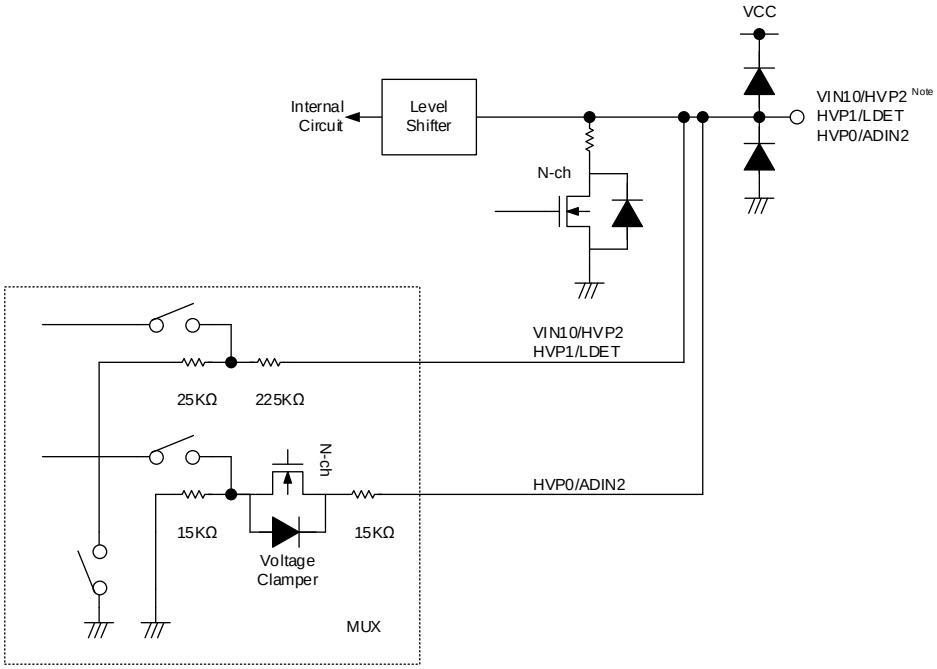
3.5.3 VIN10/HVP2, VIN9 to VIN1 Pin

Figure 3-13 Pin Block Diagram of VIN10/HVP2, VIN9 to VIN1 Pin



3.5.4 HVP0/ADIN2, HVP1/LDET, and VIN10/HVP2 Pin

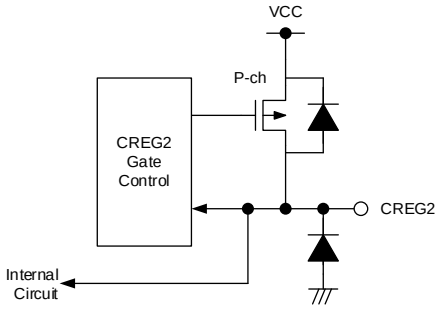
Figure 3-14 Pin Block Diagram of HVP0/LDET, HVP1/ADIN2, and VIN10/HVP2 Pin



Note When VIN9 pin is used for TOPCELL input, VIN10/HVP2 pin is available for one of high voltage analog input.

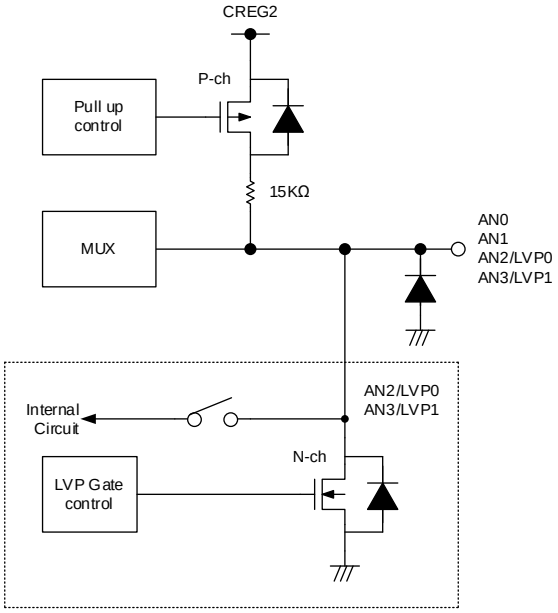
3.5.5 CREG2 Pin

Figure 3-15 Pin Block Diagram of CREG2 Pin



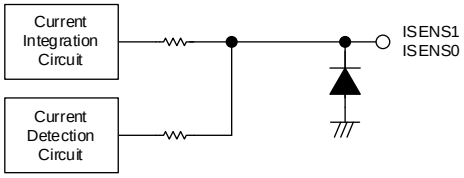
3.5.6 AN0, AN1, AN2/LVP0, AN3/LVP1 Pin

Figure 3-16 Pin Block Diagram of AN0, AN1, AN2 and AN3 Pin



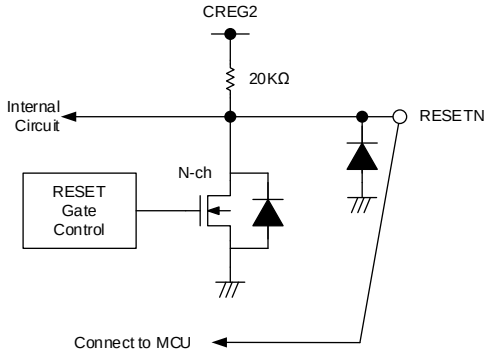
3.5.7 ISENS0 and ISENS1 Pin

Figure 3-17 Pin Block Diagram of ISENS0 and ISENS1 Pin



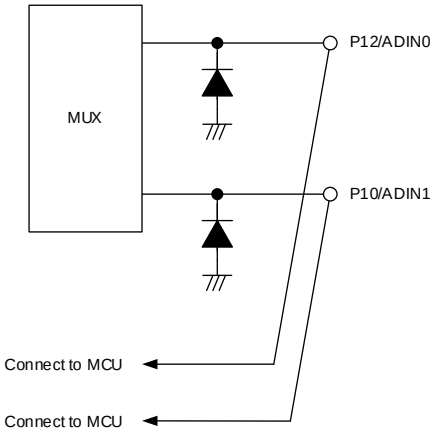
3.5.8 RESETN Pin

Figure 3-18 Pin Block Diagram of RESETN Pin



3.5.9 P12/ADIN0 and P10/ADIN1

Figure 3-19 P12/ADIN0 and P10/ADIN0 Pin



4. ELECTRICAL SPECIFICATIONS

Caution This product has an on-chip debug function, which is provided for development and evaluation. Do not use the on-chip debug function in products designated for mass production because the guaranteed number of rewritable times of the flash memory may be exceeded when this function is used, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when the on-chip debug function is used.

4.1 Absolute Maximum Ratings

Table 4 Absolute Maximum Ratings

Parameter	Symbols	Conditions		Ratings	Unit
Supply voltage	V_{CC}	VCC		-0.5 to +60.0	V
	GND	VSS, GND0, GND1		-0.5 to 0.3	V
	V_{REG2}	CREG2 Note 2		-0.3 to 6.5	V
REGC pin input voltage	V_{IREGC}	REGC Note 1		-0.3 to 2.8 and -0.3 to (CREG2+0.3) Note 3	V
Input voltage	V_{I1}	P10 to P12, P16, P17, P40 (TOOL0), P122, P137, RESETN		-0.3 to (CREG2+0.3) Note 3	V
	V_{I2}	P60, P61(N-ch open-drain)		-0.3 to +6.5	V
	V_{IN-H1}	VIN10, VIN9, VIN8, VIN7, VIN6, VIN5, VIN4, VIN3, VIN2, VIN1		-0.5 to +60.0	V
	V_{IN-H2}	HVP2, HVP1, HVP0		-0.5 to (VCC+0.3) Note 4	V
	V_{IN-B}	VIN10 to VIN9, VIN9 to VIN8, VIN8 to VIN7, VIN7 to VIN6, VIN6 to VIN5, VIN5 to VIN4, VIN4 to VIN3, VIN3 to VIN2, VIN2 to VIN1, VIN1 to GND0		-0.5 to +6.5	V
	V_{IN-M}	AN3/LVP1, AN2/LVP0, AN1, AN0		-0.5 to (CREG2+0.3) Note 3	V
	V_{IN-L}	ISENS0, ISENS1		-0.5 to +2.0	V
	V_{PONL}	PONL		-0.5 to +60.0	V
Output voltage	V_{O1}	P10 to P12, P16, P17, P40 (TOOL0), SCL (P60), SDA (P61)		-0.3 to (CREG2+0.3) Note 3	V
	V_{O-H1}	CFOUT A/B, DFOUT A/B		-0.5 to +60.0	V
	V_{O-H2}	HVP2, HVP1, HVP0		-0.5 to +60.0	V
	V_{O-M}	LVP1, LVP0		-0.5 to (CREG2+0.3) Note 3	V
High-level output current	I_{OH}	Per pin	P10 to P12, P16, P17, P40/TOOL0	-40	mA
		Total of all pins	P10 to P12, P16, P17, P40/TOOL0	-70	mA
Low-level output current	I_{OL1}	Per pin	P10 to P12, P16, P17, P40/TOOL0	+40	mA
		Total of all pins	P10 to P12, P16, P17, P40/TOOL0	+70	mA
Power consumption	Pd	Topr = 25 C		300	mW
Operating ambient Temperature	Ta	-		-40 to +85	°C
Storage temperature	Tstg	-		-65 to +150	°C

Note 1. Connect the REGC pin to VSS via a capacitor (0.47 to 1uF). This value regulates the absolute maximum rating of the REGC pin. Do not use this pin with voltage applied to it.

Note 2. Connect the CREG2 pin to GND0/1 via a capacitor (2.2uF). This value regulates the absolute maximum rating of the CREG2 pin.

Note 3. Must be 6.5V or lower.

Note 4. Must be 60.0V or lower.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. GND (GND0, GND1 and VSS): Reference voltage.

4.2 Power supply voltage condition

Table 5 Power supply voltage conditions

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power supply	VCC		8.0	-	50.0	V
	GND	GND0, GND1, VSS	-	0.0	-	V

4.3 Supply current characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX	Unit
Power down mode current 1	IPD	VCC=35V	-	-	2.0	uA
Power down mode current 2	IPDL	VCC=8.0V	-	-	1.0	uA
Power down mode with PON timer	IPDTim	VCC=35V	-	2.0	4.0	uA
Sleep mode current 1	ISLP1	MCU operating mode: STOP mode ALOCO=ON, AOCO=OFF CD=ALL ON, AFE Timer=ON AFE WDT=ON, CFOUT=L, DFOUT=L AD(AFE)=OFF, CC=OFF	-	25	50	uA
Sleep mode curernt2	ISLP2	MCU operating mode: STOP mode ALOCO=ON, AOCO=OFF CD=ALL ON, AFE Timer=ON AFE WDT=ON, CFOUT=H, DFOUT=H AD(AFE)=OFF, CC=OFF	-	40	70	uA
Normal mode current	INOM	MCU operating mode: LS (Low-speed main) mode, fHOCO=8MHz ALOCO=ON, AOCO=ON CD=ALL ON, AFE Timer=ON AFE WDT=ON, CFOUT=H, DFOUT=H AD(AFE)=ON, CC=ON	-	2.0	3.0	mA

Caution After trimming.

4.4 Oscillator Characteristics

4.4.1 MCU On-chip oscillator Characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
High-speed on-chip oscillator clock frequency Note 1	f_{IH}		-	8	-	MHz
High-speed on-chip oscillator clock frequency accuracy			-1.5	-	+1.5	%
Low-speed on-chip oscillator clock frequency	f_{IL}		-	15	-	kHz
Low-speed on-chip oscillator clock frequency accuracy			-15	-	+15	%

Note 1. High-speed on-chip oscillator frequency is selected with bits 0 to 4 of the option byte (000C2H) and bits 0 to 2 of the HOCODIV register.

Note 2. This only indicates the oscillator characteristics. Refer to AC Characteristics for instruction execution time.

4.4.2 AFE On-chip oscillator Characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
AFE on-chip oscillator clock frequency	fAOCO		-	4.194	-	MHz
AFE on-chip oscillator clock frequency accuracy			-2	-	+2	%
AFE Low-speed on-chip oscillator clock frequency	fALOCO		-	131.072	-	kHz
AFE Low-speed on-chip oscillator clock frequency accuracy			-5	-	+5	%
AFE PON on-chip oscillator clock frequency	fAPOOCO		-	32	-	kHz
AFE PON on-chip oscillator clock frequency accuracy			-50	-	+100	%

Caution After trimming.

Remark Values in parentheses are design value.

4.5 Pin Characteristics

(1/3)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, high Note 1	I_{OH}	Per pin for P10 to P12, P16, P17, P40	-	-	-10.0 Note 2	mA
		Per pin for P10 to P12, P16, P17, P40 (When duty ≤70% Note 3)	-	-	-19.0	mA
		Total of all pins (When duty ≤70% Note 3)	-	-	-135.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from the CREG2 pins to an output pin.

Note 2. Do not exceed the total current value.

Note 3. Specification for the condition where duty factor ≤ 70%.
To find the output current value for duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current from pins = (I_{OH} × 0.7)/ (n × 0.01)

<Example> Where n = 80% and I_{OH} = -10.0 mA
Total output current from pins = (-10.0 × 0.7)/ (80 × 0.01) ≈ -8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.
A current higher than the absolute maximum rating must not flow into any one pin.

Caution **P10 to P12, P16 and P17 do not output high level in N-ch open-drain mode.**

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(2/3)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output current, low Note 1	I_{OL}	Per pin for P10 to P12, P16, P17, P40	-	-	20.0 Note 2	mA
		Per pin for P60, P61	-	-	15.0 Note 2	mA
		Per pin for P10 to P12, P16, P17, P40 (When duty ≤70% Note 3)	-	-	35.0	mA
		Total of all pins (When duty ≤70% Note 3)	-	-	150.0	mA

Note 1. Value of current at which the device operation is guaranteed even if the current flows from an output pin to the VSS pins.

Note 2. Do not exceed the total current value.

Note 3. Specification for the conditions where the duty factor ≤ 70%.
To find the output current value for duty factor > 70% the duty ratio can be calculated with the following expression (when changing the duty factor from 70% to n%).

• Total output current of pins = (IOL × 0.7)/ (n × 0.01)

<Example> Where n = 80% and I_{OL} = 10.0 mA
Total output current of pins = (10.0 × 0.7)/ (80 × 0.01) ≈ 8.7 mA

However, the allowable current flow into one pin does not change with the duty factor.
A current higher than the absolute maximum rating must not flow into any one pin.

Remark Unless specified otherwise, the characteristics of alternate-function pins are the same as those of the port pins.

(3/3)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	P10 to P12, P16, P17, P122, P137, P40/TOOL0, RESETN	Normal input buffer	0.8 CREG2	-	CREG2	V
	V_{IH2}	SCL (P60), SDA (P61)		2.1	-	CREG2	V
	V_{IH3}	P10, P16, P17	TTL input buffer	2.0	-	CREG2	V
Input voltage, low	V_{IL1}	P10 to P12, P16, P17, P122, P137, P40/TOOL0, RESETN	Normal input buffer	0	-	0.2 CREG2	V
	V_{IL2}	SCL (P60), SDA (P61)		0	-	0.8	V
	V_{IL3}	P10, P16, P17	TTL input buffer	0	-	0.5	V
Output voltage, high	V_{OH}	P10 to P12, P16, P17, P40	I_{OH} = -1.5 mA	CREG2 – 0.5	-	CREG2	V
Output voltage, low	V_{OL1}	P10 to P12, P16, P17, P40	I_{OH} = -1.5 mA	-	-	0.4	V
	V_{OL2}	SCL (P60), SDA (P61)	I_{OH} = -3.0 mA	-	-	0.4	V
Input leak current, high	I_{LIH1}	P10 to P12, P16, P17, P122, P137, P40/TOOL0, RESETN	VI = CREG2	-	-	1	uA
Input leak current, low	I_{LIL1}	P10 to P12, P16, P17, P122, P137, P40/TOOL0, RESETN	VI = VSS	-	-	-1	uA
On-chip pull-up resistance	R_U	P10 to P12, P16, P17, P40 P40/TOOL0,	VI = VSS, input port	10	20	100	KΩ
	R_{UA}	AN0, AN1, AN2, AN3		11.2	15	18.8	KΩ
	R_{UAR}	RESETN		-	20	-	KΩ

Remark 1. Unless specified, the characteristics of alternate-function pins are the same as those of the port pins.

Remark 2. Regarding pin characteristics of CFOUT A/B, DFOUT A/B, refer to Section 4.8.6 Charge/Discharge FET control circuit.

Remark 3. Regarding pin characteristics of VIN1 to VIN10 refer to Section 4.8.2 Multiplexer characteristics.

Remark 4. Regarding pin characteristics of HVP0 to HVP2 refer to Section 4.8.1 High-voltage port Characteristics.

4.6 AC Characteristics

(1/2)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

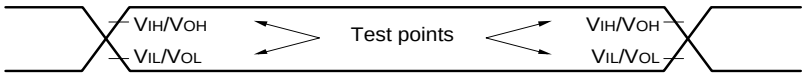
Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Instruction cycle (minimum instruction execution time)	T_{CY}	Main system clock (f_{MAIN}) operation	HS (high-speed main) mode	0.03125	-	1	us
			LS (low-speed main) mode	0.125	-	1	us
			LV (low-voltage main) mode	0.25	-	1	us
		In the self-programming mode	HS (high-speed main) mode	0.03125	-	1	us
			LS (low-speed main) mode	0.125	-	1	us
			LV (low-voltage main) mode	0.25	-	1	us

(2/2)

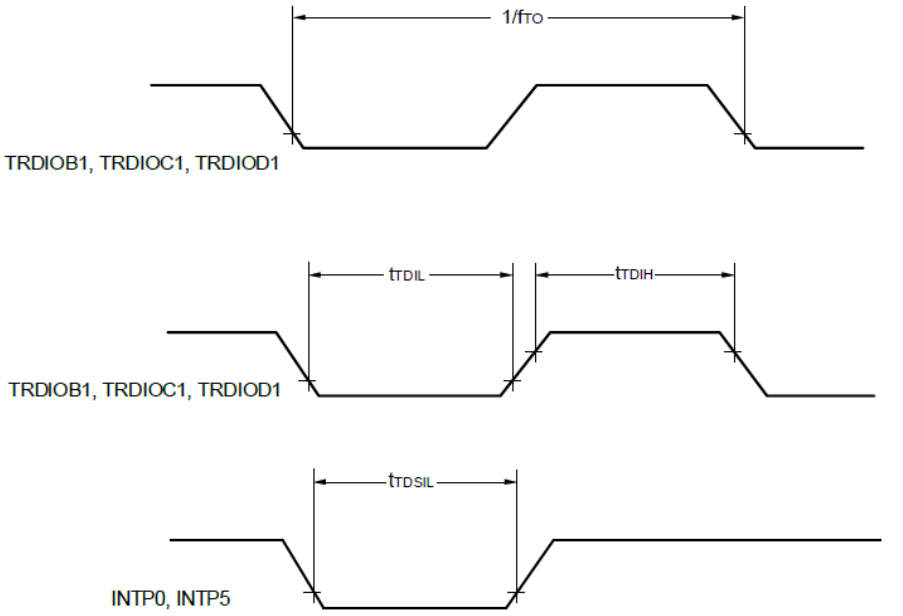
(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Timer RD input high-level width, low-level width	t_{TDIH}, t_{TDIL}	TRDIOB1, TRDIOC1, TRDIOD1	3/f_{CLK}	-	-	ns
TRDIOB1, TRDIOC1, TRDIOD1 output frequency	f_{TO}	HS (high-speed main) mode	-	-	8	MHz
		LS (low-speed main) mode	-	-	4	MHz
		LV (low-voltage main) mode	-	-	2	MHz
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTL}	INTP0, INTP5	1	-	-	us
RESETN low-level width	t_{RSL}		10	-	-	us

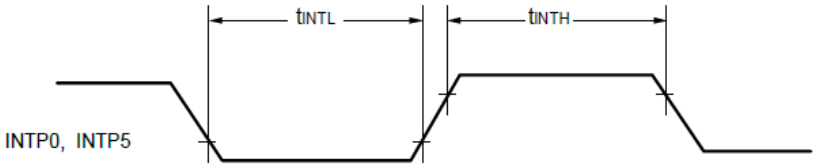
AC Timing Test Points



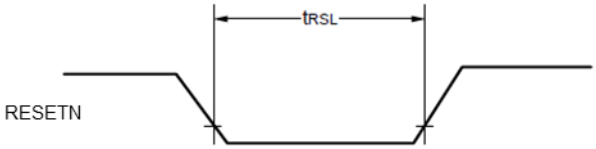
TI/TO Timing



Interrupt Request Input Timing

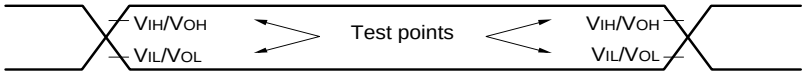


RESETN Input Timing



4.7 MCU peripheral circuit Characteristics

AC Timing Test Points



4.7.1 Serial array unit

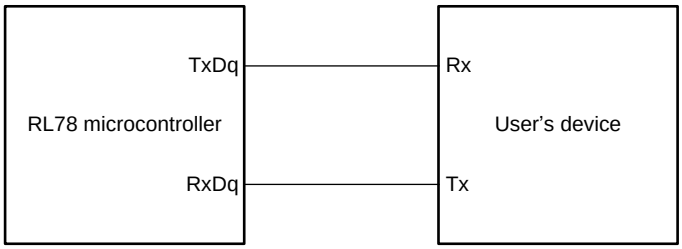
(1) During communication at same potential (UART mode) (Dedicated baud rate generator output)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

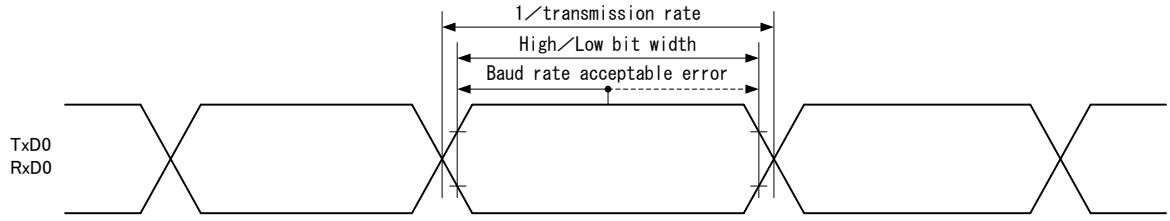
Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Transfer rate Note 1			-	fMCK/6	-	fMCK/6	-	fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK	-	5.3	-	1.3	-	0.6	Mbps

Note 1. Transfer rate in the SNOOZE mode is 4800 bps only.

Caution **Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).**



UART mode connection diagram (During communication at same potential)



UART mode bit width (During communication at same potential) (reference)

Remarks 1. q: UART number (q = 0, 1), g: PIM and POM number (g = 1)

Remarks 2. fMCK: Serial array unit operation clock frequency
(Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number,
n: Channel number (mn = 00,02)

(2) During communication at same potential (CSI mode) (master mode, SCKp... internal clock output)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V) Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time	t_{KCY1}	$t_{KCY1} \geq 4/f_{CLK}$	125	-	500	-	1000	-	ns
SCKp high-/low-level width	t_{KH1}, t_{KL1}		t_{KCY1}/2 - 18	-	t_{KCY1}/2 - 50	-	t_{KCY1}/2 - 50	-	ns
SIp setup time (to SCKp ↑) Note 1	t_{SIK1}		44	-	110	-	110	-	ns
SIp hold time (from SCKp ↑) Note 2	t_{KSI1}		19	-	19	-	19	-	ns
Delay time from SCKp ↓ to SOp output Note 3	t_{KSO1}	C = 30 pF Note 4	-	25	-	25	-	25	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes “to SCKp ↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes “from SCKp ↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes “from SCKp ↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 10), m: Unit number (m = 0), n: Channel number (n = 2), g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 02))

(3) During communication at same potential (CSI mode) (slave mode, SCKp... external clock input)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCKp cycle time Note 5	t_{KCY2}	1 MHz < f_{MCK}	8/f_{MCK}	-	-	-	-	-	ns
		f_{MCK} ≤ 16 MHz	6/f_{MCK}	-	6/f_{MCK}	-	6/f_{MCK}	-	ns
SCKp high-/low-level width	t_{KH2}, t_{KL2}		t_{KCY2}/2 - 8	-	t_{KCY2}/2 - 8	-	t_{KCY2}/2 - 8	-	ns
SIp setup time (to SCKp ↑) Note 1	t_{SIK2}		1/f_{MCK} + 20	-	1/f_{MCK} + 30	-	1/f_{MCK} + 30	-	ns
SIp hold time (from SCKp ↑) Note 2	t_{KSI2}		1/f_{MCK} + 31	-	1/f_{MCK} + 31	-	1/f_{MCK} + 31	-	ns
Delay time from SCKp ↓ to SOp output Note 3	t_{KSO2}	C = 30pF Note 4	-	2/f_{MCK} + 44	-	2/f_{MCK} + 110	-	2/f_{MCK} + 110	ns

Note 1. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp setup time becomes "to SCKp ↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The SIp hold time becomes "from SCKp ↓" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.
The delay time to SOp output becomes "from SCKp ↑" when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

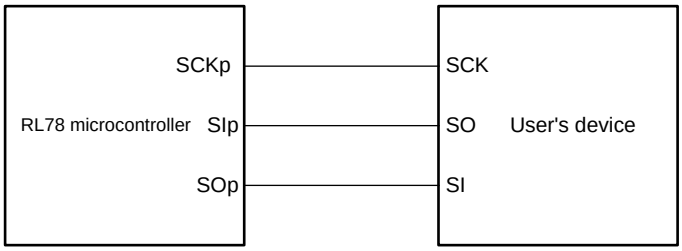
Note 4. C is the load capacitance of the SCKp and SOp output lines.

Note 5. The maximum transfer rate when using the SNOOZE mode is 1 Mbps.

Caution Select the normal input buffer for the SIp pin and the normal output mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark 1. p: CSI number (p = 10), m: Unit number (m = 0), n: Channel number (n = 2), g: PIM number (g = 1)

Remark 2. f_{MCK}: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn).
m: Unit number, n: Channel number (mn = 02))



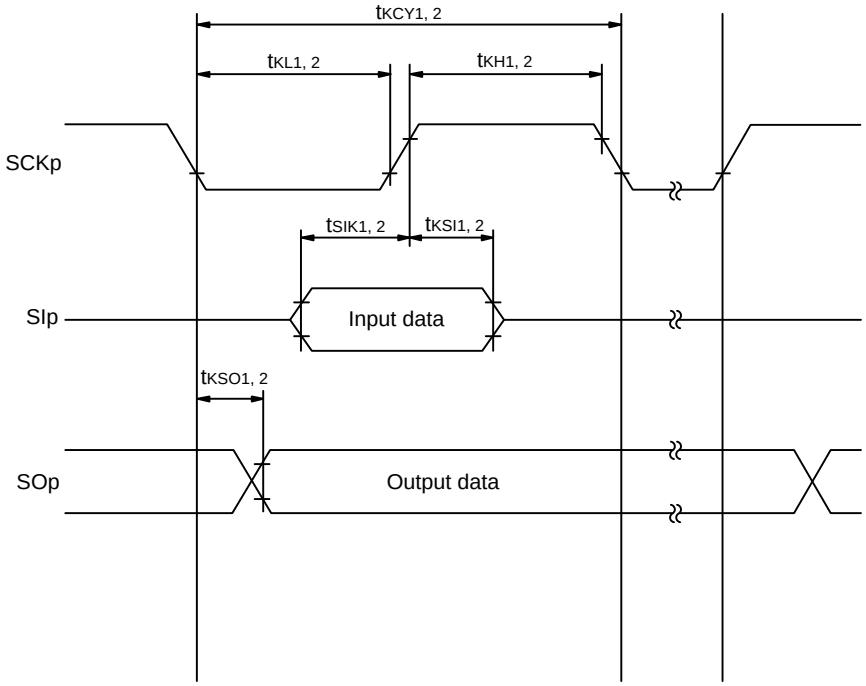
CSI mode connection diagram (during communication at same potential)

Remark 1. p: CSI number (p =10)

Remark 2. m: Unit number, n: Channel number (mn = 02)

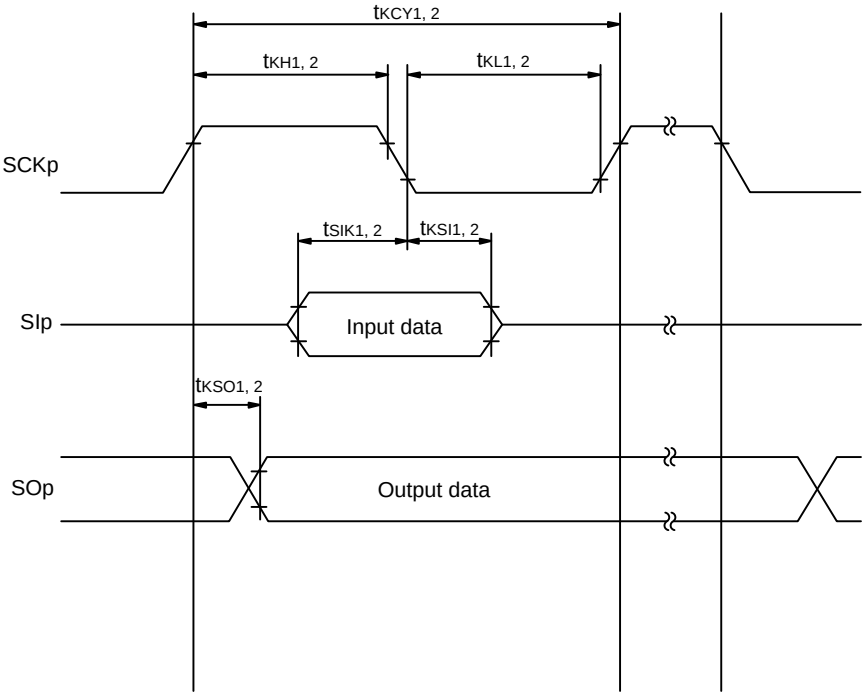
CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.)



CSI mode serial transfer timing (during communication at same potential)

(When DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.)



Remark 1. p: CSI number (p = 10)

Remark 2. m: Unit number, n: Channel number (mn = 02)

(4) During communication at same potential (simplified I²C mode)

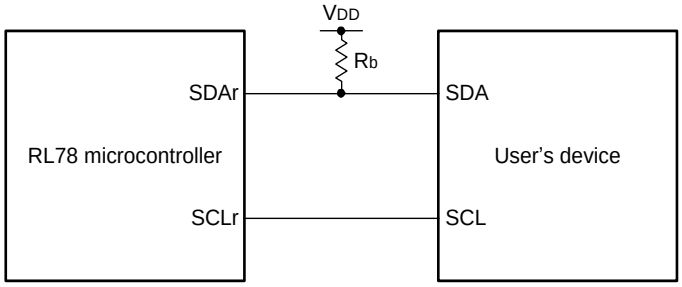
(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLr clock frequency	f_{SCL}	Cb = 50pF, Rb = 2.7kΩ	-	1000 Note 1	-	400 Note 1	-	400 Note1	kHz
Hold time when SCLr = "L"	t_{LOW}	Cb = 50pF, Rb = 2.7kΩ	475	-	1150	-	1150	-	ns
Hold time when SCLr = "H"	t_{HIGH}	Cb = 50pF, Rb = 2.7kΩ	475	-	1150	-	1150	-	ns
Data setup time (reception)	$t_{SU: DAT}$	Cb = 50pF, Rb = 2.7kΩ	1/f_{MCK} + 85 Note 2	-	1/f_{MCK} + 145 Note 2	-	1/f_{MCK} + 145 Note2	-	ns
Data hold time (transmission)	$t_{HD: DAT}$	Cb = 50pF, Rb = 2.7kΩ	0	305	0	305	0	305	ns

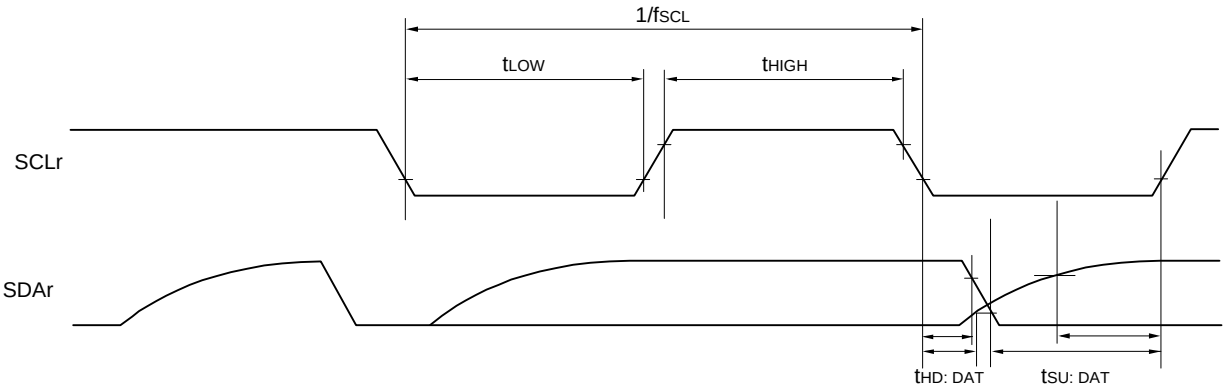
Note 1. The value must also be equal to or less than f_{MCK}/4.

Note 2. Set the fMCK value to be equal or less than the tLOW and tHIGH time values directly above

Caution Select the normal input buffer and the N-ch open drain output (VDD tolerance) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).



Simplified I²C mode connection diagram (during communication at same potential)



Simplified I²C mode serial transfer timing (during communication at same potential)

Remark 1. Rb[Ω]: Communication line (SDAr) pull-up resistance, Cb[F]: Communication line (SDAr, SCLr) load capacitance

Remark 2. r: IIC number (r = 00, 10), g: PIM, POM number (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency (Operation clock to be set by the CKSmn bit of serial mode register mn (SMRmn). m: Unit number, n: Channel number mn = 02)

4.7.2 Serial interface IICA

(1) I^2C standard mode

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Standard mode: $f_{CLK} \geq$ 1MHz	0	100	0	100	0	100	kHz
Setup time of restart condition	$t_{SU: STA}$		4.7	-	4.7	-	4.7	-	us
Hold time Note 1	$t_{HD: STA}$		4.0	-	4.0	-	4.0	-	us
Hold time when SCLA0 = “L”	t_{LOW}		4.7	-	4.7	-	4.7	-	us
Hold time when SCLA0 = “H”	t_{HIGH}		4.0	-	4.0	-	4.0	-	us
Data setup time (reception)	$t_{SU: DAT}$		250	-	250	-	250	-	ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	3.45	0	3.45	0	3.45	us
Setup time of stop condition	$t_{SU: STO}$		4.0	-	4.0	-	4.0	-	us
Bus-free time	t_{BUF}		4.7	-	4.7	-	4.7	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Standard mode: Cb = 400pF, Rb = 2.7kΩ

(2) I^2C fast mode

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode: fCLK ≥ 3.5 MHz	0	400	0	400	0	400	kHz
Setup time of restart condition	$t_{SU: STA}$		0.6	-	0.6	-	0.6	-	us
Hold time Note1	$t_{HD: STA}$		0.6	-	0.6	-	0.6	-	us
Hold time when SCLA0 = “L”	t_{LOW}		1.3	-	1.3	-	1.3	-	us
Hold time when SCLA0 = “H”	t_{HIGH}		0.6	-	0.6	-	0.6	-	us
Data setup time (reception)	$t_{SU: DAT}$		100	-	100	-	100	-	ns
Data hold time (transmission) Note2	$t_{HD: DAT}$		0	0.9	0	0.9	0	0.9	us
Setup time of stop condition	$t_{SU: STO}$		0.6	-	0.6	-	0.6	-	us
Bus-free time	t_{BUF}		1.3	-	1.3	-	1.3	-	us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected.

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode: Cb = 320pF, Rb = 1.1kΩ

(3) I^2C fast mode plus

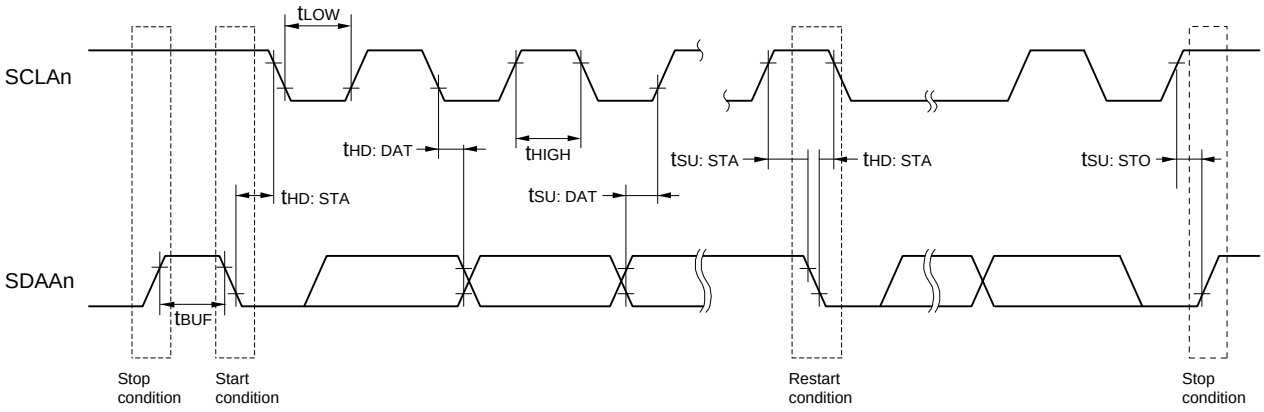
(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	HS (high-speed main) mode		LS (low-speed main) mode		LV (low-voltage main) mode		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
SCLA0 clock frequency	f_{SCL}	Fast mode plus: fCLK ≥ 10 MHz	0	1000	-		-		kHz
Setup time of restart condition	$t_{SU: STA}$		0.26	-	-		-		us
Hold time Note 1	$t_{HD: STA}$		0.26	-	-		-		us
Hold time when SCLA0 = “L”	t_{LOW}		0.5	-	-		-		us
Hold time when SCLA0 = “H”	t_{HIGH}		0.26	-	-		-		us
Data setup time (reception)	$t_{SU: DAT}$		50	-	-		-		ns
Data hold time (transmission) Note 2	$t_{HD: DAT}$		0	0.45	-		-		us
Setup time of stop condition	$t_{SU: STO}$		0.26	-	-		-		us
Bus-free time	t_{BUF}		0.5	-	-		-		us

Note 1. The first clock pulse is generated after this period when the start/restart condition is detected

Note 2. The maximum value (MAX.) of tHD: DAT is during normal transfer and a wait state is inserted in the ACK (acknowledge) timing.

Remark The maximum value of Cb (communication line capacitance) and the value of Rb (communication line pull-up resistor) at that time in each mode are as follows.
Fast mode plus: Cb = 120pF, Rb = 1.1kΩ



IICA serial transfer timing

Remark n = 0

4.7.3 Interrupt

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Interrupt input high-level width, low-level width	t_{INTH}, t_{INTHL}	INTP0, INTP5	1	-	-	us

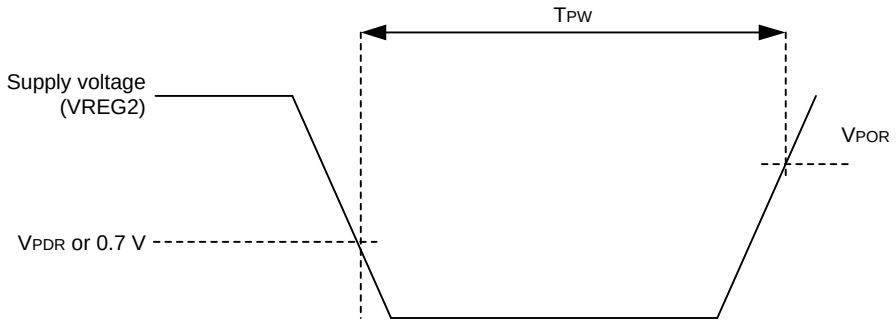
4.7.4 POR circuit characteristics (MCU)

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Power on/down reset threshold	V_{POR}	Voltage threshold on VREG2 rising	1.47	1.51	1.55	V
	V_{PDR}	Voltage threshold on VREG2 falling Note 1	1.46	1.50	1.54	V
Minimum pulse width Note 2	T_{PW}		300	-	-	us

Note 1. However, when the operating voltage falls, enter STOP mode, or enable the reset status using the external reset pin before the voltage falls below the operating voltage range shown in Section 4.6 AC Characteristics.

Note 2. Minimum time required for a POR reset when VREG2 is below VPDR. This is also the minimum time required for a POR reset when VREG2 exceeds VPOR after VREG2 is below 0.7 V during STOP mode.



4.8 AFE peripheral circuit characteristics

4.8.1 High-voltage port Characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH}		2.6	-	-	V
Input voltage, low	V_{IL}		-	-	0.7	V
Output voltage, low	VoL	IOL = 1mA	-	-	0.7	V
On resistance, high level output (Nch MOS output)	R_{ONN}	IOL= 1 mA	-	-	700	Ω
Pin leakage current	I_{LK1}	HVP0, HVP1 VI=VCC, GND0/1	-	-	±1	uA
	I_{LK2}	HVP2	-	-	±2	uA

Note 1. Reference voltage is GND0 and GND1.

Note 2. HVP0 is a multi-function pin, and its functions are High-voltage GPIO and Analog input for ADC. When HVP0 is used in High-voltage port, this pin cannot be used in Analog input. It is exclusive.

4.8.2 Multiplexer characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Gain VIN(n)-VIN(n-1)	GAIN1	VIN10,VIN9,VIN8,VIN7,VIN6,VIN5>2.0V VIN4,VIN3,VIN2,VIN1>0V Note 1	-	1.0	-	V/V
Gain HV	GAIN2	TOPCELL Note 2, PONL, HVP1/LDET, VIN10/HVP2 Note 3	-	0.1	-	V/V
Gain AN	GAIN3	AN0, 1, 2, 3, ADIN0, 1	-	1.0	-	V/V
Gain ADIN2	GAIN4	ADIN2	-	0.5	-	V/V
Input voltage range VIN(n)-VIN(n-1)	VRA1	VIN10,VIN9,VIN8,VIN7,VIN6,VIN5>2.0V VIN4,VIN3,VIN2,VIN1>0V Note 1	-0.1	-	5.1	V
Input voltage range HV	VRA2	TOPCELL Note 2, PONL, HVP1/LDET, VIN10/HVP2 Note 3	0.0	-	50.0	V
Input voltage range AN	VRA3	AN0, 1, 2, 3, ADIN0, 1, 2	0.0	-	3.3	V
Input resistance	RI2	TOPCELL Note 2, PONL, HVP1/LDET, VIN10/HVP2 Note 3	-	250	-	KΩ
Input resistance	RI4	ADIN2	-	30	-	KΩ
Pin leakage current	I_{LKV1}	VIN1=5V	-	-	2	uA
		VIN2=10V	-	-	2	uA
		VIN3=15V	-	-	2	uA
		VIN4=20V	-	-	2	uA
		VIN5=25V	-	-	2	uA
		VIN6=30V	-	-	2	uA
		VIN7=35V	-	-	2	uA
		VIN8=40V	-	-	2	uA
		VIN9=45V	-	-	2	uA
		VIN10=50V	-	-	2	uA

Note 1. Reference voltage is GND0 and GND1

Note 2. TOPCELL means the top voltage of cells, and it is inputted by VIN10 or VIN9.

Note 3. When VIN9 pin is used for TOPCELL input, VIN10/HVP2 pin is available for one of high voltage analog input.

4.8.3 Sigma-delta A/D converter characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution Note1	RESAD	Conversion time = 8ms	-	-	15	bits
		Conversion time = 4ms	-	-	14	bits
		Conversion time = 2ms	-	-	13	bits
		Conversion time = 1ms	-	-	12	bits
		Conversion time = 0.5ms	-	-	11	bits
		Conversion time = 0.25ms	-	-	10	bits
Input voltage range	VINAD		-0.1	-	5.1	V
Integral nonlinearity	INLAD	End fit	-27	-	27	LSB
Conversion result in zero input	ADZERO	VIN=0V	-	3340 Note 2	-	LSB
Temperature dependency In zero input	dTADZERO	VIN=0V	-0.24	-	+0.24	LSB/C
Conversion result in full-scale input	ADFS	VIN=5.1V	-	31010 Note 2	-	LSB
Temperature dependency in full-scale input	dTADFS	VIN=5.1V	-0.24	-	+0.24	LSB/C
Input resistance	RINAD		-	(1.0)	-	MΩ
Battery cell voltage measurement error	ERRCELL1	T_A = +25°C After calibration	-	-	±5	mV
	ERRCELL2	-20 ≤ T_A ≤ 85°C After calibration	-	-	±10	mV
	ERRCELL2L	-40 ≤ T_A ≤ 85°C After calibration	-	-	±12	mV

Note 1. AD conversion result is output in 15-bit.

Note 2. This value is before subtracting the offset voltage.

Caution 1. Except for Battery Cell voltage measurement error (ERRCELLxx), these parameters are sigma-delta converter circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Values in parentheses are design value.

4.8.4 Current integrating circuit characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution	RESCC		-	-	18	bits
Conversion time	TCC		-	250	-	ms
Input voltage range	VINCC	±50mV mode ISENS1 to ISENS0	-50	-	+50	mV
		±100mV mode ISENS1 to ISENS0	-100	-	+100	mV
		±200mV mode ISENS1 to ISENS0	-200	-	+200	mV
Integral nonlinearity	INLCC	End fit	-	-	0.02	%FSR
Input resistance	RINCC	ISENS0, ISENS1	-	(1.0)	-	MΩ
Current measurement error Note	ERRCURR	±50mV mode Ta = 25 degC	-	(±10)	-	uV
		±50mV mode	-	-	(±60)	uV
		±100mV mode Ta = 25 degC	-	(±10)	-	uV
		±100mV mode	-	-	(±100)	uV
		±200mV mode Ta = 25 degC	-	(±20)	-	uV
		±200mV mode Input voltage range: -100mV to 200mV	-	-	(±200)	uV

Note After calibration.

Caution 1. Except for Current measurement error (ERRCURR), these parameters are current integration circuit characteristics.

Caution 2. Calibration is needed to keep high accuracy in system.

Remark Value in parentheses are design value.

4.8.5 Overcurrent detection / wakeup current detection circuit characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Discharge short-circuit current detection setting voltage step	dSVSC	25mv to 200mV	-	12.5	-	mV
		200mV to 300mV	-	25	-	mV
Discharge short-circuit current detection voltage error	dVSC	25mv to 200mV setting	-	-	±12.5	mV
		225mV to 300mV setting	-	-	±25.0	mV
Discharge overcurrent detection setting voltage step	dSVDOC	15mV to 100mV	-	2.5	-	mV
		100mV to 200mV	-	5	-	mV
Discharge overcurrent detection voltage error Note 1	dVDOC	15mV to 100mV setting	-	-	±5.0	mV
		105mV to 200mV setting	-	-	±7.5	mV
Charge overcurrent detection setting voltage step	dSVCOC	-60mV to -2.5mV	-	2.5	-	mV
		-100mV to -60mV	-	5	-	mV
Charge overcurrent detection voltage error Note 1	dVCOC	-60mV to -2.5mV setting	-	-	±5.0	mV
		-100mV to -65mV setting	-	-	±7.5	mV
Discharge wakeup current detection setting voltage step	dSVDWU	0mV to 140mV	-	1.25	-	mV
Charge wakeup current detection setting voltage step	dSVCWU	-140mV to 0mV	-	1.25	-	mV
Heavy Load detection setting voltage step	dSVHLD	0mV to 140mV	-	1.25	-	mV
Discharge wakeup current detection voltage error Note 1	dVDWU	20 times mode ISENS1 to ISENS0: 0.25mV to 2.5mV	-0.10	0.0	+0.25	mV
Charge wakeup current detection voltage error Note 1	dVCWU	20 times mode ISENS1 to ISENS0: -0.25mV to -2.5mV	-0.25	0.0	+0.10	mV
Heavy Load detection voltage error Note 1	dVHLD	20 times mode ISENS1 to ISENS0: 0.25mV to 2.5mV	-0.10	0.0	+0.25	mV
Discharge short-circuit current detection time error Note 2	dTSC	0us to 916us (61us step)	0.0	-	30.5	us
Discharge overcurrent detection time error Note 2	dTDOC	0.488ms to 32s (0.488ms step)	0.0	-	122	us
Charge overcurrent detection time error Note 2	dTCOC	0us to 15564us (61us step)	0.0	-	30.5	us
Discharge wakeup current detection time error Note 2	dTDWU	3.91ms to 62.56ms (3.91ms step)	-3.91	-	0	ms
Charge wakeup current detection time error Note 2	dTCWU	3.91ms to 62.56ms (3.91ms step)	-3.91	-	0	ms
Heavy Load detection time error Note 2	dTHLD	61us to 916us (61us step)	0.0	-	30.5	us

Note 1. This is the specification after zero-calibration is executed.

Note 2. The frequency error of AFE On-chip oscillator (AOCO and ALOCO) is excluded from these detection time error.

4.8.6 Charge/Discharge FET control circuit

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
CFOUT and DFOUT on	VFETON	VCC>12V with load resistance of 10MΩ	10	12.5	15	V
		VCC<=12V with load resistance of 10MΩ	VCC-2	VCC-1	VCC	V
CFOUT and DFOUT ON rise time	tFET_ON	CFOUT/DFOUT driving an equivalent load capacitance of 10nF, measured from 10% to 90%.	-	200	250	us
DFOUT pull-down OFF fall time	tDF_OFF	DFOUT driving an equivalent load capacitance of 10nF, measured from 90% to 10%	-	60	90	us
CFOUT pull-down OFF resistance to GND0/1	RCF_OFF	When CFOUT disabled, CFOUT held at 12V.	70	100	130	KΩ
DFOUT pull-down OFF resistance to GND0/1	RDF_OFF	When DFOUT disabled, DFOUT held at 12V.	1.75	2.50	4.25	KΩ

Caution After trimming.

Remark Values in parentheses are design value.

4.8.7 Power on circuit Characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	VIH		2.6	-	VCC	V
Input voltage, low	VIL	IC enable	GND0/1	-	1.0	V
Pull-up resistance	Rpu		-	12.4	-	MΩ

4.8.8 Series regulator circuit characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Output voltage	VR2O	50uA<=Io<=20mA	3.20	3.30	3.40	V
Load drive capability	IOMAX	8.0V<=VCC<=50.0V	20	-	-	mA

Note In case of using load drive, total power consumption must be under the maximum ratings power consumption (Pd).

Caution After trimming.

4.8.9 AFE reset circuit characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
VREG2 release voltage	VREL	At power on	2.8	2.9	3.0	V
VREG2 detection voltage	VDET	After trimming	2.7	2.8	2.9	V

4.8.10 Cell balancing circuit characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
On resistance	Ron	V(n+1)-V(n) = 3.5V, n=1~9	100	200	400	Ω

4.8.11 Power on timer characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Time setting range	T_{PonT}	Time is selectable from 1, 2, 4, 8, 16, 32, 64, 128, 256 min.	1	-	256	minutes
Time error	dT_{PonT}		-50	-	+100	%

4.8.12 Low Voltage GPIO; AFE GPIO characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

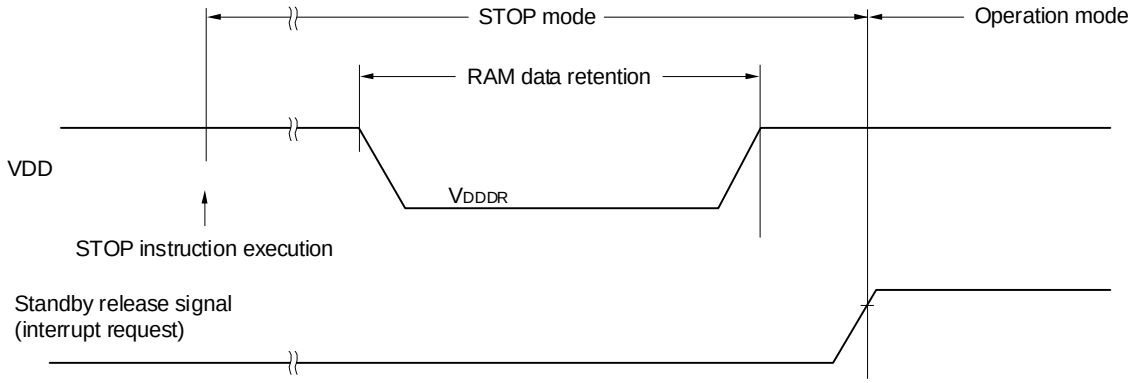
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input Voltage High	VIH_LVP		0.8 x CREG2	-	CREG2	V
Input Voltage Low	VIL_LVP		0.0	-	0.2 x CREG2	V
Output Voltage Low	VOL_LVP	IOL=1mA	-	-	0.4	V
Output Current Low	IOL_LVP		-	-	6.0	mA
Totally Output Current Low	IOL_T_LVP	LVP0+LVP1	-	-	12.0	mA
Leakage in High input	ILIH_LVP	VI=CREG2	-	-	1	uA
Leakage in Low input	ILIL_LVP	VI=GND0/1	-	-	1	uA

4.8.13 RAM Data Retention characteristics

(T_A= -40 to +85°C, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention supply voltage	V_{DDDR}		1.46 Note	-	CREG2	V

Note The value depends on the POR detection voltage. When the voltage drops, the RAM data is retained before a POR reset is effected, but RAM data is not retained when a POR reset is effected.



4.9 Flash memory programming characteristics

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TP.	MAX.	Unit
System clock frequency	f_{CLK}		1	-	32	MHz
Number of code flash rewrites Note 1, 2, 3	C_{erwr}	Retained for 20 years T_A = 85 °C	1,000	-	-	Times
Number of data flash rewrites Note 1, 2, 3		Retained for 1 year T_A = 25 °C	-	1,000,000	-	
		Retained for 5 years T_A = 85 °C	100,000	-	-	
		Retained for 20 years T_A = 85 °C	10,000	-	-	

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until rewrite after the rewrite.

Note 2. When using flash memory programmer and Renesas Electronics self-programming library.

Note 3. This flash memory characteristic is the result of the reliability test.

4.10 Dedicated Flash Memory Programmer Communication (UART)

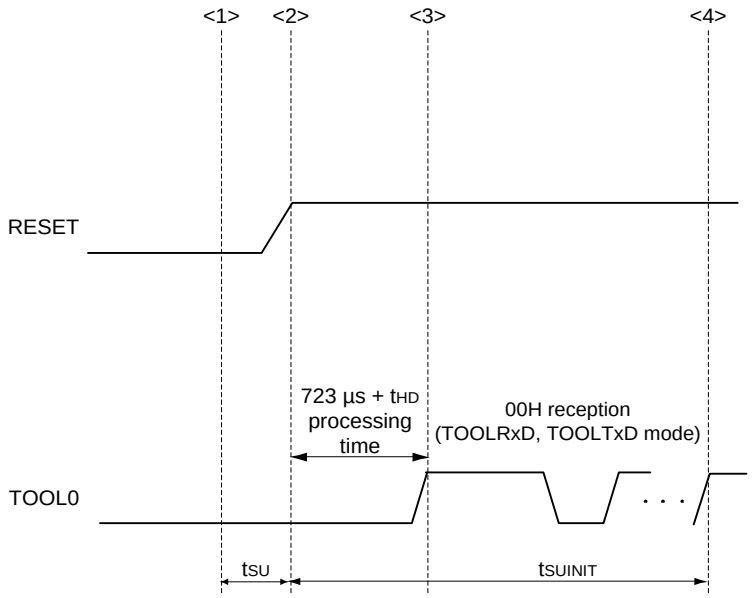
(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Transfer rate		During serial programming	115,200	-	1,000,000	bps

4.11 Timing of Entry to Flash Memory Programming Modes

(T_A= -40 to +85°C, 8.0<=VCC<=50V, GND0/1=VSS=0V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
The time needed from when an external reset ends until the initial communication settings are specified	tSUINIT	POR and LVD reset must end before the external reset ends.	-	-	100	ms
The time needed from when the TOOL0 pin is placed at low level until an external reset ends	tSU	POR and LVD reset must end before the external reset ends.	10	-	-	us
The time needed for the TOOL0 pin to be kept at low level after an external reset ends (excluding the processing time of the firmware to control the flash memory)	tHD	POR and LVD reset must end before the external reset ends.	1	-	-	ms



<1> The low level is input to the TOOL0 pin.

<2> The external reset ends (POR and LVD reset must end before the external reset ends).

<3> The TOOL0 pin is set to the high level.

<4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tSUINIT: The segment shows that it is necessary to finish specifying the initial communication settings within 100 ms from when the external resets end.

tSU: Time needed for the TOOL0 pin is placed at low level until the pin reset ends

tHD: Time needed for the TOOL0 pin at low level from when the external resets end (excluding the processing time of the firmware to control the flash memory)

5. DETAILED DESCRIPTION

5.1 Overview

RAJ240310 is Renesas Li-ion battery fuel gauge IC (FGIC) which consists of a MCU device and an AFE device in a single package. Pack with a variety of battery management features and Renesas RL78 CPU core which has multiple low power modes and capable of achieving high performance in ultra-low power operation.
The RAJ240310 has embedded flash memory on an MCU (same as other RL78 family) and use it to store program instructions (code) as well as data on to perform battery voltage / current / temperature measurement, remaining capacity estimation, over current / voltage / temperature protection and other battery management operations.

5.2 System Block diagram

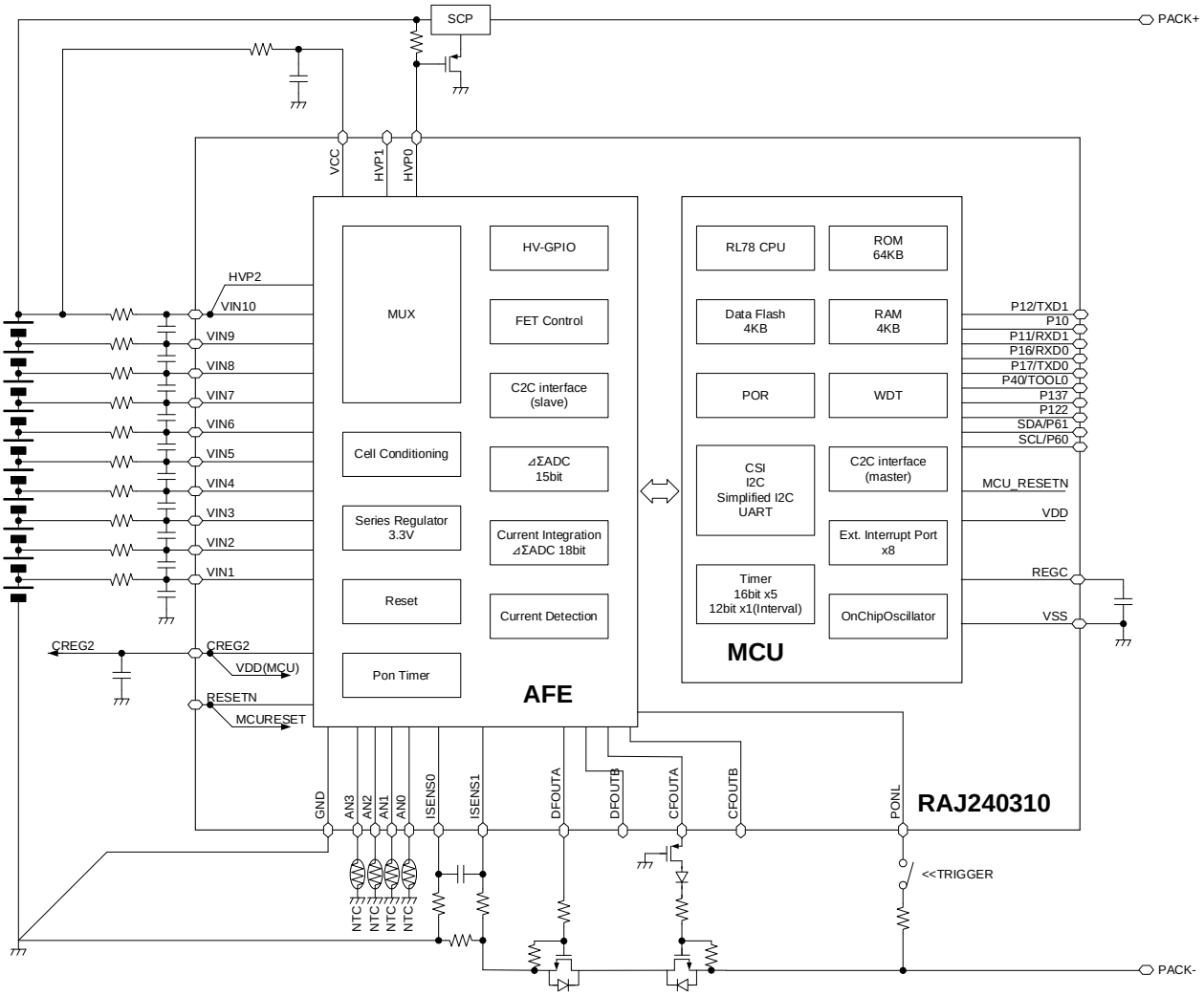


Figure 20 System block diagram

Caution The example peripheral circuit does not guarantee proper operation. Please perform sufficient evaluation using the actual application to determine the circuits and peripherals.

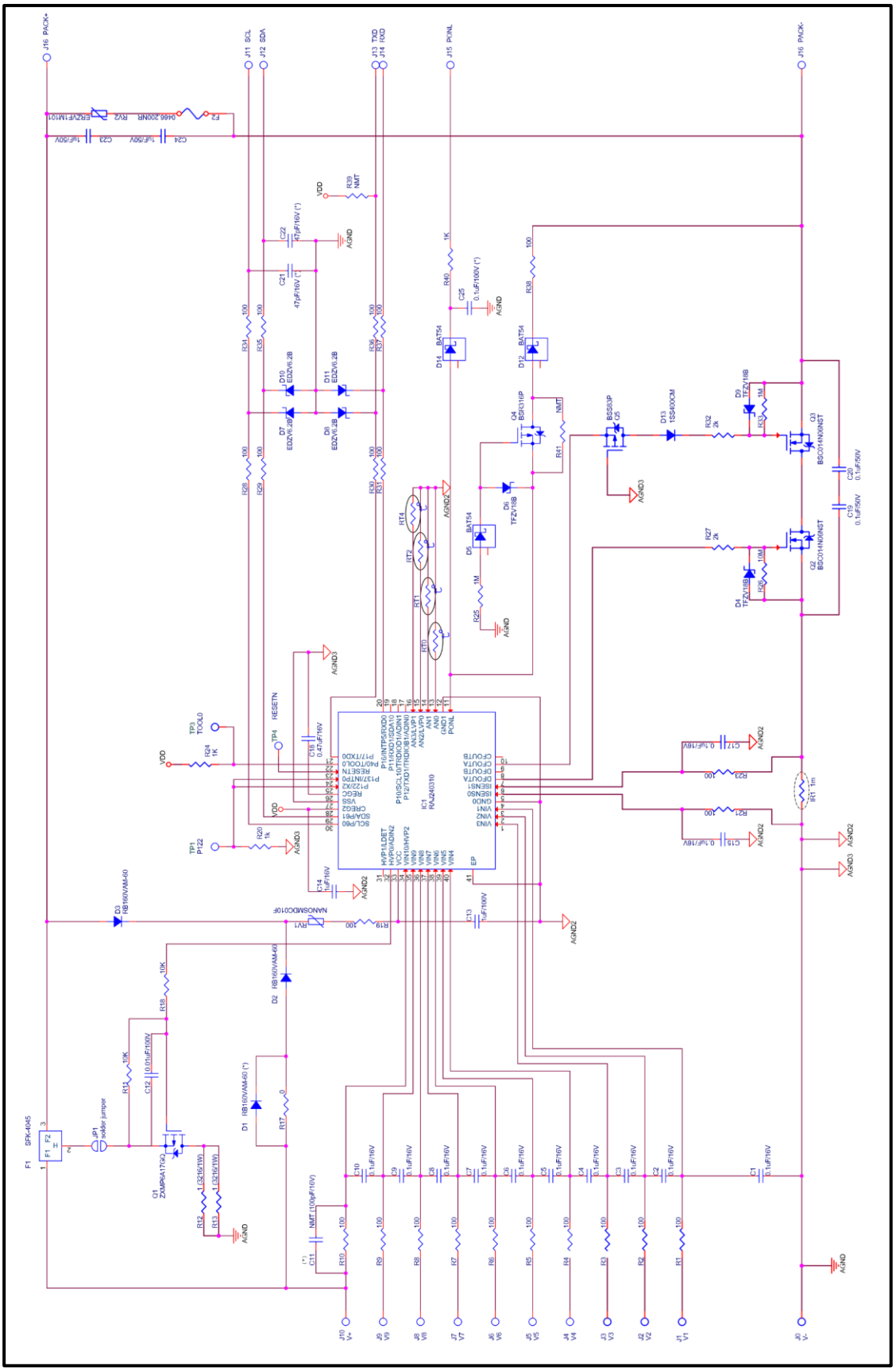
6. APPLICATION GUIDELINE

6.1 Typical Application Specification

A typical specification example of Li-ion battery management unit as shown below.
From the next page, the typical application guideline is explained for RAJ240310.

Battery cell assembly	10S1P	
Host Interface	System Management Bus (SMBus) Specification, version 1.1. UART	
Primary protection	Charge FET and Discharge FET	
Secondary protection	Fuse blow by FGIC or a secondary protection device.	
Connect pins	Pack+	Positive battery pack terminal
	SCL	SMBus clock
	SDA	SMBus data
	UART	UART communication port
	PONL	High voltage port for battery power on
	Pack-	Negative battery pack terminal
Additional Features	External reverse charge protection circuit Battery and charge/discharge MOSFET temperature measurement with three thermistors	

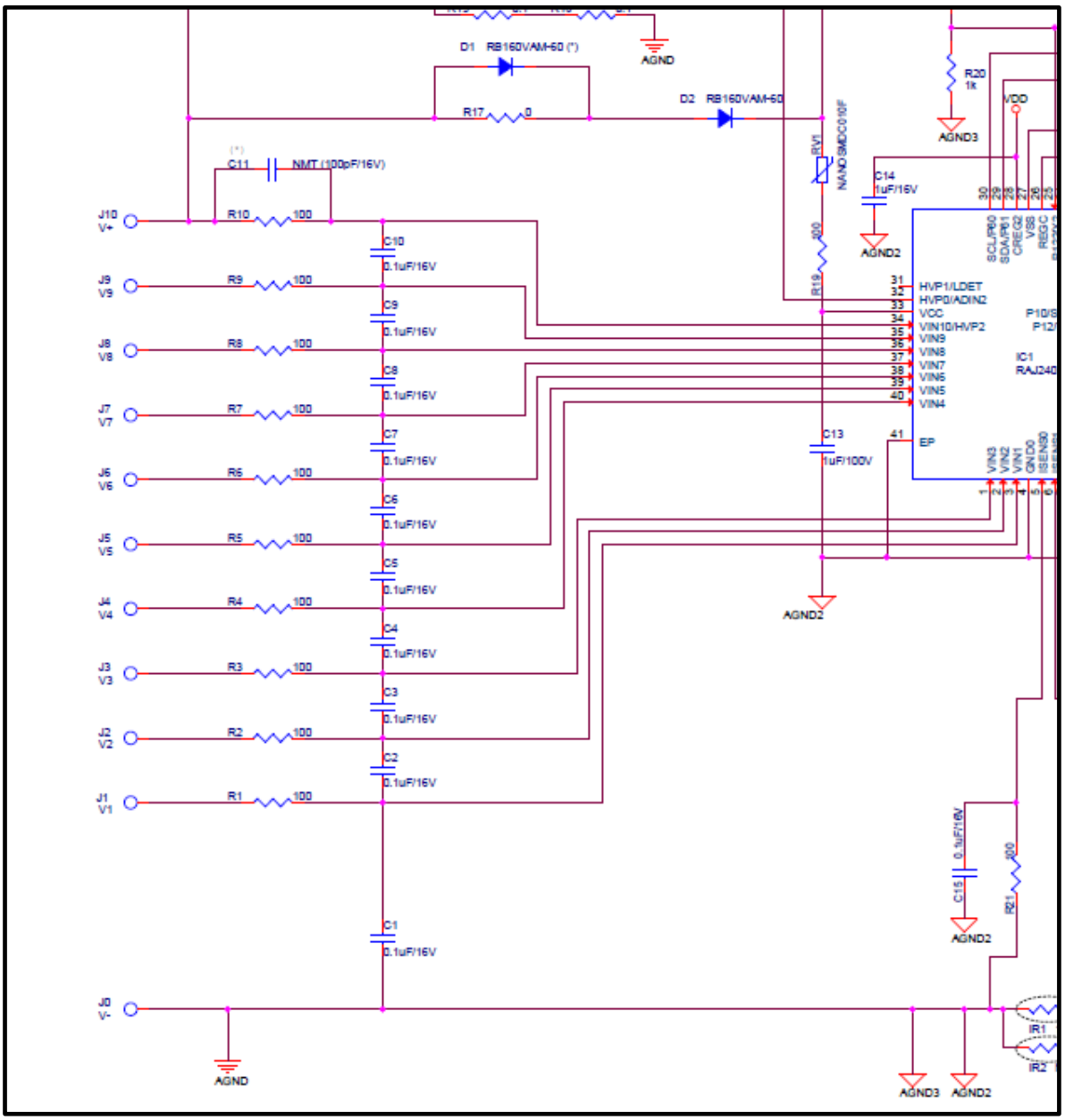
6.2 Typical Application Circuit



6.3 Circuit Design Guideline

6.3.1 Cell voltage monitor circuit

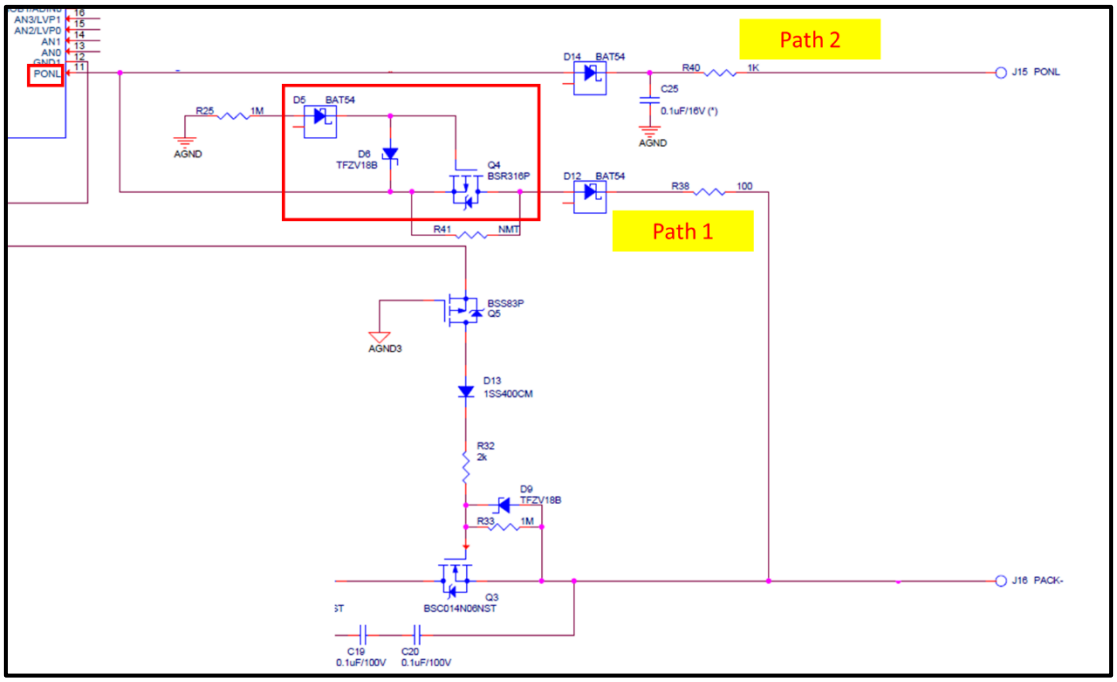
- Place an input filter between FGIC's VIN port and each of the cells.
- Place resistors valued approximately 100Ω and capacitors valued around 0.1uF to VIN1 - VIN10 for surge protection. It is necessary to calculate the cut-off frequency and use correct resistance and capacitance value based on application.



6.3.2 Battery power on circuit

- Path 1 is for Charger presence detection. Path 2 can be used for trigger pull detection.
- Place Diode (D14) that Path 2 input does not affect Path 1.
- Place Diode (D12) for reverse input protection and D5, D6 and Q4 is used for negative voltage input protection.
- Place CR filter (1KΩ, 0.1uF) on Path 2 to PONL for surge protection.

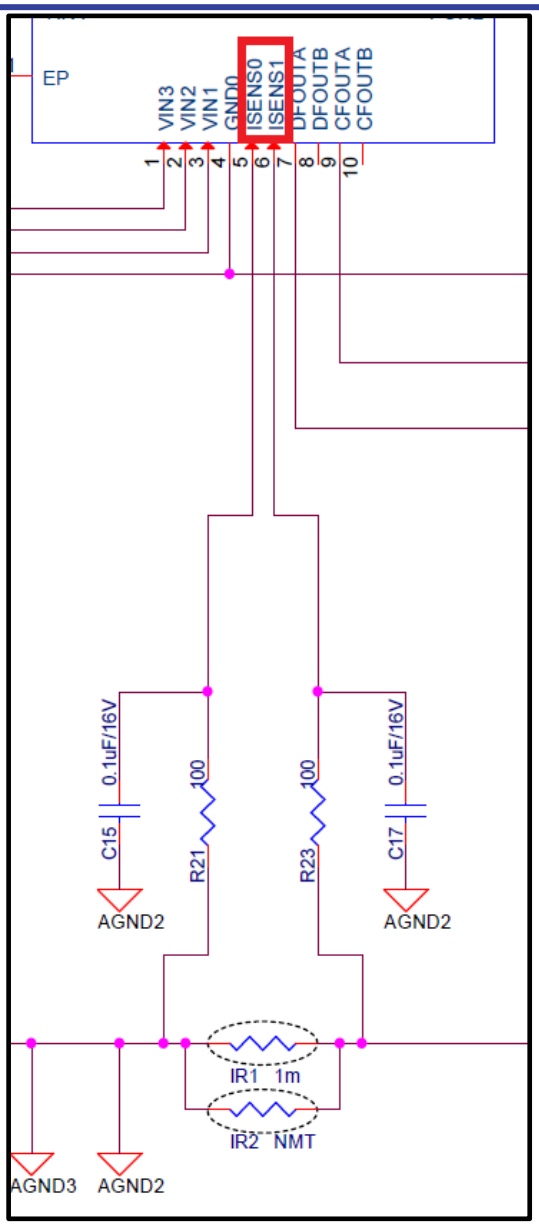
  It is necessary to calculate cut-off frequency and use correct resistance and capacitance value based on application.



6.3.3 Current monitor

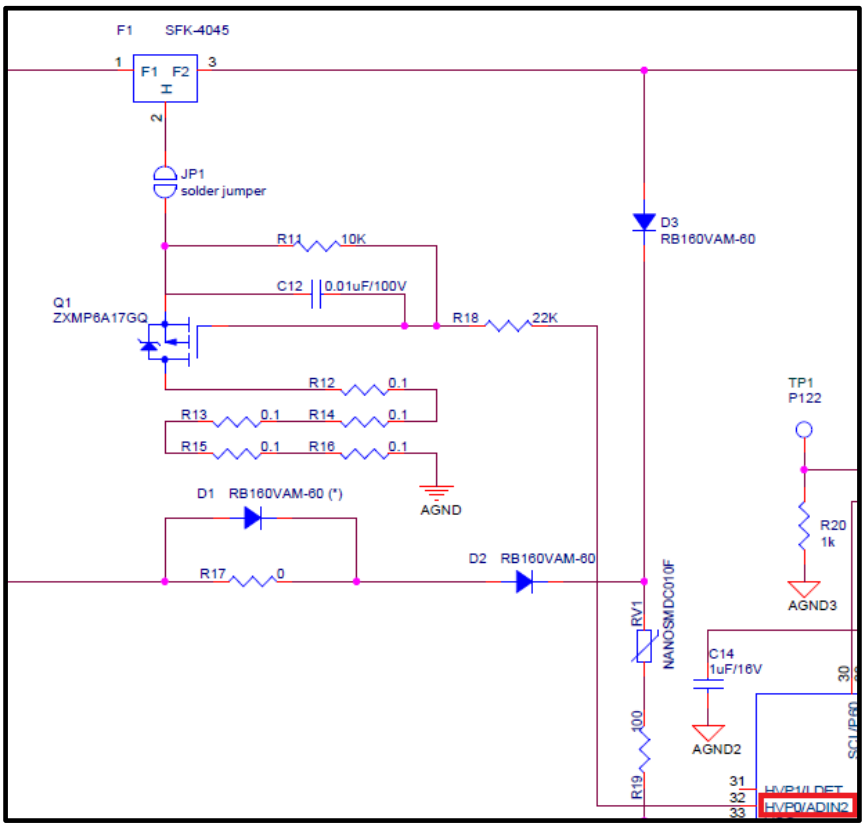
- Potential difference on the sense resistor is monitored by current integration circuit.
- Place a Low Pass Filter (100Ω, 0.1uF) at input stage.

  LPF's ground should be connected from a place close to FGIC ground (GND0/1).
- Sense lines should be shielded if small voltage difference is detected to ensure high accurate current sensing.


EP
VIN3
VIN2
VIN1
GND0
ISENS0
ISENS1
DFOUTA
DFOUTB
CFOUTA
CFOUTB
1
2
3
4
5
6
7
8
9
10
0.1uF/16V
C15
100
R21
100
R23
0.1uF/16V
C17
AGND2
AGND2
IR1 1m
IR2 NMT
AGND3
AGND2

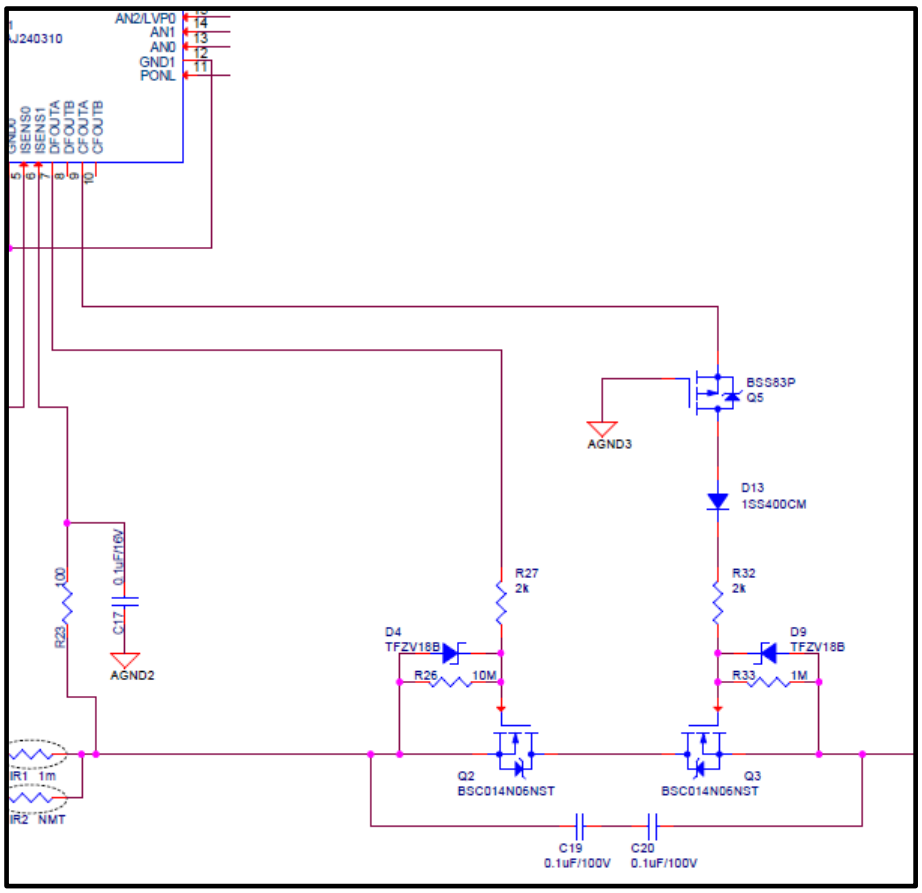
6.3.4 Fuse control

- Self-control protector (SCP) is used for fuse in reference circuit.
- The fuse will blow when RAJ240310 drives HVP0 (High voltage GPIO) pin low to make Q1 ON.
- The fuse will blow when overcurrent exceeds the limit of SCP.
- R12 – R16 are used for battery electrochemical migration short circuit countermeasures.



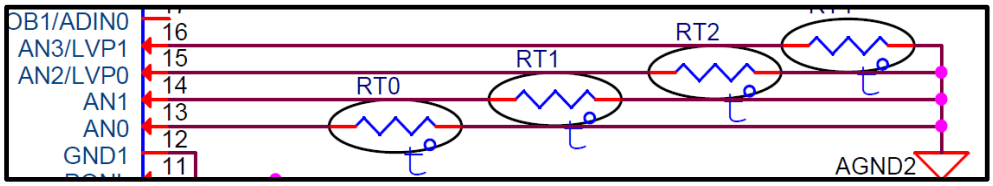
6.3.5 C-FET and D-FET control

- R27 and R32 are use as gate protection and C-FET/D-FET noise reduction. (2kΩ is recommended.)
- R26 and R33 are used to fix C-FET/D-FET gate voltage in order to keep stable off state when FET is turn off. 10MΩ is recommended for DFET control and 1MΩ is recommended for CFET control.
- D4 and D9 is for Q2 and Q3 protection.
- Q5 is used for negative voltage protection and D13 is used to prevent reverse input from the system.



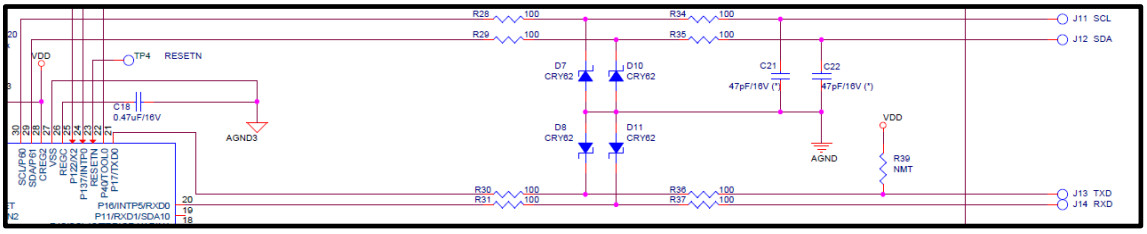
6.3.6 Thermistor inputs

- ADC voltage measurement pins (AN0, AN1, AN2, AN3) are assigned for thermistor.



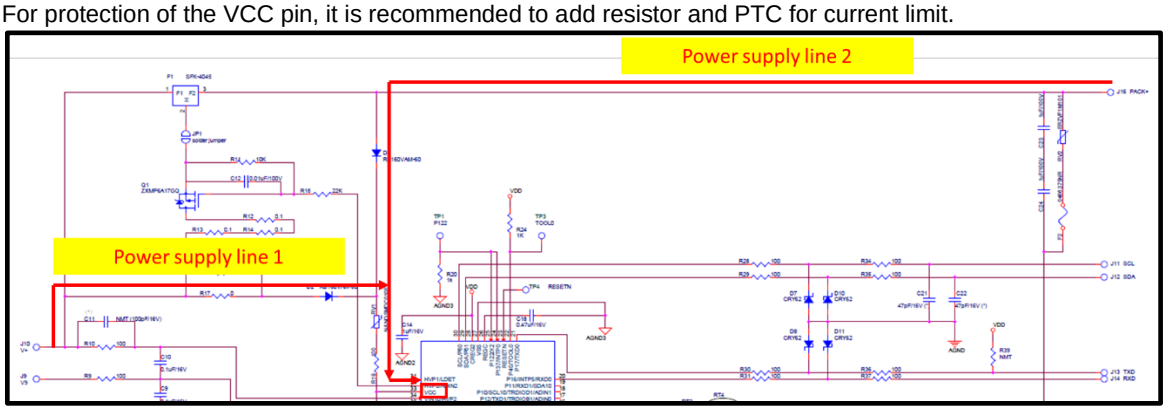
6.3.7 Communication line

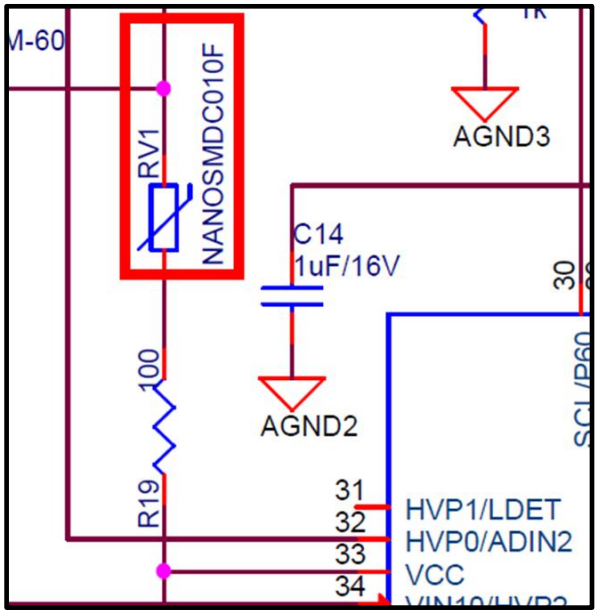
- RAJ240310 support 2 kinds of communication, SMBus and UART.
- For electrical over stress countermeasure, input 100Ω, 100Ω resistor, Zener diode, and capacitance are recommended in SMBus communication line.
- For UART communication, P16 and P17 pins have VDD output circuit, therefore RXD/TXD line pull up voltage should be the same as VDD.



6.3.8 Power supply path

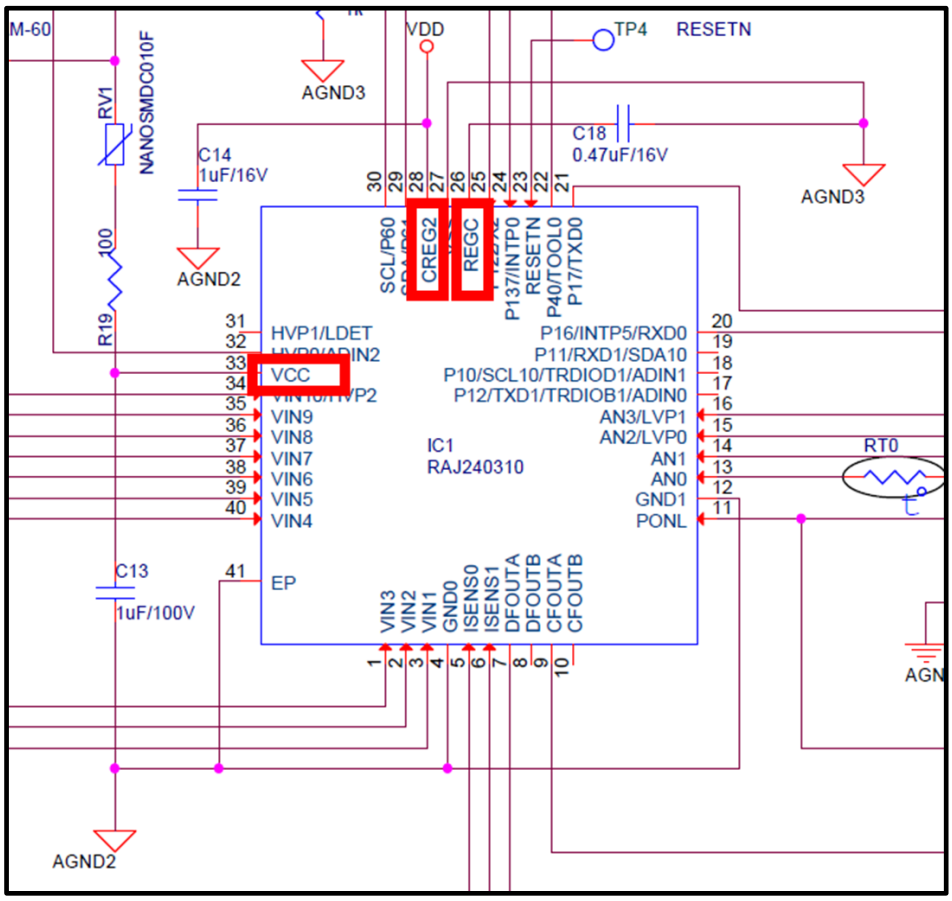
- Power is supplied to VCC through the following two paths depending on circumstance.
- Power supplied from battery side when fuse is blown. See power supply line 1.
- Higher output voltage from battery and charger is used as power supply. See power supply line 2.
- For protection of the VCC pin, it is recommended to add resistor and PTC for current limit.





6.3.9 VCC, CREG2, and REGC capacitance

- The following decoupling capacitors must be located adjacent to each terminal.
- C13: VCC (1uF is recommended.)
- C14: CREG2 (1uF is recommended.)
- C18: REGC (0.47uF is recommended.)



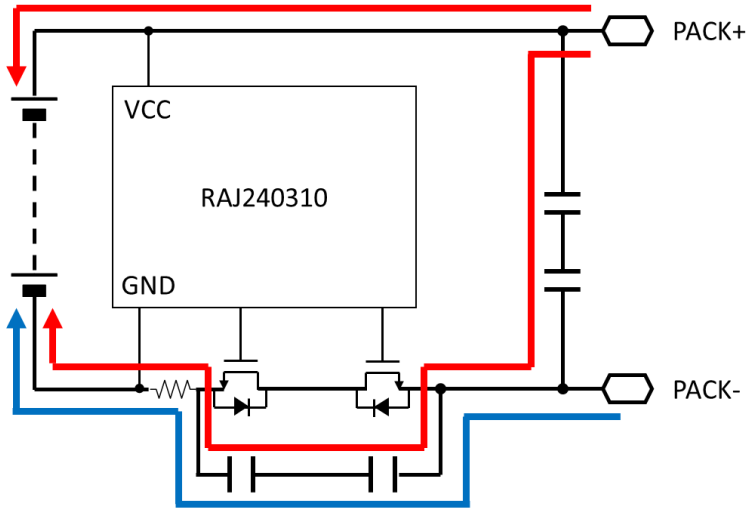
6.4 Layout Guidelines

6.4.1 Summary

- Large current patterns must be wide and short to minimize voltage drop and heat generation.
- Bypass capacitors must be mounted as close as possible to the device VCC and GND pins to prevent erroneous operation due to noise from power supply.
- Capacitors for voltage regulators must be located close to regulator pins to ensure loop stability and ESD tolerance.
- All IC ground must be connected to the negative terminal of battery cells except ground for communication lines.
- Communication lines must be away from small signal current sense line to prevent the input signal from being disturbed by the incoming radiation noise.
- To decrease parasitic PCB impedance and improve tolerance against noise, it is preferred to enhance ground pattern as much as possible.
- FGIC (RAJ240310) must be located away from any heat source (FET, current sense resistor and large current patterns) to minimize the influence of heat.

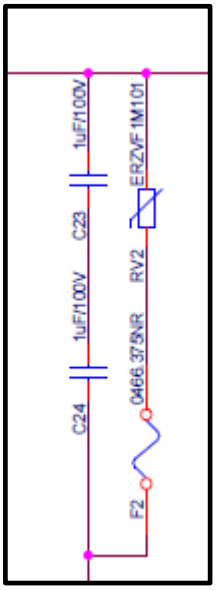
6.4.2 ESD protections on each terminal (basic policy)

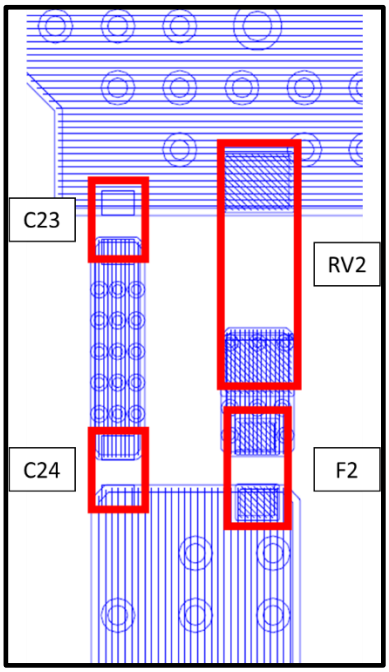
- ESD on Pack+ terminal must be discharged to the top side of the cell or to Pack- terminal through a capacitor.
- ESD on Pack- terminal must be discharged to the GND side of the cell.
- ESD on communication terminals and other GPIOs must be discharged to the GND side of the cell via Pack- terminal.
- The noise from PACK+ or PACK- must be discharged to the battery cells so that it will not interfere with FGIC functions and measurements.



6.4.3 Pack+, Pack- (Noise protection element)

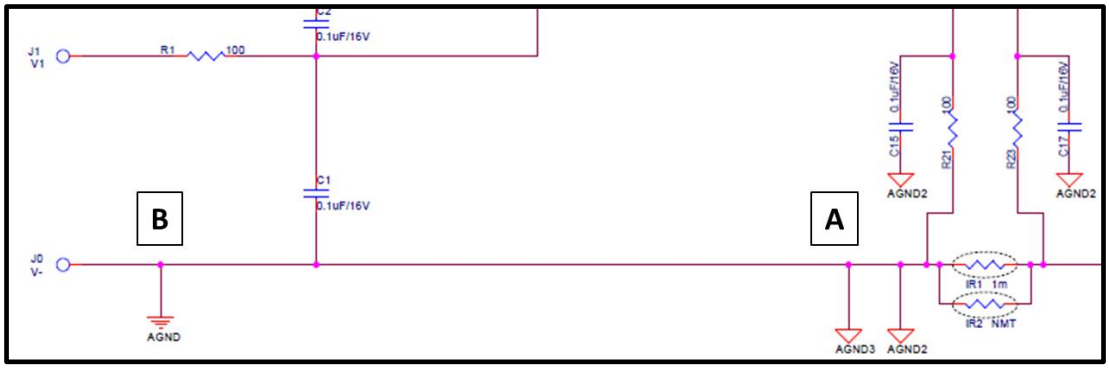
- A bypass capacitor must be placed between Pack+ and Pack-. (Countermeasure against ESD)
- A bypass capacitor must be located adjacent to Pack+, Pack-. (Minimize the ESD influence)
- Capacitors must be placed in series. (Countermeasure against short-circuit of capacitors)
- Don’t use tantalum capacitor. (Tantalum capacitor can end up with short-circuited failure when damaged.)
- For the terminal protection against noise and overvoltage, It is recommended to add varistor or TVS diode. (RV2)
- It is recommended to add Fuse to prevent short circuit. (F2)
- C23, C24, RV, F2 must be placed as short as possible between PACK + and PACK-. However, be careful not to narrow the distance between Pack + and Pack-.

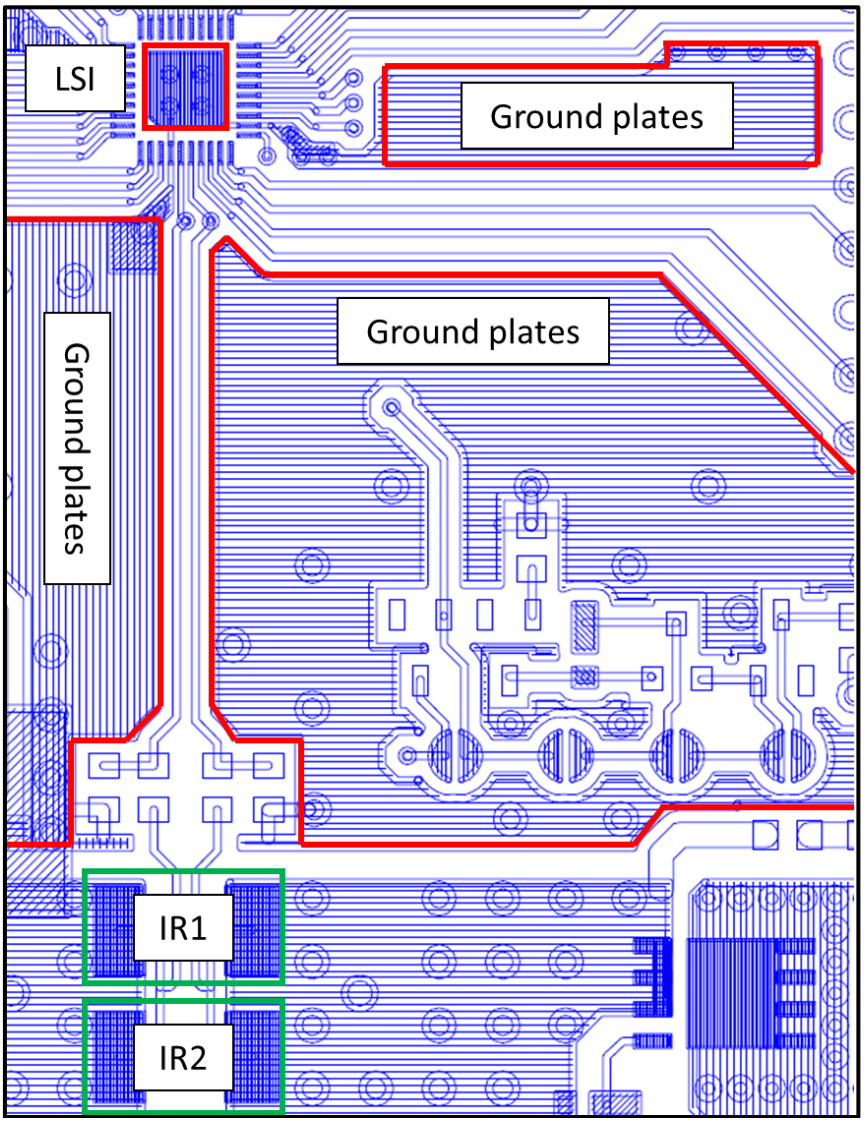




6.4.4 GND connection

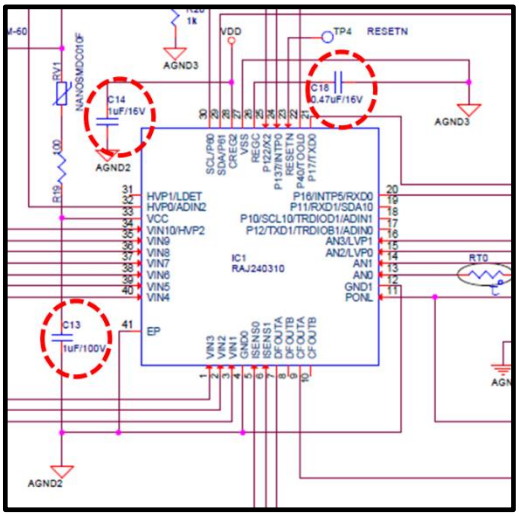
- Each analog GND of FGIC should be connected to the point (A) of current detection resistor of the cell side by the pattern with an adequate width. (Prevent potential variation by large current.)
- Minimize parasitic impedance between point (A) and (B).
- Minimize parasitic impedance between GND0 and GND1.
- Secure ground plates to improve noise immunity.

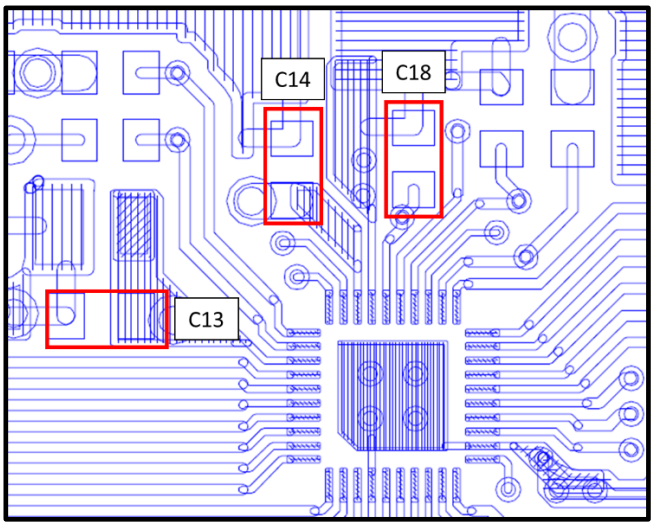




6.4.5 Bypass capacitor between VCC/VDD/CREG2/REGC and GND0/GND1/VSS

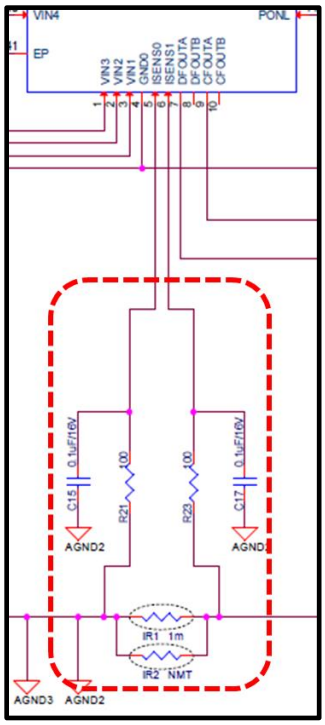
- The patterns between VCC/CREG2 pin and GND0/1 pin, and VDD/REGC pin and VSS pin, a bypass capacitor is connected and the path must be as short as possible. (Countermeasure for ESD, EMC noise and etc.)
- The lines to bypass capacitor must be wide and short. (To keep bypass capacitor effective in suppressing the potential variation.)

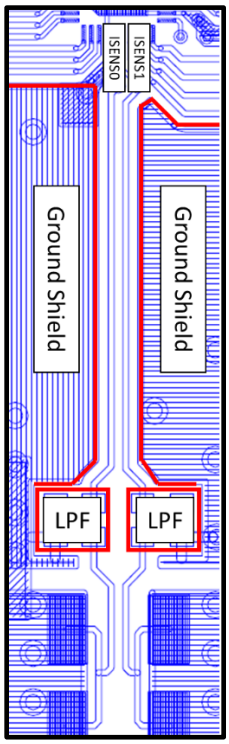




6.4.6 Current Monitor (ISENS0, ISENS1)

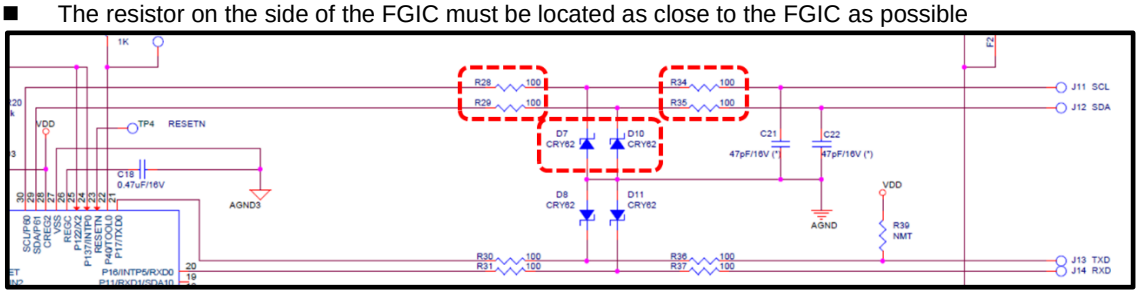
- Two lines from current sense resistor to ISENS0, ISENS1 must be the same in width and length, and in parallel with the same space between the two lines. (Prevent erroneous detections due to noise).
- LPF (100Ω and 0.1 uF) and a shield pattern should be placed to ISENS0/1 lines. (Countermeasure against noise)





6.4.7 Communication line (SMBus)

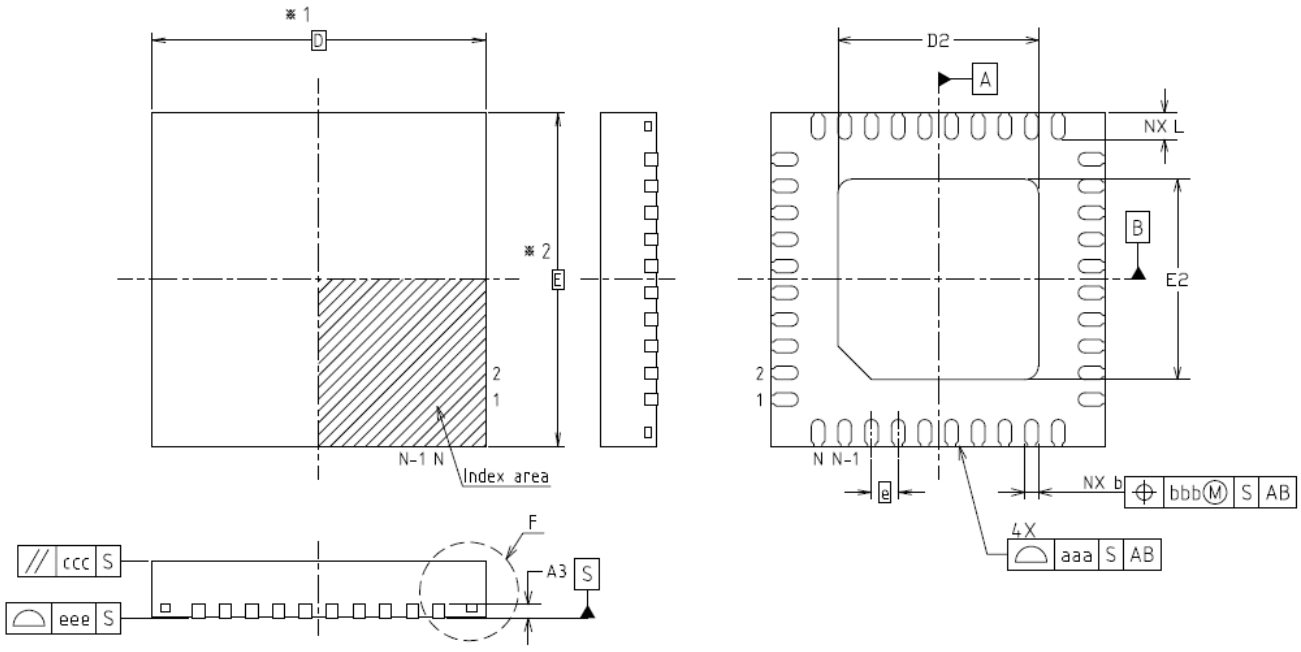
- SMBus lines must be equipped with Zener diodes. And it is necessary to mount resistors on the side of FGIC and pack connecter. (Zener diode and the resistor on the side of connector are for surge countermeasures, the resistor on the side of FGIC for noise countermeasure.)
- The resistor on the side of the FGIC must be located as close to the FGIC as possible

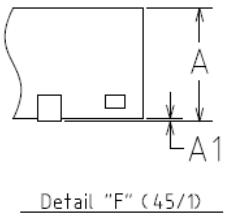


6.4.8 Unused Pins

- Unused pins are recommended to be connected to GND via resistors as ESD countermeasure. (Setting low output by software prevents the terminal from becoming indefinite).

7. PACKAGE OUTLINE





Detail "F" (45/1)

*1,2…Not include resin residue.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
A	——	——	0.95
A1	——	——	0.05
A3	0.20 REF		
b	0.15	0.20	0.25
L	0.30	0.40	0.50
e	0.40		
N	40		
D2	——	3.00	——
E2	——	3.00	——
D	5.00		
E	5.00		
aaa	0.20		
bbb	0.10		
ccc	0.10		
eee	0.08		

REVISION HISTORY

Rev.	Date	Page	Description
1.00	May 31, 2021	-	First release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on Processing during Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate undetermined and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states state of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for possible future expansion of functions only. Do not access these addresses; the correct operation of LSI will not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, the reset line will only be released after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, system-evaluation test needs to be implemented for the given product.

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