

# RAJ2810024H12HPD

## Intelligent Power Device for automotive application

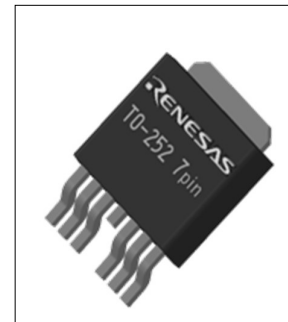
### 1. Overview

RAJ2810024H12HPD is a 2.3mΩ single channel Intelligent Power Device (IPD) available in a TO252-7 package. This device is a 4.5V to 28V N-channel High-Side Switch (HSS) with a charge pump, diagnostic feedback and integrated protection function. It is designed for use in automotive 12V systems.

The RAJ2810024H12HPD helps reduce power losses in the vehicle thanks to its 0.5uA standby current, which makes it suitable for use in power distribution switches, heaters, and glow plugs.

### 1.1 Features

- Improved current sense accuracy with offset cancelation (+9.5%/-11% @30A)
- Keep on-resistance during cranking condition (max 4mΩ@3.2V/24ms/25°C)
- Low standby current (0.5uA max @25°C )
- Short circuit protection
  - Shutdown by over current detection
  - Shutdown by absolute channel over temperature detection
- Built-in diagnostic function
  - Proportional load current sensing
  - Defined fault signal in case of abnormal load condition
- Reverse battery protection by self-turn ON
- Loss of ground protection
- Von clamp operation at inductive load switch-off
- AEC-Q100 Grade 1 qualified
- Built-in charge pump
- 3.3V compatible logic interface



### 1.2 Product summary

**Table 1 Product summary**

Parameter	Symbol	Values
Operating Voltage	Vcc	4.5V to 28V
On-state resistance at 25°C	Ron	Typ. 2.3 mΩ, Max. 3.0 mΩ
Inductive load switch-off energy dissipation single pulse	EAS	170mJ
Inductive load switch-off energy dissipation repetitive pulse	EAR	50mJ
Over current detection current1	IL1(SC)	Min. 70A, Typ. 106A
Over current detection current2	IL2(SC)	Min. 95A, Typ. 125A
Current sense ratio with offset cancel at IL=30A	KILIS	Min. 57000 Typ. 64000, Max. 70000

### 2. Ordering Information

**Table 2 Ordering Information**

Part No.	Lead plating	Packing	Package
RAJ2810024H12HPD	Pure Matte Sn	Tape 2500pcs/reel	TO252-7

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### 3. Specification

#### 3.1 Block Diagram

##### 3.1.1 Nch High-side Single Channel Device Block Diagram

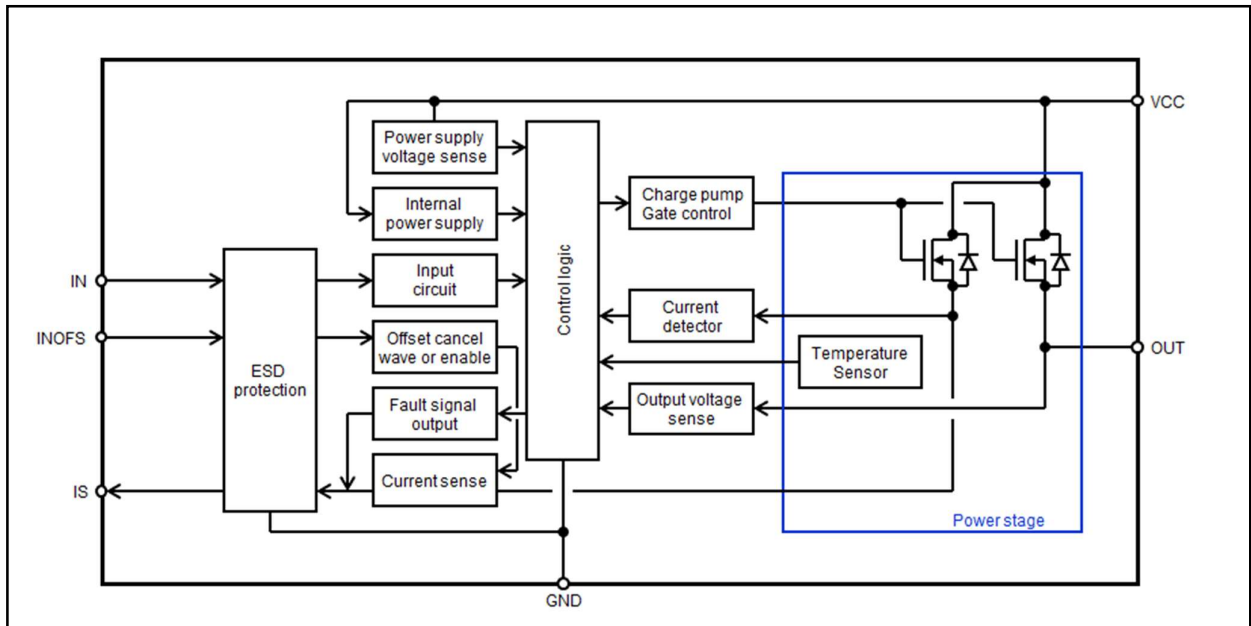


Figure 1 Block Diagram of RAJ2810024H12HPD

##### 3.1.2 Voltage and Current Definition

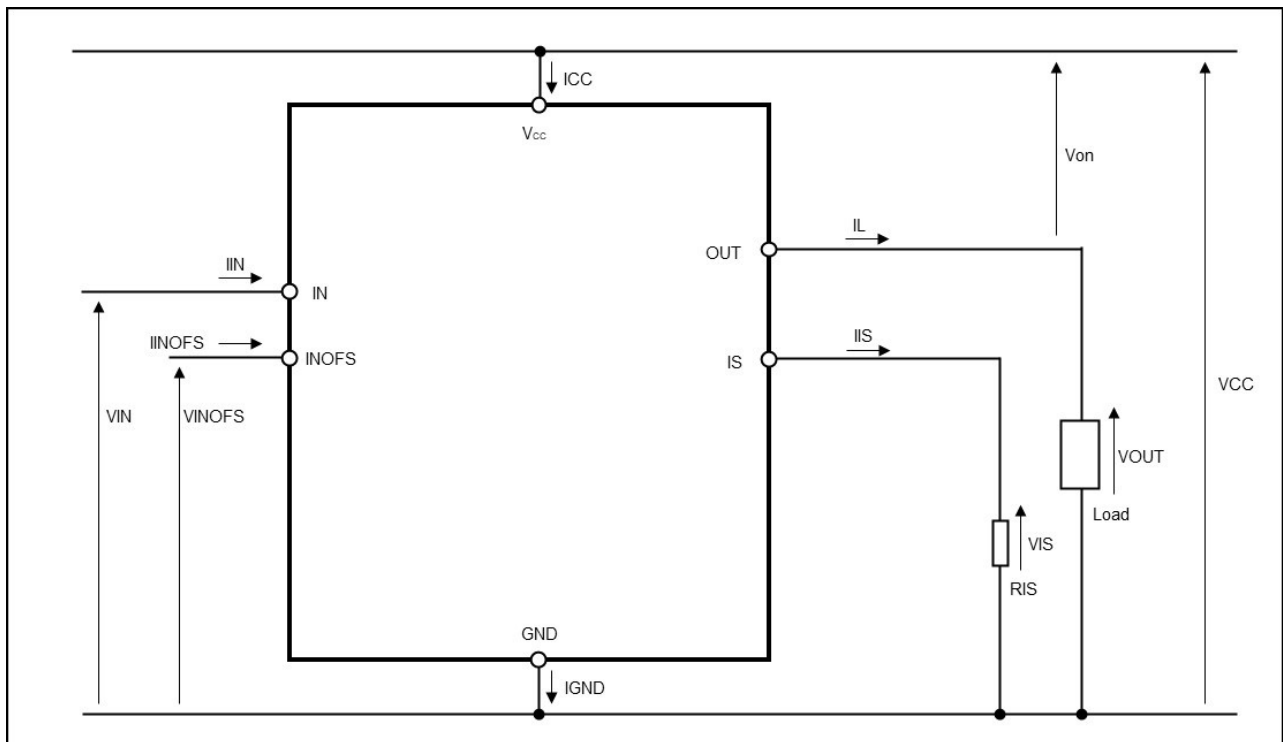
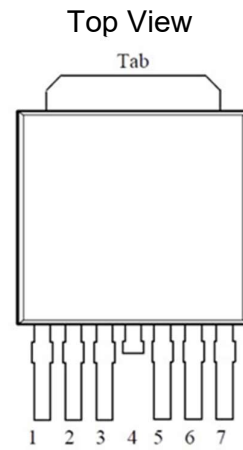


Figure 2 Voltage and Current Definition

### 3.2 Pin Configuration

**Table 3 TO252-7 Pin Configuration**

Pin No.	Terminal Name
1	OUT
2	GND
3	IN
4, Tab	VCC
5	IS
6	INOFS
7	OUT



**Figure 3 Pin Configuration**

**Table 4 Pin function**

Terminal Name	Pin function	Recommended connection	
		Sense current improved accuracy function enabled	Sense current improved accuracy function disabled
GND	Ground connection	Connected to GND through a 47Ω resistor	
IN	Input signal for channel activation Active high	Connected to MCU's output port through a 2k-50kΩ serial resistor	
IS	Current sense and Diagnosis output signal	Connected to GND through a 1k-6kΩ resistor with LPF. Refer to chapter 6.	Connected to GND through a 1k-6kΩ resistor.
		Connect the resistor even if this pin is not used.	
OUT	Protected high-side power output	Connected to load with 50-100nF capacitor in parallel.	
VCC	Positive power supply for logic supply as well as output power supply	Connected to battery voltage with 22nF capacitor in parallel. Refer to chapter 6.	
INOFS	Input signal for sense current improved accuracy Active high	Connected to MCU's output port through a 2k-50kΩ serial resistor to use sense current improved accuracy function.	This pin should be open.

### 3.3 Absolute Maximum Ratings

Stress values that exceed those listed here may cause permanent damage to the device. Exposure to absolute maximum rating condition for extended periods may affect device reliability. Integrated protection functions are designed to prevent IC destruction under fault condition described in the data sheet. Fault conditions are considered as out of normal operation.

**Table 5 Absolute Maximum Ratings**

Ta=25°C, unless otherwise specified

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
VCC Voltage	VCC	-	-	28	V	
VCC Voltage at reverse battery condition	-VCC	-	-	16	V	At nominal load current, t<2min, RIN=2kΩ, RIS=1kΩ, RGND=47Ω
VCC voltage under Load Dump condition	Vload dump	-	-	35	V	RI=1Ω, RL=Nominal load, RIS=1kΩ, RIN=2kΩ, RGND=47Ω, td=400ms
Load Current	IL	-	-	Self-limited	A	
Total power dissipation for whole device (DC)	PD	-	-	1.85	W	Ta=85°C Device on 50mmx50mmx1.5mm epoxy PCB FR4 with 6 cm2 of 70 um copper area
Voltage at IN/INOFS pin	VIN	-2	-	16	V	DC RIN=2kΩ
	VINOFS	-16	-	-		At reverse battery condition, t<2min, RIN=2kΩ
IN/INOFS pin current	IIN	-	-	10	mA	DC
	IINOFS					
Voltage at IS pin	VIS	-2	-	VCC	V	DC RIS=1kΩ
		-16	-	-	V	At reverse battery condition, t<2min, RL= Nominal load, RIS=1kΩ
Channel Temperature	Tch	-40	-	150	°C	
Storage Temperature	Tstg	-55	-	150	°C	
Inductive load switch-off energy dissipation single pulse	EAS	-	-	170	mJ	VCC=13.5V, T <sub>ch, start</sub> <sup>1)</sup> <150°C, RL=Nominal load, Refer to 3.7.12
Inductive load switch-off energy dissipation repetitive pulse	EAR	-	-	50	mJ	VCC=13.5V, T <sub>ch, start</sub> <sup>1)</sup> =85°C, RL=Nominal load, Refer to 3.7.12

Remark) All voltages refer to ground pin of the device.

1) T<sub>ch, start</sub> means T<sub>ch</sub> at the start of the test.

### 3.4 ESD

**Table 6 ESD**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition		
ESD susceptibility	VESD	-2000	-	2000	V	HBM	AEC-Q100-002 std. R=1.5kΩ, C=100pF	All pin
		-4000	-	4000			IEC61000-4-2 std. R=330Ω, C=150pF, 100nF at VCC and OUT	

### 3.5 Thermal Characteristics

**Table 7 Thermal Characteristics**

Parameter	Symbol	Min.	Typ.	Max.	Unit	Test Condition
Thermal characteristics	Rth(ch-a)	-	35	-	°C/W	According to JEDEC JESD51-2, -5, -7 on FR4 2s2p board
	Rth(ch-c)	-	0.65	-	°C/W	

### 3.6 Electrical Characteristics

**Table 8 Operation function**

$T_{ch}=-40$  to  $150^{\circ}\text{C}$ ,  $V_{CC}=7$  to  $18\text{V}$ , unless otherwise specified  
 Typ:  $T_{ch}=25^{\circ}\text{C}$ ,  $V_{CC}=13.5\text{V}$  unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Operating Voltage	VCC	4.5	-	28	V	$V_{IN}=4.5\text{V}$ , $R_L$ =Nominal load, Refer to 3.7.12
Operating current	IGND	-	3.4	6.8	mA	$V_{IN}=4.5\text{V}$
Output Leakage current	IL (off)	-	-	0.2	$\mu\text{A}$	$T_{ch}=25^{\circ}\text{C}$
		-	-	5		$T_{ch}=-40$ to $125^{\circ}\text{C}$
Standby current	ICC (off)	-	-	0.5	$\mu\text{A}$	$T_{ch}=25^{\circ}\text{C}$
		-	-	1.5		$T_{ch}=-40$ to $85^{\circ}\text{C}$
On-state resistance	Ron	-	2.3	3.0	m $\Omega$	$T_{ch}=25^{\circ}\text{C}$
		-	-	4.8		$T_{ch}=150^{\circ}\text{C}$
Low level IN/INOFS pin voltage	VIL VILOFS	-	-	0.8	V	
High level IN/INOFS pin voltage	VIH VIHOFS	2.5	-	-	V	
Low level IN/INOFS pin current	IIL IILOFS	2	-	30	$\mu\text{A}$	$V_{IN}=0.8\text{V}$ $V_{INOFS}=0.8\text{V}$
High level IN/INOFS pin current	IIH IIHOFS	2	-	30	$\mu\text{A}$	$V_{IN}=2.5\text{V}$ $V_{INOFS}=2.5\text{V}$
Clamping IN/INOFS pin voltage <sup>1)</sup>	VZIN VZINOFS	5	6	-	V	
Operating current at cranking	IGND (cr)	-	0.5	-	mA	$V_{CC}=3.2\text{V}$ , $R_{GND}=47\Omega$ , $R_L$ = Nominal load, Pulse duration=24ms, Refer to 3.7.12
Cranking mode voltage	VCC (cr)	-	-	4.5	V	
On-state resistance at cranking	Ron(cr)	-	-	4.0	m $\Omega$	$V_{CC}=3.2\text{V}$ , $R_{GND}=47\Omega$ , $T_{ch}=25^{\circ}\text{C}$ , $R_L$ = Nominal load, Pulse duration=24ms, Refer to 3.7.3 and 3.7.12
Operating Voltage range for cranking	VCC (Uv,cr)	3.2	-	-	V	$R_{GND}=47\Omega$ , $T_{ch}=25^{\circ}\text{C}$ , Pulse duration=24ms, $R_L$ =Nominal load, Refer to 3.7.12
Operation start voltage	VCC (start)	-	-	4.5	V	
Turn on time	ton	-	260	550	$\mu\text{s}$	$V_{CC}=13.5\text{V}$ , $R_L$ =Nominal load, Refer to 3.7.12 $T_{ch}=25^{\circ}\text{C}$ to $150^{\circ}\text{C}$
Turn on delay time	td(on)	-	75	150	$\mu\text{s}$	
Turn off time	toff	-	190	420	$\mu\text{s}$	
Turn off delay time	td(off)	-	135	290	$\mu\text{s}$	
Slew rate on	dV/dton	-	0.10	0.4	V/ $\mu\text{s}$	
Slew rate off	-dV/dtoff	-	0.28	0.83	V/ $\mu\text{s}$	
Turn on time	ton	-	250	550	$\mu\text{s}$	$V_{CC}=13.5\text{V}$ , $R_L$ =Nominal load, Refer to 3.7.12 $T_{ch}=-40^{\circ}\text{C}$
Turn on delay time	td(on)	-	80	160	$\mu\text{s}$	
Turn off time	toff	-	220	550	$\mu\text{s}$	
Turn off delay time	td(off)	-	165	430	$\mu\text{s}$	
Slew rate on	dV/dton	-	0.12	0.4	V/ $\mu\text{s}$	
Slew rate off	-dV/dtoff	-	0.29	0.83	V/ $\mu\text{s}$	
Turn on energy loss <sup>1)</sup>	Eon	-	15	-	mJ	$V_{CC}=13.5\text{V}$ , $T_{ch}=25^{\circ}\text{C}$ , $R_L$ =Nominal load, Refer to 3.7.12
Turn off energy loss <sup>1)</sup>	Eoff	-	5	-	mJ	
Driving capability <sup>1)</sup>	Dr(capa)	153	-	-	m $\Omega$	$V_{CC}=16.0\text{V}$ , $T_{ch}=25^{\circ}\text{C}$

Remark) All voltages refer to ground pin of the device.

1) not subjected production test, guaranteed by design

**Table 9 Protection function**

$T_{ch}=-40$  to  $150^{\circ}\text{C}$ ,  $V_{CC}=7$  to  $18\text{V}$ , unless otherwise specified  
 Typ:  $T_{ch}=25^{\circ}\text{C}$ ,  $V_{CC}=13.5\text{V}$  unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Over current detection current1	IL1(SC)	70	106	-	A	$V_{CC}=13.5\text{V}$ , $V_{on}=5\text{V}$ , $T_{ch}=25^{\circ}\text{C}$
Over current detection Current2	IL2(SC)	95	125	-	A	$V_{CC}=13.5\text{V}$ , $V_{on}<V_{on}(\text{kilis})$ , $T_{ch}=25^{\circ}\text{C}$
Sense current output trigger threshold	$V_{on}(\text{kilis})$	-	0.5	-	V	$V_{CC}=13.5\text{V}$ , $T_{ch}=25^{\circ}\text{C}$
Von check in over current state	$V_{on}(\text{OC})$	-	0.4	-	V	$V_{CC}=13.5\text{V}$ , $T_{ch}=25^{\circ}\text{C}$
Turn on check delay in over current state	tdOC (OC)	0.8	1.4	2.1	ms	$V_{CC}=13.5\text{V}$ , $T_{ch}=25^{\circ}\text{C}$ , Over Current state
Von check at cranking in over current state	$V_{onCR}(\text{OC})$	-	0.2	-	V	$V_{CC}=3.2\text{V}$ , $T_{ch}=25^{\circ}\text{C}$
Absolute thermal shutdown temperature	aTth	150	-	-	$^{\circ}\text{C}$	
Von clamp voltage at inductive load switch-off	$V_{on,clamp}$	35	43	47	V	$V_{CC}=13.5\text{V}$ , $I_L=40\text{mA}$ , $T_{ch}=25^{\circ}\text{C}$
Output current while GND disconnection	IL(GND)	-	-	1	mA	$I_{IN}=0\text{A}$ , $I_{GND}=0\text{A}$ , $I_{IS}=0\text{A}$ , $I_{INOF5}=0\text{A}$
On-state resistance at reverse battery condition	Ron(rev)	-	2.3	3.0	m $\Omega$	$T_{ch}=25^{\circ}\text{C}$
		-	-	4.8		$T_{ch}=150^{\circ}\text{C}$
GND current at reverse battery condition	IGND (rev)	-	-2	-	mA	$V_{CC}=-16\text{V}$ , $T_{ch}=25^{\circ}\text{C}$

Remark) All voltages refer to ground pin of the device.  
 Protection functionality is kept  $V_{CC}=6\text{V}$  min.

**Table 10 Diagnosis function**  $T_{ch}=-40$  to  $150^{\circ}\text{C}$ ,  $V_{CC}=7$  to  $18\text{V}$ ,  $V_{IN}=4.5\text{V}$ , unless otherwise specified  
 Typ:  $T_{ch}=25^{\circ}\text{C}$ ,  $V_{CC}=13.5\text{V}$  unless otherwise specified

Parameter	Symbol	Min	Typ	Max	Unit	Test Condition
Current sense ratio	KILIS	56000	64000	70500	-	$I_L=4\text{A}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func)
		57000	64000	70000	-	$I_L=10\text{A}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func) <sup>1)</sup>
		57000	64000	70000	-	$I_L=15\text{A}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func) <sup>1)</sup>
		57000	64000	70000	-	$I_L=30\text{A}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func)
		28000	64000	105000	-	$I_L=4\text{A}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func)
		42000	64000	86000	-	$I_L=10\text{A}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func) <sup>1)</sup>
		48000	64000	80000	-	$I_L=15\text{A}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func) <sup>1)</sup>
		53000	64000	75000	-	$I_L=30\text{A}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func)
Current sense drift depends on temperature	dKILIS	-6	-	4	%	$V_{CC}=13.5\text{V}$ , $T_{ch, start}=25^{\circ}\text{C}$ , $I_L=30\text{A}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func), Refer to 3.7.12
		-10	-	10	%	$V_{CC}=13.5\text{V}$ , $T_{ch, start}=25^{\circ}\text{C}$ , $I_L=30\text{A}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func), Refer to 3.7.12
Offset current of sense current	lis,offset	-	-	2.5	$\mu\text{A}$	$I_L=0\text{A}$ , $T_{ch}=25^{\circ}\text{C}$ , $V_{IN}OFS=4.5\text{V}$ (use improved accuracy func)
		-	-	20	$\mu\text{A}$	$I_L=0\text{A}$ , $T_{ch}=25^{\circ}\text{C}$ , $V_{IN}OFS=0\text{V}$ (no use improved accuracy func)
Sense voltage under fault condition	Vis,fault	4.5	5.6	7.0	V	$R_{IS}=1\text{k}\Omega$
Sense current settling time after input signal positive slope	tsis(on)	-	460	700	$\mu\text{s}$	$V_{CC}=13.5\text{V}$ , $V_{IN}=0\text{V}$ to $4.5\text{V}$ , $I_L/I_{IS}=KILIS$ , $R_L=\text{Nominal load}$ , No LPF <sup>2)</sup> , Refer to 3.7.12
Sense current settling time after input signal negative slope <sup>1)</sup>	tsis(off)	-	5	10	$\mu\text{s}$	$V_{IN}=4.5\text{V}$ to $0\text{V}$ , No LPF <sup>2)</sup>
Fault signal delay after over current detection1 <sup>1)</sup>	tdsc(fault)1	-	5	15	$\mu\text{s}$	$V_{IN}=0\text{V}$ to $4.5\text{V}$ , $I_L=I_{L1}(SC)$ No LPF <sup>2)</sup>
Fault signal delay after over current detection2 <sup>1)</sup>	tdsc(fault)2	-	30	55	$\mu\text{s}$	$V_{IN}=0\text{V}$ to $4.5\text{V}$ , $I_L=I_{L2}(SC)$ No LPF <sup>2)</sup>
Fault signal delay after absolute thermal shutdown <sup>1)</sup>	tdot(fault)	-	8	18	$\mu\text{s}$	Refer to Figure 12, No LPF <sup>2)</sup>
Fault signal off delay after input negative slope <sup>1)</sup>	tdoff(fault)	-	5	10	$\mu\text{s}$	$V_{IN}=4.5\text{V}$ to $0\text{V}$ , No LPF <sup>2)</sup>

Remark) All voltages refer to ground pin of the device.  
 1) Not subjected production test, guaranteed by design  
 2) Refer to chapter 6 Application example in principle  
 Diagnosis functionality is kept  $V_{CC}=6\text{V}$  min.

### 3.7 Feature Description

#### 3.7.1 Driving Circuit

The high-side output is turned on if the input pin is over  $V_{IH}$ . The high-side output is turned off, if the input pin is open or the input pin is below  $V_{IL}$ . Threshold is designed between  $V_{IH}$  min and  $V_{IL}$  max with hysteresis. IN terminal is pulled down with a constant current source.

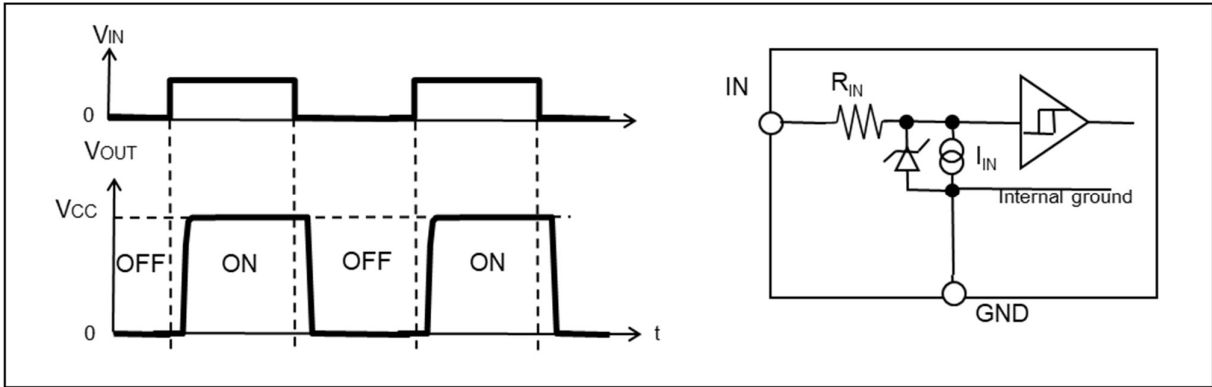


Figure 4 Driving Circuit

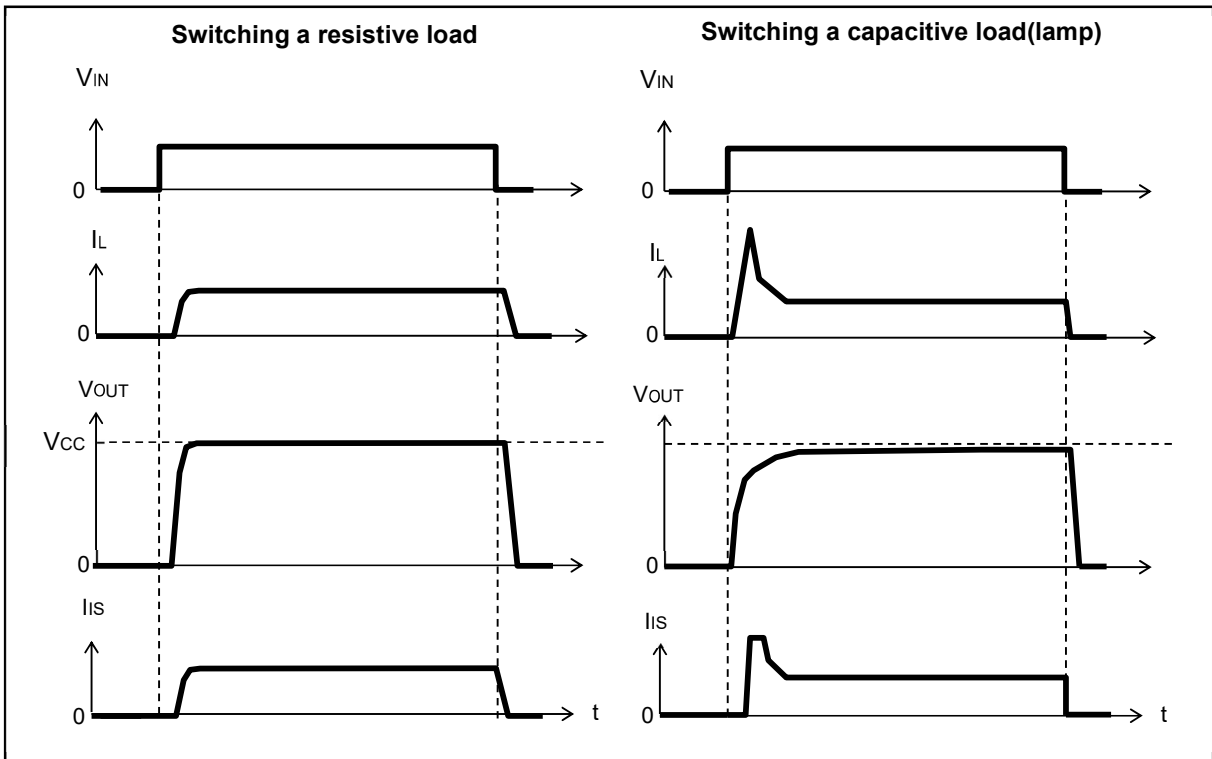


Figure 5-a Switching waveform



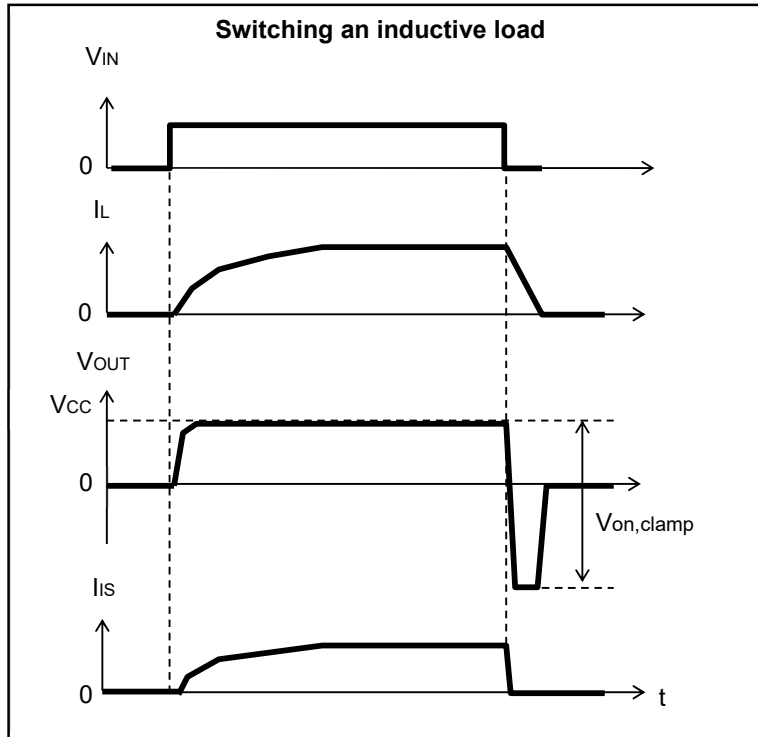


Figure 5-b Switching waveform

When the inductive load is switched off, the voltage of OUT falls below 0V. The internal MOSFET goes into breakdown state and keeps the voltage  $V_{on,clamp}$ .

### 3.7.2 Device behavior at over voltage condition

In case of supply voltage greater than  $V_{load\ dump}$ , logic circuitry is clamped by  $ZD_{AZ}$  (35V min). The current through the logic circuitry is limited by external ground resistor ( $R_{GND}$ ). In addition, N-ch MOSFET switches off to protect the load from over voltage. Test conditions of  $V_{load\ dump}$  are specified in Table 5.

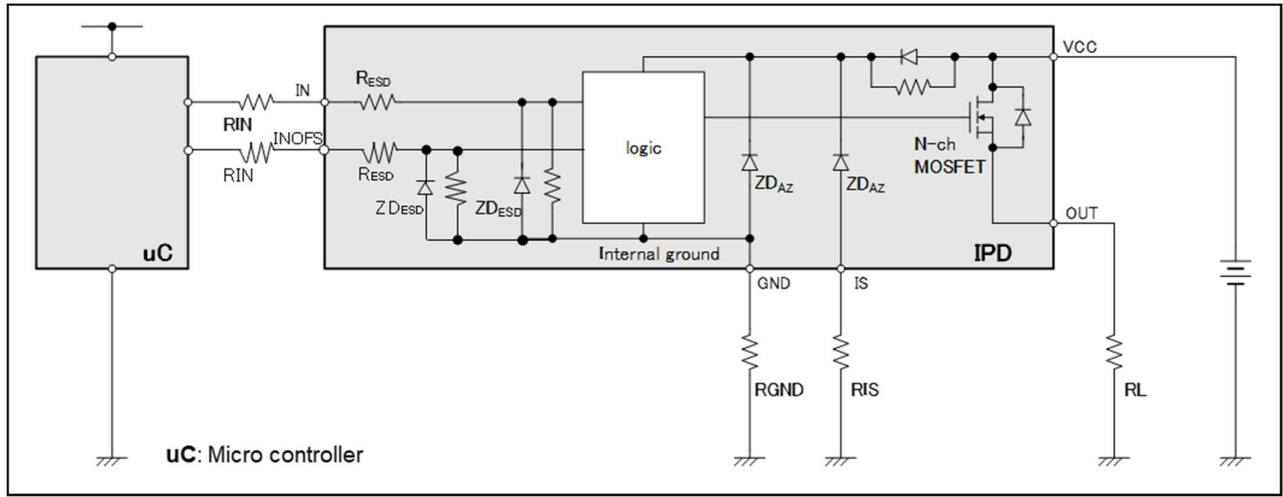


Figure 6 Device behavior at over voltage condition

### 3.7.3 Device behavior at low voltage condition

If the voltage supply ( $V_{CC}$ ) goes down under  $V_{CC(CR)}$ , the device outputs shut down in case of  $V_{on} > V_{onCR(OC)}$ . If voltage supply ( $V_{CC}$ ) increases over  $V_{CC(start)}$ , the device outputs turn back on automatically. The IS output is cleared during off-state.

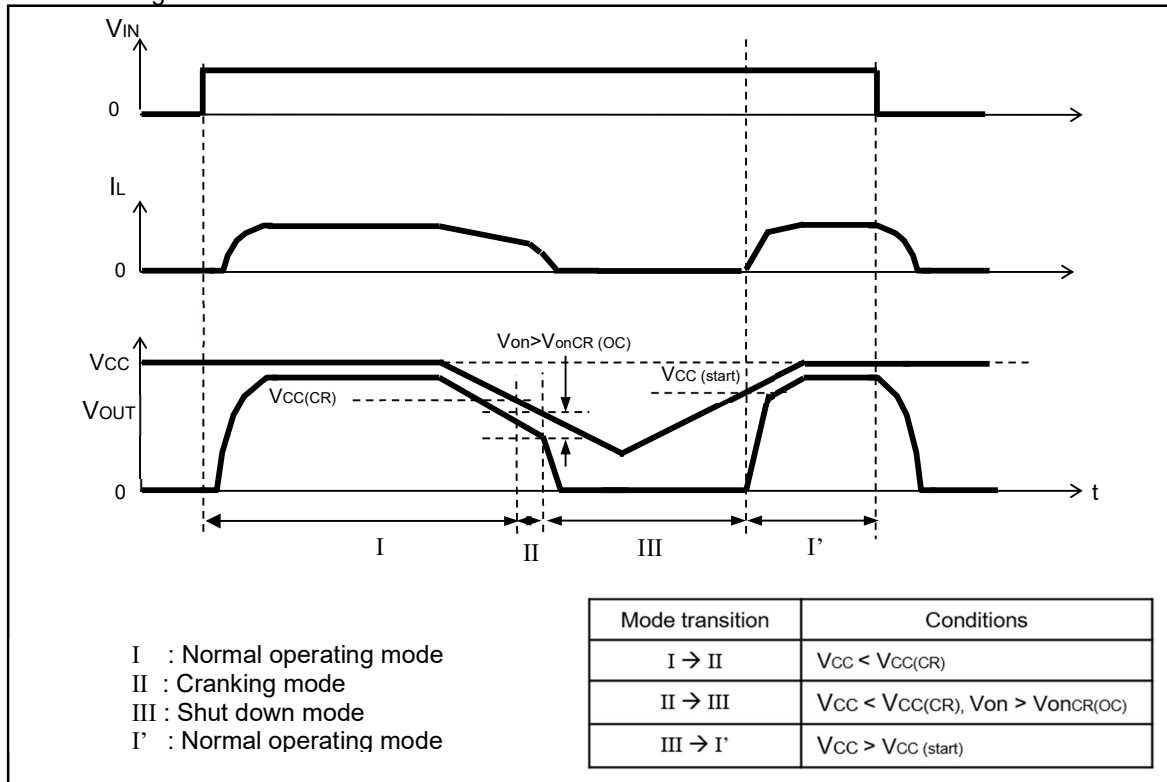


Figure 7 Device behavior at low voltage condition

Table 11 Function and protection availability by mode

○: Enable, ✕: Disable,

Function/Protection	Modes of Figure 7			Note
	I, I'	II	III	
Turn on	○	✕	✕	
Turn off	○	○	✕	
Keep on-state	○	○ (*1)	✕	(*1) Ron is defined as Ron (Cr).
KILIS function	○	✕	✕	In case of $V_{on} < V_{on(kilis)}$
Over current detection current1 : IL1(SC)	○ (*2)	✕	✕	(*2) Disabled when $V_{CC} < 6V(max)$ , Rafer to 3.7.6
Over current detection current2 : IL2(SC)	○ (*3)	✕	✕	(*3) Disabled when $V_{CC} < 6V(max)$ , Rafer to 3.7.6
Von check in over current state: Von (OC), Turn on check delay in over current state: tdoc (OC)	○	✕	✕	$V_{on} > V_{on(OC)}$ after $t_{doc(OC)}$ , Refer to 3.7.6
Von check at cranking in over current state : VonCR (OC)	✕	○	✕	$V_{on} > V_{onCR(OC)}$ at cranking mode, Refer to 3.7.6
Absolute thermal shutdown temperature : aTth	○	○	✕	$T_{ch} > aTth$ , Refer to 3.7.6

### 3.7.4 Definition of on-state resistance at cranking

On-state resistance at Cranking (Figure 7, mode II) is defined  $R_{on}(CR)$  as shown in Figure 8.  $R_{on}(CR)$  is adapted in the condition of  $V_{CC} > 3.2V$  and within 24ms.

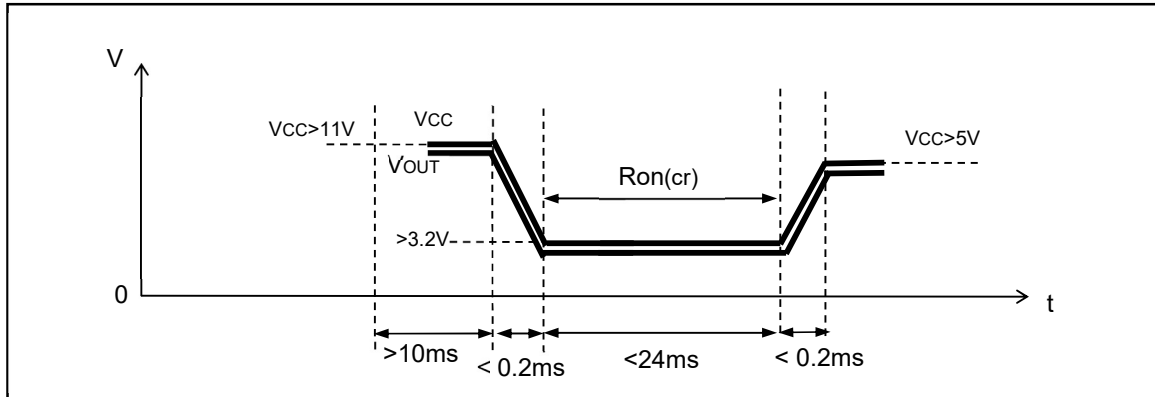


Figure 8 Definition of on-state resistance at cranking

### 3.7.5 Loss of Ground protection

In case of complete loss of the device ground connection with or without load, the device securely changes to off if  $V_{IN}$  was initially greater than  $V_{IH}$  state or keeps the off state if  $V_{IN}$  was initially lower than  $V_{IL}$  state. In case of loss of ground, there is a potential that the current flow from IN terminal to MCU. Therefore, insert a protective resistor between MCU and IN terminal.

### 3.7.6 Over Current protection

The N-ch MOSFET switches off automatically when condition (a), (b), (c), (d) or (e) is detected. In case of (a), (b), (c), (d), the IS pin outputs  $V_{is, fault}$ . The MOSFET maintains off state until the IN pin turns low level ( $V_{IL}$ ).

- (a)  $I_L > I_{L1}(SC)$
- (b)  $I_L > I_{L2}(SC)$
- (c)  $V_{on} > V_{on}(OC)$  after  $t_{doc}(OC)$
- (d)  $T_{ch} > aT_{th}$
- (e)  $V_{on} > V_{onCR}(OC)$  at cranking mode

### 3.7.7 Diagnostic signal

Table 12 Truth table

	Input (IN)	Input (INOFs)	Output (OUT)	Diagnostic output (IS)
Normal Operation	H	H	V <sub>CC</sub>	IIS = IL/KILIS <sup>7)</sup>
		L		IIS = IL/KILIS <sup>8)</sup>
	L	H	L <sup>2)</sup>	L <sup>3)</sup>
		L		
Shutdown by over current detection <sup>1)</sup>	H	H	L <sup>2)</sup>	Vis,fault <sup>4)</sup>
		L		
	L	H	L <sup>2)</sup>	L <sup>3)</sup>
		L		
Shutdown by over absolute channel temperature detection	H	H	L <sup>2)</sup>	Vis,fault <sup>5)</sup>
		L		
	L	H	L <sup>2)</sup>	L <sup>3)</sup>
		L		
Short circuit to V <sub>CC</sub>	H	H	V <sub>CC</sub>	<IIS
		L		
	L	H	V <sub>OUT</sub> <sup>6)</sup>	L <sup>3)</sup>
		L		

- 1) Over Current detection is included IL1(SC), IL2(SC), Von (OC)after t<sub>DOC</sub> (OC) or VonCR (OC).
- 2) In case of OUT terminal is connected to GND via load.
- 3) In case of IS terminal is connected to GND via resistor.
- 4) IS terminal keeps Vis,fault as long as input signal activate after the over current detection.
- 5) IS terminal keeps Vis,fault as long as input signal activate after over absolute channel temperature detection.
- 6) V<sub>OUT</sub> depends on the ratio of V<sub>CC</sub> -OUT-GND resistive component.
- 7) The current sense ratio (KILIS) is the value when the improved accuracy function is used.
- 8) The current sense ratio (KILIS) is the value when the improved accuracy function is not used.

### 3.7.8 Current sense output

The device outputs analog feedback current proportional to output current from IS pin. In the case of much higher current than nominal load current, current sense output is saturated at Vis,fault.

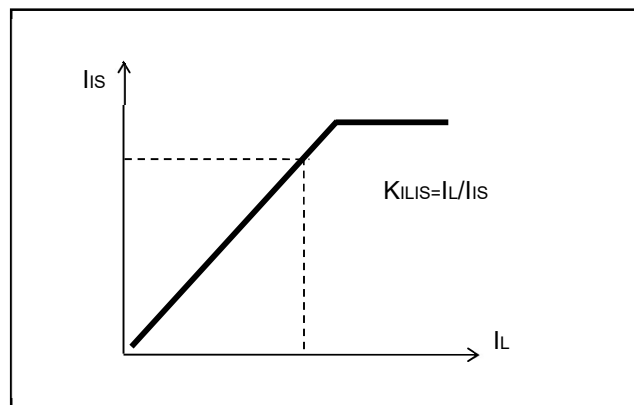


Figure 9 Current sense output

### 3.7.9 Timings

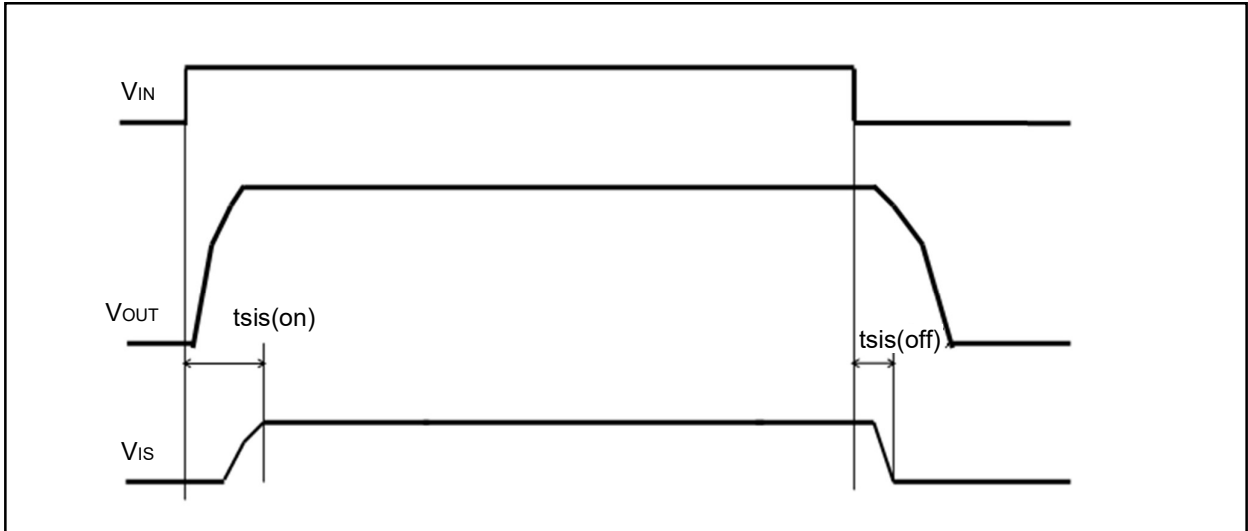


Figure 10 Sense voltage setting time

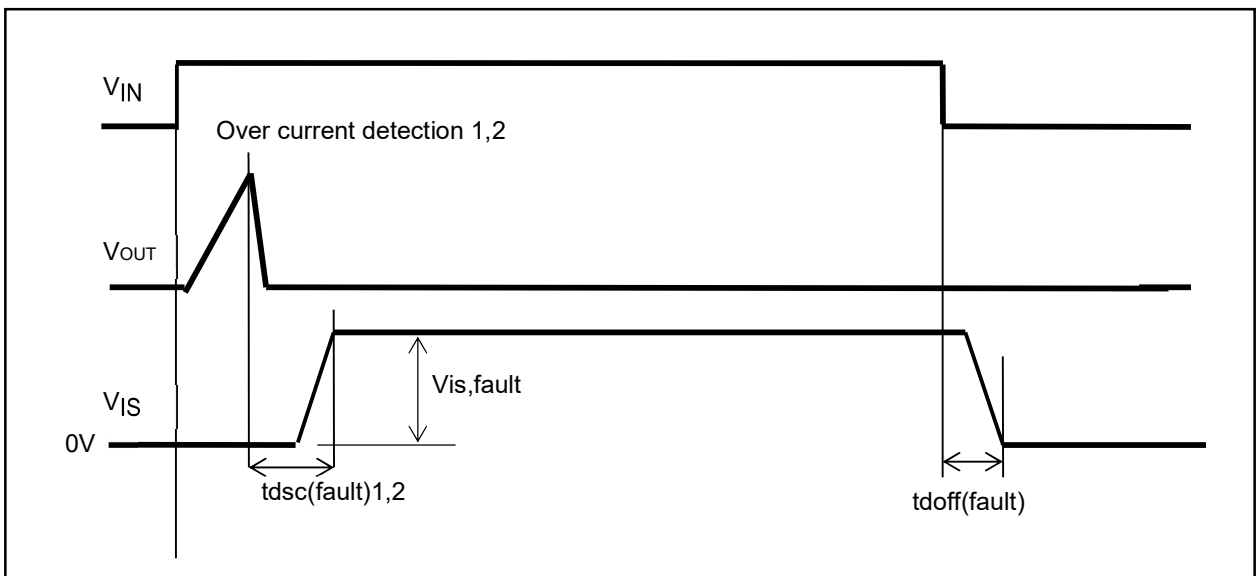


Figure 11 Fault signal delay time at over current detection and input negative slope

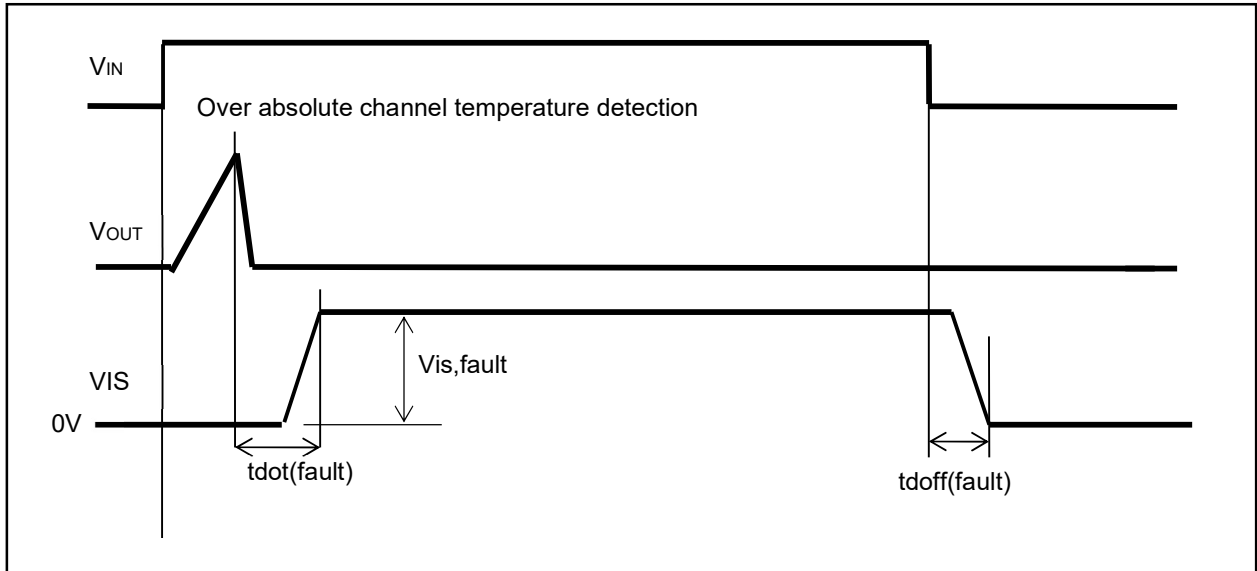


Figure 12 Fault signal delay time at over absolute channel temperature detection and input negative slope

3.7.10 Measurement condition

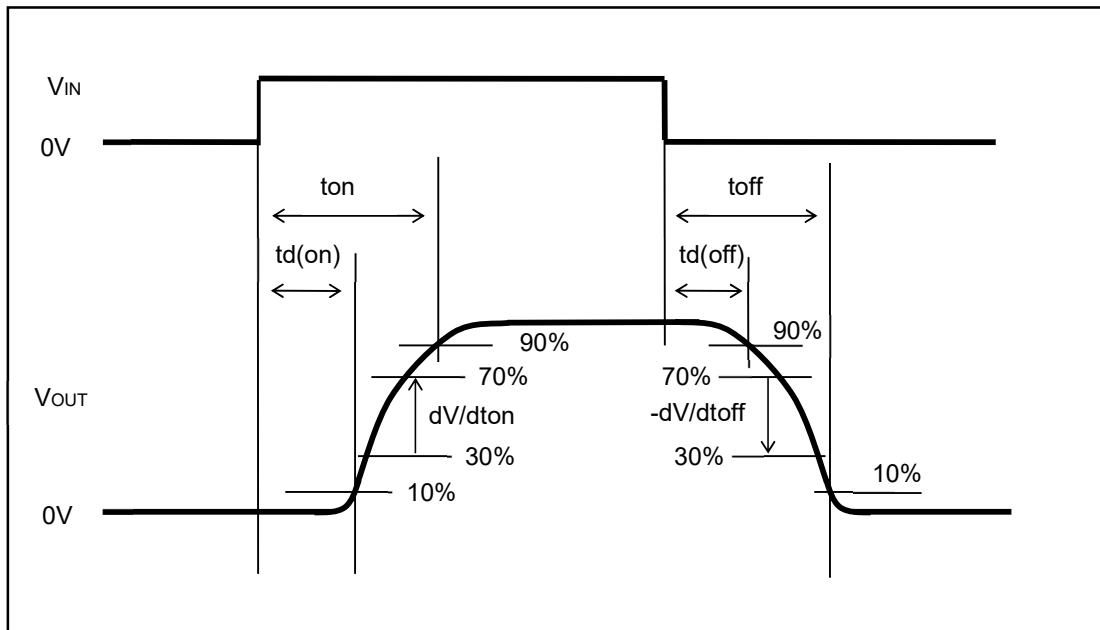


Figure 13 Switching waveform of OUT terminal

### 3.7.11 Measurement condition for Turn on check in over current state

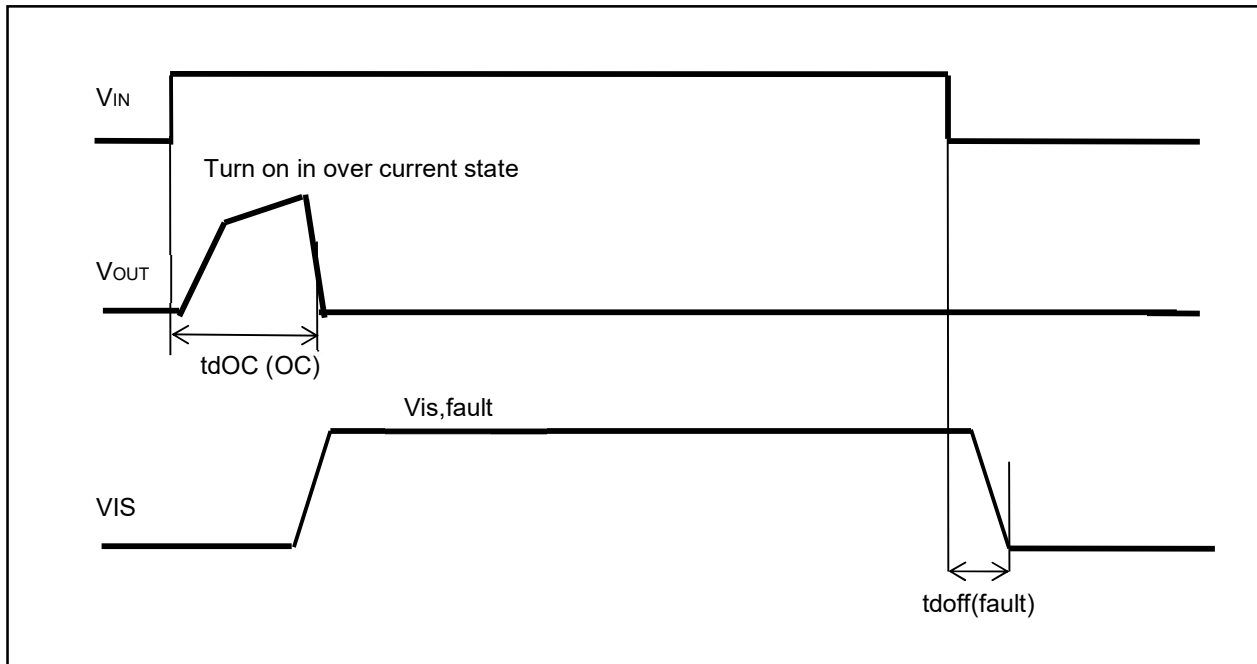


Figure 14 Measurement condition for Turn on check in over current state

### 3.7.12 Nominal load and nominal current

Table 13 Nominal load and nominal current

Parameter	Values	Condition
Nominal load	0.45 $\Omega$	Tch $\leq$ 150°C (Vcc=13.5V)
Nominal current	30 A	Tch = 25°C
Nominal current 2	19.6A	Ta=85°C, Tch $\leq$ 150°C



### 3.7.13 Driving Capability

Driving Capability is specified as load impedance. Over current detection characteristics is designed above Driving Capability characteristics. If the estimated load impedance which comes from peak inrush current is lower than Driving Capability characteristics, then the device does not detect inrush current as over current and does not shutdown the output. If estimated load impedance which comes from peak inrush current is higher than Driving Capability characteristics and reach the IL1(SC) or IL2(SC) thresholds level, then the device detects inrush current as over current and shutdown the output.

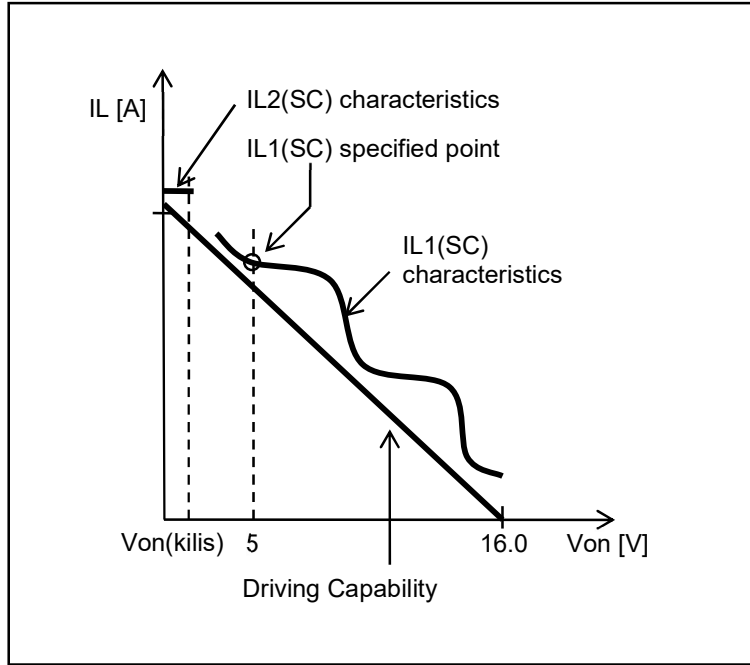


Figure 15 Driving capability

### 3.7.14 Cross current protection in case of H-bridge high side usage

In case of using High side driver in H-bridge circuit, the High side driver protects itself and the low side driver from high power dissipation by cross current when low side driver switches on.

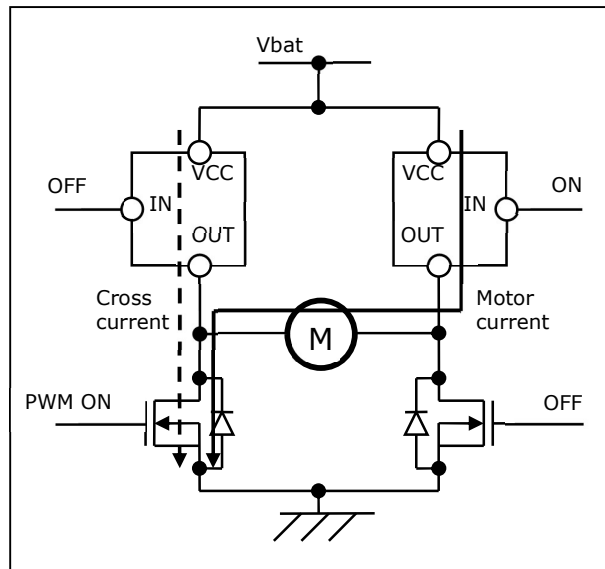


Figure 16 Cross current protection in case of H-bridge high side usage

### 3.7.15 Reverse Battery Protection by turning on the output

In case a reverse battery is applied to the device, the N-ch MOSFET will turn on only if reverse current flow into the GND pin. The reverse current through the N-ch MOSFET must be limited by the connected load. IGND (rev) is limited internally approx. 2mA even without external RGND. Reverse current flow from IN, INOFS and IS should be limited by external components such as recommendation value in Pin function, refer to 3.2 Pin configuration.

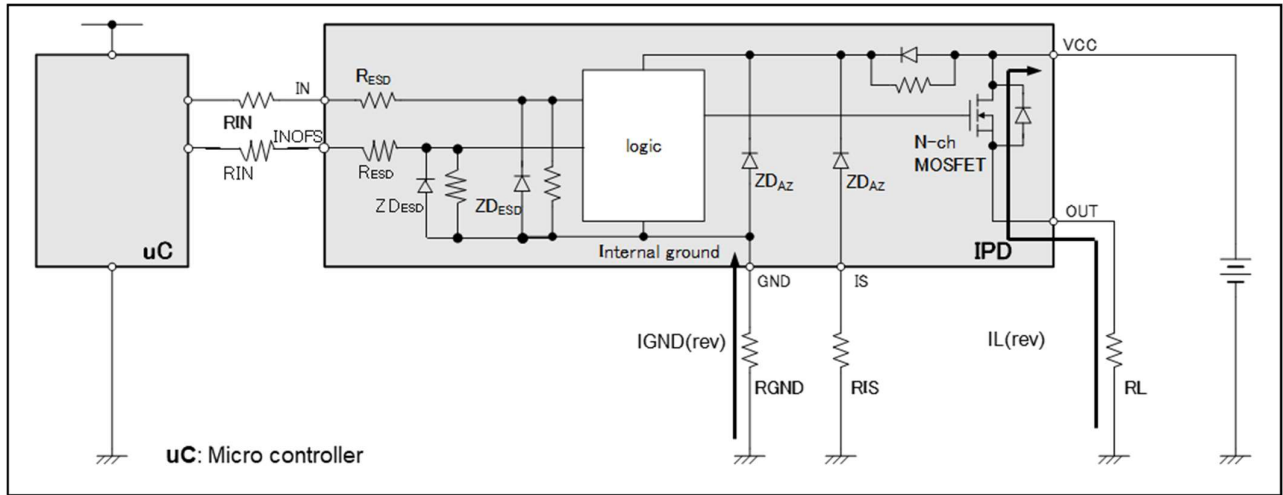


Figure 17 Reverse Battery Protection by turning on the output

3.8 Package drawing (TO252-7)

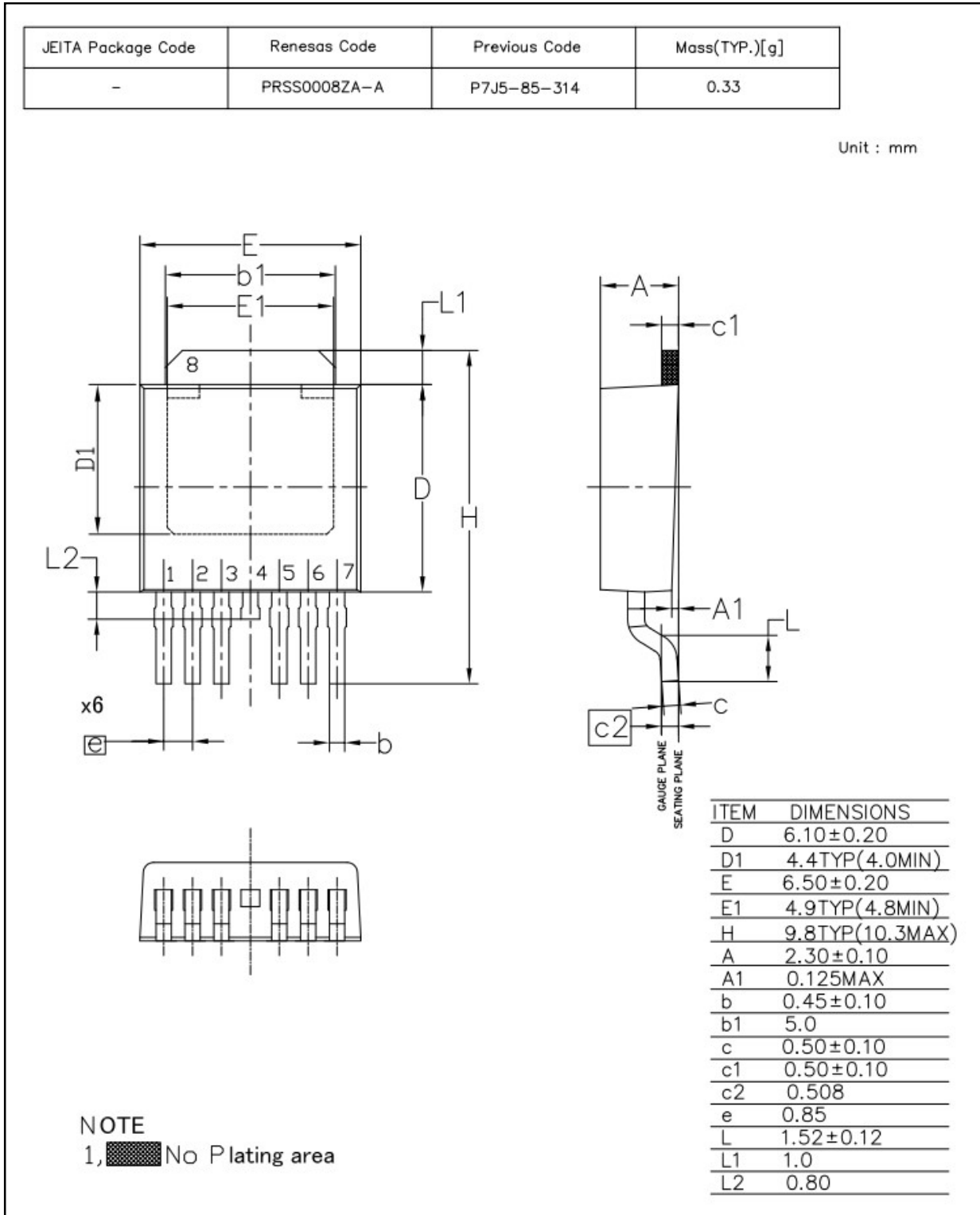


Figure 18 TO252-7 Package Outline

### 3.9 Taping information

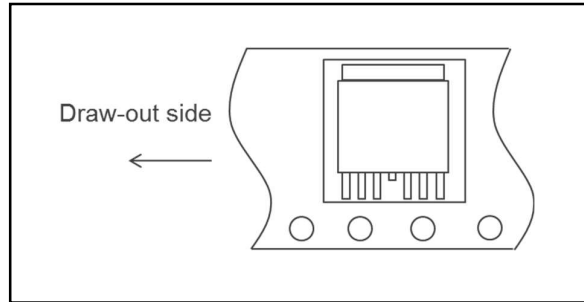


Figure 19 Taping information

### 3.10 Marking information

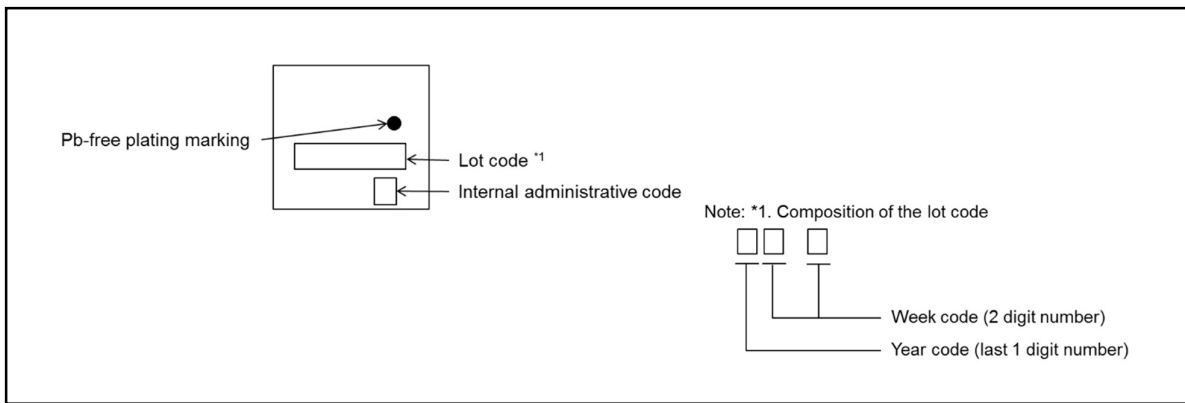


Figure 20 Marking information

### 4 Typical characteristics

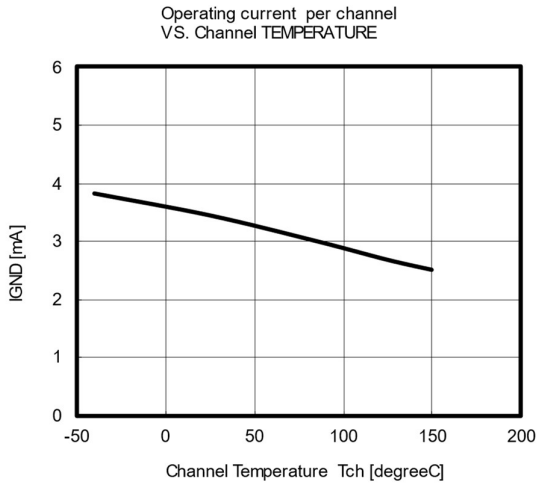


Figure 21. IGND

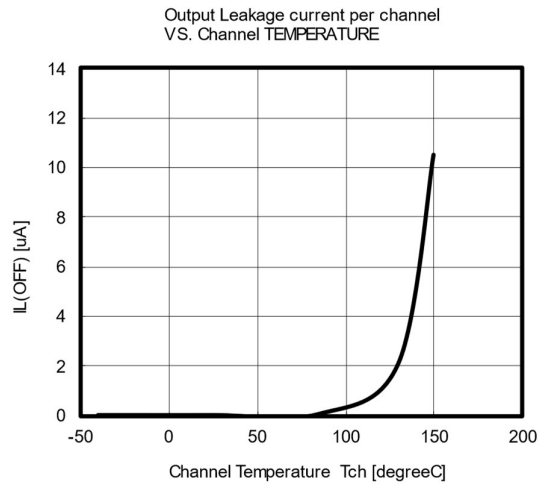


Figure 22. IL(OFF)

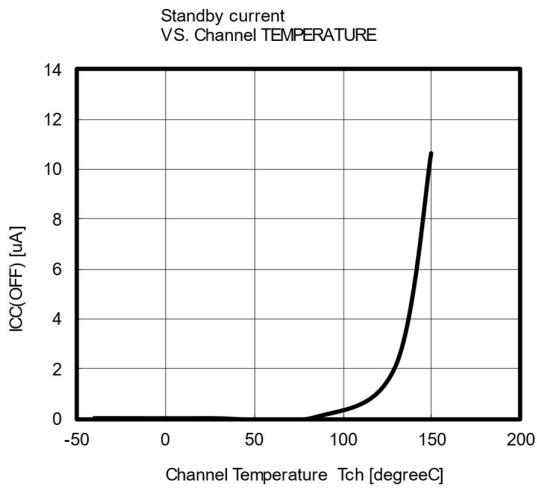


Figure 23. ICC(OFF)

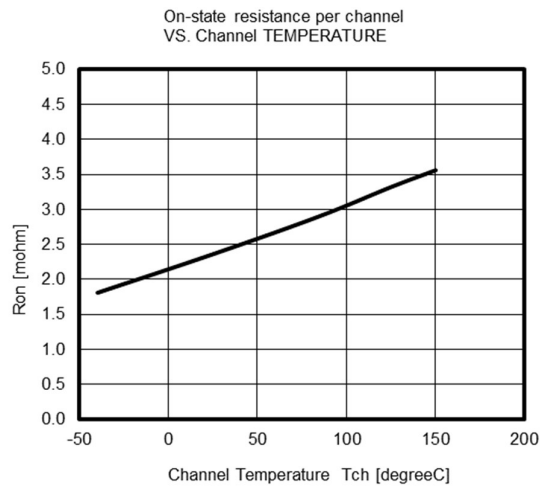


Figure 24. Ron

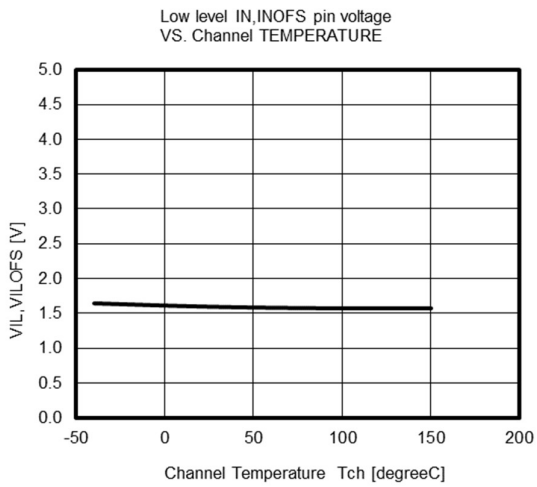


Figure 25. VIL, VILOFS

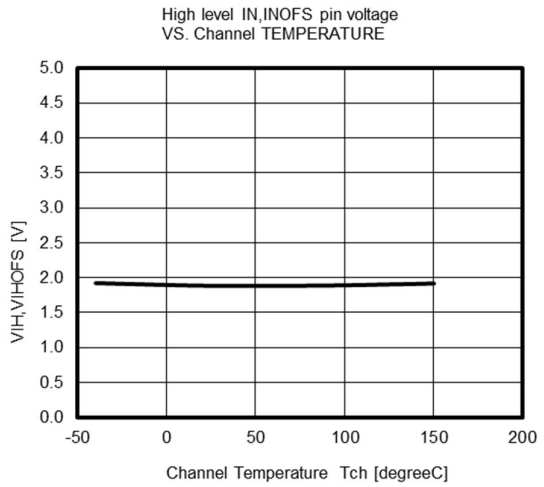


Figure 26. VIH, VIHOFs

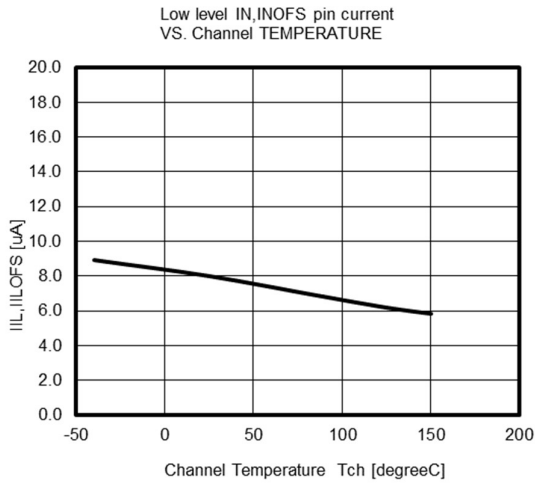


Figure 27. IIL, ILOFS

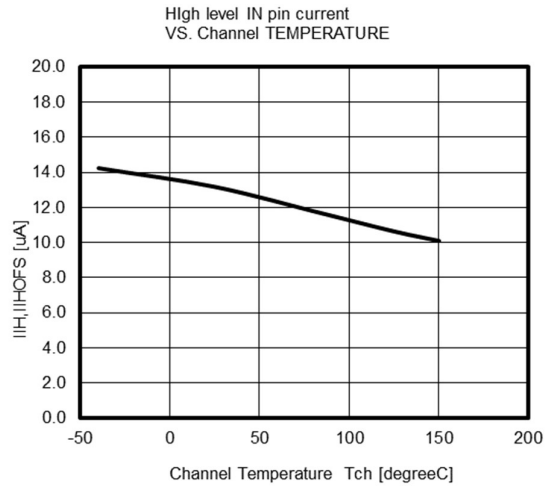


Figure 28. IIH, IHOFS

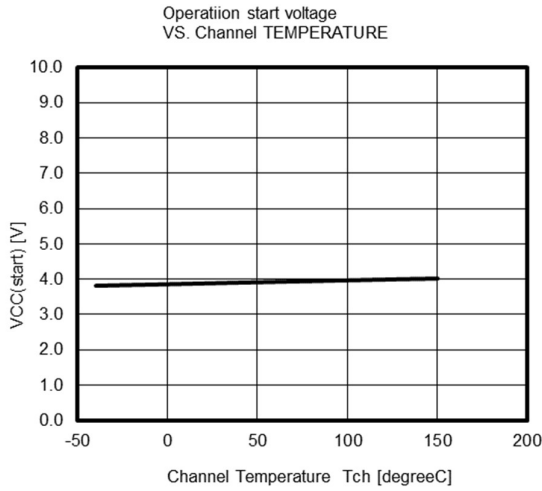


Figure 29. VCC (start)

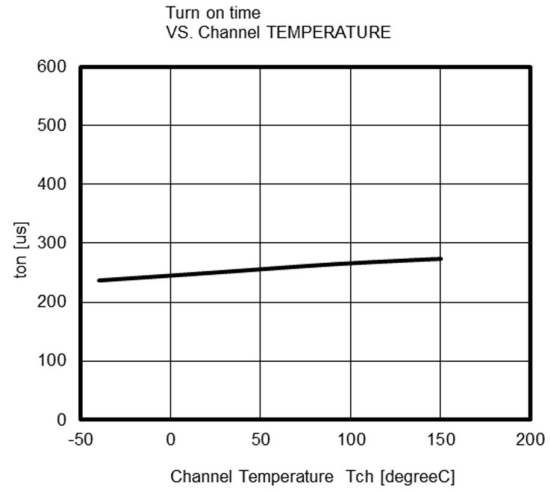


Figure 30. ton

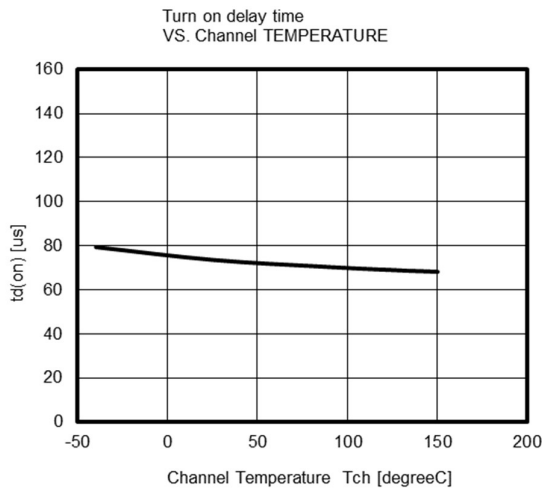


Figure 31. td(on)

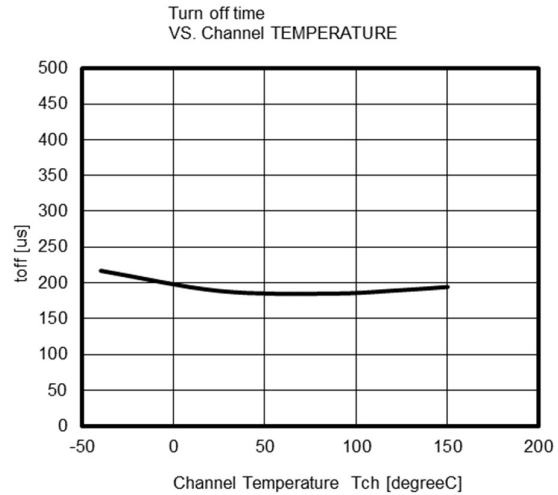


Figure 32. toff

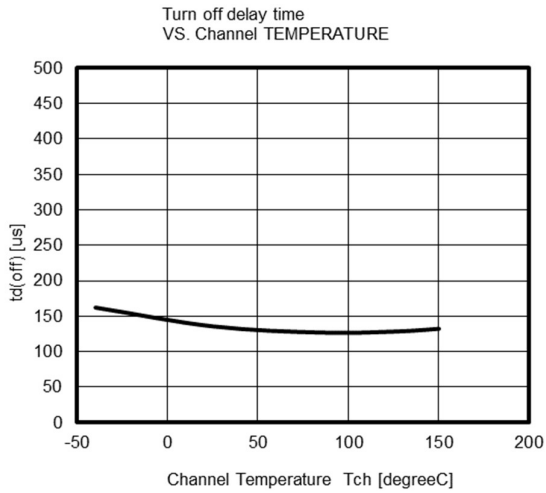


Figure 33. td(off)

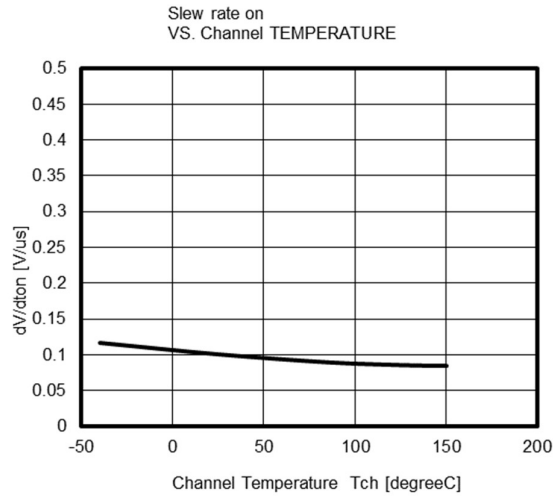


Figure 34. dV/dton

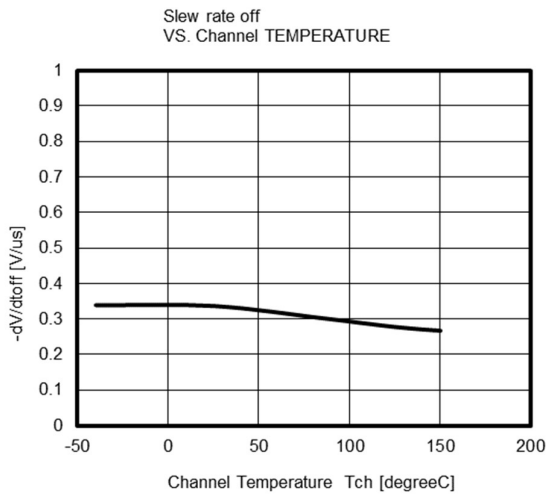


Figure 35. -dV/dtoff

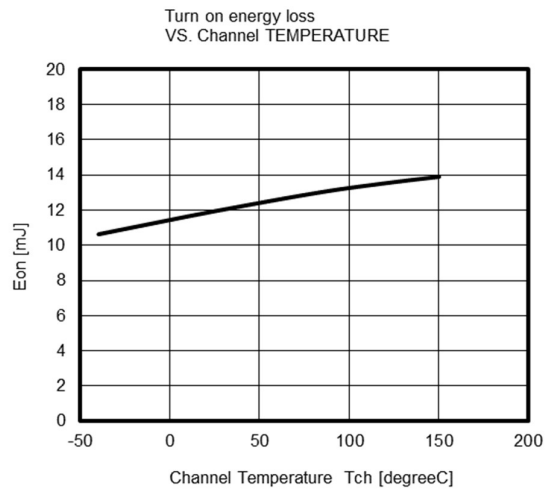


Figure 36. Eon

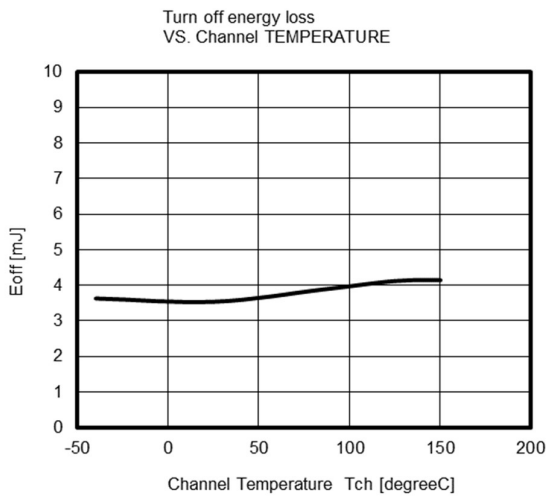


Figure 37. Eoff

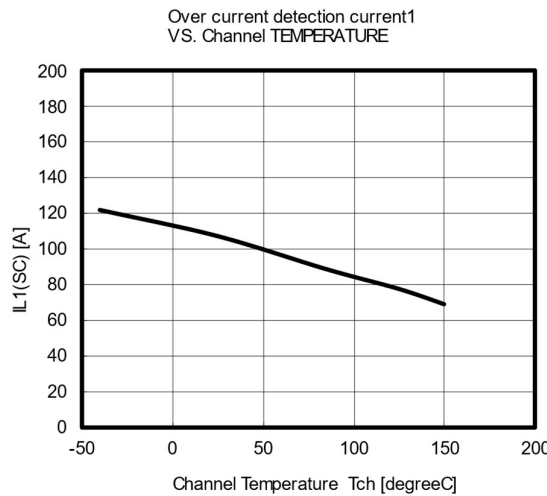


Figure 38. IL1(SC)

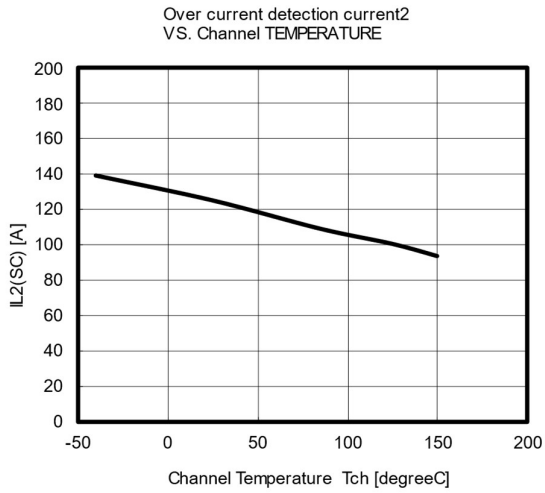


Figure 39. IL2(SC)

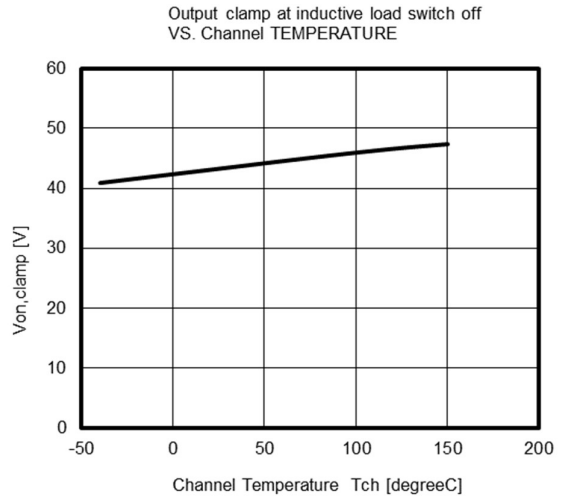


Figure 40. Von,clamp

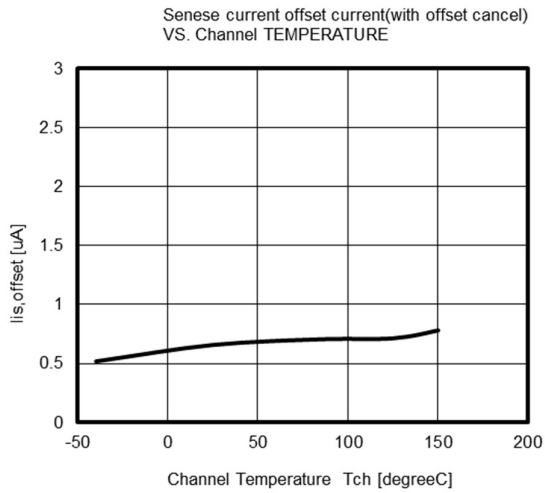


Figure 41. Iis,offset  
(use improved accuracy func)

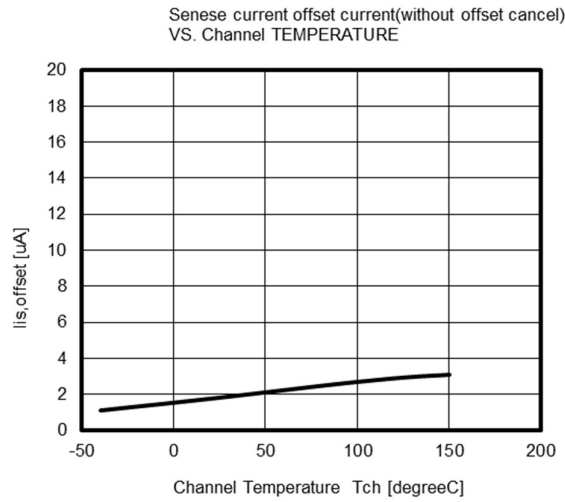


Figure 42. Iis,offset  
(no use improved accuracy func)

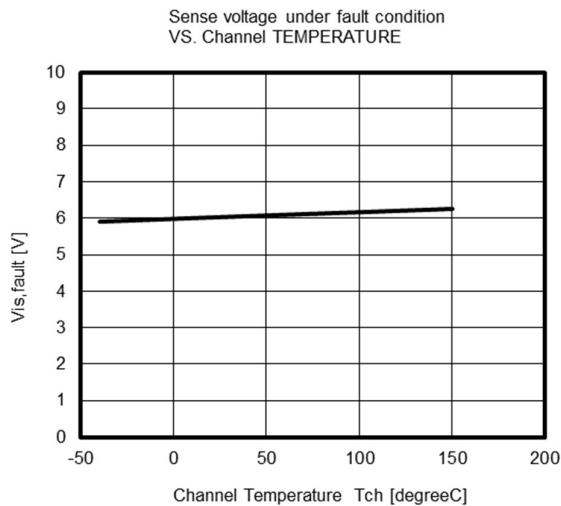


Figure 43. Vis,fault



## 5 Thermal characteristics

### 5.1 Thermal characteristics board condition(2s2p)

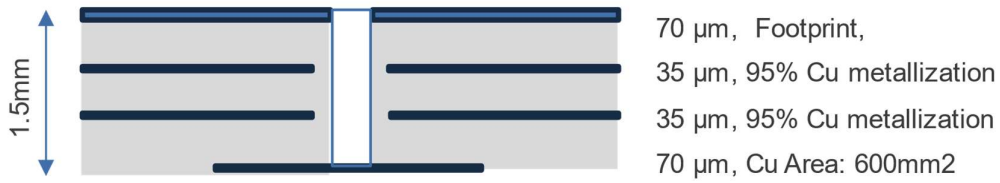


Figure 44 Cross section 2s2p board

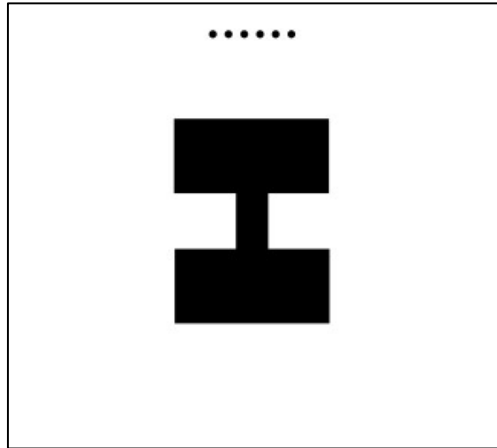


Figure 45: Botom layer pattern

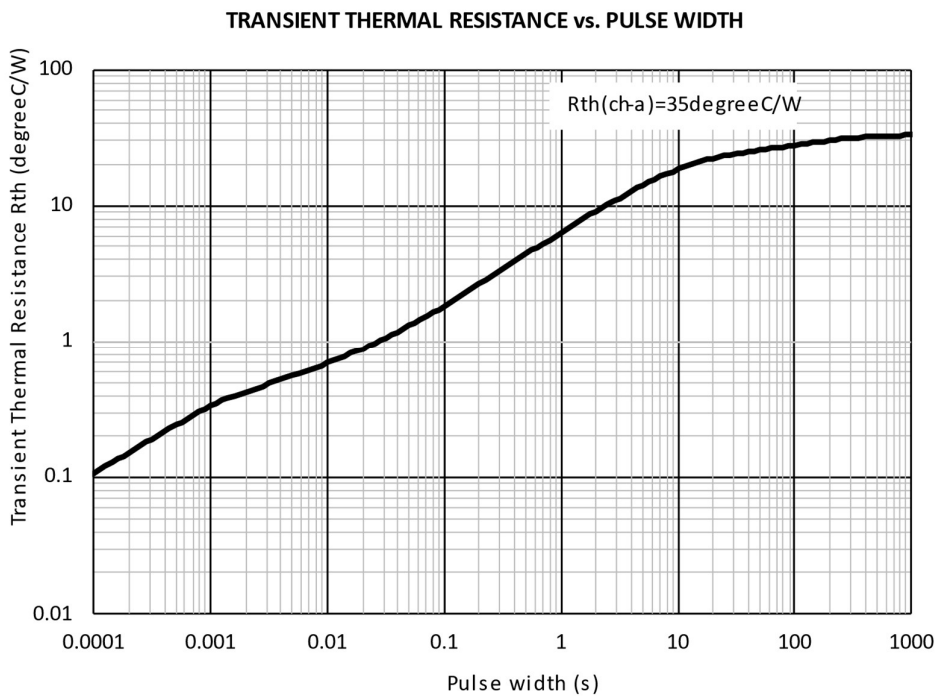


Figure 46 Thermal characteristics(2s2p)

## 5.2 2<sup>nd</sup> layer connected condition metallization dependency

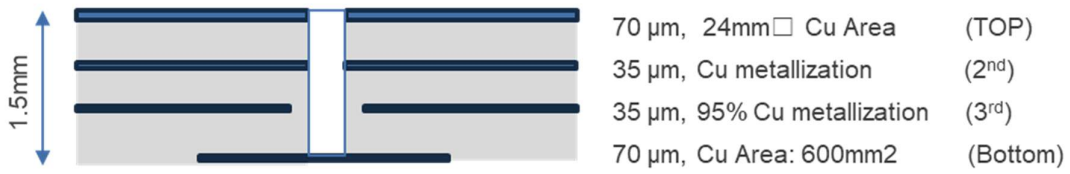


Figure 47 Cross section of 2<sup>nd</sup> layer metallization dependency

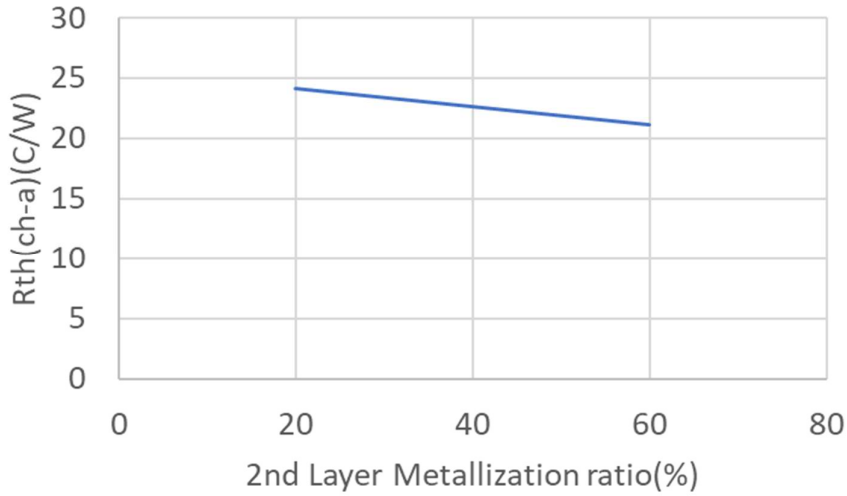


Figure 48 2<sup>nd</sup> layer metallization dependency

## 6 Application example in principle

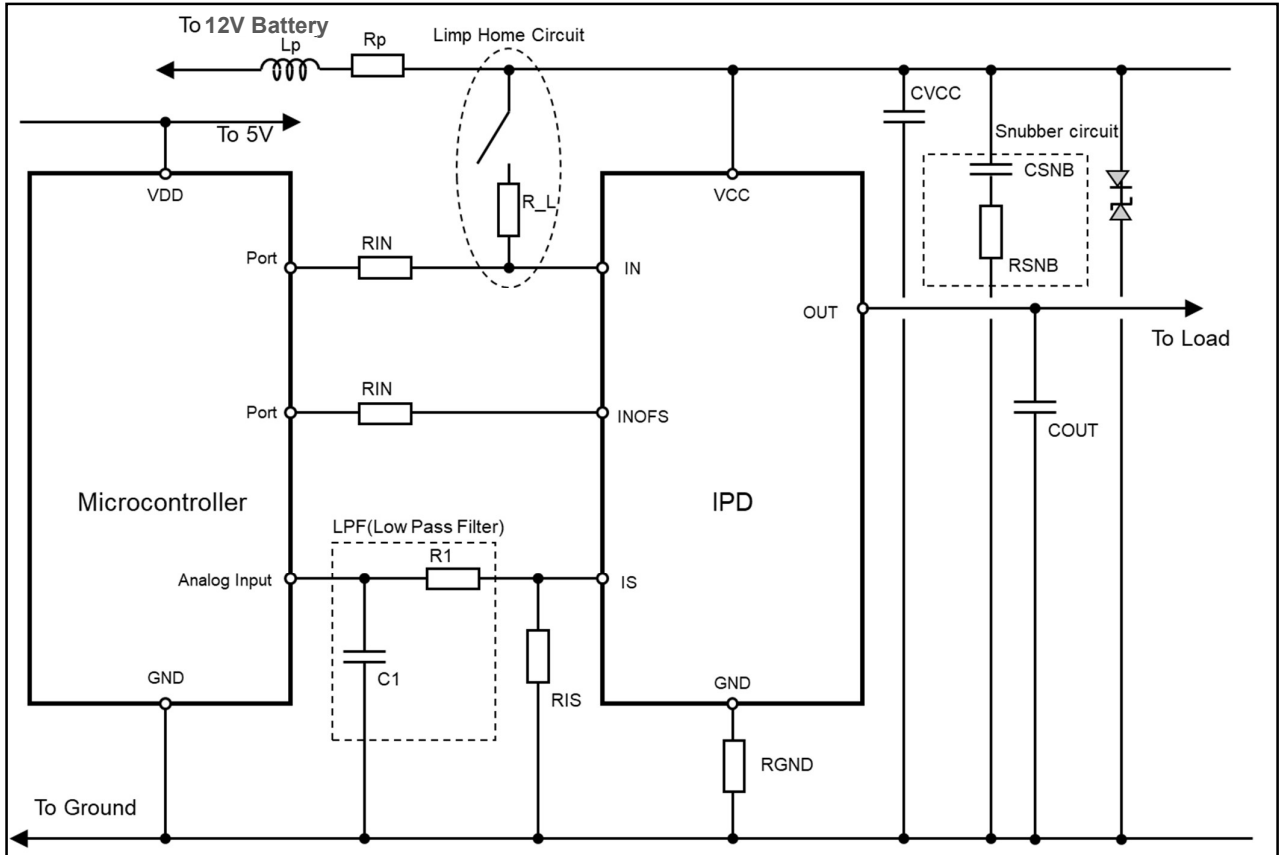


Figure 45 Application example in principle

RIN values are in range of 2k to 50kΩ depending on microcontroller while R<sub>L</sub> value is typically 4kΩ.

RIS values are in range of 1k to 6kΩ.

Time constant parameter of LPF for KILIS improved accuracy function T(kilis) is represented as follows.

$$T(\text{kilis}) = (R1 + RIS) \times C1$$

Time constant parameter of LPF for Vis, fault function T(fault) is represented as follows.

$$T(\text{fault}) = R1 \times C1$$

R1 values are in range of over 2kΩ.

100us or more is recommended as T(kilis), considering T(fault) parameter.

If necessary to raise HBM tolerated dose, adding a resistor between OUT terminal and Ground is effective, the resistor's value is typically 100kΩ.

Additional snubber circuit is recommended if necessary, to prevent VCC drop less than minimum operating voltage threshold, by parasitic inductance (Lp) and parasitic resistance (Rp) resonance.

Recommended values are as follows:

CVCC : 22nF

RSNB<sup>1)</sup> :  $RSNB = \sqrt{(Lp / CVCC) \cdot 0.125W}$  (ex. Lp:3.94uH -> RSNB=10Ω)

CSNB<sup>2)</sup> : 1.0uF (ex. GCM21BR71H105MA03(Murata Manufacturing Co.Ltd.)).

- 1) High pulse withstands resistor.
- 2) High pulse withstands capacitor.

RGND is recommended if necessary for unexpected external surge protection.

47 ohm is recommended as RGND.

## 7 Revision History

Rev.	Date	Description	
		Page	Summary
1.0	May.13.2024		Initial release

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