

RBA300N10EHPF-5UA02

REXFET-1 N-Channel Power [MOSFET](#)

100V - 340A - 1.5mΩ

R07DS1574EJ0100

Rev.1.00

Nov.08.2024

Description

Renesas TOLG technology features ultra compact, gullwing leads designs for compatible with the footprint to the TOLL, enhanced thermal performance, management, and higher thermal cycling on board performance. Renesas new split gate technology provide suitable for use in low RDS(on) and switching capability for high power & high-frequency application.

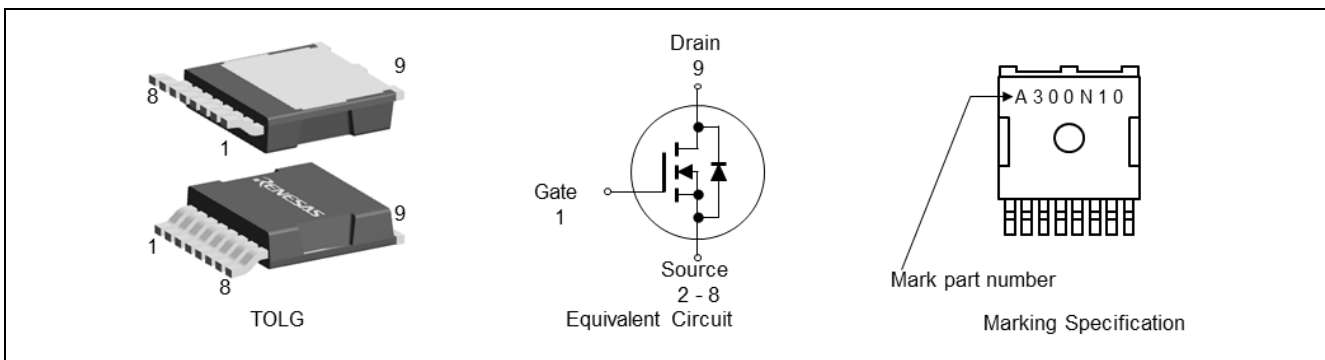
Features

- Standard level gate drive voltage : $V_{GS(th)} = 2.0\sim 4.0V$
- Super Low on-state resistance : $R_{DS(on)} = 1.5m\Omega$ Max.
- Low input capacitance
- Low thermal resistance
- AEC-Q101 qualified
- PPAP capable
- Pb-free lead plating : RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

- Automotive : Small Traction (2-wheel, 3-wheel vehicle), 48V load, OBC, Charging station, LDC, etc.
- Industrial / Infrastructure : Energy infrastructure, Micro inverter, Power-tool, DC-DC, etc.

Outline



Absolute Maximum Ratings

($T_j=25^\circ C$ unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$ <small>Notes1,2,5</small>	± 340	A
Drain Current (Chip limitation)		± 380	A
Drain Current (pulse)	$I_{D(pulse)}$ <small>Notes1,3,5</small>	± 1360	A
Power Dissipation	P_D <small>Notes1,5</small>	468	W
Junction Temperature	T_j	175	$^\circ C$
Storage Temperature	T_{stg}	-55 to 175	$^\circ C$
Single Avalanche Current	I_{AS} <small>Notes4</small>	64	A
Single Avalanche Energy	E_{AS} <small>Notes4</small>	409	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j-c)}$ ^{Notes4}	0.32	°C/W

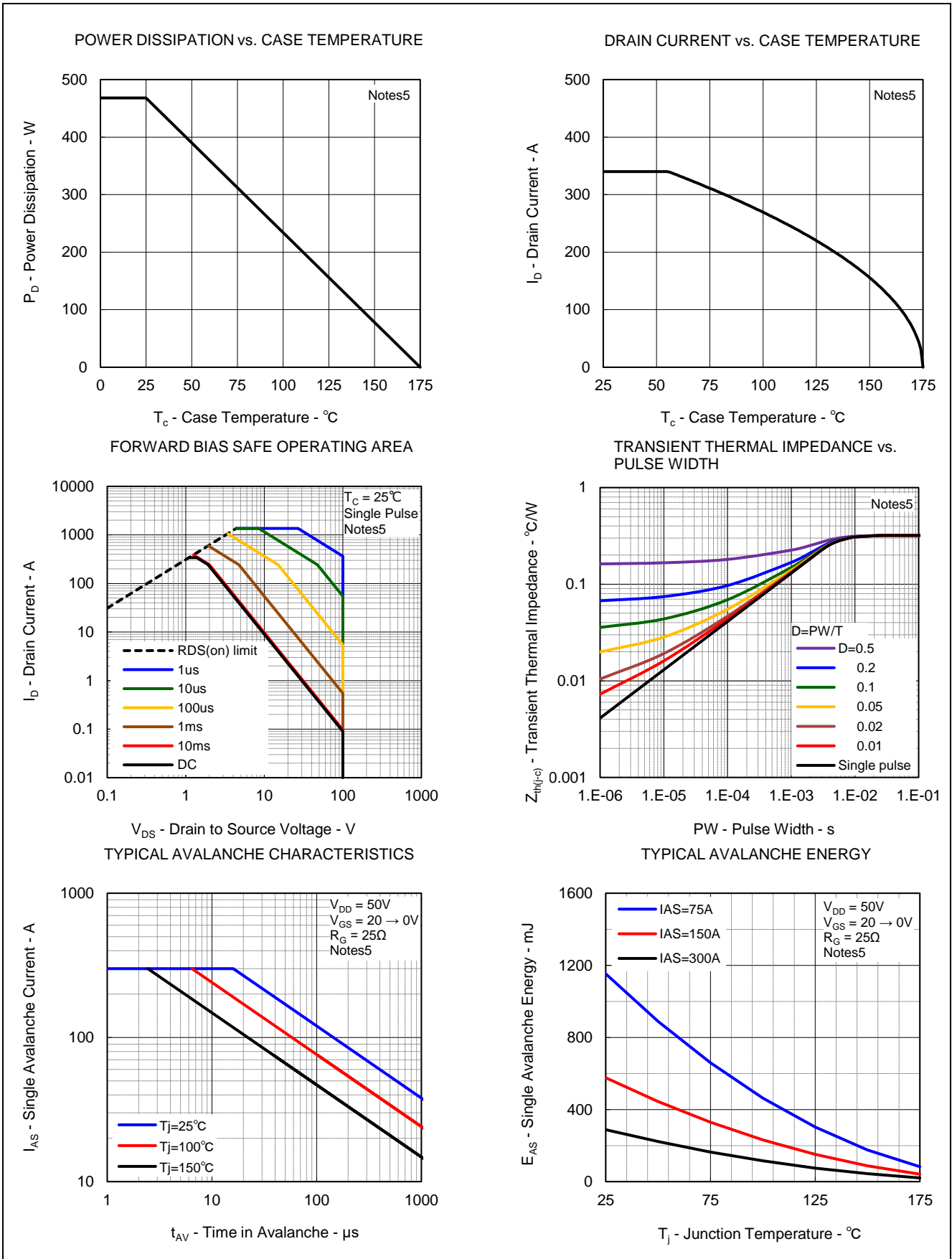
Electrical Characteristics

(T_j=25°C unless otherwise notice.)

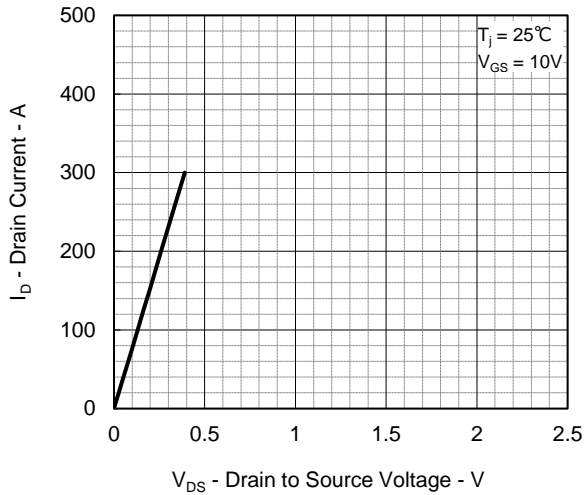
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	V _{DS} = 100 V, V _{GS} = 0 V
Gate Leakage Current	I_{GSS}	—	—	±500	nA	V _{GS} = ± 20 V, V _{DS} = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	—	4.0	V	V _{DS} = V _{GS} , I _D = 250 μA
Drain to Source On-state Resistance	$R_{DS(on)}$	—	1.3	1.5	mΩ	V _{GS} = 10 V, I _D = 100 A
Input Capacitance	C_{iss}	—	13000	—	pF	V _{DS} = 50 V V _{GS} = 0 V f = 100 kHz
Output Capacitance	C_{oss}	—	3300	—	pF	
Reverse Transfer Capacitance	C_{rss}	—	80	—	pF	
Gate resistance	R_g	—	1.8	—	Ω	
Turn-on Delay Time	$t_{d(on)}$	—	75	—	ns	V _{DD} = 50 V, I _D = 100 A V _{GS} = 10 V R _G = 5 Ω
Rise Time	t_r	—	60	—	ns	
Turn-off Delay Time	$t_{d(off)}$	—	130	—	ns	
Fall Time	t_f	—	55	—	ns	
Total Gate Charge	Q_g	—	170	—	nC	V _{DD} = 50 V V _{GS} = 10 V I _D = 100 A
Gate to Source Charge	Q_{gs}	—	75	—	nC	
Gate to Drain Charge	Q_{gd}	—	30	—	nC	
Body Diode Forward Voltage	$V_{F(S-D)}$	—	0.9	1.5	V	I _F = 100 A, V _{GS} = 0 V
Reverse Recovery Time	t_{rr}	—	110	—	ns	I _F = 100 A, V _{GS} = 0 V
Reverse Recovery Charge	Q_{rr}	—	300	—	nC	di/dt = 100 A/μs

- Notes
1. T_c = 25°C
 2. Value is limited by overall system design including PCB.
 3. PW ≤ 10 μs
 4. L = 100μH, V_{DD} = 50V, V_{GS} = 20 → 0V, R_G = 25 Ω
 5. Defined by design. Not subject to production test.

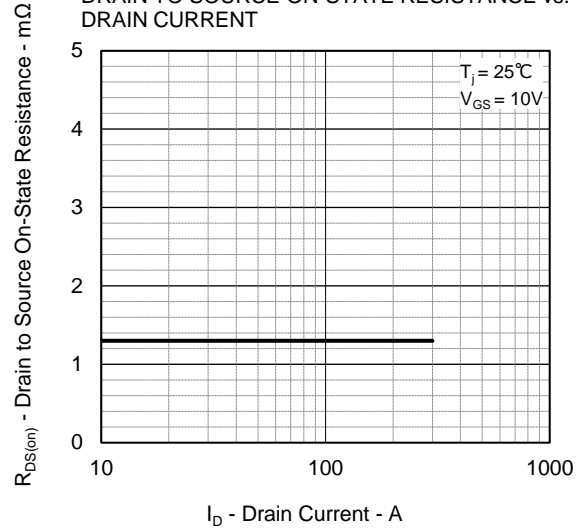
Typical Characteristics



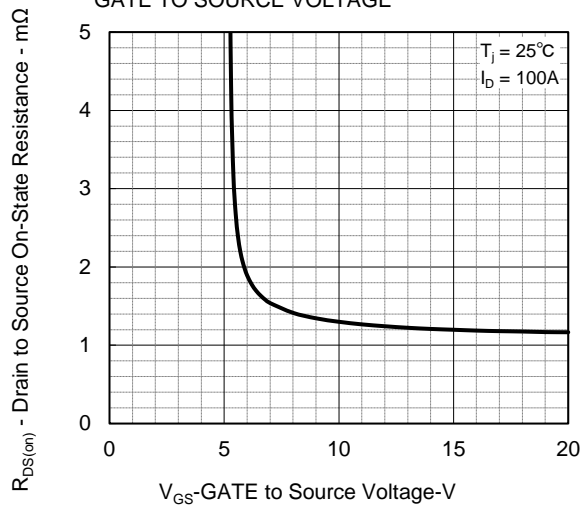
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



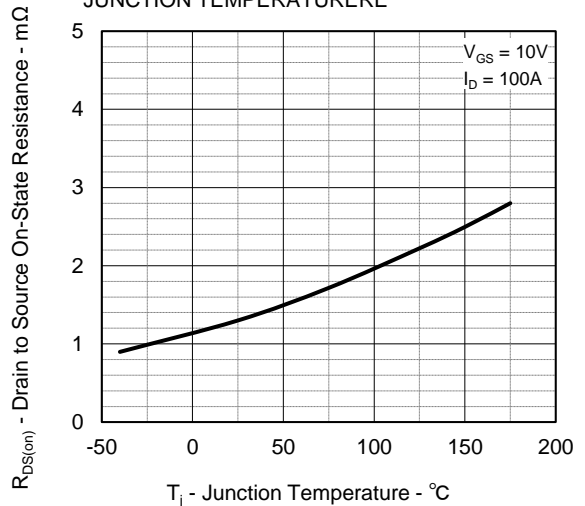
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



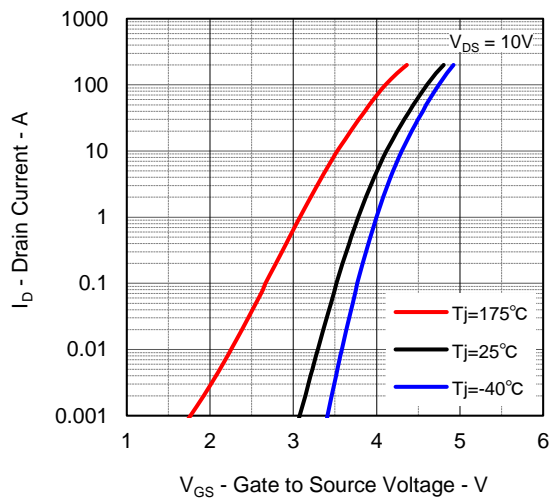
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



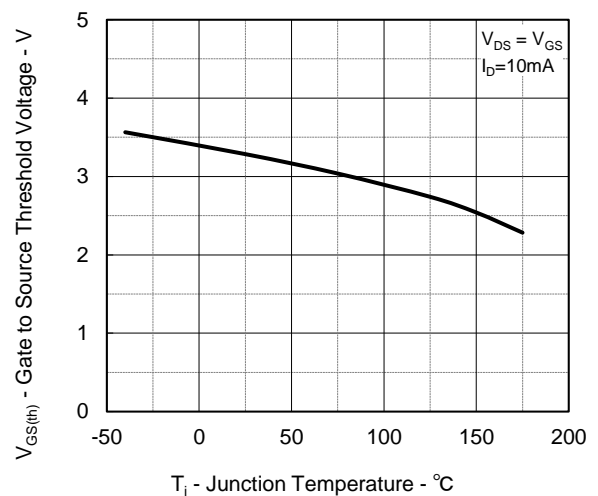
DRAIN TO SOURCE ON-STATE RESISTANCE vs. JUNCTION TEMPERATURE



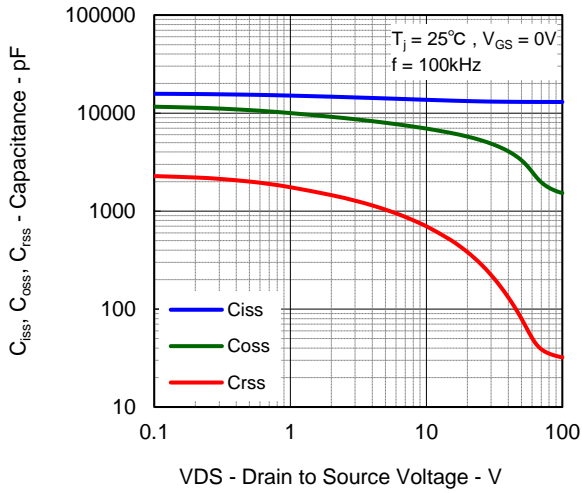
FORWARD TRANSFER CHARACTERISTICS



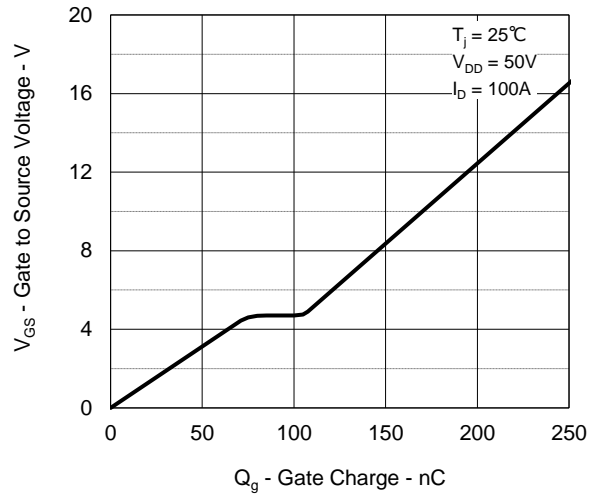
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE



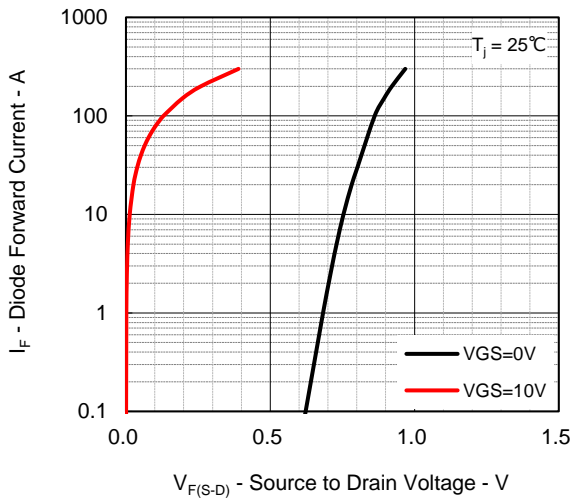
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



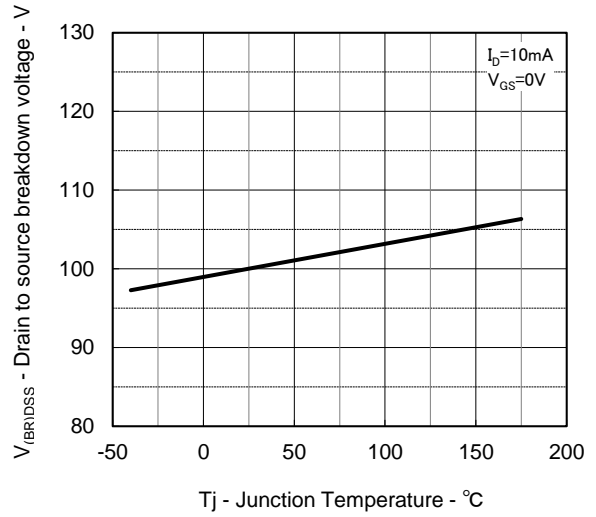
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



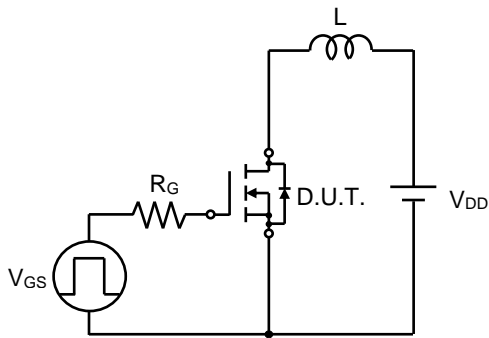
DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE



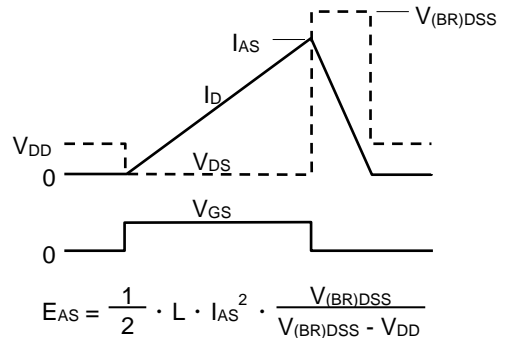
Test Circuit

Avalanche

Test Circuit

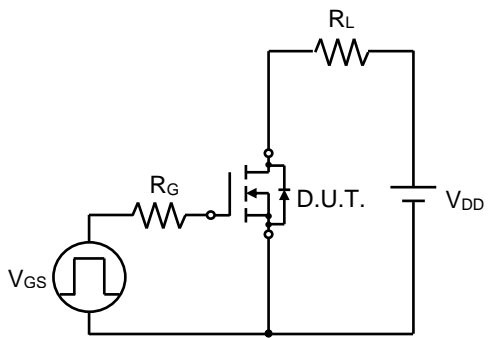


Waveform

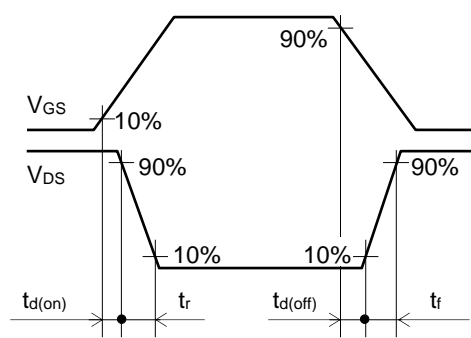


Switching Time

Test Circuit

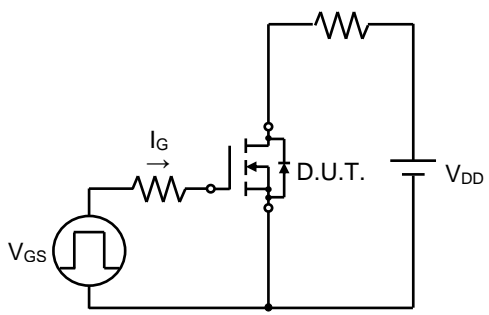


Waveform

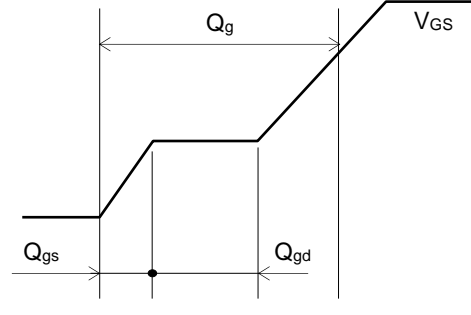


Gate Charge

Test Circuit

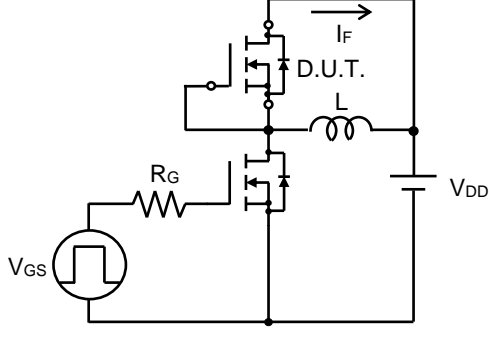


Waveform

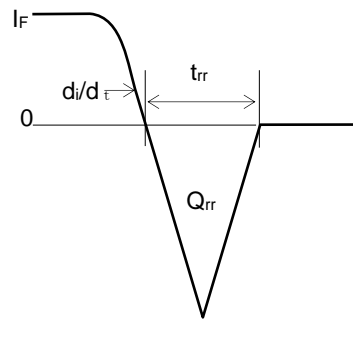


Reverse Recovery

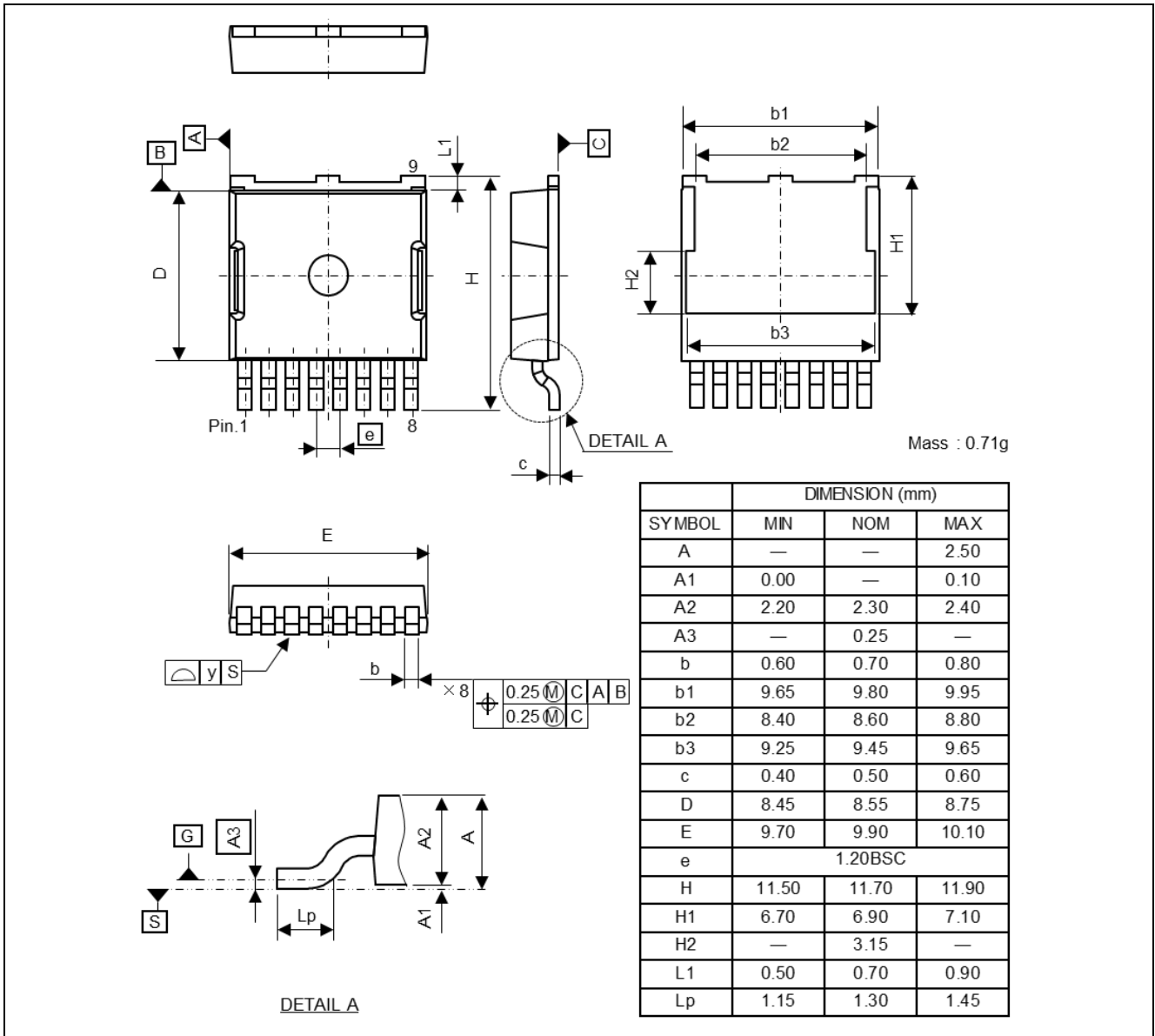
Test Circuit



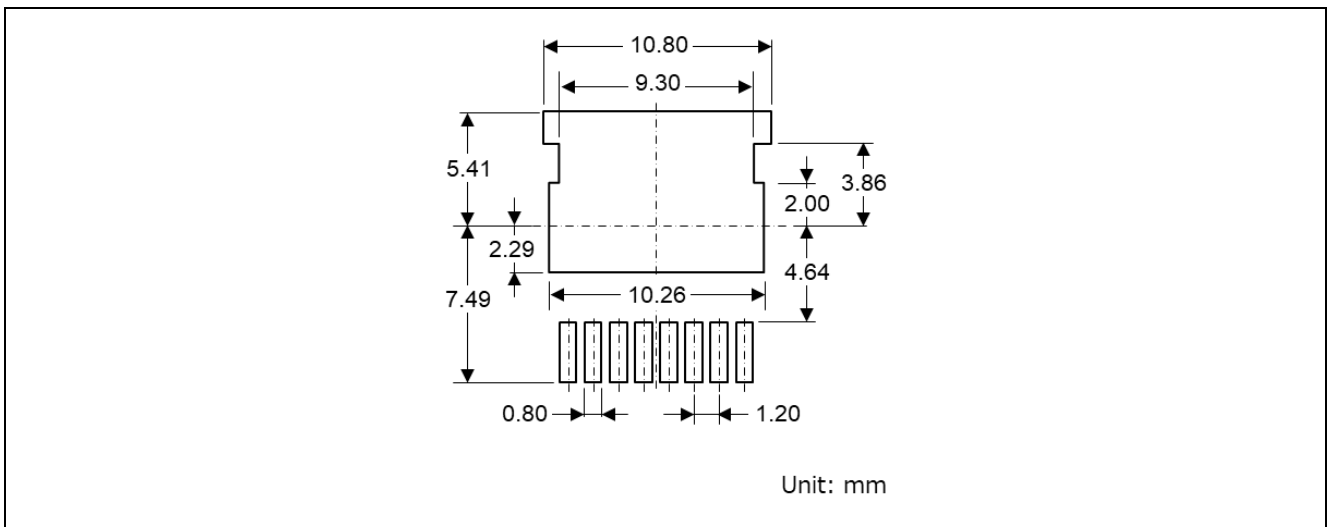
Waveform



Package Dimensions



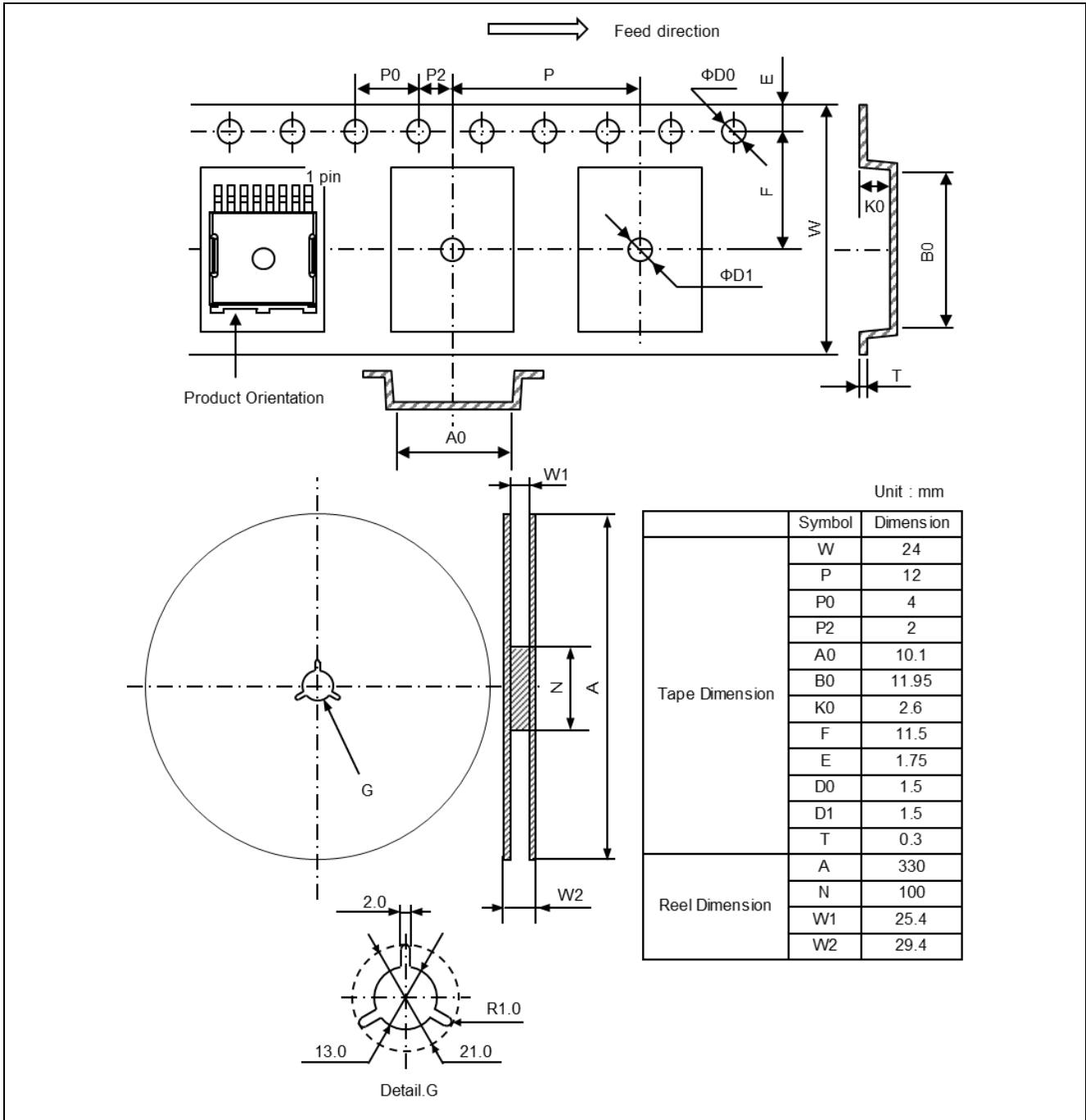
Mount pad



Ordering Information

Part No.	Packing	Quantity
RBA300N10EHPF-5UA02#GB0	Taping	1500pcs/reel

Packing Specification



Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook. As for life test at negative gate bias, not tested at absolute maximum rating.

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