RENESAS

RBA300N10EHPF-5UA02

REXFET-1 N-Channel Power MOSFET

100V - 340A - 1.5mΩ

R07DS1574EJ0100
Rev.1.00
Nov.08.2024

Description

Renesas TOLG technology features ultra compact, gullwing leads designs for compatible with the footprint to the TOLL, enhanced thermal performance, management, and higher thermal cycling on board performance. Renesas new split gate technology provide suitable for use in low RDS(on) and switching capability for high power & high-frequency application.

Features

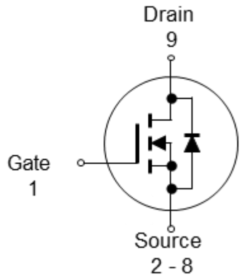
- Standard level gate drive voltage : $V_{GS(th)}$ = 2.0~4.0V
- Super Low on-state resistance : $R_{DS(on)}$ = 1.5mΩ Max.
- Low input capacitance
- Low thermal resistance
- AEC-Q101 qualified
- PPAP capable
- Pb-free lead plating : RoHS compliant
- MSL1 classified according to IPC/JEDEC J-STD-020

Application

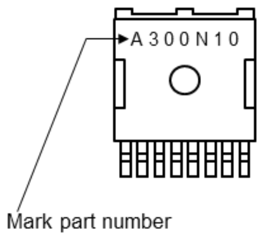
- Automotive : Small Traction (2-wheel, 3-wheel vehicle), 48V load, OBC, Charging station, LDC, etc.
- Industrial / Infrastructure : Energy infrastructure, Micro inverter, Power-tool, DC-DC, etc.

Outline

TOLG



Equivalent Circuit



Marking Specification

Absolute Maximum Ratings

(T_j=25°C unless otherwise notice.)

Item	Symbol	Ratings	Unit
Drain to Source Voltage	V_{DSS}	100	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$ Notes1,2,5	±340	A
Drain Current (Chip limitation)		±380	A
Drain Current (pulse)	$I_{D(pulse)}$ Notes1,3,5	±1360	A
Power Dissipation	P_D Notes1,5	468	W
Junction Temperature	T_j	175	°C
Storage Temperature	T_{stg}	-55 to 175	°C
Single Avalanche Current	I_{AS} Notes4	64	A
Single Avalanche Energy	E_{AS} Notes4	409	mJ

Thermal Resistance

Item	Symbol	Max.	Unit
Junction to Case Thermal Resistance	$R_{th(j\text{-}c)}$ Notes4	0.32	°C/W

Electrical Characteristics

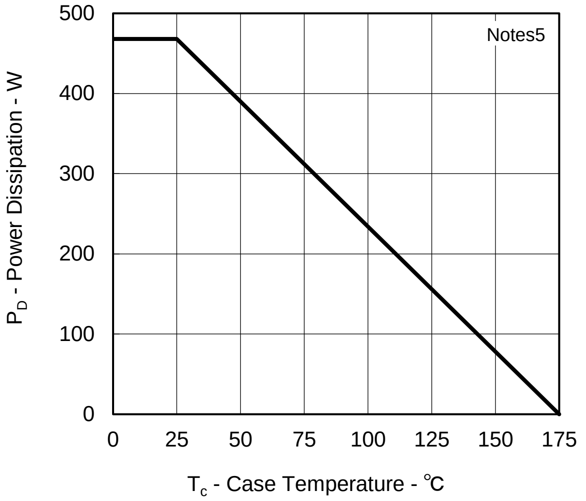
(T_j=25°C unless otherwise notice.)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Zero Gate Voltage Drain Current	I_{DSS}	—	—	10	μA	VDS = 100 V, VGS = 0 V
Gate Leakage Current	I_{GSS}	—	—	±500	nA	VGS = ± 20 V, VDS = 0 V
Gate to Source Threshold Voltage	$V_{GS(th)}$	2.0	—	4.0	V	VDS = VGS, ID = 250 μA
Drain to Source On-state Resistance	$R_{DS(on)}$	—	1.3	1.5	mΩ	VGS = 10 V, ID = 100 A
Input Capacitance	C_{iss}	—	13000	—	pF	VDS = 50 V
Output Capacitance	C_{oss}	—	3300	—	pF	VGS = 0 V
Reverse Transfer Capacitance	C_{rss}	—	80	—	pF	f = 100 kHz
Gate resistance	R_g	—	1.8	—	Ω	
Turn-on Delay Time	$t_{d(on)}$	—	75	—	ns	VDD = 50 V, ID = 100 A
Rise Time	t_r	—	60	—	ns	VGS = 10 V
Turn-off Delay Time	$t_{d(off)}$	—	130	—	ns	RG = 5 Ω
Fall Time	t_f	—	55	—	ns	
Total Gate Charge	Q_g	—	170	—	nC	VDD = 50 V
Gate to Source Charge	Q_{gs}	—	75	—	nC	VGS = 10 V
Gate to Drain Charge	Q_{gd}	—	30	—	nC	ID = 100 A
Body Diode Forward Voltage	$V_{F(S\text{-}D)}$	—	0.9	1.5	V	IF = 100 A, VGS = 0 V
Reverse Recovery Time	t_{rr}	—	110	—	ns	IF = 100 A, VGS = 0 V
Reverse Recovery Charge	Q_{rr}	—	300	—	nC	di/dt = 100 A/μs

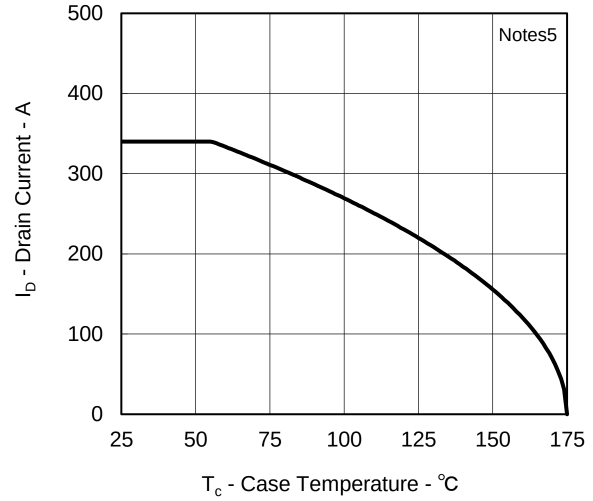
Notes
1. T_c = 25°C
2. Value is limited by overall system design including PCB.
3. PW ≤ 10 μs
4. L = 100μH , V_{DD} = 50V , V_{GS} = 20 → 0V , R_G = 25 Ω
5. Defined by design. Not subject to production test.

Typical Characteristics

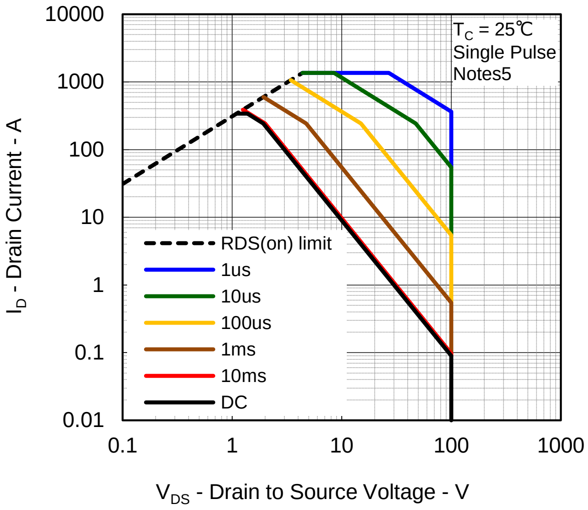
POWER DISSIPATION vs. CASE TEMPERATURE



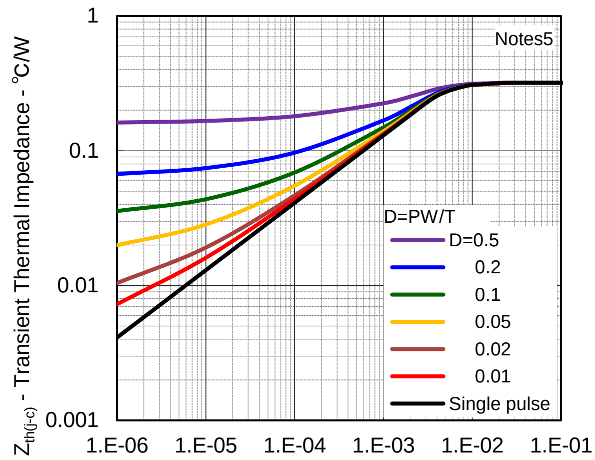
DRAIN CURRENT vs. CASE TEMPERATURE



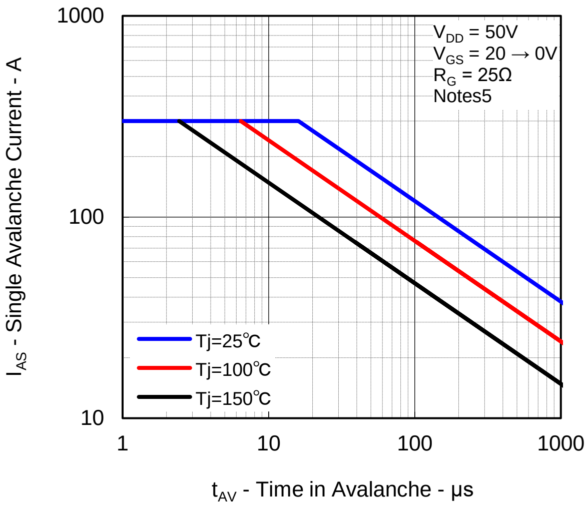
FORWARD BIAS SAFE OPERATING AREA



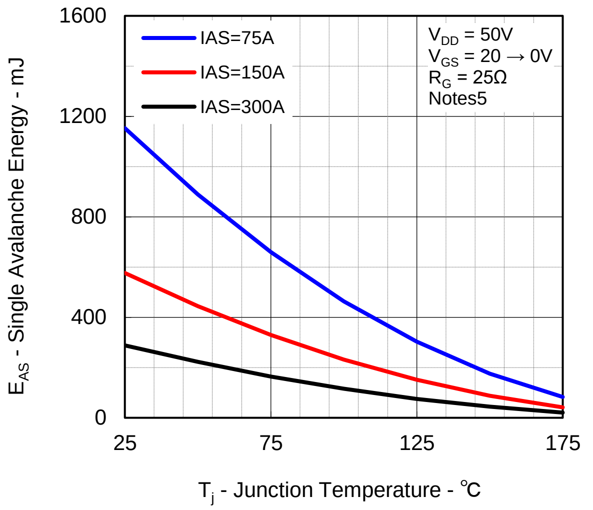
TRANSIENT THERMAL IMPEDANCE vs.
PULSE WIDTH



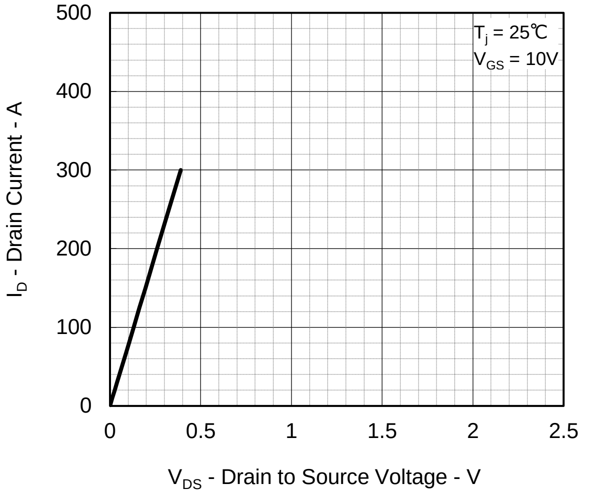
TYPICAL AVALANCHE CHARACTERISTICS



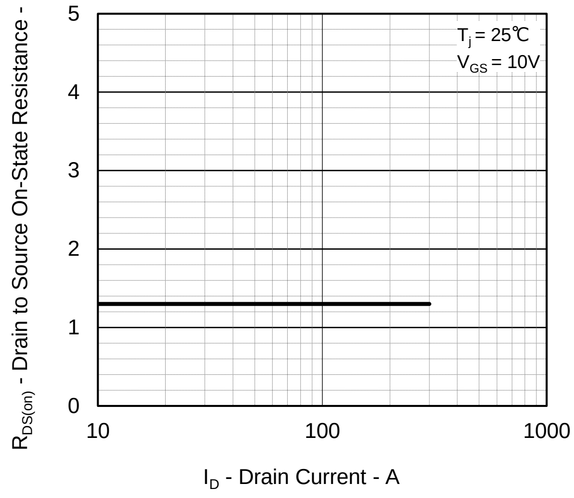
TYPICAL AVALANCHE ENERGY



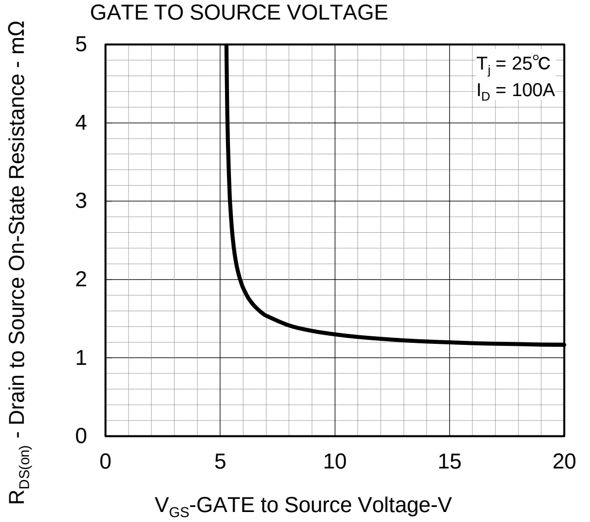
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



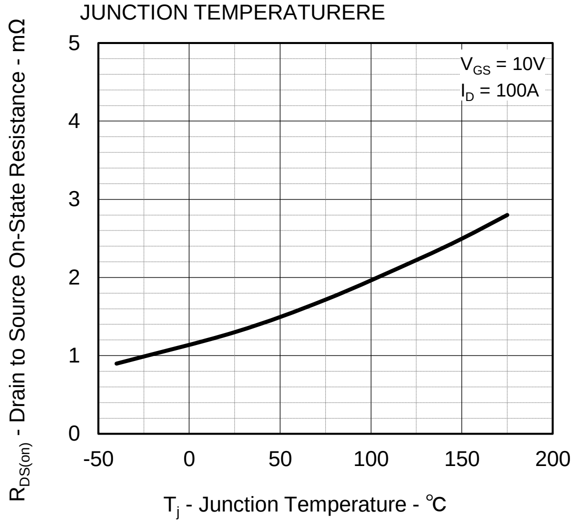
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



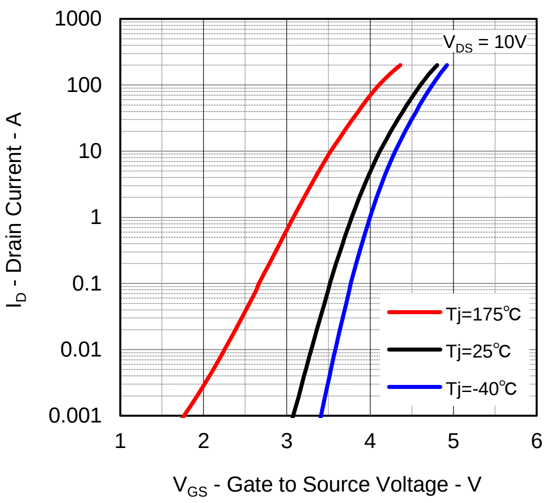
DRAIN TO SOURCE ON-STATERESISTANCE vs. GATE TO SOURCE VOLTAGE



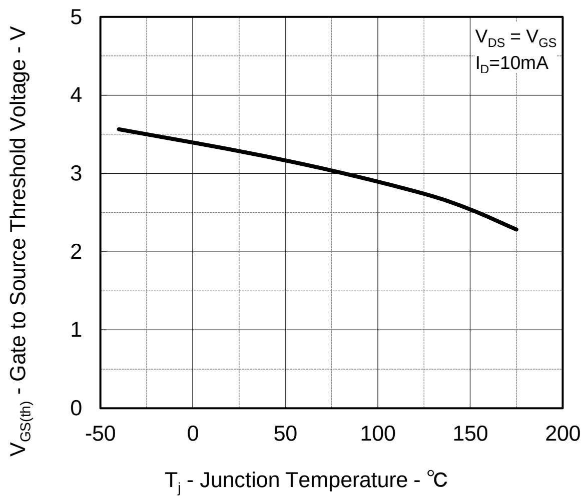
DRAIN TO SOURCE ON-STATE RESISTANCE vs JUNCTION TEMPERATURERE

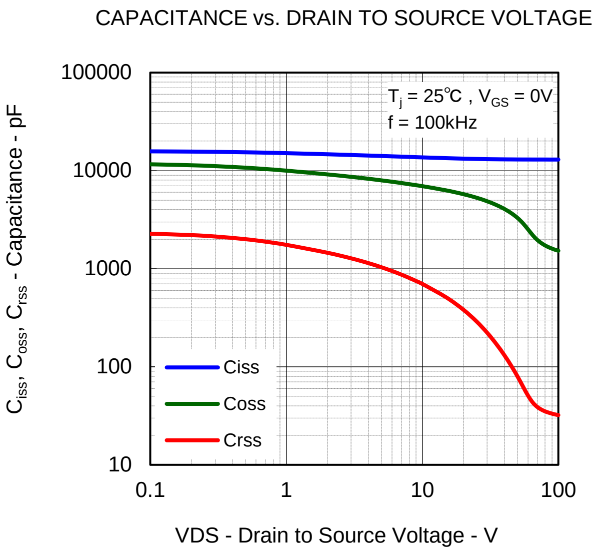


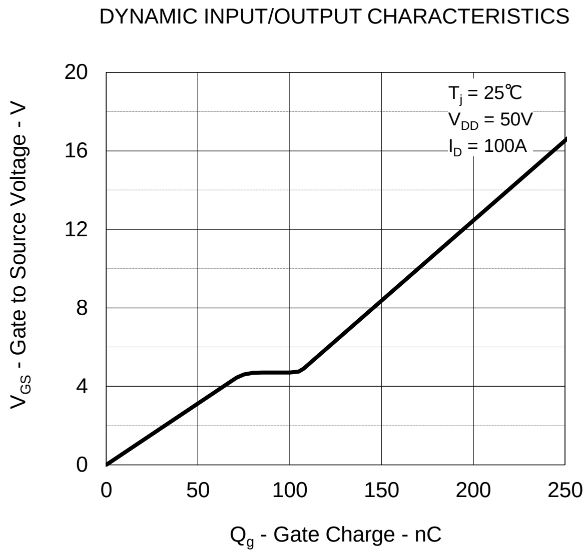
FORWARD TRANSFER CHARACTERISTICS

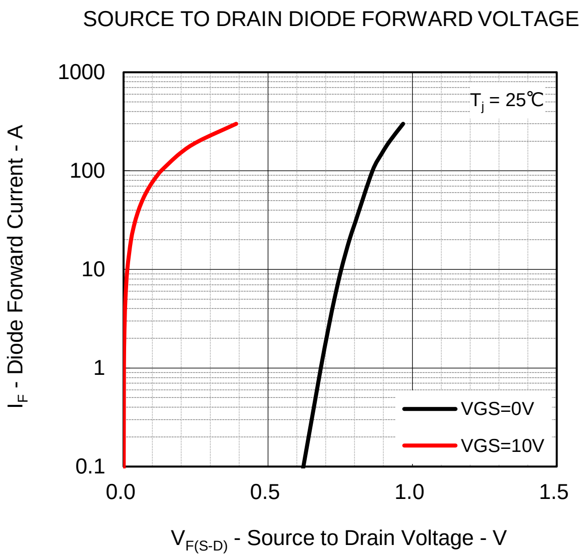


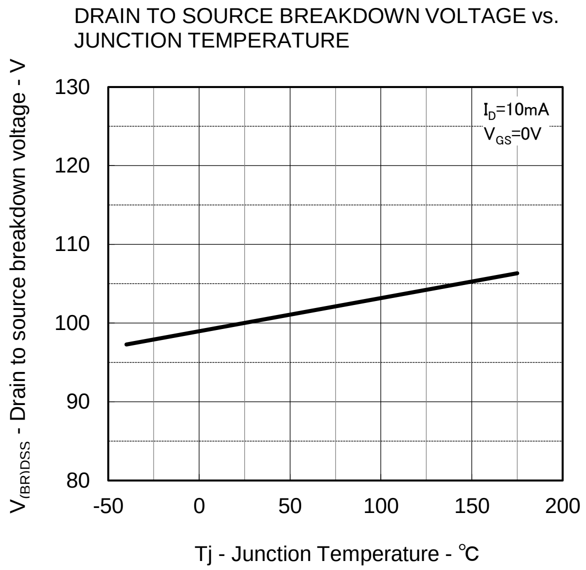
GATE TO SOURCE THRESHOLD VOLTAGE vs. JUNCTION TEMPERATURE




CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE
T_j = 25℃ , V_{GS} = 0V
f = 100kHz
Ciss
Coss
Crss
C_{iss}, C_{oss}, C_{rss} - Capacitance - pF
VDS - Drain to Source Voltage - V


DYNAMIC INPUT/OUTPUT CHARACTERISTICS
T_j = 25℃
V_{DD} = 50V
I_D = 100A
V_{GS} - Gate to Source Voltage - V
Q_g - Gate Charge - nC

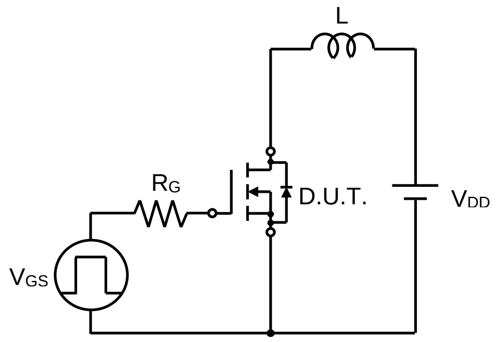

SOURCE TO DRAIN DIODE FORWARD VOLTAGE
T_j = 25℃
VGS=0V
VGS=10V
I_F - Diode Forward Current - A
$V_{F(S-D)}$ - Source to Drain Voltage - V


DRAIN TO SOURCE BREAKDOWN VOLTAGE vs. JUNCTION TEMPERATURE
I_D=10mA
V_{GS}=0V
$V_{(BR)DSS}$ - Drain to source breakdown voltage - V
Tj - Junction Temperature - ℃

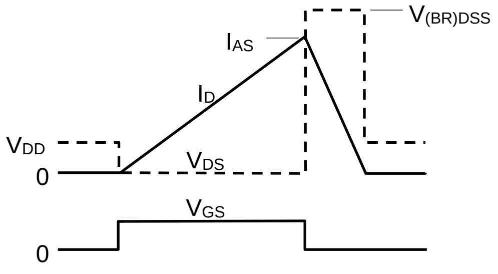
Test Circuit

Avalanche

Test Circuit



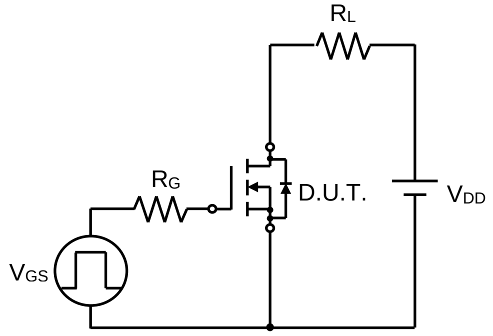
Waveform



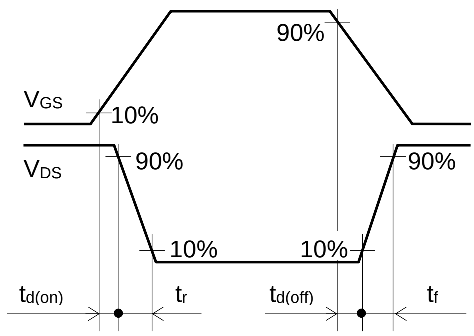
$$E_{AS} = \frac{1}{2} \cdot L \cdot I_{AS}^{2} \cdot \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

Switching Time

Test Circuit

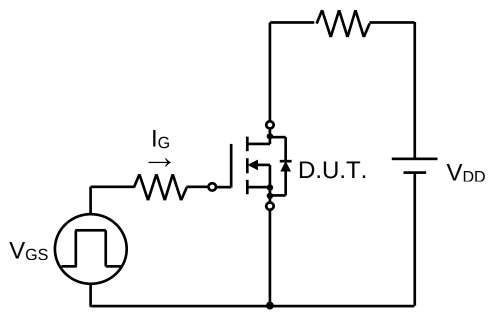


Waveform

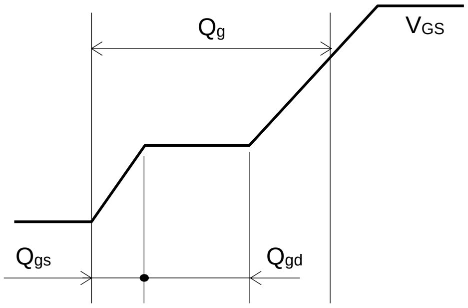


Gate Charge

Test Circuit

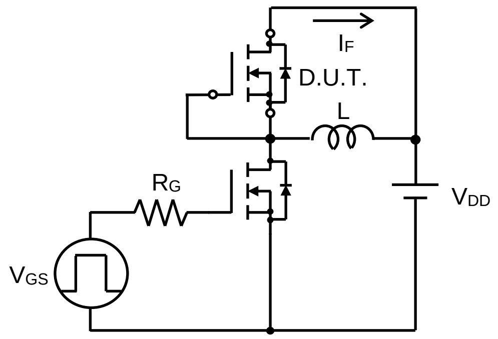


Waveform

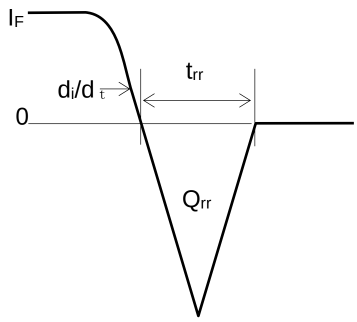


Reverse Recovery

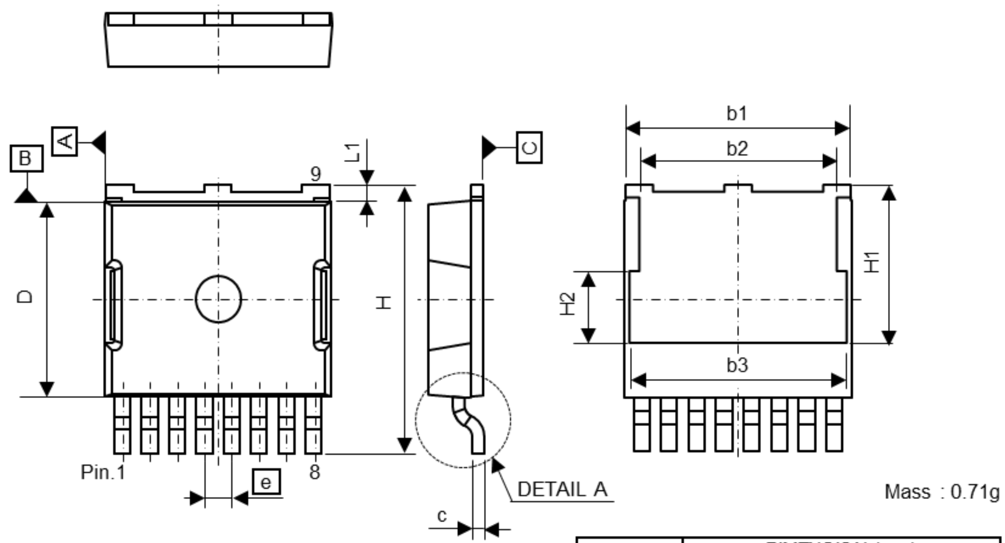
Test Circuit

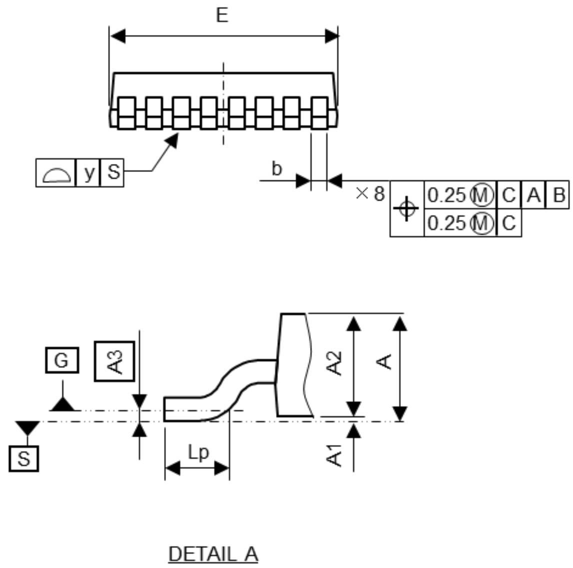


Waveform



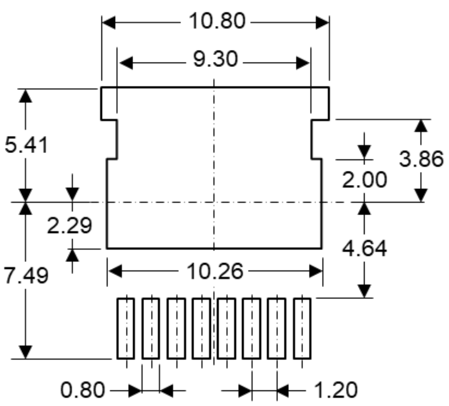
Package Dimensions





	DIMENSION (mm)		
SYMBOL	MIN	NOM	MAX
A	—	—	2.50
A1	0.00	—	0.10
A2	2.20	2.30	2.40
A3	—	0.25	—
b	0.60	0.70	0.80
b1	9.65	9.80	9.95
b2	8.40	8.60	8.80
b3	9.25	9.45	9.65
c	0.40	0.50	0.60
D	8.45	8.55	8.75
E	9.70	9.90	10.10
e	1.20BSC		
H	11.50	11.70	11.90
H1	6.70	6.90	7.10
H2	—	3.15	—
L1	0.50	0.70	0.90
Lp	1.15	1.30	1.45

Mount pad

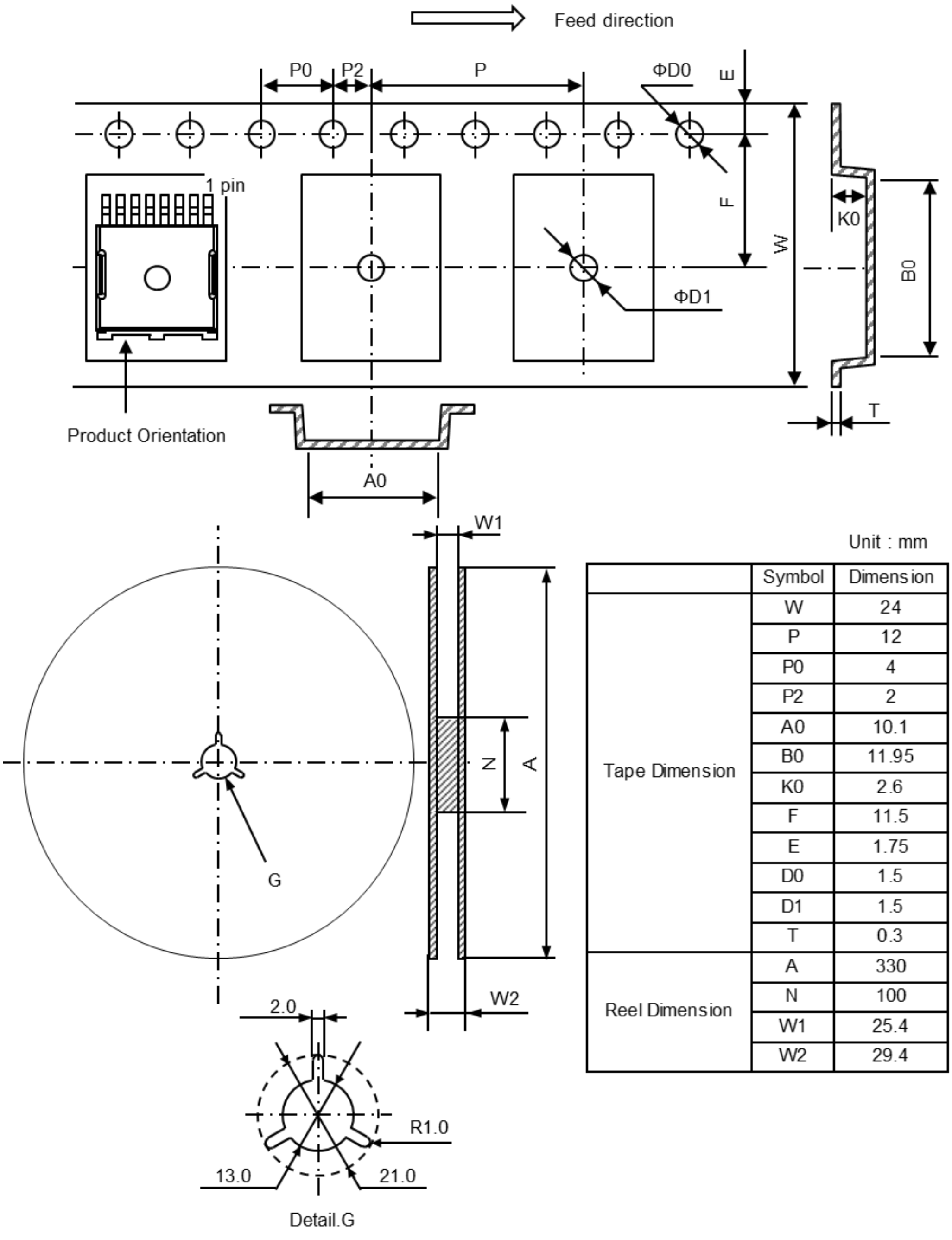


Unit: mm

Ordering Information

Part No.	Packing	**Quantity**
RBA300N10EHPF-5UA02#GB0	Taping	1500pcs/reel

Packing Specification



Unit : mm

	Symbol	Dimension
Tape Dimension	W	24
	P	12
	P0	4
	P2	2
	A0	10.1
	B0	11.95
	K0	2.6
	F	11.5
	E	1.75
	D0	1.5
	D1	1.5
	T	0.3
Reel Dimension	A	330
	N	100
	W1	25.4
	W2	29.4

Remark : Strong electric field, when exposed to this device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred.

Continuous heavy condition (e.g. high temperature/voltage/current or high variation of temperature) may affect reliability even if it is within the absolute maximum ratings. Please consider derating condition for appropriate reliability in reference Renesas Semiconductor Reliability Handbook. As for life test at negative gate bias, not tested at absolute maximum rating.

Corporate Headquarters

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Contact information

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