RC191xx

PCIe Gen7 1.8V Fanout Buffer Family with LOS

The RC191xx (RC19108, RC19104, and RC19102) ultra-high performance fanout buffers support PCIe Gen1-7. They provide a Loss-Of-Signal (LOS) output for system monitoring and redundancy. The devices also incorporate Power Down Tolerant (PDT) and Flexible Startup Sequencing (FSS) features, easing system design. They can drive both source-terminated and double-terminated loads, operating up to 400MHz.

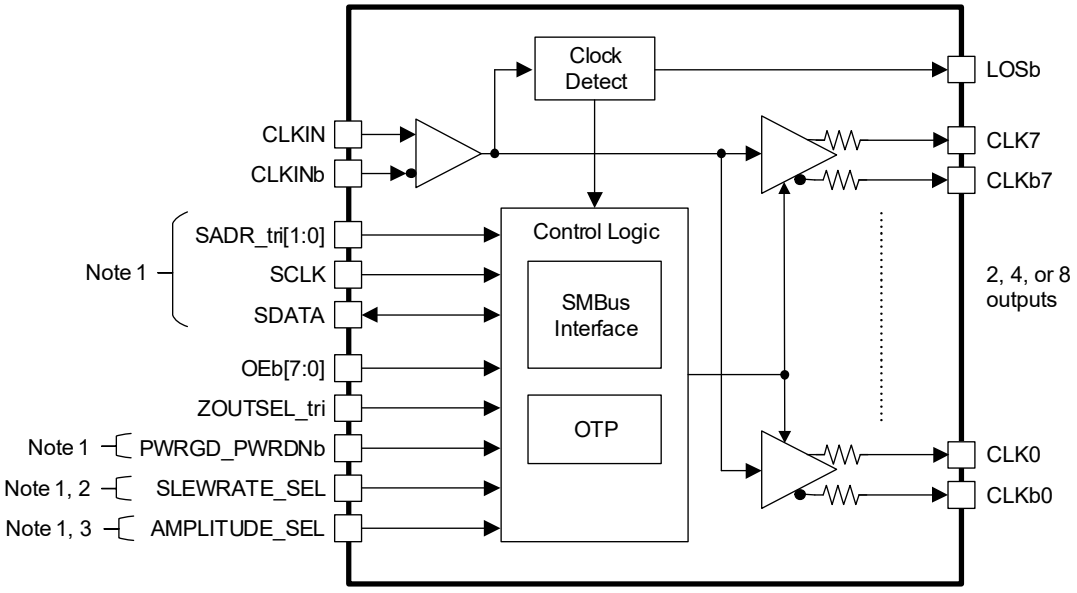
The family offers 2, 4, or 8 Low-Power (LP) HCSL output pairs in 3 × 3, 4 × 4, and 5 × 5 mm packages. The RC191xx devices offer higher output counts in smaller packages compared to earlier buffer families. The buffers support both Common Clock (CC) and Independent Reference (IR) PCIe clock architectures.

Applications

- Cloud/High-performance computing
- nVME storage
- Networking
- AI Accelerators

Features

- PCIe Gen5 additive phase jitter: 5.9fs RMS
- PCIe Gen6 additive phase jitter: 3.5fs RMS
- PCIe Gen7 additive phase jitter: 2.4fs RMS
- DB2000Q additive phase jitter: 10fs RMS
- 12kHz to 20MHz additive phase jitter: 33fs RMS at 156.25MHz
- Power Down Tolerant (PDT) inputs
- Flexible Startup Sequencing (FSS)
- Automatic Clock Parking (ACP) upon loss of CLKIN
- Spread-spectrum tolerant
- CLKIN accepts HCSL or LVDS signal levels
- -40 to +105°C, 1.8V ± 5% operation
- Devices provide:
  - Pin or SMBus selectable 33Ω, 85Ω, or 100Ω differential output impedance
  - Pin or SMBus selectable output slew rate
  - Pin or SMBus selectable output amplitude
  - 9 SMBus addresses plus write protection



1. RC19102 does not have these pins.
2. RC19108, RC19104 only.
3. RC19108A001 and RC19104A001 only.

Figure 1. RC191xx Block Diagram

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1. Pin Information

1.1 Signal Types

Term	Description [1]
I	Input
O	Input
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don’t care
SE	Single ended
DIF	Differential
PWR	1.8 V power
GND	Ground
PDT	Power Down Tolerant: These signals tolerate being driven when the device is powered down. For information, see Absolute Maximum Ratings.

1. Some pins have both internal pull-up and pull-down resistors which bias the pins to VDD/2. Other pins are multi-mode and have an internal pull-up or internal pull-down depending on the mode.

1.2 RC19108 Pin Information

1.2.1 RC19108 Pin Assignments

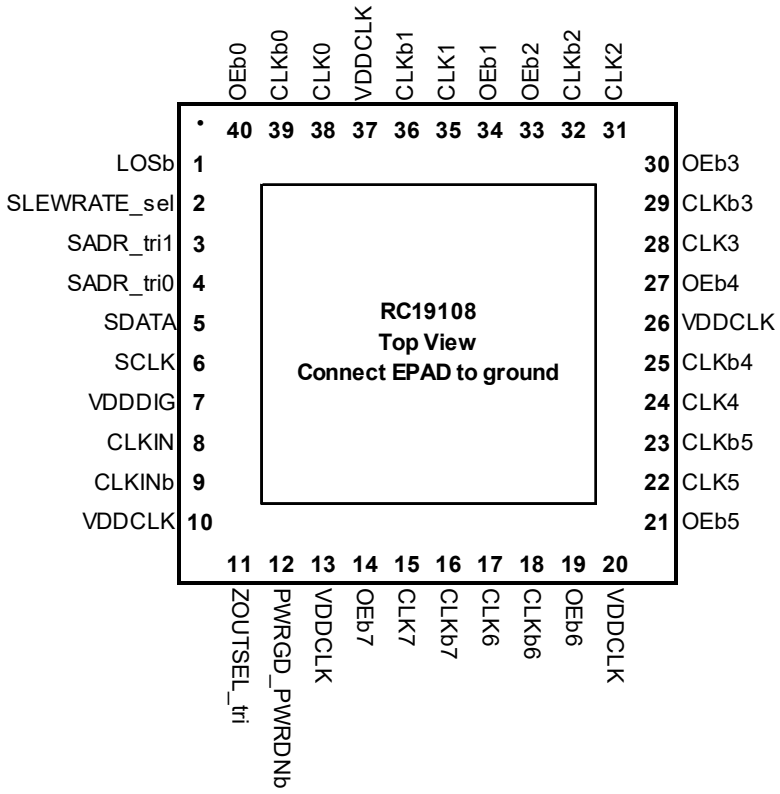


Figure 2. RC19108 40-VFQFPN – Top View

1.2.2 RC19108 Pin Descriptions

Table 1. RC19108 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
2	SLEWRATE_SEL	I, SE, PU, PDT	Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate.
3	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and tri-level input thresholds in the electrical tables.
4	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and tri-level input thresholds in the electrical tables.
5	SDATA	I/O, SE, OD	Data pin for SMBus interface.
6	SCLK	I, SE	Clock pin of SMBus interface.
7	VDDDIG	PWR	Digital power.
8	CLKIN	I, DIF	True clock input.
9	CLKINb	I, DIF	Complementary clock input.
10	VDDCLK	PWR	Clock Power supply.
11	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85ohm, 1 = 100ohm, M = 33ohm

Table 1. RC19108 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
12	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
13	VDDCLK	PWR	Clock power supply.
14	OEb7	I, SE, PU, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.
15	CLK7	O, DIF	True clock output.
16	CLKb7	O, DIF	Complementary clock output.
17	CLK6	O, DIF	True clock output.
18	CLKb6	O, DIF	Complementary clock output.
19	OEb6	I, SE, PU, PDT	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output.
20	VDDCLK	PWR	Clock power supply.
21	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
22	CLK5	O, DIF	True clock output.
23	CLKb5	O, DIF	Complementary clock output.
24	CLK4	O, DIF	True clock output.
25	CLKb4	O, DIF	Complementary clock output.
26	VDDCLK	PWR	Clock Power supply.
27	OEb4	I, SE, PU, PDT	Active low input for enabling output 4. 0 = Enable output, 1 = Disable output.
28	CLK3	O, DIF	True clock output.
29	CLKb3	O, DIF	Complementary clock output.
30	OEb3	I, SE, PU, PDT	Active low input for enabling output 3. 0 = Enable output, 1 = Disable output.
31	CLK2	O, DIF	True clock output.
32	CLKb2	O, DIF	Complementary clock output.
33	OEb2	I, SE, PU, PDT	Active low input for enabling output 2. 0 = Enable output, 1 = Disable output.
34	OEb1	I, SE, PU, PDT	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
35	CLK1	O, DIF	True clock output.
36	CLKb1	O, DIF	Complementary clock output.
37	VDDCLK	PWR	Clock power supply.
38	CLK0	O, DIF	True clock output.
39	CLKb0	O, DIF	Complementary clock output.
40	OEb0	I, SE, PU, PDT	Active low input for enabling output 0. 0 = Enable output, 1 = Disable output.
41	EPAD	GND	Connect Epad to ground.

1.3 RC19108A001 Pin Information

1.3.1 RC19108A001 Pin Assignments

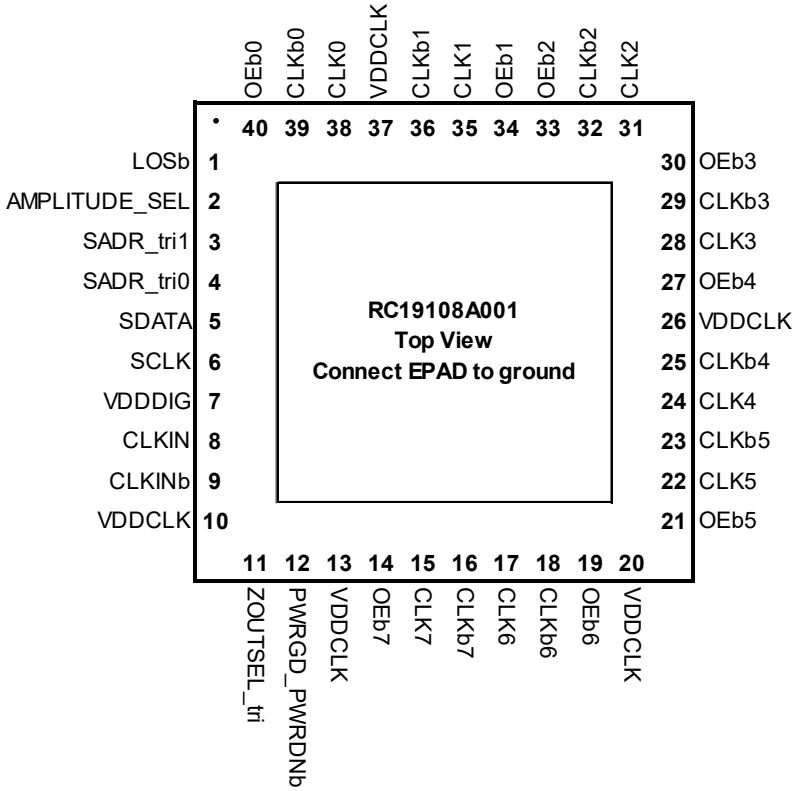


Figure 3. RC19108 40-VFQFPN – Top View

1.3.2 RC19108A001 Pin Descriptions

Table 2. RC19108A001 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open-drain output and requires an external pull-up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
2	AMPLITUDE_SEL	I, SE, PD, PD	Input to select output amplitude. The values are programmable with defaults listed below. For the default amplitude and AMP_CTRL_ALT for the alternate amplitude, see AMP_CTRL_DEF. 0 = Select Default Amplitude (800mV), 1 = Select Alternate Amplitude (900mV)
3	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and tri-level input thresholds in the electrical tables.
4	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and tri-level input thresholds in the electrical tables.
5	SDATA	I/O, SE, OD	Data pin for SMBus interface.
6	SCLK	I, SE	Clock pin of SMBus interface.
7	VDDDIG	PWR	Digital power.
8	CLKIN	I, DIF	True clock input.
9	CLKINb	I, DIF	Complementary clock input.
10	VDDCLK	PWR	Clock Power supply.

Table 2. RC19108A001 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
11	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85ohm, 1 = 100ohm, M = 33ohm
12	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
13	VDDCLK	PWR	Clock power supply.
14	OEb7	I, SE, PU, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.
15	CLK7	O, DIF	True clock output.
16	CLKb7	O, DIF	Complementary clock output.
17	CLK6	O, DIF	True clock output.
18	CLKb6	O, DIF	Complementary clock output.
19	OEb6	I, SE, PU, PDT	Active low input for enabling output 6. 0 = Enable output, 1 = Disable output.
20	VDDCLK	PWR	Clock power supply.
21	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
22	CLK5	O, DIF	True clock output.
23	CLKb5	O, DIF	Complementary clock output.
24	CLK4	O, DIF	True clock output.
25	CLKb4	O, DIF	Complementary clock output.
26	VDDCLK	PWR	Clock Power supply.
27	OEb4	I, SE, PU, PDT	Active low input for enabling output 4. 0 = Enable output, 1 = Disable output.
28	CLK3	O, DIF	True clock output.
29	CLKb3	O, DIF	Complementary clock output.
30	OEb3	I, SE, PU, PDT	Active low input for enabling output 3. 0 = Enable output, 1 = Disable output.
31	CLK2	O, DIF	True clock output.
32	CLKb2	O, DIF	Complementary clock output.
33	OEb2	I, SE, PU, PDT	Active low input for enabling output 2. 0 = Enable output, 1 = Disable output.
34	OEb1	I, SE, PU, PDT	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
35	CLK1	O, DIF	True clock output.
36	CLKb1	O, DIF	Complementary clock output.
37	VDDCLK	PWR	Clock power supply.
38	CLK0	O, DIF	True clock output.
39	CLKb0	O, DIF	Complementary clock output.
40	OEb0	I, SE, PU, PDT	Active low input for enabling output 0. 0 = Enable output, 1 = Disable output.
41	EPAD	GND	Connect Epad to ground.

1.4 RC19104 Pin Information

1.4.1 RC19104 Pin Assignments

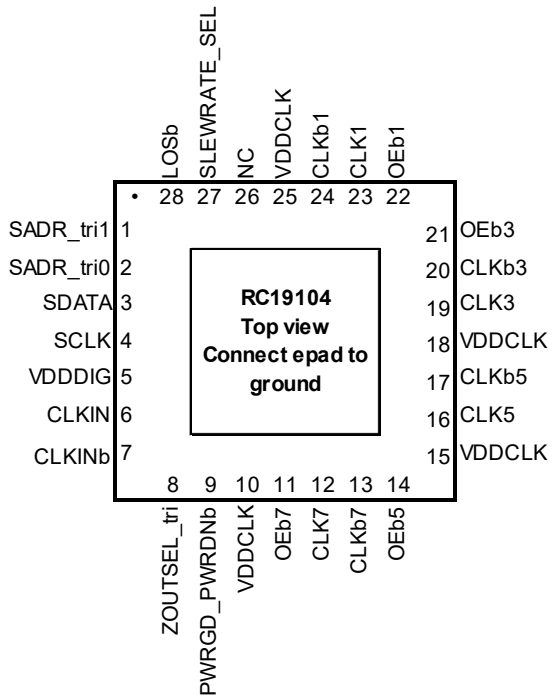


Figure 4. RC19104 28-VFQFPN – Top View

1.4.2 RC19104 Pin Descriptions

Table 3. RC19104 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
2	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
3	SDATA	I/O, SE, OD	Data pin for SMBus interface.
4	SCLK	I, SE	Clock pin of SMBus interface.
5	VDDDIG	PWR	Digital power.
6	CLKIN	I, DIF	True clock input.
7	CLKINb	I, DIF	Complementary clock input.
8	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85ohm, 1 = 100ohm, M = 33ohm
9	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
10	VDDCLK	PWR	Clock power supply.
11	OEb7	I, SE, PU, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.
12	CLK7	O, DIF	True clock output.
13	CLKb7	O, DIF	Complementary clock output.
14	OEb5	I, SE, PD, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.

Table 3. RC19104 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
15	VDDCLK	PWR	Clock power supply.
16	CLK5	O, DIF	True clock output.
17	CLKb5	O, DIF	Complementary clock output.
18	VDDCLK	PWR	Clock power supply.
19	CLK3	O, DIF	True clock output.
20	CLKb3	O, DIF	Complementary clock output.
21	OEb3	I, SE, PDT, PU	Active low input for enabling output 3. OE mode with internal pull-down: 0 = Enable output, 1 = Disable output.
22	OEb1	I, SE, PDT, PU	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
23	CLK1	O, DIF	True clock output.
24	CLKb1	O, DIF	Complementary clock output.
25	VDDCLK	PWR	Clock power supply.
26	NC	NC	No connect.
27	SLEWRATE_SEL	I, SE, PU, PDT	Input to select default slew rate of the outputs. 0 = Slow Slew Rate, 1 = Fast Slew Rate.
28	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
29	EPAD	GND	Connect to ground.

1.5 RC19104A001 Pin Information

1.5.1 RC19104A001 Pin Assignments

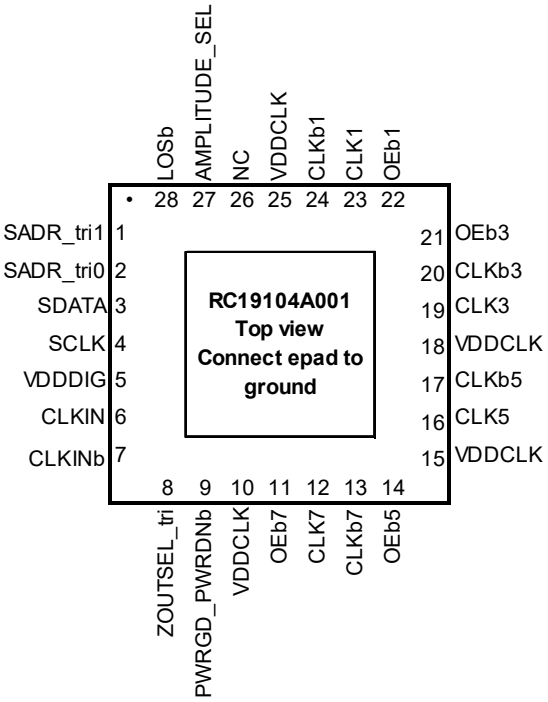


Figure 5. RC19104A100 28-VFQFPN – Top View

1.5.2 RC19104A001 Pin Descriptions

Table 4. RC19104A100 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
2	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Decode table and the tri-level input thresholds in the electrical tables.
3	SDATA	I/O, SE, OD	Data pin for SMBus interface.
4	SCLK	I, SE	Clock pin of SMBus interface.
5	VDDDIG	PWR	Digital power.
6	CLKIN	I, DIF	True clock input.
7	CLKINb	I, DIF	Complementary clock input.
8	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85ohm, 1 = 100ohm, M = 33ohm
9	PWRGD_PWRDNb	I, SE, PU, PDT	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
10	VDDCLK	PWR	Clock power supply.
11	OEb7	I, SE, PU, PDT	Active low input for enabling output 7. 0 = Enable output, 1 = Disable output.
12	CLK7	O, DIF	True clock output.
13	CLKb7	O, DIF	Complementary clock output.
14	OEb5	I, SE, PD, PDT	Active low input for enabling output 5. 0 = Enable output, 1 = Disable output.
15	VDDCLK	PWR	Clock power supply.
16	CLK5	O, DIF	True clock output.
17	CLKb5	O, DIF	Complementary clock output.
18	VDDCLK	PWR	Clock power supply.
19	CLK3	O, DIF	True clock output.
20	CLKb3	O, DIF	Complementary clock output.
21	OEb3	I, SE, PDT, PU	Active low input for enabling output 3. OE mode with internal pull-down: 0 = Enable output, 1 = Disable output.
22	OEb1	I, SE, PDT, PU	Active low input for enabling output 1. 0 = Enable output, 1 = Disable output.
23	CLK1	O, DIF	True clock output.
24	CLKb1	O, DIF	Complementary clock output.
25	VDDCLK	PWR	Clock power supply.
26	NC	NC	No connect.
27	AMPLITUDE_SEL	I, SE, PD, PD	Input to select output amplitude. The values are programmable. See register map for details. 0 = Select Amplitude 0, 1 = Select Amplitude 1
28	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
29	EPAD	GND	Connect to ground.

1.6 RC19102 Pin Information

1.6.1 RC19102 Pin Assignments

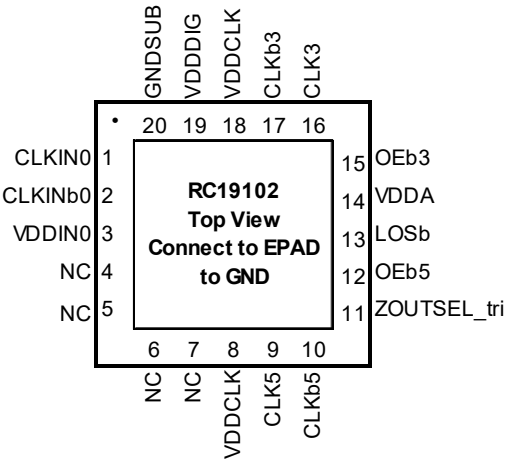


Figure 6. RC19102 20-VFQFPN – Top View

1.6.2 RC19102 Pin Descriptions

Table 5. RC19102 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	CLKIN0	I, DIF, PDT	True clock input.
2	CLKINb0	I, DIF, PDT	Complementary clock input.
3	VDDCLK	PWR	Clock power supply.
4	NC	NC	No connect.
5	NC	NC	No connect.
6	NC	NC	No connect.
7	NC	NC	No connect.
8	VDDCLK	PWR	Clock power supply.
9	CLK5	O, DIF	True clock output.
10	CLKb5	O, DIF	Complementary clock output.
11	ZOUTSEL_tri	I, SE, PD	Input to select differential output impedance. 0 = 85ohm, 1 = 100ohm, M = 33ohm
12	OEb5	I, SE, PU, PDT	Active low input for enabling output 5. 1 = disable output, 0 = enable output.
13	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
14	VDDCLK	PWR	Clock power supply.
15	OEb3	I, SE, PU, PDT	Active low input for enabling output 3. 1 = disable output, 0 = enable output.
16	CLK3	O, DIF	True clock output.
17	CLKb3	O, DIF	Complementary clock output.
18	VDDCLK	PWR	Clock power supply.
19	VDDDIG	PWR	Digital power.
20	GNDSUB	GND	Ground pin for substrate.
21	EPAD	GND	Connect to ground.

2. Specifications

2.1 Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Condition	Minimum	Maximum	Unit
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin	-0.5	2.2	V
V_{IN}	Input Voltage for non-PDT inputs	Input pins not labeled as PDT [1]	-0.5	V_{DDx} + 0.3	V
V_{INPDT}	Input Voltage for PDT inputs	PDT input pins, see below for LOSb output pin [2]	-0.5	3.6	V
V_{PUPSMB}	Pull up resistor voltage for SMBus interface	SCLK, SDATA pins			
V_{PUPLOS}	Pull up resistor voltage for LOSb pin	LOSb pin [3]	-0.5	1.9	V
I_{IN}	Input Current	All SE inputs and CLKIN [1]	-	±50	mA
I_{OUT}	Output Current – Continuous	CLK	-	30	mA
		SDATA	-	25	mA
	Output Current – Surge	CLK	-	60	mA
		SDATA	-	50	mA
T_J	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
ESD	Human Body Model	JESD22-A114 (JS-001) Classification	-	2000	V
	Charged Device Model	JESD22-C101 Classification	-	500	V

1. Inputs not designated Power Down Tolerant (PDT) in the pin description tables.
2. Inputs designated Power Down Tolerant (PDT) in the pin description tables.
3. The V_{PUP} voltage may be applied before main VDD is applied. The LOSb pin is PDT to this voltage, not to 3.6V.

Table 7. Recommended Operation Conditions

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	25	105	°C
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin, 1.8V ±5% supply.	1.71	1.8	1.89	V
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

2.2 Thermal Specifications

Table 8. Thermal Characteristics

Package [1]	Symbol	Condition	Typical Value (°C/W)
5 × 5 mm 40-VFQFPN (3.3 × 3.3 mm ePad)	θ_{Jc}	Junction to Case	37.0
	θ_{Jb}	Junction to Base	4.8
	θ_{JA0}	Junction to Ambient, still air	33.1
	θ_{JA1}	Junction to Ambient, 1 m/s air flow	29.6
	θ_{JA3}	Junction to Ambient, 3 m/s air flow	28.0
	θ_{JA5}	Junction to Ambient, 5 m/s air flow	27.1
4 × 4 mm 28-VFQFPN (2.6 × 2.6 mm ePad)	θ_{Jc}	Junction to Case	45.3
	θ_{Jb}	Junction to Board	2.2
	θ_{JA0}	Junction to Ambient, still air	36.3
	θ_{JA1}	Junction to Ambient, 1 m/s air flow	32.7
	θ_{JA3}	Junction to Ambient, 3 m/s air flow	31.0
	θ_{JA5}	Junction to Ambient, 5 m/s air flow	30.0
3 × 3 mm 20-VFQFPN (1.65 × 1.65 mm Epad)	θ_{Jc}	Junction to Case	96.3
	θ_{Jb}	Junction to Board	20.4
	θ_{JA0}	Junction to Ambient, still air	54.8
	θ_{JA1}	Junction to Ambient, 1 m/s air flow	51.1
	θ_{JA3}	Junction to Ambient, 3 m/s air flow	47.7
	θ_{JA5}	Junction to Ambient, 5 m/s air flow	46.2

1. ePad soldered to board.

2.3 Electrical Specifications

2.3.1 Phase Jitter

Table 9. PCIe Refclk Phase Jitter - Normal Conditions [1][2][3]

Symbol	Parameter	Condition	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC 0 or -0.5%	PCIe Gen1 (2.5 GT/s)	321	501	86,000	fs p-p
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	44	60	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	16	22	3,000	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	15	20	1,000	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [4][5]	15	20	500	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [4] [6]	5.9	8.0	150	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [4] [7]	3.5	4.7	100	
$t_{jphPCIeG7-CC}$		PCIe Gen7 (128 GT/s) [4][8]	2.4	3.3	100	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.5%	PCIe Gen2 (5.0 GT/s)	37	48	[9]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	15	19		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3] [4]	15	20		
$t_{jphPCIeG5-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.3%	PCIe Gen5 (32.0 GT/s) [3] [5]	4.3	5.6		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3] [7]	3.0	3.9		
$t_{jphPCIeG7-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.15%	PCIe Gen7 (128 GT/s) [3][7]	2.1	2.7		

1. The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 7.0, Revision 0.7*. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
5. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The *PCI Express Base Specification 7.0, Revision 0.7* provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 10. PCIe Refclk Phase Jitter - Degraded Conditions [1][2][3]

Symbol	Parameter	Condition	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture) SSC 0 or -0.5%	PCIe Gen1 (2.5 GT/s)	321	536	86,000	fs p-p
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	44	67	3,100	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	16	22	3,000	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	15	23	1,000	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [4][5]	15	23	500	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [4] [6]	5.9	8.9	150	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [4] [7]	3.5	5.2	100	
$t_{jphPCIeG7-CC}$		PCIe Gen7 (128 GT/s) [4][8]	2.4	3.7	100	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.5%	PCIe Gen2 (5.0 GT/s)	37	54	[9]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	15	22		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3] [4]	15	22		
$t_{jphPCIeG5-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.3%	PCIe Gen5 (32.0 GT/s) [3] [5]	4.3	6.3		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3] [7]	3.0	4.5		
$t_{jphPCIeG7-IR}$	Additive PCIe Phase Jitter (IR Architectures - SRIS, SRNS) SSC 0 or -0.15%	PCIe Gen7 (128 GT/s) [3][7]	2.1	3.1		

1. The Refclk jitter is measured after applying the filter functions found in the *PCI Express Base Specification 7.0, Revision 0.7*. For the exact measurement setup, see Test Loads. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements are made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be made with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. Differential input swing ≥ 1600mV and input slew rate ≥ 3.5V/ns. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
4. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
5. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
8. Note that 0.10ps RMS is to be used in channel simulations to account for additional noise in a real system.
9. The *PCI Express Base Specification 7.0, Revision 0.7* provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, therefore, the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user can choose to use this more relaxed value as the jitter limit.

Table 11. Non-PCIe Refclk Phase Jitter [1][2][3]

Symbol	Parameter	Condition	Typical	Maximum	Specification Limit	Unit
$t_{jphDB2000Q}$	Additive Phase Jitter - normal conditions[4]	100MHz, Intel-supplied filter [3]	9.4	12.0	80 [5]	fs RMS
$t_{jph12k-20M}$		156.25MHz (12kHz to 20MHz)	37	45	N/A	
$t_{jphDB2000Q}$	Additive Phase Jitter - degraded conditions [6]	100MHz, Intel-supplied filter [3]	9.4	13.4	80 [5]	
$t_{jph12k-20M}$		156.25MHz (12kHz to 20MHz)	37	47	N/A	

1. See Test Loads for test configuration.
2. SMA100B used as signal source.
3. The RC19xxx devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. Differential input swing = 1,600mV and input slew rate = 3.5V/ns.
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns.

2.3.2 Output Frequencies, Startup Time, and LOS Timing

Table 12. Output Frequencies, Startup Time, and LOS Timing

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
f_{OP}	Operating Frequency	Automatic Clock Parking (ACP) Circuit disabled	0.00001	-	400	MHz
		Automatic Clock Parking (ACP) Circuit enabled	25	-	400	
$t_{STARTUP}$	Start-up Time	[1]	-	0.55	1.6	ms
$t_{STARTUP}$	Start-up Time	[2]	-	70	87	ns
t_{LATOEb}	OEb latency	OEb assertion/de-assertion CLK start/stop latency. Input clock must be running.	4	5	6	clks
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of input clock to LOS assert. [3][4]	-	240	300	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of input clock to LOS de-assert. [3][5]	-	6	7	clks

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PWRDNb tied to VDD in this case.
2. VDD stable, measured from de-assertion of PWRGD_PWRDNb.
3. The clock detect circuit does not qualify the accuracy of the input clock. The first input clock must appear to release the power on reset and enable the LOS circuit at power up.
4. PWRGD_PWRDNb high. The Automatic Clock Parking (ACP) circuit - if enabled - will park the outputs in a low/low state within this time. See Byte4, bit 4, LOSb_ACP_ENABLE.
5. PWRGD_PWRDNb high. The device will drive the outputs to a high/low state within this time and then begin clocking the outputs.

2.3.3 CLK AC/DC Output Characteristics

Table 13. 85Ω CLK AC/DC Characteristics – Source-Terminated 100MHz PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1066	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-216	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	703	832	960	-	mV
V_{LOW}	Voltage Low [3]		-200	-87	26	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 800mV, scope averaging off.	349	417	486	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		21	26	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	1.9	2.9	3.9	1.8 to 4	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	1.6	2.5	3.4	1.5 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	2	13	20	%
		V_{HIGH} set to 800mV. Slow slew rate.	-	3	11	20	%
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	774	913	1052	-	mV
V_{LOW}	Voltage Low [3]		-215	-94	28	-	
V_{CROSS}	Crossing Voltage (abs) [3] [6][7]	V_{HIGH} set to 900mV, scope averaging off.	371	449	526	300 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3] [6][8]		20	26	31	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.	2.0	3.1	4.1	1.9 to 4.2	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.	1.6	2.6	3.6	1.5 to 3.7	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	2	12	20	%
		V_{HIGH} set to 900mV. Slow slew rate.	-	4	15	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49	50.1	51	45 to 55	%

1. Standard high impedance load with C_L= 2pF. For more information, see Figure 9, ZOUTSEL_tri = 0.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 14. 100Ω CLK AC/DC Characteristics – Source-Terminated 100MHz PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1075	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-170	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	811	868	926	-	mV
V_{LOW}	Voltage Low [3]		-140	-102	-64	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 800mV, scope averaging off.	346	445	543	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		21	25	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.	2.4	3.3	4.2	2.3 to 4.3	V/ns
		V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.	1.8	2.6	3.4	1.7 to 3.5	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV. Fast slew rate.	-	8	18.6	20	%
		V_{HIGH} set to 800mV. Slow slew rate.	-	14	19.7		
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	896	963	1030	-	mV
V_{LOW}	Voltage Low [3]		-183	-	-	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 900mV, scope averaging off.	388	486	584	300 to 600	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		21	25	30	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.	2.5	3.5	4.5	2.4 to 4.6	V/ns
		V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.	1.9	2.7	3.6	1.8 to 3.7	
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV. Fast slew rate.	-	8	17.8	20	%
		V_{HIGH} set to 900mV. Slow slew rate.	-	12	19.5		
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49	50.0	51	45 to 55	%

1. Standard high impedance load with C_L= 2pF. For more information, see Figure 9, ZOUTSEL_tri = 1.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 15. 85ohm CLK AC/DC Characteristics – Source-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	645	808	989	mV
V_{OL}	Output Low Voltage [2]		-220	-39	39	
V_{CROSS}	Crossing Voltage (abs) [3]		275	376	471	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	32	
t_R	Rise Time [2] VT = 20% to 80% of swing		290	425	601	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		271	418	623	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	739	867	1094	mV
V_{OL}	Output Low Voltage [2]		-236	-41	43	
V_{CROSS}	Crossing Voltage (abs) [3]		285	391	475	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	31	
t_R	Rise Time [2] VT = 20% to 80% of swing		308	518	729	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		311	468	625	
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48	50	52	%

1. Standard high impedance load with C_L= 2pF. For more information, see Figure 9, ZOUTSEL_tri = 0.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 16. 85ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	382	410	436	mV
V_{OL}	Output Low Voltage [2]		-8	13	33	
V_{CROSS}	Crossing Voltage (abs) [3]		186	207	226	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-9	8	25	
t_R	Rise Time [2] VT = 20% to 80% of swing		256	369	491	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		225	308	417	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	415	449	480	mV
V_{OL}	Output Low Voltage [2]		-6	14	35	
V_{CROSS}	Crossing Voltage (abs) [3]		192	216	239	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-9	8	27	
t_R	Rise Time [2] VT = 20% to 80% of swing		289	419	558	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		227	303	406	
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	49	50	51	%

1. Both Tx and Rx are terminated (double-terminated) with C_L= 2pF. This reduces amplitude by 50%. For more information, see Figure 10, ZOUTSEL_tri = 0.

2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 17. 100ohm CLK AC/DC Characteristics – Source-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	636	833	958	mV
V_{OL}	Output Low Voltage [2]		-165	-49	49	
V_{CROSS}	Crossing Voltage (abs) [3]		285	420	571	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	32	
t_R	Rise Time [2] VT = 20% to 80% of swing		285	390	494	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		279	419	593	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz. (Slow slew rate is not recommended for frequencies > 100MHz)	732	902	1070	mV
V_{OL}	Output Low Voltage [2]		-183	-52	52	
V_{CROSS}	Crossing Voltage (abs) [3]		325	449	598	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		21	26	33	
t_R	Rise Time [2] VT = 20% to 80% of swing		383	487	592	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		334	457	579	
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48	50	52	%

1. Standard high impedance load with C_L= 2pF. For more information, see Figure 9, ZOUTSEL_tri = 1.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 18. 100ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz)	399	428	456	mV
V_{OL}	Output Low Voltage [2]		-7	13	34	
V_{CROSS}	Crossing Voltage (abs) [3]		200	228	256	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-12	8	30	
t_R	Rise Time [2] VT = 20% to 80% of swing		196	273	358	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		214	294	388	

Table 18. 100ohm CLK AC/DC Characteristics – Double-Terminated, Non-PCIe Applications [1] (Cont.)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	438	475	510	mV
V_{OL}	Output Low Voltage [2]		-7	14	36	
V_{CROSS}	Crossing Voltage (abs) [3]		218	247	276	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-13	8	31	
t_R	Rise Time [2] VT = 20% to 80% of swing		203	301	408	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		207	279	369	
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	49	50	51	%

1. Both Tx and Rx are terminated (double-terminated) with C_L= 2pF. This reduces amplitude by 50%. For more information, see Figure 10, ZOUTSEL_tri = 1.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 19. 34ohm CLK AC/DC Characteristics - Rx-Terminated, Non-PCIe Applications [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies > 100MHz)	554	602	650	mV
V_{OL}	Output Low Voltage [2]		-3	19	40	
V_{CROSS}	Crossing Voltage (abs) [3]		281	317	352	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-21	11	42	
t_R	Rise Time [2] VT = 20% to 80% of swing		130	267	404	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		133	317	500	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate, 156.25MHz, 312.5MHz - amplitude is reduced by ~50% due to double termination. (Slow slew rate is not recommended for frequencies >100MHz)	564	630	695	mV
V_{OL}	Output Low Voltage [2]		-3	19	40	
V_{CROSS}	Crossing Voltage (abs) [3]		290	331	372	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-22	11	45	
t_R	Rise Time [2] VT = 20% to 80% of swing		122	263	404	ps
t_F	Fall Time [2] VT = 20% to 80% of swing		124	312	501	
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	48	49.5	51	%

1. ZOUTSEL_tri = M. This setting turns off the source termination, provided approximately 75% of the source-terminated amplitude at the receiver with C_L= 2pF. For more information, see Figure 10,
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

2.3.4 CLKIN AC/DC Characteristics

Table 20. CLKIN AC/DC Characteristics

Symbol	Parameter	Condition	Minimum [1]	Typical	Maximum	Unit
V_{IHMAX}	Maximum Input Voltage	Single-ended value.	-	-	1.2	V
V_{CROSS}	Input Crossover Voltage	Lo/Lo Detect Disabled.	100	-	-	mV
		Lo/Lo Detect Enabled.	131	-	-	mV
V_{SWING}	Input Swing	Differential value. Lo/Lo Detect Disabled.	200	-	-	mV
		Differential value. Lo/Lo Detect Enabled.	528	-	-	mV
dv/dt	Input Slew Rate	Measured differentially. [2] Lo/Lo Detect Disabled.	0.6	-	-	V/ns

1. For values required for performance, see the Phase Jitter tables.
2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

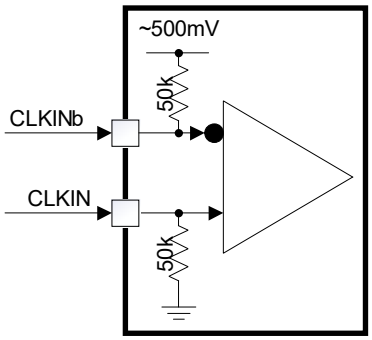


Figure 7. Clock Input Bias Network

2.3.5 Output-to-Output and Input-to-Output Skew

Table 21. Output-to-Output and Input-to-Output Skew [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2]	Any two outputs, all outputs at fast slew rate.	-	36	50	ps
		Any two outputs, all outputs at slow slew rate.	-	32	60	ps
t_{PD}	Input-to-Output Delay [3]	Clock in to any output, all outputs at fast slew rate.	0.8	1.0	1.2	ns
		Clock in to any output, all outputs at slow slew rate.	1.0	1.3	1.5	ns
Δt_{PD}	Input-to-Output Delay Variation [3]	A single device, over temperature and voltage.	-	0.9	1.0	ps/°C

1. These parameters are measured with the loads in Figure 10.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Defined as the time between to output rising edge and the input rising edge that caused it.

2.3.6 I/O Electrical Characteristics

Table 22. I/O Electrical Characteristics

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [1][2]	Single-ended inputs, unless otherwise listed.	0.65 × VDD	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [1][2]		-0.3	-	0.35 × VDD	V
V_{IH}	Input High Voltage	SADR_tri[1:0].	0.75 × VDD	-	VDD + 0.3	V
V_{IM}	Input Mid Voltage		0.45 × VDD	0.5 × VDD	0.55 × VDD	V
V_{IL}	Input Low Voltage		-0.3	-	0.25 × VDD	V
V_{OL}	Output Low Voltage	LOSb, I_{OL} = 2mA.	-	0.1	0.4	V
I_{IH}	Input Leakage Current High, V_{IN} = VDD	CLKIN	5	-	15	µA
		CLKINb	-3	-	+3	
		PWRGD_PWRDNb	-35	-	-20	
		SADR_tri[1:0]	25	-	35	
		Single-ended inputs not otherwise listed	25	-	35	
I_{IL}	Input Leakage Current Low, V_{IN} = 0V	CLKIN	-3	-	+3	µA
		CLKINb	-12	-	-6	
		PWRGD_PWRDNb	-35	-	-20	
		SADR_tri[1:0]	-35	-	-20	
		Single-ended inputs not otherwise listed	-35	-	-20	
Rp	PD_CLKIN	Value of internal pull-down resistor to ground (CLKIN)	-	53	-	kΩ
	PU_CLKINb	Value of internal pull-up resistor to 0.5V (CLKINb).	-	57	-	
	Pull-up/Pull-down Resistor	Single-ended inputs.	-	125	-	
Zo	Output Impedance	CLK/CLKb single-ended impedance, 85Ω setting	-	34	-	Ω
		CLK/CLKb single-ended impedance, 100Ω setting	-	39	-	
		CLK/CLKb single-ended impedance, 33Ω setting	-	14	-	

1. For SCLK and SDATA, see the SMBus DC Electrical Characteristics table.
2. These values are compliant with JESD8-7A 1.8V Normal Range.

2.3.7 Power Supply Current

Table 23. Power Supply Current [1][2][3]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{DDCLK}	V_{DDCLK} Operating Current – RC19108, 85Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	76	79	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	88	89	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	95	100	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	115	121	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19104, 85Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	45	47	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	51	52	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	51	60	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	58	71	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19102, 85Ω impedance	Fast slew rate, source-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	30	30	mA
		Fast slew rate, double-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	33	33	
		Fast slew rate, source-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	39	41	
		Fast slew rate, double-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	44	46	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19108, 100Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	73	79	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	88	98	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	100	105	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	116	120	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19104, 100Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	44	47	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	53	59	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	53	63	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	60	71	

Table 23. Power Supply Current [1][2][3] (Cont.)

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
I_{DDCLK}	V_{DDCLK} Operating Current – RC19102, 100Ω impedance	Fast slew rate, source-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	29	31	mA
		Fast slew rate, double-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	33	37	
		Fast slew rate, source-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	40	42	
		Fast slew rate, double-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	43	48	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19108, 34Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	83	96	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	97	111	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	144	170	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	164	192	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19104, 34Ω impedance	Fast slew rate, source-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	38	53	mA
		Fast slew rate, double-terminated load at 100MHz. PWRGD_PWRDNb = 1.	-	59	64	
		Fast slew rate, source-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	74	93	
		Fast slew rate, double-terminated load at maximum output frequency. PWRGD_PWRDNb = 1.	-	97	103	
I_{DDCLK}	V_{DDCLK} Operating Current – RC19102, 34Ω impedance	Fast slew rate, source-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	35	35	mA
		Fast slew rate, double-terminated load at 100MHz. (RC19102 is always powered up when VDD is applied.)	-	41	39	
		Fast slew rate, source-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	61	59	
		Fast slew rate, double-terminated load at maximum output frequency. (RC19102 is always powered up when VDD is applied.)	-	70	63	
I_{DDDIG}	V_{DDDIG} Operating Current	PWRGD_PWRDNb = 1.	-	0.14	0.3	mA
I_{DDCLK_PD}	V_{DDCLK} Power-down Current	PWRGD_PWRDNb = 0.	-	3.7	5	mA
I_{DDDIG_PD}	V_{DDDIG} Power-down Current	PWRGD_PWRDNb = 0.	-	0.14	0.3	mA

1. For more information, see Test Loads.
2. Output voltage set to 800mV. Slew rate has negligible effect on current consumption, so only fast is listed.
3. Total operating current is obtained by adding IDDCLK + IDDDIG. Power down current is obtained by adding IDDCLK_PD + IDDDIG_PD.

2.3.8 SMBus Electrical Characteristics

This section applies to all devices except the RC19102 because the RC19102 does not have an SMBus interface.

Table 24. SMBus DC Electrical Characteristics [1]

Symbol	Parameter	Condition	Minimum	Typical	Maximum	Unit
V_{IH}	High-level Input Voltage for SMBCLK and SMBDAT	VDD = 1.8V	0.8 VDD	-	3.4	V
V_{IL}	Low-level Input Voltage for SMBCLK and SMBDAT	VDD = 1.8V	-	-	0.3 VDD	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	-	0.05 VDD	-	-	
V_{OL}	Low-level Output Voltage for SMBCLK and SMBDAT	I_{OL} = 4mA	-	0.28	0.4	
I_{IN}	Input Leakage Current per Pin	-	[2]	-	[2]	µA
C_B	Capacitive Load for Each Bus Line	-	-	-	400	pF

1. V_{OH} is governed by the V_{PUP}, the voltage rail to which the pull-up resistors are connected. The maximum V_{PUP} voltage is 3.6V.
2. See I/O Electrical Characteristics.

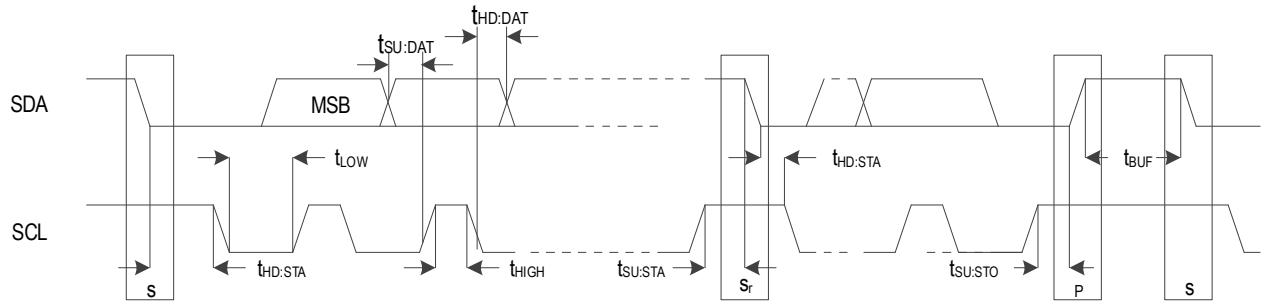


Figure 8. SMBus Target Timing Diagram

Table 25. SMBus AC Electrical Characteristics

Symbol	Parameter	Condition	100kHz Class		Unit
			Minimum	Maximum	
f_{SMB}	SMBus Operating Frequency	[1]	10	100	kHz
t_{BUF}	Bus free time between STOP and START Condition	-	4.7	-	µs
$t_{HD:STA}$	Hold Time after (REPEATED) START Condition	[2]	4	-	µs
$t_{SU:STA}$	REPEATED START Condition Setup Time	-	4.7	-	µs
$t_{SU:STO}$	STOP Condition Setup Time	-	4	-	µs
$t_{HD:DAT}$	Data Hold Time	[3]	300	-	ns
$t_{SU:DAT}$	Data Setup Time	-	250	-	ns
$t_{TIMEOUT}$	Detect SCL_SCLK Low Timeout	[4]	25	35	ms
$t_{TIMEOUT}$	Detect SDA_nCS Low Timeout	[5]	25	35	ms
t_{LOW}	Clock Low Period	-	4.7	-	µs
t_{HIGH}	Clock High Period	[6]	4	50	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time - Target (Slave)	[7]	N/A		ms
$t_{LOW:MEXT}$	Cumulative Clock Low Extend Time - Host (Master)	[8]	N/A		ms
t_F	Clock/Data Fall Time	[9]	-	300	ns
t_R	Clock/Data Rise Time	[9]	-	1000	ns
t_{SPIKE}	Noise Spike Suppression Time	[10]	-	-	ns

1. Power must be applied and PWRGD_PWRDNb must be a 1 for the SMBus to be active.

2. A host (master) should not drive the clock at a frequency below the minimum f_{SMB}. Further, the operating clock frequency should not be reduced below the minimum value of fSMB due to periodic clock extending by target devices as defined in Section 5.3.3 of System Management Bus (SMBus) Specification, Version 3.1, dated 19 Mar 2018. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:\ SEXT}$ and $t_{LOW:\ MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} - t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100 µs in a non-periodic way.
3. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the VIH,MIN of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
4. Target devices may have caused other target devices to hold SDA low. This is the maximum time that a device can hold SMBDAT low after the host raises SMBCLK after the last bit of a transaction. A target device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the host in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can host the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SMBDATA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for hosts to detect bus idle conditions. A host can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. tLOW:MEXT is the cumulative time a host device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a target device or another host will also extend the clock causing the combined clock low time to be greater than tLOW:MEXT on a given byte. This parameter is measured with a full-speed target device as the sole target of the host.
9. The rise and fall time measurement limits are defined as follows:
   Rise Time Limits: $(V_{IL:MAX} - 0.15\ V)$ to $(V_{IH:MIN} + 0.15\ V)$
   Fall Time Limits: $(V_{IH:MIN} + 0.15\ V)$ to $(V_{IL:MAX} - 0.15\ V)$
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

3. Test Loads

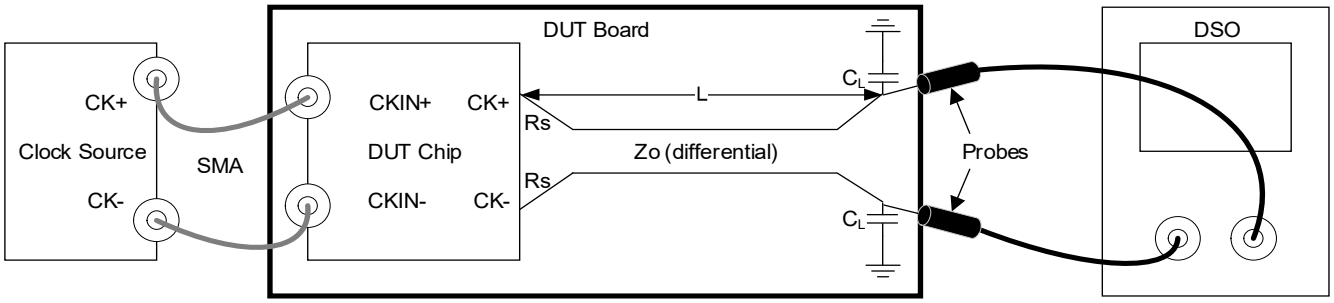


Figure 9. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

Table 26. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)

Clock Source	L (cm)	C_L (pF)	ZOUTSEL_tri Pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	2	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (33 ohms)	85	External 25.5
				100	External 33.3

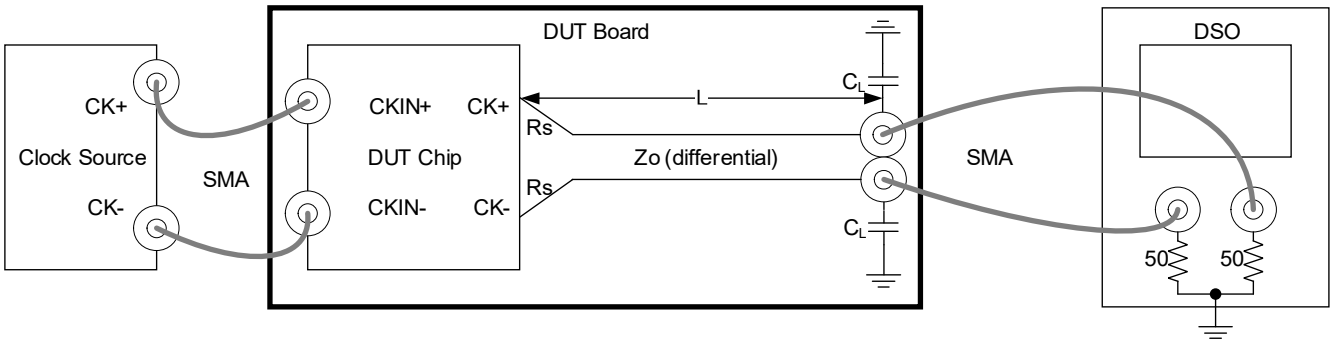


Figure 10. AC/DC Test Load for Differential Outputs (Double-Terminated or Receiver-Terminated)

Table 27. Parameters for AC/DC Test Load (Double-Terminated)

Clock Source	L (cm)	C_L (pF)	ZOUTSEL_tri Pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	2	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (33 ohms)	85	None[1]
				100	

1. This setting is designed to provide additional amplitude for receiver-terminated loads by turning off the source termination in the output driver. There is no reflection with receiver terminated loads since the receiver termination absorbs the incident waveform.

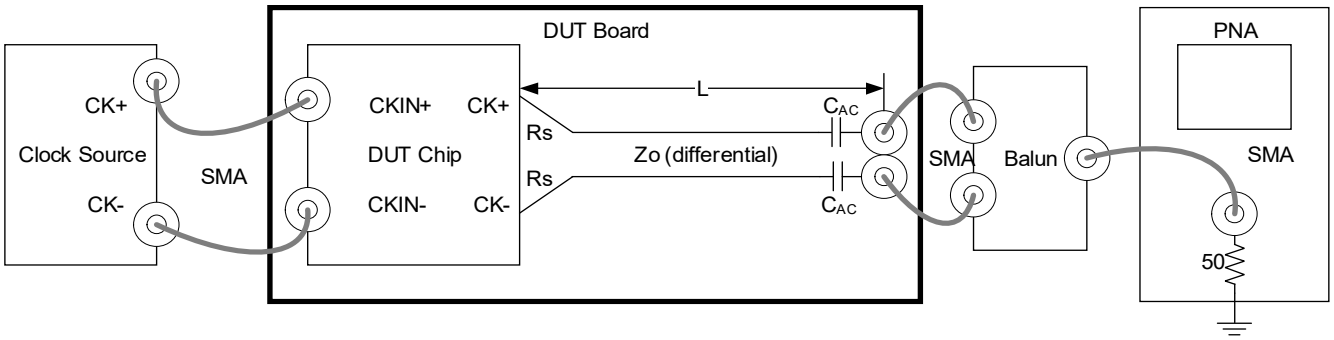


Figure 11. Test Load for PCIe Phase Jitter Measurements

Table 28. Parameters for PCIe Phase Jitter Measurements

Clock Source	L (cm) [1]	C_{AC} (uF)	ZOUTSEL_tri Pin	Zo (ohms)	Rs (ohms)
SMA100B	25.4	0.1	0 (85 ohms)	85	Internal
			1 (100 ohms)	100	Internal
			Mid (33 ohms)		None

1. PCIe Gen6 specifies L = 0cm for 32 and 64 GT/s. L = 25.4cm is more conservative.

4. General SMBus Serial Interface Information

This section applies to all device except the RC19102 which does not have an SMBus interface.

4.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas (Target/Receiver)**
T	starT bit		
Target Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

4.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas (Target/Receiver)**
T	starT bit		
Target Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Target Address			
RD	ReaD		
			ACK
			Data Byte Count = X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not acknowledge		
P	stoP bit		

4.3 SMBus Bit Types

Bit Description	Definition
RO	Read-only
RW	Read-write
RW1C	Read/Write ‘1’ to clear
RESERVED	Undefined do not write

4.4 Write Lock Functionality

WRITE_LOCK	WRITE_LOCK RW1C	SMBus Write Protect
0	0	No
0	1	Yes
1	0	Yes
1	1	Yes

4.5 SMBus Address Decode

Address Selection		Binary Value								Hex Value
SADR_tri1	SADR_tri0	7	6	5	4	3	2	1	Rd/Wrt	
0	0	1	1	0	1	0	1	1	0	D6
	M	1	1	0	1	1	0	0	0	D8
	1	1	1	0	1	1	0	1	0	DA
M	0	1	1	0	0	0	1	1	0	C6
	M	1	1	0	0	1	0	0	0	C8
	1	1	1	0	0	1	0	1	0	CA
1	0	1	1	0	0	0	1	1	0	A6
	M	1	1	0	0	1	0	0	0	A8
	1	1	1	0	0	1	0	1	0	AA

4.6 SMBus Registers

Table 29. Register Index

Offset (Hex)	Register Module Base Address: 0x0	
	Register Name	Register Description
0x0	OUTPUT_ENABLE	Output Enable Register
0x2	OEB_PIN_READBACK	OEb Pin Readback Register
0x4	LOS_CONFIG	Loss of Signal and Async Mode Configuration Register
0x5	VENDOR_REVISION_ID	Vendor ID, Revision ID Register
0x6	DEVICE_ID	Device ID Register
0x7	BYTE_COUNT	Number of Bytes Returned on an SMBus Block Read
0xA	SLEW_AMP_SELECT	Multifunction Pin Configuration Register
0xE	INPUT_PULLUP_PULLDOWN_4	Internal Pull-up / Pull-down Configuration Register
0x10	AMP_CTRL_ALT	Alternate Amplitude Selection Register
0x11	AMP_CTRL_DEF	Default Amplitude Selection Register
0x12	PD_RESTORE_LOSb_CONFIG	Configuration and Status Register
0x14	OUTPUT_IMPEDANCE_7_0	Output Impedance Select Register 0
0x15	OUTPUT_REC_SEL_7_0	Output Impedance Select Register 1
0x16	OUTPUT_SLEW_RATE_7_0	Output Slewrate Select Register
0x20	LOW-LOW_DETECT	CLKIN Low-Low Detect Enable Register
0x23	RECEIVER_CONTROL	CLKIN Configuration Register
0x26	WRITE_LOCK	Non-Clearable Write Lock Register
0x27	WRITE_LOCK_LOS_EVT	Clearable Write Lock and LOS Event Sticky Register

4.6.1 OUTPUT_ENABLE

Output Enable Register.

OUTPUT_ENABLE Bit Field Descriptions				
Bit Field	Field Name	Field Type	Default Value	Description
7	clk7_en	RW	0x1	CLK7 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
6	clk6_en	RW	0x1	CLK6 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
5	clk5_en	RW	0x1	CLK5 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
4	clk4_en	RW	0x1	CLK4 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
3	clk3_en	RW	0x1	CLK3 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
2	clk2_en	RW	0x1	CLK2 enable. 0 = Output is disabled (low/low) 1 = Output is enabled

OUTPUT_ENABLE Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
1	clk1_en	RW	0x1	CLK1 enable. 0 = Output is disabled (low/low) 1 = Output is enabled
0	clk0_en	RW	0x1	CLK0 enable. 0 = Output is disabled (low/low) 1 = Output is enabled

4.6.2 OEB_PIN_READBACK

OEb Pin Readback Register.

OEB_PIN_READBACK Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	rb_oeb7	RO	0x1	State of OEb7 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
6	rb_oeb6	RO	0x1	State of OEb6 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
5	rb_oeb5	RO	0x1	State of OEb5 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
4	rb_oeb4	RO	0x1	State of OEb4 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
3	rb_oeb3	RO	0x1	State of OEb3 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
2	rb_oeb2	RO	0x1	State of OEb2 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
1	rb_oeb1	RO	0x1	State of OEb1 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high
0	rb_oeb0	RO	0x1	State of OEb0 pin. The default pin state is 1 if not driven to a 0. 0 = Pin low 1 = Pin high

4.6.3 LOS_CONFIG

Loss of Signal and Async Mode Configuration Register.

LOS_CONFIG Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	reserved	RW	0x0	Reserved
6	losb_rw1c_en	RW	0x1	LOS sticky bit enable. Enables the LOS sticky bit (B0x27[1]). This bit must be set to 1 if B0x4[2] is set to 0. 0 = Disable 1 = Enable
5	reserved	RW	0x0	Reserved

LOS_CONFIG Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
4	losb_acp_en	RW	0x1	Automatic clock parking enable. Enables Automatic Clock Parking of outputs to a low/low state when LOS condition occurs. 0 = Disable 1 = Enable
3	reserved	RW	0x0	Reserved
2	losb_config	RW	0x1	Configure LOSb pin operating mode. Determines if the LOSb pin is a real-time or sticky. If sticky, the LOSb pin is driven by the LOSb RW1C sticky bit. 1 = LOSb real-time 0 = LOSb from RW1C sticky bit
1:0	reserved	RW	0x0	Reserved

4.6.4 VENDOR_REVISION_ID

Vendor ID, Revision ID Register.

VENDOR_REVISION_ID Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	rid	RO	0x0	REVISION ID. Silicon Revision. 0x0 = A revision
3:0	vid	RO	0x1	VENDOR ID. Vendor ID. 0x1 = Renesas

4.6.5 DEVICE_ID

Device ID Register.

DEVICE_ID Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:0	device_id	RO	0x18	RC19108 device ID listed as default. 0x18 = RC19108 0x14 = RC19104

4.6.6 BYTE_COUNT

Number of Bytes Returned on an SMBus Block Read.

BYTE_COUNT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:5	reserved	RW	0x0	Reserved
4:0	byte_count	RW	0x7	Writing to this register configures how many bytes will be returned on an SMBus block read.

4.6.7 SLEW_AMP_SELECT

Multifunction Pin Configuration Register.

SLEW_AMP_SELECT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	slew_amp_sel	RW	0x0	Multi-function pin selection. The pin is defined as either Slew Rate Select or Amplitude Select. If Amplitude Select is chosen, refer to registers 0x10 and 0x11. 0 = Pin is Slew Rate Select pin (RC191xxA) 1 = Pin is Amplitude Select pin (RC191xxA001)
6:0	reserved	RW	0x0	Reserved

4.6.8 INPUT_PULLUP_PULLDOWN_4

Internal Pull-up / Pull-down Configuration Register.

INPUT_PULLUP_PULLDOWN_4 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	reserved	RW	0x8	Reserved
3	sdata_pullup	RW	0x0	Enable/disable internal pull-up. The default pin state is high when the internal pull-up is enabled. If the SMBus is not used, this bit may be set to hold the SDATA pin in an inactive state. It should not be set if the SMBus is used in the system. 0 = Disable internal pull-up 1 = Enable internal pull-up
2	reserved	RW	0x0	Reserved
1	sclk_pullup	RW	0x0	Enable/disable internal pull-up. The default pin state is high when the internal pull-up is enabled. If the SMBus is not used, this bit may be set to hold the SDATA pin in an inactive state. It should not be set if the SMBus is used in the system. 0 = Disable internal pull-up 1 = Enable internal pull-up
0	reserved	RW	0x0	Reserved

4.6.9 AMP_CTRL_ALT

Alternate Amplitude Selection Register.

AMP_CTRL_ALT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	amp_cntrl_alt	RW	0xB	Alternate amplitude control. When the multifunction pin is configured as Amplitude Select, this field defines the single-ended output amplitude when the pin = 1. When the multifunction pin is configured as Slew Rate Selection, this field has no impact. 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV
amp_cntrl_alt (continued)				0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV
3:0	reserved	RW	0x0	Reserved

4.6.10 AMP_CTRL_DEF

Default Amplitude Selection Register.

AMP_CTRL_DEF Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:4	amp_cntrl_def	RW	0x7	Default amplitude control. When the multifunction pin is configured as Slewrate Select, or when the pin is configured as Amplitude Select and the pin = 0, this field defines the single-ended output amplitude. 0x0 = 625mV 0x1 = 650mV 0x2 = 675mV 0x3 = 700mV 0x4 = 725mV 0x5 = 750mV 0x6 = 775mV 0x7 = 800mV 0x8 = 825mV 0x9 = 850mV
amp_cntrl_def (continued)				0xA = 875mV 0xB = 900mV 0xC = 925mV 0xD = 950mV 0xE = 975mV 0xF = 1000mV
3:0	reserved	RW	0x0	Reserved

4.6.11 PD_RESTORE_LOSb_CONFIG

Configuration and Status Register.

PD_RESTORE_LOSb_CONFIG Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:5	reserved	RW	0x0	Reserved
4	ck_acquire_rb	RO	0x0	Clock acquired readback. This bit indicates if a clock was ever detected (LOSb de-asserted) for the current power cycle. 0 = Clock never acquired 1 = Clock acquired at least once before
3	pd_restoreb	RW	0x1	Save configuration in power-down. This bit determines the behavior of the device when the PWRGD_PWRDNb pin is asserted low. This bit is automatically returned to 1 after PWRGD_PWRDNb is toggled 1-0-1 with the bit set to 0. 0 = Config Cleared 1 = Config Saved
2	sdata_time_out_en	RW	0x1	Enable SMB time out monitoring SDATA. This bit enables a timeout for the SMBus data path. This timeout monitor is in addition to the mandatory SCLK timeout monitor. These monitors release a hung SMBus. 0 = Disable SDATA time out 1 = Enable SDATA time out
1	reserved	RO	0x0	Reserved
0	losb_rb	RO	0x0	Real-time read back of input clock detect. This bit provides a real-time status of the clock input. The default value assumes no input clock present. 0 = LOS event detected (no CLKIN detected) 1 = No LOS event detected (CLKIN detected)

4.6.12 OUTPUT_IMPEDANCE_7_0

Output Impedance Select Register 0.

OUTPUT_IMPEDANCE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_impedance0	RW	0x0	CLK7 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[7] are set to 0. ZOUTSEL_tri = M: this bit is set to 0 and B0x15[7] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[7] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
6	clk6_impedance0	RW	0x0	CLK6 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[6] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[6] is set to 1. ZOUTSEL_tri = 1: this bit is set to 1 and B0x15[6] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
5	clk5_impedance0	RW	0x0	CLK5 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[5] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[5] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[5] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
4	clk4_impedance0	RW	0x0	CLK4 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[4] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[4] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[4] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended

OUTPUT_IMPEDANCE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
3	clk3_impedance0	RW	0x0	CLK3 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[3] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[3] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[3] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
2	clk2_impedance0	RW	0x0	CLK2 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[2] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[2] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[2] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
1	clk1_impedance0	RW	0x0	CLK1 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[1] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[1] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[1] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended
0	clk0_impedance0	RW	0x0	CLK0 impedance select bit 0. ZOUTSEL_tri = 0: this bit and B0x15[0] are set to 0. ZOUTSEL_tri = M: this bit is set to 0, ignored, and B0x15[0] is set to 1. ZOUTSEL_tri= 1: this bit is set to 1 and B0x15[0] is set to 0. 0 = 85 ohm differential, 42.5 ohm single-ended 1 = 100 ohm differential, 50 ohm single-ended

4.6.13 OUTPUT_REC_SEL_7_0

Output Impedance Select Register 1.

OUTPUT_REC_SEL_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_impedance1	RW	0x1	CLK7 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[7]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[7] is set to 0 and ignored. 0 = See B0x14[7] 1 = 33 ohm differential, 17 ohm single-ended
6	clk6_impedance1	RW	0x1	CLK6 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[6]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[6] is set to 0 and ignored. 0 = See B0x14[6] 1 = 33 ohm differential, 17 ohm single-ended
5	clk5_impedance1	RW	0x1	CLK5 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[5]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[5] is set to 0 and ignored. 0 = See B0x14[5] 1 = 33 ohm differential, 17 ohm single-ended
4	clk4_impedance1	RW	0x1	CLK4 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[4]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[4] is set to 0 and ignored. 0 = See B0x14[4] 1 = 33 ohm differential, 17 ohm single-ended

OUTPUT_REC_SEL_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
3	clk3_impedance1	RW	0x1	CLK3 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[3]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[3] is set to 0 and ignored. 0 = See B0x14[3] 1 = 33 ohm differential, 17 ohm single-ended
2	clk2_impedance1	RW	0x1	CLK2 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[2]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[2] is set to 0 and ignored. 0 = See B0x14[2] 1 = 33 ohm differential, 17 ohm single-ended
1	clk1_impedance1	RW	0x1	CLK1 impedance select bit 1. ZOUTSEL_tri = 0 or 1: this bit is set to 0 at power up and the appropriate value is set in B0x14[1]. ZOUTSEL_tri = M: this bit is set to 1 at power up, B0x14[1] is set to 0 and ignored. 0 = See B0x14[1] 1 = 33 ohm differential, 17 ohm single-ended
0	clk0_impedance1	RW	0x1	CLK0 impedance select bit 1. ZOUTSEL_tri = 0 or 1: This bit is set to 0 at power up and the appropriate value is set in B0x14[0]. ZOUTSEL_tri = M: This bit is set to 1 at power up, B0x14[0] is set to 0 and ignored. 0 = See B0x14[0] 1 = 33 ohm differential, 17 ohm single-ended

4.6.14 OUTPUT_SLEW_RATE_7_0

Output Slewrate Select Register.

OUTPUT_SLEW_RATE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7	clk7_slewrate	RW	0x1	CLK7 slew rate select. If B0xA[7] = 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7] = 1 at startup, default = 1 0 = Slow slew rate 1 = Fast slew rate
6	clk6_slewrate	RW	0x1	CLK6 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
5	clk5_slewrate	RW	0x1	CLK5 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
4	clk4_slewrate	RW	0x1	CLK4 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
3	clk3_slewrate	RW	0x1	CLK3 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate

OUTPUT_SLEW_RATE_7_0 Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
2	clk2_slewrate	RW	0x1	CLK2 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
1	clk1_slewrate	RW	0x1	CLK1 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate
0	clk0_slewrate	RW	0x1	CLK0 slew rate select. If B0xA[7]= 0 at power up, the SLEWRATE_SEL pin sets the default. After power up, the value can be changed via SMBus. If B0xA[7]= 1 at startup, default=1 0 = Slow slew rate 1 = Fast slew rate

4.6.15 LOW-LOW_DETECT

CLKIN Low-Low Detect Enable Register.

LOW-LOW_DETECT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:3	reserved	RW	0x12	Reserved
2	low_low_det_enable	RW	0x1	Enable low-low detect circuit on CLKIN. Allows the device to detect a low-low condition on CLKIN and turn off the receiver. (Low-low is not a valid differential state). 0 = Disable 1 = Enable
1:0	reserved	RW	0x0	Reserved

4.6.16 RECEIVER_CONTROL

CLKIN Configuration Register.

RECEIVER_CONTROL Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:2	reserved	RW	0x0	Reserved
1	ac_in	RW	0x0	AC-couple CLKIN. When AC-coupling CLKIN, set this bit to enable internal bias circuitry on the CLKIN. This eliminates the need for external bias components on the CLKIN side of the AC-coupling capacitor. 0 = Disable internal bias (DC-coupled) 1 = Enable internal bias (AC-coupled)
0	rx_term	RW	0x0	Enable internal termination for CLKIN. Applications requiring receiver terminations may set this bit to enable termination resistors to ground on both the CLKIN and CLKINb pins. PCIe applications generally require Rx_TERM to be 0. 0 = Disable internal termination (PCIe) 1 = Enable internal termination

4.6.17 WRITE_LOCK

Non-Clearable Write Lock Register.

WRITE_LOCK Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:1	reserved	RW	0x0	Reserved
0	write_lock	RW	0x0	Non-clearable SMBus write lock bit. When written to one, the SMBus registers cannot be written. They may be read. This bit can only be cleared by cycling power. 0 = SMBus writes are not prohibited by WRITE_LOCK 1 = SMBus locked for writing

4.6.18 WRITE_LOCK_LOS_EVT

Clearable Write Lock and LOS Event Sticky Register.

WRITE_LOCK_LOS_EVT Bit Field Descriptions				
Bit Field	**Field Name**	**Field Type**	**Default Value**	**Description**
7:2	reserved	RW1C	0x0	Reserved
1	los_evt_rw1c	RW1C	0x0	LOS event sticky bit. A 1 indicates that an LOS event occurred. The bit can be cleared by writing a 1. 0 = No LOS event detected 1 = LOS event detected.
0	write_lock_rw1c	RW1C	0x0	Clearable SMBus write lock bit. When written to one, the SMBus control registers cannot be written. They may be read. This bit may be cleared by writing a 1 to it. 0 = SMBus writes are not prohibited by WRITE_LOCK_RW1C 1 = SMBus locked for writing

5. Applications Information

5.1 Inputs, Outputs, and Output Enable Control

The CLKIN/CLKINb inputs of the RC191xx devices have an internal bias network that prevents self-oscillation from floating input clock condition.

5.1.1 Recommendations for Unused Inputs and Outputs

5.1.1.1 Unused Single-ended Control Inputs

The single-ended control pins have internal pull-up and/or internal pull-down resistors and do not require external resistors. They can be left floating if the default pin state is the desired state. If external resistors are needed to change the pin state or are desired for design robustness, 10kohm is the recommended value.

5.1.1.2 Unused Differential CLK Outputs

All unused CLK outputs can be left floating. Renesas recommends that no trace be attached to unused CLK outputs. While not required (but highly recommended), the best design practice is to disable unused CLK outputs. This is easily accomplished with the dedicated OEb pin for each output.

5.1.1.3 Unused SMBus Clock and Data Pins

If the SMBus interface is not used, the clock and data pins must be pulled high with an external resistor. The two pins can share a resistor if there is no possibility of using the SMBus interface for debug purposes. If the interface might be used for debug, separate resistors must be used. 10kohm is the recommended value. The SMBus pins are 3.3V tolerant and may be used with a 3.3V pull-up voltage.

5.1.2 Differential CLKIN Configurations

The RC191xx clock input buffer supports four configurations:

- Direct connection to HCSL-level clocks
- AC-coupled connection to LVDS-level clocks with *external* termination resistor
- Internal self-bias circuit for applications that *externally* AC-couple the input clock
  This feature is enabled by the **AC_IN** bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  This feature is enabled by the **Rx_TERM** bit.

Devices with multiple input clocks have individual AC_IN and Rx_TERM configuration bits for each input. The internal input clock terminations prevent reflections and are useful for non-PCIe applications, where the frequency and transmission line length vary from the 100MHz PCIe standard.

The following table summarize the CLKIN configuration bit settings for the various configurations that are displayed in Figure 12 to Figure 15.

Table 30. CLKIN Configuration Bits

Configuration	AC_IN B35[1]	RX_TERM B35[0]	Notes
HCSL Input Levels (PCIe Standard)	0	0	Default Values
LVDS Input Levels	1	0	Eliminates need for external bias circuit. Must use external RT.
External AC-Coupling	1	0	Eliminates need for external bias circuit.
Receiver Termination	0	1	Prevents reflections for non-PCIe applications.

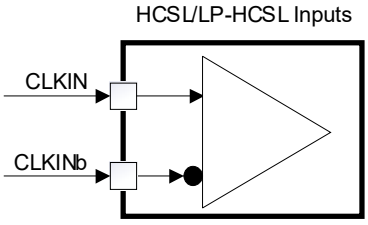


Figure 12. HCSL Input Levels (PCIe Standard)

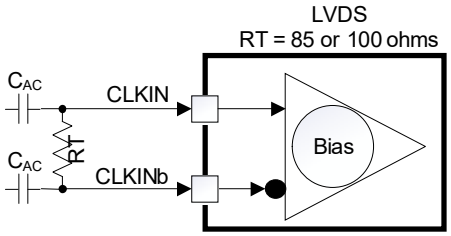


Figure 13. LVDS Input Levels

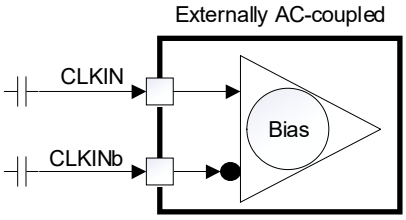


Figure 14. External AC-Coupling

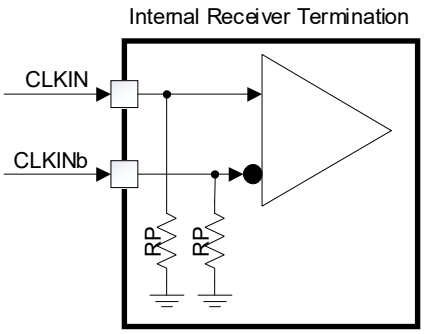


Figure 15. Receiver Termination

5.1.3 Differential CLK Output Configurations

5.1.3.1 Direct-Coupled HCSL Loads

The RC191xx LP-HCSL CLK outputs have internal source terminations and directly drive industry-standard HCSL-level inputs with no external components. They support both 85ohm and 100ohm differential impedances. The CLK outputs can also drive receiver-terminated HCSL loads. The combination of source termination and receiver termination results in a double-terminated load. When double-terminated, the CLK output swing will be half of the source-terminated values.

5.1.3.2 AC-Coupled non-HCSL Loads

The RC191xx CLK output can directly drive AC-coupling capacitors without any termination components. The clock input side of the AC-coupling capacitor may require an input-dependent bias network (BN). For examples of terminating the RC191xx CLK outputs to other logic families such as LVDS, LVPECL, or CML, see AN-891.

Figure 16 to Figure 19 show the various CLK output configurations.

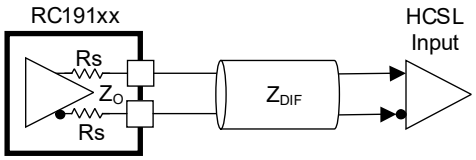


Figure 16. Direct-Coupled Source-Terminated HCSL (ZOUT_SEL_tri = 0 or 1)

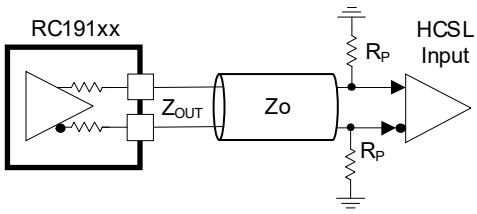


Figure 17. Direct-Coupled Double-Terminated HCSL

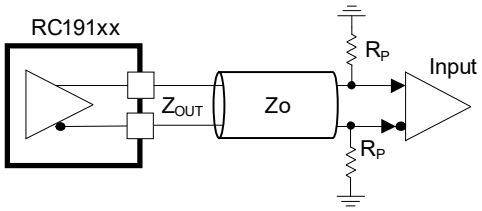


Figure 18. Receiver-Terminated Load (ZOUT_SEL_tri = M)

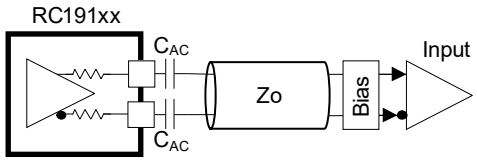


Figure 19. AC-Coupled Non-PCIe Load

5.2 Power Down Tolerant Pins

Power Down Tolerant (PDT) pins can be driven even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the RC191xx may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the RC191xx before it has received power. See the pin descriptions to identify which pins are PDT. PDT pins are also 3.3V tolerant.

5.3 Flexible Startup Sequencing

RC191xx devices support Flexible Startup Sequencing (FSS). FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table 31 shows the supported sequences; that is, the RC191xx devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Table 31. Flexible Startup Sequences

VDD	PWRGD_PWRDNb	CLKIN/CLKINb
Not present	X	Running
		Floating
		Low/Low
Present	0 or 1	Running
		Floating
		Low/Low

5.4 Loss of Signal and Automatic Clock Parking

The RC191xx buffers and multiplexers have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the “b” suffix indicates “bar”, or active-low) and sets the LOS_EVT bit in the SMBus register space. CLKIN is represented differentially in Figure 20.

Figure 20 shows the LOSb de-assertion timing for the RC191xx clock buffers. LOSb defaults to low at power up.

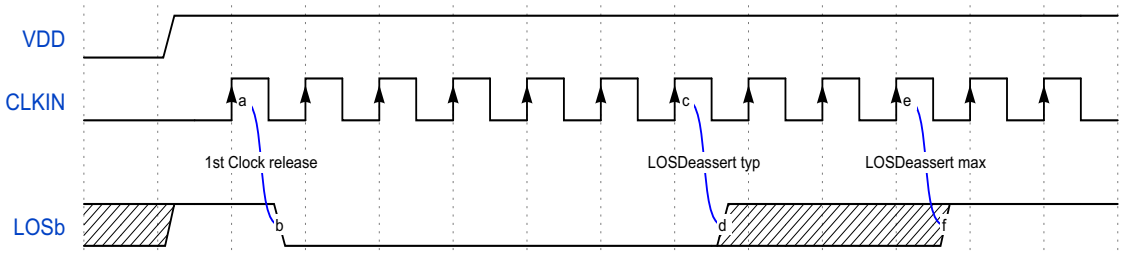


Figure 20. LOSb De-assert Timing RC191xx Devices

The following diagram shows the LOSb assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Specifications.

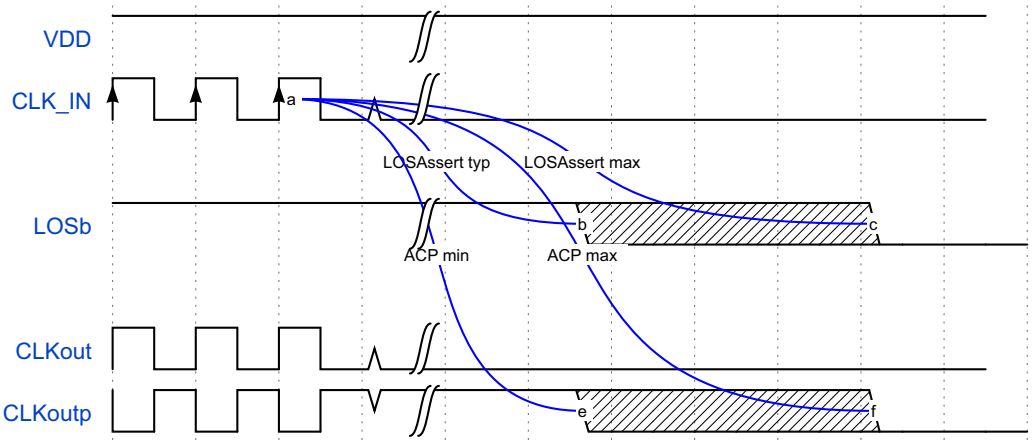


Figure 21. LOSb Assert Timing

5.5 Output Enable Control

The RC191xx buffer family provides two mechanisms to enable or disable clock outputs. All three mechanisms start and stop the output clocks in a synchronous, glitch-free manner. A clock output is enabled only when all mechanisms indicate “enabled.” The following sections describe the mechanisms.

5.5.1 SMBus Output Enable Bits

This section does not apply to the RC19102 because it does not have an SMBus.

The RC191xx clock buffer family has a traditional SMBus output enable bit for each output. The power-up default is 1, or enabled. Changing this bit to a 0 disables the output to a low/low state. The transitions between the enable and disable states are glitch-free in both directions.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

5.5.2 Output Enable (OEb) Pins

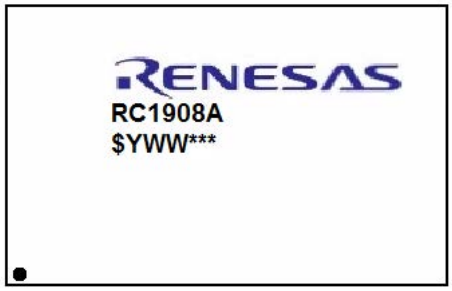
The OEb (Note: the “b” suffix indicates “bar”, or active-low) pins on the RC191xx family provide flexible CLKREQb functionality for PCIe slots and/or banked OE control for ‘motherboard-down’ devices (depending on the device). If the OEb pin is low the controlled output is enabled. If the OEb pin is high, the controlled output is disabled to a low/low state. All OEb pins enable and disable the controlled outputs in a glitch-free, synchronous manner.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

6. Package Outline Drawings

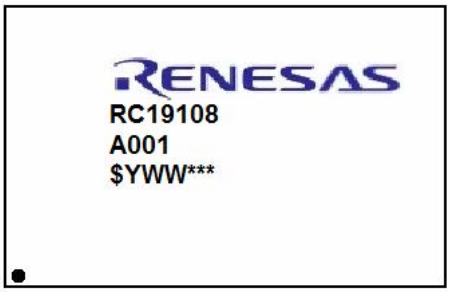
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see the package links in Ordering Information). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagrams



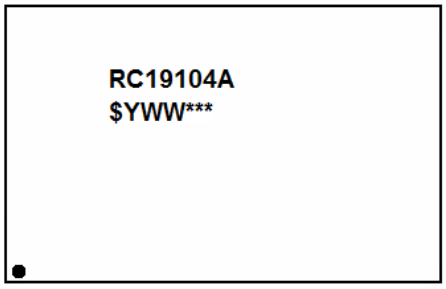
RC19108A

- Line 1 is the part number.
- Line 2:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.
  - “***” indicates the assembly lot number.



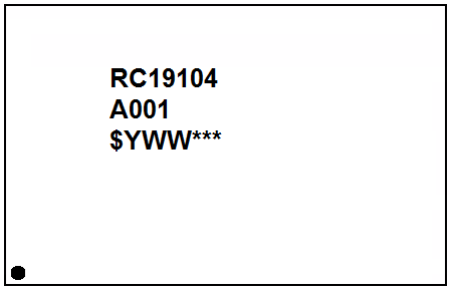
RC19108A001

- Lines 1 and 2 comprise the part number.
- Line 3:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.
  - “***” indicates the assembly lot number.



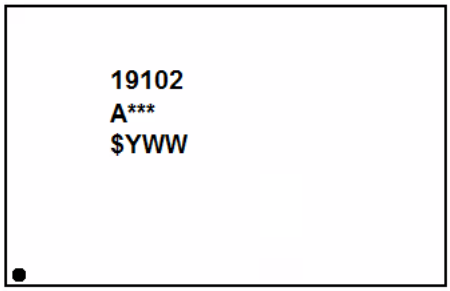
RC19104A

- Line 1 is the part number.
- Line 2:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.
  - “***” indicates the assembly lot number.



RC19104A001

- Lines 1 and 2 comprise the part number.
- Line 3:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.
  - “***” indicates the assembly lot number.



RC19102A

- Lines 1 and 2 comprise the part number (RC excluded).
- Line 2: “***” indicates the assembly lot number.
- Line 3:
  - “$” indicates the mark code.
  - “YWW” indicates the last digit of the year and work week the part was assembled.

8. Ordering Information

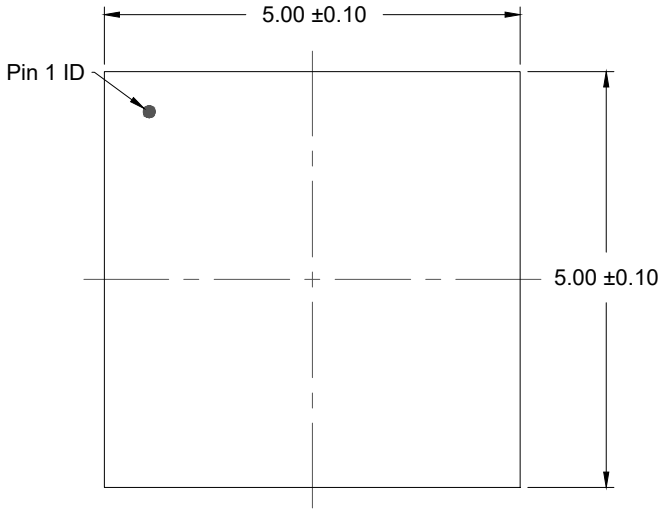
Part Number	Carrier Type	Pin Function Option	Number of Outputs	Package	Temp. Range
RC19108AGND#BB0	Tray	Slewrate Selection	8	5 × 5 mm, 0.4mm pitch, 40-VFQFPN	-40 to +105°C
RC19108AGND#KB0	Tape and Reel (EIA-481-D)				
RC19108A001GND#BB0	Tray	Amplitude Selection			
RC19108A001GND#KB0	Tape and Reel (EIA-481-D)				
RC19104AGNL#BB0	Tray	Slewrate Selection	4	4 × 4 mm, 0.4mm pitch, 28-VFQFPN	-40 to +105°C
RC19104AGNL#KB0	Tape and Reel (EIA-481-D)				
RC19104A001GNL#BB0	Tray	Amplitude Selection			
RC19104A001GNL#KB0	Tape and Reel (EIA-481-D)				
RC19102AGNT#BD0	Tray	N/A	2	3 × 3 mm, 0.4mm pitch, 20-VFQFPN	-40 to +105°C
RC19102AGNT#KD0	Tape and Reel (EIA-481-D)				

9. Revision History

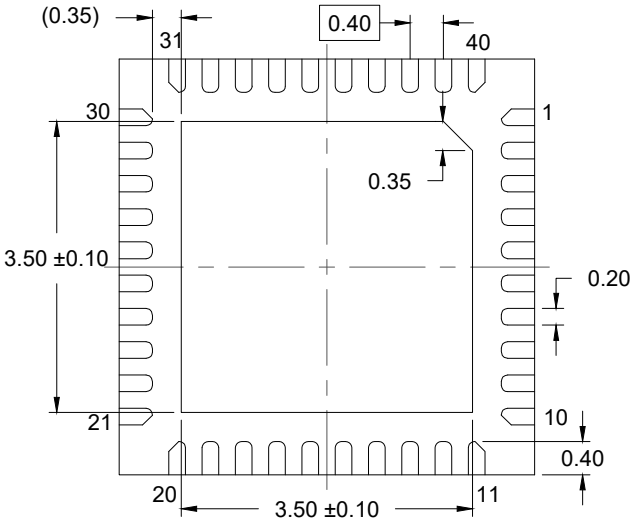
Revision	Date	Description
1.02	Jan 31, 2025	▪ Updated the binary values of [3:1] in SMBus Address Decode. ▪ Changed master/slave to host/target where appropriate.
1.01	Nov 6, 2024	▪ Added PCIe Gen7 information to Table 9 and Table 10. Also updated front page text accordingly. ▪ Corrected Table 11.
1.00	July 31, 2024	Initial release.

Package Outline Drawing

Package Code:NDG40P2
40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4292-02, Revision: 02, Date Created: Aug 30, 2022

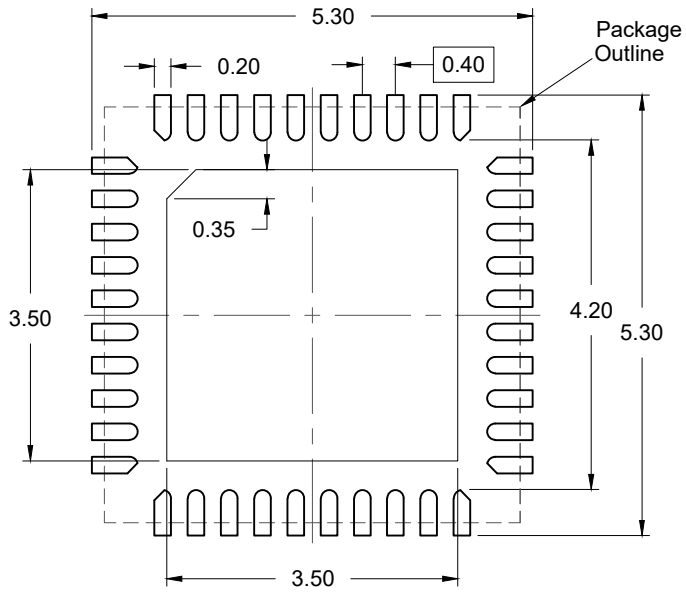


TOP VIEW



BOTTOM VIEW

SIDE VIEW



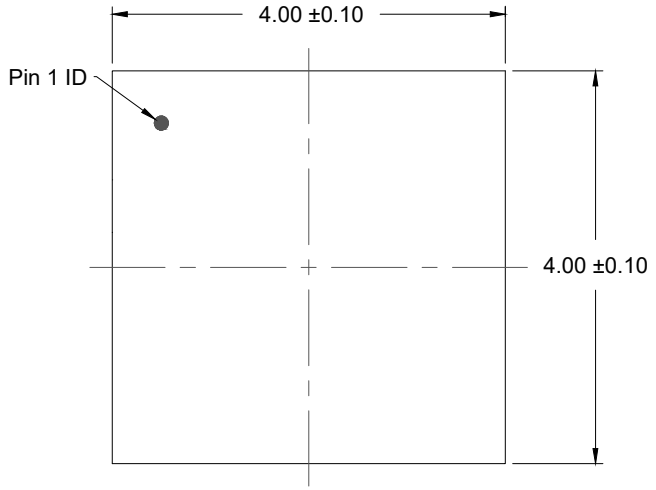
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

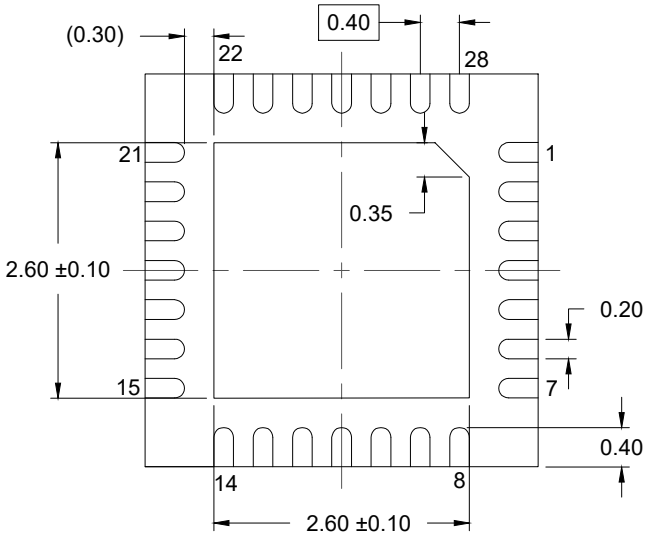
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

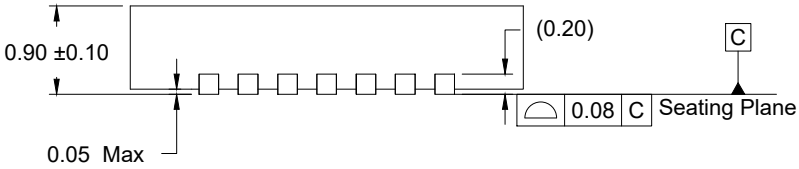
Package Code:NDG28P1
28-VFQFPN 4.0 x 4.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4249-01, Revision: 02, Date Created: Feb 06, 2024



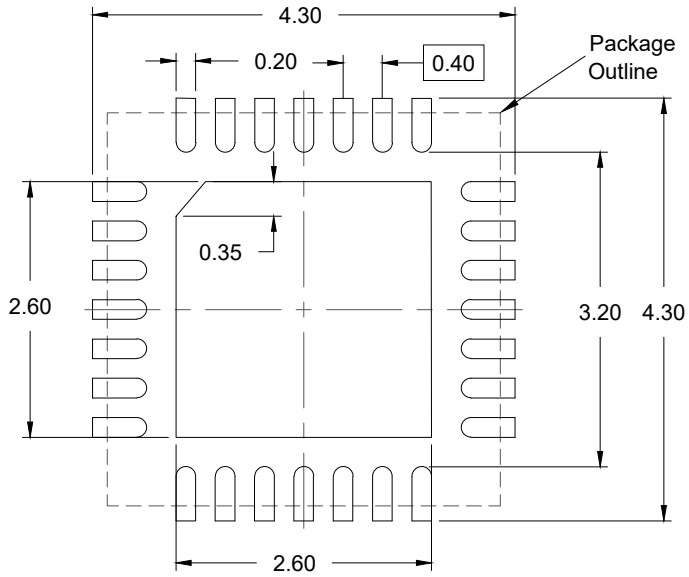
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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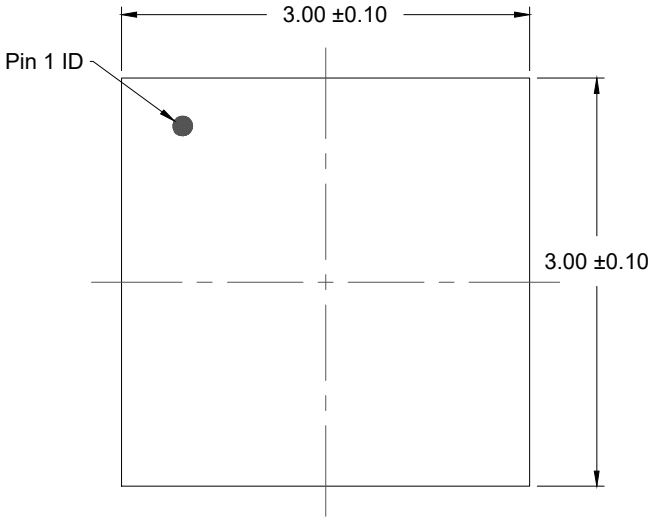
(PCB Top View, NSMD Design)

NOTES:

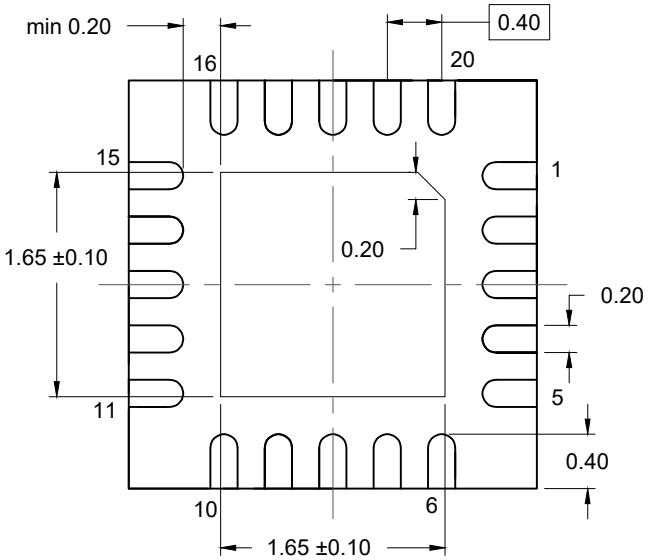
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

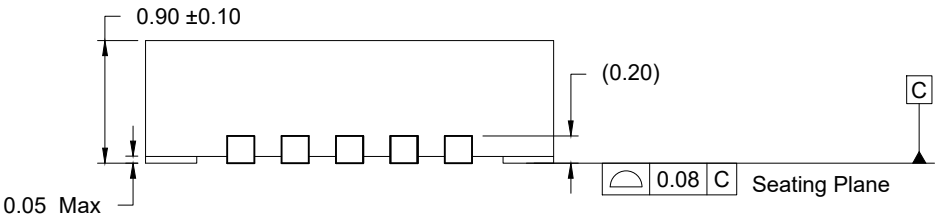
Package Code:NDG20P2
20-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4179-02, Revision: 02, Date Created: Jan 29, 2024



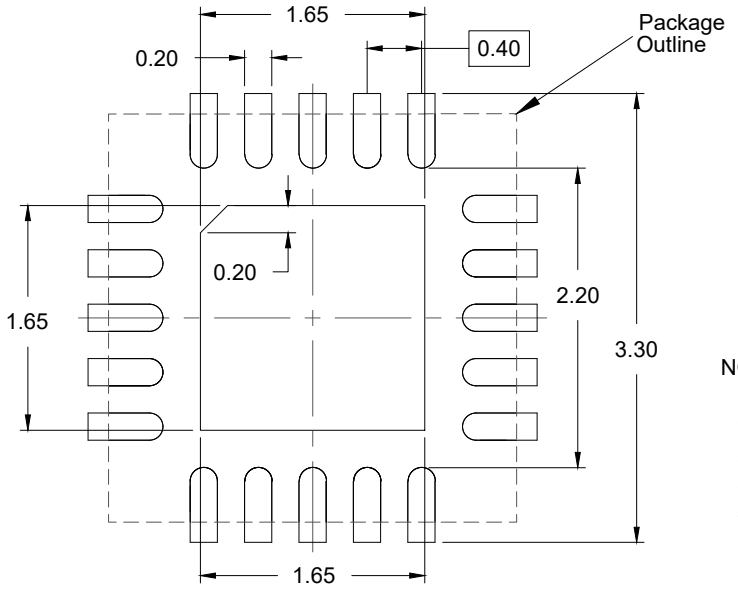
TOP VIEW



BOTTOM VIEW



SIDE VIEW



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(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
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