RC192xx

PCIe Gen5/6 2-Input Clock Mux Family with LOS

The RC192xx (RC19202, RC19204, RC19208, RC19216) are ultra-high performance clock muxes supporting PCIe Gen5 and Gen6. They provide a Loss-Of-Signal (LOS) output for system monitoring and redundancy. The devices also incorporate Power Down Tolerance (PDT), Flexible Power Sequencing (FPS), and Automatic Clock Parking (ACP) features to insure good behavior under abnormal system conditions. They can drive both source-terminated and double-terminated loads up to 400MHz. The CLKIN inputs also support either HCSL or LVDS signaling levels, making the devices ideal for LVDS to HCSL level translation. The excellent phase jitter and PNSR performance make the RC192xx well suited for network applications.

Applications

- Cloud/High-performance computing
- nVME storage
- Networking
- Accelerators

Key Specifications

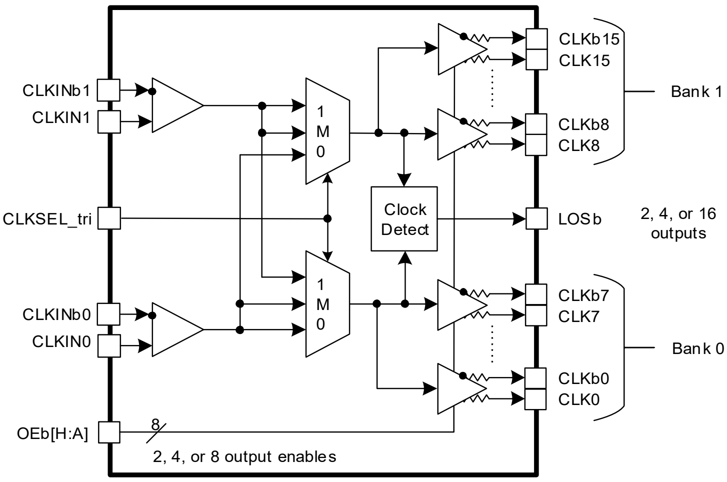
- PCIe Gen5 additive phase jitter: 7fs RMS
- PCIe Gen6 additive phase jitter: 4fs RMS
- DB2000Q additive phase jitter: 9fs RMS
- 12kHz-20MHz additive phase jitter: 37fs RMS at 156.25MHz
- 1MHz to 400MHz operation with ACP disabled
- 25MHz to 400MHz operation with ACP enabled

Features

- 2, 4, 8, or 16 Low-Power (LP) HCSL outputs saves up to 64 resistors
- 2:N or 2 x 1:N/2 modes (N is number of outputs)
- 85Ω or 100Ω output impedance
- Outputs drive both source-terminated and double-terminated loads
- Open-drain LOS output
- FPS allows inputs and clocks to be applied before power is applied or power to be applied with no input clock
- ACP cleanly parks outputs in low/low state when selected input clock is lost
- Spread-spectrum tolerant
- Up to eight output enable pins
- Selectable 4-wire Side-Band-Interface (SBI) for hardware output enable (RC19208, RC19216)
- SMBus write protection features (RC19216)
- CLKIN pins directly support HCSL or LVDS signaling levels
- 3 × 3 mm 20-VFQFPN to 6 × 6 mm 80-VFQFPN packages

PCIe Clocking Architectures

- Common Clocked (CC)
- Independent Reference (IR) with and without spread spectrum



CLKSEL_tri	0	1	M
Bank 0	CLKIN0	CLKIN1	CLKIN0
Bank 1	CLKIN0	CLKIN1	CLKIN1

Figure 1. Simplified Block Diagram and Mux Logic

Contents

1. Pin Information

1.1 Signal Types

Term	Description
I	Input
O	Input
OD	Open Drain Output
I/O	Bi-Directional
PD	Pull-down
PU	Pull-up
Z	Tristate
D	Driven
X	Don't care
SE	Single-ended
DIF	Differential
PWR	3.3 V power
GND	Ground
PDT	Power Down Tolerant: These signals tolerate being driven when the device is powered down (VDD is not present).

1.2 RC19216/RC19208 Pin Information

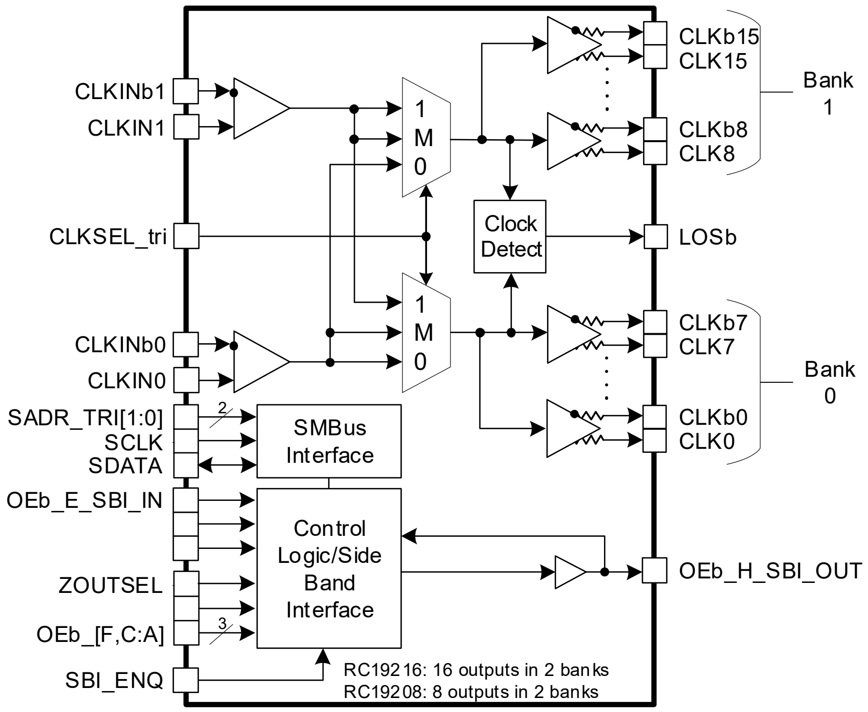


Figure 2. RC19216/RC19208 Block Diagram

1.2.1 RC19216 Pin Assignments

	1	2	3	4	5	6	7	8	9	10	11	12	
A	GNDSUB	CLKb0	CLK0	CLKb1	CLK1	CLKb2	CLK2	CLKb3	CLK3	CLKb4	CLK4	CLKb5	A
B	ZOUTSEL	VDDCLK_0	NC	OEb_A	NC	OEb_B	NC	SBI_ENQ	VDDCLK_0	NC	SADR_tri1	CLK5	B
C	VDDDIG	NC									OEb_C	CLKb6	C
D	CLKIN0	PWRGD_PWRDNb									NC	CLK6	D
E	CLKINb0	NC									OEb_D_SBI_CLK	CLKb7	E
F	SADR_tri0	VDDIN0									VDDA	CLK7	F
G	CLKIN1	NC									NC	VDDCLK_0	G
H	CLKINb1	SDATA									VDDCLK_1	LOSb	H
J	SCLK	VDDIN1									NC	CLKb8	J
K	VDDCLK_1	NC									OEb_E_SBI_IN	CLK8	K
L	CLK15	OEb_H_SBI_OUT	NC	CLKSEL_tri	NC	OEb_G_SHFT_LDb	VDDCLK_1	NC	NC	NC	OEb_F	CLKb9	L
M	CLKb15	CLK14	CLKb14	CLK13	CLKb13	CLK12	CLKb12	CLK11	CLKb11	CLK10	CLKb10	CLK9	M
	1	2	3	4	5	6	7	8	9	10	11	12	

RC19216
80-VFQFPN Package
Connect to EPAD to GND
Top View

Figure 3. 80-VFQFPN – Top View

1.2.2 RC19216 Pin Descriptions

Table 1. RC19216 Pin Descriptions

Pin Number		Pin Name	Type	Description
A	1	GNDSUB	GND	Ground pin for substrate.
A	2	CLKb0	O, DIF	Complementary clock output.
A	3	CLK0	O, DIF	True clock output.
A	4	CLKb1	O, DIF	Complementary clock output.
A	5	CLK1	O, DIF	True clock output.
A	6	CLKb2	O, DIF	Complementary clock output.
A	7	CLK2	O, DIF	True clock output.
A	8	CLKb3	O, DIF	Complementary clock output.

Table 1. RC19216 Pin Descriptions (Cont.)

Pin Number		Pin Name	Type	Description
A	9	CLK3	O, DIF	True clock output.
A	10	CLKb4	O, DIF	Complementary clock output.
A	11	CLK4	O, DIF	True clock output.
A	12	CLKb5	O, DIF	Complementary clock output.
B	1	ZOUTSEL	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω
B	2	VDDCLK_0	PWR	Power supply for clock output bank 0.
B	3	NC	NC	No connect.
B	4	OEb_A	I, SE, PDT, PU	Active low input for enabling output group A. See Table 5 for details. 1 =disable output, 0 = enable output
B	5	NC	NC	No Connect.
B	6	OEb_B	I, SE, PDT, PU	Active low input for enabling output group B. See Table 5 for details. 1 = disable output, 0 = enable output
B	7	NC	NC	No Connect.
B	8	SBI_ENQ	I, SE, PDT, PD	Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change. 0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins.
B	9	VDDCLK_0	PWR	Power supply for clock output bank 0.
B	10	NC	NC	No connect.
B	11	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19208, RC19216) table and refer to the tri-level input thresholds in the electrical tables.
B	12	CLK5	O, DIF	True clock output.
C	1	VDDDIG	PWR	Digital power.
C	2	NC	NC	No Connect.
C	11	OEb_C	I, SE, PD, PDT	Active low input for enabling output group B. See Table 5 for details. 0 = enable output, 1 = disable output.
C	12	CLKb6	O, DIF	Complementary clock output.
D	1	CLKIN0	I, DIF	True clock input.
D	2	PWRGD_PWRDNb	I, SE, PDT, PU	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
D	11	NC	NC	No connect.
D	12	CLK6	O, DIF	True clock output.
E	1	CLKINb0	I, DIF	Complementary clock input.
E	2	NC	NC	No connect.

Table 1. RC19216 Pin Descriptions (Cont.)

Pin Number		Pin Name	Type	Description
E	11	OEb_D_SBI_CLK	I, SE, PDT, PU or PD	Active low input for enabling output group D, or the clock pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section and Table 5 for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band mode: SBI clock input with internal pull-down.
E	12	CLKb7	O, DIF	Complementary clock output.
F	1	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19208, RC19216) table and refer to the tri-level input thresholds in the electrical tables.
F	2	VDDIN0	PWR	Power supply for clock input 0.
F	11	VDDA	PWR	Power supply for analog circuitry.
F	12	CLK7	O, DIF	True clock output.
G	1	CLKIN1	I, DIF	True clock input.
G	2	NC	NC	No connect.
G	11	NC	NC	No connect.
G	12	VDDCLK_0	PWR	Power supply for clock output bank 0.
H	1	CLKINb1	I, DIF	Complementary clock input.
H	2	SDATA	I/O, SE, OD, PDT	Data pin for SMBus interface.
H	11	VDDCLK_1	PWR	Power supply for clock output bank 1.
H	12	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
J	1	SCLK	I, SE, PDT	Clock pin of SMBus interface.
J	2	VDDIN1	PWR	Power supply for clock input 1.
J	11	NC	NC	No connect.
J	12	CLKb8	O, DIF	Complementary clock output.
K	1	VDDCLK_1	PWR	Power supply for clock output bank 1.
K	2	NC	NC	No connect.
K	11	OEb_E_SBI_IN	I, SE, PDT, PU or PD	Active low input for enabling output group E, or the data pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section and Table 5 for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band mode with internal pull-down: SBI shift-register data input.
K	12	CLK8	O, DIF	True clock output.
L	1	CLK15	O, DIF	True clock output.

Table 1. RC19216 Pin Descriptions (Cont.)

Pin Number		Pin Name	Type	Description
L	2	OEb_H_SBI_OUT	I/O, PU, SE	Active low input for enabling output group H, or the SBI shift register data output. The function of is this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section and Table 5 for details. ***NOTE*: This pin is NOT PDT.** OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band Mode: SBI shift register data output.
L	3	NC	NC	No connect.
L	4	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
L	5	NC	NC	No connect.
L	6	OEb_G_SHFT_LDb	I, SE, PDT, PU or PD	Active low input for enabling output group 12 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section and Table 5 for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band Mode with internal pull-down: 0 = disable SBI shift register, 1 = enable SBI shift register. A falling edge transfers SBI shift register contents to SBI output control register.
L	7	VDDCLK_1	PWR	Power supply for clock output bank 1.
L	8	NC	NC	No connect.
L	9	NC	NC	No connect.
L	10	NC	NC	No connect.
L	11	OEb_F	I, SE, PU, PDT	Active low input for enabling output group F. Refer to the Table 5 for details. 0 = enable output, 1 = disable output.
L	12	CLKb9	O, DIF	Complementary clock output.
M	1	CLKb15	O, DIF	Complementary clock output.
M	2	CLK14	O, DIF	True clock output.
M	3	CLKb14	O, DIF	Complementary clock output.
M	4	CLK13	O, DIF	True clock output.
M	5	CLKb13	O, DIF	Complementary clock output.
M	6	CLK12	O, DIF	True clock output.
M	7	CLKb12	O, DIF	Complementary clock output.
M	8	CLK11	O, DIF	True clock output.
M	9	CLKb11	O, DIF	Complementary clock output.
M	10	CLK10	O, DIF	True clock output.
M	11	CLKb10	O, DIF	Complementary clock output.
M	12	CLK9	O, DIF	True clock output.
N/A		EPAD	GND	Ground pin.

1.2.3 RC19208 Pin Assignments

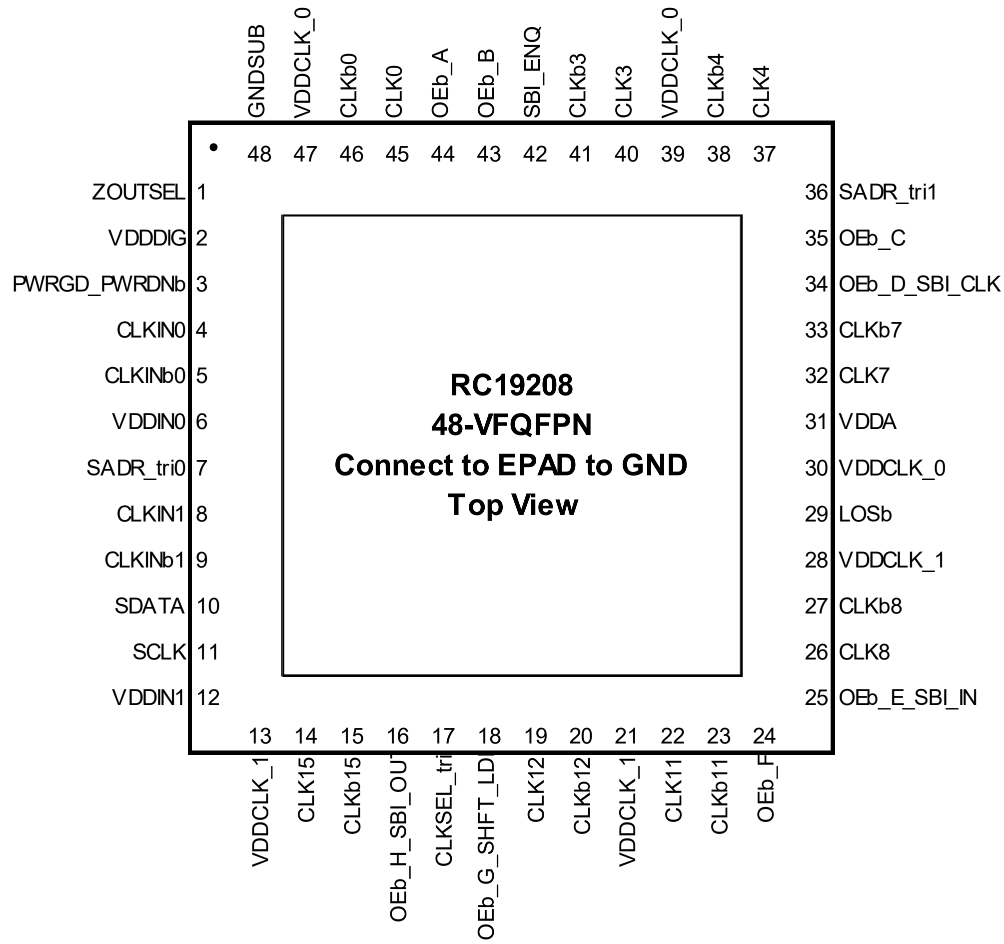


Figure 4. 48-VFQFPN – Top View

1.2.4 RC19208 Pin Descriptions

Table 2. RC19208 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	ZOUTSEL	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω
2	VDDDIG	PWR	Digital power.
3	PWRGD_PWRDNb	I, SE, PDT, PU	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
4	CLKIN0	I, DIF	True clock input.
5	CLKINb0	I, DIF	Complementary clock input.
6	VDDIN0	PWR	Power supply for clock input 0.
7	SADR_tri0	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19208, RC19216) table and refer to the tri-level input thresholds in the electrical tables.
8	CLKIN1	I, DIF	True clock input.
9	CLKINb1	I, DIF	Complementary clock input.

Table 2. RC19208 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
10	SDATA	I/O, SE, OD, PDT	Data pin for SMBus interface.
11	SCLK	I, SE, PDT	Clock pin of SMBus interface.
12	VDDIN1	PWR	Power supply for clock input 1.
13	VDDCLK_1	PWR	Power supply for clock output bank 1.
14	CLK15	O, DIF	True clock output.
15	CLKb15	O, DIF	Complementary clock output.
16	OEb_H_SBI_OUT	I/O, PU, SE	Active low input for enabling output group H, or the SBI shift register data output. The function of is this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section for details. ***Note*: This pin is NOT PDT.** OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band Mode: SBI shift register data output.
17	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
18	OEb_G_SHFT_LDb	I, SE, PDT, PU or PD	Active low input for enabling output group 12 or SHFT_LDb pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band Mode with internal pull-down: 0 = disable SBI shift register, 1 = enable SBI shift register. A falling edge transfers SBI shift register contents to SBI output control register.
19	CLK12	O, DIF	True clock output.
20	CLKb12	O, DIF	Complementary clock output.
21	VDDCLK_1	PWR	Power supply for clock output bank 1.
22	CLK11	O, DIF	True clock output.
23	CLKb11	O, DIF	Complementary clock output.
24	OEb_F	I, SE, PDT, PU	Active low input for enabling output group F. See the OEb_Assignment registers in Table 33 for output control details. 0 = enable output, 1 = disable output.
25	OEb_E_SBI_IN	I, SE, PDT, PU or PD	Active low input for enabling output group E, or the data pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band mode with internal pull-down: SBI shift-register data input.
26	CLK8	O, DIF	True clock output.
27	CLKb8	O, DIF	Complementary clock output.

Table 2. RC19208 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
28	VDDCLK_1	PWR	Power supply for clock output bank 1.
29	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
30	VDDCLK_0	PWR	Power supply for clock output bank 0.
31	VDDA	PWR	Power supply for analog circuitry.
32	CLK7	O, DIF	True clock output.
33	CLKb7	O, DIF	Complementary clock output.
34	OEb_D_SBI_CLK	I, SE, PDT, PU or PD	Active low input for enabling output group D, or the clock pin for the Side-Band Interface. The function of this pin is controlled by the SBI_EN or SBI_ENQ pin. Refer to the Side-band Interface section for details. OE mode with internal pull-up: 0 = enable output, 1 = disable output. Side-Band mode: SBI clock input with internal pull-down.
35	OEb_C	I, SE, PU, PDT	Active low input for enabling output group C. See the OEb_Assignment registers in Table 33 for output control details. 0 = enable output, 1 = disable output.
36	SADR_tri1	I, SE, PD, PU	SMBus address bit. This is a tri-level input that works in conjunction with other SADR pins, if present, to decode SMBus Addresses. See the SMBus Address Selection (RC19208, RC19216) table and refer to the tri-level input thresholds in the electrical tables.
37	CLK4	O, DIF	True clock output.
38	CLKb4	O, DIF	Complementary clock output.
39	VDDCLK_0	PWR	Power supply for clock output bank 0.
40	CLK3	O, DIF	True clock output.
41	CLKb3	O, DIF	Complementary clock output.
42	SBI_ENQ	I, SE, PD, PDT	Input that selects function of pins that are multiplexed between OE and SBI functionality. SMBus output enable bits and non-multiplexed OE pins remain functional when SBI is enabled. This pin must be strapped to its desired state. It cannot dynamically change. 0 = SBI is disabled. Multiplexed pins function as output enables. 1 = SBI is enabled. Multiplexed pins function as SBI control pins.
43	OEb_B	I, SE, PU, PDT	Active low input for enabling output group B. See the OEb_Assignment registers in Table 33 for output control details. 0 = enable output, 1 = disable output.
44	OEb_A	I, SE, PU, PDT	Active low input for enabling output group A. See the OEb_Assignment registers in Table 33 for output control details. 0 = enable output, 1 = disable output.
45	CLK0	O, DIF	True clock output.
46	CLKb0	O, DIF	Complementary clock output.
47	VDDCLK_0	PWR	Power supply for clock output bank 0.
48	GNDSUB	GND	Ground pin for substrate.
49	EPAD	PWR	Ground.

1.3 RC19204/RC19202 Pin Information

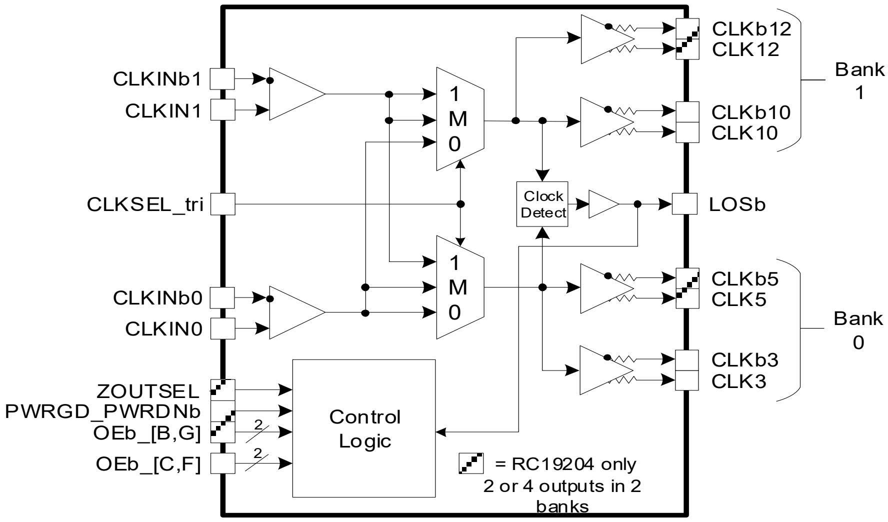


Figure 5. RC19204/RC19202 Block Diagram

1.3.1 RC19204 Pin Assignments

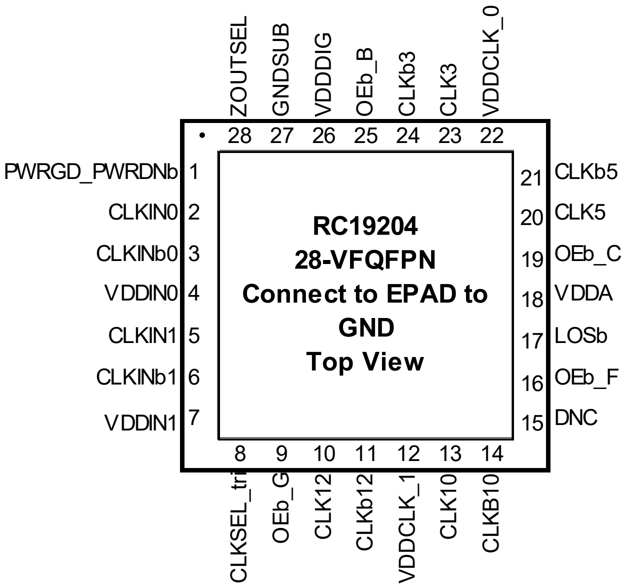


Figure 6. 28-VFQFPN – Top View

1.3.2 RC19204 Pin Descriptions

Table 3. RC19204 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	PWRGD_PWRDNb	I, SE, PDT, PU	Input notifies device to sample latched inputs and start up on first high assertion. Low enters Power Down Mode, subsequent high assertions exit Power Down Mode.
2	CLKIN0	I, DIF	True clock input.
3	CLKINb0	I, DIF	Complementary clock input.
4	VDDIN0	PWR	Power supply for clock input 0.
5	CLKIN1	I, DIF	True clock input.

Table 3. RC19204 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
6	CLKINb1	I, DIF	Complementary clock input.
7	VDDIN1	PWR	Power supply for clock input 1.
8	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
9	OEb_G	I, SE, PU, PDT	Active low input for enabling output group G. Refer to the Side-band Interface section and Table 5 for details.0 = enable output, 1 = disable output.
10	CLK12	O, DIF	True clock output.
11	CLKb12	O, DIF	Complementary clock output.
12	VDDCLK_1	PWR	Power supply for clock output bank 1.
13	CLK10	O, DIF	True clock output.
14	CLKB10	O, DIF	Complementary clock output.
15	DNC	-	Do not connect anything to this pin.
16	OEb_F	I, SE, PU, PDT	Active low input for enabling output group F. Refer to the Side-band Interface section and Table 5 for details. 0 = enable output, 1 = disable output.
17	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
18	VDDA	PWR	Power supply for analog circuitry.
19	OEb_C	I, SE, PU, PDT	Active low input for enabling output group C. Refer to the Side-band Interface section and Table 5 for details. 0 = enable output, 1 = disable output.
20	CLK5	O, DIF	True clock output.
21	CLKb5	O, DIF	Complementary clock output.
22	VDDCLK_0	PWR	Power supply for clock output bank 0.
23	CLK3	O, DIF	True clock output.
24	CLKb3	O, DIF	Complementary clock output.
25	OEb_B	I, SE, PU, PDT	Active low input for enabling output group B. Refer to the Side-band Interface section and Table 5 for details. 0 = enable output, 1 = disable output.
26	VDDDIG	PWR	Digital power.
27	GNDSUB	GND	Ground pin for substrate.
28	ZOUTSEL	I, SE, PD	Input to select differential output impedance. 0 = 85Ω, 1 = 100Ω
29	EPAD	GND	Connect to ground.

1.3.3 RC19202 Pin Assignments

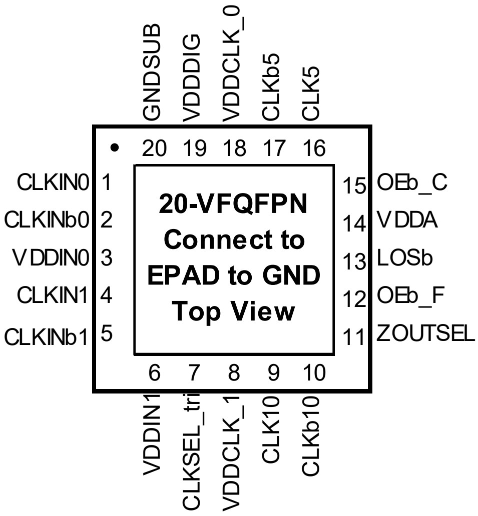


Figure 7. 20-VFQFPN – Top View

1.3.4 RC19202 Pin Descriptions

Table 4. RC19202 Pin Descriptions

Pin Number	Pin Name	Type	Description
1	CLKIN0	I, DIF	True clock input.
2	CLKINb0	I, DIF	Complementary clock input.
3	VDDIN0	PWR	Power supply for clock input 0.
4	CLKIN1	I, DIF	True clock input.
5	CLKINb1	I, DIF	Complementary clock input.
6	VDDIN1	PWR	Power supply for clock input 1.
7	CLKSEL_tri	I, SE, PD, PU	Input to select differential input clock 0 or differential input clock 1. This input has an internal pull-up and pull-down resistor to bias a floating pin to the mid-point. 0 = CLKIN0 selected for all outputs. 1 = CLKIN1 selected for all outputs. M = CLKIN0 goes to bank 0 and CLKIN1 goes to bank 1.
8	VDDCLK_1	PWR	Power supply for clock output bank 1.
9	CLK10	O, DIF	True clock output.
10	CLKb10	O, DIF	Complementary clock output.
11	ZOUTSEL	I, SE, PD	Input to select differential output impedance 0 = 85Ω, 1 = 100Ω.
12	OEb_F	I, SE, PU, PDT	Active low input for enabling output group F. Refer to the Side-band Interface section and Table 5 for details. 0 = enable output, 1 = disable output.
13	LOSb	O, OD, PDT	Output indicating Loss of Input Signal. This pin is an open drain output and requires an external pull up resistor for proper functionality. A low output on this pin indicates a loss of signal on the input clock.
14	VDDA	PWR	Power supply for analog circuitry.

Table 4. RC19202 Pin Descriptions (Cont.)

Pin Number	Pin Name	Type	Description
15	OEb_C	I, SE, PU, PDT	Active low input for enabling output group C. Refer to the Side-band Interface section and Table 5 for details. 0 = enable output, 1 = disable output.
16	CLK5	O, DIF	True clock output.
17	CLKb5	O, DIF	Complementary clock output.
18	VDDCLK_0	PWR	Power supply for clock output bank 0.
19	VDDDIG	PWR	Digital power.
20	GNDSUB	GND	Ground pin for substrate.
21	EPAD	GND	Connect to ground.

1.4 OEb Pin to CLK Output Mapping

Table 5. Output Enable Mapping by Device [1]

Device	Pin Name	Default Output Control	Alternate Output Control via SMBus
RC19216	OEb_A	0	1
	OEb_B	2	3
	OEb_C	4	5
	OEb_D_SBI_CLK	6	7
	OEb_E_SBI_IN	8	9
	OEb_F	10	11
	OEb_G_SHFT_LDb	12	13
	OEb_H_SBI_OUT	14	15
RC19208	OEb_A	0	-
	OEb_B	3	-
	OEb_C	4	-
	OEb_D_SBI_CLK	7	-
	OEb_E_SBI_IN	8	-
	OEb_F	11	-
	OEb_G_SHFT_LDb	12	-
	OEb_H_SBI_OUT	15	-
RC19204	OEb_B	3	-
	OEb_C	5	-
	OEb_F	10	-
	OEb_G	12	-
RC19202	OEb_C	5	-
	OEb_F	10	-

1. Assuming Side-Band Interface is not enabled.

2. Specifications

2.1 Absolute Maximum Ratings

Table 6. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Unit
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin	-0.5	3.9	V
V_{IN}	Input Voltage	[1]	-0.5	3.9	V
V_{IN}	Input Voltage	[2]	-0.5	V_{DDx} + 0.3	V
I_{IN}	Input Current	All SE inputs and CLKIN [2]	-	±50	mA
I_{OUT}	Output Current – Continuous	CLK	-	30	mA
		SDATA, SBI_OUT	-	25	mA
	Output Current – Surge	CLK	-	60	mA
		SDATA, SBI_OUT	-	50	mA
T_J	Maximum Junction Temperature	-	-	150	°C
T_S	Storage Temperature	Storage Temperature	-65	150	°C
ESD	Human Body Model	JESD22-A114 (JS-001) Classification	-	2000	V
	Charged Device Model	JESD22-C101 Classification	-	500	V

1. Pins designated Power Down Tolerant (PDT) in the pin description table.
2. Pins not designated Power Down Tolerant (PDT) in the pin description table.

2.2 Recommended Operation Conditions

All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise. All conditions in this table must be met to guarantee device functionality and performance.

Table 7. Recommended Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
T_J	Maximum Junction Temperature	-	-	-	125	°C
T_A	Ambient Operating Temperature	-	-40	25	105	°C
V_{DDx}	Supply Voltage with respect to Ground	Any VDD pin, 3.3V ±10% supply.	2.97	3.3	3.63	V
t_{PU}	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic)	Power-up time for all VDDs to reach minimum specified voltage (power ramps must be monotonic).	0.05	-	5	ms

2.3 Thermal Specifications

Table 8. Thermal Specifications

Package [1]	Symbol	Conditions	Typical Value (°C/W)
6 × 6 mm 80-VFQFPN (2.8 × 2.8 mm Epad)	θ_{Jc}	Junction to Case	44.2
	θ_{Jb}	Junction to Base	2.4
	θ_{JA0}	Junction to Air, still air	33.1
	θ_{JA1}	Junction to Air, 1 m/s air flow	29.5
	θ_{JA3}	Junction to Air, 3 m/s air flow	28
	θ_{JA5}	Junction to Air, 5 m/s air flow	27.1
6 × 6 mm 48-VFQFPN (4.2 x 4.2 mm Epad)	θ_{Jc}	Junction to Case	28.5
	θ_{Jb}	Junction to Base	3.3
	θ_{JA0}	Junction to Air, still air	28.5
	θ_{JA1}	Junction to Air, 1 m/s air flow	25.4
	θ_{JA3}	Junction to Air, 3 m/s air flow	22.9
	θ_{JA5}	Junction to Air, 5 m/s air flow	21.8
4 × 4 mm 28-VFQFPN (2.6 × 2.6 mm Epad)	θ_{Jc}	Junction to Case	45.3
	θ_{Jb}	Junction to Base	2.2
	θ_{JA0}	Junction to Air, still air	36.3
	θ_{JA1}	Junction to Air, 1 m/s air flow	32.7
	θ_{JA3}	Junction to Air, 3 m/s air flow	31.0
	θ_{JA5}	Junction to Air, 5 m/s air flow	30.0
3 × 3 mm 20-VFQFPN (1.65 × 1.65 mm Epad)	θ_{Jc}	Junction to Case	96.3
	θ_{Jb}	Junction to Base	20.4
	θ_{JA0}	Junction to Air, still air	54.8
	θ_{JA1}	Junction to Air, 1 m/s air flow	51.1
	θ_{JA3}	Junction to Air, 3 m/s air flow	47.7
	θ_{JA5}	Junction to Air, 5 m/s air flow	46.2

1. Epad soldered to board.

2.4 Electrical Characteristics

2.4.1 PCIe Phase Jitter

All PCIe Phase Jitter measurements are made with one input at 100MHz and the other input at 99.75MHz to approximate the impact of SSC.

Table 9. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) – Normal Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	521	590	86,000 [6]	fs pk-pk
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	31	35	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	9	10	3,000 [6]	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	15	17	1,000 [6]	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	15	17	500 [6]	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	6	7	150 [6]	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	3.5	4	100 [6]	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	40	45	[7]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	11	12		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	11	12		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	9	10		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	12	13		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 1600mV and input slew rate = 3.5V/ns

Table 10. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) – Degraded Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	686	812	86,000[6]	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	40	47	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	11	13	3,000 [6]	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	19	23	1,000 [6]	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	19	23	500 [6]	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	8	9	150 [6]	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	5	6	100 [6]	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	52	60	[7]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	14	16		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	14	16		
$t_{jphPCIeG5-IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	12	14		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	15	18		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 800mV and input slew rate = 1.5V/ns

Table 11. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Both CLKIN Running) – Normal Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1\text{-}CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	2520	4560	86,000 [6]	fs pk-pk
$t_{jphPCIeG2\text{-}CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	73	128	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	116	189	3,000 [6]	
$t_{jphPCIeG3\text{-}CC}$		PCIe Gen3 (8.0 GT/s)	59	98	1,000 [6]	
$t_{jphPCIeG4\text{-}CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	59	98	500 [6]	
$t_{jphPCIeG5\text{-}CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	18	30	150 [6]	
$t_{jphPCIeG6\text{-}CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	12	21	100 [6]	
$t_{jphPCIeG2\text{-}IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	259	429	[7]	fs RMS
$t_{jphPCIeG3\text{-}IR}$		PCIe Gen3 (8.0 GT/s)	82	141		
$t_{jphPCIeG4\text{-}IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	87	149		
$t_{jphPCIeG5\text{-}IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	34	55		
$t_{jphPCIeG6\text{-}IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	48	78		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 800mV and input slew rate = 1.5V/ns

Table 12. PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Both CLKIN Running) – Degraded Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	2680	3450	86,000 [6]	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	91	146	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	123	154	3,000 [6]	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	64	83	1,000 [6]	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	64	83	500 [6]	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	19	26	150 [6]	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	14	18	100 [6]	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	285	381	[7]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	88	112		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	93	118		
$t_{jphPCIeG5-IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	38	47		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	55	76		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 800mV and input slew rate = 1.5V/ns

Table 13. PCIe Refclk Phase Jitter (CLKSEL_tri = M, Both CLKIN Running) – Normal Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3570	4790	86,000 [6]	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	72	114	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	157	336	3,000 [6]	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	60	94	1,000 [6]	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	60	94	500 [6]	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	26	62	150 [6]	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	14	24	100 [6]	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	256	398	[7]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	113	157		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	108	142		
$t_{jphPCIeG5-IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	38	52		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	47	74		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 1600mV and input slew rate = 3.5V/ns

Table 14. PCIe Refclk Phase Jitter (CLKSEL_tri = M, Both CLKIN Running) – Degraded Conditions [1][2][3][8]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphPCIeG1-CC}$	Additive PCIe Phase Jitter (Common Clocked Architecture)	PCIe Gen1 (2.5 GT/s)	3640	7860	86,000 [6]	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen2 Hi Band (5.0 GT/s)	86	146	3,100 [6]	fs RMS
		PCIe Gen2 Lo Band (5.0 GT/s)	161	338	3,000 [6]	
$t_{jphPCIeG3-CC}$		PCIe Gen3 (8.0 GT/s)	64	99	1,000 [6]	
$t_{jphPCIeG4-CC}$		PCIe Gen4 (16.0 GT/s) [3][4]	64	99	500 [6]	
$t_{jphPCIeG5-CC}$		PCIe Gen5 (32.0 GT/s) [3][5]	26	61	150 [6]	
$t_{jphPCIeG6-CC}$		PCIe Gen6 (64.0 GT/s) [3][5]	15	25	100 [6]	
$t_{jphPCIeG2-IR}$	Additive PCIe Phase Jitter (IR Architectures)	PCIe Gen2 (5.0 GT/s)	278	415	[7]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen3 (8.0 GT/s)	116	216		
$t_{jphPCIeG4-IR}$		PCIe Gen4 (16.0 GT/s) [3][4]	112	196		
$t_{jphPCIeG5-IR}$		PCIe Gen5 (32.0 GT/s) [3][5]	41	68		
$t_{jphPCIeG6-IR}$		PCIe Gen6 (64.0 GT/s) [3][5]	52	78		

1. The Refclk jitter is measured after applying the filter functions found in PCI Express Base Specification 6.0, Revision 0.9. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed.
7. The PCI Express Base Specification 6.0, Revision 0.9 provides the filters necessary to calculate SRIS jitter values; it does not provide specification limits, hence the reference to this footnote in the Limit column. SRIS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. Differential input swing = 800mV and input slew rate = 1.5V/ns

2.4.2 Other Phase Jitter

Table 15. Non-PCIe Refclk Phase Jitter (CLKSEL_tri = 0 or 1, Unselected CLKIN Off) [1][2][3]

Symbol	Parameter	Conditions	Typical	Maximum	Specification Limit	Unit
$t_{jphDB2000Q}$	Additive Phase Jitter	100MHz, Intel-supplied filter [3][4]	10	11	80 [5]	fs RMS
		100MHz, Intel-supplied filter [3][6]	13	15	80 [5]	
$t_{jph12k\text{-}20M}$	Additive Phase Jitter	156.25MHz (12kHz to 20MHz) [4]	31	35	N/A	
		156.25MHz (12kHz to 20MHz) [6]	39	45	N/A	

1. See Test Loads for test configuration. Measured with one input at 100MHz and the other at 156.25MHz.
2. SMA100B used as signal source.
3. The RC19xxx devices meet all legacy QPI/UPI specifications by meeting the PCIe and DB2000Q specifications listed in this document.
4. Differential input swing = 1600mV and input slew rate = 3.5V/ns
5. The rms sum of the source jitter and the additive jitter (arithmetic sum for PCIe Gen1) must be less than the jitter specification listed. CLKSEL_tri = M is only recommended for PCIe applications.
6. Differential input swing = 800mV and input slew rate = 1.5V/ns

Note: Dual-mode operation (CLKSEL_tri = M, both CLKIN running) is not recommended for non-PCIe applications.

2.4.3 Output Frequencies, Startup Time and LOS Timing

Table 16. Output Frequencies, Startup Time and LOS Timing

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{OP}	Operating Frequency	Automatic Clock Parking (ACP) Circuit disabled.	1	-	400	MHz
		Automatic Clock Parking (ACP) Circuit enabled.	25	-	400	
$t_{STARTUP}$	Start-up Time	[1]	-	1.2	3	ms
		[2]	-	0.3	1	ms
t_{LATOEb}	OEb Latency	OEb assertion/de-assertion CLK start/stop latency. Selected input clock must be running.	4	5	10	clks
$t_{LOSAssert}$	LOS Assert Time	Time from disappearance of selected input clock to LOS assert. [3][4]	-	123	200	ns
$t_{LOSDeassert}$	LOS De-assert Time	Time from appearance of selected input clock to LOS de-assert. [2][5]	6	-	9	clks

1. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. PWRGD_PGWRDNb tied to VDD in this case.
2. VDD stable, measured from de-assertion of PWRGD_PWRDNb.
3. The clock detect circuit does not qualify the accuracy of the input clock.
4. PWRGD_PWRDNb high. The clock detect circuit will park the outputs in a low/low state within this time.
5. PWRGD_PWRDNb high. The clock detect circuit will drive the outputs to a high/low state within this time and then begin clocking the outputs.

2.4.4 CLK (LP-HCSL) AC/DC Output Characteristics

Table 17. 85Ω CLK AC/DC Characteristics for Source-Terminated 100MHz PCIe [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1040	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-93	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	724	827	933	-	
V_{LOW}	Voltage Low [3]		-88	15	87	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 800mV, scope averaging off.	333	421	511	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		-	14	88	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, scope averaging on.	2.5	3.0	3.6	2 to 4	V/ns
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV.	-	2.7	12.4	20	%
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	811	921	1032	-	mV
V_{LOW}	Voltage Low [3]		-56	14	87	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 900mV, scope averaging off.	363	455	549	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		-	15	92	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, scope averaging on.	2.7	3.2	3.9	2 to 4	V/ns
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV.	-	5.2	18.0	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49.6	49.9	50.3	45 to 55	

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. The specification limits are taken from either the PCIe Base Specification Revision 6.0 or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 18. 100Ω CLK AC/DC Characteristics for Source-Terminated 100MHz PCIe [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Specification Limit [2]	Unit
V_{MAX}	Absolute Max Voltage Includes 300mV of Overshoot (Vovs) [3][4]	Across all settings in this table at 100MHz.	-	-	1062	1150	mV
V_{MIN}	Absolute Min Voltage Includes -300mV of Undershoot (Vuds) [3][5]		-139	-	-	-300	
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 800mV.	734	846	940	-	
V_{LOW}	Voltage Low [3]		-47	29	103	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 800mV, scope averaging off.	313	413	474	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		-	12	71	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 800mV, scope averaging on.	2.3	2.9	3.4	2 to 4	V/ns
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 800mV.	-	5.7	17.9	20	%
V_{HIGH}	Voltage High [3]	V_{HIGH} set to 900mV.	818	943	1051	-	mV
V_{LOW}	Voltage Low [3]		-52	30	112	-	
V_{CROSS}	Crossing Voltage (abs) [3][6][7]	V_{HIGH} set to 900mV, scope averaging off.	366	475	539	250 to 550	
ΔV_{CROSS}	Crossing Voltage (var) [3][6][8]		-	13	78	140	
dv/dt	Slew Rate [9][10]	V_{HIGH} set to 900mV, scope averaging on.	2.6	3.3	3.8	2 to 4	V/ns
$\Delta T_{R/F}$	Rise/Fall Matching [3][11]	V_{HIGH} set to 900mV.	-	2.5	15.7	20	%
t_{DC}	Output Duty Cycle [9]	V_T = 0V differential.	49.6	50.0	50.3	45 to 55	

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. The specification limits are taken from either the PCIe Base Specification Revision 6.0 or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 19. 85Ω CLK AC/DC Characteristics for Non-PCIe Applications, Source-Terminated Loads [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz	702	826	937	mV
V_{OL}	Output Low Voltage [2]		-71	22	115	
V_{CROSS}	Crossing Voltage (abs) [3]		306	414	517	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	19	104	
t_R	Rise Time [2] V_T = 20% to 80% of swing		236	377	535	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		236	382	508	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz	766	919	1074	mV
V_{OL}	Output Low Voltage [2]		-87	23	133	
V_{CROSS}	Crossing Voltage (abs) [3]		355	452	545	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	16	81	
t_R	Rise Time [2] V_T = 20% to 80% of swing		231	430	617	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		251	382	511	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V	47.6	49.8	52.0	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 20. 100Ω CLK AC/DC Characteristics for Non-PCIe Applications, Source-Terminated Loads [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz	704	834	951	mV
V_{OL}	Output Low Voltage [2]		-69	26	117	
V_{CROSS}	Crossing Voltage (abs) [3]		328	422	539	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	12	83	
t_R	Rise Time [2] V_T = 20% to 80% of swing		292	414	541	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		255	378	483	ps

Table 20. 100Ω CLK AC/DC Characteristics for Non-PCIe Applications, Source-Terminated Loads [1] (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz	764	928	1078	mV
V_{OL}	Output Low Voltage [2]		-85	26	135	
V_{CROSS}	Crossing Voltage (abs) [3]		336	472	635	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	12	65	
t_R	Rise Time [2] V_T = 20% to 80% of swing		309	417	546	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		277	389	504	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V	47.2	49.8	52.1	%

1. Standard high impedance load with C_L = 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 21. 85ohm CLK AC/DC Output Characteristics for Non-PCIe Applications, Double-Terminated Loads [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz. (amplitude is reduced by ~50% due to double termination).	400	435	475	mV
V_{OL}	Output Low Voltage [2]		-30	7	45	
V_{CROSS}	Crossing Voltage (abs) [3]		165	208	245	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	10	45	
t_R	Rise Time [2] V_T = 20% to 80% of swing		256	357	475	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		198	277	380	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination).	440	483	525	mV
V_{OL}	Output Low Voltage [2]		-31	8	48	
V_{CROSS}	Crossing Voltage (abs) [3]		180	223	265	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	10	45	
t_R	Rise Time [2] V_T = 20% to 80% of swing		300	410	545	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		200	275	370	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	49.2	49.8	50.4	%

1. Both Tx and Rx are terminated (double-terminated) with CL= 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.

5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

Table 22. 100ohm CLK AC/DC Output Characteristics for Non-PCIe Applications, Double-Terminated Loads [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz. (amplitude is reduced by ~50% due to double termination).	364	404	444	mV
V_{OL}	Output Low Voltage [2]		-31	7	45	
V_{CROSS}	Crossing Voltage (abs) [3]		159	196	233	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	6	41	
t_R	Rise Time [2] V_T = 20% to 80% of swing		226	344	462	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		165	268	371	ps
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, 25MHz, 100MHz, 156.25MHz, 312.5MHz (amplitude is reduced by ~50% due to double termination).	408	450	492	mV
V_{OL}	Output Low Voltage [2]		-33	7	47	
V_{CROSS}	Crossing Voltage (abs) [3]		177	219	261	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	7	42	
t_R	Rise Time [2] V_T = 20% to 80% of swing		203	338	473	ps
t_F	Fall Time [2] V_T = 20% to 80% of swing		175	270	365	ps
t_{DC}	Output Duty Cycle [6]	Across all settings in this table, V_T = 0V.	49.2	49.9	50.5	%

1. Both Tx and Rx are terminated (double-terminated) with CL= 2pF. This reduces amplitude by 50%. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in VCROSS for any particular system.
6. Measured from differential waveform.

2.4.5 CLKIN AC/DC Characteristics

Table 23. CLKIN AC/DC Characteristics

Symbol	Parameter	Conditions	Minimum [1]	Typical	Maximum	Unit
V_{CROSS}	Input Crossover Voltage	-	100	-	1400	mV
V_{SWING}	Input Swing	Differential value.	200	-	2000	mV
dv/dt	Input Slew Rate	Measured differentially. [2]	0.6	-	-	V/ns

1. See the PCIe Phase Jitter tables for values required for performance.
2. Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero-crossing.

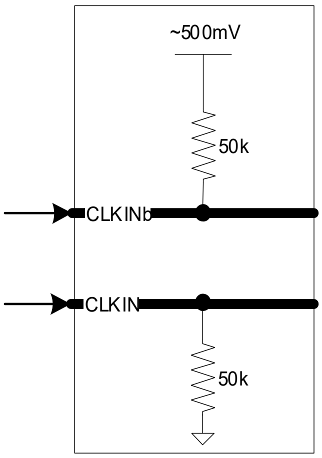


Figure 8. Clock Input Bias Network

2.4.6 Skew

Table 24. Output-to-Output and Input-to-Output Skew [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2]	Any two outputs in the same Bank.	-	20	45	ps
		Any two outputs regardless of Bank.	-	35	55	ps
t_{PD}	Input-to-Output Delay [3]	Clock in to any output. Double-terminated.	1.1	1.3	1.5	ns
		Clock in to any output. Source-terminated.	1.1	1.4	1.7	ns
Δt_{PD}	Input-to-Output Delay Variation [3]	A single device, over temperature and voltage.	-	1.2	2	ps/°C

1. See Test Loads.
2. This parameter is defined in accordance with JEDEC Standard 65.
3. Defined as the time between to output rising edge and the input rising edge that caused it.

2.4.7 I/O Signals

Table 25. I/O Electrical Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [2]	Bi-level, single-ended control inputs.	2	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [2]		-0.3	-	0.8	V
V_{IH}	Input High Voltage	Tri-level, single-ended control inputs, SADR_tri[1:0], CLKSEL_tri	2.4	-	VDD + 0.3	V
V_{IM}	Input Mid Voltage		1.2	-	1.8	V
V_{IL}	Input Low Voltage		-0.3	-	0.8	V
V_{OH}	Output High Voltage [2]	SBI_OUT, I_{OH} = -2mA.	2.4	3.2	VDD + 0.3	V
V_{OL}	Output Low Voltage [2]	SBI_OUT, LOSb, I_{OL} = 2mA.	-	0.1	0.4	V
I_{IL}	Input Leakage Current, V_{IN} = VDD	CLKIN0, CLKIN1	8	-	12	µA
		CLKIN0b, CLKIN1b	-1	-	2	
		Single-ended inputs, unless otherwise listed, when internal pull down is enabled. See the pin description of the specific device for details.	26	-	32	
		Single-ended inputs, unless otherwise listed, when internal pull down is disabled. See the pin description of the specific device for details.	-1	-	1	
		PWRGD_PWRDNb	1	-	5	
		SADR_tri[1:0], CLKSEL_tri	25	-	34	
I_{IL}	Input Leakage Current, V_{IN} = 0V	CLKIN0, CLKIN1	-1	-	1	µA
		CLKIN0b, CLKIN1b	-11	-	-6	
		Single-ended inputs, unless otherwise listed, when internal pull up is enabled. See the pin description of the specific device for details.	-32	-	-22	
		Single-ended inputs, unless otherwise listed, when internal pull up is disabled. See the pin description of the specific device for details.	-1	-	1	
		PWRGD_PWRDNb	-30	-26	-22	
		SADR_tri[1:0], CLKSEL_tri	-32	-	-22	
Rp	Pull-up CLK_IN	Value of internal pull-down resistor to ground on CLK_IN0, CLK_IN1	-	53	-	kΩ
	Pull-down, CLKINb	Value of internal pull-up resistor to 0.5V on CLK_INb0, CLK_INb1	-	57	-	
	Pull-up/Pull-down Resistor	Single-ended inputs.	-	120	-	
Zo	Output Impedance [3]	SBI_OUT pin.	-	49.9	-	Ω
		CLKn/CLKnb, ZOUTSEL = 1 (50Ω single-ended, 100Ω differential).	-	50	-	
		CLKn/CLKnb, ZOUTSEL = 0 (42.5Ω single-ended, 85Ω differential).	-	42.5	-	

1. For SCLK and SDATA, see the SMBus Electrical Characteristics table.
2. These values are compliant with JESD8C.01.
3. Measured from single-ended waveform.

2.4.8 Power Supply Current

Table 26. Power Supply Current [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCLK} [3]	V_{DDCLK} Output Supply Current – RC19216	100Ω impedance, source-terminated load, 100MHz.	-	139	151	mA
		100Ω impedance, receiver-terminated load, 100MHz.	-	181	197	
		100Ω impedance, source-terminated load at maximum output frequency.	-	243	263	
		100Ω impedance, receiver-terminated load at maximum output frequency.	-	292	316	
		85Ω impedance, source-terminated load, 100MHz.	-	162	176	
		85Ω impedance, receiver-terminated load, 100MHz.	-	174	188	
		85Ω impedance, source-terminated load at maximum output frequency.	-	280	303	
		85Ω impedance, receiver-terminated load at maximum output frequency.	-	300	325	
I_{DDCLK} [3]	V_{DDCLK} Output Supply Current – RC19208	100Ω impedance, source-terminated load, 100MHz.	-	53	59	mA
		100Ω impedance, receiver-terminated load, 100MHz.	-	89	97	
		100Ω impedance, source-terminated load at maximum output frequency.	-	95	103	
		100Ω impedance, receiver-terminated load at maximum output frequency.	-	143	155	
		85Ω impedance, source-terminated load, 100MHz.	-	76	83	
		85Ω impedance, receiver-terminated load, 100MHz.	-	105	114	
		85Ω impedance, source-terminated load at maximum output frequency.	-	111	120	
		85Ω impedance, receiver-terminated load at maximum output frequency.	-	158	171	
I_{DDCLK} [3]	V_{DDCLK} Output Supply Current – RC19204	100Ω impedance, source-terminated load, 100MHz.	-	24	30	mA
		100Ω impedance, receiver-terminated load at 100MHz.	-	44	50	
		100Ω impedance, source-terminated load at maximum output frequency.	-	55	60	
		100Ω impedance, receiver-terminated load at maximum output frequency.	-	82	87	
		85Ω impedance, source-terminated load, 100MHz.	-	28	33	
		85Ω impedance, receiver-terminated load, 100MHz.	-	45	51	
		85Ω impedance, source-terminated load at maximum output frequency.	-	64	69	
		85Ω impedance, receiver-terminated load at maximum output frequency.	-	89	94	

Table 26. Power Supply Current [1][2] (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{DDCLK} [3]	V_{DDCLK} Output Supply Current – RC19202	100Ω impedance, source-terminated load, 100MHz.	-	17	23	mA
		100Ω impedance, receiver-terminated load, 100MHz.	-	26	32	
		100Ω impedance, source-terminated load at maximum output frequency.	-	40	45	
		100Ω impedance, receiver-terminated load at maximum output frequency.	-	51	56	
		85Ω impedance, source-terminated load, 100MHz.	-	22	27	
		85Ω impedance, receiver-terminated load, 100MHz.	-	28	33	
		85Ω impedance, source-terminated load at maximum output frequency.	-	46	52	
		85Ω impedance, receiver-terminated load at maximum output frequency.	-	55	60	
I_{DDDINx}	V_{DDDINx} Operating Supply Current	Input channel not selected, per VDDIN pin.	-	1.4	2.0	mA
		Input channel selected, per VDDIN pin.	-	12	15	
I_{DDDIG}	V_{DDD} Operating Supply Current	-	-	0.5	1.0	
I_{DDA}	V_{DDA} Operating Supply Current	Core logic supply, independent of either bank.	-	1.2	2.0	
I_{DDCLK_PD}	V_{DDCLK_x} Power Down Current	PWRGD_PWRDNb = 0, (does not apply to RC19202)	-	1.4	2.0	mA
I_{DDDIG_PD}	V_{DDDIG} Power Down Current	PWRGD_PWRDNb = 0 (does not apply to RC19202)	-	0.8	2.0	
I_{DDA_PD}	V_{DDA}Power Down Current	PWRGD_PWRDNb = 0 (does not apply to RC19202)	-	1.1	2.0	

1. See Test Loads.
2. Output voltage set to 800mV.
3. All outputs running.

2.4.9 SMBus Electrical Characteristics

Table 27. SMBus DC Electrical Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	High-level Input Voltage for SMBCLK and SMBDAT	-	0.8 VDD	-	-	V
V_{IL}	Low-level Input Voltage for SMBCLK and SMBDAT	-	-	-	0.3 VDD	
V_{HYS}	Hysteresis of Schmitt Trigger Inputs	-	0.05 VDD	-	-	
V_{OL}	Low-level Output Voltage for SMBCLK and SMBDAT	I_{OL} = 46mA.	-	-	0	
I_{IN}	Input Leakage Current per Pin	-	[2]	-	[2]	µA
C_B	Capacitive Load for each Bus Line	-	-	-	400	pF

1. V_{OH} is governed by the V_{PUP}, the voltage rail to which the pull-up resistors are connected.
2. See I/O Electrical Characteristics table.

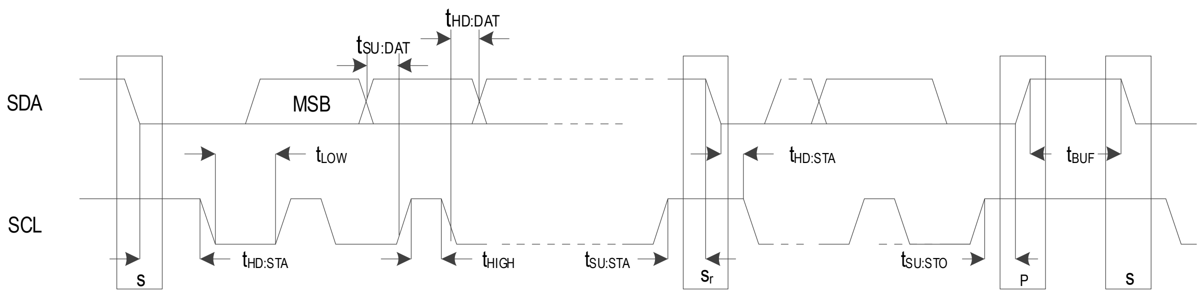


Figure 9. SMBus Slave Timing Diagram

Table 28. SMBus AC Electrical Characteristics

Symbol	Parameter	Conditions	100kHz Class		400kHz Class		Unit
			Minimum	Maximum	Minimum	Maximum	
f_{SMB}	SMBus Operating Frequency	[1]	10	100	10	400	kHz
t_{BUF}	Bus free time between STOP and START Condition	-	4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold Time after (REPEATED) START Condition	[2]	4	-	0.6	-	µs
$t_{SU:STA}$	REPEATED START Condition Setup Time	-	4.7	-	0.6	-	µs
$t_{SU:STO}$	STOP Condition Setup Time	-	4	-	0.6	-	µs
$t_{HD:DAT}$	Data Hold Time	[3]	300	-	300	-	ns
$t_{SU:DAT}$	Data Setup Time	-	250	-	100	-	ns
$t_{TIMEOUT}$	Detect SCL_SCLK Low Timeout	[4]	25	35	25	35	ms
$t_{TIMEOUT}$	Detect SDA_nCS Low Timeout	[5]	25	35	25	35	ms
t_{LOW}	Clock Low Period	-	4.7	-	1.3	-	µs
t_{HIGH}	Clock High Period	[6]	4	50	0.6	50	µs
$t_{LOW:SEXT}$	Cumulative Clock Low Extend Time (slave device)	[7]	N/A. The RC192xx does not extend the clock.				ms
$t_{LOW:MEXT}$	Cumulative Clock Low Extend Time (master device)	[8]	N/A. The RC192xx is not a master device.				ms
t_F	Clock/Data Fall Time	[9]	-	300	-	300	ns

Table 28. SMBus AC Electrical Characteristics (Cont.)

Symbol	Parameter	Conditions	100kHz Class		400kHz Class		Unit
			Minimum	Maximum	Minimum	Maximum	
t_R	Clock/Data Rise Time	[9]	-	1000	-	300	ns
t_{SPIKE}	Noise Spike Suppression Time	[10]	-	-	0	50	ns

1. Power must be applied and PWRGD_PWRDNb must be a 1 for the SMBus to be active.
2. A master shall not drive the clock at a frequency below the minimum f_{SMB}. Further, the operating clock frequency shall not be reduced below the minimum value of fSMB due to periodic clock extending by slave devices as defined in Section 5.3.3 of System Management Bus (SMBus) Specification, Version 3.1, dated 19 Mar 2018. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW: SEXT}$ and $t_{LOW: MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH,MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB,MIN} – t_{HIGH,MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100 µs in a non-periodic way.
3. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the VIH,MIN of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
4. Slave devices may have caused other slave devices to hold SDA low. This is the maximum time that a device can hold SMBDAT low after the master raises SMBCLK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
5. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT,MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT,MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT,MAX}$ or longer.
6. The device has the option of detecting a timeout if the SMBDATA pin is also low for this time.
7. $t_{HIGH,MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH,MAX}$.
8. $t_{LOW:MEXT}$ is the cumulative time a master device is allowed to extend its clock cycles within each byte of a message as defined from START-to-ACK, ACK-to-ACK, or ACK-to-STOP. It is possible that a slave device or another master will also extend the clock causing the combined clock low time to be greater than tLOW:MEXT on a given byte. This parameter is measured with a full speed slave device as the sole target of the master.
9. The rise and fall time measurement limits are defined as follows:
   Rise Time Limits: ($V_{IL:MAX}$ - 0.15 V) to ($V_{IH:MIN}$ + 0.15 V)
   Fall Time Limits: ($V_{IH:MIN}$ + 0.15 V) to ($V_{IL:MAX}$ - 0.15 V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

2.4.10 Side-band Interface

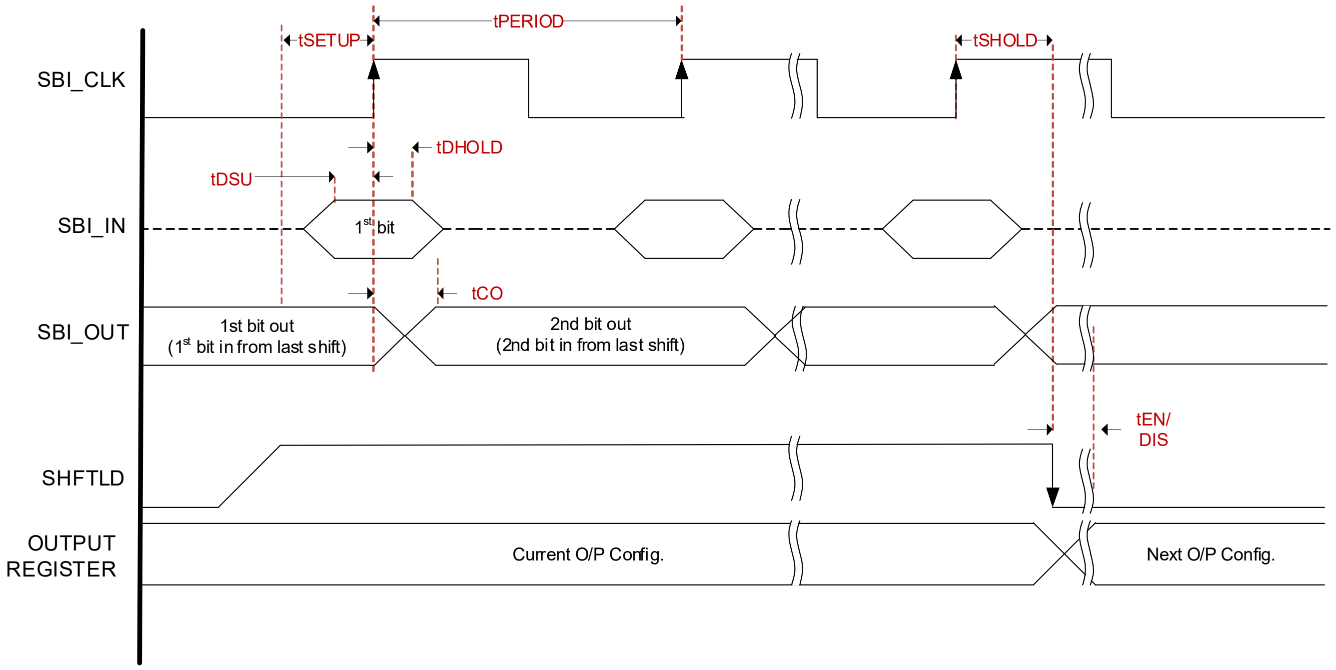


Figure 10. Side-Band Interface Timing

Table 29. Side-Band Interface AC/DC Electrical Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{PERIOD}	Clock Period	Clock period.	40	-	-	ns
t_{SETUP}	SHFT Setup Time to Clock	SHFT_LD# high to SBI_CLK rising edge.	10	-	-	ns
t_{DSU}	SBI_IN Setup Time	SBI_IN setup to SBI_CLK rising edge.	5	-	-	ns
t_{DHOLD}	SBI_IN Hold Time	SBI_IN hold after SBI_CLK rising edge.	2	-	-	ns
t_{CO}	SBI_CLK to SBI_OUT	SBI_CLK rising edge to SBI_OUT valid.	2	-	-	ns
t_{SHOLD}	SHFT Hold Time	SHFT_LD# hold (high) after SBI_CLK rising edge (SBI_CLK to SHFT_LD# falling edge).	10	-	-	ns
$t_{EN/DIS}$	Enable/Disable Time	Delay from SHFT_LD# falling edge to next output configuration taking effect. [1]	4	-	12	clocks
t_{SLEW}	Slew Rate	SBI_CLK input (between 20% and 80%). [2]	0.7	-	6	V/ns

1. Refers to the output frequency for the selected clock.
2. Control input must be monotonic from 20% to 80% of input swing.

3. Test Loads

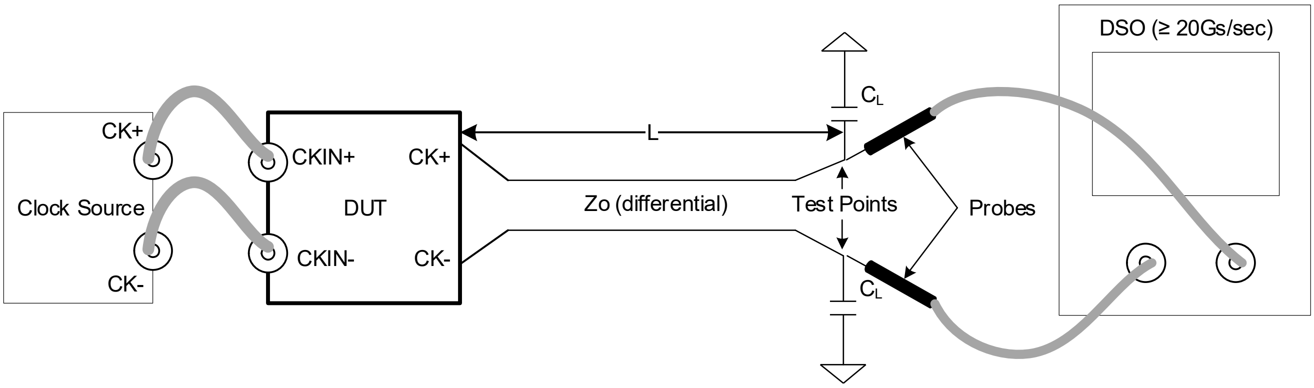


Figure 11. AC/DC Test Load for Differential Outputs (Standard PCIe Source-Terminated)

Table 30. Parameters for AC/DC Test Load (Standard PCIe Source-Terminated)

ZOUTSEL	Clock Source	Rs (ohms)	Zo (ohms)	L (cm)	C_L (pF)
0	SMA100B	Internal	85	25.4	2
1	SMA100B	Internal	100	25.4	2

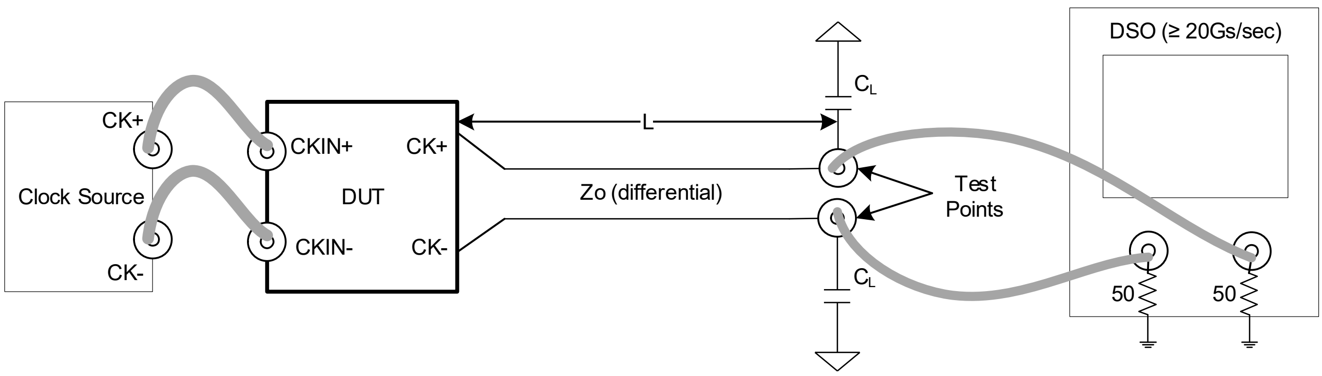


Figure 12. AC/DC Test Load for Differential Outputs (Double-Terminated)

Table 31. Parameters for AC/DC Test Load (Double-Terminated)

ZOUTSEL	Clock Source	Rs (ohms)	Zo (ohms)	L (cm)	C_L (pF)
0	SMA100B	Internal	85	25.4	2
1	SMA100B	Internal	100	25.4	2

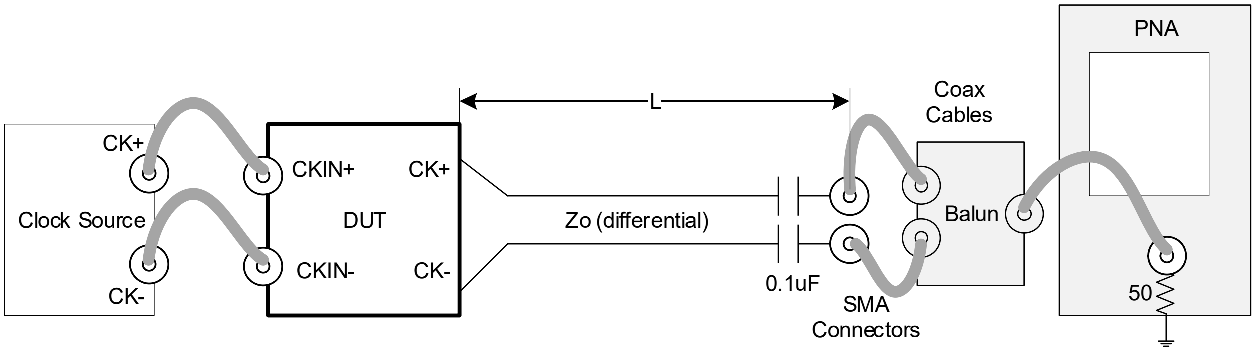


Figure 13. Test Load for PCIe Phase Jitter Measurements

Table 32. Parameters for PCIe Gen5 Jitter Measurement

ZOUTSEL	Clock Source	Rs (ohms)	Zo (ohms)	L (cm) [1]	C_L (pF)
0	SMA100B	Internal	85	25.4	2
1	SMA100B	Internal	100	25.4	2

1. PCIe Gen6 specifies L = 0cm for 32 and 64 GT/s. L = 25.4cm is more conservative.

4. General SMBus Serial Interface Information

4.1 How to Write

- Controller (host) sends a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) sends the byte count = X
- Renesas clock will **acknowledge**
- Controller (host) starts sending Byte **N through Byte N+X-1**
- Renesas clock will **acknowledge** each byte one at a time
- Controller (host) sends a stop bit

Index Block Write Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
Data Byte Count = X			
			ACK
Beginning Byte N		X Byte	
			ACK
O			
O			O
O			O
			O
Byte N + X - 1			
			ACK
P	stoP bit		

4.2 How to Read

- Controller (host) will send a start bit
- Controller (host) sends the write address
- Renesas clock will **acknowledge**
- Controller (host) sends the beginning byte Location = N
- Renesas clock will **acknowledge**
- Controller (host) will send a separate start bit
- Controller (host) sends the read address
- Renesas clock will **acknowledge**
- Renesas clock will send the data byte count = X
- Renesas clock sends Byte **N+X-1**
- Renesas clock sends **Byte L through Byte X (if X(H) was written to Byte 7)**
- Controller (host) will need to acknowledge each byte
- Controller (host) will send a not acknowledge bit
- Controller (host) will send a stop bit

Index Block Read Operation			
Controller (Host)			**Renesas**
T	starT bit		
Slave Address			
WR	WRite		
			ACK
Beginning Byte = N			
			ACK
RT	Repeat starT		
Slave Address			
RD	ReaD		
			ACK
			Data Byte Count=X
ACK			
		X Byte	Beginning Byte N
ACK			
			O
O			O
O			O
O			
			Byte N + X - 1
N	Not		
P	stoP bit		

4.3 Write Lock Functionality (RC19208, RC19216)

WRITE_LOCK	WRITE_LOCK RW1C	SMBus Write Protect
0	0	No
0	1	Yes
1	0	Yes
1	1	Yes

4.4 SMBus Address Selection (RC19208, RC19216)

Device	Address Selection		Binary Value								Hex Value	
	SADR_TRI1	SADR_TRI0	7	6	5	4	3	2	1	Rd/Wrt		
RC19216 RC19208	0	0	1	1	0	1	1	0	0	0	D8	Standard Addresses
		M	1	1	0	1	1	0	1	0	DA	
		1	1	1	0	1	1	1	1	0	DE	
	M	0	1	1	0	0	0	0	1	0	C2	
		M	1	1	0	0	0	1	0	0	C4	
		1	1	1	0	0	0	1	1	0	C6	
	1	0	1	1	0	0	1	0	1	0	CA	
		M	1	1	0	0	1	1	0	0	CC	
		1	1	1	0	0	1	1	1	0	CE	

4.5 SMBus Register Set (RC19208, RC19216)

Table 33. RC19208 and RC19216 SMBus Register Set

Byte	Register	Name	Bit	Type	Default	Description	Definition
0	RC19216 OUTPUT_ENABLE_0	CLK7_En	7	RW	1	Output Enable	0 = output is disabled (low/low) 1 = output is enabled
		CLK6_En	6	RW	1	Output Enable	
		CLK5_En	5	RW	1	Output Enable	
		CLK4_En	4	RW	1	Output Enable	
		CLK3_En	3	RW	1	Output Enable	
		CLK2_En	2	RW	1	Output Enable	
		CLK1_En	1	RW	1	Output Enable	
		CLK0_En	0	RW	1	Output Enable	
	RC19208 OUTPUT_ENABLE_0	CLK7_En	7	RW	1	Output Enable	0 = output is disabled (low/low) 1 = output is enabled
		CLK6_En	6	RW	0	Output Enable	
		CLK5_En	5	RW	0	Output Enable	
		CLK4_En	4	RW	1	Output Enable	
		CLK3_En	3	RW	1	Output Enable	
		CLK2_En	2	RW	0	Output Enable	
		CLK1_En	1	RW	0	Output Enable	
		CLK0_En	0	RW	1	Output Enable	

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
1	RC19216 OUTPUT_ENABLE_1	CLK15_En	7	RW	1	Output Enable	0 = output is disabled (low/low) 1 = output is enabled
		CLK14_En	6	RW	1	Output Enable	
		CLK13_En	5	RW	1	Output Enable	
		CLK12_En	4	RW	1	Output Enable	
		CLK11_En	3	RW	1	Output Enable	
		CLK10_En	2	RW	1	Output Enable	
		CLK9_En	1	RW	1	Output Enable	
		CLK8_En	0	RW	1	Output Enable	
	RC19208 OUTPUT_ENABLE_1	CLK15_En	7	RW	1	Output Enable	0 = output is disabled (low/low) 1 = output is enabled
		CLK14_En	6	RW	0	Output Enable	
		CLK13_En	5	RW	0	Output Enable	
		CLK12_En	4	RW	1	Output Enable	
		CLK11_En	3	RW	1	Output Enable	
		CLK10_En	2	RW	0	Output Enable	
		CLK9_En	1	RW	0	Output Enable	
		CLK8_En	0	RW	1	Output Enable	
2	RESERVED	RESERVED	7:0	RO	0	RESERVED	-
3	OEb_PIN_READBACK_1	RB_OEb_H	7	RO	pin	Status of OEb_H	0 = pin low 1 = pin high
		RB_OEb_G	6	RO	pin	Status of OEb_G	
		RB_OEb_F	5	RO	pin	Status of OEb_F	
		RB_OEb_E	4	RO	pin	Status of OEb_E	
		RB_OEb_D	3	RO	pin	Status of OEb_D	
		RB_OEb_C	2	RO	pin	Status of OEb_C	
		RB_OEb_B	1	RO	pin	Status of OEb_B	
		RB_OEb_A	0	RO	pin	Status of OEb_A	
4	SBEN_READBACK_ LOS_CFG	RESERVED	7	RW	1	RESERVED	0 = disable, 1 = enable
		RESERVED	6	RW	1	RESERVED	0 = disable, 1 = enable
		LOS1b_ACP_ENABLE	5	RW	1	Enable bank 1 Automatic Clock parking	0 = disable, 1 = enable
		LOS0b_ACP_ENABLE	4	RW	1	Enable bank 0 Automatic Clock parking	0 = disable, 1 = enable
		LOS1b_config	3	RW	1	LOSb config for bank 1	1 = LOS1b real time, 0 = LOS1b from RW1C sticky bit
		LOS0b_config	2	RW	1	LOSb config for bank 0	1 = LOS0b real time, 0 = LOS0b from RW1C sticky bit
		RESERVED	1	RW	0	RESERVED	-
		SBI_ENQ_Readback	0	RO	pin	Status of SBI_ENQ	0 = pin low 1 = pin high

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
5	VENDOR_REVISION_ID	RID	7:4	RO	0x0	Revision ID	-
		VID	3:0	RO	0x1	Vendor ID, Renesas/IDT/ICS	-
6	DEVICE_ID	DEVICE_ID	7:0	RO	See definition	Device ID	RC19216 = 0h30 RC19208 = 0h28
7	BYTE_COUNT	RESERVED	7:5	RW	0x0	RESERVED	-
		BC	4:0	RW	0x7	Writing to this register configures how many bytes will be read back	-
8	SBI_MASK_0	Mask7	7	RW	0	Masks off Side-band Disable	0 = Side-band may disable output 1 = Side-band may not disable output
		Mask6	6	RW	0	Masks off Side-band Disable	
		Mask5	5	RW	0	Masks off Side-band Disable	
		Mask4	4	RW	0	Masks off Side-band Disable	
		Mask	3	RW	0	Masks off Side-band Disable	
		Mask2	2	RW	0	Masks off Side-band Disable	
		Mask1	1	RW	0	Masks off Side-band Disable	
		Mask0	0	RW	0	Masks off Side-band Disable	
9	SBI_MASK_1	Mask15	7	RW	0	Masks off Side-band Disable	0 = Side-band may disable output 1 = Side-band may not disable output
		Mask14	6	RW	0	Masks off Side-band Disable	
		Mask13	5	RW	0	Masks off Side-band Disable	
		Mask2	4	RW	0	Masks off Side-band Disable	
		Mask11	3	RW	0	Masks off Side-band Disable	
		Mask10	2	RW	0	Masks off Side-band Disable	
		Mask9	1	RW	0	Masks off Side-band Disable	
		Mask8	0	RW	0	Masks off Side-band Disable	

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
10	CLOCK_SELECT	RESERVED	7:6	RW	0x0	RESERVED	-
		CLKSEL<1:0>	5:4	RW	0x0	Clock source select	00 = both bank from CLKIN0 01 = bank0 from CLKIN0, bank1 from CLKIN1 10 = invalid 11 = both bank from CLKIN1
		RESERVED	3:1	RW	0x0	RESERVED	-
		CLKSEL_CNTRL	0	RW	0x0	Select input control from pin or SMB	0 = use CLKSEL pin control 1 = use CLKSEL SMB control
11	SBI_READBACK_0	SBI_CLK7	7	RO	1'b1	Readback of Side-band Disable	0 = bit low 1 = bit high
		SBI_CLK6	6	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK5	5	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK4	4	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK3	3	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK2	2	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK1	1	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK0	0	RO	1'b1	Readback of Side-band Disable	
12	SBI_READBACK_1	SBI_CLK15	7	RO	1'b1	Readback of Side-band Disable	0 = bit low 1 = bit high
		SBI_CLK14	6	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK13	5	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK12	4	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK11	3	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK10	2	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK9	1	RO	1'b1	Readback of Side-band Disable	
		SBI_CLK8	0	RO	1'b1	Readback of Side-band Disable	
13	RESERVED	**RESERVED**	7:0	RW	0	**RESERVED**	-

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
14	RC19216 OEb_ASSIGNMENT_0	CLK7_OEb_En	7	RW	0	Output Enable by OEb_D	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK6_OEb_En	6	RW	1	Output Enable by OEb_D	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK5_OEb_En	5	RW	0	Output Enable by OEb_C	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK4_OEb_En	4	RW	1	Output Enable by OEb_C	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK3_OEb_En	3	RW	0	Output Enable by OEb_B	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK2_OEb_En	2	RW	1	Output Enable by OEb_B	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK1_OEb_En	1	RW	0	Output Enable by OEb_A	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK0_OEb_En	0	RW	1	Output Enable by OEb_A	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
14	RC19208 OEb_ASSIGNMENT_0	CLK7_OEb_En	7	RW	1	Output Enable by OEb_D	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK6_OEb_En	6	RW	0	Output Enable by OEb_D	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK5_OEb_En	5	RW	0	Output Enable by OEb_C	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK4_OEb_En	4	RW	1	Output Enable by OEb_C	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK3_OEb_En	3	RW	1	Output Enable by OEb_B	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK2_OEb_En	2	RW	0	Output Enable by OEb_B	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK1_OEb_En	1	RW	0	Output Enable by OEb_A	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK0_OEb_En	0	RW	1	Output Enable by OEb_A	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
15	RC19216 OEb_ASSIGNMENT_1	CLK15_OEb_En	7	RW	0	Output Enable by OEb_H	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK14_OEb_En	6	RW	1	Output Enable by OEb_H	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK13_OEb_En	5	RW	0	Output Enable by OEb_G	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK12_OEb_En	4	RW	1	Output Enable by OEb_G	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK11_OEb_En	3	RW	0	Output Enable by OEb_F	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK10_OEb_En	2	RW	1	Output Enable by OEb_F	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK9_OEb_En	1	RW	0	Output Enable by OEb_E	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK8_OEb_En	0	RW	1	Output Enable by OEb_E	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
15	RC19208 OEb_ASSIGNMENT_1	CLK15_OEb_En	7	RW	1	Output Enable by OEb_H	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK14_OEb_En	6	RW	0	Output Enable by OEb_H	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK13_OEb_En	5	RW	0	Output Enable by OEb_G	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK12_OEb_En	4	RW	1	Output Enable by OEb_G	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK11_OEb_En	3	RW	1	Output Enable by OEb_F	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK10_OEb_En	2	RW	0	Output Enable by OEb_F	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK9_OEb_En	1	RW	0	Output Enable by OEb_E	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
		CLK8_OEb_En	0	RW	0	Output Enable by OEb_E	0 = output stop by OEb is disabled 1 = output stop by OEb is enabled
16	RESERVED	RESERVED	7:0	RW	0	RESERVED	-
17	LPHCSL_AMP_CTRL	AMP_bank1	7:4	RW	0x7	Bank1 Output Amplitude Control	0.6V~1V 25mV/step Default = 0.8V
		AMP_bank0	3:0	RW	0x7	Bank0 Output Amplitude Control	0.6V~1V 25mV/step Default = 0.8V

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
18	PD_RESTORE_LOSb_ENABLE	**RESERVED**	7:4	RW	0	**RESERVED**	-
		PD_RESTOREb	3	RW	1	Save Configuration in Power Down	0 = Config Cleared 1 = Config Saved
		SDATA_time_out_enable	2	RW	1	Enable SMB time out monitoring of SDATA	0 = disable SDATA time out 1 = enable SDATA time out
		LOS1b_RB	1	RO	1'bX	Real-time read back of bank 1 loss detect block output	0 = LOS event detected 1 = NO LOS event detected.
		LOS0b_RB	0	RO	1'bX	Real-time read back of bank 0 loss detect block output	0 = LOS event detected 1 = NO LOS event detected.
19	RESERVED	RESERVED	7:0	RW	0x7	RESERVED	-
20	OUTPUT IMPEDANCE 7_0	CLK7_IMPEDANCE	7	RW	Latch	CLK7 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK6_IMPEDANCE	6	RW	Latch	CLK6 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK5_IMPEDANCE	5	RW	Latch	CLK5 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK4_IMPEDANCE	4	RW	Latch	CLK4 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK3_IMPEDANCE	3	RW	Latch	CLK3 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK2_IMPEDANCE	2	RW	Latch	CLK2 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK1_IMPEDANCE	1	RW	Latch	CLK1 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK0_IMPEDANCE	0	RW	Latch	CLK0 Impedance Select	0 = 85Ω 1 = 100Ω

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
21	OUTPUT IMPEDANCE 15_8	CLK15_IMPEDANCE	7	RW	Latch	CLK15 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK14_IMPEDANCE	6	RW	Latch	CLK14 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK13_IMPEDANCE	5	RW	Latch	CLK13 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK12_IMPEDANCE	4	RW	Latch	CLK12 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK11_IMPEDANCE	3	RW	Latch	CLK11 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK10_IMPEDANCE	2	RW	Latch	CLK10 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK9_IMPEDANCE	1	RW	Latch	CLK9 Impedance Select	0 = 85Ω 1 = 100Ω
		CLK8_IMPEDANCE	0	RW	Latch	CLK8 Impedance Select	0 = 85Ω 1 = 100Ω
22-34, 37	RESERVED	RESERVED	-	-	-	RESERVED	RESERVED
35	CLKIN CONFIG	RESERVED	7:4	RW	0	RESERVED	RESERVED
		AC_IN1	3	RW	0	Input is externally AC-coupled, enable receiver bias resistor for CLKIN1.	0 = DC coupled input 1 = AC coupled input
		Rx_TERM1	2	RW	0	Enable termination for CLKIN1	0 = input termination is disabled 1 =input termination is enabled
		AC_IN0	1	RW	0	input is AC coupled, enable receiver bias resistor for CLKIN0	0 = DC coupled input 1 = AC coupled input
		Rx_TERM0	0	RW	0	Input is externally AC-coupled, enable receiver bias resistor for CLKIN0.	0 = input termination is disabled 1 =input termination is enabled
38	WRITE_LOCK	RESERVED	7:1	RW	0	RESERVED	-
		WRITE_LOCK	0	RW	0	Non-clearable SMBus Write Lock bit. When written to one, the SMBus control registers cannot be written. This bit can only be cleared by cycling power.	0 = SMBus locked for writing if WRITE_LOCK_RW1C bit is set 1 = SMBus locked for writing

Table 33. RC19208 and RC19216 SMBus Register Set (Cont.)

Byte	Register	Name	Bit	Type	Default	Description	Definition
39	WRITE_LOCK_LOS_EVT	**RESERVED**	7:3	R/W 1C	0	**RESERVED**	-
		LOS1_EVT	2	R/W 1C	0	LOS1 Event Status When high, indicates that a LOS1 event was detected. Can be cleared by writing a 1 to it.	0 = No LOS1 event detected 1 = LOS1 event detected.
		LOS0_EVT	1	R/W 1C	0	LOS Event Status When high, indicates that a LOS event was detected. Can be cleared by writing a 1 to it.	0 = No LOS event detected 1 = LOS event detected.
		WRITE_LOCK_RW1C	0	R/W 1C	0	Clearable SMBus Write Lock bit When written to one, the SMBus control registers cannot be written. This bit may be cleared by writing a 1 to it.	0 = SMBus locked for writing if WRITE_LOCK is set 1 = SMBus locked for writing

5. Applications Information

5.1 Inputs, Outputs, and Output Enable Control

5.1.1 Recommendations for Unused Inputs and Outputs

5.1.1.1 Unused Differential CLKIN Inputs

The CLKIN/CLKINb inputs of the RC19xxx devices have internal bias networks that protect the devices from a floating input clock condition. For RC192xx multiplexers that use only one input clock, the unused input can be left open. Renesas recommends that no trace be attached to unused CLKIN pins.

5.1.1.2 Unused Single-ended Control Inputs

The single-ended control pins have internal pull-up and/or internal pull-down resistors and do not require external resistors. They can be left floating if the default pin state is the desired state. If external resistors are needed to change the pin state or are desired for design robustness, 10kohm is the recommended value.

5.1.1.3 Unused Differential CLK Outputs

All unused CLK outputs can be left floating. Renesas recommends that no trace be attached to unused CLK outputs. While not required (but is highly recommended), the best design practice is to disable unused CLK outputs.

5.1.1.4 Unused SMBus Clock and Data Pins

If the SMBus interface is not used, the clock and data pins must be pulled high with an external resistor. The two pins can share a resistor if there is no possibility of using the SMBus interface for debug purposes. If the interface may be used for debug, separate resistors should be used. 10kohm is the recommended value.

5.1.2 Differential CLKIN Configurations

The RC19xxx clock input buffer supports four configurations:

- Direct connection to HCSL-level inputs
- Direct connection to LVDS-level inputs with *external* termination resistor
- Internal self-bias circuit for applications that *externally* AC-couple the input clock
  This feature is enabled by the **AC_IN** bit.
- Internal pull-down resistors (Rp) to terminate the clock input at the receiver.
  This feature is enabled by the **Rx_TERM** bit.

Devices with multiple input clocks have individual AC_IN and Rx_TERM configuration bits for each input. The internal input clock terminations prevent reflections and are useful for non-PCIe applications, where the frequency and transmission line length vary from the 100MHz PCIe standard.

Figure 14 through Figure 17 illustrate the above items.

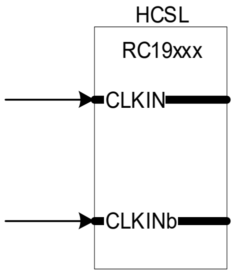


Figure 14. HCSL Input Levels (PCIe Standard)

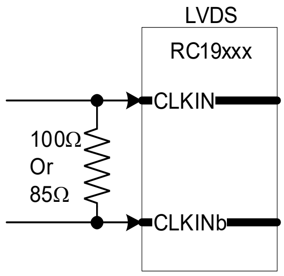


Figure 15. LVDS Input Levels

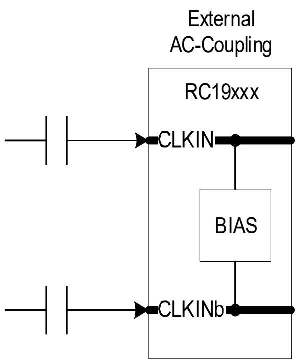


Figure 16. External AC-Coupling

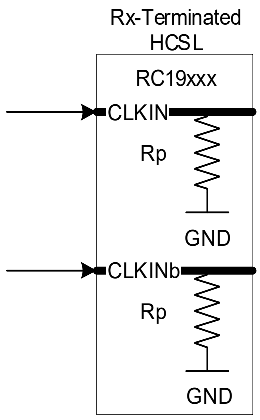


Figure 17. Receiver Termination

5.1.3 Differential CLK Output Configurations

5.1.3.1 Direct-Coupled HCSL Loads

The RC19xxx LP-HCSL CLK outputs have internal source terminations and directly drive industry-standard HCSL-level inputs with no external components. They support both 85ohm and 100ohm differential impedances. The CLK outputs can also drive receiver-terminated HCSL loads. The combination of source termination and receiver termination results in a double-terminated load. When double-terminated, the CLK output swing will be half of the source-terminated values.

5.1.3.2 AC-Coupled non-HCSL Loads

The RC19xxx CLK output can directly drive AC-coupling capacitors without any termination components. The clock input side of the AC-coupling capacitor may require an input-dependent bias network (BN). For examples of terminating the RC19xxx CLK outputs to other logic families such as LVDS, LVPECL, or CML, see AN-891.

Figure 18 to Figure 20 show the various CLK output configurations.

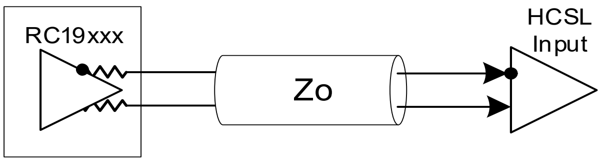


Figure 18. Direct-Coupled Source-Terminated HCSL

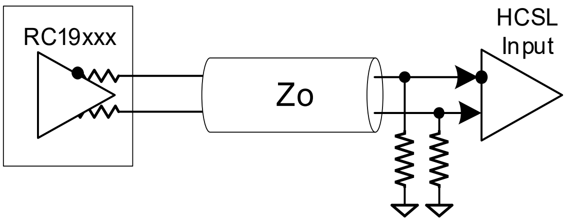


Figure 19. Direct-Coupled Double-Terminated HCSL

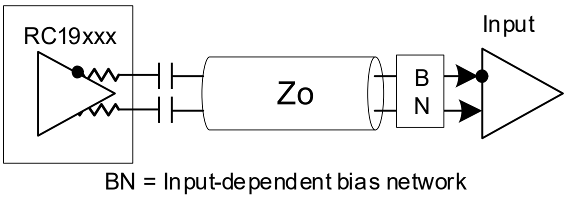


Figure 20. AC-Coupled

5.2 Power Down Tolerant Pins

Pins that are Power Down Tolerant (PDT) can be driven by voltages as high as the normal VDD of the chip, even though VDD is not present (the device is not powered). There will be no ill effects to the device and it will power up normally. This feature supports disaggregation, where the RC19xxx may be on one circuit board and devices that interface with it are on other boards. These boards may power up at different times, driving pins on the RC19xxx before it has received power. Figure 21 provides an example of a PDT call-out in a data sheet.

5.3 Flexible Startup Sequencing

RC19216 Pin Descriptions

Pin Number		Pin Name	Type	Description
A	1	GNDSUB	GND	Ground pin for substrate.
A	2	CLKb0	O, DIF	Complementary clock output.
A	3	CLK0	O, DIF	True clock output.
A	4	CLKb1	O, DIF	Complementary clock output.
A	5	CLK1	O, DIF	True clock output.
A	6	CLKb2	O, DIF	Complementary clock output.
A	7	CLK2	O, DIF	True clock output.
A	8	CLKb3	O, DIF	Complementary clock output.
A	9	CLK3	O, DIF	True clock output.
A	10	CLKb4	O, DIF	Complementary clock output.
A	11	CLK4	O, DIF	True clock output.
A	12	CLKb5	O, DIF	Complementary clock output.

Figure 21. Example: Power Down Tolerant Pin Descriptions

RC19xxx devices support Flexible Startup Sequencing (FSS). FSS allows application of CLKIN at different times in the device/system startup sequence. FSS is an additional feature that helps the system designer manage the impact of disaggregation. Table 34 shows the supported sequences; that is, the RC19xxx devices can have CLKIN running before VDD is applied, and can have VDD applied and sit for extended periods with no input clock.

Table 34. Flexible Startup Sequences

VDD	PWRGD_PWRDNb	CLKIN/CLKINb
Not present	X	Running
		Floating
		Low/Low
Present	0 or 1	Running
		Floating
		Low/Low

5.4 Loss of Signal and Automatic Clock Parking

The RC19 devices have a Loss of Signal (LOS) circuit to detect the presence or absence of an input clock. The LOS circuit drives the open-drain LOSb pin (the "b" suffix indicates "bar", or active-low) and sets the LOS_EVT bit in the SMBus register space. Figure 22 shows the LOSb de-assertion timing for the 20-output buffers and all RC192xx clock multiplexers. LOSb on the 20-output buffers and all RC192xx multiplexers defaults to low at power up. CLKIN is represented differentially in Figure 23.

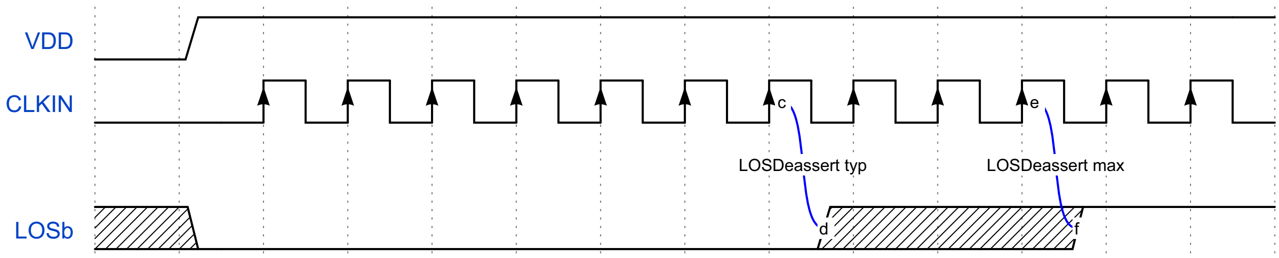


Figure 22. LOSb De-assert Timing RC192xx Devices

Note: The LOSb pin monitors the *selected input clock* in the RC192xx multiplexers.

The following diagram shows the LOSb assertion sequence when the CLKIN is lost. It also shows the Automatic Clock Parking (ACP) circuit bring the inputs to a Low/Low state after an LOS event. For exact timing, see Electrical Characteristics.

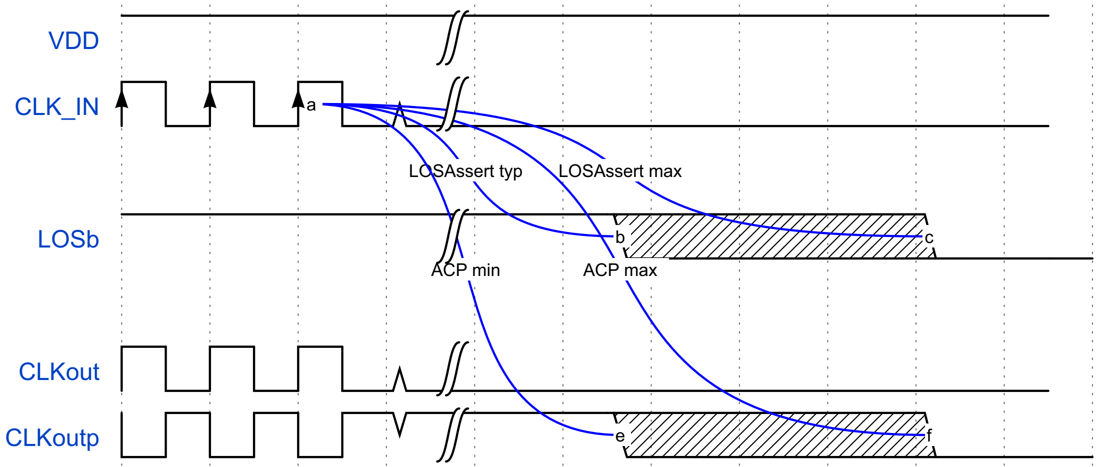


Figure 23. LOSb Assert Timing

5.5 Output Enable Control

The RC19xxx buffer/mux family provides three mechanisms to enable or disable clock outputs. All three mechanisms start and stop the output clocks in a synchronous, glitch-free manner. A clock output is enabled only when all three mechanisms indicate “enabled.” The following sections describe the three mechanisms.

5.5.1 SMBus Output Enable Bits

The RC19xxx Clock buffer/multiplexer family has a traditional SMBus output enable bit for each output. The power-up default is 1, or enabled. Changing this bit to a 0 disables the output to a low/low state. The transitions between the enable and disable states are glitch-free in both directions.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

5.5.2 Output Enable (OEb) Pins

The OEb (Note: the “b” suffix indicates “bar”, or active-low) pins on the RC19xxx family provide flexible CLKREQb functionality for PCIe slots and/or banked OE control for ‘motherboard-down’ devices (depending on the device). If the OEb pin is low the controlled output is enabled. If the OEb pin is high, the controlled output is disabled to a low/low state. All OEb pins enable and disable the controlled outputs in a glitch-free, synchronous manner.

Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

5.6 RC192xx Clock Multiplexer OEb Pins

The RC192xx Clock Multiplexers have a maximum of 8 OEb pins. Additionally, the SBI_ENQ pin multiplexes 4 OEb pins with the Side Band Interface (SBI) on the RC19216 and RC19208. The RC19204 and RC19202 do not have an SBI and use an SMBENb latch to multiplex 2 OEb pins with an SMBus interface. Details are provided in Table 35 and Table 36.

Table 35. RC19216 and RC19208 OEb Mapping

<table>
<tr><th>Pin Name</th><th>SBI_ENQ Pin</th><th>RC19216 Default Pin Function</th><th>RC19216 Optional Pin Function[1]</th><th>RC19208 Default Pin Function</th><th>RC19208 Optional Pin Function</th></tr>
<tr><td>OEb_A</td><td>X</td><td>CLK0 OEb</td><td>CLK1 OEb</td><td>CLK0 OE</td><td rowspan="12">N/A</td></tr>
<tr><td>OEb_B</td><td>X</td><td>CLK2 OEb</td><td>CLK3 OEb</td><td>CLK3 OE</td></tr>
<tr><td>OEb_C</td><td>X</td><td>CLK4 OEb</td><td>CLK5 OEb</td><td>CLK4 OE</td></tr>
<tr><td rowspan="2">OEb_D_SBI_CLK</td><td>0 (Disabled)</td><td>CLK6 OEb</td><td>CLK7 OEb</td><td>CLK7 OE</td></tr>
<tr><td>1 (Enabled)</td><td>SBI_CLK</td><td>N/A</td><td>SBI_CLK</td></tr>
<tr><td rowspan="2">OEb_E_SBI_IN</td><td>0 (Disabled)</td><td>CLK8 OEb</td><td>CLK9 OEb</td><td>CLK8 OE</td></tr>
<tr><td>1 (Enabled)</td><td>SBI_IN</td><td>-</td><td>SBI_IN</td></tr>
<tr><td>OEb_F</td><td>X</td><td>CLK10 OEb</td><td>CLK11 OEb</td><td>CLK11 OE</td></tr>
<tr><td rowspan="2">OEb_G_SHFT_LDb</td><td>0 (Disabled)</td><td>CLK12 OEb</td><td>CLK13 OEb</td><td>CLK12 OE</td></tr>
<tr><td>1 (Enabled)</td><td>SHFT_LDb</td><td>-</td><td>SHFT_LDb</td></tr>
<tr><td rowspan="2">OEb_H_SBI_OUT</td><td>0 (Disabled)</td><td>CLK14 OEb</td><td>CLK15 OEb</td><td>CLK15 OE</td></tr>
<tr><td>1 (Enabled)</td><td>SBI_OUT</td><td>-</td><td>SBI_OUT</td></tr>
</table>

1. See the OEb_ASSIGNMENT registers in the RC192xx data sheet.

Table 36. RC19204 and RC19202 OEb Mapping

<table>
<tr><th>Pin Name</th><th>SBI_ENQ Pin</th><th>RC19204 Default Pin Function</th><th>RC19204 Optional Pin Function[1]</th><th>RC19202 Default Pin Function</th><th>RC19202 Optional Pin Function</th></tr>
<tr><td>OEb_B</td><td rowspan="4">N/A</td><td>CLK3 OEb</td><td>CLK5 OEb</td><td>-</td><td>-</td></tr>
<tr><td>OEb_C</td><td>CLK5 OEb</td><td>-</td><td>CLK5 OEb</td><td>-</td></tr>
<tr><td>OEb_F</td><td>CLK10 OEb</td><td>-</td><td>CLK10 OEb</td><td>-</td></tr>
<tr><td>OEb_G</td><td>CLK12 OEb</td><td>CLK10 OEb</td><td>-</td><td>-</td></tr>
</table>

1. See the OEb_ASSIGNMENT registers in the RC192xx data sheet.

5.6.1 Side-Band Interface (SBI)

This section does not apply to the RC19202 because it does not have a side-band interface.

SMBus output enable bits and OEb pins are the traditional methods for enabling and disabling clocks. The 2-wire SMBus interface can enable or disable all clock outputs in a device. This pin efficiency is its advantage. The SMBus interface's main drawback is that it is a relatively slow physical interface, whose software is one of several routines running on an often overtaxed micro-controller. OEb pins are real-time and are ideally dedicated to an individual clock output. As buffers grow in output count, dedicated OEb pins become problematic for two reasons. First, the clock buffer pin count becomes much larger than it otherwise would be, resulting in a larger package. Second, unless the OEb pins are used for CLKREQ# functionality, the number of pins that need to be controlled outgrows the GPIO pins of an FPGA or micro-controller.

A third output enable/disable mechanism, the Side-Band Interface (SBI), addresses these issues. The SBI is a simple 3-wire (4-wire if the SBI_OUT pin is used) interface that can control all outputs across multiple devices. The SBI is only slightly less pin efficient than the SMBus, and is much more pin efficient than a dedicated OEb pins per output. It is protocol-free, hardware-oriented and runs at speeds up to 25MHz, much faster than SMBus.

Another SBI advantage is that it is active after power is applied and before PWRGD is asserted. External logic can disable specific outputs before PWRGD is asserted, and can then dynamically adjust the output run state during device operation. The SBI can make the adjustments much more rapidly than SMBus.

The RC192xx 4-wire SBI interface consists of the SBI_IN, SBI_CLK, SHFT_LDb, and SBI_OUT pins. The RC192xx SBI is enabled by strapping the SBI_ENQ pin to 1. When enabled, various OEb pins become the SBI interface. The exact pins that are multiplexed vary with device.

The SBI_ENQ pin strap takes effect as soon as power is applied and is not dependent on the assertion of PWRGD_PWRDNb to 1. Because of this, the SBI_ENQ must be static and cannot change once power is applied. If SBI_ENQ is 0 when power is applied, the SBI is disabled and has no impact on enabling or disabling outputs.

The SBI consists of a shift register, an SMBus readback register (of the shift register contents), and an SMBus MASK register. The SBI shifts a bit stream containing the enable/disable pattern into the shift register. A 1 enables an output and a 0 disables an output. All shift-register bits default to 1 at power up, indicating an enabled state. This means that the SBI can be used to disable outputs at power up because the default is enabled.

The SBI has its own SBI_CLK and does not need a running CLKIN to shift in an enable/disable pattern. This provides utmost flexibility for setting output run state before the SMBus becomes active or before the CLKIN is applied. When the SBI indicates enabled, the standard SMBus output enable bits and OEb pins can control the outputs.

The SBI feeds common output enable/disable synchronization logic ensuring glitch-free enable and disable of outputs. Note: The glitch-free synchronization logic requires the CLKIN be running to enable or disable the outputs with this mechanism.

If the application does not use the SBI, the SBI_ENQ pin can be tied to 0, and the entire SBI has no impact on enabling or disabling clock outputs.

The SBI Mask registers allow the user to block the disable function of the SBI via the SMBus. The SBI Mask registers default to 0 at power-up, allowing the SBI shift register bits to disable their respective output. After asserting the PWRGD_PWRDNb pin high, the SMBus is active and the SBI mask registers can be configured via SMBus to mask off (block) the SBI disable function. In other words, setting and SBI Mask bit to 1 forces the SBI to always indicate "enable" for the respective output. This allows the user to prevent the SBI from accidentally turning off a critical output.

The RC192xx clock multiplexer provides the ability to read back the SBI shift register contents via the SMBus. The SMBus readback values update on each falling edge of SHFT_LDb. Note: The SBI shift register can only be read using the SMBus; the SMBus *cannot* be used to load it.

Figure 24 shows the high-level functional description of SBI.

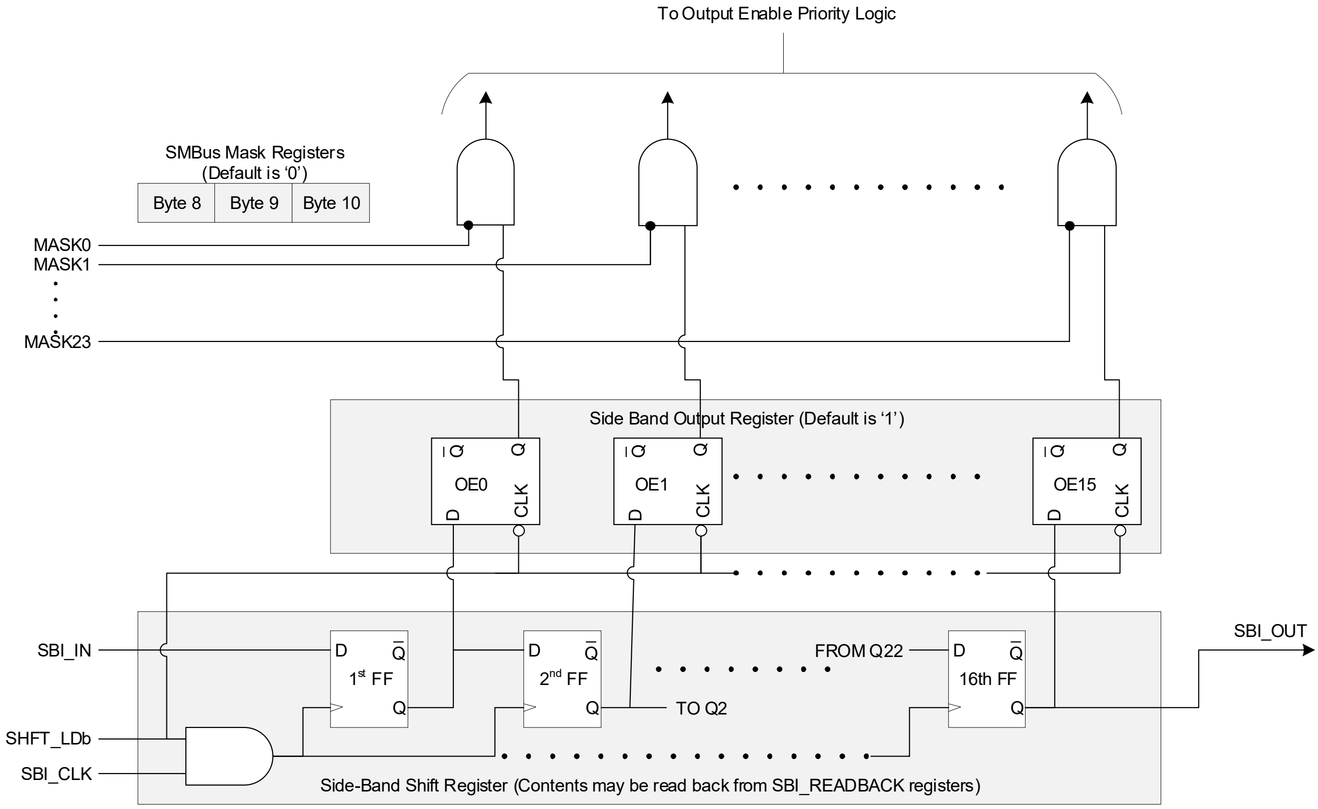


Figure 24. Side-band Interface High-Level Functional Diagram (RC192xx shown)

5.6.1.1 Using the SBI

Using the RC19216 as an example, we see the SBI shift order follows the order of the SMBus enable bits. in Byte [1:0] as shown in Figure 25. The first bit shifted in would be the output enable/disable bit for the CLK15, which is in Byte 1 bit 7. The last bit shifted in would be the output enable/disable for CLK0, which is in Byte 0, bit 0.

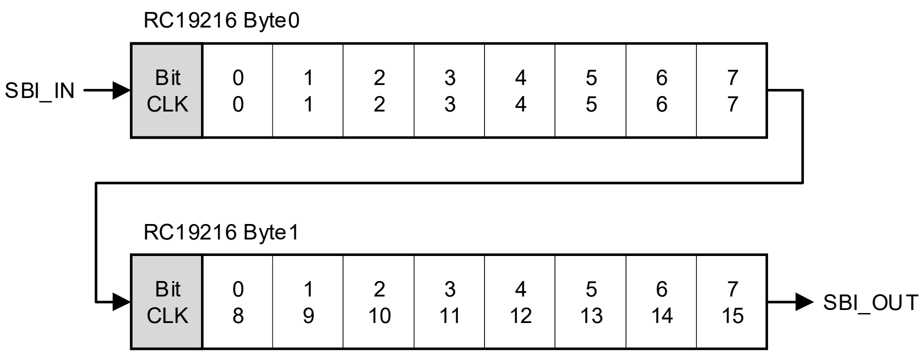


Figure 25. RC19216 Side Band Shift Order

Figure 26 shows the Side Band Shift Order for the RC19208 clock multiplexer. Notice that the Side Band Shift Count is equal to the number of outputs in each device.

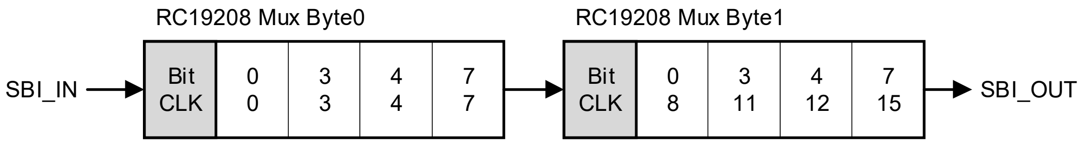


Figure 26. RC19208 Side Band Shift Order

5.6.1.2 Side-Band Interface Timing

Figure 27 shows the basic timing of the side-band interface. The SHFT_LDb pin goes high to enable the SBI_CLK input. Next, the rising edge of SBI_CLK clocks SBI_IN data into the shift register. After the 16th clock (assuming the RC19216, stop the SBI_CLK low and drive the SHFT_LDB pin low. The falling edge of SHFT_LDb latches the shift register contents to the output control register, disabling or enabling the outputs. Always shift the complete set of bits into the shift register to control the outputs. For the Side-Band Interface AC/DC Electrical Characteristics, see Table 29.

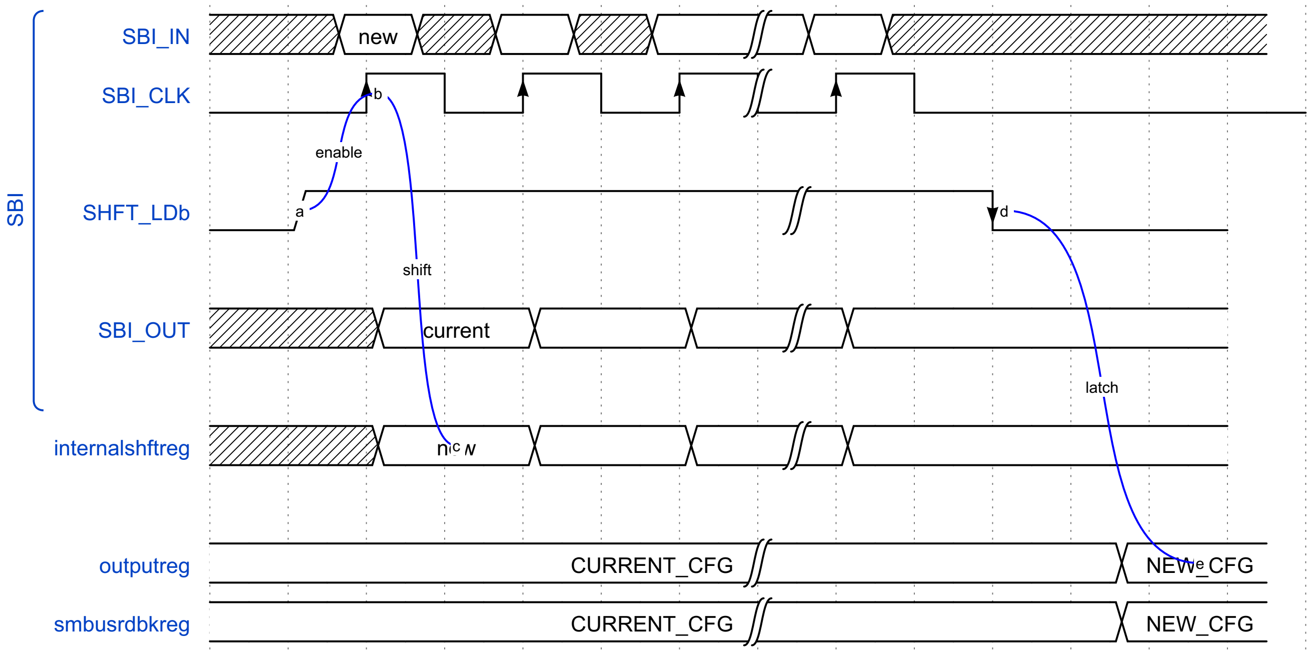


Figure 27. Side-Band Interface Functional Timing

5.6.1.3 Side-Band Interface Connection Topologies

The RC192xx mux devices support two SBI connection topologies: star and daisy chain. In a star topology, multiple devices can share the SBI_CLK and SBI_IN pins. In this topology, each RC192xx has a dedicated SHFT_LDb pin. In a daisy-chain topology, the SBI_OUT of one device connects to the SBI_IN of a downstream device. When using the daisy-chain topology, the user must shift a complete set of bits for the combined devices. Two daisy-chained RC19216 devices require shifting of 2 × 16 = 32 bits. An RC19216 followed by an RC19208 would require shifting 8 + 16 = 24 bits. When the SHFT_LDb pin is low, the SBI interface ignores any activity on the SBI_CLK and SBI_IN pins.

Figure 28 shows a star topology connection for the RC192xx SBI interface. The star topology allows independent configuration of each device. For the RC19216, this means shifting 16 bits at a time. A disadvantage is that a separate SHFT_LDb pin is required for each device. The star topology allows additional devices to be controlled at the cost of an additional GPIO per device.

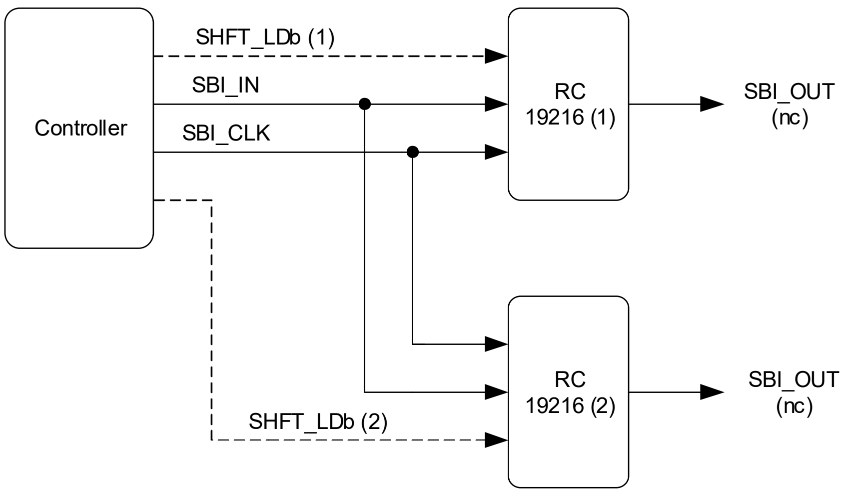


Figure 28. Side-Band Interface Star Topology

The daisy-chain topology allows configuration of any number of devices with only three signals from the SBI controller. It uses the SBI_OUT pin of one device to drive the SBI_IN pin of the next device in the daisy chain. Users must take care to shift the proper number of bits in this configuration. For the example shown in Figure 29, the SBI bit stream consists of 48 bits.

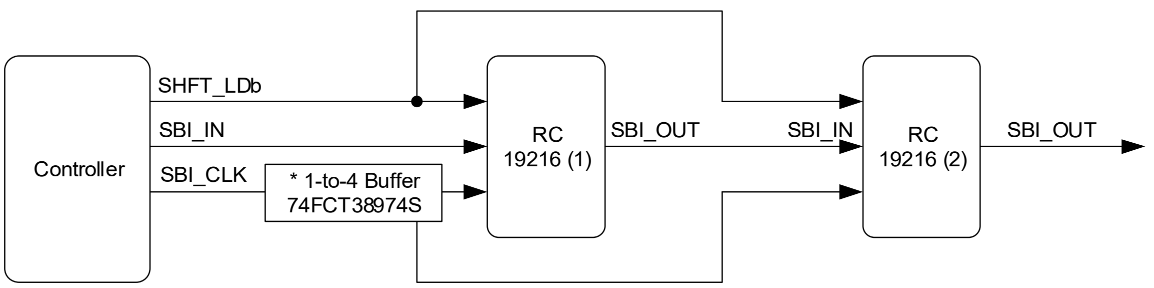


Figure 29. Side-Band Interface Daisy-Chain Topology

* *Note*: The 74FCT3807S is DC-coupled, which allows the SBI_CLK to start and stop with the data transfer. If an AC-coupled buffer is used, SBI_CLK must be continuously free-running. DC-coupled buffers are recommended.

5.6.2 Output Enable/Disable Priority

The RC192xx output enable/disable priority is an “AND” function of all enable methods. This means that the SMBus output enable bit AND the OEb pin (if present/assigned) AND the SBI must indicate that the output is enabled in order for the output to be enabled. A logical representation of the priority logic is shown in Figure 30.

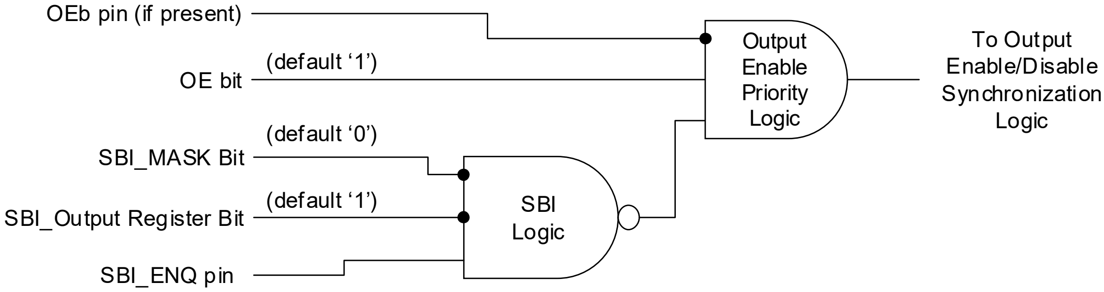
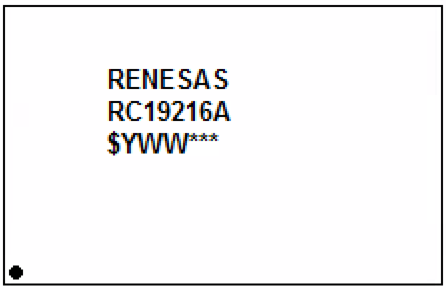


Figure 30. Output Enable/Disable Priority (Logical)

6. Package Outline Drawings

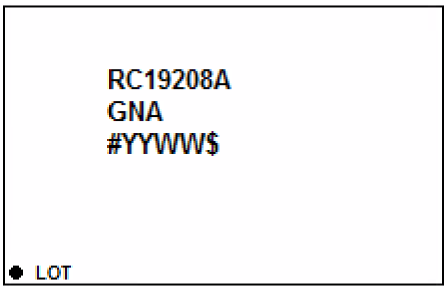
The package outline drawings are located at the end of this document and are accessible from the Renesas website (see Ordering Information for POD links). The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagrams



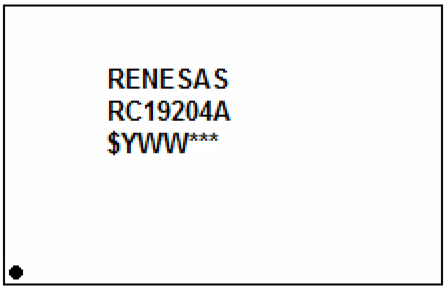
RC19216 80-VFQFPN

- Lines 2 is the part number
- Line 3:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.



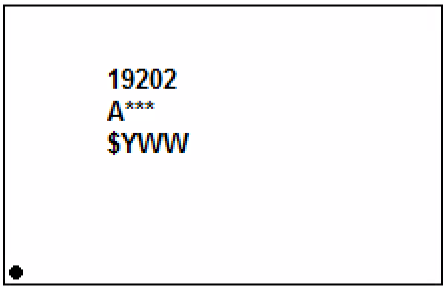
RC19208 48-VFQFPN

- Lines 1 and 2 are the part number
- Line 3:
  - “#” denotes the stepping number.
  - “YYWW” denotes the last two digits of the year and the work week the part was assembled.
  - “$” denotes the mark code.



RC19204 28-VFQFPN

- Line 2 is the part number
- Line 3:
  - "#" denotes the stepping number.
  - "YYWW" denotes the last two digits of the year and the work week the part was assembled.
  - "$" denotes the mark code.



RC19202 20-VFQFPN

- Line 1 is the part number
- Line 2 "A" is part of the part number and "***" is the sequential code
- Line 3:
  - "$" denotes the mark location code.
  - "YWW" denotes the assembly date: "Y" is the last digit of the year and "WW" are the last two digits of work week.

8. Ordering Information

Part Number	Carrier Type	Number of Outputs	Output Impedance	Package	Temp. Range
RC19216AGN6#BD0	Tray	16	Selectable	6 × 6 mm, 0.5mm pitch 80-VFQFPN	-40 to +105°C
RC19216AGN6#KD0	Tape and Reel (EIA-481-D)				
RC19208AGNA#BB0	Tray	8	Selectable	6 × 6 mm, 0.4mm pitch 48-VFQFPN	-40 to +105°C
RC19208AGNA#KB0	Tape and Reel (EIA-481-D)				
RC19204AGNL#BB0	Tray	4	Selectable	4 × 4 mm, 0.4mm pitch 28-VFQFPN	-40 to +105°C
RC19204AGNL#KB0	Tape and Reel (EIA-481-D)				
RC19202AGNT#BD0	Tray	2	Selectable	3 × 3 mm, 0.4mm pitch 20-VFQFPN	-40 to +105°C
RC19202AGNT#KD0	Tape and Reel (EIA-481-D)				

9. Revision History

Revision	Date	Description
1.09	Mar 31, 2025	▪ Added PU to the Type information for the OEb_H_SBI_OUT pin in Table 1 and Table 2
1.08	Jul 30, 2024	▪ Updated references to the 6 x 6 package to 80-VFQFPN. No technical changes were made
1.07	Jul 26, 2023	▪ Updated title in Figure 22 ▪ Updated text to RC192xx(A) from RC19xxxA or RC190xxA in section 5.6.1 ▪ Updated Figure 24 ▪ Updated text in section 5.6.1.2 ▪ Updated part numbers in section 5.6.1.3 ▪ Removed references and figures that referenced RC190xx.
1.06	Jun 29, 2023	▪ Updated RC19216 information for pins E11, K11, L2, L6, and L11 in Table 1 ▪ Updated RC19208 information for pins 16, 18, 24, 25, 34, 35, 43, and 44 in Table 2 ▪ Updated RC19204 information for pins 9, 16, 19, and 25 in Table 3 ▪ Updated RC19202 information for pins 12 and 15 in Table 4
1.05	Nov 17, 2022	▪ Changed t_{SLEW} to 6 from 4 in Table 29
1.04	Oct 17, 2022	▪ Completed a minor, non-technical update to Table 19 ▪ Completed other minor changes
1.03	July 6, 2022	▪ Corrected labeling of multiplexer inputs in all block diagrams
1.02	May 4, 2022	▪ Updated the marking information for the RC19202
1.01	Apr 11, 2022	▪ Updated Pin Type of all pins beginning with OEb to properly indicate internal pull-down (PD) resistors ▪ Minor reformatting of Pin Descriptions to reduce required space in Pin Description tables and to provide consistency across devices
1.00	Feb 24, 2022	Initial release.

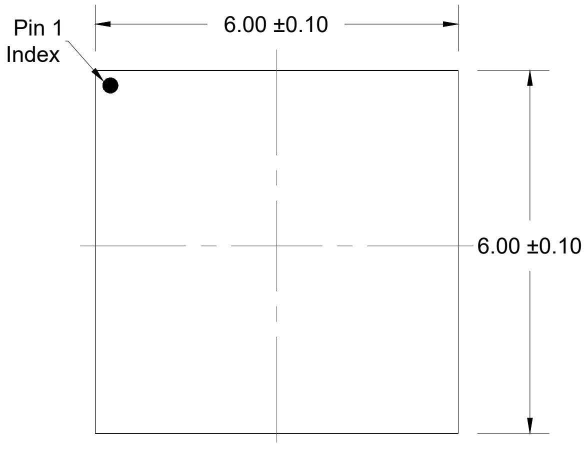
RENESAS

Package Outline Drawing

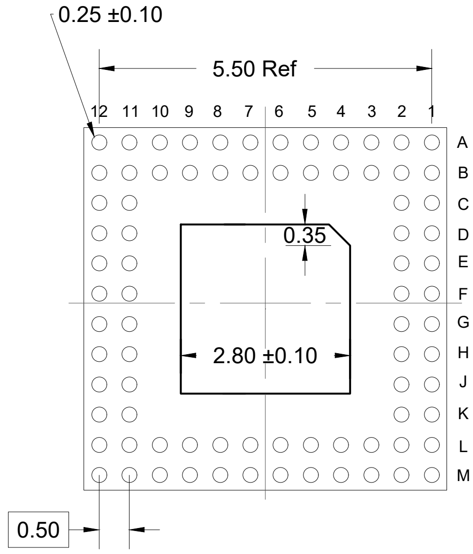
Package Code: NHG80P1

80-VFQFPN 6.00 x 6.00 x 0.80 mm Body 0.50mm Pitch

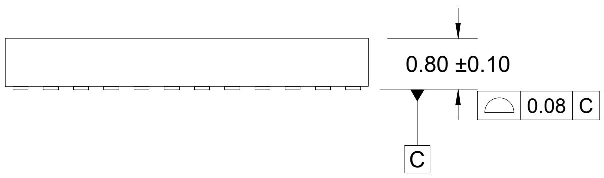
PSC-4496-01, Rev 01, Created: Jan 19, 2022



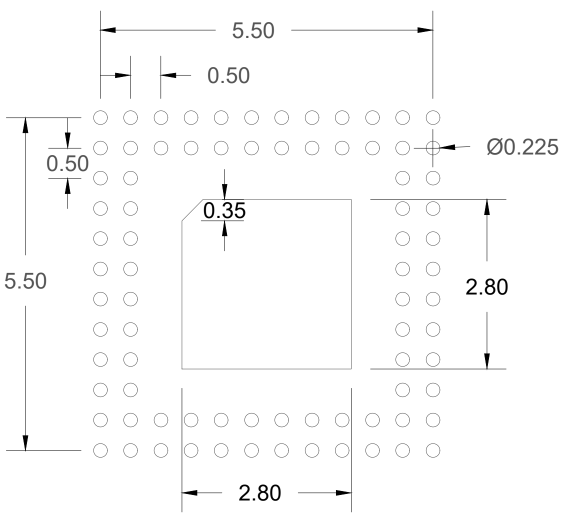
TOP VIEW



BOTTOM VIEW



SIDE VIEW

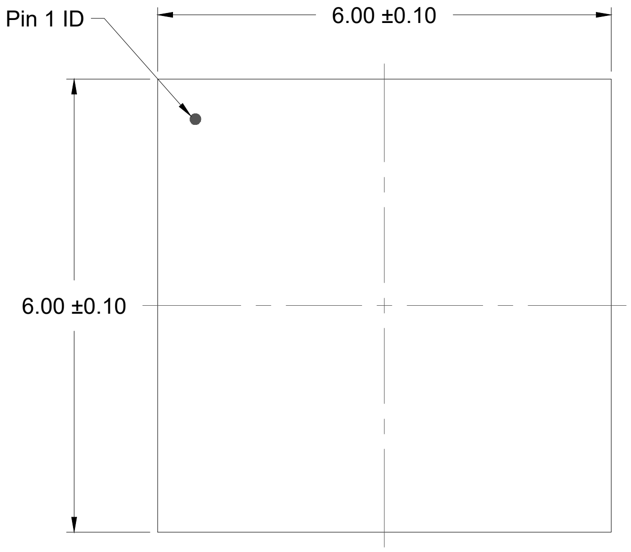


RECOMMENDED LAND PATTERN

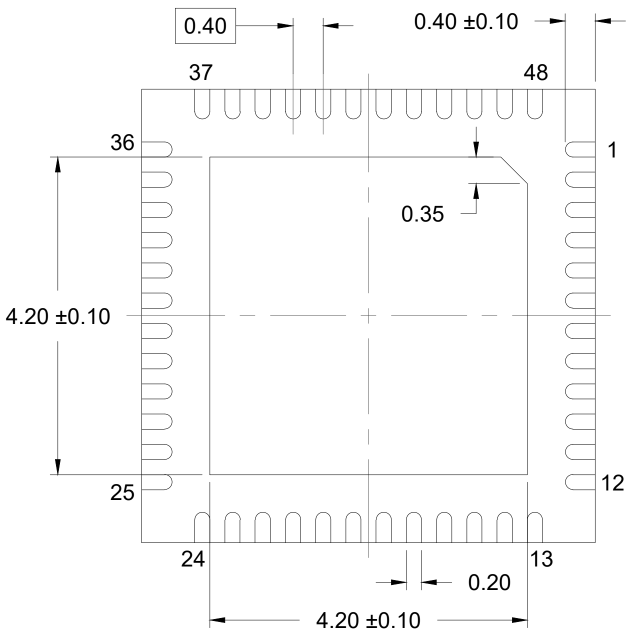
(PCB Top View, NSMD Design)

NOTES:

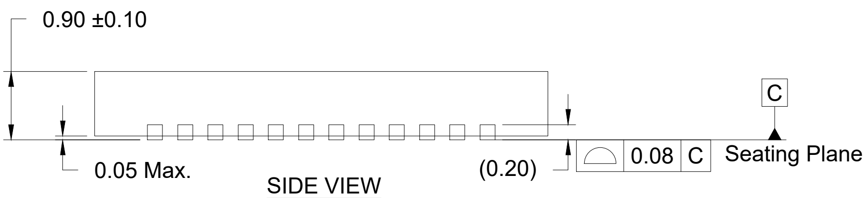
1. JEDEC compatible
2. All dimensions are in mm and angles are in degrees
3. Use ±0.05 mm tolerance for all other dimensions
4. Numbers in ( ) are for reference only



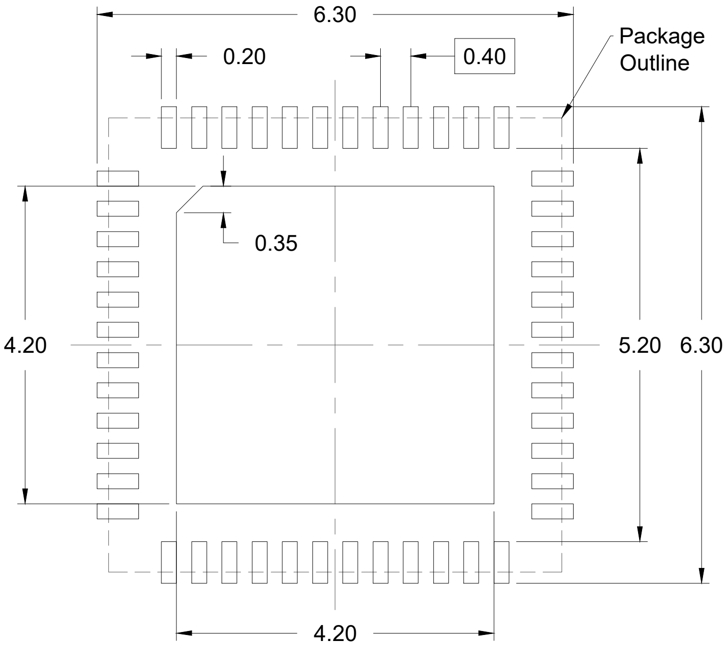
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

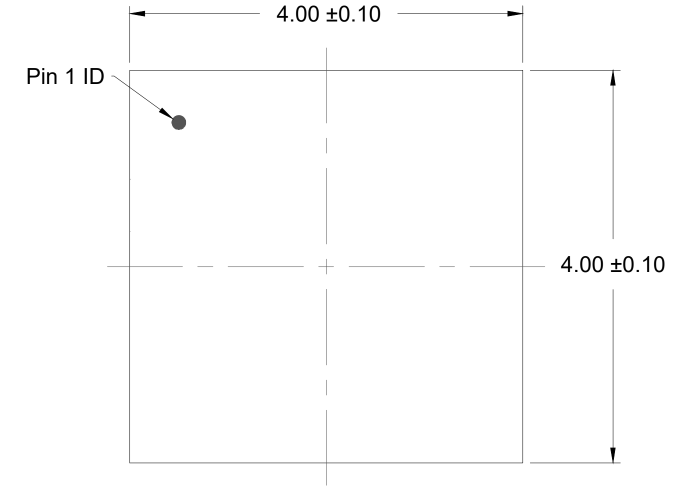
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

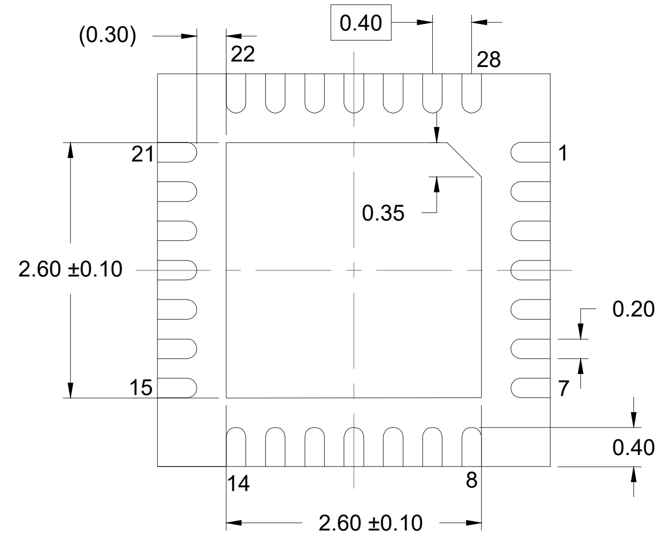
Package Code:NDG28P1

28-VFQFPN 4.0 x 4.0 x 0.9 mm Body, 0.4mm Pitch

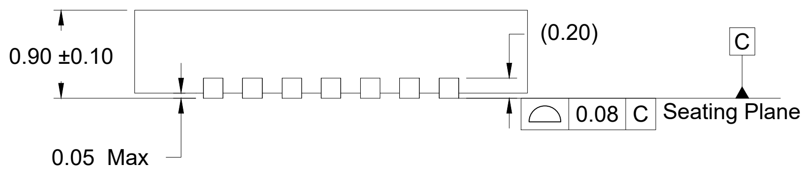
PSC-4249-01, Revision: 02, Date Created: Feb 06, 2024



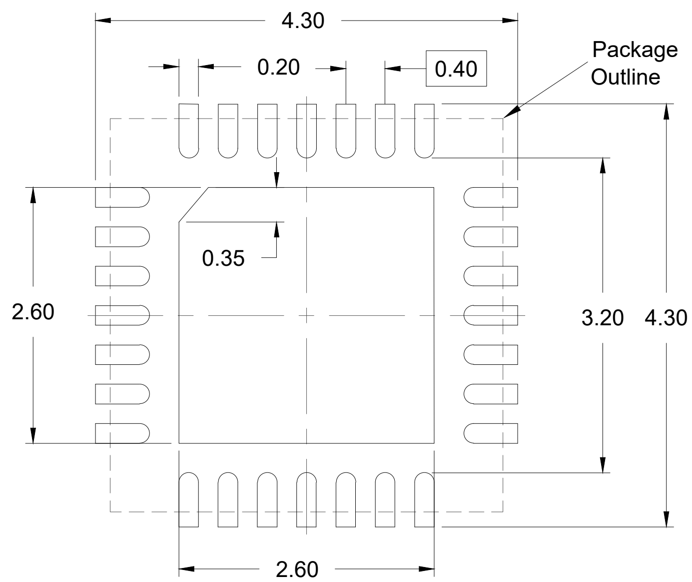
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

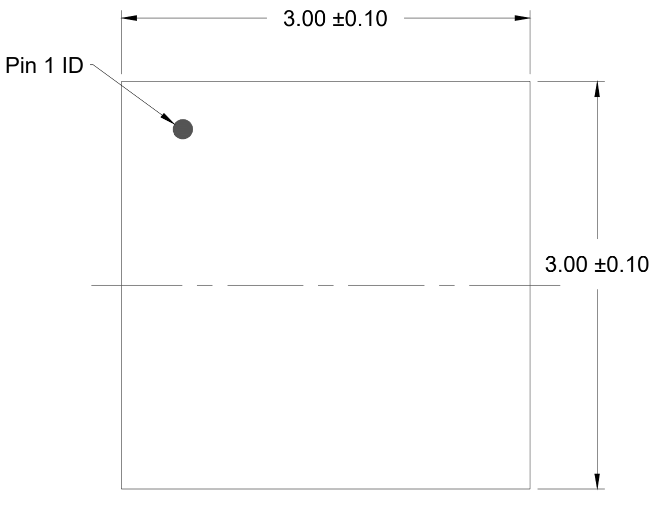
(PCB Top View, NSMD Design)

NOTES:

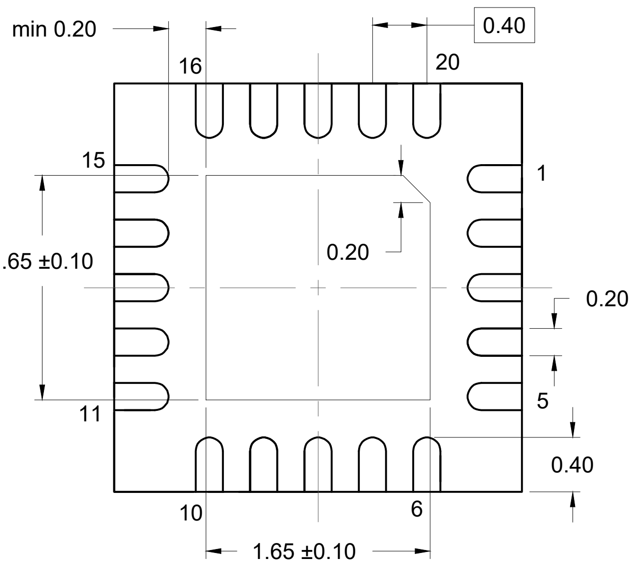
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

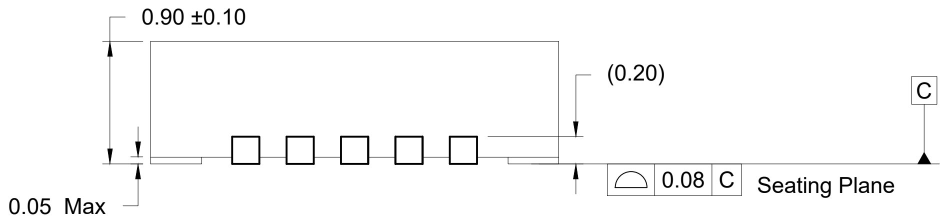
Package Code:NDG20P2
20-VFQFPN 3.0 x 3.0 x 0.9 mm Body, 0.4mm Pitch
PSC-4179-02, Revision: 02, Date Created: Jan 29, 2024



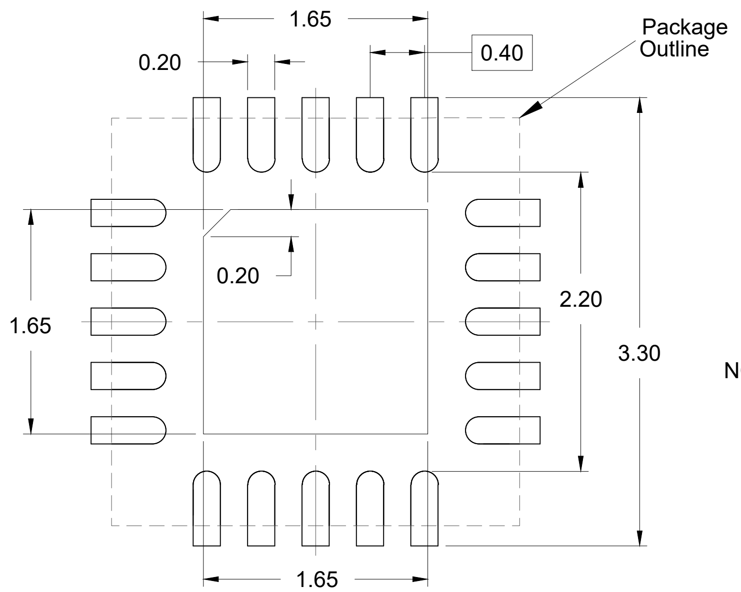
TOP VIEW



BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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