RC2121xA

AutoClock Automotive Programmable Clock Generator Family

The RC2121xA family of devices are high-performance programmable clock generators with added diagnostic features to support automotive applications. The RC2121xA has the following characteristics:

- ISO9001 compliant
- AEC-Q100 qualified
- -40° to +105°C (Grade 2 equivalent) operation
- PPAP support

Diagnostic Features

- Redundant crystal option with automatic switching
- Cyclic Redundancy Check (CRC) monitors for OTP image, I^2C accesses, and register contents
- Output frequency monitors
- APLL loss-of-lock monitor
- Power-on self-test
- Programmable GPIO to indicate internal error or fault conditions

Applications

- Infotainment
- Gateway
- Domain controller
- Zone controller

Features

- 169fs RMS phase jitter (12kHz to 20MHz, 156.25MHz)
- PCIe® Gen6 Common Clock (CC) 27fs RMS
- PCIe SRIS and SRNS support
- 1kHz to 650MHz (differential) and 1kHz to 200MHz (single-ended) outputs
- LVCMOS, LVDS, or Low-Power HCSL output types with simple AC-coupling to LVPECL and CML. LP-HCSL integrates terminations.
- Seven programmable General Purpose Input-Outputs (GPIO)
- 1MHz I^2C serial port
- Multiple configurations can be stored in internal One-Time Programmable (OTP) memory.
- 1.8V and/or 3.3V operation
- Package options:
  - 12 differential or 24 single-ended outputs
    - 6 × 6 × 0.75 mm, 48-QFN package
    - RC21211: Single crystal
    - RC21212: Dual crystal
  - 8 differential or 16 single-ended outputs
    - 5 × 5 × 0.75 mm, 40-QFN package
    - RC21213: Single crystal
    - RC21214: Dual crystal

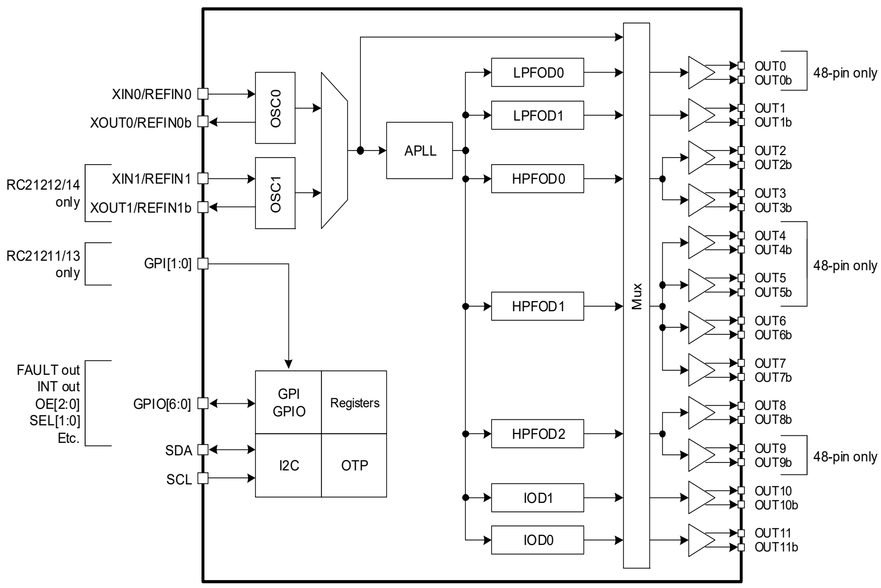

Figure 1. RC2121xA Block Diagram

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1. Pin Information

1.1 Pin Assignments

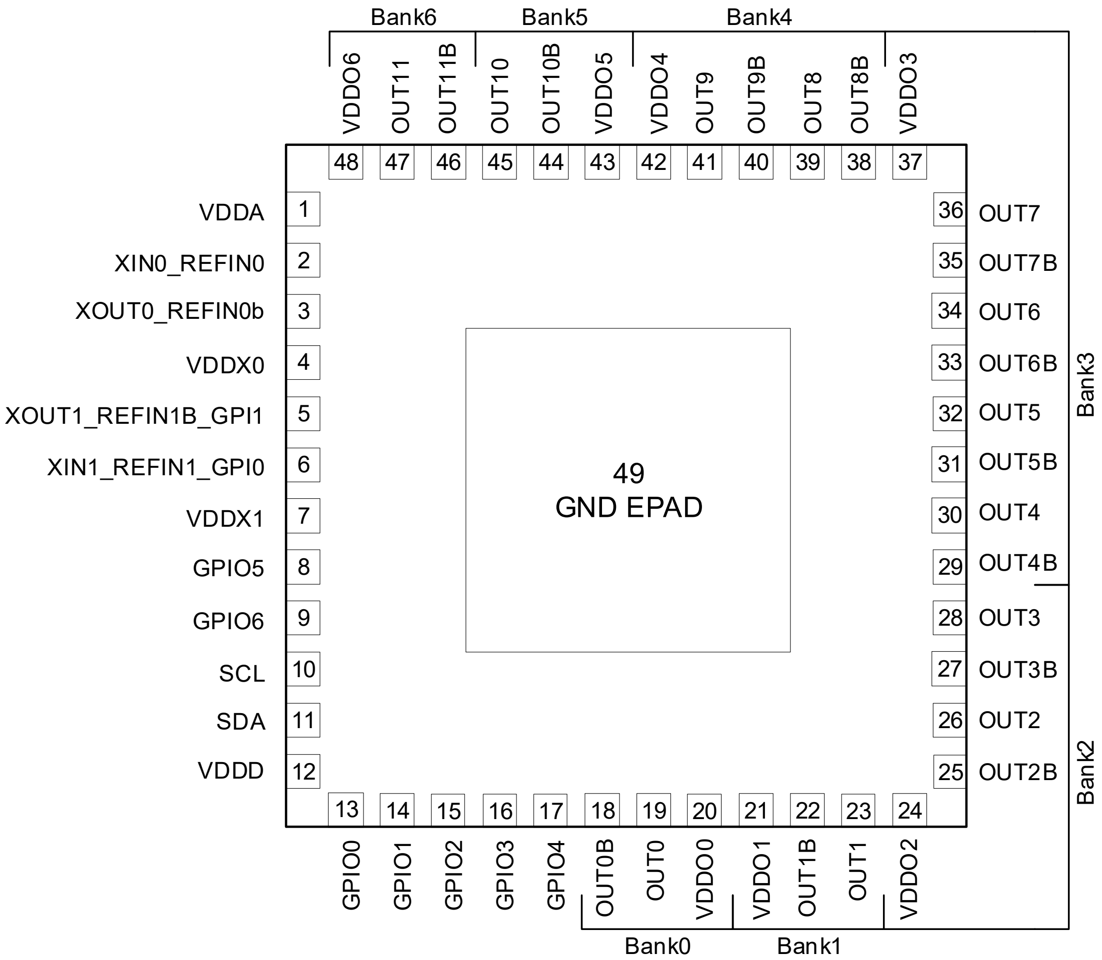


Figure 2. 48-QFN (6 × 6) Pin Assignments – Top View

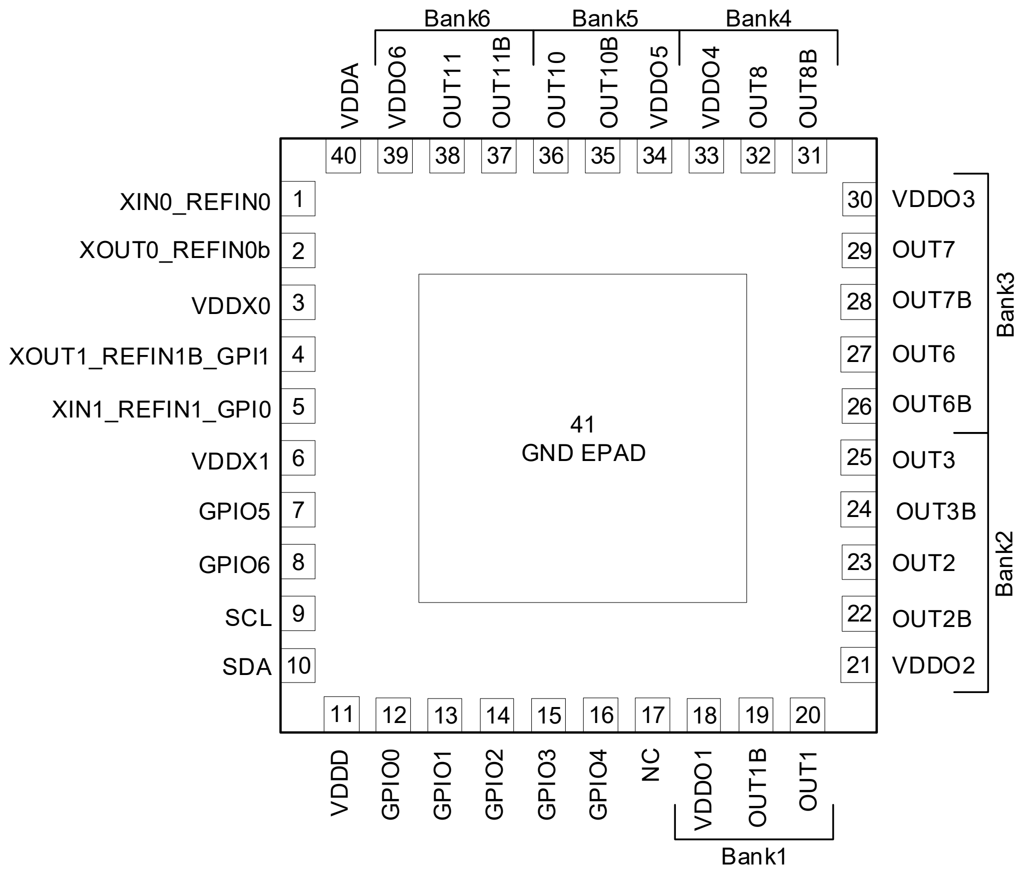


Figure 3. 40-QFN (5 × 5) Pin Assignments – Top View

1.2 Pin Descriptions

Table 1. Pin Descriptions

48-QFN	40-QFN	Name	Type	Description
1	40	VDDA	Power	Power supply for analog, 1.8/3.3V supported
2	1	XIN0_REFIN0	I	Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input. For more information, see Crystal/Reference Input.
3	2	XOUT0_REFIN0b	I/O	Crystal Output or differential reference clock negative input. This pin should be connected to a crystal. If an oscillator is connected to XIN0_REFIN0, then this pin must be left unconnected.
4	3	VDDX0	Power	Power supply for Crystal oscillator. 1.8/3.3V supported
5	4	XOUT1_REFIN1b_GPI1	I/O	For single crystal variants: General purpose input. Not 3.3V tolerant. For dual crystal variants: Crystal Output or differential reference clock negative input. This pin should be connected to a crystal. If an oscillator is connected to XIN1_REFIN1, then this pin must be left unconnected.
6	5	XIN1_REFIN1_GPI0	I	For single crystal variants: General purpose input. Not 3.3V tolerant. For dual crystal variants: Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input. For more information, see Crystal/Reference Input.
7	6	VDDX1	Power	Power supply for Crystal oscillator. 1.8/3.3V supported
8	7	GPIO5	I/O	General purpose input/open drain output, 3.3V tolerant.

Table 1. Pin Descriptions (Cont.)

48-QFN	40-QFN	Name	Type	Description
9	8	GPIO6	I/O	General purpose input/open drain output, 3.3V tolerant.
10	9	SCL	I	I^2C interface clock input, 3.3V tolerant.
11	10	SDA	I/O	I^2C interface bi-directional data in open-drain mode, 3.3V tolerant.
12	11	VDDD	Power	Power supply for digital core. 1.8/3.3V supported When programming the OTP, this supply must be 3.3V.
13	12	GPIO0	I/O	General purpose input/output, **not** 3.3V tolerant.
14	13	GPIO1	I/O	General purpose input/open drain output, 3.3V tolerant.
15	14	GPIO2	I/O	General purpose input/open drain output, 3.3V tolerant.
16	15	GPIO3	I/O	General purpose input/open drain output, 3.3V tolerant.
17	16	GPIO4	I/O	General purpose input/open drain output, 3.3V tolerant.
NA	17	NC		No Connect
18	NA	nOUT0b	O	Output Clock 0 negative.
19	NA	OUT0	O	Output Clock 0 positive.
20	NA	VDDO0	Power	Supply voltage for output bank 0 and LPFOD 0. 1.8/3.3V supported
21	18	VDDO1	Power	Supply voltage for output bank 1 and LPFOD 1 (on 40 pin variant also LPFOD 0). 1.8/3.3V supported.
22	19	OUT1b	O	Output Clock 1 negative.
23	20	OUT1	O	Output Clock 1 positive
24	21	VDDO2	Power	Supply voltage for output bank 2 and HPFOD 0. 1.8/3.3V supported
25	22	OUT2b	O	Output Clock 2 negative.
26	23	OUT2	O	Output Clock 2 positive.
27	24	OUT3b	O	Output Clock 3 negative.
28	25	OUT3	O	Output Clock 3 positive.
29	NA	OUT4b	O	Output Clock 4 negative.
30	NA	OUT4	O	Output Clock 4 positive.
31	NA	OUT5b	O	Output Clock 5 negative.
32	NA	OUT5	O	Output Clock 5 positive.
33	26	OUT6b	O	Output Clock 6 negative.
34	27	OUT6	O	Output Clock 6 positive.
35	28	OUT7b	O	Output Clock 7 negative.
36	29	OUT7	O	Output Clock 7 positive.
37	30	VDDO3	Power	Supply voltage for output bank 3 and HPFOD 1. 1.8/3.3V supported
38	31	OUT8b	O	Output Clock 8 negative
39	32	OUT8	O	Output Clock 8 positive.
40	NA	OUT9b	O	Output Clock 9 negative.
41	NA	OUT9	O	Output Clock 9 positive.
42	33	VDDO4	Power	Supply voltage for output bank 4 and HPFOD 2. 1.8/3.3V supported.
43	34	VDDO5	Power	Supply voltage for output bank 5 and IOD 1. 1.8/3.3V supported

Table 1. Pin Descriptions (Cont.)

48-QFN	40-QFN	Name	Type	Description
44	35	OUT10b	O	Output Clock 10 negative.
45	36	OUT10	O	Output Clock 10 positive.
46	37	OUT11b	O	Output Clock 11 negative.
47	38	OUT11	O	Output Clock 11 positive.
48	39	VDDO6	Power	Supply voltage for output bank 6 and IOD 0. 1.8/3.3V supported
EPAD	EPAD	GND	Power	Ground. EPAD must be connected to ground before any VDD is applied.

1.3 Pin Characteristics

Table 2. Pin Characteristics

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Unit
C_{IN}	Input Capacitance	XIN0_REFIN0 [1]	7	7.9	9	pF
		XOUT_REFIN0b [1]	1.5	2.6	4	
		XIN1_REFIN1_GPI0 [2]	7	7.9	9	
		XOUT1_REFIN1b_GPI1 [2]	1	2.4	3.5	
		SCL, SDA	1	2.3	3.5	
		GPIO[0]	4.5	5.8	7.5	
		GPIO[1:4]	2	3.4	5.5	
R_{PULLUP}	Input Pull-up Resistor	All pins with internal pull up capability	49.6	53	58.1	kΩ
$R_{PULLDOWN}$	Input Pull-down Resistor	All pins with internal pull down capability	49.7	53	58.3	kΩ
Z_{OUTDC}	LP-HCSL Single-ended Output Impedance, VDDO = 3.3V	50Ω single-ended (100Ω differential).	42	47.5	63	Ω
		42.5Ω single-ended (85Ω differential).	35	41.2	55	
		17Ω single-ended (33Ω differential).	12	18.2	28	
	LP-HCSL Single-ended Output Impedance, VDDO = 1.8V.	50Ω single-ended (100Ω differential).	49	53.1	71	Ω
		42.5Ω single-ended (85Ω differential).	42	46.5	73	
		17Ω single-ended (33Ω differential).	20	22.1	41	
	LVCMOS Output Impedance	V_{DDO} = 3.3V	14	19.1	23	Ω
		V_{DDO} = 1.8V	15	20	27	

1. When used as a reference clock input.
2. When used as a reference clock input or a General Purpose Input (GPI).

2. Specifications

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC2121xA at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

2.1 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Minimum</th><th>Maximum</th><th>Unit</th></tr>
<tr><td>V_{DD}</td><td>Supply Voltage with respect to Ground</td><td>Any VDD pin</td><td>-0.5</td><td>3.63</td><td>V</td></tr>
<tr><td rowspan="4">V_{IN}</td><td rowspan="4">Input Voltage [1]</td><td>XIN_REFIN, XOUT_REFINb [2]</td><td>-0.5</td><td>V_{DD} + 0.3</td><td>V</td></tr>
<tr><td>CLKIN[1:0]_GPI[1:0], CLKIN[1:0]b_GPI[3:2]</td><td>-0.5</td><td>V_{DD} + 0.3</td><td>V</td></tr>
<tr><td>GPIO[4:0] used as inputs</td><td>-0.5</td><td>V_{DD} + 0.3</td><td>V</td></tr>
<tr><td>SCL, SDA</td><td>-0.5</td><td>3.63</td><td>V</td></tr>
<tr><td>I_{IN}</td><td>Input Current</td><td>CLKIN[1:0]_GPI[1:0], CLKIN[1:0]b_GPI[3:2]</td><td>-</td><td>±50</td><td>mA</td></tr>
<tr><td rowspan="4">I_{OUT}</td><td rowspan="2">Output Current - Continuous</td><td>OUT[11:0], OUT[11:0]b</td><td>-</td><td>30</td><td>mA</td></tr>
<tr><td>GPIO[4:0] used as outputs, SDA</td><td>-</td><td>25</td><td>mA</td></tr>
<tr><td rowspan="2">Output Current - Surge</td><td>OUT[11:0], OUT[11:0]b</td><td>-</td><td>60</td><td>mA</td></tr>
<tr><td>GPIO[4:0] used as outputs, SDA</td><td>-</td><td>50</td><td>mA</td></tr>
<tr><td>T_J</td><td>Maximum Junction Temperature</td><td></td><td>-</td><td>150</td><td>°C</td></tr>
<tr><td>T_S</td><td>Storage Temperature</td><td>Storage Temperature</td><td>-65</td><td>150</td><td>°C</td></tr>
<tr><td rowspan="2">ESD</td><td>Human Body Model</td><td>JESD22-A114 (JS-001) Classification</td><td>-</td><td>2000</td><td>V</td></tr>
<tr><td>Charged Device Model</td><td>JESD22-C101 Classification</td><td>-</td><td>500</td><td>V</td></tr>
</table>

1. VDD refers to the VDD pin that supplies the particular input. To determine to which VDD pin the specification applies, see Table 30.
2. This limit only applies when XIN_REFIN/XOUT_REFINb are configured as an “Input Buffer” for use with an external oscillator. No limit is implied when connected directly to a crystal.

2.2 Recommended Operating Conditions

Table 4. Recommended Operating Conditions [1][2]

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Unit</th></tr>
<tr><td>T_J</td><td>Maximum Junction Temperature</td><td></td><td>-</td><td>-</td><td>125</td><td>°C</td></tr>
<tr><td>T_A</td><td>Ambient Operating temperature</td><td></td><td>-40</td><td>-</td><td>105</td><td>°C</td></tr>
<tr><td rowspan="2">V_{DDx}</td><td rowspan="2">Supply Voltage with respect to Ground</td><td>Any VDD pin, 1.8V supply</td><td>1.71</td><td>1.8</td><td>1.89</td><td>V</td></tr>
<tr><td>Any VDD pin, 3.3V supply</td><td>3.135</td><td>3.3</td><td>3.465</td><td>V</td></tr>
<tr><td>t_{PU}</td><td>Power-up time for all VDDs to reach minimum specified voltage.</td><td>Power ramps must be monotonic. For more considerations, see Application Information.</td><td>0.2</td><td>-</td><td>5</td><td>ms</td></tr>
</table>

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise. VDDA must be ≤ VDD.
2. All conditions in this table must be met to guarantee device functionality and performance.

2.3 Electrical Characteristics

All parameters in this section are specified over the recommended operating conditions as specified in Table 4.

Table 5. PCIe Refclk Jitter, VDDO = 1.8V or 3.3V [1][2]

Symbol	Parameter	Conditions	Typical	Maximum	PCIe Limit	Unit
$t_{jphPCIeG1-CC}$	PCIe Refclk Jitter in Clock Generator Mode (Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%)	PCIe Gen 1 (2.5 GT/s)	6,674	15,282	86,000	fs pk-pk
$t_{jphPCIeG2-CC}$		PCIe Gen 2 Hi Band (5 GT/s)	587	1,114	3000	fs RMS
		PCIe Gen 2 Lo Band (5 GT/s)	154	367	3100	
$t_{jphPCIeG3-CC}$		PCIe Gen 3 (8 GT/s)	193	372	1000	
$t_{jphPCIeG4-CC}$		PCIe Gen 4 (16 GT/s) [3][4]	141	372	500	
$t_{jphPCIeG5-CC}$		PCIe Gen 5 (32 GT/s) [3][5]	77	150	150	
$t_{jphPCIeG6-CC}$		PCIe Gen 6 (64 GT/s) [3][6]	34	86	100	
$t_{jphPCIeG2-IR}$	PCIe Refclk Jitter Clock Generator Mode (IR Architecture, SSC = 0% or -0.5%)	PCIe Gen 2 (5 GT/s)	245	905	N/A [7]	fs RMS
$t_{jphPCIeG3-IR}$		PCIe Gen 3 (8 GT/s)	199	542		
$t_{jphPCIeG4-IR}$		PCIe Gen 4 (16 GT/s)	161	535		
$t_{jphPCIeG5-IR}$	PCIe Refclk Jitter Clock Generator Mode (IR Architecture, SSC =0% or -0.3%)	PCIe Gen 5 (32 GT/s)	54	147		
$t_{jphPCIeG6-IR}$		PCIe Gen 6 (64 GT/s)	40	109		

1. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification Revision 6.2*. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements shall be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. The *PCI Express Base Specification Revision 6.2* provides the filters necessary to calculate SRIS and SRNS (IR) jitter values; it does not provide specification limits, hence the N/A in the Limit column. IR values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an IR system, the channel is short and the user may choose to use this more relaxed value as the jitter limit.

Table 6. Phase Jitter and Phase Noise – 1.8V or 3.3V VDDO [1][2]

Symbol	Parameter	Conditions	Typical	Maximum	Unit
tjit(Φ)	Random Phase Jitter, (50MHz XTAL, Synthesizer Mode)	OUT0: Frequency = 24MHz Integration Range: 12kHz-5MHz	850	1,050	fs (RMS)
		OUT10: Frequency = 40MHz Integration Range: 12kHz-5MHz	160	270	
		OUT8, OUT9: Frequency = 80MHz Integration Range: 12kHz-20MHz	300	450	
		OUT4, OUT5, OUT6, OUT7: Frequency = 100MHz, Integration Range: 12kHz-20MHz, SSC Off	230	440	
		OUT11: Frequency = 125MHz Integration Range: 12kHz-20MHz	260	380	
		OUT2: Frequency = 156.25MHz Integration Range: 12kHz-20MHz	240	330	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface. All outputs active at the same time.

Table 7. Clock Input Frequencies [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{INAPLL}	APLL Input Frequency for clock generation.	Over-driving Crystal Input, Doubler Logic Disabled	1	-	650	MHz
		Over-driving Crystal Input, Doubler Logic Enabled	1	-	250	

1. For crystal characteristics, see Table 8.

Table 8. External Crystal Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
-	Resonance Mode			Fundamental		-
f_{INXTAL} [1]	Crystal input frequency	Fundamental mode	8	-	62.5	MHz
ESR [1]	Equivalent Series Resistance	8MHz ≤ f_{INXTAL} ≤ 12MHz, C_L = 12pF	-	-	120	Ω
		12MHz < f_{INXTAL} ≤ 28MHz, C_L = 12pF	-	-	80	
		28MHz < f_{INXTAL} ≤ 54MHz, C_L = 12pF	-	-	50	
		54MHz < f_{INXTAL} ≤ 80MHz, C_L = 8pF	-	-	50	
C_O [1]	Shunt Capacitance		-	7	-	pF
C_L [1]	Load Capacitance		6	8	12	
Drive [1]	Drive Level		-	-	100	µW
F_{TOL}	Frequency Tolerance	Center frequency at 25°C	-	-	[2]	ppm
F_{STAB}	Frequency Stability	Over Operating Temperature Range with respect to F_{TOL}	-	-		
Aging	Per Year		-	-		

1. These parameters are required, regardless of crystal used.
2. These parameters are customer/application dependent. Common maximum values are F_{TOL} = ±20ppm, F_{STAB} = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.

Table 9. Output Frequencies and Startup Times [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{OUT}	Output Frequency	Differential Output.	0.001	-	650	MHz
		LVCMOS Output.	0.001	-	200	
f_{MON}	Reference Monitor Operating Frequency		-	-	40	MHz
f_{VCO}	VCO (APLL) Operating Frequency		9.5	-	10.7	GHz
$t_{STARTUP}$	Start-up Time [2][3]	Synthesizer mode.	-	8	11	ms

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP. For important additional power supply sequencing considerations, see Power Considerations.
3. Start-up time will depend on the actual configuration used. For more information, please contact Renesas technical support

Table 10. Output-to-Output Skew – LP-HCSL Outputs 1.8V or 3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2][3]	Any two outputs within the same bank	-	13	50	ps
		Any two outputs across all outputs banks sources from the same divider	-	15	92	
		Any two outputs across all output banks source from a different divider.	-	17	119	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65

Table 11. Output-to-Output Skew – LVDS Outputs 1.8V or 3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2][3]	Any two outputs within the same bank	-	13	50	ps
		Any two outputs across all outputs banks sources from the same divider	-	15	92	
		Any two outputs across all output banks source from a different divider.	-	17	119	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65

Table 12. Output-to-Output Skew – LVCMOS Outputs 1.8V or 3.3V VDDO [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
t_{SK}	Output-to-Output Skew [2][3]	Any two outputs within the same bank	-	26	85	ps
		Any two outputs across all outputs banks sources from the same divider	-	34	203	
		Any two outputs across all output banks source from a different divider.	-	60	310	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65

Table 13. LVCMOS AC/DC Output Characteristics - 1.8V VDDO[1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	I_{OH} = -2mA	VDDO - 0.45	VDDO - 0.04	VDDO + 0.3	V
V_{OL}	Output Low Voltage [2]	I_{OL} = 2mA	-	0.04	0.45	
IOZ	Output Leakage Current	Outputs Tri-stated	-5	0	5	µA
dV/dt	Slew Rate[3]	ODRV_CNFG[3:2] = 0	0.64	1.25	2.7	V/ns
		ODRV_CNFG[3:2] = 1	0.63	1.25	2.7	
		ODRV_CNFG[3:2] = 2	0.64	1.25	2.7	
		ODRV_CNFG[3:2] = 3	0.61	1.3	2.8	
tDC	Output Duty Cycle	V_T = VDDO/2	45	49.8	55	%

1. See Test Loads for additional information.
2. These values are compliant with JESD8-7A.
3. V_T = 20% to 80% of VDDO, C_L = 4.7pF.

Table 14. LVCMOS AC/DC Output Characteristics - 3.3V VDDO[1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	I_{OH} = -2mA	2.4	3.2	VDDO + 0.3	V
V_{OL}	Output Low Voltage [2]	I_{OL} = 2mA	-	0.04	0.4	
IOZ	Output Leakage Current	Outputs Tri-stated	-5	0	5	µA
dV/dt	Slew Rate[3]	ODRV_CNFG[3:2] = 0	1	4.2	5.1	V/ns
		ODRV_CNFG[3:2] = 1	0.8	2.7	4.2	
		ODRV_CNFG[3:2] = 2	0.7	2.2	4.2	
		ODRV_CNFG[3:2] = 3	0.9	2.6	4.8	
tDC	Output Duty Cycle	V_T = VDDO/2	45	50.7	55	%

1. See Test Loads for additional information.
2. These values are compliant with JESD8C.01.
3. V_T = 20% to 80% of VDDO, C_L = 4.7pF.

Table 15. LVDS AC/DC Output Characteristics – 1.8V V_{DDO} [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OT} (+)	TRUE binary state.	out_prog = 0x00	233	340	447	mV
V_{OT} (-)	FALSE binary state.		-493	-360	-227	
V_{OT} (+)	TRUE binary state.	out_prog = 0x01	227	341	454	mV
V_{OT} (-)	FALSE binary state.		-483	-369	-254	
V_{OT} (+)	TRUE binary state.	out_prog = 0x02	189	319	450	mV
V_{OT} (-)	FALSE binary state.		-483	-337	-191	
V_{OT} (+)	TRUE binary state.	out_prog = 0x03	211	331	452	mV
V_{OT} (-)	FALSE binary state.		-474	-349	-224	
ΔV_{OT}	Change in V_{OT} between Complimentary States		-	43	59	mV
V_{CMR}	Common Mode Voltage		1	1.17	1.32	V
ΔV_{CMR}	Change in V_{CMR} between Complimentary States		-	25	40.1	mV
I_{OS}	Short Circuit Current	V_{OUT+} = 0V	-	8.1	8.9	mA
		V_{OUT+} = VDD	-	0.7	1.8	mA
		V_{OUT-} = 0V	-	0.1	0.2	mA
		V_{OUT-} = VDD	-	9.6	11	mA
I_{OSD}	Differential Short Circuit Current	V_{OUT+} = V_{OUT-}	4	4.5	6	
t_R/t_F	Rise/Fall Time [2] V_T = 20% to 80% of swing.	Fout ≤ 400MHz	221	374	522	ps
		Fout > 400MHz	152	305	457	ps
t_{DC}	Duty Cycle	V_T = 0V differential, Fout ≤ 400MHz	47	50	53	%
		V_T = 0V differential, Fout > 400MHz	45	49.5	55	%

1. See Test Loads for additional test conditions.
2. Single-ended measurement

Table 16. LVDS AC/DC Output Characteristics – 3.3V V_{DDO} [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OT} (+)	TRUE binary state.	out_prog = 0x00	240	348	457	mV
V_{OT} (-)	FALSE binary state.		-464	-356	-247	
V_{OT} (+)	TRUE binary state.	out_prog = 0x01	255	366	477	mV
V_{OT} (-)	FALSE binary state.		-483	-372	-261	
V_{OT} (+)	TRUE binary state.	out_prog = 0x02	211	311	411	mV
V_{OT} (-)	FALSE binary state.		-427	-325	-224	
V_{OT} (+)	TRUE binary state.	out_prog = 0x03	225	330	434	mV
V_{OT} (-)	FALSE binary state.		-446	-341	-235	
ΔV_{OT}	Change in V_{OT} between Complimentary States		14	37	60	mV
V_{CMR}	Common Mode Voltage		1.16	1.21	1.32	V
ΔV_{CMR}	Change in V_{CMR} between Complimentary States		-	25	40	mV
I_{OS}	Short Circuit Current	V_{OUT+} = 0V	-	7.3	8	mA
		V_{OUT+} = VDD	-	0.7	6	mA
		V_{OUT-} = 0V	-	0.1	0.2	mA
		V_{OUT-} = VDD	-	12.6	15	mA
I_{OSD}	Differential Output Short Circuit Current	$V_{OUT+} = V_{OUT-}$	3	4	5	
t_R/t_F	Rise/Fall Time [2] V_T = 20% to 80% of swing.	Fout ≤ 400MHz	221	374	527	ps
		Fout >400MHz	152	305	458	ps
t_{DC}	Duty Cycle	V_T = 0V differential, Fout ≤ 400MHz	47	50	53	%
		V_T = 0V differential, Fout > 400MHz	45	49.5	55	%

1. See Test Loads for additional test conditions.
2. Single-ended measurement

Table 17. LP-HCSL AC/DC Output Characteristics, Non-PCIe Frequencies – 1.8V V_{DDO} [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate.	826	879	932	mV
V_{OL}	Output Low Voltage [2]		12	23	34	
V_{CROSS}	Crossing Voltage (abs) [3]		119	364	608	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	20	72	
t_R/t_F	Rise/Fall Time [2] V_T = 20% to 80% of swing	V_{HIGH} = 800mV, Fast Slew Rate, f ≤ 400MHz.	374	499	624	ps
	Rise/Fall Time [2] V_T = 20% to 80% of swing	V_{HIGH} = 800mV, Fast Slew Rate, f > 400MHz,	118	247	376	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate.	850	913	980	mV
V_{OL}	Output Low Voltage [2]		-1	5	11	
V_{CROSS}	Crossing Voltage (abs) [3]		120	376	632	
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	21	91	
t_R/t_F	Rise/Fall Time [2] V_T = 20% to 80% of swing.	V_{HIGH} = 900mV, Fast Slew Rate, f ≤ 400MHz.	386	498	609	ps
	Rise/Fall Time [2] V_T = 20% to 80% of swing.	V_{HIGH} = 900mV, Fast Slew Rate, f > 400MHz.	107	241	374	
t_{DC}	Output Duty Cycle [6]	Across all settings, V_T = 0V.	45	50	55	%

1. Standard high impedance load with C_L= 2pF. See Test Loads. Tested at 25MHz, 100MHz, 156.25MHz, 312.5MHz and 625MHz.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum variance in V_{CROSS} for any particular system.
6. Measured from differential waveform.

Table 18. LP-HCSL AC/DC Output Characteristics, Non-PCIe Frequencies – 3.3V V_{DDO} [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{OH}	Output High Voltage [2]	V_{HIGH} = 800mV, Fast Slew Rate.	858	910	963	mV
V_{OL}	Output Low Voltage [2]		12	22	33	mV
V_{CROSS}	Crossing Voltage (abs) [3]		223	414	605	mV
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	23	90	mV
t_R/t_F	Rise/Fall Time [2] V_T = 20% to 80% of swing	V_{HIGH} = 800mV, Fast Slew Rate, f ≤ 400MHz.	344	500	656	ps
	Rise/Fall Time [2] V_T = 20% to 80% of swing	V_{HIGH} = 800mV, Fast Slew Rate, f > 400MHz.	124	200	276	
V_{OH}	Output High Voltage [2]	V_{HIGH} = 900mV, Fast Slew Rate.	800	934	1051	mV
V_{OL}	Output Low Voltage [2]		-95	5	68	mV
V_{CROSS}	Crossing Voltage (abs) [3]		222	437	651	mV
ΔV_{CROSS}	Crossing Voltage (var) [3][4][5]		-	24	100	mV

Table 18. LP-HCSL AC/DC Output Characteristics, Non-PCIe Frequencies – 3.3V V_{DDO} [1] (Cont.)

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Unit</th></tr>
<tr><td rowspan="2">t_R/t_F</td><td>Rise/Fall Time [2]
V_T = 20% to 80% of swing</td><td>V_{HIGH} = 900mV, Fast Slew Rate, f ≤ 400MHz.</td><td>348</td><td>502</td><td>656</td><td rowspan="2">ps</td></tr>
<tr><td>Rise/Fall Time [2]
V_T = 20% to 80% of swing</td><td>V_{HIGH} = 900mV, Fast Slew Rate, f > 400MHz.</td><td>126</td><td>209</td><td>292</td></tr>
<tr><td>t_{DC}</td><td>Output Duty Cycle [6]</td><td>Across all settings, V_T = 0V.</td><td>45</td><td>50</td><td>55</td><td>%</td></tr>
</table>

1. Standard high impedance load with C_L= 2pF. See Test Loads. Tested at 25MHz, 100MHz, 156.25MHz, 312.5MHz and 625MHz.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in V_{CROSS} for any particular system.
6. Measured from differential waveform.

Table 19. LP-HCSL AC/DC Output Characteristics, 100MHz PCIe – 1.8V or 3.3V V_{DDO} [1]

<table>
<tr><th>Symbol</th><th>Parameter</th><th>Conditions</th><th>Minimum</th><th>Typical</th><th>Maximum</th><th>Spec. Limit [2]</th><th>Unit</th></tr>
<tr><td>V_{MAX}</td><td>Absolute Max Voltage
Includes 300mV of overshoot (Vovs) [3][4]</td><td rowspan="2">Across all settings in this table.</td><td>-</td><td>-</td><td>1120</td><td>1150</td><td rowspan="2">mV</td></tr>
<tr><td>V_{MIN}</td><td>Absolute Min Voltage
Includes -300mV of undershoot (Vuds) [3][5]</td><td>-143</td><td>-</td><td>-</td><td>-300</td></tr>
<tr><td>V_{HIGH}</td><td>Voltage High [3]</td><td rowspan="2">V_{HIGH} set to 800mV.</td><td>767</td><td>904</td><td>1041</td><td>-</td><td rowspan="4">mV</td></tr>
<tr><td>V_{LOW}</td><td>Voltage Low [3]</td><td>-69</td><td>-13</td><td>44</td><td>-</td></tr>
<tr><td>V_{CROSS}</td><td>Crossing Voltage (abs) [3][6][7]</td><td rowspan="2">V_{HIGH} set to 800mV, scope averaging off.</td><td>290</td><td>417</td><td>543</td><td>250 to 550</td></tr>
<tr><td>ΔV_{CROSS}</td><td>Crossing Voltage (var) [3][6][8]</td><td>-</td><td>30</td><td>42</td><td>140</td></tr>
<tr><td rowspan="2">dv/dt</td><td rowspan="2">Slew rate [9][10]</td><td>V_{HIGH} set to 800mV, Fast slew rate, scope averaging on.</td><td>1</td><td>2,3</td><td>3.7</td><td rowspan="2">1 to 4</td><td rowspan="2">V/ns</td></tr>
<tr><td>V_{HIGH} set to 800mV, Slow slew rate, scope averaging on.</td><td>0.7</td><td>1.9</td><td>3.1</td></tr>
<tr><td>$\Delta T_{R/F}$</td><td>Rise/fall matching [3][11]</td><td>V_{HIGH} set to 800mV. Fast or slow slew rate.</td><td>-</td><td>8</td><td>20</td><td>20</td><td>%</td></tr>
<tr><td>V_{HIGH}</td><td>Voltage High [3]</td><td rowspan="2">V_{HIGH} set to 900mV.</td><td>825</td><td>973</td><td>1121</td><td>-</td><td rowspan="4">mV</td></tr>
<tr><td>V_{LOW}</td><td>Voltage Low [3]</td><td>-71</td><td>-14</td><td>43</td><td>-</td></tr>
<tr><td>V_{CROSS}</td><td>Crossing Voltage (abs) [3][6][7]</td><td rowspan="2">V_{HIGH} set to 900mV, scope averaging off.</td><td>322</td><td>460</td><td>597</td><td>300 to 600</td></tr>
<tr><td>ΔV_{CROSS}</td><td>Crossing Voltage (var) [3][6][8]</td><td>-</td><td>30</td><td>46</td><td>140</td></tr>
<tr><td rowspan="2">dv/dt</td><td rowspan="2">Slew rate [9][10]</td><td>V_{HIGH} set to 900mV, Fast slew rate, scope averaging on.</td><td>1.1</td><td>2.5</td><td>3.9</td><td rowspan="2">1 to 4</td><td rowspan="2">V/ns</td></tr>
<tr><td>V_{HIGH} set to 900mV, Slow slew rate, scope averaging on.</td><td>0.8</td><td>2</td><td>3.2</td></tr>
</table>

Table 19. LP-HCSL AC/DC Output Characteristics, 100MHz PCIe – 1.8V or 3.3V V_{DDO} [1] (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Spec. Limit [2]	Unit
$\Delta T_{R/F}$	Rise/fall matching [3][11]	V_{HIGH} set to 900mV. Fast or slow slew rate.	-	8	20	20	%
t_{DC}	Output Duty Cycle [9]	Across all settings in this table, V_T = 0V.	49	50	52	45 to 55	%
$t_{jcyc\text{-}cyc}$	Jitter, Cycle to cycle [9]	Across all settings in this table.	-	34	45	50	ps

1. Standard high impedance load with C_L= 2pF. See Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.2* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in V_{CROSS} for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

Table 20. 100MHz PCIe Output Clock Accuracy and SSC

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	PCIe Limit[1]	Unit
$T_{PERIOD\_AVG\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices supporting 32GT/s or 64GT/s CC mode at any speed. [2][3]	SSC ≤ -0.5%, includes spread-spectrum modulation, if any.	0	-	2410	-100 to +2600	ppm
$T_{PERIOD\_AVG\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][3]	SSC ≤ -0.3%, includes spread-spectrum modulation, if any.	0	-	1430	-100 to +1600	ppm
$T_{PERIOD\_AVG\_32G\_64G}$	Average Clock Period Accuracy for devices supporting 32GT/s CC/SRNS mode at any speed. [2][3]	SSC = 0% (SSC Off).	0	-	0	±100	ppm

Table 20. 100MHz PCIe Output Clock Accuracy and SSC (Cont.)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	PCIe Limit[1]	Unit
$T_{PERIOD\_ABS\_32G\_64G\_CC}$	Average Clock Period Accuracy for devices supporting 32GT/s CC mode at any speed. [2][4]	SSC ≤ -0.5%, includes jitter and spread-spectrum modulation.	10	-	10.024	9.849 to 10.201	ns
$T_{PERIOD\_ABS\_32G\_64G\_SRIS}$	Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][4]	SSC ≤ -0.3%, includes jitter and spread-spectrum modulation.	10	-	10.014	9.849 to 10.181	
$T_{PERIOD\_ABS\_32G\_64G}$	Average Clock Period Accuracy for devices supporting 32GT/ s CC/SRNS mode at any speed. [2][4]	SSC = 0% (SSC Off), includes jitter.	10	-	10	9.849 to 10.151	
$F_{REFCLK\_32G\_64G}$	Refclk Frequency for devices that support 32GT/s or 64GT/s.	SSC = 0% (SSC Off)	100	-	100	99.99 to 100.01	MHz
F_{SSC}	SSC Modulation Frequency		31.1	31.6	32.1	30 to 33	kHz
$T_{SSC\_FREQ\_DEV}$	SSC Deviation for all devices and architectures except 32GT/s or 64GT/s devices operating in SRIS mode.	SSC = -0.5%	-0.490	-0.488	-0.486	-0.5	%
$T_{SSC\_FREQ\_DEV\_32G\_64G\_SRIS}$	SSC Deviation for devices that support 32 or 64GT/s operating in SRIS mode, at any speeds.	SSC = -0.3%	-0.300	-0.295	-0.290	-0.3	%
$T_{SSC\_MAX\_FREQ\_SLEW}$	Max df/dt of the SSC. [5]		-	310	372	1250	ppm/us
$T_{TRANSPORT\_DELAY}$	Tx-Rx transport delay used for PCIe Jitter calculations. [6]	Applies to Common Clocked architectures only.	-	-	12	12	ns

1. The specification limits are taken from either the *PCIe Base Specification Revision 6.2* or from relevant x86 processor specifications, whichever is more stringent.
2. Measured from differential waveform.
3. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100PPM, then we have an error budget of 100Hz/PPM * 100PPM = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±100PPM applies to systems that do not employ Spread-Spectrum Clocking, or that use common clock source. For systems employing Spread-Spectrum Clocking, there is an additional 2,500PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600PPM for Common Clock Architectures. SRIS Architectures may have a lower allowed spread percentage. Devices meeting these specifications automatically meet the less stringent -300ppm to +2800ppm tolerances for data rates ≤16GT/s. Refer to Section 8.6 of the *PCI Express Base Specification, Revision 6.0*.
4. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread-spectrum modulation. Devices meeting these specifications automatically meet the less stringent and 9.847ns to 10.203ns tolerances for data rates ≤16GT/s.
5. Measurement is made over a 0.5us time interval with a 1st order LPF with an fC of 60x the SSC modulation frequency (1.89MHz for 31.5kHz modulation frequency).
6. This is the default value used for all PCIe Common Clock architecture jitter calculations. There are form factors (for example topologies including long cables) that may exceed this limit. Contact Renesas for assistance calculating jitter if your topology exceeds 12ns.

Table 21. Spread-Spectrum Programmability

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
f_{SSCMOD}	SSC Modulation Frequency	Modulation frequency.	30	-	63	kHz
SSC%	Spread percentage [1]	Down Spread.	-1	-	-0.5	%
		Center Spread.	±0.025	-	±0.75	
f_{OUTSSC}	Output frequency	Allowable output frequency range when SSC is enabled.	30	-	650	MHz

1. Spread off is 0%.

Table 22. GPI/GPIO Electrical Characteristics – 1.8V VDDD, VDDR, or VDDX [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [3]	XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0].	0.65 VDD	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [3]	XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0].	-0.3	-	0.35 VDD	
V_{OH}	Output High Voltage [3]	GPIO[4:0], IOH = -2mA.	VDD - 0.45	-	VDD + 0.3	
V_{OL}	Output Low Voltage [3]	GPIO[4:0], IOL = 2mA.	-	-	0.45	

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 22, see GPI and GPIO VDD pin assignments in Pin Information. For SCL, SDA_SDI, see the I2C/SMBus electrical characteristics Table 26 and Table 27.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-7A. These values only apply to XIN_REFIN and XOUT_REFINB when "Input Buffer" mode is selected. See the Applications section for more details.

Table 23. GPI/GPIO Electrical Characteristics – 3.3V VDDD, VDDR, or VDDX [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	Input High Voltage [3]	XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0].	2.2	-	VDD + 0.3	V
V_{IL}	Input Low Voltage [3]	XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0].	-0.3	-	0.8	
V_{OH}	Output High Voltage [3]	GPIO[4:0], IOH = -2mA.	2.4	-	VDD + 0.3	
V_{OL}	Output Low Voltage [3]	GPIO[4:0], IOL = 2mA.	-	-	0.4	

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 23, see GPI and GPIO VDD pin assignments in Pin Information. For SCL, SDA_SDI, see the I2C/SMBus electrical characteristics Table 26 and Table 27.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8C-01. These values only apply to XIN_REFIN and XOUT_REFINB when "Input Buffer" mode is selected. See the Applications section for more details.

Table 24. CMOS GPI/GPIO Common Electrical Characteristics [1][2]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
I_{IL}	Input Leakage Current	Includes input pull up/pull down resistor current. V_{IL} = 0V, V_{IH} = V_{DD}.	-74	-	74	µA
		Does NOT include input pull up/pull down resistor current. V_{IL} = 0V, V_{IH} = V_{DD}.	-5	-	5	

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. For VDD pin mapping, see GPI and GPIO VDD pin assignments in Pin Information.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.

Table 25. Power Supply Current [1]

Symbol	Parameter	Conditions	Typical	Maximum	Unit
I_{DDX0}	V_{DDX0} Supply Current	V_{DDXn} = any valid supply.	7.5	8.1	mA
I_{DDX1}	V_{DDX1} Supply Current		8	11	mA
I_{DDA}	V_{DDA} Supply Current	V_{DDA} = any valid supply.	106	138	mA
I_{DDD}	V_{DDD} Supply Current	V_{DDD} = any valid supply.	54	64	mA
I_{DDO_CMOS}	V_{DDO} Supply Current per output pair, CMOS mode (both OUT[x] and OUT[x]b enabled). [2][3]	V_{DDO} = 1.8V + 0.1V.	9	22	mA
		V_{DDO} = 3.3V $\pm$5%.	16	35	
	V_{DDO} Supply Current per output pair, CMOS mode (OUT[x] or OUT[x]b enabled, other output Hi-Z). [2][3]	V_{DDO} = 1.8V + 0.1V.	6	13	mA
		V_{DDO} = 3.3 $\pm$5%.	10	17	
I_{DDO_LPHCSL}	V_{DDO} Supply Current per output pair [2][3]	LP-HCSL outputs, 85ohm impedance, fast slew rate, 650MHz. V_{DDO} = any valid supply.	20	33	mA
		LP-HCSL outputs, 85ohm impedance, fast slew rate, 100MHz, C_L = 2pF for PCIe. V_{DDO} = any valid supply.	20	30	
I_{DDO_LVDS}	V_{DDO} Supply Current per output pair, LVDS mode [3]	V_{DDO} = any valid supply.	12	28	mA
I_{DD_IOD}	V_{DDO} Divider Supply Current	Current consumed per IOD (V_{DDO5} and V_{DDO6}).	36	44	mA
I_{DD_LPFOD}	V_{DDO} Divider Supply Current	Current consumed per LPFOD (V_{DDO0} and V_{DDO1}).	38	69	mA
I_{DD_HPFOD}	V_{DDO} Divider Supply Current	Current consumed per HPFOD (V_{DDO2}, V_{DDO3}, and V_{DDO4})	75	117	mA

1. Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply enabled and all outputs running at maximum speed, unless otherwise noted. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device. To determine actual consumption for the user's device configuration, see Power Considerations. Outputs are not terminated. Values apply to all voltage levels unless noted.
2. I_{DDO_x} denotes the current consumed by each output driver and does not include output divider current. These values are measured at maximum output frequency, unless otherwise stated (200MHz for LVCMOS outputs and 650MHz for differential outputs).
3. Please refer to the Output Driver and Output Divider V_{DDO} Pin Assignments Table to determine the allocation of I_{DDO_IOD}, I_{DDO_FOD} and I_{DDO_x} to each V_{DDO} pin.

Table 26. I2C Bus DC Electrical Characteristics [1]

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
V_{IH}	High-level input voltage for SCL and SDA		0.7 V_{DDD}	-	-	V
V_{IL}	Low-level input voltage for SCL and SDA		-	-	0.3 V_{DDD}	V
V_{HYS}	Hysteresis of Schmitt trigger inputs		0.05 V_{DDD}	-	-	V
V_{OL}	Low-level output voltage for SCL and SDA	I_{OL} = 4mA	-	-	0.4	V
I_{IN}	Input leakage current per pin		-5	-	5	µA
C_B	Capacitive Load for Each Bus Line		-	-	400	pF

1. V_{OH} is governed by the V_{PUP}, the voltage rail to which the pull up resistors are connected.

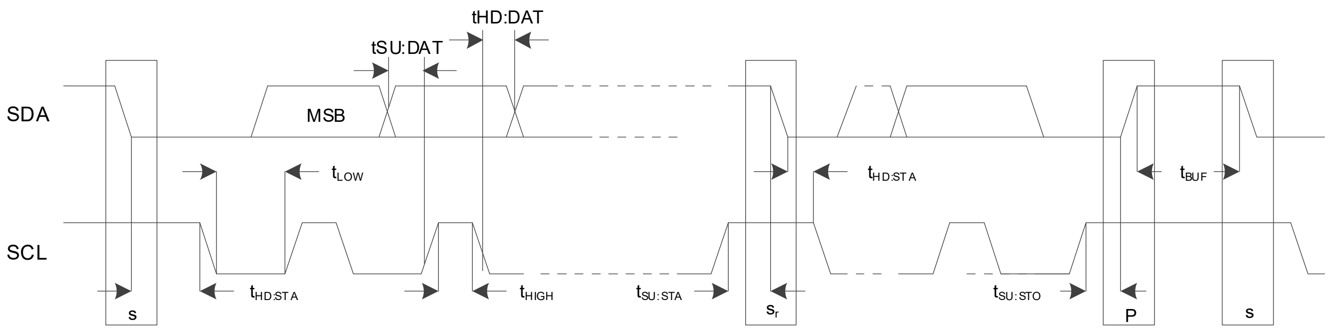


Figure 4. I2C Slave Timing Diagram

Table 27. I2C Bus AC Electrical Characteristics

Symbol	Parameter	Conditions	100kHz Class Minimum	100kHz Class Maximum	400kHz Class Minimum	400kHz Class Maximum	Unit
f_{SMB}	I2C Operating Frequency [1]		10	100	10	400	kHz
t_{BUF}	Bus free time between STOP and START Condition		4.7	-	1.3	-	µs
$t_{HD:STA}$	Hold time after (REPEATED) START Condition [2]		4	-	0.6	-	
$t_{SU:STA}$	REPEATED START Condition setup time		4.7	-	0.6	-	
$t_{SU:STO}$	STOP Condition setup time		4	-	0.6	-	
$t_{HD:DAT}$	Data hold time [3]		300	-	300	-	ns
$t_{SU:DAT}$	Data setup time		250	-	100	-	
$t_{TIMEOUT}$	Detect SCL low timeout [4]		25	35	25	35	ms
$t_{TIMEOUT}$	Detect SDA low timeout [5]		25	35	25	35	
t_{LOW}	Clock low period		4.7	-	1.3	-	µs
t_{HIGH}	Clock high period [6]		4	50	0.6	50	

Table 27. I2C Bus AC Electrical Characteristics (Cont.)

Symbol	Parameter	Conditions	100kHz Class Minimum	100kHz Class Maximum	400kHz Class Minimum	400kHz Class Maximum	Unit
$t_{LOW:SEXT}$	Cumulative clock low extend time (slave device) [7]		N/A, the RC2121xA do not extend the clock low.				ms
$t_{LOW:MEXT}$	Cumulative clock low extend time (master device) [8]		N/A, the RC2121xA are not bus masters.				ms
t_F	Clock/Data Fall Time [9]		-	120	-	120	ns
t_R	Clock/Data Rise Time [9]		-	120	-	120	ns
t_{SPIKE}	Noise spike suppression time [10]		-	N/A	-	50	ns

1. A master shall not drive the clock at a frequency below the minimum f_{SMB}. Further, the operating clock frequency shall not be reduced below the minimum value of f_{SMB} due to periodic clock extending by slave devices as defined in Section 5.3.3 of the *SMBus 2.0 Specification*. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:SEXT}$ and $t_{LOW:MEXT}$ limits. For example, if the SCK is high for $t_{HIGH:MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB:MIN} – t_{HIGH:MAX}$. This requirement does not pertain to a device that extends the SCK low for data processing of a received byte, data buffering and so forth for longer than 100µs in a non-periodic way.
2. A device must internally provide sufficient hold time for the SDA signal (with respect to the $V_{IH:MIN}$ of the SCK signal) to bridge the undefined region of the falling edge of SCK.
3. Slave devices may have caused other slave devices to hold SDA low. The maximum time that a device can hold SDA low after the master raises SCK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
4. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT:MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT:MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SCK low for $t_{TIMEOUT:MAX}$ or longer.
5. The device has the option of detecting a timeout if the SDA pin is also low for this time.
6. $t_{HIGH:MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH:MAX}$.
7. $t_{HIGH:MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH:MAX}$.
8. $t_{LOW:SEXT}$ is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that another slave device or the master will also extend the clock causing the combined clock low extend time to be greater than $t_{LOW:SEXT}$. Therefore, this parameter is measured with the slave device as the sole target of a full-speed master.
9. The rise and fall time measurement limits are defined as follows:

   Rise Time Limits: ($V_{IL:MAX}$ - 0.15V) to ($V_{IH:MIN}$ + 0.15V)

   Fall Time Limits: ($V_{IH:MIN}$ + 0.15V) to ($V_{IL:MAX}$ - 0.15V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

Table 28. Power Supply Noise Rejection

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Unit
PSNR	Power Supply Noise Rejection [1][2][3][4] 1.8V operation	VDDO[0:6] [5], $f_{NOISE} \leq$ 1MHz, LVDS/LPHCSL output type	-40	-36	-	dBc
		VDDO[0:6] [5], $f_{NOISE} \leq$ 1MHz, LVCMOS output type	-30	-28	-	
		VDDD, VDDA, VDDX0, VDDX1, $f_{NOISE} \leq$ 1MHz	-47	-38	-	
		VDDD, VDDA, VDDX0, VDDX1, 100kHz $\leq f_{NOISE} \leq$ 1MHz	-134	--120	-	
		VDDD, VDDA, VDDX0, VDDX1, $f_{NOISE} \leq$ 100kHz	-139	-135	-	
PSNR	Power Supply Noise Rejection [1][3][4][6] 3.3V operation	VDDO[0:6] [5], $f_{NOISE} \leq$ 1MHz, LVDS/LPHCSL output type,	-70	-32	-	dBc
		VDDO[0:6] [5], $f_{NOISE} \leq$ 1MHz, LVCMOS output type	-47	-32	-	
		VDDD, VDDA, VDDX0, VDDX1, $f_{NOISE} \leq$ 1MHz	-72	-65	-	
		VDDD, VDDA, VDDX0, VDDX1, 100kHz $\leq f_{NOISE} \leq$ 1MHz	-132	-110	-	
		VDDD, VDDA, VDDX0, VDDX1, $f_{NOISE} \leq$ 100kHz	-17	-130	-	

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. VDDX0 = VDDX1 = VDDD = VDDA = VDD[0:6] = 1.8V ±5%, VSS = 0V, TA = -40°C to 105°C.
3. 50mV peak-to-peak sine wave applied injected on indicated power supply pin(s).
4. Noise spur amplitude measured relative to 156.25MHz carrier frequency.
5. Excluding VDDOx of the output being measured.
6. VDDX0 = VDDX1 = VDDD = VDDA = VDD[0:6] = 3.3V ±5%, VSS = 0V, TA = -40°C to 105°C.

3. Overview

The following sections provide an overview of the RC2121xA family.

3.1 Power-Up, Configuration, and Serial Interfaces

The RC2121xA can be powered-up and configured from one of eight configurations stored in internal OTP. These configurations are referred to as User Configurations (UserCfg). The power-up configuration can be selected via external GPIO pins or by programming a field to select a default configuration to load. This is useful when external GPIO are not used to select a UserCfg at power-up.

The crystal oscillator starts, the APLL locks, and various power-on-self tests are run. The outputs remain disabled until the power-up sequence completes successfully. After the power-up sequence completes, the outputs are enabled according to register settings and OE pins as programed into the OTP.

The RC2121xA has a slave I^2C serial interface that can be used to change configuration after power-up or monitor the device during operation. The I^2C slave address is programmable.

3.2 Input Clocks

The RC2121[2/4]A supports two crystal/reference inputs.

The RC2121[1/3]A supports one crystal/reference inputs.

3.2.1 Crystal/Reference Input

The crystal input supports crystal frequencies of 8MHz to 80MHz. It has programmable internal load capacitors to support crystals with CL = 6pF to 12pF.

The crystal input supports being over-driven with a single-ended or differential clock, or a 0.8VPP clipped sine-wave TCXO. Refer to

The supported input frequency range is same as reference clock inputs: 1MHz to 650MHz in differential mode, and 8kHz to 250MHz in single-ended mode. Input reference monitoring is not supported for frequencies over 62.5MHz.

3.3 GPIO and GPI

There are seven GPIO pins GPIO[6:0] and two GPI pins. The GPI pins are only available in single crystal variants. These pins are typically assigned special functions such as the following:

- INT – Interrupt, up to 1 pin (GPIO only)
- FAULT – Fault, up to 1 pin (GPIO only)
- SEL – OTP image select, up to 3 pins
- OE – Output enable, up to 6 pins

GPIO[6:1] are open drain (or input), and are 3.3V tolerant when powered from 1.8V. GPIO[0] is push-pull driver (or input), and is *not* 3.3V tolerant when powered at 1.8V VDDD. All GPIO pins are 3.3 V tolerant when powered at 3.3V VDDD.

GPI pins are *not* 3.3V tolerant when powered at 1.8V VDDX1. GPI pins are 3.3 V tolerant when powered at 3.3V VDDX1.

In addition, the GPIO pins can be used to read/write a logic level on a pin. Similarly, the GPI pins can be used to read a logic level.

All GPI and GPIO pins have programmable pull-down.

3.4 APLL

The APLL is fractional LC-VCO based PLL with an operating range from 9.5GHz to 10.7GHz.

Any of the available crystals or input reference clock can be selected to provide a reference to the APLL. The input reference can be frequency doubled for increased performance. The APLL is temperature compensated for the utmost frequency stability. Lock detect status is also provided and can be read from an internal register.

3.5 Dividers

3.5.1 Output Dividers

The RC2121xA provides two integer, two limited-performance fractional output dividers, and three high-performance fractional output dividers.

3.5.2 Integer Output Dividers (IOD)

There are two IODs. IODs use a 25-bit divider to provide output frequencies from 1kHz to 650MHz from the VCO clock. Changing IOD values results in an immediate change to the new frequency. Glitch-less squelch and release of the IOD clock is supported. When enabled, this mimics a gapped clock behavior when an IOD frequency is changed.

3.5.3 Limited-Performance Fractional Output Dividers (LPFOD)

There are two limited-performance fractional output dividers (LPFODs). Each LPFOD can divide down the VCO clock to provide frequencies of 1kHz to 650MHz. Each LPFOD is implemented in a similar manner as the IOD. The difference is that the MMD (Multi Modulus Divider) is modulated by a first order SDM (sigma delta modulator). The output period has an additional ~1.0ps (VCO frequency ~10GHz) cycle-to-cycle jitter, from the modulation. The LPFOD can be programed to operate in IOD mode with the same performance as an IOD.

3.5.4 High-Performance Fractional Output Dividers (HPFOD)

There are three high-performance fractional output dividers (HPFODs). Each HPFOD can divide down the VCO clock to provide frequencies of 1kHz to 650MHz. Each HPFOD is implemented in two stages. The first stage is an 8-bit fractional divider with Digital Control Delay (DCD) correction followed by a divide-by-2. The DCD is a phase interpolator to reduce cycle-to-cycle jitter introduced by the first order SDM. The first stage allows a divide down of the VCO clock to 33MHz to 657MHz. The HPFOD's second stage divider is a 17-bit integer divider with minimum divide ratio of 4. This allows output frequencies lower than 30MHz. For output frequencies above 33MHz, this second-stage divider can be bypassed.

3.5.4.1 Spread-Spectrum Clocking (SSC)

HPFOD0 and HPFOD1 support SSC. SCC modulation is supported from 25MHz to 650MHz.

If SSC is enabled then the spread-spectrum engine modulates a triangular frequency profile onto the HPFOD divider ratio. The modulation amplitude is programmable. The modulation type can be programmed to either down-spread or center-spread. The supported modulation frequency is from 30kHz to 63kHz. When turning off spreading, it stops when the current spreading cycle completes (the frequency returns to the SSC off value).

Table 29. SSC Characteristics

SSC Direction	SSC Modulation Freq. (kHz)	Minimum SSC Amount (%)	Maximum SSC Amount (%)
Down	30 - 63	< -0.05	- 3
Center	30 - 63	< ± 0.025	± 1.5

If the HPFOD0 and HPFOD1 SSC are programmed to the same modulation frequency, they can be programed to be in phase. The modulation amplitude and mode (down or center spread) can be set differently. SSC clock outputs meets the phase jitter and ppm accuracy requirements of PCI-Express Gen1 to Gen5.

3.6 Clock Outputs

The RC2121xA outputs are individually programmable to support single-ended and differential output types.

3.6.1 Output Types

Differential outputs can be set to 85ohm HCSL, 100ohm HCSL, or LVDS. The HCSL outputs types are low-power push-pull HCSL (LPHCSL). They require external terminations to drive standard HCSL inputs, such as those found in PCIe applications. HCSL outputs have programmable output swing and HCSL outputs also have two slew rate settings (2V/ns to 4V/ns and 3V/ns to 5V/ns). LVDS outputs require only a 100ohm resistor between the true and complement inputs of the clock input being driven. Both LVDS and HCSL provide output swing levels that are compatible with LVPECL and CML with external AC coupling.

If set to single-ended mode, the output pair can drive either pin or both pins. If both pins are enabled, they can be in phase, or inverted phase. The single-ended outputs support LVCMOS swings of 1.8V or 3.3V as determined by their VDDO voltage.

3.6.2 Output Banks

The RC2121xA maps the internal and external frequency sources to output banks according to the following table.

Table 30. Output Bank Source Mapping

	Bank 0 VDDO0 (OUT0)	**Bank 1 VDDO1 (OUT1)**	**Bank 2 VDDO2 (OUT[3:2])**	**Bank 3 VDDO3 OUT[7:4])**	**Bank 4 VDDO4 (OUT[9:8])**	**Bank 5 VDDO5 (OUT10)**	**Bank 6 VDDO6 (OUT11)**
LPFOD0	**Yes(48)** [1]	**Yes(40)** [2]					
LPFOD1	Yes	**Yes**[3]	Yes				
HPFOD0	Yes	Yes	**Yes**	Yes			
HPFOD1	Yes	Yes	Yes	**Yes**	Yes	Yes	Yes
HPFOD2				Yes	**Yes**	Yes	Yes
IOD1					Yes	**Yes**	Yes
IOD0						Yes	**Yes**
APLL REF						Yes	Yes

1. Bold **Yes(48)** indicates that the divider is powered from the bank VDD0 on 48-pin variant.
2. Bold **Yes(40)** indicates that the divider is powered from the bank VDD0 on 40-pin variant.
3. Bold **Yes** indicates that the divider is powered from the bank VDD0 on all variants.

3.7 Fault Monitors and Diagnostics

3.7.1 Overview

The RC2121xA implements many diagnostic and fault detection features. Some at power on and some run during operation. When a fault is detected either the interrupt pin (INT) or fault pin (FAULT) is activated, if enabled. The mechanisms are as follows:

- Each monitor maps to the FAULT output or to the INT output, or none, configurable by register bit.
- Supports fail safe: when an error is detected (and enabled, and set to FAULT mode) the RC2121xA goes to its safe state:
  - All outputs are disabled.
  - FAULT pin asserted, active low.
  - I^2C is operational
- Provides fault insertion capabilities to insert all faults that are monitored.

- Dual crystal support, such that if the active crystal fails the device performs a hitless switch.
- If an error is detected, and enabled, the associated output is disabled.

3.7.2 System Interface

The RC2121xA provides an I^2C slave interface, whereby the system may read various status information to determine if there are any issues. The I^2C slave interface is CRC protected. Default configuration provides a GPIO pin used for INT, and another GPIO pin is used for FAULT; both are open-drain active-low signals. The expected use case is that some errors (e.g., a crystal switch over or a single output clock failure) would be mapped to an interrupt, and the SoC could take appropriate action. Other failures (e.g., the APLL loss of lock) would trigger a FAULT, and this would be used to put the system in a safe state. APLL losing lock would affect all outputs.

3.7.3 Redundant Crystals

The RC2121[2/4]A supports redundant crystals. If the active crystal monitors detect an error condition, the mux will perform a hitless switch to the other crystal, assuming it is operating correctly. The crystals must operate within 200ppm of each other, for crystals equal to or lower than 50MHz, and 100ppm for crystals greater than 50MHz. The switching between crystals is non-revertive.

3.7.4 Monitors

The RC2121xA provides the following monitors:

- Loss of signal on crystal of reference input.
- PPM warning and error thresholds between the two crystals.
- Loss of lock on APLL.
- Frequency error detection at each enabled output, and if enabled, the output is disabled.
- 8-bit CRC check on I^2C interface.
- 32-bit CRC check on OTP download.
- 32-bit CRC check on control registers for soft errors, every 10ms.

3.7.5 Power-on Self Test

The RC2121xA provides the following:

- Digital built-in self test.
- Checking of monitors via fault insertion.

4. Application Information

4.1 Recommendations for Unused Input and Output Pins

4.1.1 XIN0_REFIN0/XOUT0_REFIN0b, XIN1_REFIN1_GPI0/XOUT1_REFIN1b_GPI1

If used as crystal inputs, each set of pins must be connected to a crystal. For applications using the pins as REFIN inputs, both inputs of each pair should be left floating. If used as LVCMOS control pins, GPI0 and GPI1 have internal pull-ups or pull-downs. Additional resistance is not required but can be added for additional protection. A 10kΩ resistor can be used. If using these pins as REFIN0/REFIN0b or REFIN1/REFIN1b, see Overdriving the XTAL Interface for important information.

4.1.2 LVCMOS Outputs

Any LVCMOS output can be left floating if unused. There should be no trace attached. The output buffer should be set to high-impedance state to avoid unnecessary noise generation.

4.1.3 Differential Outputs

All unused differential outputs can be left floating. Renesas recommends that no trace be attached and that the outputs be set to high impedance. Both sides of the differential output pair should be treated the same, either left floating or terminated.

4.2 Crystal or Reference Clock Inputs

The RC2121xA provides a programmable input buffer for reference clock inputs, as shown in Figure 5. This programmable buffer supports most standard signaling protocols with no need for external termination components at the receiver end of the transmission line.

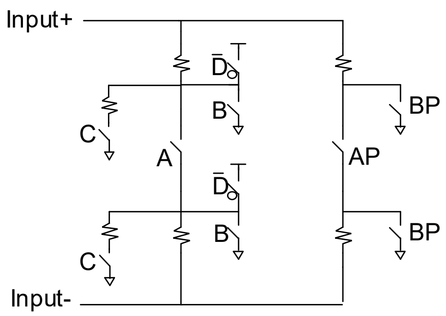


Figure 5. Programmable Input Buffer Logical Diagram

By making appropriate register selections, the switches labeled in Figure 5 can be closed as shown in Table 31 to support the indicated protocols. With the switches closed as indicated, the input buffer will operate as shown in Figure 6 for the various input reference signal protocols. Note that HCSL is used in both 100ohm and 85ohm transmission line environments and this input buffer supports both with no external terminations required.

Table 31. Input Buffer Programming Options for Specific Signaling Protocols

Input Signaling Protocol	Switches Closed	V_{DDR} Voltage Required
2.5V LVPECL	A, C	2.5V
3.3V LVPECL	A, C	3.3V
LVDS (85 ohms)	A, AP	1.8V / 2.5V / 3.3V
LVDS (100 ohms)	A	1.8V / 2.5V / 3.3V
1.8V LVCMOS	-	1.8V
2.5V LVCMOS	-	2.5V

Table 31. Input Buffer Programming Options for Specific Signaling Protocols (Cont.)

Input Signaling Protocol	Switches Closed	V_{DDR} Voltage Required
3.3V LVCMOS	-	3.3V
CML	D	3.3V
HCSL (42.5 ohms)	B, BP	1.8V / 2.5V / 3.3V
HCSL (42 ohms)	B	1.8V / 2.5V / 3.3V
Externally AC-coupled[1]	-	1.8V / 2.5V / 3.3V

1. In this mode of operation, AC-coupling capacitors must be used to isolate the voltage level of the transmitter from the receiver. The signal must be properly terminated on the transmitter side of the AC-coupling capacitors. Bias terminations are needed between the AC-coupling capacitors and the RC2121xA.

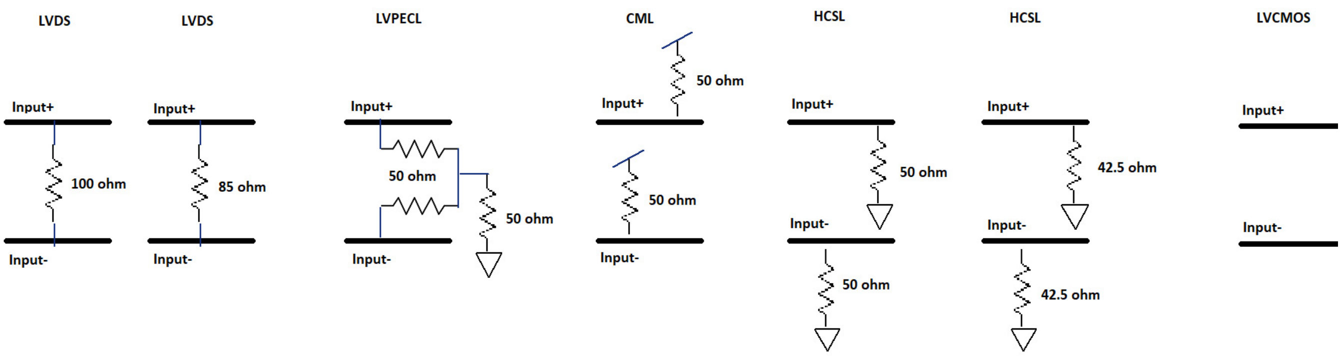


Figure 6. Input Buffer Behavior by Protocol

4.3 Overdriving the XTAL Interface

4.3.1 XTAL Interface Set to Input Buffer (REFIN) Mode

The RC2121xA has two bits to disconnect the internal XO and enable input buffer mode on the XIN_REFIN/XOUT_REFINb and XIN_REFIN0_GPI0/XOUT_REFIN1_GPI1 pins. First, setting sel_ib_xo = 0, disconnects the internal XO. Next, setting xo_ib_cmos_sel = 1 enables the LVCMOS input clock path. Setting these two bits as indicated removes any AC-coupling or input voltage requirements for overdriving the XTAL interface. Note that the maximum input swing is still governed by the VDDX0 and VDDX1 supply rails. When set to Input Buffer Mode, the input can be directly driven with a single-ended or differential oscillator. There is no internal termination capability when using input buffer mode.

4.3.2 XTAL Interface in XO Mode, Input Buffer (REFIN) Mode Not Selected

If the two bits mentioned above are not set as indicated, then there is a limitation of 1.2V on the XIN_REFIN/XOUT_REFINb pins. Input buffer mode is preferred as described in section 4.3.1.

The XIN_REFIN input may be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.2V, and the slew rate must be ≥ 0.2V/ns. For 1.2V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 7. For LVCMOS drivers with > 1.2V swing, the amplitude must be reduced from full swing to less than 1.2V in order to prevent signal interference with the power rail. The sum of the driver output impedance and Rs must equal the transmission line impedance to prevent overshoot and undershoot.

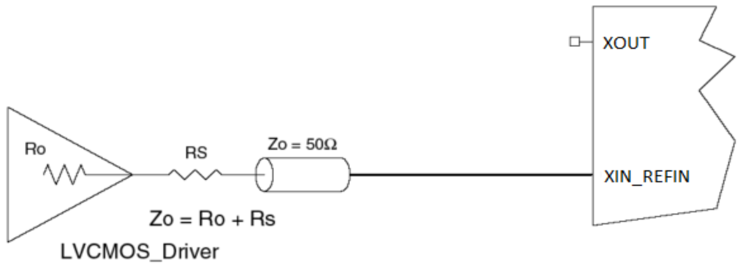


Figure 7. 1.2V LVCMOS Driver to XTAL Input Interface

Figure 8 shows an example of the interface diagram for a high-speed 1.8V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equal the transmission line impedance. In addition, matched termination at the XIN_REFIN input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. Attenuation can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver.

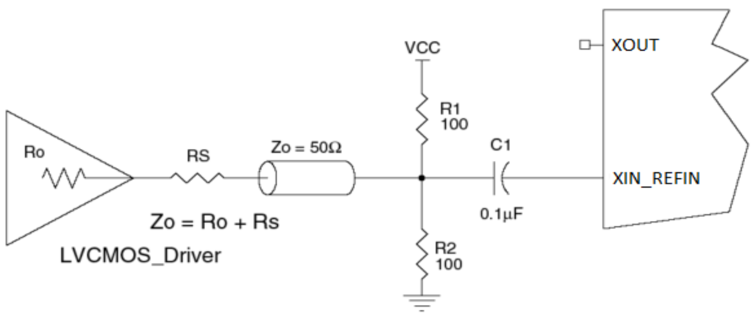


Figure 8. LVCMOS Driver to XTAL Input Interface with Amplitude Attenuation

Figure 9 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN_REFIN input. It is recommended that all components in the schematics be placed in the layout. Though some components may not be used, they can be used for debugging purposes.

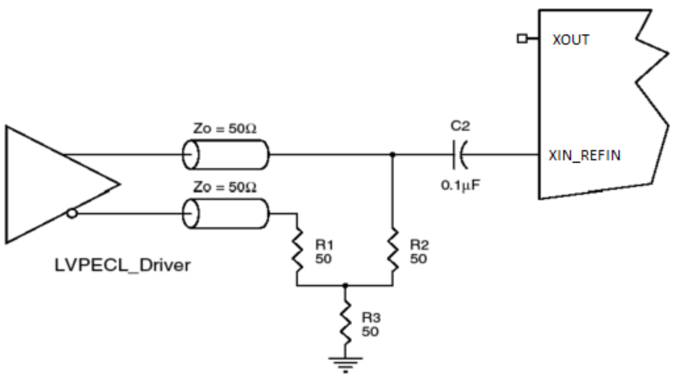


Figure 9. LVPECL Driver to XTAL Input Interface

4.4 Differential Output Termination

4.4.1 Direct-Coupled LP-HCSL Termination

For LP-HCSL differential protocol, the following termination scheme is recommended (see Figure 10). The RC2121xA supports integrated source termination in the figure that presents a differential output impedance of 85 or 100 ohms.

Note: For Rev A silicon with output monitoring is turned on then the LP-HCSL output impedance is ~17 ohms and external series resistors must be used. The monitor looks at the voltage on the output pin and transmission line reflections may interfere with the monitor when the internal terminations are used.

For alternate termination schemes, see *Driving LVPECL, LVDS, CML, and SSTL Logic with Renesas' "Universal" Low-Power HCSL Outputs"* (AN-891) at Renesas.com, or contact Renesas Electronics for support.

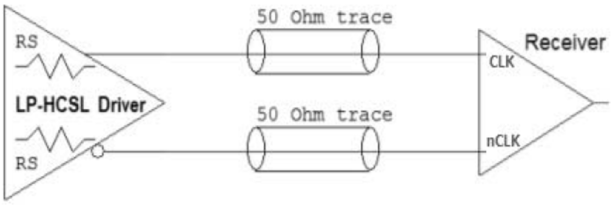


Figure 10. Standard LP-HCSL Termination

4.4.2 Direct-Coupled LVDS Termination

For LVDS differential protocol, the following termination scheme is recommended (see Figure 11). The recommended value for the termination impedance (Z_T) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance (Z_0) of your transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver and a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, the components should be surface-mounted and must be placed as close to the receiver as possible.

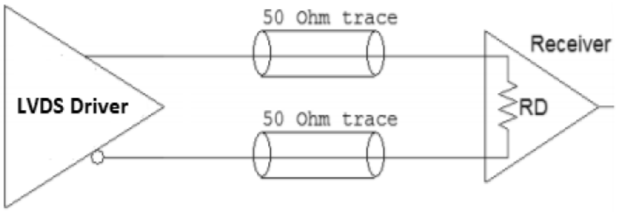


Figure 11. Standard LVDS Termination

For alternate termination schemes, see "LVDS Termination" in *Quick Guide - Output Terminations (AN-953)* located on the RC2121xA product page, or contact Renesas for support.

4.4.3 AC-Coupled Differential Termination

For any other type of differential protocol, AC-coupling should be used as shown in Figure 12, which assumes a 100Ω differential transmission-line environment. The RC2121xA should be programmed in LP-HCSL mode when using AC-coupling, with an appropriate voltage swing selection for the receiver being driven. The device supports a wide range of programmable voltage swing options.

No terminations are needed between the RC2121xA and the AC-coupling capacitors. The resistors on the receiver side of the AC-coupling capacitors should be selected to provide an appropriate voltage bias for the particular receiver. For details, consult the receiver specifications. Finally, a 100Ω resistor across the differential pair (located near the receiver), will attenuate or prevent reflections that may corrupt the clock signal integrity.

It may also be useful to consult *Driving LVPECL, LVDS, CML, and SSTL Logic with Renesas' "Universal" Low-Power HCSL Outputs"* (AN-891) located on the RC2121xA product page, or contact Renesas for support.

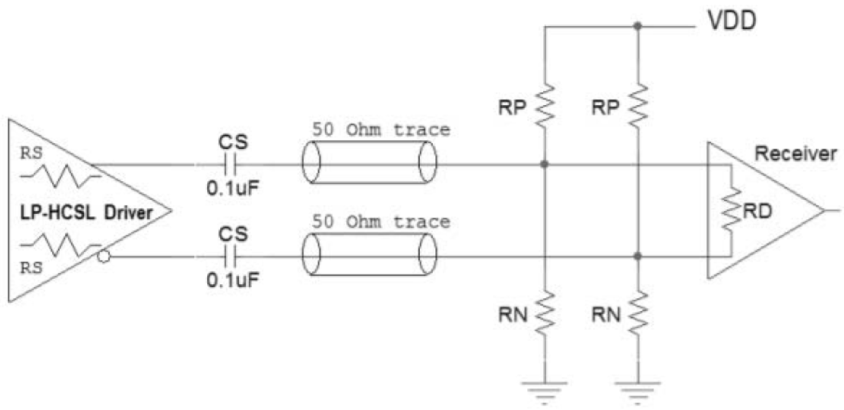


Figure 12. AC-Coupling Termination

It should be noted that many receivers of the type expected to be used with a high-performance device like the RC2121xA are equipped with internal terminations that can include trace termination, voltage biasing, and even AC-coupling in some cases. Please consult with the receiver specifications to determine if any or all of the above indicated external components are needed.

4.5 Crystal Recommendation

For the latest vendor / frequency recommendations, please contact Renesas.

4.6 Power Considerations

The electrical characteristics tables provide current consumption values for various blocks and output configurations, and can be used to estimate total current consumption for a particular design. The Renesas IC Toolbox, available on the Renesas website, can also be used to estimate current consumption.

Note: In this section, the term “power rail” refers to the power connection to a particular VDD pin. This means that different VDD pins may be connected to the same voltage, yet may also be connected to different power rails. “Power rail” is also used when discussing power sequencing considerations.

4.6.1 Power Sequencing Considerations

The power sequencing considerations must be followed to ensure robust operation of the RC2121xA. When the entire RC2121xA is powered from a single power rail, these considerations are easy to meet. For applications where multiple supply rails are used, meeting these considerations requires a bit of planning.

Renesas recommends ramping the VDDA and VDDD power supply rails at the same time. They do not need to be the same voltage, although they may be. In all cases VDDA must be ≤ VDD. Logic powered by the VDDA/VDDD pins controls the internal reset sequencer. After the VDDA/VDDD rails ramp, the VDDO rails need to ramp within $t_{VDDODLY}$ of the VDDA/VDDD rails. This means the VDDO rails may ramp at the same time as the VDDA/VDDD rails, or may be delayed as much as 4ms. The reference voltage for measuring the ramp is 1.62V regardless of the supply voltage. Figure 13 shows the power supply timing requirements.

For power and current consumption calculations, refer to the Renesas IC Toolbox on the Renesas website.

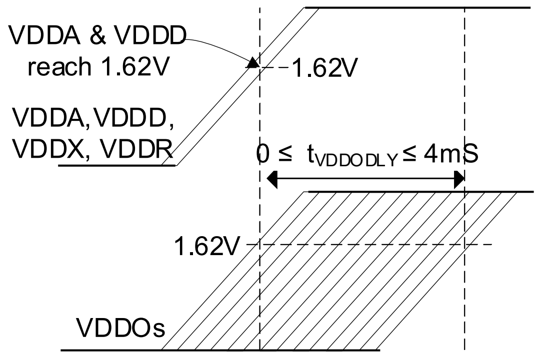


Figure 13. Power Supply Sequencing without PWRGD/PWRDN# or PWRGD/RESTART#

5. Thermal Information

5.1 Epad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e., “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern.

Note: These recommendations are to be used as a guideline only. For additional information, see the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

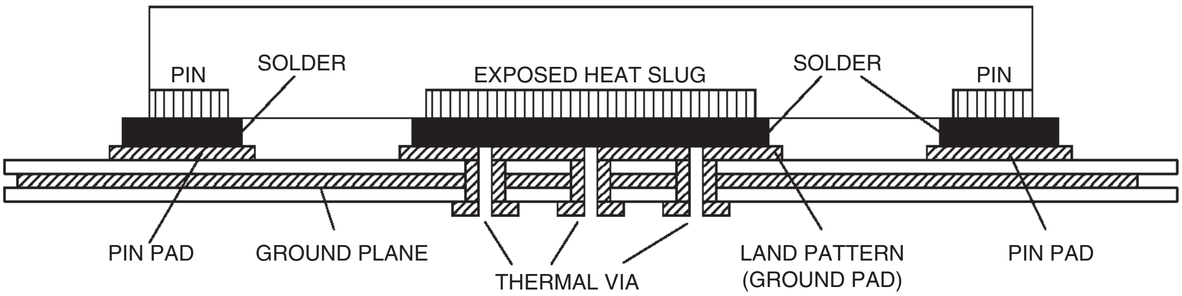


Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (Drawing not to Scale)

5.2 Thermal Characteristics

Table 32. Thermal Characteristics (48-pin) [1]

Symbol	Parameter	Value	Unit
θ_{JC}	Junction to Device Case Thermal Coefficient [2]	20.1	°C/W
θ_{JB}	Junction to Board Thermal Coefficient [2]	1.9	
θ_{JA}	Junction to Ambient Air Thermal Coefficient (still air)	25.2	
	Junction to Ambient Air Thermal Coefficient (1 m/s airflow)	21.7	
	Junction to Ambient Air Thermal Coefficient (2 m/s airflow)	20.2	
	Junction to Ambient Air Thermal Coefficient (3 m/s airflow)	19.3	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePAD is connected to a ground plane using a grid of 25 thermal vias.

Table 33. Thermal Characteristics (40-pin) [1]

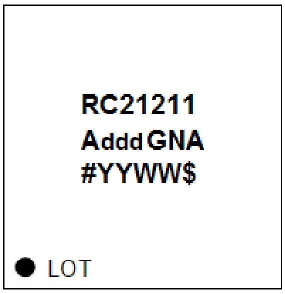
Symbol	Parameter	Value	Unit
θ_{JC}	Junction to Device Case Thermal Coefficient [2]	26.9	°C/W
θ_{JB}	Junction to Board Thermal Coefficient [2]	1.3	
θ_{JA}	Junction to Ambient Air Thermal Coefficient (still air)	30.5	
	Junction to Ambient Air Thermal Coefficient (1 m/s air flow)	26.8	
	Junction to Ambient Air Thermal Coefficient (2 m/s air flow)	25.2	
	Junction to Ambient Air Thermal Coefficient (3m/s air flow)	24.3	
-	Moisture Sensitivity Rating (Per J-STD-020)	3	

1. Multi-Layer PCB with two ground and two voltage planes.
2. Assumes ePAD is connected to a ground plane using a grid of 16 thermal vias.

6. Package Outline Drawings

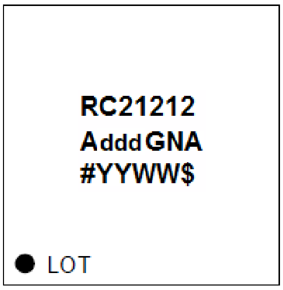
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

7. Marking Diagrams



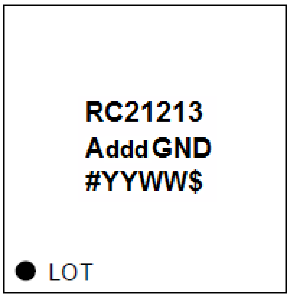
RC21211A

- Lines 1 and 2: part number.
  - "ddd" indicates preprogrammed device custom configuration dash code.
- Line 3:
  - "#" indicates the stepping number.
  - "YYWW" indicates the last two digits of the year and work week the part was assembled.
  - "$" indicates the mark code.



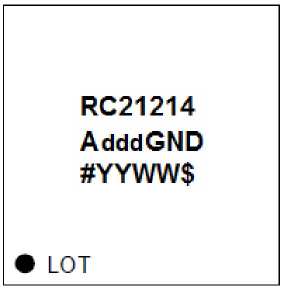
RC21212A

- Lines 1 and 2: part number.
  - "ddd" indicates preprogrammed device custom configuration dash code.
- Line 3:
  - "#" indicates the stepping number.
  - "YYWW" indicates the last two digits of the year and work week the part was assembled.
  - "$" indicates the mark code.



RC21213A

- Lines 1 and 2: part number.
  - "ddd" indicates preprogrammed device custom configuration dash code.
- Line 3:
  - "#" indicates the stepping number.
  - "YYWW" indicates the last two digits of the year and work week the part was assembled.
  - "$" indicates the mark code.



RC21214A

- Lines 1 and 2: part number.
  - "ddd" indicates preprogrammed device custom configuration dash code.
- Line 3:
  - "#" indicates the stepping number.
  - "YYWW" indicates the last two digits of the year and work week the part was assembled.
  - "$" indicates the mark code.

8. Ordering Information

Table 34. Ordering Information

Part Number [1]	Description	XTALs	Carrier Type	Package	Temp. Range
RC21211A000GNA#BB0	12-output Unprogrammed part	1	Tray	6 × 6 × 0.75 mm 48-VFQFN Wettable flank	-40° to +105°C
RC21211A000GNA#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21211AdddGNA#BB0	12-output Preprogrammed part		Tray		
RC21211AdddGNA#KB0			Tape and Reel, Pin Orientation: EIA-481-D		
RC21212A000GNA#BB0	12-output Unprogrammed Part	2	Tray		
RC21212A000GNA#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21212AdddGNA#BB0	12-output Preprogrammed part		Tray		
RC21212AdddGNA#KB0			Tape and Reel, Pin 1Orientation: EIA-481-D		
RC21213A000GND#BB0	8-output Unprogrammed part	1	Tray	5 × 5 × 0.75 mm 40-VFQFN Wettable flank	-40° to +105°C
RC21213A000GND#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21213AdddGND#BB0	8-output Preprogrammed part		Tray		
RC21213AdddGND#KB0			Tape and Reel, Pin Orientation: EIA-481-D		
RC21214A000GND#BB0	8-output Unprogrammed Part	2	Tray		
RC21214A000GND#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D		
RC21214AdddGND#BB0	8-output Preprogrammed part		Tray		
RC21214AdddGND#KB0			Tape and Reel, Pin 1 Orientation: EIA-481-D		

1. Replace "ddd" with the desired pre-programmed configuration code provided by Renesas in response to a custom configuration request.

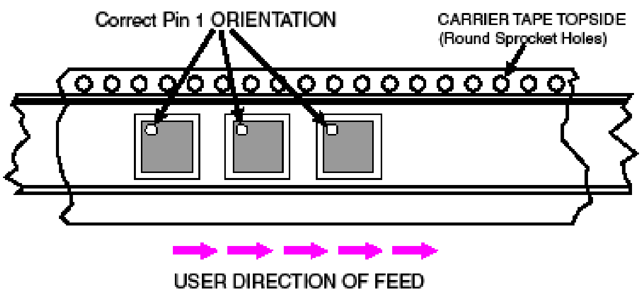


Figure 15. Pin 1 Orientation in Tape and Reel Packaging

Table 35. Product Identification

Part Number	Product ID
RC21211	212B
RC21212	212C
RC21213	212D
RC21214	212E

9. Revision History

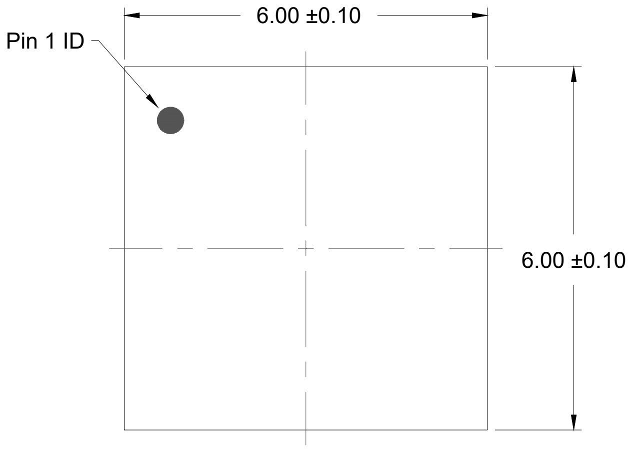
Revision	Date	Description
1.01	Apr 24, 2024	Completed minor changes to the front matter.
1.00	Apr 4, 2024	Initial release.

Package Outline Drawing

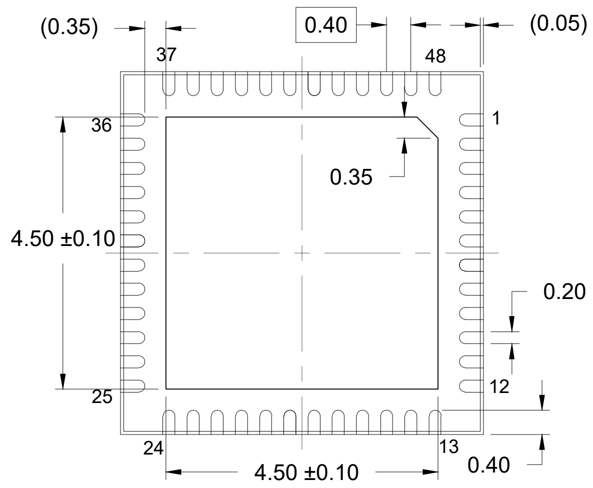
Package Code: NTG48S2

48-VFQFPN 6.0 x 6.0 x 0.75 mm Body, 0.4mm Pitch

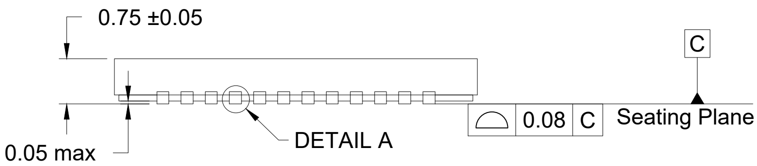
PSC-4294-03, Revision: 02, Date Created: Dec 05, 2023



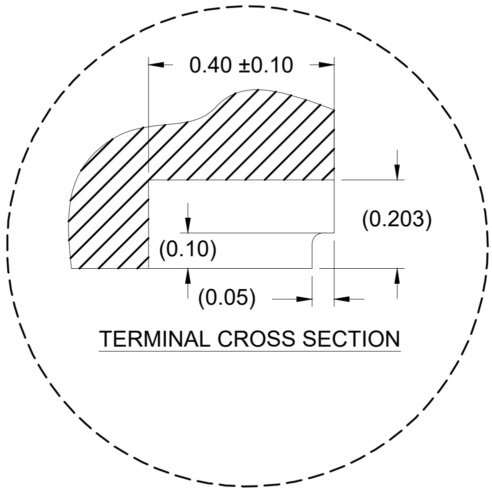
TOP VIEW



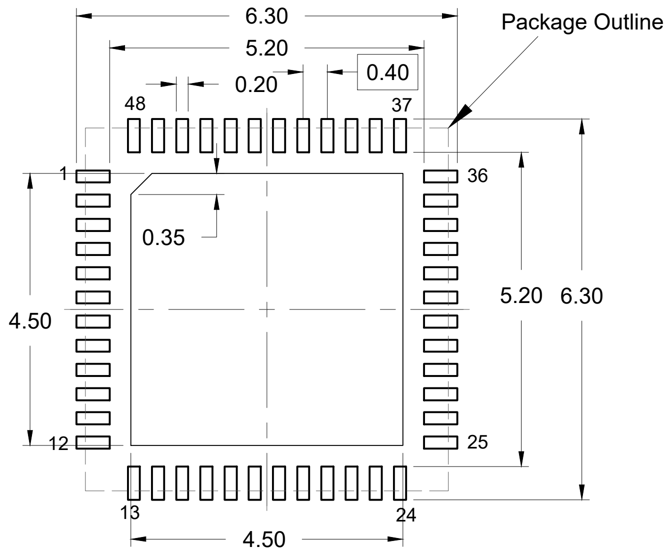
BOTTOM VIEW



SIDE VIEW



DETAIL A: WETTABLE FLANK OPTION



RECOMMENDED LAND PATTERN

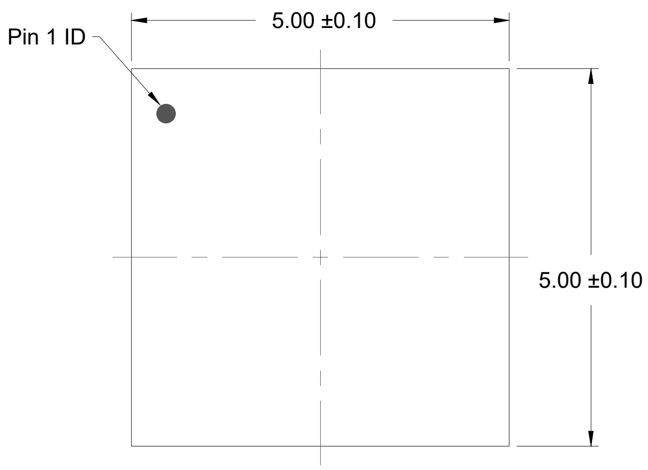
(PCB Top View, NSMD Design)

NOTES:

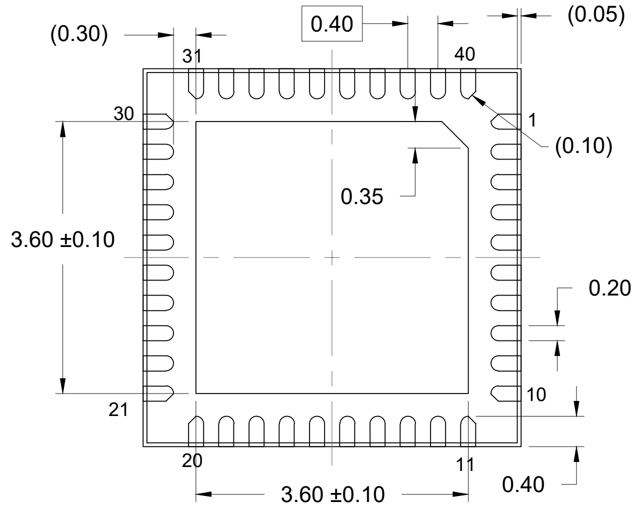
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Package Outline Drawing

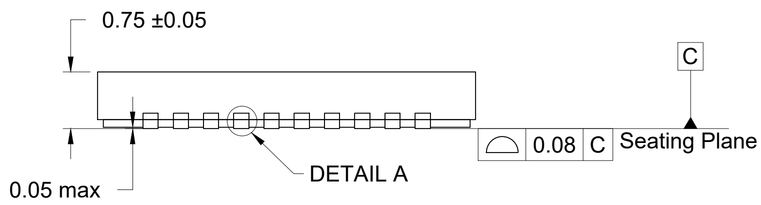
Package Code: NTG40S1
40-VFQFPN 5.0 x 5.0 x 0.75 mm Body, 0.4mm Pitch
PSC-4295-03, Revision: 02, Date Created: Dec 05, 2023



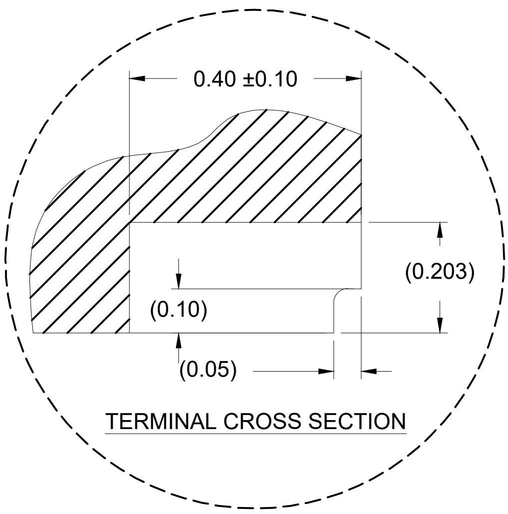
TOP VIEW



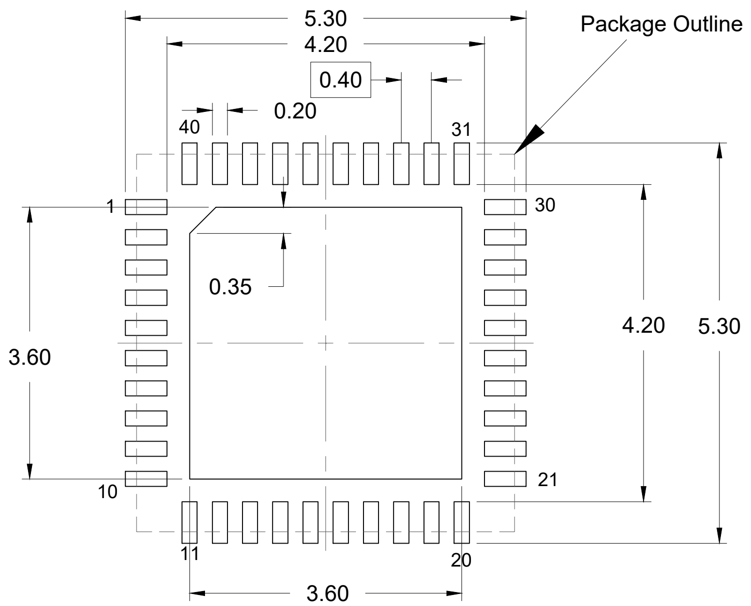
BOTTOM VIEW



SIDE VIEW



DETAIL A: WETTABLE FLANK OPTION



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

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