Datasheet

# RC310xxB

VersaClock 7 Programmable Jitter Attenuator Family

The RC310xxB are high-performance programmable jitter attenuators with network synchronization capabilities. The devices support JEDEC JESD204B/C for converter synchronization, and SyncE for network-based synchronization.

The RC310xxB are ideal for driving converter circuits in wire-line infrastructure, data center equipment, and instrumentation applications.

## Applications

- Switches / Routers
- Synchronous Ethernet (SyncE) equipment
- Telecom Time Slave Clock (T-TSC) equipment
- Jitter attenuation for 10 / 25 / 40 / 100 / 200 / 400 Gbps Ethernet PHYs or Switches
- Small Cell for 4.5G and 5G

## Features

- 169fs RMS typical phase jitter
- PCIe® Gen6 Common Clock (CC) 27fs RMS
- Compliant with ITU-T G.8262 and G.8262.1 for synchronous Ethernet Equipment Clock (EEC/eEEC)
- Jitter attenuation with programmable loop bandwidth from 0.1Hz to 12kHz
- 1kHz to 650MHz LVDS/LP-HCSL outputs
- 1kHz to 200MHz LVCMOS outputs
- Simple AC-coupling to LVPECL and CML
- Integrated 100Ω and 85Ω LP-HCSL terminations
- JESD204B/C support on differential or single-ended outputs with DC-coupling or AC-coupling
- Up to four single-ended or two differential clock inputs; one crystal/TCXO/OCXO input
- 1MHz I2C, 400kHz SMBus or 20MHz SPI support
- Configuration via factory-programmed One-Time Programmable (OTP) memory, serial interface, or external I2C EEPROM
- OTP holds up to four complete or 27 partial configurations
- 1.8V, 2.5V, 3.3V, -40° to +85°C operation
- RC31012B – 12 output pairs/24 single-ended outputs
  - 6 × 6 mm 48-QFN, integrated crystal option
- RC31008B – 8 differential/16 single-ended outputs
  - 5 × 5 mm 40-QFN, integrated crystal option
- RC31005B – 5 differential/10 single-ended outputs
  - 4 × 4 mm 32-LGA with integrated crystal

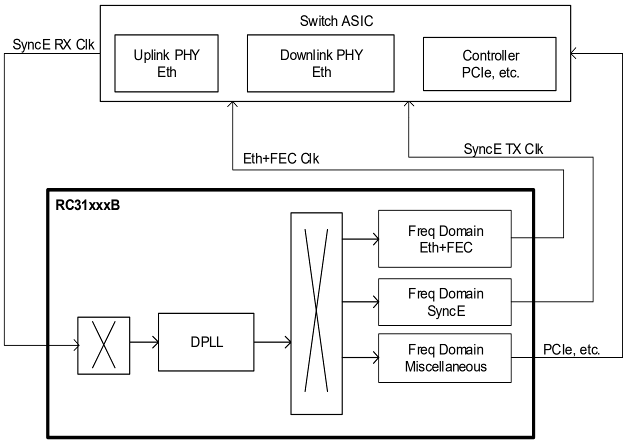
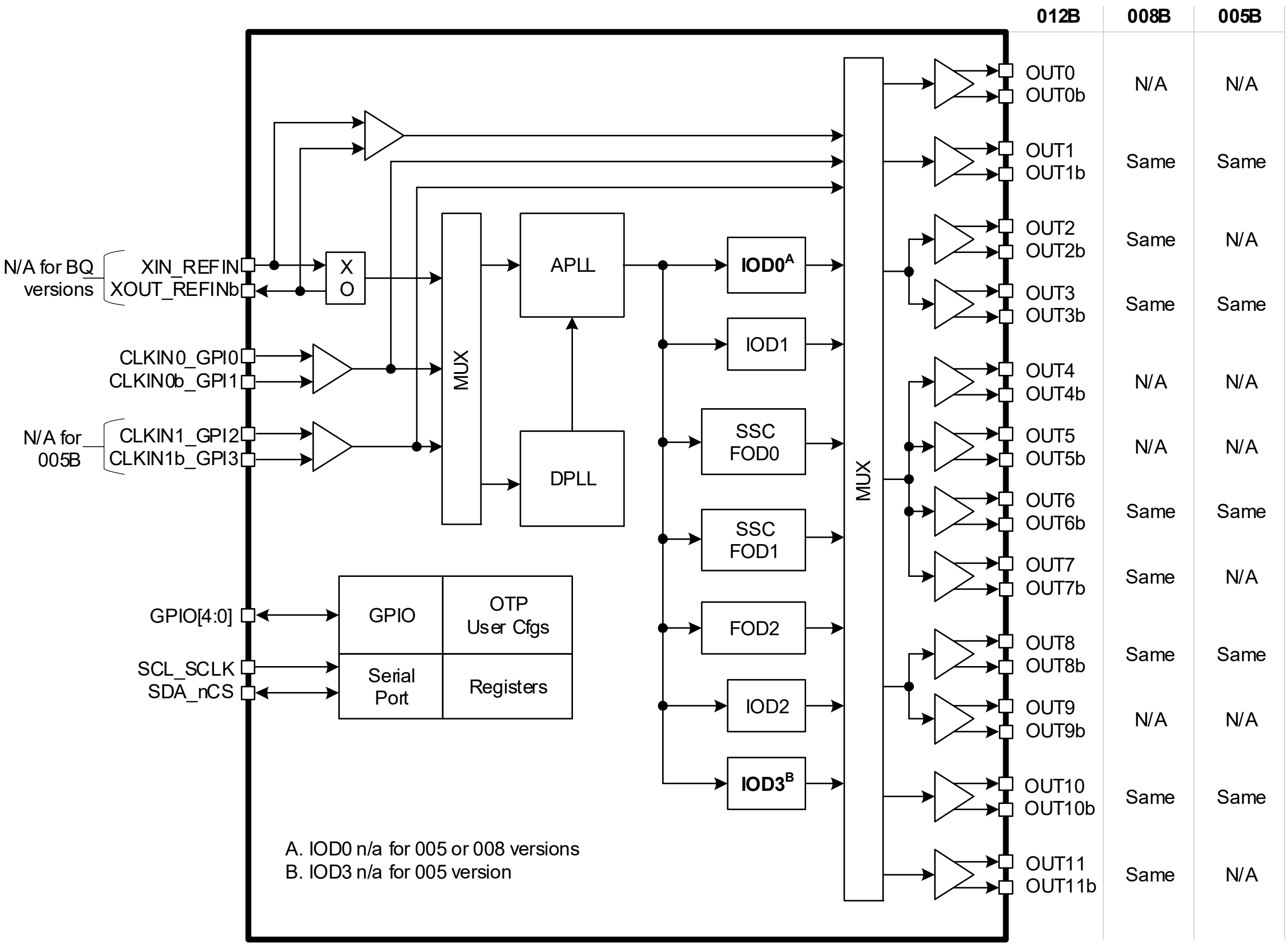


**Figure 1. Typical Wire-line Infrastructure Use Case**

## RC310xxB Block Diagram



A. IOD0 n/a for 005 or 008 versions
B. IOD3 n/a for 005 version

| 012B | 008B | 005B |
|---|---|---|
| OUT0<br>OUT0b | N/A | N/A |
| OUT1<br>OUT1b | Same | Same |
| OUT2<br>OUT2b | Same | N/A |
| OUT3<br>OUT3b | Same | Same |
| OUT4<br>OUT4b | N/A | N/A |
| OUT5<br>OUT5b | N/A | N/A |
| OUT6<br>OUT6b | Same | Same |
| OUT7<br>OUT7b | Same | N/A |
| OUT8<br>OUT8b | Same | Same |
| OUT9<br>OUT9b | N/A | N/A |
| OUT10<br>OUT10b | Same | Same |
| OUT11<br>OUT11b | Same | N/A |

**Figure 2. RC310xxB Block Diagram**

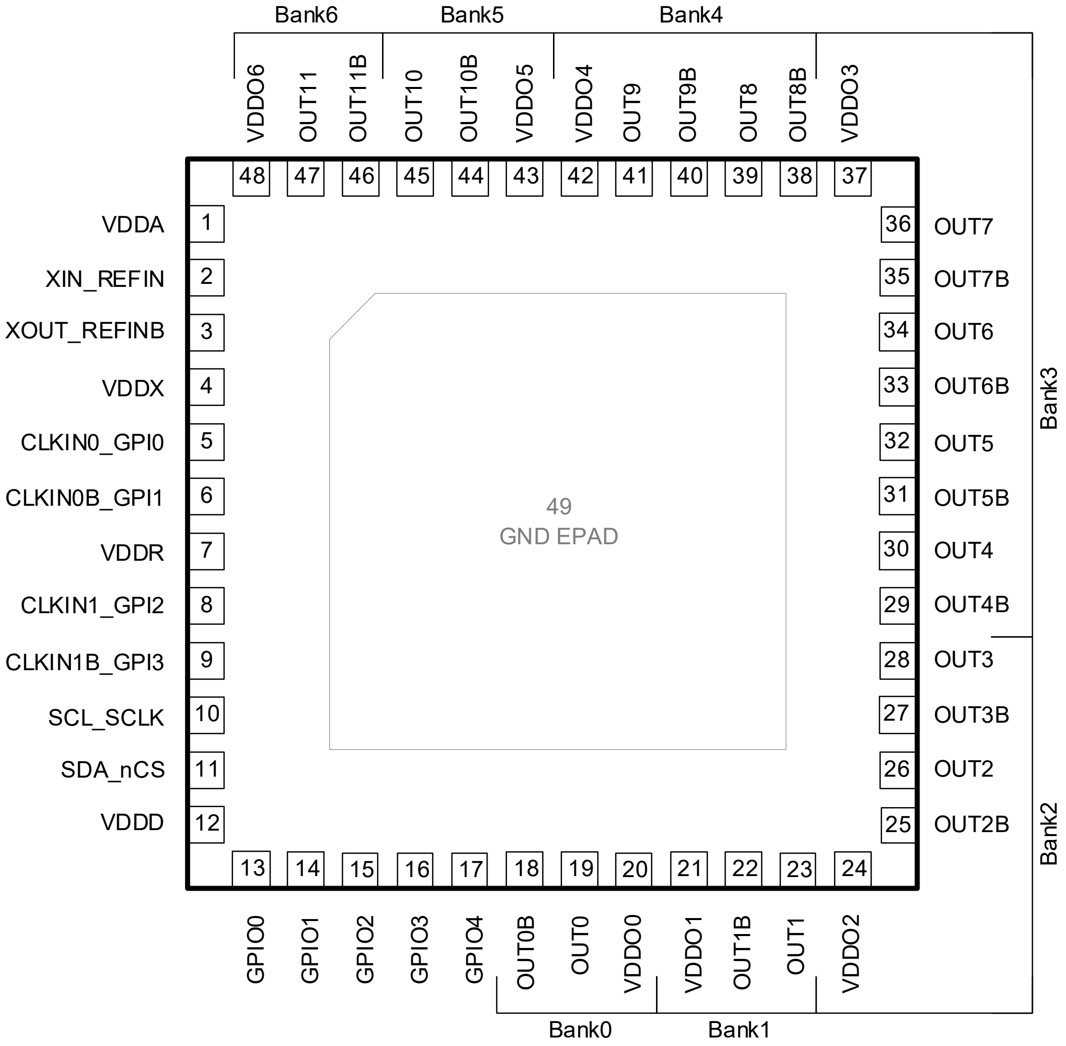
# Contents

# Figures

# Tables

# 1. Pin Information

## 1.1 Pin Assignments – RCxxx12B (Top View)



## 1.2 Pin Descriptions – RCxxx12B

Table 1. RCxxx12B Pin Descriptions

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | VDDA | Power | Analog power supply. SeeTable 8 for supported voltages. |
| 2 | XIN_REFIN | I | Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input. |
| 3 | XOUT_REFINb | I/O | Crystal Output or differential reference clock negative input.<br>This pin should be connected to a crystal. If an oscillator is connected to XIN_REFIN, then this pin must be left unconnected. |
| 4 | VDDX | Power | Crystal oscillator power supply. See Table 8 for supported voltages. |
| 5 | CLKIN0_GPI0 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI0. |
| 6 | CLKIN0b_GPI1 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1. |

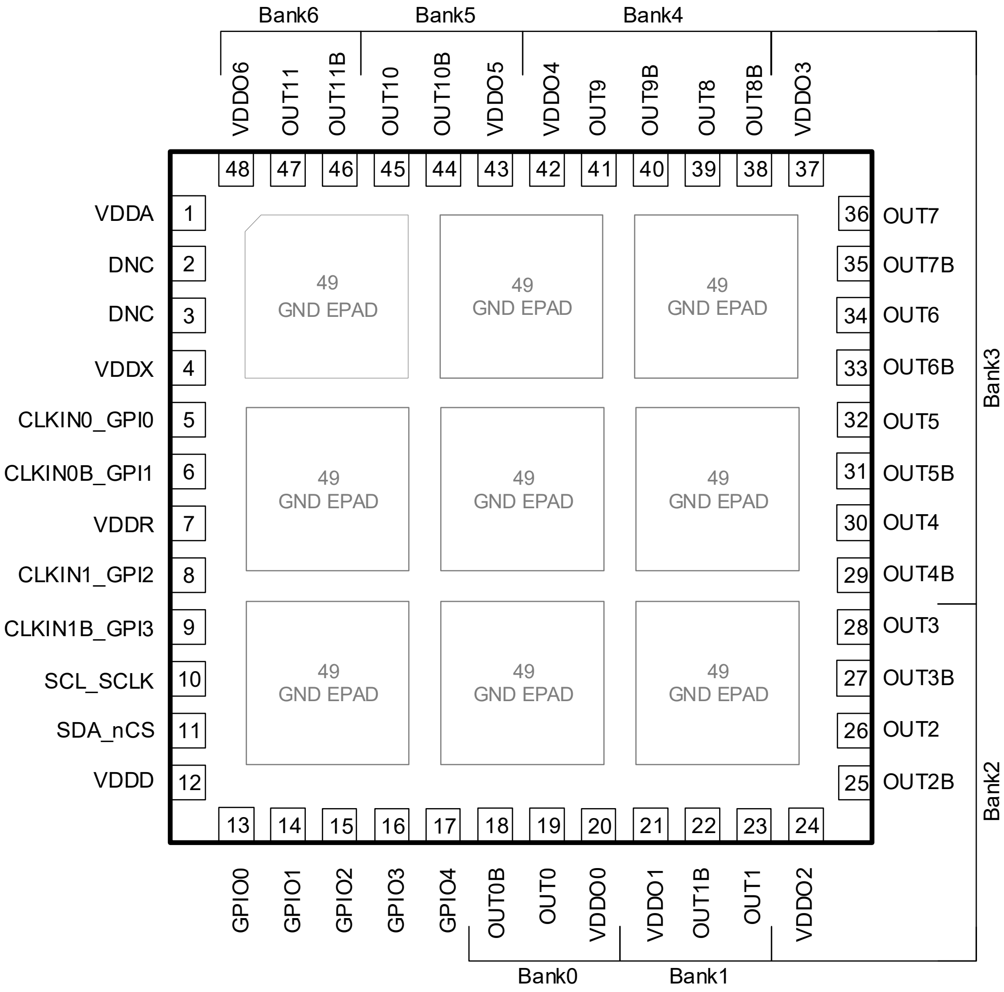
**Table 1. RCxxx12B Pin Descriptions (Cont.)**

| Number | Name | Type | Description |
|---|---|---|---|
| 7 | VDDR | Power | CLKIN (receiver) power supply. See Table 8 for supported voltages. |
| 8 | CLKIN1_GPI2 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2. |
| 9 | CLKIN1b_GPI3 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3. |
| 10 | SCL_SCLK | I | I2C Mode: I$^2$C interface bi-directional clock.<br>SPI Mode: Serial Clock<br>This pin is 3.3V tolerant. |
| 11 | SDA_nCS | I | I2C Mode: I$^2$C interface bi-directional data in open-drain mode. SPI Mode: Chip Select (active low)<br>This pin is 3.3V tolerant. |
| 12 | VDDD | Power | Digital core and GPIO power supply. See Table 8 for supported voltages. When programming the OTP, this supply must be 2.5V or 3.3V. |
| 13 | GPIO0 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 14 | GPIO1 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 15 | GPIO2 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 16 | GPIO3 | I/O | General purpose input/output. |
| 17 | GPIO4 | I/O | General purpose input/output. |
| 18 | nOUT0b | O | Output Clock 0 negative. |
| 19 | OUT0 | O | Output Clock 0 positive. |
| 20 | VDDO0 | Power | Power supply for output bank 0 and IOD 0. See Table 8 for supported voltages. |
| 21 | VDDO1 | Power | Power supply for output bank 1 and IOD 1. See Table 8 for supported voltages. |
| 22 | OUT1b | O | Output Clock 1 negative. |
| 23 | OUT1 | O | Output Clock 1 positive. |
| 24 | VDDO2 | Power | Power supply for output bank 2 and FOD 0. See Table 8 for supported voltages. |
| 25 | OUT2b | O | Output Clock 2 negative. |
| 26 | OUT2 | O | Output Clock 2 positive. |
| 27 | OUT3b | O | Output Clock 3 negative. |
| 28 | OUT3 | O | Output Clock 3 positive. |
| 29 | OUT4b | O | Output Clock 4 negative. |
| 30 | OUT4 | O | Output Clock 4 positive. |
| 31 | OUT5b | O | Output Clock 5 negative. |
| 32 | OUT5 | O | Output Clock 5 positive. |
| 33 | OUT6b | O | Output Clock 6 negative. |
| 34 | OUT6 | O | Output Clock 6 positive. |
| 35 | OUT7b | O | Output Clock 7 negative. |
| 36 | OUT7 | O | Output Clock 7 positive. |

Table 1. RCxxx12B Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 37 | VDDO3 | Power | Power supply for output bank 3 and FOD 1. See Table 8 for supported voltages. |
| 38 | OUT8b | O | Output Clock 8 negative. |
| 39 | OUT8 | O | Output Clock 8 positive. |
| 40 | OUT9b | O | Output Clock 9 negative. |
| 41 | OUT9 | O | Output Clock 9 positive. |
| 42 | VDDO4 | Power | Power supply for output bank 4 and FOD 2. See Table 8 for supported voltages. |
| 43 | VDDO5 | Power | Power supply for output bank 5 and IOD 2. See Table 8 for supported voltages. |
| 44 | OUT10b | O | Output Clock 10 negative. |
| 45 | OUT10 | O | Output Clock 10 positive. |
| 46 | OUT11b | O | Output Clock 11 negative. |
| 47 | OUT11 | O | Output Clock 11 positive. |
| 48 | VDDO6 | Power | Supply voltage for output bank 6 and IOD 3. See Table 8 for supported voltages. |
| EPAD | GND | Power | Ground. ePad must be connected to ground before any VDD is applied. |

## 1.3 Pin Assignments – RCxxx12BQ (Top View)



## 1.4 Pin Descriptions – RCxxx12BQ

**Table 2. RCxxx12B Pin Descriptions**

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | VDDA | Power | Analog power supply. See Table 8 for supported voltages. |
| 2 | DNC | N/A | Do not connect. This pin should have no stubs. |
| 3 | DNC | N/A | Do not connect. This pin should have no stubs. |
| 4 | VDDX | Power | Crystal oscillator power supply. See Table 8 for supported voltages. |
| 5 | CLKIN0_GPI0 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI0. |
| 6 | CLKIN0b_GPI1 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1. |
| 7 | VDDR | Power | CLKIN (receiver) power supply. See Table 8 for supported voltages. |
| 8 | CLKIN1_GPI2 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2. |
| 9 | CLKIN1b_GPI3 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3. |

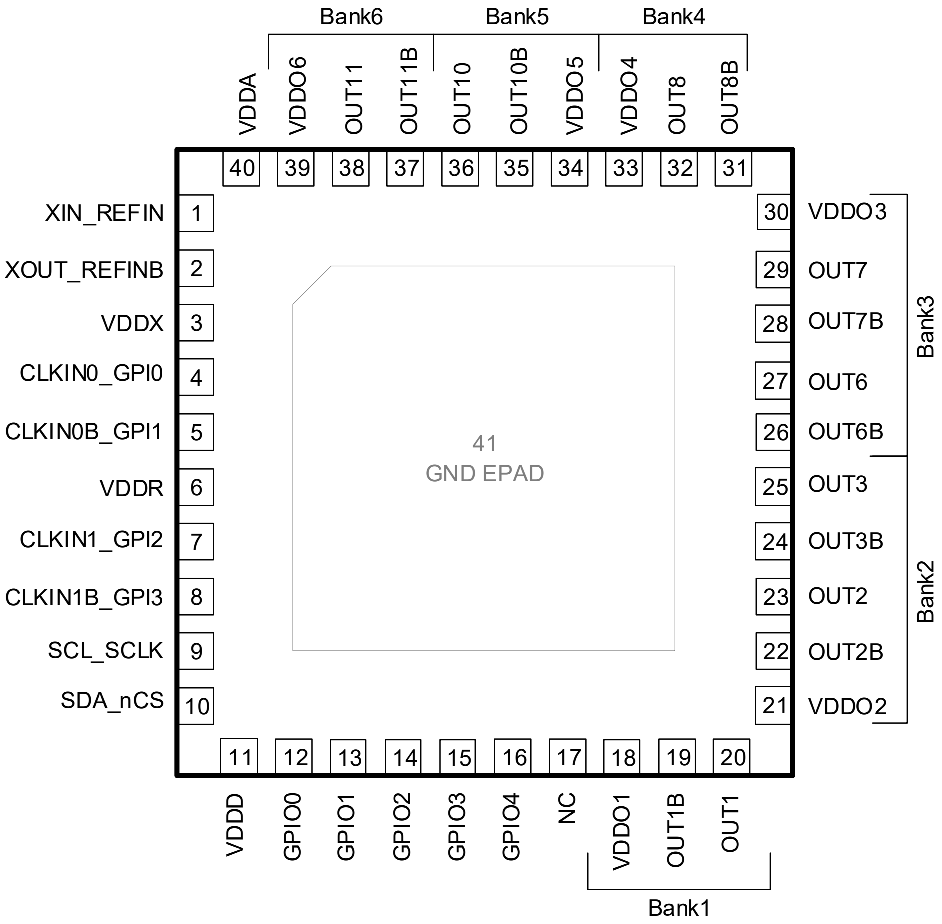
**Table 2. RCxxx12B Pin Descriptions (Cont.)**

| Number | Name | Type | Description |
|---|---|---|---|
| 10 | SCL_SCLK | I | I2C Mode: I$^2$C interface bi-directional clock.<br>SPI Mode: Serial Clock<br>This pin is 3.3V tolerant. |
| 11 | SDA_nCS | I | I2C Mode: I$^2$C interface bi-directional data in open-drain mode. SPI Mode: Chip Select (active low)<br>This pin is 3.3V tolerant. |
| 12 | VDDD | Power | Digital core and GPIO power supply. See Table 8 for supported voltages. When programming the OTP, this supply must be 2.5V or 3.3V. |
| 13 | GPIO0 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 14 | GPIO1 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 15 | GPIO2 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 16 | GPIO3 | I/O | General purpose input/output. |
| 17 | GPIO4 | I/O | General purpose input/output. |
| 18 | nOUT0b | O | Output Clock 0 negative. |
| 19 | OUT0 | O | Output Clock 0 positive. |
| 20 | VDDO0 | Power | Power supply for output bank 0 and IOD 0. See Table 8 for supported voltages. |
| 21 | VDDO1 | Power | Power supply for output bank 1 and IOD 1. See Table 8 for supported voltages. |
| 22 | OUT1b | O | Output Clock 1 negative. |
| 23 | OUT1 | O | Output Clock 1 positive. |
| 24 | VDDO2 | Power | Power supply for output bank 2 and FOD 0. See Table 8 for supported voltages. |
| 25 | OUT2b | O | Output Clock 2 negative. |
| 26 | OUT2 | O | Output Clock 2 positive. |
| 27 | OUT3b | O | Output Clock 3 negative. |
| 28 | OUT3 | O | Output Clock 3 positive. |
| 29 | OUT4b | O | Output Clock 4 negative. |
| 30 | OUT4 | O | Output Clock 4 positive. |
| 31 | OUT5b | O | Output Clock 5 negative. |
| 32 | OUT5 | O | Output Clock 5 positive. |
| 33 | OUT6b | O | Output Clock 6 negative. |
| 34 | OUT6 | O | Output Clock 6 positive. |
| 35 | OUT7b | O | Output Clock 7 negative. |
| 36 | OUT7 | O | Output Clock 7 positive. |
| 37 | VDDO3 | Power | Power supply for output bank 3 and FOD 1. See Table 8 for supported voltages. |
| 38 | OUT8b | O | Output Clock 8 negative. |
| 39 | OUT8 | O | Output Clock 8 positive. |
| 40 | OUT9b | O | Output Clock 9 negative. |

Table 2. RCxxx12B Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 41 | OUT9 | O | Output Clock 9 positive. |
| 42 | VDDO4 | Power | Power supply for output bank 4 and FOD 2. See Table 8 for supported voltages. |
| 43 | VDDO5 | Power | Power supply for output bank 5 and IOD 2. See Table 8 for supported voltages. |
| 44 | OUT10b | O | Output Clock 10 negative. |
| 45 | OUT10 | O | Output Clock 10 positive. |
| 46 | OUT11b | O | Output Clock 11 negative. |
| 47 | OUT11 | O | Output Clock 11 positive. |
| 48 | VDDO6 | Power | Supply voltage for output bank 6 and IOD 3. See Table 8 for supported voltages. |
| EPAD | GND | Power | Ground. ePad must be connected to ground before any VDD is applied. |

## 1.5 Pin Assignments – RCxxx08B (Top View)



## 1.6 Pin Descriptions – RCxxx08B

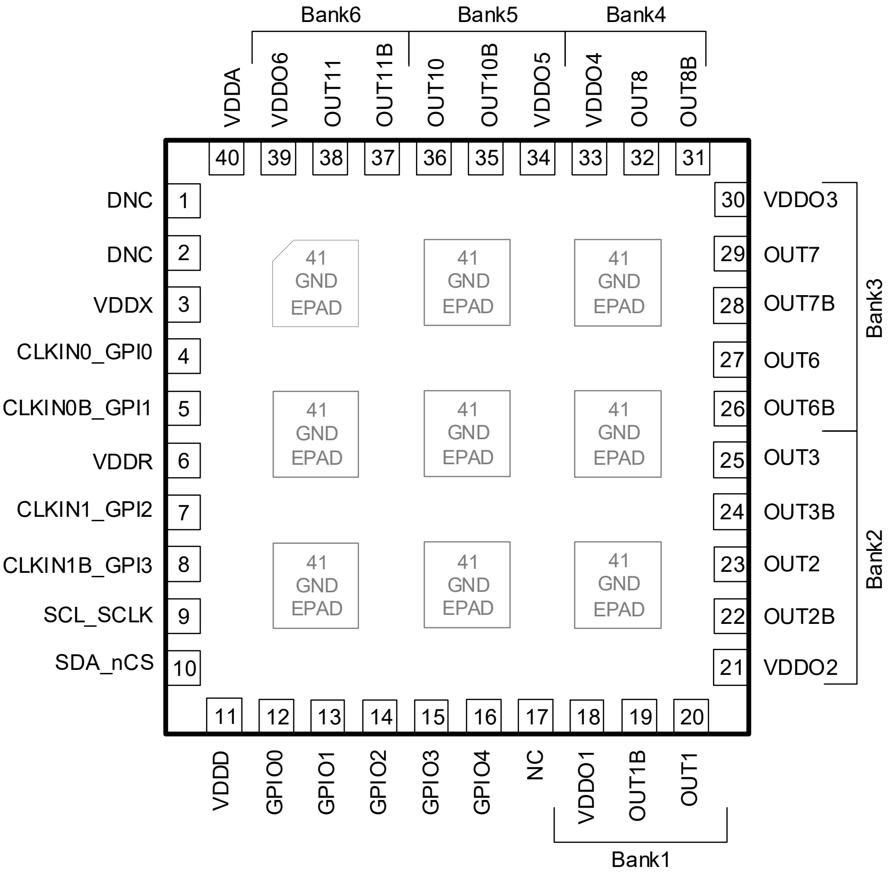
**Table 3. RCxxx08B Pin Descriptions**

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | XIN_REFIN | I | Crystal Input or differential reference clock positive input / CMOS single-ended reference clock input. |
| 2 | XOUT_REFINb | I/O | Crystal Output or differential reference clock negative input.<br>This pin should be connected to a crystal. If an oscillator is connected to XIN_REFIN, then this pin must be left unconnected. |
| 3 | VDDX | Power | Crystal oscillator power supply. See Table 8 for supported voltages. |
| 4 | CLKIN0_GPI0 | I | differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI0. |
| 5 | CLKIN0b_GPI1 | I | differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1. |
| 6 | VDDR | Power | CLKIN (receiver) power supply. See Table 8 for supported voltages. |
| 7 | CLKIN1_GPI2 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2. |
| 8 | CLKIN1b_GPI3 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3. |
| 9 | SCL_SCLK | I | I2C Mode: I$^2$C interface bi-directional clock.<br>SPI Mode: Serial Clock<br>This pin is 3.3V tolerant. |

Table 3. RCxxx08B Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 10 | SDA_nCS | I/O | I2C Mode: I$^2$C interface bi-directional data in open-drain mode.<br>SPI Mode: Chip Select (active low)<br>This pin is 3.3V tolerant. |
| 11 | VDDD | Power | Digital core and GPIO power supply. See Table 8 for supported voltages. When programming the OTP, this supply must be 2.5V or 3.3V. |
| 12 | GPIO0 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 13 | GPIO1 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 14 | GPIO2 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 15 | GPIO3 | I/O | General purpose input/output. |
| 16 | GPIO4 | I/O | General purpose input/output. |
| 17 | NC | I | Not connected. |
| 18 | VDDO1 | Power | Power supply for output bank 1 and IOD 1. See Table 8 for supported voltages. |
| 19 | OUT1b | O | Output Clock 1 negative. |
| 20 | OUT1 | O | Output Clock 1 positive |
| 21 | VDDO2 | Power | Power supply for output bank 2 and FOD 0. See Table 8 for supported voltages. |
| 22 | OUT2b | O | Output Clock 2 negative. |
| 23 | OUT2 | O | Output Clock 2 positive. |
| 24 | OUT3b | O | Output Clock 3 negative. |
| 25 | OUT3 | O | Output Clock 3 positive. |
| 26 | OUT6b | O | Output Clock 6 negative. |
| 27 | OUT6 | O | Output Clock 6 positive. |
| 28 | OUT7b | O | Output Clock 7 negative. |
| 29 | OUT7 | O | Output Clock 7 positive. |
| 30 | VDDO3 | Power | Power supply for output bank 3 and FOD 1. See Table 8 for supported voltages. |
| 31 | OUT8b | O | Output Clock 8 negative. |
| 32 | OUT8 | O | Output Clock 8 positive. |
| 33 | VDDO4 | Power | Power supply for output bank 4 and FOD 2. See Table 8 for supported voltages. |
| 34 | VDDO5 | Power | Power supply for output bank 5 and IOD 2. See Table 8 for supported voltages. |
| 35 | OUT10b | O | Output Clock 10 negative. |
| 36 | OUT10 | O | Output Clock 10 positive. |
| 37 | OUT11b | O | Output Clock 11 negative. |
| 38 | OUT11 | O | Output Clock 11 positive. |
| 39 | VDDO6 | Power | Supply voltage for output bank 6 and IOD 3. See Table 8 for supported voltages. |
| 40 | VDDA | Power | Analog power supply. See Table 8 for supported voltages. |
| EPAD | GND | Power | Ground. ePad must be connected to ground before any VDD is applied. |

## 1.7 Pin Assignments – RCxxx08BQ (Top View)



## 1.8 Pin Descriptions – RCxxx08BQ

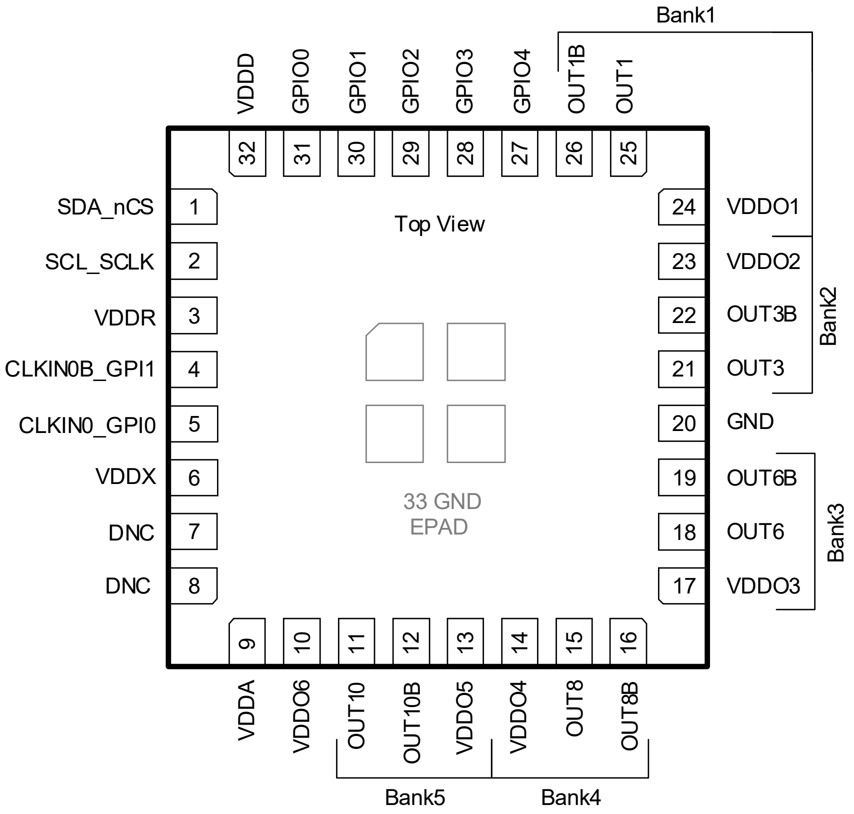
**Table 4. RCxxx08BQ Pin Descriptions**

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | DNC | N/A | Do not connect. This pin should have no stubs. |
| 2 | DNC | N/A | Do not connect. This pin should have no stubs. |
| 3 | VDDX | Power | Crystal oscillator power supply. See Table 8 for supported voltages. |
| 4 | CLKIN0_GPI0 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI0. |
| 5 | CLKIN0b_GPI1 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1. |
| 6 | VDDR | Power | CLKIN (receiver) power supply. See Table 8 for supported voltages. |
| 7 | CLKIN1_GPI2 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI2. |
| 8 | CLKIN1b_GPI3 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI3. |
| 9 | SCL_SCLK | I | I2C Mode: I$^2$C interface bi-directional clock.<br>SPI Mode: Serial Clock<br>This pin is 3.3V tolerant. |
| 10 | SDA_nCS | I/O | I2C Mode: I$^2$C interface bi-directional data in open-drain mode.<br>SPI Mode: Chip Select (active low)<br>This pin is 3.3V tolerant. |

Table 4. RCxxx08BQ Pin Descriptions (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 11 | VDDD | Power | Digital core and GPIO power supply. See Table 8 for supported voltages. When programming the OTP, this supply must be 2.5V or 3.3V. |
| 12 | GPIO0 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 13 | GPIO1 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 14 | GPIO2 | I/O | General purpose input/output.<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 15 | GPIO3 | I/O | General purpose input/output. |
| 16 | GPIO4 | I/O | General purpose input/output. |
| 17 | NC | I | Not connected. |
| 18 | VDDO1 | Power | Power supply for output bank 1 and IOD 1. See Table 8 for supported voltages. |
| 19 | OUT1b | O | Output Clock 1 negative. |
| 20 | OUT1 | O | Output Clock 1 positive |
| 21 | VDDO2 | Power | Power supply for output bank 2 and FOD 0. See Table 8 for supported voltages. |
| 22 | OUT2b | O | Output Clock 2 negative. |
| 23 | OUT2 | O | Output Clock 2 positive. |
| 24 | OUT3b | O | Output Clock 3 negative. |
| 25 | OUT3 | O | Output Clock 3 positive. |
| 26 | OUT6b | O | Output Clock 6 negative. |
| 27 | OUT6 | O | Output Clock 6 positive. |
| 28 | OUT7b | O | Output Clock 7 negative. |
| 29 | OUT7 | O | Output Clock 7 positive. |
| 30 | VDDO3 | Power | Power supply for output bank 3 and FOD 1. See Table 8 for supported voltages. |
| 31 | OUT8b | O | Output Clock 8 negative. |
| 32 | OUT8 | O | Output Clock 8 positive. |
| 33 | VDDO4 | Power | Power supply for output bank 4 and FOD 2. See Table 8 for supported voltages. |
| 34 | VDDO5 | Power | Power supply for output bank 5 and IOD 2. See Table 8 for supported voltages. |
| 35 | OUT10b | O | Output Clock 10 negative. |
| 36 | OUT10 | O | Output Clock 10 positive. |
| 37 | OUT11b | O | Output Clock 11 negative. |
| 38 | OUT11 | O | Output Clock 11 positive. |
| 39 | VDDO6 | Power | Supply voltage for output bank 6 and IOD 3. See Table 8 for supported voltages. |
| 40 | VDDA | Power | Analog power supply. See Table 8 for supported voltages. |
| EPAD | GND | Power | Ground. ePad must be connected to ground before any VDD is applied. |

## 1.9 Pin Assignments – RCxxx05BQ (Top View)



## 1.10 Pin Descriptions – RCxxx05BQ

**Table 5. RCxxx05BQ Pin Descriptions**

| Number | Name | Type | Description |
|---|---|---|---|
| 1 | SDA_nCS | I/O | I2C Mode: I$^2$C interface bi-directional data in open-drain mode.<br>SPI Mode: Chip Select (active low)<br>This pin is 3.3V tolerant. |
| 2 | SCL_SCLK | I | I2C Mode: I$^2$C interface bi-directional clock.<br>SPI Mode: Serial Clock<br>This pin is 3.3V tolerant. |
| 3 | VDDR | Power | CLKIN (receiver) power supply. See Table 8 for supported voltages. |
| 4 | CLKIN0b_GPI1 | I | Differential clock negative input / CMOS single-ended reference clock input or general purpose input pin GPI1 |
| 5 | CLKIN0_GPI0 | I | Differential clock positive input / CMOS single-ended reference clock input or general purpose input pin GPI0 |
| 6 | VDDX | Power | Crystal oscillator power supply. See Table 8 for supported voltages. |
| 7 | DNC | NA | Do not connect. This pin should have no stubs. |
| 8 | DNC | NA | Do not connect. This pin should have no stubs. |
| 9 | VDDA | Power | Analog power supply. See Table 8 for supported voltages. |
| 10 | VDDO6 | Power | Supply voltage for output bank 6 and IOD 3. See Table 8 for supported voltages. |
| 11 | OUT10 | O | Output Clock 10 positive. |
| 12 | OUT10b | O | Output Clock 10 negative. |

Table 5. RCxxx05BQ Pin Descriptions  (Cont.)

| Number | Name | Type | Description |
|---|---|---|---|
| 13 | VDDO5 | Power | Power supply for output bank 5 and IOD 2. See Table 8 for supported voltages. |
| 14 | VDDO4 | Power | Power supply for output bank 4 and FOD 2. See Table 8 for supported voltages. |
| 15 | OUT8 | O | Output Clock 8 positive. |
| 16 | OUT8b | O | Output Clock 8 negative. |
| 17 | VDDO3 | Power | Power supply for output bank 3 and FOD 1. See Table 8 for supported voltages. |
| 18 | OUT6 | O | Output Clock 6 positive. |
| 19 | OUT6b | O | Output Clock 6 negative. |
| 20 | GND | Power | Ground |
| 21 | OUT3 | O | Output Clock 3 positive. |
| 22 | OUT3b | O | Output Clock 3 negative. |
| 23 | VDDO2 | Power | Power supply for output bank 2 and FOD 0. See Table 8 for supported voltages. |
| 24 | VDDO1 | Power | Power supply for output bank 1 and IOD 1. See Table 8 for supported voltages. |
| 25 | OUT1 | O | Output Clock 1 positive |
| 26 | OUT1b | O | Output Clock 1 negative. |
| 27 | GPIO4 | I/O | General purpose input/output |
| 28 | GPIO3 | I/O | General purpose input/output |
| 29 | GPIO2 | I/O | General purpose input/output<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 30 | GPIO1 | I/O | General purpose input/output<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 31 | GPIO0 | I/O | General purpose input/output<br>3-level logic input during power-up and CMOS level logic after unless set to 3-level. |
| 32 | VDDD | Power | Digital core and GPIO power supply. See Table 8 for supported voltages. When programming the OTP, this supply must be 2.5V or 3.3V. |
| EPAD | GND | Power | Ground. ePad must be connected to ground before any VDD is applied. |

## 1.11 Pin Characteristics

Table 6. Pin Characteristics

| Symbol | Parameter | Test Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | CLKIN[1:0], CLKIN[1:0]b, GPI[0:3] | - | 2 | - | pF |
| | | SCL_SCLK, SDA_nCS | - | 3 | - | |
| | | XIN_REFIN [1] | - | 5 | - | |
| | | XOUT_REFINb [1] | - | 4 | - | |
| | | GPIO[0:4] | - | 5 | - | |
| $R_{PULLUP}$ | Input Pull-Up Resistor | All pins with internal pull up capability | - | 52.6 | - | kΩ |
| $R_{PULLDOWN}$ | Input Pull-Down Resistor | All pins with internal pull down capability | - | 52.6 | - | |
| $Z_{OUTDC}$ | Single-ended LP-HCSL Output Impedance | 50Ω single-ended (100Ω differential). | - | 51 | - | 40 to 60Ω |
| | | 42.5Ω single-ended (85Ω differential). | - | 44 | - | 34 to 51Ω |
| | LVCMOS Output Impedance | VDDO = 3.3V | - | 17.3 | - | Ω |
| | | VDDO = 2.5V. | - | 19.5 | - | |
| | | VDDO = 1.8V | - | 17.6 | - | |

1. When used as clock input.

# 2. Specifications

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the RC310xxB at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

## 2.1 Absolute Maximum Ratings

**Table 7. Absolute Maximum Ratings**

| Symbol | Parameter | Conditions | Minimum | Maximum | Unit |
|---|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage with respect to Ground | Any VDD pin | -0.5 | 3.63 | V |
| $V_{IN}$ | Input Voltage [1] | XIN_REFIN, XOUT_REFINb [2] | -0.5 | $V_{DD}$ + 0.3 | V |
| | | CLKIN[1:0]_GPI[1:0],<br>CLKIN[1:0]b_GPI[3:2] | -0.5 | $V_{DD}$ + 0.3 | V |
| | | GPIO[4:0] used as inputs | -0.5 | $V_{DD}$ + 0.3 | V |
| | | SCL_SCLK, SDA_nCS | -0.5 | 3.63 | V |
| $I_{IN}$ | Input Current | CLKIN[1:0]_GPI[1:0],<br>CLKIN[1:0]b_GPI[3:2] | - | ±50 | mA |
| $I_{OUT}$ | Output Current - Continuous | OUT[11:0], OUT[11:0]b | - | 30 | mA |
| | | GPIO[4:0] used as outputs, SDA_nCS | - | 25 | mA |
| | Output Current - Surge | OUT[11:0], OUT[11:0]b | - | 60 | mA |
| | | GPIO[4:0] used as outputs, SDA_nCS | - | 50 | mA |
| $T_J$ | Maximum Junction Temperature | | - | 150 | °C |
| $T_S$ | Storage Temperature | Storage Temperature | -65 | 150 | °C |
| ESD | Human Body Model | JESD22-A114 (JS-001) Classification | - | 2000 | V |
| | Charged Device Model | JESD22-C101 Classification | - | 500 | V |

1. VDD refers to the VDD pin that supplies the particular input. To determine to which VDD pin the specification applies, see Table 46.
2. This limit only applies when XIN_REFIN/XOUT_REFINb are configured as an “Input Buffer” for use with an external oscillator. No limit is implied when connected directly to a crystal.

## 2.2 Recommended Operating Conditions

**Table 8. Recommended Operating Conditions [1][2]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $T_J$ | Maximum Junction Temperature | | - | - | 125 | °C |
| $T_A$ | Ambient Operating temperature | | -40 | - | 85 | °C |
| $V_{DDx}$ | Supply Voltage with respect to Ground | Any VDD pin, 1.8V supply | 1.71 | 1.8 | 1.89 | V |
| | | Any VDD pin, 2.5V supply | 2.375 | 2.5 | 2.625 | V |
| | | Any VDD pin, 3.3V supply | 3.135 | 3.3 | 3.465 | V |
| $t_{PU}$ | Power-up time for all VDDs to reach minimum specified voltage. | Power ramps must be monotonic. For more considerations, see Application Information. | 0.2 | - | 5 | ms |

1. All electrical characteristics are specified over Recommended Operating Conditions unless noted otherwise.
2. All conditions in this table must be met to guarantee device functionality and performance.

## 2.3 Electrical Characteristics

**Table 9. PCIe Refclk Jitter for VDDO = 1.8V [1][2]**

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1\text{-}CC}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(Common Clocked Architecture,<br>SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 4330 | 8622 | 86,000 | fs pk-pk |
| $t_{jphPCIeG2\text{-}CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 265 | 547 | 3000 | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 76 | 210 | 3100 | |
| $t_{jphPCIeG3\text{-}CC}$ | | PCIe Gen 3 (8 GT/s) | 126 | 246 | 1000 | |
| $t_{jphPCIeG4\text{-}CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 126 | 246 | 500 | |
| $t_{jphPCIeG5\text{-}CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 49 | 95 | 150 | |
| $t_{jphPCIe6\text{-}CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 29 | 59 | 100 | |
| $t_{jphPCIeG2\text{-}SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 1342 | 1474 | N/A [7] | fs RMS |
| $t_{jphPCIeG3\text{-}SRIS}$ | | PCIe Gen 3 (8 GT/s) | 313 | 355 | | |
| $t_{jphPCIeG4\text{-}SRIS}$ | | PCIe Gen 4 (16 GT/s) | 137 | 178 | | |
| $t_{jphPCIeG5\text{-}SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC =0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 104 | 146 | | |
| $t_{jphPCIeG6\text{-}SRIS}$ | | PCIe Gen 6 (64 GT/s) | 115 | 174 | | |
| $t_{jphPCIeG2\text{-}SRNS}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(SRNS Architecture,<br>SSC = 0%) | PCIe Gen 2 (5 GT/s) | 137 | 277 | N/A [7] | fs RMS |
| $t_{jphPCIeG3\text{-}SRNS}$ | | PCIe Gen 3 (8 GT/s) | 61 | 131 | | |
| $t_{jphPCIeG4\text{-}SRNS}$ | | PCIe Gen 4 (16 GT/s) | 61 | 131 | | |
| $t_{jphPCIeG5\text{-}SRNS}$ | | PCIe Gen 5 (32 GT/s) | 24 | 52 | | |
| $t_{jphPCIeG6\text{-}SRNS}$ | | PCIe Gen 6 (64 GT/s) | 15 | 31 | | |

**Table 9. PCIe Refclk Jitter for VDDO = 1.8V [1][2] (Cont.)**

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1-CC}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(CC Architecture,<br>SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 3242 | 10190 | N/A [7][8] | fs pk-pk |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 201 | 656 | | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 44 | 160 | | |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen 3 (8 GT/s) | 88 | 268 | | |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 88 | 268 | | |
| $t_{jphPCIeG5-CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 34 | 102 | | |
| $t_{jphPCIe6-CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 22 | 67 | | |
| $t_{jphPCIeG2-SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 252 | 833 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRIS}$ | | PCIe Gen 3 (8 GT/s) | 65 | 210 | | |
| $t_{jphPCIeG4-SRIS}$ | | PCIe Gen 4 (16 GT/s) | 67 | 217 | | |
| $t_{jphPCIeG5-SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC = 0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 58 | 192 | | |
| $t_{jphPCIeG6-SRIS}$ | | PCIe Gen 6 (64 GT/s) | 76 | 257 | | |
| $t_{jphPCIeG2-SRNS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(SRNS Architecture, SSC = 0%) | PCIe Gen 2 (5 GT/s) | 244 | 843 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRNS}$ | | PCIe Gen 3 (8 GT/s) | 63 | 212 | | |
| $t_{jphPCIeG4-SRNS}$ | | PCIe Gen 4 (16 GT/s) | 65 | 219 | | |
| $t_{jphPCIeG5-SRNS}$ | | PCIe Gen 5 (32 GT/s) | 57 | 194 | | |
| $t_{jphPCIeG6-SRNS}$ | | PCIe Gen 6 (64 GT/s) | 74 | 264 | | |

1. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

**Table 10. PCIe Refclk Jitter for VDDO = 2.5V [1][2]**

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1-CC}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 4054 | 5248 | 86,000 | fs pk-pk |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 241 | 322 | 3000 | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 67 | 142 | 3100 | |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen 3 (8 GT/s) | 118 | 150 | 1000 | |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 118 | 150 | 500 | |
| $t_{jphPCIeG5-CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 46 | 60 | 150 | |
| $t_{jphPCIe6-CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 28 | 35 | 100 | |
| $t_{jphPCIeG2-SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture, SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 1328 | 1366 | N/A [7] | fs RMS |
| $t_{jphPCIeG3-SRIS}$ | | PCIe Gen 3 (8 GT/s) | 309 | 323 | | |
| $t_{jphPCIeG4-SRIS}$ | | PCIe Gen 4 (16 GT/s) | 133 | 142 | | |
| $t_{jphPCIeG5-SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture, SSC = 0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 99 | 115 | | |
| $t_{jphPCIeG6-SRIS}$ | | PCIe Gen 6 (64 GT/s) | 106 | 132 | | |
| $t_{jphPCIeG2-SRNS}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(SRNS Architecture, SSC = 0%) | PCIe Gen 2 (5 GT/s) | 125 | 215 | N/A [7] | fs RMS |
| $t_{jphPCIeG3-SRNS}$ | | PCIe Gen 3 (8 GT/s) | 55 | 81 | | |
| $t_{jphPCIeG4-SRNS}$ | | PCIe Gen 4 (16 GT/s) | 55 | 81 | | |
| $t_{jphPCIeG5-SRNS}$ | | PCIe Gen 5 (32 GT/s) | 21 | 33 | | |
| $t_{jphPCIeG6-SRNS}$ | | PCIe Gen 6 (64 GT/s) | 13 | 19 | | |
| $t_{jphPCIeG1-CC}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(CC Architecture, SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 2032 | 5139 | N/A [7][8] | fs pk-pk |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 122 | 277 | | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 34 | 65 | | |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen 3 (8 GT/s) | 57 | 137 | | |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 55 | 137 | | |
| $t_{jphPCIeG5-CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 23 | 56 | | |
| $t_{jphPCIe6-CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 14 | 33 | | |
| $t_{jphPCIeG2-SRIS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(SRIS Architecture, SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 152 | 310 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRIS}$ | | PCIe Gen 3 (8 GT/s) | 40 | 84 | | |
| $t_{jphPCIeG4-SRIS}$ | | PCIe Gen 4 (16 GT/s) | 41 | 86 | | |
| $t_{jphPCIeG5-SRIS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(SRIS Architecture, SSC = 0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 36 | 94 | | |
| $t_{jphPCIeG6-SRIS}$ | | PCIe Gen 6 (64 GT/s) | 46 | 108 | | |
| $t_{jphPCIeG2-SRNS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode<br>(SRNS Architecture, SSC = 0%) | PCIe Gen 2 (5 GT/s) | 164 | 348 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRNS}$ | | PCIe Gen 3 (8 GT/s) | 43 | 94 | | |
| $t_{jphPCIeG4-SRNS}$ | | PCIe Gen 4 (16 GT/s) | 45 | 97 | | |
| $t_{jphPCIeG5-SRNS}$ | | PCIe Gen 5 (32 GT/s) | 39 | 102 | | |
| $t_{jphPCIeG6-SRNS}$ | | PCIe Gen 6 (64 GT/s) | 49 | 116 | | |

1. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the Test Loads section of the data sheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.

2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20 GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately - Jitter measurements may be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200 MHz (at 300 MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5 GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2 MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7 ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25 ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15 ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

**Table 11. PCIe Refclk Jitter for VDDO = 3.3V [1][2]**

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1\text{-}CC}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(Common Clocked Architecture, SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 4042 | 5554 | 86,000 | fs pk-pk |
| $t_{jphPCIeG2\text{-}CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 241 | 332 | 3000 | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 65 | 146 | 3100 | |
| $t_{jphPCIeG3\text{-}CC}$ | | PCIe Gen 3 (8 GT/s) | 118 | 164 | 1000 | |
| $t_{jphPCIeG4\text{-}CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 118 | 164 | 500 | |
| $t_{jphPCIeG5\text{-}CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 46 | 65 | 150 | |
| $t_{jphPCIe6\text{-}CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 27 | 37 | 100 | |
| $t_{jphPCIeG2\text{-}SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 1329 | 1392 | N/A [7] | fs RMS |
| $t_{jphPCIeG3\text{-}SRIS}$ | | PCIe Gen 3 (8 GT/s) | 309 | 328 | | |
| $t_{jphPCIeG4\text{-}SRIS}$ | | PCIe Gen 4 (16 GT/s) | 133 | 145 | | |
| $t_{jphPCIeG5\text{-}SRIS}$ | PCIe Refclk Jitter Clock Generator Mode<br>(SRIS Architecture,<br>SSC = 0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 99 | 114 | | |
| $t_{jphPCIeG6\text{-}SRIS}$ | | PCIe Gen 6 (64 GT/s) | 106 | 132 | | |
| $t_{jphPCIeG2\text{-}SRNS}$ | PCIe Refclk Jitter in Clock Generator Mode<br>(SRNS Architecture, SSC = 0%) | PCIe Gen 2 (5 GT/s) | 125 | 208 | N/A [7] | fs RMS |
| $t_{jphPCIeG3\text{-}SRNS}$ | | PCIe Gen 3 (8 GT/s) | 56 | 81 | | |
| $t_{jphPCIeG4\text{-}SRNS}$ | | PCIe Gen 4 (16 GT/s) | 56 | 81 | | |
| $t_{jphPCIeG5\text{-}SRNS}$ | | PCIe Gen 5 (32 GT/s) | 22 | 32 | | |
| $t_{jphPCIeG6\text{-}SRNS}$ | | PCIe Gen 6 (64 GT/s) | 13 | 19 | | |

### Table 11. PCIe Refclk Jitter for VDDO = 3.3V [1][2] (Cont.)

| Symbol | Parameter | Conditions | Typical | Maximum | PCIe Limit | Unit |
|---|---|---|---|---|---|---|
| $t_{jphPCIeG1-CC}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode (CC Architecture, SSC = 0%, -0.3%, -0.5%) | PCIe Gen 1 (2.5 GT/s) | 2256 | 4829 | N/A [7][8] | fs pk-pk |
| $t_{jphPCIeG2-CC}$ | | PCIe Gen 2 Hi Band (5 GT/s) | 132 | 241 | | fs RMS |
| | | PCIe Gen 2 Lo Band (5 GT/s) | 35 | 51 | | |
| $t_{jphPCIeG3-CC}$ | | PCIe Gen 3 (8 GT/s) | 63 | 122 | | |
| $t_{jphPCIeG4-CC}$ | | PCIe Gen 4 (16 GT/s) [3][4] | 63 | 122 | | |
| $t_{jphPCIeG5-CC}$ | | PCIe Gen 5 (32 GT/s) [3][5] | 25 | 50 | | |
| $t_{jphPCIe6-CC}$ | | PCIe Gen 6 (64 GT/s) [3][6] | 15 | 29 | | |
| $t_{jphPCIeG2-SRIS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = 0.0% or -0.5%) | PCIe Gen 2 (5 GT/s) | 139 | 301 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRIS}$ | | PCIe Gen 3 (8 GT/s) | 36 | 80 | | |
| $t_{jphPCIeG4-SRIS}$ | | PCIe Gen 4 (16 GT/s) | 38 | 83 | | |
| $t_{jphPCIeG5-SRIS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRIS Architecture, SSC = 0.0% or -0.3%) | PCIe Gen 5 (32 GT/s) | 31 | 81 | | |
| $t_{jphPCIeG6-SRIS}$ | | PCIe Gen 6 (64 GT/s) | 40 | 97 | | |
| $t_{jphPCIeG2-SRNS}$ | Additive PCIe Refclk Jitter in Fan-out Buffer Mode (SRNS Architecture, SSC = 0%) | PCIe Gen 2 (5 GT/s) | 148 | 286 | N/A [7][8] | fs RMS |
| $t_{jphPCIeG3-SRNS}$ | | PCIe Gen 3 (8 GT/s) | 39 | 77 | | |
| $t_{jphPCIeG4-SRNS}$ | | PCIe Gen 4 (16 GT/s) | 40 | 79 | | |
| $t_{jphPCIeG5-SRNS}$ | | PCIe Gen 5 (32 GT/s) | 34 | 83 | | |
| $t_{jphPCIeG6-SRNS}$ | | PCIe Gen 6 (64 GT/s) | 44 | 95 | | |

1. The Refclk jitter is measured after applying the filter functions found in *PCI Express Base Specification 6.0, Revision 0.9*. See the “Test Loads” section of the datasheet for the exact measurement setup. The worst case results for each data rate are summarized in this table. Equipment noise is removed from all measurements.
2. Jitter measurements should be made with a capture of at least 100,000 clock cycles captured by a real-time oscilloscope (RTO) with a sample rate of 20GS/s or greater. Broadband oscilloscope noise must be minimized in the measurement. The measured PP jitter is used (no extrapolation) for RTO measurements. Alternately, jitter measurements can be used with a Phase Noise Analyzer (PNA) extending (flat) and integrating and folding the frequency content up to an offset from the carrier frequency of at least 200MHz (at 300MHz absolute frequency) below the Nyquist frequency. For PNA measurements for the 2.5GT/s data rate, the RMS jitter is converted to peak-to-peak jitter using a multiplication factor of 8.83.
3. SSC spurs from the fundamental and harmonics are removed up to a cutoff frequency of 2MHz taking care to minimize removal of any non-SSC content.
4. Note that 0.7ps RMS is to be used in channel simulations to account for additional noise in a real system.
5. Note that 0.25ps RMS is to be used in channel simulations to account for additional noise in a real system.
6. Note that 0.15ps RMS is to be used in channel simulations to account for additional noise in a real system.
7. The *PCI Express Base Specification 6.0, Revision 0.9* provides the filters necessary to calculate SRIS and SRNS jitter values; it does not provide specification limits, hence the N/A in the Limit column. SRIS and SRNS values are informative only. A common practice is to split the common clock budget in half. For 16GT/s data rates and above, the user must choose whether to use the output jitter specification, or the input jitter specification, which includes an allocation for the jitter added by the channel. Using 32GT/s, the Refclk jitter budget is 150fs RMS. One half of the Refclk jitter budget is 106fs RMS. At the clock input, the system must deliver 250fs RMS. One half of this value is 177fs RMS. If the clock is placed next to the PCIe device in an SRIS system, the channel is very short and the user may choose to use this more relaxed value as the jitter limit.
8. The RMS sum of the source jitter and the additive jitter must be less than the jitter specification listed for the clock generator operating mode.

**Table 12. Phase Jitter and Phase Noise – 1.8V VDDO [1][2]**

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, Synthesizer Mode) [2] | 122.88MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 194 | 266 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 213 | 271 | |
| | | 245.76MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 186 | 249 | |
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, JA Mode) [2] | 122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 211 | 274 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 208 | 258 | |
| | | 245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 201 | 259 | |
| | | 312.5MHz (VCO: 10GHz, FOD 0, 1 or 2) | 202 | 298 | |
| | | 322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 195 | 221 | |
| | | 644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 187 | 209 | |
| ΦSSB(100) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one output enabled at 156.25MHz) | 100Hz Offset | -104 | - | dBc/Hz |
| ΦSSB(1k) | | 1kHz Offset | -114 | - | |
| ΦSSB(10k) | | 10kHz Offset | -129 | - | |
| ΦSSB(100k) | | 100kHz Offset | -134 | - | |
| ΦSSB(1M) | | 1MHz Offset | -145 | - | |
| ΦSSB(10M) | | 10MHz Offset | -155 | - | |
| ΦSSB(30M) | | 30MHz Offset | -158 | - | |
| ΦSSB(10) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one IOD enabled at 245.76MHz) | 10Hz Offset | -80 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -97 | - | |
| ΦSSB(500) | | 500Hz Offset | -106 | - | |
| ΦSSB(1k) | | 1kHz Offset | -108 | - | |
| ΦSSB(10k) | | 10kHz Offset | -123 | - | |
| ΦSSB(100k) | | 100kHz Offset | -133 | - | |
| ΦSSB(200k) | | 200kHz Offset | -134 | - | |
| ΦSSB(800k) | | 800kHz Offset | -142 | - | |
| ΦSSB(5M) | | 5MHz Offset | -153 | - | |
| ΦSSB(>10M) | | > 10MHz Offset | -157 | - | |
| ΦSSB(10) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth,25MHz input from SMA-100, one IOD enabled at 122.88MHz) | 10Hz Offset | -86 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -103 | - | |
| ΦSSB(1k) | | 1kHz Offset | -113 | - | |
| ΦSSB(10k) | | 10kHz Offset | -129 | - | |
| ΦSSB(100k) | | 100kHz Offset | -139 | - | |
| ΦSSB(>1M) | | >1MHz Offset | -163 | - | |
| Φ | Spurious Signal Rejection<br>(245.76MHz) | 2Hz to < 100Hz | 66 | - | dB |
| | | 100Hz to < 1kHz | 77 | - | |
| | | 1kHz to < 491.52MHz | 70 | - | |
| | Spurious Signal Rejection<br>(122.88MHz) | 2Hz to < 100Hz | 80 | - | dB |
| | | 100Hz to < 1kHz | 84 | - | |
| | | 1kHz to < 245.76MHz | 70 | - | |

### Table 12. Phase Jitter and Phase Noise – 1.8V VDDO [1][2] (Cont.)

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| - | Harmonic Rejection<br>(Even order harmonics) | 245.76MHz | 13 | - | dBc |
| | | 122.88MHz | 12 | - | |
| - | Output-to-output Isolation: Measured in One Specific Configuration Between 2 Outputs | OUTx = 312.5MHz | 51 | - | dB |
| - | | OUTx = 491.52MHz | 54 | - | dB |
| - | | OUTx = 491.52MHz, with 7.68MHz actively running | 75 | - | dB |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

### Table 13. Phase Jitter and Phase Noise – 2.5V VDDO [1][2]

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, Synthesizer Mode) [2] | 122.88MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 214 | 229 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 231 | 253 | |
| | | 245.76MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 209 | 222 | |
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, JA Mode) [2] | 122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 232 | 272 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 231 | 252 | |
| | | 245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 220 | 253 | |
| | | 312.5MHz (VCO: 10GHz, FOD 0, 1 or 2) | 220 | 234 | |
| | | 322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 223 | 252 | |
| | | 644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 214 | 240 | |
| ΦSSB(100) | Single-Sideband Phase Noise (68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one output enabled at 156.25MHz) | 100Hz Offset | -101 | - | dBc/Hz |
| ΦSSB(1k) | | 1kHz Offset | -115 | - | |
| ΦSSB(10k) | | 10kHz Offset | -128 | - | |
| ΦSSB(100k) | | 100kHz Offset | -137 | - | |
| ΦSSB(1M) | | 1MHz Offset | -146 | - | |
| ΦSSB(10M) | | 10MHz Offset | -155 | - | |
| ΦSSB(30M) | | 30MHz Offset | -157 | - | |
| ΦSSB(10) | Single-Sideband Phase Noise (68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one IOD enabled at 245.76MHz) | 10Hz Offset | -80 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -97 | - | |
| ΦSSB(500) | | 500Hz Offset | -108 | - | |
| ΦSSB(1k) | | 1kHz Offset | -111 | - | |
| ΦSSB(10k) | | 10kHz Offset | -125 | - | |
| ΦSSB(100k) | | 100kHz Offset | -133 | - | |
| ΦSSB(200k) | | 200kHz Offset | -133 | - | |
| ΦSSB(800k) | | 800kHz Offset | -140 | - | |
| ΦSSB(5M) | | 5MHz Offset | -153 | - | |
| ΦSSB(>10M) | | >10MHz Offset | -156 | - | |

Table 13. Phase Jitter and Phase Noise – 2.5V VDDO [1][2] (Cont.)

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| ΦSSB(10) | Single-Sideband Phase Noise (68MHz Crystal, JA Mode with 10Hz loop bandwidth,25MHz input from SMA-100, one IOD enabled at 122.88MHz) | 10Hz Offset | -87 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -104 | - | |
| ΦSSB(1k) | | 1kHz Offset | -117 | - | |
| ΦSSB(10k) | | 10kHz Offset | -131 | - | |
| ΦSSB(100k) | | 100kHz Offset | -139 | - | |
| ΦSSB(>1M) | | >1MHz Offset | -163 | - | |
| Φ | Spurious Signal Rejection<br>(245.76MHz) | 2Hz to <100Hz | 65 | - | dB |
| | | 100Hz to <1kHz | 86 | - | |
| | | 1kHz to < 491.52MHz | 70 | - | |
| | Spurious Signal Rejection<br>(122.88MHz) | 2Hz to < 100Hz | 78 | - | dB |
| | | 100Hz to < 1kHz | 89 | - | |
| | | 1kHz to < 245.76MHz | 76 | - | |
| - | Harmonic Rejection<br>(Even order harmonics) | 245.76MHz | 13 | - | dBc |
| | | 122.88MHz | 12 | - | |
| - | Output-to-output Isolation:<br>Measured in One Specific Configuration Between 2 Outputs Only | OUTx = 312.5MHz | 51 | - | dB |
| - | | OUTx = 491.52MHz | 54 | - | dB |
| - | | OUTx = 491.52MHz, with 7.68MHz actively running | 74 | - | dB |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

Table 14. Phase Jitter and Phase Noise – 3.3V VDDO [1][2]

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, Synthesizer Mode) [2] | 122.88MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 211 | 225 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 231 | 245 | |
| | | 245.76MHz (VCO: 9.8304GHz, IOD 0, 1, 2 or 3) | 211 | 240 | |
| tjit(Φ) | Random Phase Jitter, 10kHz to 20MHz (68MHz XTAL, JA Mode) [2] | 122.88MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 233 | 263 | fs (RMS) |
| | | 156.25MHz (VCO: 10GHz, FOD 0, 1 or 2) | 227 | 249 | |
| | | 245.76MHz (VCO: 9.8304GHz, FOD 0, 1 or 2) | 220 | 240 | |
| | | 312.5MHz (VCO: 10GHz, FOD 0, 1 or 2) | 217 | 235 | |
| | | 322.265625MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 220 | 249 | |
| | | 644.53125MHz (VCO: 10.3125GHz, FOD 0, 1 or 2) | 212 | 236 | |

**Table 14. Phase Jitter and Phase Noise – 3.3V VDDO [1][2] (Cont.)**

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| ΦSSB(100) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one output enabled at 156.25MHz) | 100Hz Offset | -102 | - | dBc/Hz |
| ΦSSB(1k) | | 1kHz Offset | -113 | - | |
| ΦSSB(10k) | | 10kHz Offset | -128 | - | |
| ΦSSB(100k) | | 100kHz Offset | -137 | - | |
| ΦSSB(1M) | | 1MHz Offset | -147 | - | |
| ΦSSB(10M) | | 10MHz Offset | -155 | - | |
| ΦSSB(30M) | | 30MHz Offset | -157 | - | |
| ΦSSB(10) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth, 25MHz input from SMA-100, one IOD enabled at 245.76MHz) | 10Hz Offset | -85 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -96 | - | |
| ΦSSB(500) | | 500Hz Offset | -107 | - | |
| ΦSSB(1k) | | 1kHz Offset | -110 | - | |
| ΦSSB(10k) | | 10kHz Offset | -124 | - | |
| ΦSSB(100k) | | 100kHz Offset | -133 | - | |
| ΦSSB(200k) | | 200kHz Offset | -134 | - | |
| ΦSSB(800k) | | 800kHz Offset | -143 | - | |
| ΦSSB(5M) | | 5MHz Offset | -153 | - | |
| ΦSSB(>10M) | | >10MHz Offset | -157 | - | |
| ΦSSB(10) | Single-Sideband Phase Noise<br>(68MHz Crystal, JA Mode with 10Hz loop bandwidth,25MHz input from SMA-100, one IOD enabled at 122.88MHz) | 10Hz Offset | -88 | - | dBc/Hz |
| ΦSSB(100) | | 100Hz Offset | -104 | - | |
| ΦSSB(1k) | | 1kHz Offset | -116 | - | |
| ΦSSB(10k) | | 10kHz Offset | -130 | - | |
| ΦSSB(100k) | | 100kHz Offset | -139 | - | |
| ΦSSB(>1M) | | >1MHz Offset | -163 | - | |
| Φ | Spurious Signal Rejection<br>(245.76MHz) | 2Hz to < 100Hz | 65 | - | dB |
| | | 100Hz to < 1kHz | 83 | - | |
| | | 1kHz to < 491.52MHz | 70 | - | |
| | Spurious Signal Rejection<br>(122.88MHz) | 2Hz to < 100Hz | 71 | - | dB |
| | | 100Hz to < 1kHz | 85 | - | |
| | | 1kHz to < 245.76MHz | 76 | - | |
| - | Harmonic Rejection<br>(Even order harmonics) | 245.76MHz | 13 | - | dBc |
| | | 122.88MHz | 12 | - | |
| - | Output-to-output Isolation:<br>Measured in One Specific Configuration Between 2 Outputs Only | OUTx = 312.5MHz | 51 | - | dB |
| - | | OUTx = 491.52MHz | 54 | - | dB |
| - | | OUTx = 491.52MHz, with 7.68MHz actively running | 74 | - | dB |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Characterized using a Rohde and Schwarz SMA100 overdriving the XTAL interface.

### Table 15. Jitter Attenuator and Network Synchronization [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_c$ | Loop Bandwidth (-3dB cut-off frequency) | SETS Mode | 0.1 | - | 10 | Hz |
| | | JA Mode | 15 | - | 12,000 | |
| $K_p$ | Gain Peaking | Wander tolerance according to [ITU-T G.8262], clause 9.1 ([ITU-T G.8262.1], clause 9.2) at input [2] | - | 0.171 | 0.2 | dB |
| $t_{HS}$ | Output Phase Change using Hitless Switching [3] | < 1MHz input | 50 | 150 | 500 | ps |
| | | ≥ 1MHz input | 20 | 80 | 250 | ps |
| $\Delta f_{HO}$ | Initial Frequency Offset entering Holdover | Using holdover filter of 1mHz with settling time of 1hr. | - | 0.00148 | 1 | ppb |
| $\Delta t_{HO}$ | Initial Phase Shift entering Holdover | Using short-term monitor (LOS) for disqualification | - | 0 | 250 | ps |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. For eEEC only devices - Wander tolerance according to [ITU-T G.8262.1], clause 9.1 at input.
3. This parameter will vary with the quality of the TDC and system DPLL references. The typical value shown assumes an ideal reference is used as input to the TDC and system DPLL.

### Table 16. Clock Input Frequencies [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_{INAPLL}$ | APLL Input Frequency for clock generation. | Over-driving Crystal Input, Doubler Logic Disabled | 1 | - | 650 | MHz |
| | | Over-driving Crystal Input, Doubler Logic Enabled | 1 | - | 250 | |
| | | CLKIN[1:0] Differential Mode | 1 | - | 650 | |
| | | CLKIN[1:0] Single-ended Mode | 1 | - | 250 | |
| $f_{INJA}$ | JA Input Frequency | CLKIN[1:0] Differential Mode | 1 | - | 650 | MHz |
| | | CLKIN[1:0] Single-ended Mode | 0.008 | - | 250 | |

1. For crystal characteristics, see Table 17.

### Table 17. External Crystal Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| - | Resonance Mode | - | Fundamental | | | - |
| $f_{INXTAL}$ [1] | Crystal input frequency | Fundamental mode | 8 | - | 80 | MHz |
| ESR [1] | Equivalent Series Resistance | 8MHz ≤ $f_{INXTAL}$ ≤ 12MHz, $C_L$ = 12pF | - | - | 120 | Ω |
| | | 12MHz < $f_{INXTAL}$ ≤ 28MHz, $C_L$ = 12pF | - | - | 80 | |
| | | 28MHz < $f_{INXTAL}$ ≤ 54MHz, $C_L$ = 12pF | - | - | 50 | |
| | | 54MHz < $f_{INXTAL}$ ≤ 80MHz, $C_L$ = 8pF | - | - | 50 | |
| $C_O$ [1] | Shunt Capacitance | | - | 7 | - | pF |
| $C_L$ [1] | Load Capacitance | | 6 | 8 | 12 | |
| Drive [1] | Drive Level | | - | - | 100 | µW |

Table 17. External Crystal Characteristics (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $F_{TOL}$ | Frequency Tolerance | Center frequency at 25°C | - | - | [2] | ppm |
| $F_{STAB}$ | Frequency Stability | Over Operating Temperature Range with respect to $F_{TOL}$ | - | - | | |
| Aging | Per Year | | - | - | | |

1. These parameters are required, regardless of crystal used.
2. These parameters are customer/application dependent. Common maximum values are $F_{TOL}$ = ±20ppm, $F_{STAB}$ = ±20ppm, and Aging = ±5ppm/10years. The customer is free to adjust these parameters to their particular requirements.

Table 18. Internal Crystal Characteristics (Q Versions Only)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| - | Resonance Mode | | Fundamental | | | - |
| $f_{INXTAL}$ | Crystal frequency | Fundamental mode | - | 68 | - | MHz |
| $F_{STAB}$ | Frequency Stability | Includes both initial accuracy and variation over temperature. | - | - | ±30 | ppm |
| - | Aging | Over the first ten years | - | - | ±5 | |

Table 19. Output Frequencies and Startup Times [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_{OUT}$ | Output Frequency | Differential Output. | 0.001 | - | 650 | MHz |
| | | LVCMOS Output. | 0.001 | - | 200 | |
| $f_{MON}$ | Reference Monitor Operating Frequency | | - | - | 40 | MHz |
| $f_{VCO}$ | VCO (APLL) Operating Frequency | | 9.5 | - | 10.7 | GHz |
| $\Delta f_{OUT}$ | DPLL frequency tuning resolution in DCO mode | DPLL Frequency Write | 0.91 | | | ppt |
| $\Delta f_{OUT}$ | Output frequency tuning resolution in NCO mode | Fractional Output Divider | 58.21 | | | ppt |
| $f_{PFD}$ | Analog Phase / Frequency Detector (PFD) Operating Frequency | - | - | - | 108 | MHz |
| $f_{TDC}$ | Digital Phase Detector Operating Frequency | - | - | - | 33 | |
| $t_{STARTUP}$ | Start-up Time [2][3] | Synthesizer mode | - | 6 | 10 | ms |
| $t_{STARTUP}$ | Start-up Time [2][3] | DPLL mode, with a loop bandwidth setting of 300Hz | - | 263 | 400 | ms |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Measured from when all power supplies have reached > 90% of nominal voltage to the first stable clock edge on the output. A stable clock is defined as one generated from a locked PLL (as appropriate for the configuration listed) with no further perturbations in frequency expected. Includes time needed to load a configuration from internal OTP. For important additional power supply sequencing considerations, see Power Considerations.
3. Start-up time will depend on the actual configuration used. For more information, please contact Renesas technical support.

Table 20. Output-to-Output, Input-to-Output Skew – LP-HCSL Outputs 1.8V/2.5V/3.3V VDDO [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{SK}$ | Output-to-Output Skew [2][3] | FOD1 driving output banks [2:4] | - | 18 | 90 | ps |
| | | FOD1 driving all output banks | - | 39 | 124 | |
| | | FOD1 driving Bank2 | - | 21 | 63 | |
| | | IOD1 driving bank 2 | - | 22 | 65 | |
| $t_{PD}$ | Input-to-Output Delay [3][4] | Fanout buffer path to any output | 1.2 | 2 | 2.6 | ns |
| $\Delta t_{PD}$ | Input-to-Output Delay Variation [3][4] | Fanout buffer, single device, at a fixed voltage, over temperature | - | 2 | 4 | ps/°C |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65
4. Defined as the time between to output rising edge and the input rising edge that caused it.

Table 21. Output-to-Output, Input-to-Output Skew – LVDS Outputs 1.8V/2.5V/3.3V VDDO [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{SK}$ | Output-to-Output Skew [2][3] | FOD1 driving output banks [2:4] | - | 16 | 93 | ps |
| | | FOD1 driving all output banks | - | 44 | 101 | |
| | | FOD1 driving Bank2 | - | 14 | 53 | |
| | | IOD1 driving bank 2 | - | 20 | 67 | |
| $t_{PD}$ | Input-to-Output Delay [3][4] | Fanout buffer path to any output | 1.3 | 2 | 2.8 | ns |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65
4. Defined as the time between to output rising edge and the input rising edge that caused it.

Table 22. Output-to-Output, Input-to-Output Skew – LVCMOS Outputs 1.8V/2.5V/3.3V VDDO [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{SK}$ | Output-to-Output Skew [2][3] | FOD1 driving output banks [2:4] | - | 50 | 130 | ps |
| | | FOD1 driving all output banks | - | 76 | 180 | |
| | | FOD1 driving Bank2 | - | 22 | 64 | |
| | | IOD1 driving bank 2 | - | 29 | 79 | |
| $t_{PD}$ | Input-to-Output Delay [3][4] | Fanout buffer path to any output - 1.8V VDDO | 2.3 | 3.2 | 4.3 | ns |
| | | Fanout buffer path to any output - 2.5V VDDO | 1.7 | 2.4 | 3.4 | |
| | | Fanout buffer path to any output - 3.3V VDDO | 1.6 | 2.2 | 3 | |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. Defined as the time between the rising edges of two outputs of the same frequency, configuration, loading, and supply voltage.
3. This parameter is defined in accordance with JEDEC Standard 65
4. Defined as the time between to output rising edge and the input rising edge that caused it.

### Table 23. Static Phase Offset - Zero Delay Buffer Mode

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $t_{\Phi APLL}$ | APLL Static Phase Offset [1] | LVDS or LP-HCSL signaling, feedback frequency = 50MHz. VDDR = VDDOx = 2.5V or 3.3V. CLKIN0 used as feedback in. | - | 197 | 270 | ps |
| | | LVDS or LP-HCSL signaling, feedback frequency = 50MHz. VDDR = VDDOx = 1.8V. CLKIN0 used as feedback in. | - | 192 | 350 | |
| $t_{\Phi DPLL}$ | DPLL Static Phase Offset [1] | LVDS or LP-HCSL signaling, feedback frequency = 50MHz. VDDR = VDDOx = 2.5V or 3.3V. CLKIN1 used as feedback in. | - | 27 | 110 | ps |
| | | LVDS or LP-HCSL signaling, feedback frequency = 50MHz. VDDR = VDDOx = 1.8V. CLKIN1 used as feedback in. | - | 57 | 230 | |

1. This parameter is defined in accordance with JEDEC Standard 65B, which defines static phase offset as the time interval between similar points on the waveforms of the averaged input reference clock and the averaged feedback input signal when the PLL is locked and the input reference frequency is stable.

### Table 24. LVCMOS AC/DC Output Characteristics – 1.8V VDDO[1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $I_{OH}$ = -2mA | 1.6 | 1.75 | VDDO + 0.3 | V |
| $V_{OL}$ | Output Low Voltage [2] | $I_{OL}$ = 2mA | - | 0.04 | 0.4 | |
| $I_{OZ}$ | Output Leakage Current | Outputs Tri-stated | -5 | - | 5 | µA |
| dV/dt | Slew Rate[3] | ODRV_CNFG[3:2] = 0 | 0.8 | 1.5 | 2.2 | V/ns |
| | | ODRV_CNFG[3:2] = 1 | 0.7 | 1.5 | 2.2 | |
| | | ODRV_CNFG[3:2] = 2 | 0.7 | 1.5 | 2.4 | |
| | | ODRV_CNFG[3:2] = 3 | 0.8 | 1.5 | 2.3 | |
| tDC | Output Duty Cycle | $V_T$ = VDDO/2 | 45 | 51 | 55 | % |

1. See Test Loads for additional information.
2. These values are compliant with JESD8-7A.
3. $V_T$ = 20% to 80% of VDDO, $C_L$ = 4.7pF.

### Table 25. LVCMOS AC/DC Output Characteristics – 2.5V VDDO[1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $I_{OH}$ = -2mA | 2.2 | 2.4 | VDDO + 0.3 | V |
| $V_{OL}$ | Output Low Voltage [2] | $I_{OL}$ = 2mA | - | 0.04 | 0.4 | |
| $I_{OZ}$ | Output Leakage Current | Outputs Tri-stated | -5 | - | 5 | µA |
| dV/dt | Slew Rate[3] | ODRV_CNFG[3:2] = 0 | 1.2 | 2.2 | 3.6 | V/ns |
| | | ODRV_CNFG[3:2] = 1 | 0,6 | 1.6 | 3.2 | |
| | | ODRV_CNFG[3:2] = 2 | 0,5 | 1.4 | 2.6 | |
| | | ODRV_CNFG[3:2] = 3 | 0.9 | 2.0 | 3.4 | |
| tDC | Output Duty Cycle | $V_T$ = VDDO/2 | 45 | 51 | 55 | % |

1. See Test Loads for additional information.
2. These values are compliant with JESD8-5A.01.
3. $V_T$ = 20% to 80% of VDDO, $C_L$ = 4.7pF.

### Table 26. LVCMOS AC/DC Output Characteristics – 3.3V VDDO[1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2] | $I_{OH}$ = -2mA | 2.4 | 3.2 | VDDO + 0.3 | V |
| $V_{OL}$ | Output Low Voltage [2] | $I_{OL}$ = 2mA | - | 0.03 | 0.4 | |
| $I_{OZ}$ | Output Leakage Current | Outputs Tri-stated | -5 | - | 5 | µA |
| dV/dt | Slew Rate[3] | ODRV_CNFG[3:2] = 0 | 1.3 | 3.1 | 4.9 | V/ns |
| | | ODRV_CNFG[3:2] = 1 | 1.2 | 2.5 | 4.0 | |
| | | ODRV_CNFG[3:2] = 2 | 1.2 | 2.4 | 4.0 | |
| | | ODRV_CNFG[3:2] = 3 | 1.4 | 2.8 | 4.1 | |
| tDC | Output Duty Cycle | $V_T$ = VDDO/2 | 45 | 50.7 | 55 | % |

1. See Test Loads for additional information.
2. These values are compliant with JESD8C.01.
3. $V_T$ = 20% to 80% of VDDO, $C_L$ = 4.7pF.

### Table 27. LVDS AC/DC Output Characteristics – 1.8V $V_{DDO}$ [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x00 | 243 | 346 | 448 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -462 | -355 | -248 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x01 | 257 | 362 | 468 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -482 | -372 | -262 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x02 | 219 | 310 | 400 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -419 | -323 | -227 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x03 | 232 | 328 | 425 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -441 | -338 | -235 | |
| $\Delta V_{OT}$ | Change in $V_{OT}$ between Complimentary Output States | | 14 | 37 | 60 | mV |

### Table 27. LVDS AC/DC Output Characteristics – 1.8V $V_{DDO}$ [1] (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{CMR}$ | Output Common Mode Voltage | | 1.07 | 1.21 | 1.35 | V |
| $\Delta V_{CMR}$ | Change in $V_{CMR}$ between Complimentary Output States | | - | 25 | 37 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT+}$ or $V_{OUT-}$ = 0V or VDD | - | 7.5 | - | mA |
| $I_{OSD}$ | Differential Output Short Circuit Current | $V_{OUT+} = V_{OUT-}$ | - | 3.3 | - | |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing. | | 138 | 252 | 365 | ps |
| $t_{DC}$ | Output Duty Cycle [3] | f ≤ 400MHz, $V_T$ = 0V. | 45 | 49.7 | 55 | % |
| | | f > 400MHz., $V_T$ = 0V. | 43.9 | 49.7 | 56.1 | % |

1. See Test Loads for additional test conditions.
2. Single-ended measurement
3. Measured from differential waveform.

### Table 28. LVDS AC/DC Output Characteristics – 2.5V/3.3V $V_{DDO}$ [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x00 | 240 | 348 | 457 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -464 | -356 | -247 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x01 | 255 | 366 | 477 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -483 | -372 | -261 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x02 | 211 | 311 | 411 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -427 | -325 | -224 | |
| $V_{OT}$ (+) | TRUE binary state. | out_prog = 0x03 | 225 | 330 | 434 | mV |
| $V_{OT}$ (-) | FALSE binary state. | | -446 | -341 | -235 | |
| $\Delta V_{OT}$ | Change in $V_{OT}$ between Complimentary Output States | | 14 | 37 | 60 | mV |
| $V_{CMR}$ | Output Common Mode Voltage | | 1.16 | 1.21 | 1.32 | V |
| $\Delta V_{CMR}$ | Change in $V_{CMR}$ between Complimentary Output States | | - | 25 | 37 | mV |
| $I_{OS}$ | Output Short Circuit Current | $V_{OUT+}$ or $V_{OUT-}$ = 0V or VDD | - | 7.5 | - | mA |
| $I_{OSD}$ | Differential Output Short Circuit Current | $V_{OUT+} = V_{OUT-}$ | - | 3.3 | - | |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing. | | 138 | 252 | 365 | ps |
| $t_{DC}$ | Output Duty Cycle [3] | f ≤ 400MHz, $V_T$ = 0V. | 45 | 49.7 | 55 | % |
| | | f > 400MHz, $V_T$ = 0V. | 43.9 | 49.7 | 56.1 | % |

1. See Test Loads for additional test conditions.
2. Single-ended measurement
3. Measured from differential waveform.

**Table 29. LP-HCSL AC/DC Characteristics, Non-PCIe Frequencies – 1.8V $V_{DDO}$ [1]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2]<br>f < 400MHz | $V_{HIGH}$ = 800mV,<br>Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz. | 680 | 849 | 1018 | mV |
|  | Output High Voltage [2]<br>f ≥ 400MHz |  | 522 | 657 | 792 |  |
| $V_{OL}$ | Output Low Voltage [2] |  | -130 | -4 | 123 |  |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] |  | 166 | 423 | 680 |  |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] |  | - | 30 | 43 |  |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f < 400MHz |  | 232 | 392 | 552 | ps |
|  | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f ≥ 400MHz |  | 160 | 300 | 439 |  |
| $V_{OH}$ | Output High Voltage [2]<br>f < 400MHz | $V_{HIGH}$ = 900mV,<br>Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz. | 718 | 924 | 1130 | mV |
|  | Output High Voltage [2]<br>f ≥ 400MHz |  | 551 | 703 | 855 |  |
| $V_{OL}$ | Output Low Voltage [2] |  | -164 | -2 | 160 |  |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] |  | 170 | 446 | 722 |  |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] |  | - | 27 | 41 |  |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f < 400MHz |  | 217 | 402 | 588 | ps |
|  | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f ≥ 400MHz |  | 169 | 298 | 428 |  |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings, f < 400MHz<br>$V_T$ = 0V. | 47 | 50 | 53 | % |
|  |  | Across all settings, f ≥ 400MHz<br>$V_T$ = 0V. | 45 | 50 | 55 |  |

1. Standard high impedance load with $C_L$= 2pF. See Test Loads
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum variance in $V_{CROSS}$ for any particular system.
6. Measured from differential waveform.

**Table 30. LP-HCSL AC/DC Characteristics, Non-PCIe Frequencies – 2.5V/3.3V $V_{DDO}$ [1]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{OH}$ | Output High Voltage [2]<br>f < 400MHz. | $V_{HIGH}$ = 800mV,<br>Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz. | 667 | 861 | 1055 | mV |
| | Output High Voltage [2]<br>f ≥ 400MHz. | | 552 | 717 | 881 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -164 | -4 | 156 | mV |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 261 | 384 | 507 | mV |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 27 | 42 | mV |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f < 400MHz. | | 214 | 393 | 606 | ps |
| | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing<br>f ≥ 400MHz | | 148 | 302 | 456 | |
| $V_{OH}$ | Output High Voltage [2]<br>f < 400MHz. | $V_{HIGH}$ = 900mV,<br>Fast Slew Rate, 25MHz, 100MHz, 156.25MHz, 312.5MHz or 625MHz. | 694 | 917 | 1140 | mV |
| | Output High Voltage [2]<br>f ≥ 400MHz. | | 598 | 757 | 917 | mV |
| $V_{OL}$ | Output Low Voltage [2] | | -164 | -8 | 148 | mV |
| $V_{CROSS}$ | Crossing Voltage (abs) [3] | | 238 | 455 | 673 | mV |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][4][5] | | - | 27 | 42 | mV |
| $t_R/t_F$ | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing,<br>f < 400MHz. | | 218 | 397 | 581 | ps |
| | Rise/Fall Time [2]<br>$V_T$ = 20% to 80% of swing<br>f ≥ 400MHz | | 174 | 300 | 426 | |
| $t_{DC}$ | Output Duty Cycle [6] | Across all settings, f < 400MHz<br>$V_T$ = 0V. | 48 | 50 | 52 | % |
| | | Across all settings, f ≥ 400MHz<br>$V_T$ = 0V. | 45 | 50 | 55 | |

1. Standard high impedance load with $C_L$= 2pF. See Test Loads.
2. Measured from single-ended waveform.
3. Measured at crossing point where the instantaneous voltage value of the rising edge of CLK equals the falling edge of CLKb.
4. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
5. Defined as the total variation of all crossing voltages of Rising CLK and Falling CLKb. This is the maximum allowed variance in $V_{CROSS}$ for any particular system.
6. Measured from differential waveform.

Table 31. LP-HCSL AC/DC Characteristics, 100MHz PCIe – 1.8V $V_{DDO}$ [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Spec. Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage<br>Includes 300mV of overshoot (Vovs) [3][4] | $V_{HIGH}$ set to 900mV. | - | - | 1103 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage<br>Includes -300mV of undershoot (Vuds) [3][5] | | -152 | - | - | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 825 | 886 | 984 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -70 | -15 | 44 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 266 | 406 | 545 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | - | 27 | 49 | 140 | |
| dv/dt | Slew rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 1.6 | 2.6 | 3.6 | 1 to 4 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1.2 | 1.8 | 2.4 | | |
| $\Delta T_{R/F}$ | Rise/fall matching [3][11] | $V_{HIGH}$ set to 800mV. Fast or slow slew rate. | - | 7 | 19.3 | 20 | % |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 844 | 940 | 1037 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -79 | -14 | 51 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 301 | 451 | 600 | 300 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | - | 28 | 44 | 140 | |
| dv/dt | Slew rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 1.7 | 2.7 | 3.7 | 1 to 4 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.3 | 1.9 | 2.5 | | |
| $\Delta T_{R/F}$ | Rise/fall matching [3][11] | $V_{HIGH}$ set to 900mV. Fast or slow slew rate. | - | 4 | 18.5 | 20 | % |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V. | 49 | 50 | 51 | 45 to 55 | |
| $t_{jcyc\text{-}cyc}$ | Jitter, Cycle to cycle [9] | Across all settings in this table at 100MHz. | - | 33 | 49.3 | 50 | ps |

1. Standard high impedance load with $C_L$= 2pF. See Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.
4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in $V_{CROSS}$ for any particular system.

9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 32. LP-HCSL AC/DC Characteristics, 100MHz PCIe – 2.5V/3.3V $V_{DDO}$ [1]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Spec. Limit [2] | Unit |
|---|---|---|---|---|---|---|---|
| $V_{MAX}$ | Absolute Max Voltage<br>Includes 300mV of overshoot (Vovs) [3][4] | $V_{HIGH}$ set to 900mV. | - | - | 1088 | 1150 | mV |
| $V_{MIN}$ | Absolute Min Voltage<br>Includes -300mV of undershoot (Vuds) [3][5] | | -174 | - | - | -300 | |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 800mV. | 743 | 869 | 994 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -92 | -7 | 58 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 800mV, scope averaging off. | 256 | 406 | 533 | 250 to 550 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | - | 27 | 40 | 140 | |
| dv/dt | Slew rate [9][10] | $V_{HIGH}$ set to 800mV, Fast slew rate, scope averaging on. | 1.3 | 2.6 | 3.9 | 1 to 4 | V/ns |
| | | $V_{HIGH}$ set to 800mV, Slow slew rate, scope averaging on. | 1 | 1.7 | 3.1 | | |
| $\Delta T_{R/F}$ | Rise/fall matching [3][11] | $V_{HIGH}$ set to 800mV. Fast or slow slew rate. | - | 8 | 19.7 | 20 | % |
| $V_{HIGH}$ | Voltage High [3] | $V_{HIGH}$ set to 900mV. | 800 | 925 | 1051 | - | mV |
| $V_{LOW}$ | Voltage Low [3] | | -95 | -2 | 68 | - | |
| $V_{CROSS}$ | Crossing Voltage (abs) [3][6][7] | $V_{HIGH}$ set to 900mV, scope averaging off. | 286 | 454 | 629 | 250 to 600 | |
| $\Delta V_{CROSS}$ | Crossing Voltage (var) [3][6][8] | | - | 27 | 40 | 140 | |
| dv/dt | Slew rate [9][10] | $V_{HIGH}$ set to 900mV, Fast slew rate, scope averaging on. | 1.4 | 2.8 | 4.2 | 1 to 4.2 | V/ns |
| | | $V_{HIGH}$ set to 900mV, Slow slew rate, scope averaging on. | 1.2 | 2.0 | 3 | | |
| $\Delta T_{R/F}$ | Rise/fall matching [3][11] | $V_{HIGH}$ set to 900mV. Fast or slow slew rate. | - | 6 | 18.7 | 20 | % |
| $t_{DC}$ | Output Duty Cycle [9] | $V_T$ = 0V. | 49 | 50 | 51 | 45 to 55 | |
| $t_{jcyc-cyc}$ | Jitter, Cycle to cycle [9] | Across all settings in this table at 100MHz. | - | 30 | 48.3 | 50 | ps |

1. Standard high impedance load with $C_L$= 2pF. See Test Loads.
2. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
3. Measured from single-ended waveform.

4. Defined as the maximum instantaneous voltage including overshoot.
5. Defined as the minimum instantaneous voltage including undershoot.
6. Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-.
7. Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
8. Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in $V_{CROSS}$ for any particular system.
9. Measured from differential waveform.
10. Measured from -150 mV to +150 mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300 mV measurement window is centered on the differential zero crossing.
11. Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75 mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate.

**Table 33. 100MHz PCIe Output Clock Accuracy and SSC**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | PCIe Limit[1] | Unit |
|---|---|---|---|---|---|---|---|
| $T_{PERIOD\_AVG\_32G\_64G\_CC}$ | Average Clock Period Accuracy for devices supporting 32GT/s or 64GT/s CC mode at any speed. [2][3] | SSC ≤ -0.5%, includes spread-spectrum modulation, if any. | 0 | - | 2410 | -100 to +2600 | ppm |
| $T_{PERIOD\_AVG\_32G\_64G\_SRIS}$ | Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][3] | SSC ≤ -0.3%, includes spread-spectrum modulation, if any. | 0 | - | 1430 | -100 to +1600 | |
| $T_{PERIOD\_AVG\_32G\_64G}$ | Average Clock Period Accuracy for devices supporting 32GT/s CC/SRNS mode at any speed. [2][3] | SSC = 0% (SSC Off). | 0 | - | 0 | ±100 | |
| $T_{PERIOD\_ABS\_32G\_64G\_CC}$ | Average Clock Period Accuracy for devices supporting 32GT/s CC mode at any speed. [2][4] | SSC ≤ -0.5%, includes jitter and spread-spectrum modulation. | 10 | - | 10.024 | 9.849 to 10.201 | ns |
| $T_{PERIOD\_ABS\_32G\_64G\_SRIS}$ | Average Clock Period Accuracy for devices supporting 32GT/s SRIS mode at any speed. [2][4] | SSC ≤ -0.3%, includes jitter and spread-spectrum modulation. | 10 | - | 10.014 | 9.849 to 10.181 | |
| $T_{PERIOD\_ABS\_32G\_64G}$ | Average Clock Period Accuracy for devices supporting 32GT/ s CC/SRNS mode at any speed. [2][4] | SSC = 0% (SSC Off), includes jitter. | 10 | - | 10 | 9.849 to 10.151 | |
| $F_{REFCLK\_32G\_64G}$ | Refclk Frequency for devices that support 32GT/s or 64GT/s. | SSC = 0% (SSC Off) | 100 | - | 100 | 99.99 to 100.01 | MHz |
| $F_{SSC}$ | SSC Modulation Frequency | | 31.2 | 31.5 | 31.9 | 30 to 33 | kHz |
| $T_{SSC\_FREQ\_DEV}$ | SSC Deviation for all devices and architectures except 32GT/s or 64GT/s devices operating in SRIS mode. | SSC = -0.5% | -0.490 | -0.488 | -0.486 | -0.5 | % |

Table 33. 100MHz PCIe Output Clock Accuracy and SSC (Cont.)

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | PCIe Limit[1] | Unit |
|---|---|---|---|---|---|---|---|
| $T_{SSC\_FREQ\_DEV\_32G\_64G\_SRIS}$ | SSC Deviation for devices that support 32 or 64GT/s operating in SRIS mode, at any speeds. | SSC = -0.3% | -0.300 | -0.295 | -0.290 | -0.3 | % |
| $T_{SSC\_MAX\_FREQ\_SLEW}$ | Max df/dt of the SSC. [5] | | - | 310 | 372 | 1250 | ppm/us |
| $T_{TRANSPORT\_DELAY}$ | Tx-Rx transport delay used for PCIe Jitter calculations. [6] | Applies to Common Clocked architectures only. | - | - | 12 | 12 | ns |

1. The specification limits are taken from either the *PCIe Base Specification Revision 6.0* or from relevant x86 processor specifications, whichever is more stringent.
2. Measured from differential waveform.
3. PPM refers to parts per million and is a DC absolute period accuracy specification. 1 PPM is 1/1,000,000th of 100.000000MHz exactly or 100Hz. For 100PPM, then we have an error budget of 100Hz/PPM * 100PPM = 10kHz. The period is to be measured with a frequency counter with measurement window set to 100 ms or greater. The ±100PPM applies to systems that do not employ Spread-Spectrum Clocking, or that use common clock source. For systems employing Spread-Spectrum Clocking, there is an additional 2,500PPM nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2,600PPM for Common Clock Architectures. SRIS Architectures may have a lower allowed spread percentage. Devices meeting these specifications automatically meet the less stringent -300ppm to +2800ppm tolerances for data rates ≤16GT/s. Refer to Section 8.6 of the *PCI Express Base Specification, Revision 6.0*.
4. Defined as the absolute minimum or maximum instantaneous period. This includes cycle-to-cycle jitter, relative PPM tolerance, and spread-spectrum modulation. Devices meeting these specifications automatically meet the less stringent and 9.847ns to 10.203ns tolerances for data rates ≤16GT/s.
5. Measurement is made over a 0.5us time interval with a 1st order LPF with an fC of 60x the SSC modulation frequency (1.89MHz for 31.5kHz modulation frequency).
6. This is the default value used for all PCIe Common Clock architecture jitter calculations. There are form factors (for example topologies including long cables) that may exceed this limit. Contact Renesas for assistance calculating jitter if your topology exceeds 12ns.

Table 34. Spread-Spectrum Programmability

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_{SSCMOD}$ | SSC Modulation Frequency | Modulation frequency. | 30 | - | 63 | kHz |
| SSC% | Spread percentage [1] | Down Spread. | -1 | - | -0.05 | % |
| | | Center Spread. | ±0.025 | - | ±0.75 | |
| $f_{OUTSSC}$ | Output frequency | Allowable output frequency range when SSC is enabled. | 33 | - | 650 | MHz |

1. Spread off is 0%.

### Table 35. CLKIN Differential Electrical Characteristics [1]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{PP\_DIF}$ | Peak-to-Peak differential input voltage [2] | VDDR = 1.8V, 2.5V or 3.3V | 0.3 | - | 2.2 | V |
| $V_{CMR\_LOW}$ | Common mode voltage range - low range setting [3] | VDDR = 1.8V | 0.15 | - | 0.6 | V |
| | | VDDR = 2.5V or 3.3V | 0.15 | - | $<V_{DDR}/2$ | |
| $V_{CMR\_HIGH}$ | Common mode voltage range - high range setting [3] | VDDR = 1.8V | 0.75 | - | $V_{DDR}$-0.3 | V |
| | | VDDR = 2.5V or 3.3V | $\geq V_{DDR}/2$ | - | $V_{DDR}$-0.3 | |
| $t_{SLEW}$ | CLKIN differential slew rate | 20/80% threshold | 0.5 | - | - | V/ns |

1. This table applies when CLKIN0 or CLKIN1 are used as differential input clocks. If used as single-ended input clocks, the values in the GPO/GPIO Electrical Characteristics tables apply. The DC input voltage limits specified in the GPI/GPIO Electrical Characteristics tables must be followed at all times. This means that an input clock with VPP_DIF = 0.3V will have a wider range of allowable common mode voltages than an input clock with a higher VPP_DIF.
2. This value is 2 x the single-ended amplitude of the CLKIN signal.
3. The correct setting is automatically selected by the RICBox design software.

### Table 36. GPI/GPIO Electrical Characteristics – 1.8V VDDD, VDDR, or VDDX [1][2]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | 0.65 VDD | - | VDD + 0.3 | V |
| $V_{IL}$ | Input Low Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | -0.3 | - | 0.35 VDD | |
| $V_{OH}$ | Output High Voltage [3] | GPIO[4:0], IOH = -2mA. | VDD - 0.45 | - | VDD + 0.3 | |
| $V_{OL}$ | Output Low Voltage [3] | GPIO[4:0], IOL = 2mA. | - | - | 0.45 | |
| $V_{IH}$ | Input High Voltage | GPIO[2:0], when set to tri-level. | 0.75 VDD | - | VDD + 0.3 | |
| $V_{IM}$ | Input Mid Voltage | GPIO[2:0], when set to tri-level. | 0.45 VDD | - | 0.55 VDD | |
| $V_{IL}$ | Input Low Voltage | GPIO[2:0], when set to tri-level. | -0.3 | - | 0.25 VDD | |

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 36, see GPI and GPIO VDD pin assignments in Pin Information. For SCL_SCLK, SDA_SDI, see the I2C/SMBus electrical characteristics Table 41 and Table 42.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-7A. These values only apply to XIN_REFIN and XOUT_REFINB when “Input Buffer” mode is selected. See the Applications section for more details.

### Table 37. GPI/GPIO Electrical Characteristics – 2.5V VDDD, VDDR, or VDDX [1][2]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | 1.7 | - | VDD + 0.3 | V |
| $V_{IL}$ | Input Low Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | -0.3 | - | 0.7 | |
| $V_{OH}$ | Output High Voltage [3] | GPIO[4:0], IOH = -2mA. | 1.7 | - | VDD + 0.3 | |
| $V_{OL}$ | Output Low Voltage [3] | GPIO[4:0], IOL = 2mA. | - | - | 0.7 | |
| $V_{IH}$ | Input High Voltage | GPIO[2:0], when set to tri-level. | 0.75 VDD | - | VDD + 0.3 | |
| $V_{IM}$ | Input Mid Voltage | GPIO[2:0], when set to tri-level. | 0.45 VDD | - | 0.55 VDD | |
| $V_{IL}$ | Input Low Voltage | GPIO[2:0], when set to tri-level. | -0.3 | - | 0.25 VDD | |

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 37, see GPI and GPIO VDD pin assignments in Pin Information. For SCL_SCLK, SDA_SDI, see the I2C/SMBus electrical characteristics Table 41 and Table 42.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-5A.01. These values only apply to XIN_REFIN and XOUT_REFINB when "Input Buffer" mode is selected. See the Applications section for more details.

### Table 38. GPI/GPIO Electrical Characteristics – 3.3V VDDD, VDDR, or VDDX [1][2]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input High Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | 2.2 | - | VDD + 0.3 | V |
| $V_{IL}$ | Input Low Voltage [3] | XIN_REFIN, XOUT_REFINB, GPI[3:0], GPIO[4:0]. | -0.3 | - | 0.8 | |
| $V_{OH}$ | Output High Voltage [3] | GPIO[4:0], IOH = -2mA. | 2.4 | - | VDD + 0.3 | |
| $V_{OL}$ | Output Low Voltage [3] | GPIO[4:0], IOL = 2mA. | - | - | 0.4 | |
| $V_{IH}$ | Input High Voltage | GPIO[2:0], when set to tri-level. | 0.75 VDD | - | VDD + 0.3 | |
| $V_{IM}$ | Input Mid Voltage | GPIO[2:0], when set to tri-level. | 0.45 VDD | - | 0.55 VDD | |
| $V_{IL}$ | Input Low Voltage | GPIO[2:0], when set to tri-level. | -0.3 | - | 0.25 VDD | |

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. To determine which VDD pin is referenced for each group in Table 38, see GPI and GPIO VDD pin assignments in Pin Information. For SCL_SCLK, SDA_SDI, see the I2C/SMBus electrical characteristics Table 41 and Table 42.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.
3. These values are compliant with JESD8-5A.01. These values only apply to XIN_REFIN and XOUT_REFINB when "Input Buffer" mode is selected. See the Applications section for more details.

### Table 39. CMOS GPI/GPIO Common Electrical Characteristics [1][2]

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $I_{IL}$ | Input Leakage Current | Includes input pull up/pull down resistor current. $V_{IL}$ = 0V, $V_{IH}$ = $V_{DD.}$ | -15 | - | 15 | µA |

1. Input specifications refer to signals XIN_REFIN, XOUT_REFINb, GPI[3:0], GPIO[4:0], when acting as inputs. Output specifications refer to signals GPIO[4:0], when acting as outputs. For VDD pin mapping, see GPI and GPIO VDD pin assignments in Pin Information.
2. CLKIN[1:0]/CLKIN[1:0]b used as two single-ended clocks rather than as a differential clock.

**Table 40. Power Supply Current [1]**

| Symbol | Parameter | Conditions | Typical | Maximum | Unit |
|---|---|---|---|---|---|
| $I_{DDR}$ | $V_{DDR}$ Supply Current | CMOS inputs (per input) [2][3] | 11 | 20 | mA |
| | | HCSL inputs (per input pair) [3] | 12 | 15 | |
| | | LVDS inputs (per input pair) [2][3] | 13 | 14 | |
| | | LVPECL inputs (per input pair) [3][4]<br>$V_{DDR}$ = 2.5V or 3.3V, | 13 | 15 | |
| | | CML inputs (per input pair) [3][4]<br>$V_{DDR}$ = 2.5V or 3.3V, input termination disabled. | 14 | 16 | |
| | | CML inputs (per input pair) [3][4]<br>$V_{DDR}$ = 2.5V or 3.3V, input termination enabled. | 33 | 54 | |
| $I_{DDRBIAS}$ | Bias Supply Current | Internal DC-bias circuit when enabled for AC-coupled external clock (per input pair) [3] | 13 | 24 | mA |
| $I_{DDX}$ | $V_{DDX}$ Supply Current | Crystal oscillator supply | 3.5 | 5 | mA |
| $I_{DDA}$ | $V_{DDA}$ Supply Current | $V_{DDA}$ = any valid supply. | 142 | 151 | mA |
| $I_{DDD}$ | $V_{DDD}$ Supply Current | $V_{DDD}$ = any valid supply. | 69 | 73 | mA |
| $I_{DDO\_CMOS}$ | $V_{DDO}$ Supply Current per output pair, CMOS mode (both OUT[x] and OUT[x]b enabled). [5][6] | $V_{DDO}$ = 1.8V ±5%. | 13 | 20 | mA |
| | | $V_{DDO}$ = 2.5V ±5%. | 18 | 24 | |
| | | $V_{DDO}$ = 3.3V ±5%. | 25 | 33 | |
| | $V_{DDO}$ Supply Current per output pair, CMOS mode (OUT[x] or OUT[x]b enabled, other output Hi-Z). [5][6] | $V_{DDO}$ = 1.8V ±5%. | 8 | 16 | mA |
| | | $V_{DDO}$ = 2.5 ±5%. | 11 | 17 | |
| | | $V_{DDO}$ = 3.3 ±5%. | 15 | 23 | |
| $I_{DDO\_LPHCSL}$ | $V_{DDO}$ Supply Current per output pair [5][6] | LP-HCSL outputs, 85ohm impedance, fast slew rate, 650MHz. $V_{DDO}$ = any valid supply. | 12 | 19 | mA |
| | | LP-HCSL outputs, 85ohm impedance, fast slew rate, 100MHz for PCIe. $V_{DDO}$ = any valid supply. | 13 | 17 | |
| $I_{DDO\_LVDS}$ | $V_{DDO}$ Supply Current per output pair, LVDS mode [3][4] | $V_{DDO}$ = any valid supply. | 8 | 17 | mA |
| $I_{DD\_IOD}$ | $V_{DDO}$ Divider Supply Current | Portion of VDDO used by IOD | 25 | 28 | mA |
| $I_{DD\_FOD}$ | $V_{DDO}$ Divider Supply Current | Portion of VDDO used by FOD | 38 | 51 | mA |
| $I_{DD\_PD}$ | Total Power Down Current | Power Down Mode Enabled, VDDs = 1.8V | 13 | 16 | mA |
| | | Power Down Mode Enabled, VDDs = 2.5V | 15 | 23 | |
| | | Power Down Mode Enabled, VDDs = 3.3V | 19 | 38 | |

1. Current consumption figures represent a worst-case consumption with all functions associated with the particular voltage supply enabled and all outputs running at maximum speed, unless otherwise noted. This information is provided to allow for design of appropriate power supply circuits that will support all possible register-based configurations for the device. To determine actual consumption for the user's device configuration, see Power Considerations. Outputs are not terminated. Values apply to all voltage levels unless noted.
2. Voltage of the input signal must be appropriate for the $V_{DDR}$ voltage supply level when using a DC-coupled connection. For example, when supplying an LVDS input signal that is referenced to a 2.5V supply at its source, the $V_{DDR}$ supply must also be 2.5V nominal voltage. When using a 3.3V CMOS input signal, $V_{DDR}$ must be 3.3V

3. There are two possible input clock pairs. If both are used, the current for each type must be added together. If the external clock(s) is/are AC-coupled, the internal DC-bias must be enabled and also added to the total $I_{DDR}$ current.
4. LVPECL and CML input clocks are not supported when $V_{DDR}$ = 1.8V.
5. $I_{DDO\_x}$ denotes the current consumed by each output driver and does not include output divider current. These values are measured at maximum output frequency, unless otherwise stated (200MHz for LVCMOS outputs and 650MHz for differential outputs).
6. Please refer to the Output Driver and Output Divider $V_{DDO}$ Pin Assignments Table to determine the allocation of $I_{DDO\_IOD}$, $I_{DDO\_FOD}$ and $I_{DDO\_x}$ to each $V_{DDO}$ pin.

**Table 41. I²C/SMBus Bus DC Electrical Characteristics [1]**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage for SCL_SCLK and SDA_nCS | - | 0.7 $V_{DDD}$ | - | - | V |
| $V_{IL}$ | Low-level input voltage for SCL_SCLK and SDA_nCS | - | - | - | 0.3 $V_{DDD}$ | V |
| $V_{HYS}$ | Hysteresis of Schmitt trigger inputs | - | 0.05 $V_{DDD}$ | - | - | V |
| $V_{OL}$ | Low-level output voltage for SCL_SCLK and SDA_nCS | $I_{OL}$ = 4mA | - | - | 0.4 | V |
| $I_{IN}$ | Input leakage current per pin | - | -10 | - | 10 | µA |
| $C_B$ | Capacitive Load for Each Bus Line | - | - | - | 400 | pF |

1. $V_{OH}$ is governed by the $V_{PUP}$, the voltage rail to which the pull up resistors are connected.

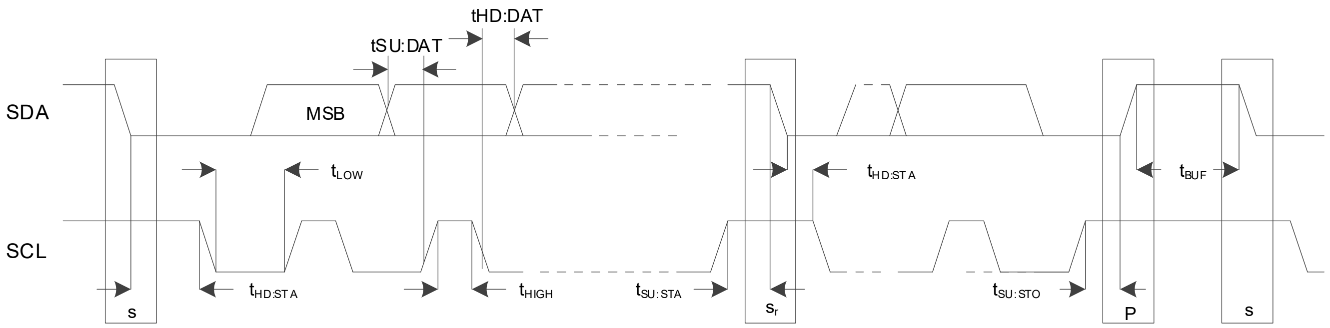


**Figure 3. I²C/SMBus Slave Timing Diagram**

**Table 42. I²C/SMBus Bus AC Electrical Characteristics**

| Symbol | Parameter | Conditions | 100kHz Class Minimum | 100kHz Class Maximum | 400kHz Class Minimum | 400kHz Class Maximum | Unit |
|---|---|---|---|---|---|---|---|
| fSMB | SMBus Operating Frequency [1] | | 10 | 100 | 10 | 400 | kHz |
| tBUF | Bus free time between STOP and START Condition | | 4.7 | - | 1.3 | - | µs |
| tHD:STA | Hold time after (REPEATED) START Condition [2] | | 4 | - | 0.6 | - | |
| tSU:STA | REPEATED START Condition setup time | | 4.7 | - | 0.6 | - | |
| tSU:STO | STOP Condition setup time | | 4 | - | 0.6 | - | |
| tHD:DAT | Data hold time [3] | | 300 | - | 300 | - | ns |
| tSU:DAT | Data setup time | | 250 | - | 100 | - | |

Table 42. I²C/SMBus Bus AC Electrical Characteristics (Cont.)

| Symbol | Parameter | Conditions | 100kHz Class Minimum | 100kHz Class Maximum | 400kHz Class Minimum | 400kHz Class Maximum | Unit |
|---|---|---|---|---|---|---|---|
| $t_{TIMEOUT}$ | Detect SCL_SCLK low timeout [4] | | 25 | 35 | 25 | 35 | ms |
| $t_{TIMEOUT}$ | Detect SDA_nCS low timeout [5] | | 25 | 35 | 25 | 35 | |
| $t_{LOW}$ | Clock low period | | 4.7 | - | 1.3 | - | µs |
| $t_{HIGH}$ | Clock high period [6] | | 4 | 50 | 0.6 | 50 | |
| $t_{LOW:SEXT}$ | Cumulative clock low extend time (slave device) [7] | | N/A, the RC310xxB do not extend the clock low. | | | | ms |
| $t_{LOW:MEXT}$ | Cumulative clock low extend time (master device) [8] | | N/A, the RC310xxB are not bus masters. | | | | |
| $t_F$ | Clock/Data Fall Time [9] | | - | 120 | - | 120 | ns |
| $t_R$ | Clock/Data Rise Time [9] | | - | 120 | - | 120 | |
| $t_{SPIKE}$ | Noise spike suppression time [10] | | - | N/A | - | 50 | |

1. A master should not drive the clock at a frequency below the minimum $f_{SMB}$. Further, the operating clock frequency should not be reduced below the minimum value of $f_{SMB}$ due to periodic clock extending by slave devices as defined in Section 5.3.3 of the *SMBus 2.0 Specification*. This limit does not apply to the bus idle condition, and this limit is independent from the $t_{LOW:SEXT}$ and $t_{LOW:MEXT}$ limits. For example, if the SMBCLK is high for $t_{HIGH:MAX}$, the clock must not be periodically stretched longer than $1/f_{SMB:MIN} – t_{HIGH:MAX}$. This requirement does not pertain to a device that extends the SMBCLK low for data processing of a received byte, data buffering and so forth for longer than 100µs in a non-periodic way.
2. A device must internally provide sufficient hold time for the SMBDAT signal (with respect to the $V_{IH:MIN}$ of the SMBCLK signal) to bridge the undefined region of the falling edge of SMBCLK.
3. Slave devices may have caused other slave devices to hold SDA low. The maximum time that a device can hold SMBDAT low after the master raises SMBCLK after the last bit of a transaction. A slave device may detect how long SDA is held low and release SDA after the time out period.
4. Devices participating in a transfer can abort the transfer in progress and release the bus when any single clock low interval exceeds the value of $t_{TIMEOUT:MIN}$. After the master in a transaction detects this condition, it must generate a stop condition within or after the current data byte in the transfer process. Devices that have detected this condition must reset their communication and be able to receive a new START condition no later than $t_{TIMEOUT:MAX}$. Typical device examples include the host controller, and embedded controller, and most devices that can master the SMBus. Some simple devices do not contain a clock low drive circuit; this simple kind of device typically may reset its communications port after a start or a stop condition. A timeout condition can only be ensured if the device that is forcing the timeout holds the SMBCLK low for $t_{TIMEOUT:MAX}$ or longer.
5. The device has the option of detecting a timeout if the SDA_nCS pin is also low for this time.
6. $t_{HIGH:MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH:MAX}$.
7. $t_{HIGH:MAX}$ provides a simple guaranteed method for masters to detect bus idle conditions. A master can assume that the bus is free if it detects that the clock and data signals have been high for greater than $t_{HIGH:MAX}$.
8. $t_{LOW:SEXT}$ is the cumulative time a given slave device is allowed to extend the clock cycles in one message from the initial START to the STOP. It is possible that another slave device or the master will also extend the clock causing the combined clock low extend time to be greater than $t_{LOW:SEXT}$. Therefore, this parameter is measured with the slave device as the sole target of a full-speed master.
9. The rise and fall time measurement limits are defined as follows:

   Rise Time Limits: ($V_{IL:MAX}$ - 0.15V) to ($V_{IH:MIN}$ + 0.15V)

   Fall Time Limits: ($V_{IH:MIN}$ + 0.15V) to ($V_{IL:MAX}$ - 0.15V)
10. Devices must provide a means to reject noise spikes of a duration up to the maximum specified value.

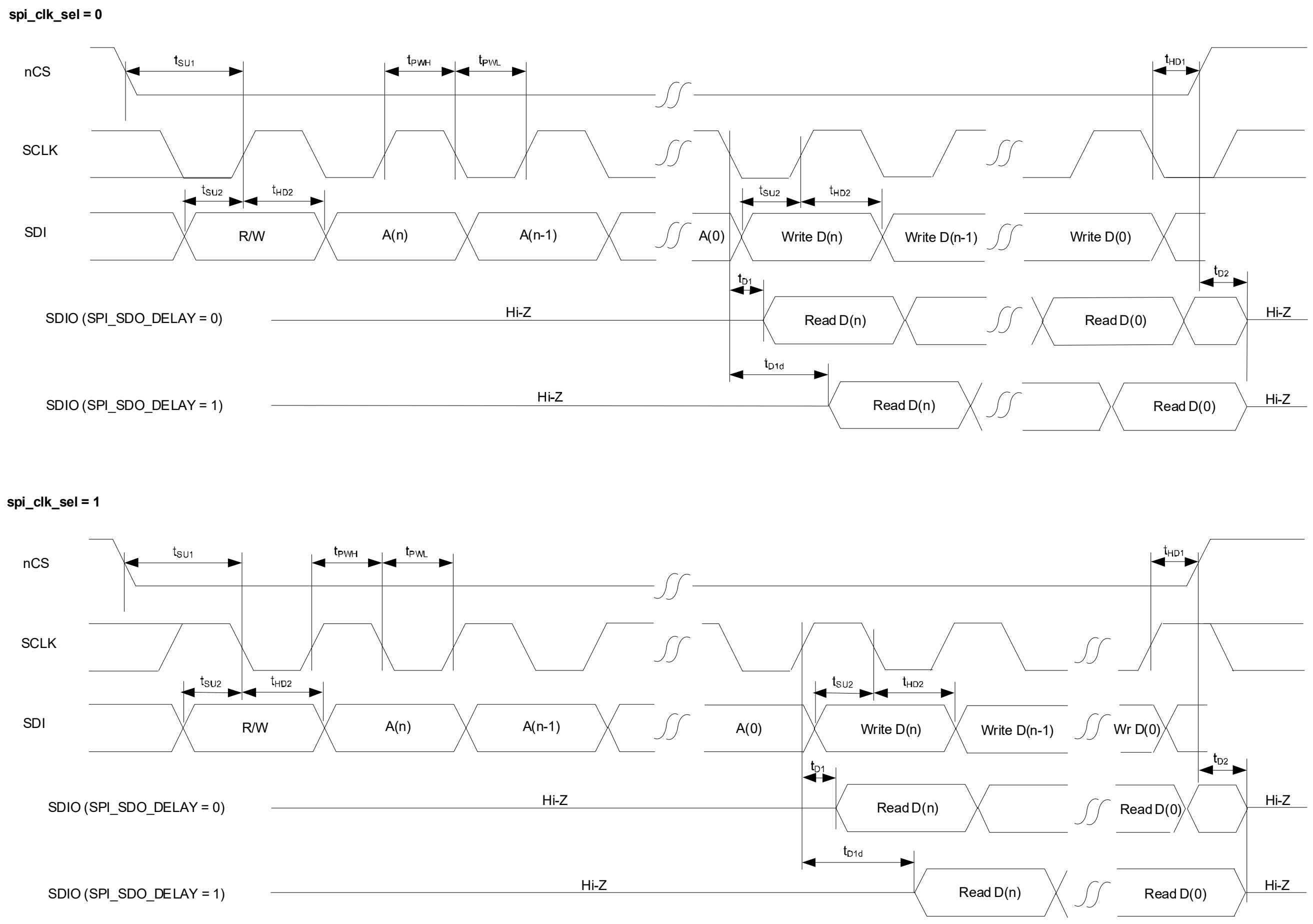


Figure 4. SPI Bus Timing

Table 43. SPI Slave Interface Electrical Characteristics

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| $f_{OP}$ | Operating frequency | | 0.1 | - | 20 | MHz |
| $t_{PWH}$ | SCLK Pulse Width High | | - | 25 | - | ns |
| $t_{PWL}$ | SCLK Pulse Width Low | | - | 25 | - | |
| $t_{SU1}$ | nCS Setup Time to SCLK rising or falling edge | | - | 7 | - | ns |
| $t_{HD1}$ | nCS Hold Time from SCLK rising or falling edge | | - | 10 | - | ns |
| $t_{SU2}$ | SDIO Setup Time to SCLK rising or falling edge | | - | 4 | - | ns |
| $t_{HD2}$ | SDIO Hold Time from SCLK rising or falling edge | | - | 1 | - | ns |
| $t_{D1}$ | Read Data Valid Time from SCLK rising or falling edge with no data delay added | | - | 6 | - | ns |
| $t_{D1d}$ | Read Data Valid Time from SCLK rising or falling edge including half period of SCLK delay added to data timing | [1] | - | 6 + half SCLK period | - | ns |
| $t_{D2}$ | SDIO Read Data Hi-Z Time from CS High | [2] | - | 10 | - | ns |

1. Adding the extra half period of delay is a register programming option to emulate read data being clocked out on the opposite edge of the SCLK to the write data.
2. This is the time until the device releases the signal. Rise time to any specific voltage is dependent on pull-up resistor strength and PCB trace loading.

**Table 44. Power Supply Noise Rejection**

| Symbol | Parameter | Conditions | Minimum | Typical | Maximum | Unit |
|---|---|---|---|---|---|---|
| PSNR | Power Supply Noise Rejection [1][2][3][4]<br>1.8V operation | $f_{NOISE} \leq$ 1MHz, VDDO[0:6] [5] | -146 | -112 | - | dBc |
| | | $f_{NOISE} \leq$ 1MHz | -76 | -69 | - | |
| | | $f_{NOISE} \leq$ 100kHz | -138 | -135 | - | |
| | | $f_{NOISE} \leq$ 100kHz | -97 | -85 | - | |
| | | 100kHz $\leq f_{NOISE} \leq$ 500kHz | -140 | -139 | - | |
| | | 100kHz $\leq f_{NOISE} \leq$ 500kHz | -138 | -105 | - | |
| | | 500kHz $\leq f_{NOISE} \leq$ 1MHz | -144 | -143 | - | |
| | | 500kHz $\leq f_{NOISE} \leq$ 1MHz | -93 | -90 | - | |
| PSNR | Power Supply Noise Rejection [1][3][4][6]<br>2.5V or 3.3V operation | $f_{NOISE} \leq$ 1MHz, VDDO[0:6] [5] | -146 | -112 | - | dBc |
| | | $f_{NOISE} \leq$ 1MHz | -76 | -69 | - | |
| | | $f_{NOISE} \leq$ 100kHz | -138 | -135 | - | |
| | | $f_{NOISE} \leq$ 100kHz | -94 | -85 | - | |
| | | 100kHz $\leq f_{NOISE} \leq$ 500kHz | -140 | -139 | - | |
| | | 100kHz $\leq f_{NOISE} \leq$ 500kHz | -138 | -105 | - | |
| | | 500kHz $\leq f_{NOISE} \leq$ 1MHz | -144 | -143 | - | |
| | | 500kHz $\leq f_{NOISE} \leq$ 1MHz | -93 | -90 | - | |

1. Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
2. VDDX = VDDR = VDDR2 = VDDA = VDD[0:6] = 1.8V ±5%, VSS = 0V, TA = -40°C to 85°C.
3. 50mV peak-to-peak sine wave applied injected on indicated power supply pin(s).
4. Noise spur amplitude measured relative to 156.25MHz carrier frequency.
5. Excluding VDDOx of the output being measured.
6. VDDX = VDDR = VDDR2 = VDDA = VDD[0:6] = 2.5V or 3.3V ±5%, VSS = 0V, TA = -40°C to 85°C.

# 3. Functional Description

The RC310xxB is a small-form factor, fully integrated, low-power, high performance frequency synthesizer with jitter attenuation and network synchronization capabilities. The device is optimized to deliver excellent phase noise as required for driving Ethernet PHYs/switch, ASICs, or FPGAs. The RC310xxB supports JEDEC JESD204B/C for converter synchronization, JEDEC JESD204B/C converter synchronization, IEEE1588, and SyncE for network-based synchronization.

The following sections provide an overview of the RC310xxB.

## 3.1 Power-Up, Configuration, and Serial Interfaces

The RC310xxB can be powered up and configured in three ways:

1. From 1 of 27 internal non-volatile memory using OTP user configurations (UserCfgs)
2. From its slave serial interface
3. From an external I2C EEPROM

The RC310xxB supports three slave serial interfaces (I2C, SPI, and SMBUS), and one serial master interface (I2C). These interfaces share the same pins, so only one is available at a time.

## 3.2 Input Clocks

The RC310xxB supports one crystal/reference input that is used as a reference to the analog PLL (APLL) and up to two differential or four single-ended clock inputs that are used as a reference to the digital PLL (DPLL) and support hitless reference switching.

### 3.2.1 Crystal/Reference Input

The crystal input supports crystal frequencies of 8MHz to 80MHz. It has programmable internal load capacitors to support crystals with CL = 6pF to 12pF.

The crystal input may being over-driven with differential or single-ended inputs with proper external terminations. It also supports being over-driven with a clipped sine-wave TCXO with a $0.8V_{PP}$ signal.

The supported frequency range is same as reference clock inputs: 1kHz to 650MHz in differential mode, and 1kHz to 200MHz in single-ended mode.

An available LOS monitor detects the loss of signal on crystal input.

### 3.2.2 Clock Inputs

There are two differential clock inputs that support LVDS, HCSL, or single-ended CMOS logic levels without external terminations. LVPECL or CML clock inputs may be supported with external terminations and/or AC coupling. Internal terminations are available for both HCSL and LVDS logic levels. Additionally, HCSL input terminations support both 100ohm and 85ohm operating environments.

If set to single-ended type, the differential inputs turn into two single-ended inputs. CLKIN0 drives clkin0 internally, CLKIN0b drives clkin1 internally. CLKIN1 drives clkin2 internally, and CLKIN1b drives clkin3 internally. If set to differential type, CLKIN0/CLKIN0b pair drives clkin0 while CLKIN1/CLKIN1b pair drives clkin2. Internal biasing is available for AC-coupled applications. The two clock inputs can be left floating when unused. An available LOS monitor detects the loss of signal on crystal input. Frequency monitoring is also available on the clock inputs.

## 3.3 Clock Input Monitors

There are two types of reference clock monitors. The APLL input is monitored for Loss of Signal (LOS). While the DPLL clock inputs (CLKIN0, CLKIN0B, CLKIN1, CLKIN1B) each have LOS, activity and frequency monitoring.

- The LOS monitor detects missing edges over a window of several reference clock periods. For the best accuracy, it is recommended to program the window to be equal to at least 8 times that of the measuring clock period.
- The frequency monitor may be configured to measure the reference over a nominal 5ms time window in order to achieve ~1ppm granularity.
- The frequency monitor may be configured to measure the reference over a nominal 0.4s time window in order to achieve ~12ppb granularity.

## 3.4 APLL

The APLL is fractional LC-VCO based PLL with an operating range from 9.5GHz to 10.7GHz. Any of the available input clocks can be selected to drive the APLL, and the input clock can be frequency doubled for increased performance. The APLL is temperature compensated for the utmost frequency stability. For synchronous, deterministic requirements, the APLL also supports ZDB mode where CLKIN0 is used for the feedback input.

### 3.4.1 APLL Lock Detector

The APLL lock detector indicates whether the APLL is locked to a functioning crystal or reference input by monitoring the phase errors. Lock status can be sent on to a GPIO pin or in the register map.

## 3.5 DPLL

To operate as a network synchronizer or jitter attenuator, the DPLL and APLL are nested and form a fractional-N DPLL architecture. The System APLL locks to an input clock from a crystal or a crystal oscillator and generates an output clock of approximately 10GHz. The APLL uses a fractional feedback divider with 26-b numerator and fixed 26-b denominator to generate its feedback clock. The fractional feedback divide ratio is dynamically controlled by the DPLL. The DPLL also uses the APLL’s VCO clock to generate the fractional divided DPLL feedback clock. The DPLL fractional feedback divider, which is comprised of 48-b numerator and 48-b denominator, is static during normal operation. The DPLL can also be optionally disabled to operate the RC31008/31012A in synthesizer/DCO mode.

## 3.6 DPLL Reference Selection

The DPLL can lock to one of either the two differential or the four single ended input clocks. The reference selection can be either automatic or manual and when enabled, hitless switching results in negligible (< 100ps) output clock initial phase hit during reference switching or the DPLL exiting from holdover.

### 3.6.1 Manual Reference Selection

In manual mode, the selection is set either by GPIO or GPI pins or in the register map.

### 3.6.2 Automatic Reference Selection

In automatic mode, the selection is based on clock quality statuses and priorities. The quality statuses are from clock monitors. If two clock inputs are programmed to the same priority, the one with lower index number takes precedence (e.g., clkin0 takes precedence over clkin1).

The automatic reference selection can either be revertive or non-revertive. In revertive mode, the reference clock that is qualified and of the highest priority is always selected. If a reference clock of higher priority than the currently selected one becomes qualified, the DPLL will switch to that reference clock; if a reference clock of equal or lower priority than the currently selected one becomes qualified, the DPLL will keep the current reference clock.

In non-revertive mode, if there is a higher priority reference clock is coming back (from disqualified to qualified), the current selected reference clock remains selected unless it gets disqualified.

### 3.6.3 Hitless Reference Switching

If hitless switching is enabled, the output clock initial phase hit will be minimized (< 100ps) during reference switching or the DPLL exiting from holdover, while the input clock and output clock may no longer be aligned. If hitless switching is disabled, the output clock phase change slope is determined by DPLL loop characteristics and phase slope limit.

Minimal initial phase hit of < 100ps can only be met during reference switching when the reference clocks are of same fractional frequency offset. If they are of different fractional frequency offset (up to 200ppm), the output clock phase will track to the new reference clock.

## 3.7 DPLL Operating Modes

The DPLL can operate in six different states: Free-run, Acquire, Normal, Holdover, Hitless-switch, and Write-frequency. The state transitions can either be manual or automatic.

### 3.7.1 Free-run

During power-on reset or VCO calibration or in synthesizer mode, the DPLL is in the free-run state. In this state, no reference clock is used and the output clocks are tracking the APLL reference clock.

### 3.7.2 Acquire

When there is at least one qualified reference, the DPLL will be tracking the selected qualified reference at the acquisition bandwidth and damping factor settings. If the reference clock is disqualified and no other qualified reference clock is available, the DPLL transitions to either the free-run state or the holdover state. When lock-detector detects a lock, DPLL transitions to the normal state.

### 3.7.3 Normal

In the normal state, the DPLL is tracking the selected reference clock with the normal locking bandwidth and damping factor settings. If the selected reference clock is disqualified, the state machine goes to either the holdover or the free-run state. At a reference switch, the state machine goes via the Holdover state to the Hitless Switch state or the Acquire state.

### 3.7.4 Holdover

In the holdover state, the DPLL output frequency will be held at the instantaneous value or a value that is low pass filtered and/or restored from the holdover history registers. The initial holdover accuracy is less than 50ppb.

### 3.7.5 Hitless Switch

At a hitless reference switch or a hitless transition from the holdover state, the DPLL’s TDC will measure the phase offset between the (newly) selected reference clock and the feedback clock, both of which are averaged. This offset is stored in an internal phase offset register. As a result, the output clocks will experience a minimal phase transient due to the reference switch or coming out of holdover. After the hitless switch procedure has finished, the state machine transitions to the Acquire state unless the reference clock fails.

### 3.7.6 Write Frequency

In the write-frequency mode the DPLL is not tracking any reference clock. The DPLL output frequency offset is directly controlled by preset value in the register map.

### 3.7.7 Manual Mode

The DPLL operation can be forced to the free-run, holdover, and write-frequency states.

## 3.8 DPLL Lock Detector

The DPLL lock detector declares lock when the phase from the phase detector remains within a programmable range for a programmable time interval both of which are set in the register map. This indicates that the DPLL is locked to the reference clock input. Once the phase output from the phase detector has been below the lock threshold for half of the programmed lock interval, the internal lock signal is asserted and the normal loop filter bandwidth and damping applied to the DPLL's loop filter instead of the acquire filter settings.

## 3.9 Output Dividers

The RC310xxB provides four integer and three fractional output dividers.

### 3.9.1 Integer Output Dividers

All four Integer Output Dividers (IOD) are identical. They use a 25-bit divider to provide output frequencies of 1kHz to 650MHz from the VCO clock. Changing IOD values results in an immediate change to the new frequency. Glitch-less squelch and release of the IOD clock is supported. When enabled, this mimics a gapped clock behavior when an IOD frequency is changed.

#### 3.9.1.1 SYSREF Generation

The RC310xxB supports pulse mode SYSREF generation within each IOD and the number of pulses is programmable. Partial SYSREF (generating SYSREF pulses on a subset of the outputs configured for SYSREF) is also supported. The phase of each IOD in the group can be independently adjusted if skew is intended.

### 3.9.2 Fractional Output Dividers

There are three Fractional Output Dividers (FOD). Each FOD can divide down the VCO clock to provide frequencies from 1kHz to 650MHz. Each FOD is implemented in two stages. The first stage is an 8-bit fractional divider with Digital Control Delay (DCD) correction. The DCD FOD allows a divide down of the VCO clock to 30MHz to 650MHz. A 17-bit second-stage integer divider with minimum divide ratio of 4 and a maximum ratio of $2*(2^{17}-1)$ allows output frequencies lower than 30MHz. For output frequencies above 30MHz, this second-stage divider may be bypassed.

#### 3.9.2.1 Spread-Spectrum Clocking

FOD0 and FOD1 support Spread-Spectrum Clocking (SSC).

When SSC is enabled, the spread spectrum engine modulates the FOD divider ratio with a triangular modulation pattern. The modulation can be programmed for either down-spread or center-spread. The SSC modulation frequency can be programmed to a value between 30kHz to 63kHz. The SSC amplitude can be programmed in 0.05% steps to -1.5% for down spread, or ±1.5% for center spread. When turning off SSC, the current modulation cycle completes, returning the output to the non-spreading frequency before the SSC stops.

#### 3.9.2.2 Sync and Phase Adjustment

Each FOD can adjust its output clock phase with a step size of 1/4 VCO period up to about ±20ns. The adjustment can be of either positive or negative directions.

IOD phase adjustment is same as FOD phase adjustment but with a step size of one VCO period.

#### 3.9.2.3 Digital Controlled Oscillator (DCO) Mode

In DCO mode, a frequency control word is passed directly from an external processor or FPGA to the DPLL with a step size of $1/2^{40}$ or 0.91 parts per trillion (ppt) and a full-range of ±244 parts per million (ppm) from the nominal DPLL output frequency. The frequency control word (FCW) is written to a 29-b wide register in two's-complement and then applied to the DPLL feedback divider. The reference clock inputs are unused in this mode.

#### 3.9.2.4 Numerically Controlled Oscillator (NCO) Mode

In NCO mode, each FOD can adjust its output clock frequency with a step size of $1/2^{34}$ or 58.21 ppt and is based on incrementing the numerator while holding the 34-b denominator at a fixed value. This frequency change at the output clock is gradual without glitches. The APLL can be in either clock synthesizer/DCO or in jitter attenuator mode.

## 3.10 Clock Outputs

The RC310xxB supports up to 12 differential or 24 single-ended clock outputs or any combination of differential and single-ended clock outputs. Every differential clock output can be programmed as two single-ended clock outputs.

### 3.10.1 Output Types

The RC310xxB outputs drive HCSL inputs (such as those used in PCIe applications) directly. They use Low-Power HCSL (LP-HCSL) driver technology to eliminate external termination resistors. The LP-HCSL outputs can be set to 85ohm or 100ohm differential output impedance. The LP-HCSL outputs have selectable output swing and slew rate settings.

The RC310xxB outputs may also be set to LVDS. LVDS outputs require only a 100ohm resistor between the true and complement inputs of the receiver clock input. LVDS outputs have selectable amplitude. Both LVDS and LP-HCSL outputs provide LVPECL and CML-compatible output swing levels by using external AC coupling.

If set to single-ended mode, the output pair can drive either pin or both pins. If both pins are enabled, they can be in phase, or inverted phase. The single-ended outputs support CMOS swings of 1.8V, 2.5V, or 3.3V as determined by their VDDO voltage.

### 3.10.2 Output Banks

The RC310xxB maps the internal and external frequency sources to output banks, that can be programmed in register out_bank_src, according to Table 45. There are up to 12 clock outputs arranged in seven output banks. Each bank sits on its own VDDO (each VDDO also supplies an IOD or FOD according to Table 46).

**Table 45. Output Bank Source Mapping**

<table>
<tr><th rowspan="2">output_bank_src</th><th>Bank 0</th><th>Bank 1</th><th>Bank 2</th><th>Bank 3</th><th>Bank 4</th><th>Bank 5</th><th>Bank 6</th></tr>
<tr><th>OUT0</th><th>OUT1</th><th>OUT[2:3]</th><th>OUT[4:7]</th><th>OUT[8:9]</th><th>OUT10</th><th>OUT11</th></tr>
<tr><td>0x0</td><td colspan="2">IOD0</td><td colspan="2">N/A</td><td colspan="3">CLKIN1</td></tr>
<tr><td>0x1</td><td colspan="3">IOD1</td><td colspan="2">N/A</td><td>XIN_REFIN</td><td>N/A</td></tr>
<tr><td>0x2</td><td colspan="4">N/A</td><td colspan="3">IOD2</td></tr>
<tr><td>0x3</td><td colspan="5">N/A</td><td colspan="2">IOD3</td></tr>
<tr><td>0x4</td><td colspan="4">FOD0</td><td colspan="3">N/A</td></tr>
<tr><td>0x5</td><td colspan="7">FOD1</td></tr>
<tr><td>0x6</td><td colspan="3">N/A</td><td colspan="4">FOD2</td></tr>
<tr><td>0x7</td><td colspan="4">N/A</td><td colspan="3">CLKIN0</td></tr>
</table>

**Table 46. VDD Pin Assignments for Outputs, Integer Output Dividers, and Fractional Output Dividers**

| $V_{DDO0}$ | $V_{DDO1}$ | $V_{DDO2}$ | $V_{DDO3}$ | $V_{DDO4}$ | $V_{DDO5}$ | $V_{DDO6}$ | $V_{DDX}$ | $V_{DDR}$ | $V_{DDD}$ | $V_{DDA}$ |
|---|---|---|---|---|---|---|---|---|---|---|
| IOD0, OUT0 | IOD1, OUT1 | FOD0, OUT[2:3] | FOD1, OUT[4:7] | FOD2, OUT[8:9] | IOD2, OUT10 | IOD3, OUT11 | XO, XIN_REFIN, XOUT_REFINb | GPI[3:0] | SCL_SCLK, SDA_nCS, GPIO[4:0], DPLL | PLL |

# 4. Application Information

## 4.1 Recommendations for Unused Input and Output Pins

### 4.1.1 CLKIN/CLKINb [1:0] Inputs

For applications that do not require the use of reference clock inputs, both CLKIN and CLKINb should be left floating. If the CLKIN/CLKINb inputs are connected but not used by the device, Renesas recommends that CLKIN and CLKINb be connected to static signals, not active signals.

### 4.1.2 LVCMOS Control Pins

LVCMOS control pins have selectable internal pull-ups and/or pull-downs. Additional resistance is not required but may be added for additional protection. A 10kΩ resistor can be used.

### 4.1.3 LVCMOS Outputs

Any LVCMOS output may be left floating if unused. There should be no trace attached. The mode of the output buffer should be set to high impedance state to avoid unnecessary noise generation.

### 4.1.4 Differential Outputs

All unused differential outputs may be left floating. There should be no trace attached. Both sides of the differential output pair should be treated the same, either left floating or terminated.

## 4.2 CLKIN/CLKINb Clock Inputs Interface

The RC310xxB provides a programmable input buffer for reference clock inputs, as shown in Figure 5. This programmable buffer supports most standard signaling protocols with no need for external termination components at the receiver end of the transmission line.

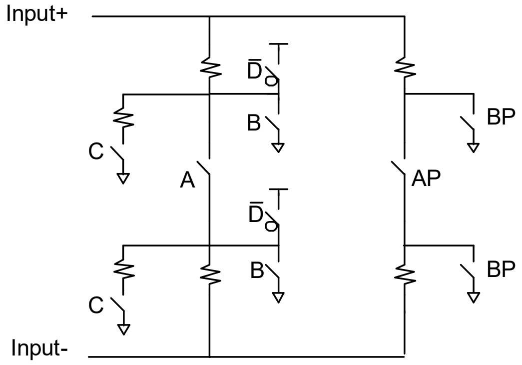


**Figure 5. Programmable Input Buffer Logical Diagram**

By making appropriate register selections, the switches labeled in Figure 5 can be closed as shown in Table 47 to support the indicated protocols. With the switches closed as indicated, the input buffer will operate as shown in Figure 6 for the various input reference signal protocols. Note that HCSL is used in both 100ohm and 85ohm transmission line environments and this input buffer supports both with no external terminations required.

Table 47. Input Buffer Programming Options for Specific Signaling Protocols

| Input Signaling Protocol | Switches Closed | $V_{DDR}$ Voltage Required |
|---|---|---|
| 2.5V LVPECL | A, C | 2.5V |
| 3.3V LVPECL | A, C | 3.3V |
| LVDS (85 ohms) | A, AP | 1.8V / 2.5V / 3.3V |
| LVDS (100 ohms) | A | 1.8V / 2.5V / 3.3V |
| 1.8V LVCMOS | - | 1.8V |
| 2.5V LVCMOS | - | 2.5V |
| 3.3V LVCMOS | - | 3.3V |
| CML | D | 3.3V |
| HCSL (42.5 ohms) | B, BP | 1.8V / 2.5V / 3.3V |
| HCSL (42 ohms) | B | 1.8V / 2.5V / 3.3V |
| Externally AC-coupled[1] | - | 1.8V / 2.5V / 3.3V |

1. In this mode of operation, AC-coupling capacitors must be used to isolate the voltage level of the transmitter from the receiver. The signal must be properly terminated on the transmitter side of the AC-coupling capacitors. Bias terminations are needed between the AC-coupling capacitors and the RC310xxB.

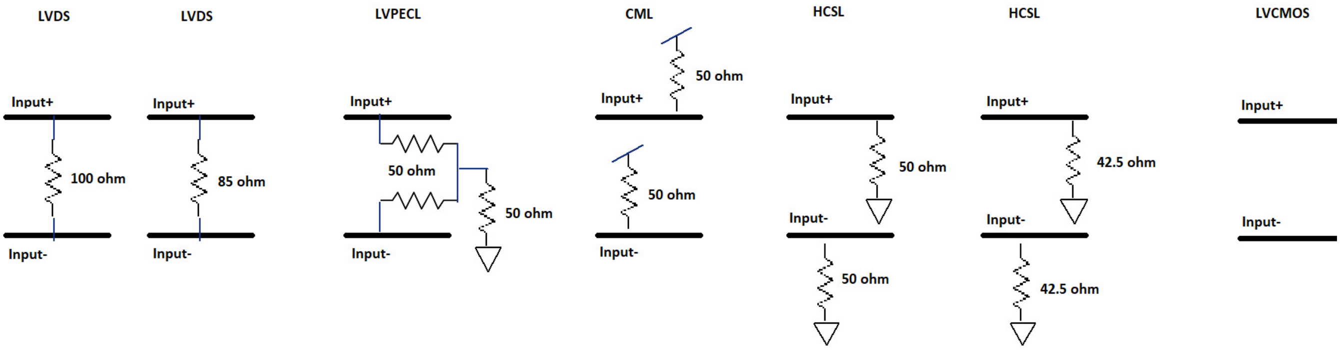


Figure 6. Input Buffer Behavior by Protocol

## 4.3 Overdriving the XTAL Interface

### 4.3.1 XTAL Interface Set to Input Buffer Mode

The RC310xxB has two bits to disconnect the internal XO and enable input buffer mode on the XIN_REFIN/XOUT_REFINb pins. First, setting sel_ib_xo = 0, disconnects the internal XO. Next, setting xo_ib_cmos_sel = 1 enables the LVCMOS input clock path. Setting these two bits as indicated removes any AC-coupling or input voltage requirements for overdriving the XTAL interface. Note that the maximum input swing is still governed by the VDDX supply rail. Once set to Input Buffer Mode, the input can be directly driven with a single-ended or differential oscillator. There is no internal termination capability when using the XTAL interface in input buffer mode. Other than this lack of internal terminations, the input buffer mode has all capabilities of the CLKIN/CLKINb interfaces.

### 4.3.2 XTAL Interface in XO Mode, Input Buffer Mode Not Selected

If the two bits mentioned above are not set as indicated, then there is a limitation of 1.2V on the XIN_REFIN/XOUT_REFINb pins. Input buffer mode is preferred as described in section 4.3.1.

The XIN_REFIN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XOUT pin can be left floating. The amplitude of the input signal should be between

500mV and 1.2V, and the slew rate must be ≥0.2V/ns. For 1.2V LVCMOS, inputs can be DC-coupled into the device as shown in Figure 7. For LVCMOS drivers with > 1.2V swing, the amplitude must be reduced from full swing to at least 1.2V in order to prevent signal interference with the power rail. The sum of the driver output impedance and Rs must equal the transmission line impedance to prevent overshoot and undershoot.

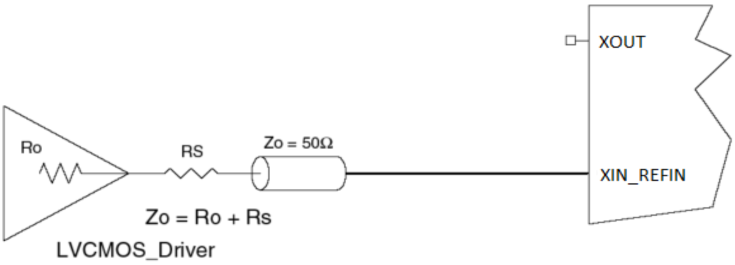


**Figure 7. 1.2V LVCMOS Driver to XTAL Input Interface**

Figure 8 shows an example of the interface diagram for a high-speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equal the transmission line impedance. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. We also need to scale the 3.3V LVCMOS swing to 1.2V (~1/3 of the swing). This yields R1 = 2 x R2 while R1 || R2 = 50Ω. Solving for a 50Ω ohm system gives R1 = 150Ω and R2 = 75Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Different scaling factors are required for 2.5V and 1.8V LVCMOS drivers.

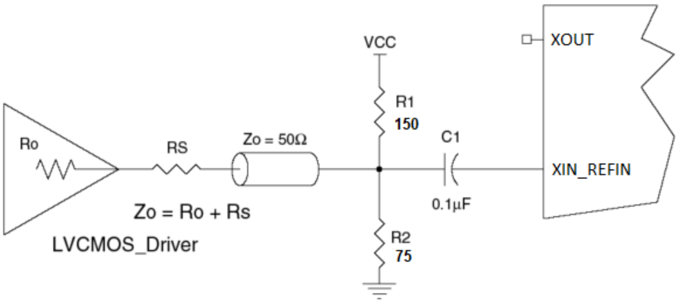


**Figure 8. LVCMOS Driver to XTAL Input Interface**

Figure 9 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XIN_REFIN input. Renesas recommends that all components in the schematics be placed in the layout. Though some components may not be used by the application, they can be used for debugging purposes.

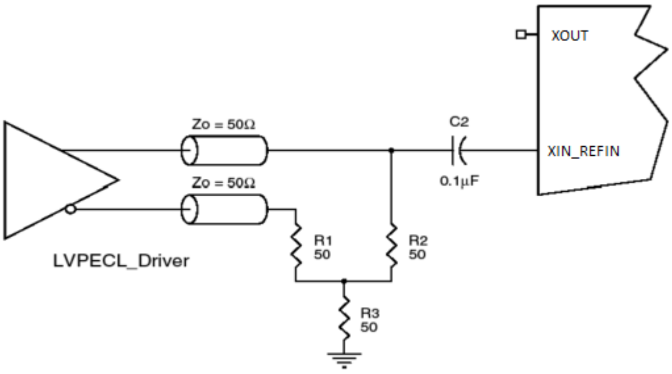


**Figure 9. LVPECL Driver to XTAL Input Interface**

## 4.4 Differential Output Terminations

### 4.4.1 Direct-Coupled LP-HCSL Termination

For the LP-HCSL differential protocol, the following termination scheme is recommended (see Figure 10). The RC310xxB supports internal source terminations (see Figure 10*)* for 85 ohm or 100 ohm differential transmission lines. No external components are needed.

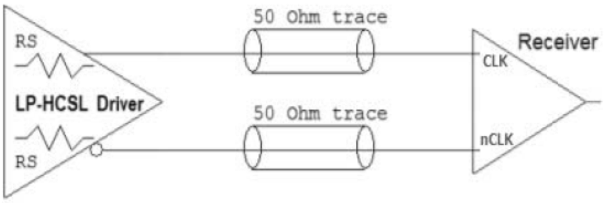


Figure 10. Standard HCSL Termination

### 4.4.2 Direct-Coupled LVDS Termination

For LVDS differential protocol, the following termination scheme is recommended (see Figure 11). The recommended value for the termination impedance ($Z_T$) is between 90Ω and 132Ω. The actual value should be selected to match the differential impedance ($Z_0$) of the transmission line. A typical point-to-point LVDS design uses a 100Ω parallel resistor at the receiver in a 100Ω differential transmission-line environment. In order to avoid any transmission-line reflection issues, any external components should be surface-mounted and must be placed as close to the receiver as possible.

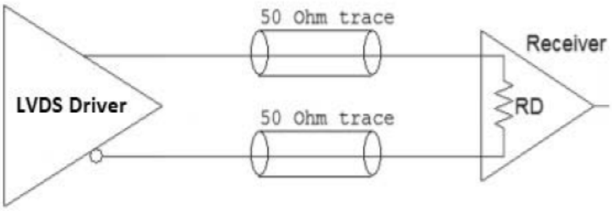


Figure 11. Standard LVDS Termination

### 4.4.3 AC-Coupled Differential Terminations for Other Protocols

Alternate differential protocols including LVPECL, CML and SSTL can be supported with AC-coupled LP-HCSL outputs. Figure 12 shows a typical AC-coupled termination scheme for a 100Ω differential transmission-line environment. The RC310xxB supports a differential swing of 1.6V or 1.8V in LP-HCSL mode.

No terminations are needed between the RC310xxB and the AC-coupling capacitors. The resistors on the receiver side of the AC-coupling capacitors provide an appropriate voltage bias for the particular receiver. Finally, a 100Ω resistor across the differential pair (located near the receiver) attenuates reflections that may corrupt the clock signal integrity.

Often, receivers used with a high-performance device like the RC310xxB are equipped with internal terminations, voltage biasing, and even AC-coupling. Please consult your particular the receiver specification to determine if any or all of the indicated external components in Figure 12 are needed.

Refer to *Driving LVPECL, LVDS, CML, and SSTL Logic with Renesas' "Universal" Low-Power HCSL Outputs"* (AN-891) on the RC310xxB product page for additional information on both re-biasing and amplitude attenuation.

If a smaller differential swing is desired as a starting point, refer to "LVDS Termination" in *Quick Guide - Output Terminations (AN-953)* located on the RC310xxB product page.

Please contact Renesas for additional support, if necessary.

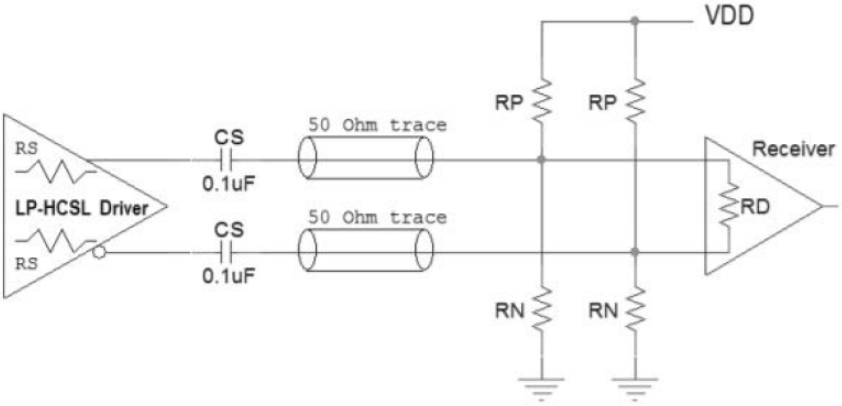


**Figure 12. AC-Coupling Termination**

## 4.5 Crystal Recommendations

For the latest vendor / frequency recommendations, please contact Renesas.

## 4.6 External I$^2$C Serial EEPROM Recommendations

An external I$^2$C EEPROM can be used to store configuration data, please contact Renesas for specific recommendations. A specific configuration code is required for the devices to access an external I$^2$C serial EEPROM at power up. See the ordering information.

## 4.7 Power Considerations

The electrical characteristics tables provide current consumption values for various blocks and output configurations, and can be used to estimate total current consumption for a particular design. The Renesas IC Toolbox, available on the Renesas website, can also be used to estimate current consumption. A quick note on terms used in this section: “power rail” refers to the power connection to a particular VDD pin. This means that different VDD pins might be connected to the same voltage, yet may also be connected to different power rails. We will use “power rail” when discussing power sequencing considerations.

### 4.7.1 Power Sequencing Considerations

The RC310xxB has no specific power sequencing requirements. The design software may be used to disconnect unused power supply pins in the silicon, which then allows the user to leave these unused supply pins unconnected. These unused pins are then removed from power sequencing considerations.

The RC310xxB also has two GPIO functions (PWRGD/PWRDN# or PWRGD/RESTART#) which give the user more control over power up timing in applications environments such as data centers. These environments often need to hold clocks in reset until the devices receiving the clocks have completed their power-up housekeeping and are ready to receive clocks. We discuss operation without this GPIO function first, followed by a discussion with this GPIO function.

#### 4.7.1.1 Power-Up Operation without PWRGD/PWRDN# or PWRGD/RESTART# Function

When PWRGD/PWRDN# or PWRGD/RESTART# is not used, the RC310xxB outputs are gated by the last VDD pin to become valid. See Table 19 for details.

#### 4.7.1.2 Power-Up Using PWRGD/PWRDN# or PWRGD/RESTART#

Using the PWRGD/PWRDN# or PWRGD/RESTART# GPIO configuration gives the user more control over power-up behavior. Holding the pin low, pauses the RC310xxB start-up sequence until the pin is asserted high. This pin should be held low from the very beginning of the power up sequence. The pin function is defined as follows:

- PWRGD means Power is Good (active high). Asserting PWRGD/PWRDN# or PWRGD/RESTART# high after all power rails are valid, tells the RC310xxB that power is good, power up completely and begin operation. The *first* high assertion of PWRGD/PWRDN# loads a new configuration into the device (selected by external pins if there are multiple configurations). Subsequent high assertions of PWRGD/PWRDN# return to the previously loaded configuration.
- PWRDN# means enter Power Down (active low). Asserting PWRGD/PWRDN# low puts (or keeps) the RC310xxB in a low power state, turning off as much internal logic as possible (including the APLL) to save the most power while keeping the power rails active. Returning from PWRDN# by asserting PWRGD/PWRDN# high resumes the previous operating state.
- RESTART# means Restart (active low). Asserting PWRGD/RESTART# low resets the RC310xxB and prepares it for a complete restart of entire power up sequence without having to remove the power supplies. Returning from RESTART# by asserting the PWRGD/RESTART# pin high loads a new configuration, which may or may not be different from the one used before RESTART# asserted low.

Figure 13 shows use of a PWRGD/PWRDN# or PWRGD/RESTART# input to hold the entire RC310xxB until all power supply rails reach 1.62V. The PWRGD\PWRDN# pin must be held low for at least $t_{HOLD}$after the last VDDO pin reaches 1.62V. It may be held longer. Using the PWRGD/PWRDN# or PWRGD/RESTART# GPIO function isolates the RC310xxB from changes to power supply sequencing that may be induced by changes to other devices in the system. A configuration can contain PWRGD/PWRDN# *or* PWRGD/RESTART#, not both. If the power down state is not used, PWRGD/RESTART# is the preferred configuration, since it allows more flexibility with GPI/GPIO assignment.

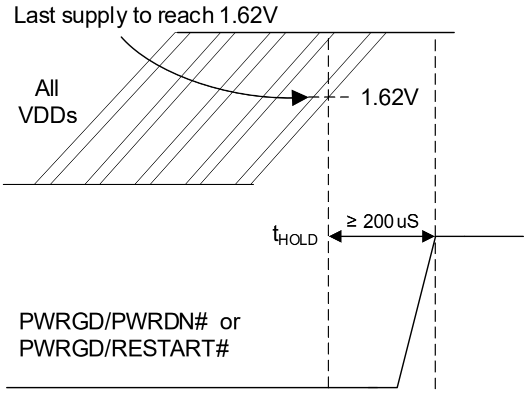


**Figure 13. Power Supply Sequencing Recommendations – Power-Up Using PWRGD/PWRDN# or POR#**

# 5. Thermal Information

## 5.1 VFQFPN ePad Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 14. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

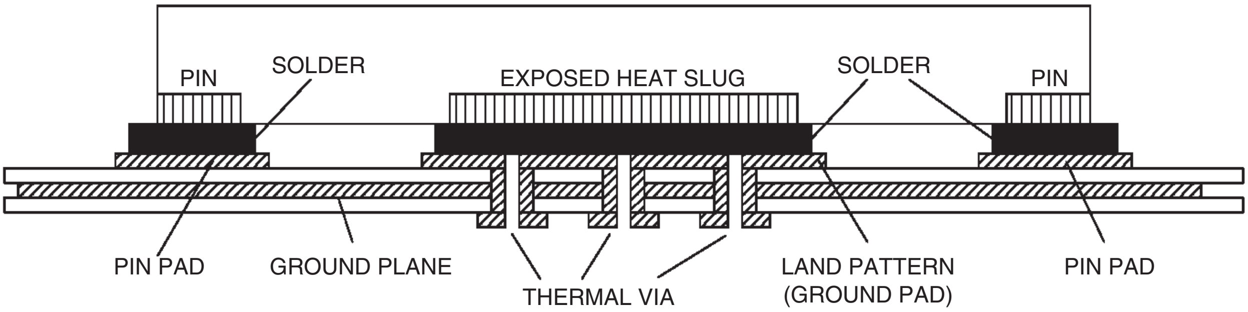


**Figure 14. P.C. Assembly for Exposed Pad Thermal Release Path – Side View**

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes.” The number of vias (i.e., “heat pipes”) are application specific and dependent on the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed.

Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33 mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Lead frame Base Package, Amkor Technology.

## 5.2 Thermal Characteristics

**Table 48. Thermal Characteristics (48-pin with External Crystal) [1]**

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JC}$ | Theta $J_C$. Junction to Device Case Thermal Coefficient [2] | 20.1 | °C/W |
| $\theta_{JB}$ | Theta $J_B$. Junction to Board Thermal Coefficient [2] | 1.9 | |
| $\theta_{JA}$ | Junction to Ambient Air Thermal Coefficient (still air) | 25.8 | |
| | Junction to Ambient Air Thermal Coefficient 1 m/s air flow | 21.5 | |
| | Junction to Ambient Air Thermal Coefficient 2 m/s air flow | 18.8 | |
| | Junction to Ambient Air Thermal Coefficient 3 m/s air flow | 17.9 | |
| - | Moisture Sensitivity Rating (Per J-STD-020) | 3 | N/A |

1. JEDEC Standard PCB (101.6 x 114.5 x 1.6 mm) with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 25 thermal vias.

Table 49. Thermal Characteristics (40-pin with External Crystal) [1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JC}$ | Theta $J_C$. Junction to Device Case Thermal Coefficient [2] | 35.7 | °C/W |
| $\theta_{JB}$ | Theta $J_B$. Junction to Board Thermal Coefficient [2] | 1.9 | |
| $\theta_{JA}$ | Junction to Ambient Air Thermal Coefficient (still air) | 28.9 | |
| | Junction to Ambient Air Thermal Coefficient 1 m/s air flow | 25.6 | |
| | Junction to Ambient Air Thermal Coefficient 2 m/s air flow | 23 | |
| | Junction to Ambient Air Thermal Coefficient 3 m/s air flow | 21.8 | |
| - | Moisture Sensitivity Rating (Per J-STD-020) | 3 | N/A |

1. JEDEC Standard PCB (101.6 × 114.5 × 1.6 mm) with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 16 thermal vias.

Table 50. Thermal Characteristics (48-pin with Internal Crystal) [1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JC}$ | Theta $J_C$. Junction to Device Case Thermal Coefficient [2] | 24.5 | °C/W |
| $\theta_{JB}$ | Theta $J_B$. Junction to Board Thermal Coefficient [2] | 15 | |
| $\theta_{JA}$ | Junction to Ambient Air Thermal Coefficient (still air) | 37.3 | |
| | Junction to Ambient Air Thermal Coefficient 1 m/s air flow | 35 | |
| | Junction to Ambient Air Thermal Coefficient 2 m/s air flow | 33 | |
| | Junction to Ambient Air Thermal Coefficient 3 m/s air flow | 32 | |
| - | Moisture Sensitivity Rating (Per J-STD-020) | 3 | N/A |

1. JEDEC Standard PCB (101.6 x 114.5 x 1.6 mm) with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 25 thermal vias.

Table 51. Thermal Characteristics (40-pin with Internal Crystal) [1]

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JC}$ | Theta $J_C$. Junction to Device Case Thermal Coefficient [2] | 35 | °C/W |
| $\theta_{JB}$ | Theta $J_B$. Junction to Board Thermal Coefficient [2] | 52.4 | |
| $\theta_{JA}$ | Junction to Ambient Air Thermal Coefficient (still air) | 70.7 | |
| | Junction to Ambient Air Thermal Coefficient 1 m/s air flow | 65.9 | |
| | Junction to Ambient Air Thermal Coefficient 2 m/s air flow | 62.5 | |
| | Junction to Ambient Air Thermal Coefficient 3 m/s air flow | 61 | |
| - | Moisture Sensitivity Rating (Per J-STD-020) | 3 | N/A |

1. JEDEC Standard PCB (101.6 × 114.5 × 1.6 mm) with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 16 thermal vias.

Table 52. Thermal Characteristics (32-pin with Internal Crystal) [1]

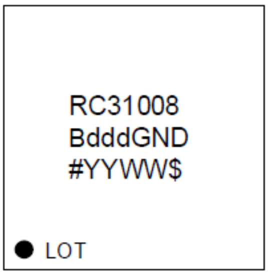
| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $\theta_{JC}$ | Theta $J_C$. Junction to Device Case Thermal Coefficient [2] | 61.2 | °C/W |
| $\theta_{JB}$ | Theta $J_B$. Junction to Board Thermal Coefficient [2] | 7.4 | |
| $\theta_{JA}$ | Junction to Ambient Air Thermal Coefficient (still air) | 40.3 | |
| | Junction to Ambient Air Thermal Coefficient 1 m/s air flow | 37.4 | |
| | Junction to Ambient Air Thermal Coefficient 2 m/s air flow | 34.8 | |
| | Junction to Ambient Air Thermal Coefficient 3 m/s air flow | 33 | |
| - | Moisture Sensitivity Rating (Per J-STD-020) | 3 | N/A |

1. JEDEC Standard PCB (101.6 x 114.5 x 1.6 mm) with two ground and two voltage planes.
2. Assumes ePad is connected to a ground plane using a grid of 4 thermal vias.

# 6. Package Outline Drawings

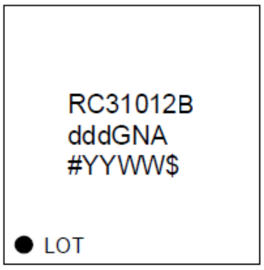
The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

# 7. Marking Diagrams



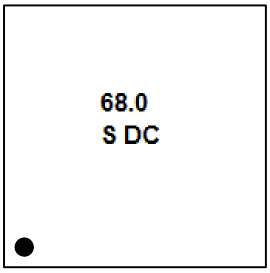
**RC31008Bddd**

- Lines 1 and 2: part number.
  - “ddd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “$” indicates the mark code.



**RC31012Bddd**

- Lines 1 and 2: part number.
  - “ddd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “$” indicates the mark code.

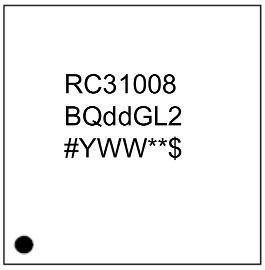


**RC31005BQdd**

Due to package construction, the marking of the RC31005BQdd is that of the integrated crystal. The “dd” dash-code is encoded in a unique digital register “marking” that is documented in the addendum. The crystal marking is defined as follows:

- Line 1: Indicates 68.0MHz crystal frequency.
- Line 2: “S” is crystal vendor. “DC” is the date code which is encoded as follows:

| Last Digit of Year | D (Year Code) | Month | C (Month Code) |
|---|---|---|---|
| 1 | A | 1 | A |
| 2 | B | 2 | B |
| 3 | C | 3 | C |
| 4 | D | 4 | D |
| 5 | E | 5 | E |
| 6 | F | 6 | F |
| 7 | G | 7 | G |
| 8 | H | 8 | H |
| 9 | J | 9 | J |
| 0 | K | 10 | K |
| - | - | 11 | L |
| - | - | 12 | M |



**RC31008BQdd**

- Lines 1 and 2: part number.
  - “dd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YWW” indicates the last digit of the year and work week the part was assembled.
  - “**” indicates the lot sequence number
  - “$” indicates the mark code.

**RC31012BQdd**

- Lines 1 and 2: part number.
  - “dd” indicates preprogrammed device custom configuration dash code.
- Line 3:
  - “#” indicates the stepping number.
  - “YYWW” indicates the last two digits of the year and work week the part was assembled.
  - “$” indicates the mark code.

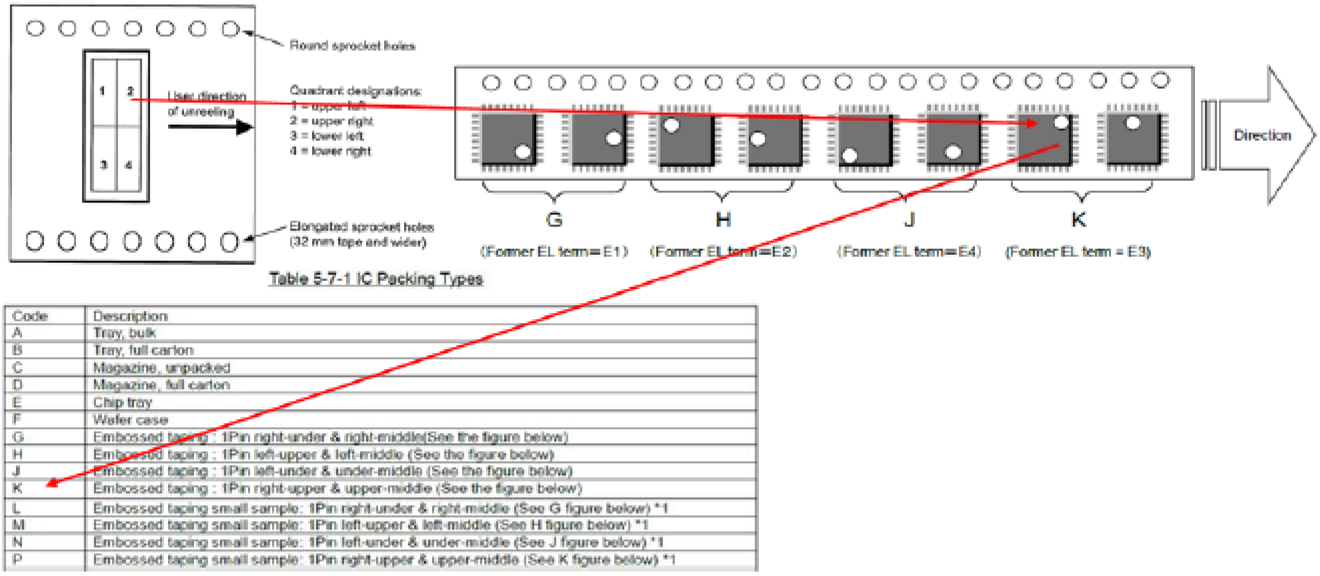


Table 5-7-1 IC Packing Types

| Code | Description |
|---|---|
| A | Tray, bulk |
| B | Tray, full carton |
| C | Magazine, unpacked |
| D | Magazine, full carton |
| E | Chip tray |
| F | Wafer case |
| G | Embossed taping : 1Pin right-under & right-middle(See the figure below) |
| H | Embossed taping : 1Pin left-upper & left-middle (See the figure below) |
| J | Embossed taping : 1Pin left-under & under-middle (See the figure below) |
| K | Embossed taping : 1Pin right-upper & upper-middle (See the figure below) |
| L | Embossed taping small sample: 1Pin right-under & right-middle (See G figure below) *1 |
| M | Embossed taping small sample: 1Pin left-upper & left-middle (See H figure below) *1 |
| N | Embossed taping small sample: 1Pin left-under & under-middle (See J figure below) *1 |
| P | Embossed taping small sample: 1Pin right-upper & upper-middle (See K figure below) *1 |

Figure 15. Pin 1 Orientation in Tape and Reel Packaging

# 8. Ordering Information

Table 53. Ordering Information

| Part Number | Description | Number of Output Pairs | Carrier Type [1] | Pkg. Desc. | Temp. Range |
|---|---|---|---|---|---|
| RC31008B000GND#BB0 | Un-programmed part with external crystal. I2C address is 0x09. | 8 | Tray | 5 × 5 × 0.9 mm, 40-VFQFPN | -40° to +85°C |
| RC31008B000GND#KB0 | | | Tape and Reel | | |
| RC31012B000GNA#BB0 | | 12 | Tray | 6 × 6 × 0.9 mm, 48-VFQFPN | |
| RC31012B000GNA#KB0 | | | Tape and Reel | | |
| RC31008B001GND#BB0 | Un-programmed part with external crystal for use with external I2C EEPROM.<br>I2C address is 0x09 after I2C EEPROM is loaded. | 8 | Tray | 5 × 5 × 0.9 mm, 40-VFQFPN | -40° to +85°C |
| RC31008B001GND#KB0 | | | Tape and Reel | | |
| RC31012B001GNA#BB0 | | 12 | Tray | 6 × 6 × 0.9 mm, 48-VFQFPN | |
| RC31012B001GNA#KB0 | | | Tape and Reel | | |
| RC31008BdddGND#BB0 [2] | Preprogrammed part with external crystal. | 8 | Tray | 5 × 5 × 0.9 mm, 40-VFQFPN | -40° to +85°C |
| RC31008BdddGND#KB0 [2] | | | Tape and Reel | | |
| RC31012BdddGNA#BB0 [2] | | 12 | Tray | 6 × 6 × 0.9 mm, 48-VFQFPN | |
| RC31012BdddGNA#KB0 [2] | | | Tape and Reel | | |
| RC31005BQ00GL2#BB0 | Un-programmed part with internal crystal. I2C address is 0x09. | 5 | Tray | 4 × 4 × 1.0 mm, 32-LGA | -40° to +85°C |
| RC31005BQ00GL2#KB0 | | | Tape and Reel | | |
| RC31008BQ00GL2#BD0 | | 8 | Tray | 5 × 5 × 1.7 mm, 40-LGA | |
| RC31008BQ00GL2#KD0 | | | Tape and Reel | | |
| RC31012BQ00GL3#BB0 | | 12 | Tray | 6 × 6 × 0.9 mm, 48-LGA | |
| RC31012BQ00GL3#KB0 | | | Tape and Reel | | |
| RC31005BQ01GL2#BB0 | Un-programmed part with internal crystal for use with external I2C EEPROM.<br>I2C address is 0x09 after I2C EEPROM is loaded. | 5 | Tray | 4 × 4 × 1.0 mm, 32-LGA | -40° to +85°C |
| RC31005BQ01GL2#KB0 | | | Tape and Reel | | |
| RC31008BQ01GL2#BD0 | | 8 | Tray | 5 × 5 × 1.7 mm, 40-LGA | |
| RC31008BQ01GL2#KD0 | | | Tape and Reel | | |
| RC31012BQ01GL3#BB0 | | 12 | Tray | 6 × 6 × 0.9 mm, 48-LGA | |
| RC31012BQ01GL3#KB0 | | | Tape and Reel | | |
| RC31005BQddGL2#BB0 [2] | Preprogrammed part with internal crystal. | 5 | Tray | 4 × 4 × 1.0 mm, 32-LGA | -40° to +85°C |
| RC31005BQddGL2#KB0 [2] | | | Tape and Reel | | |
| RC31008BQddGL2#BD0 [2] | | 8 | Tray | 5 × 5 × 1.7 mm, 40-LGA | |
| RC31008BQddGL2#KD0 [2] | | | Tape and Reel | | |
| RC31012BQddGL3#BB0 [2] | | 12 | Tray | 6 × 6 × 0.9 mm, 48-LGA | |
| RC31012BQddGL3#KB0 [2] | | | Tape and Reel | | |

1. Tape and Reel pin 1 orientation follows EIA-481-D unless noted.
2. Replace “ddd” or “dd” with the preprogrammed configuration code provided by Renesas in response to a custom configuration request.

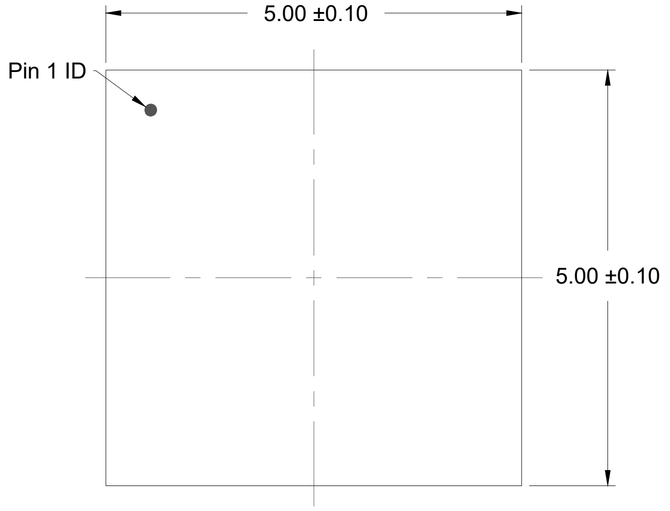
# 9. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.18 | Jun 24, 2024 | ▪ Updated the output duty cycle in Table 27 and Table 28. |
| 1.17 | Jun 4, 2024 | ▪ Updated the packaging information for the 32-LGA package in Ordering Information. |
| 1.16 | May 1, 2024 | ▪ Added Table 35 (CLKIN Differential Electrical Characteristics). |
| 1.15 | Apr 5, 2024 | ▪ Updated the Configuration and OTP bullets in Features.<br>▪ Added cross-references in Table 1, Table 2, Table 3, Table 4, and Table 5 to Table 8. |
| 1.14 | Mar 13, 2024 | ▪ Updated several part numbers in Ordering Information (RC31012BQ00GL3#BB0, RC31012BQ00GL3#KB0, RC31012BQ01GL3#BB0, and RC31012BQ01GL3#KB0). |
| 1.13 | Feb 15, 2024 | ▪ Added the internal crystal RC31005BQ, RC31008BQ and RC31012BQ information to the datasheet.<br>▪ Added BQ orderable part numbers to Ordering Information.<br>▪ Rearranged Ordering Information for readability.<br>▪ Completed other minor changes. |
| 1.12 | Jan 11, 2024 | ▪ Updated the typical and maximum values for $t_{\Phi APLL}$ in Table 23.<br>▪ Updated the document to the latest template. |
| 1.11 | Dec 21, 2023 | ▪ Updated Static Phase Offset - Zero Delay Buffer Mode table with characterized values.<br>▪ Moved to final data sheet for RC31012B and RC31008B. |
| 1.10 | Nov 10, 2023 | ▪ Corrected two package links in Ordering Information. |
| 1.09 | Oct 30, 2023 | ▪ Updated the down-spread maximum value in Table 34.<br>▪ Introduced a new document number for the datasheet. |
| 1.08 | May 31, 2023 | ▪ Changed $t_{HOLD}$ to 200uS from 200mS in Figure 13. |
| 1.07 | May 8, 2023 | ▪ Updated the device block diagram in Figure 2. |
| 1.06 | Apr 14, 2023 | ▪ Corrected an RC31005BQ part number in Ordering Information. |
| 1.05 | Mar 29, 2023 | ▪ Updated document for B-rev as follows:<br>• Updated front page references to B-rev and simplified the block diagram.<br>• Added RC31012BQ pin out and pin descriptions.<br>• Added RC11005BQ pin out and pin descriptions.<br>• Updated ordering information with new devices and revisions.<br>• Changed ePad outline and ePad text in the Pin Diagrams to grey color to highlight that the view is Top View and the ePad is on the bottom of the package.<br>• Added thermal data for 005BQ and 012BQ package.<br>• Corrected all theta ja descriptions from 0, 1, 3, and 5 m/s airflow to 0, 1, 2, and 3 m/s airflow.<br>▪ Updated Power Considerations for the B-rev silicon.<br>▪ Added Static Phase Offset - Zero Delay Buffer Mode specification. |
| 1.04 | Nov 23, 2022 | ▪ Added LVCMOS AC/DC characteristics tables (see Table 24 to Table 26).<br>▪ Completed an extensive update to Power Considerations, specifically power sequencing considerations.<br>▪ Clarified Overdriving the XTAL Interface. |

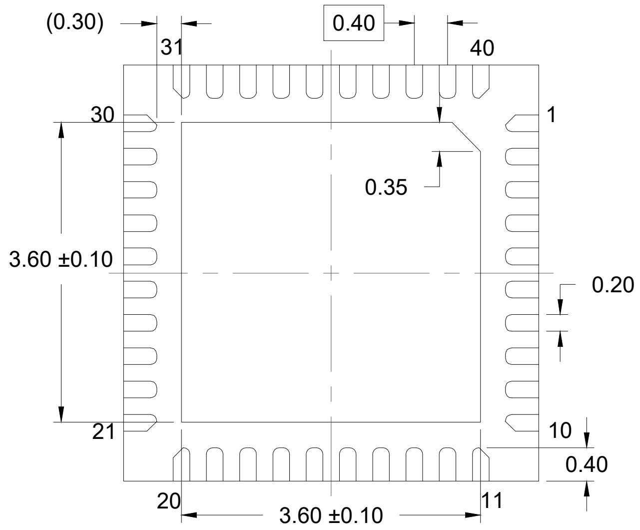
| Revision | Date | Description |
|---|---|---|
| 1.03 | Oct 7, 2022 | ▪ Changed the minimum value for $t_{PU}$ in Table 8.<br>▪ Revised the condition for $t_{HS}$ in Table 15.<br>▪ Updated Power Sequencing Considerations.<br>▪ Updated the Marking Diagrams and Ordering Information, added 01 and 001 dash codes to indicate configurations that load from external $I^2C$ EEPROMs. Also updated the table footnotes accordingly.<br>▪ Removed references to RC31005A pending final qualification. For the latest documentation on this device, please contact Renesas.<br>▪ Completed other minor changes. |
| 1.02 | Sep 6, 2022 | ▪ Completed minor updates to various Electrical Characteristics values. |
| 1.01 | Aug 9, 2022 | ▪ Corrected a typo in Pin Assignments – RCxx012A.<br>▪ Completed minor updates to various values in Electrical Characteristics.<br>▪ Completed other minor changes. |
| 1.00 | Jul 25, 2022 | Initial release. |

# Package Outline Drawing

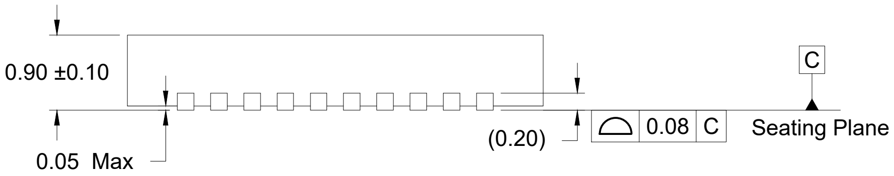
Package Code:NDG40P3
40-VFQFPN 5.0 x 5.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4292-03, Revision: 02, Date Created: Aug 30, 2022



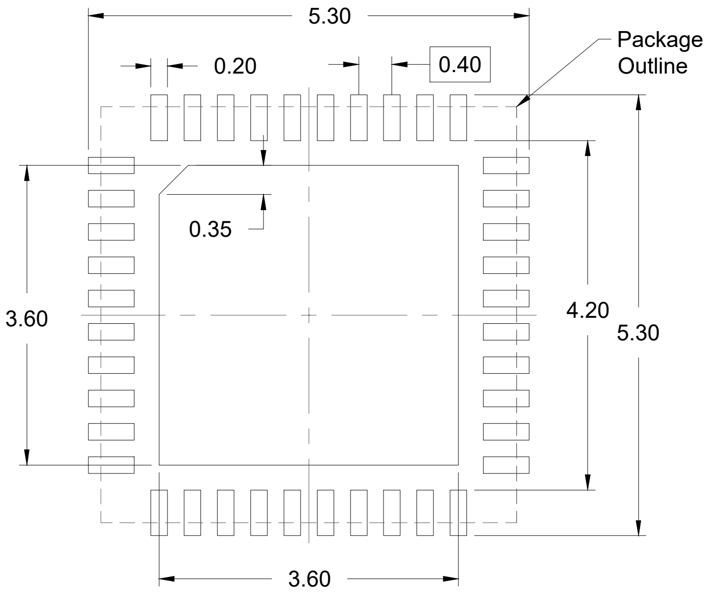
TOP VIEW



BOTTOM VIEW



SIDE VIEW



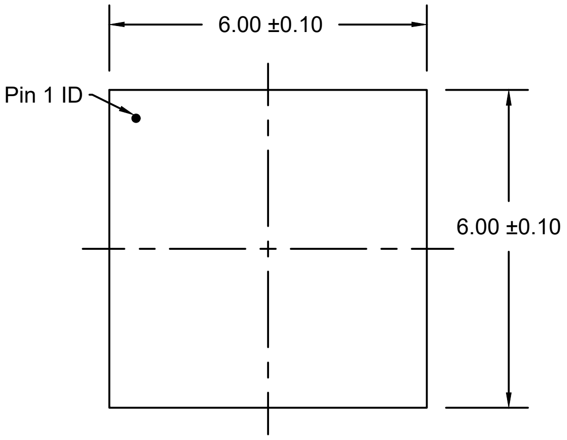
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

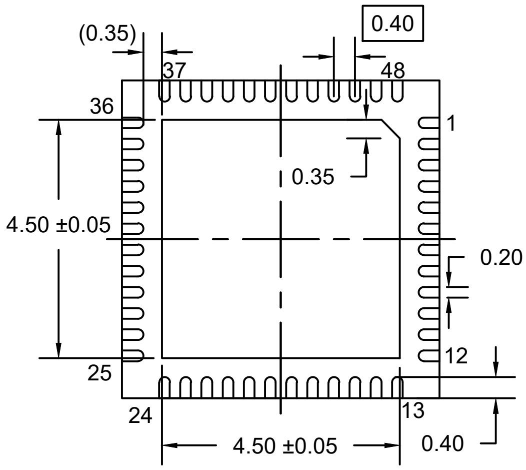
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

# Package Outline Drawing

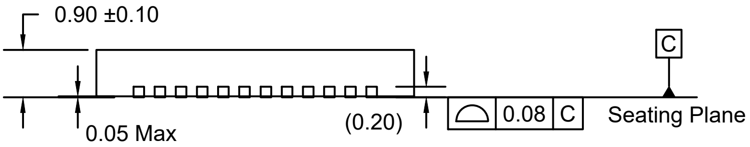
Package Code: NDG48P4
48-VFQFPN 6.0 x 6.0 x 0.9 mm Body, 0.4 mm Pitch
PSC-4212-05, Revision: 01, Date Created: Oct 18, 2022



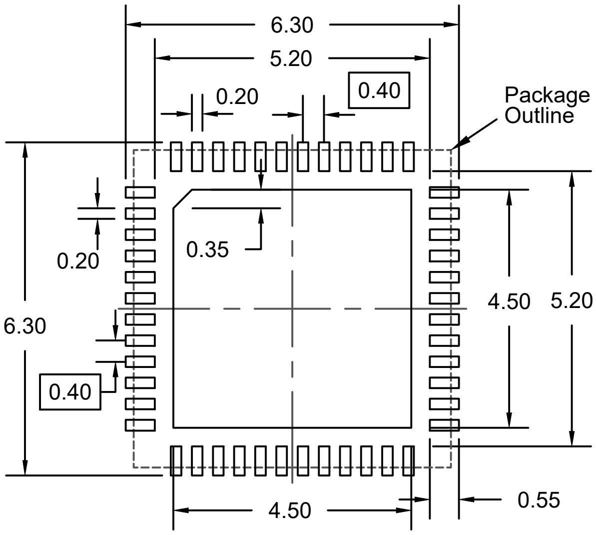
TOP VIEW



BOTTOM VIEW



SIDE VIEW



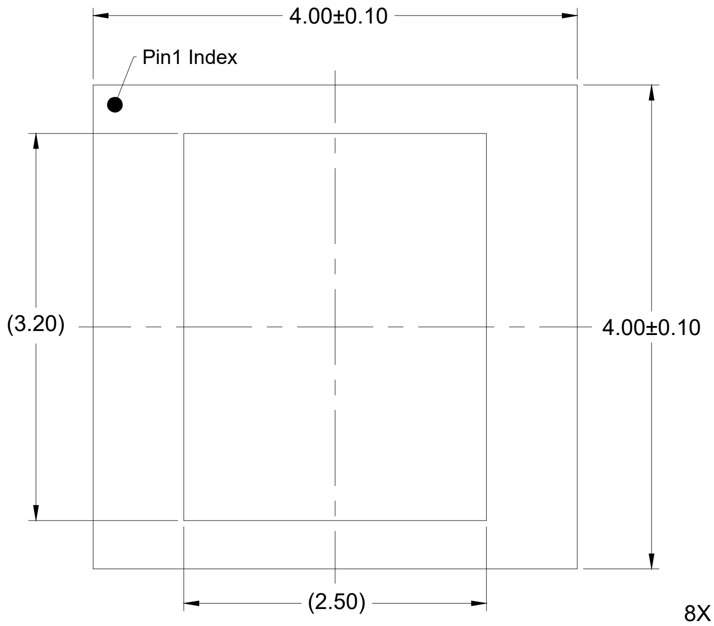
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

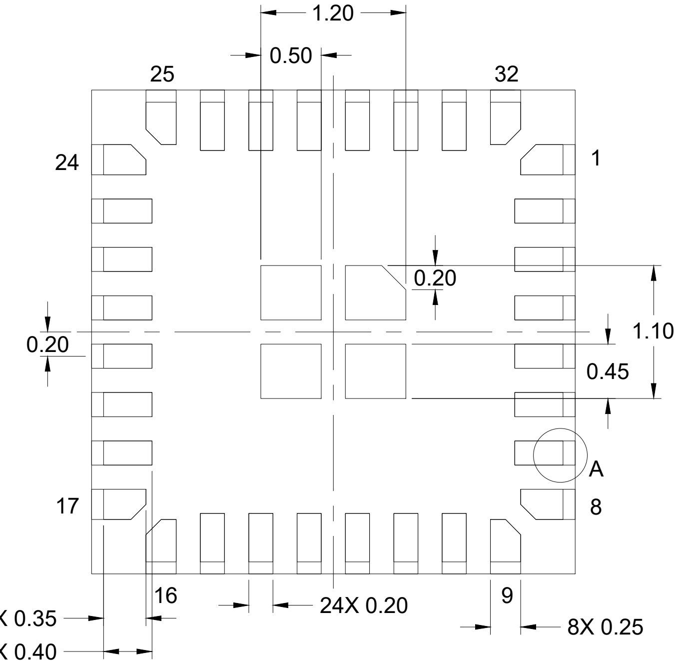
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.50 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

# Package Outline Drawing

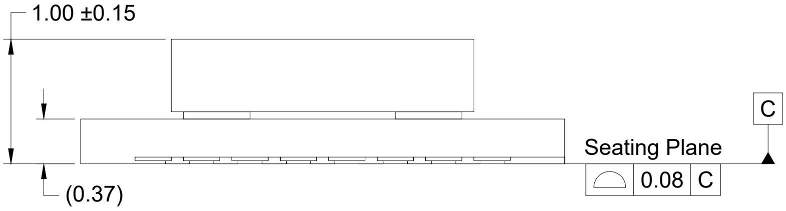
Package Code: LTW32D2
32-LGA 4.0 x 4.0 x 1.00 mm Body, 0.4mm Pitch
PSC-4889-02, Revision: 01, Date Created: May 26, 2023



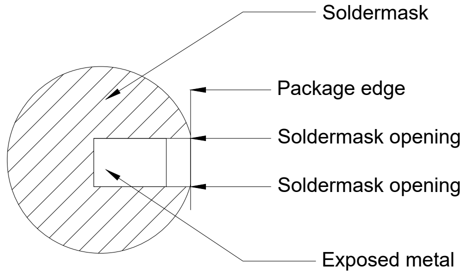
TOP VIEW



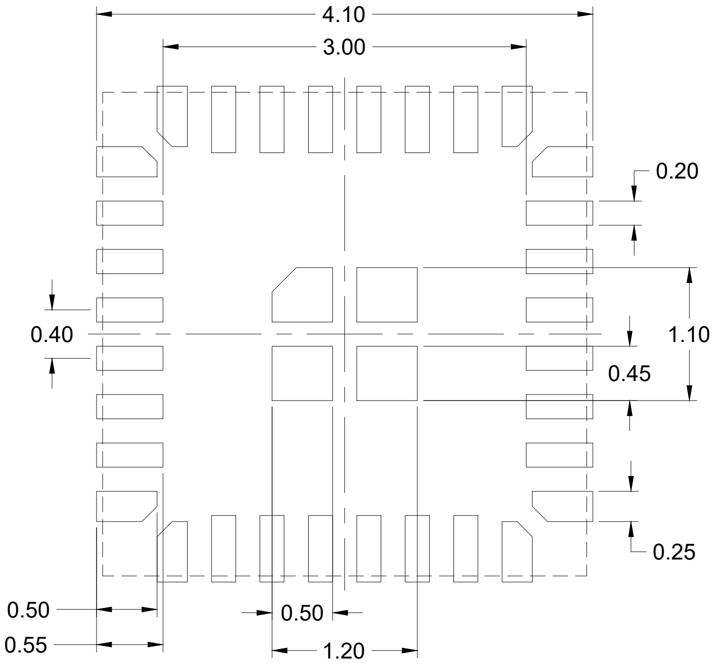
BOTTOM VIEW



SIDE VIEW



Detail A



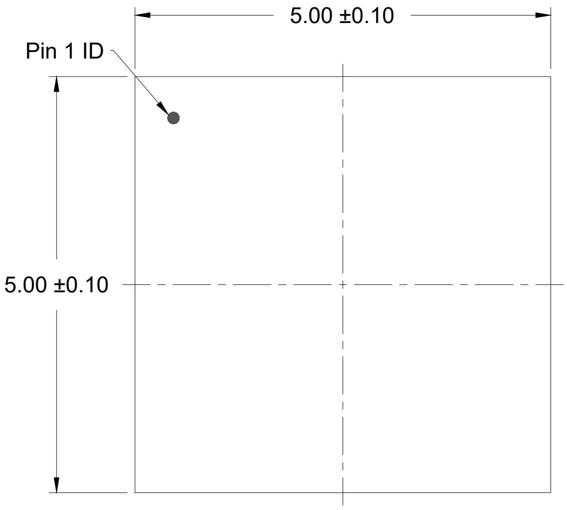
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

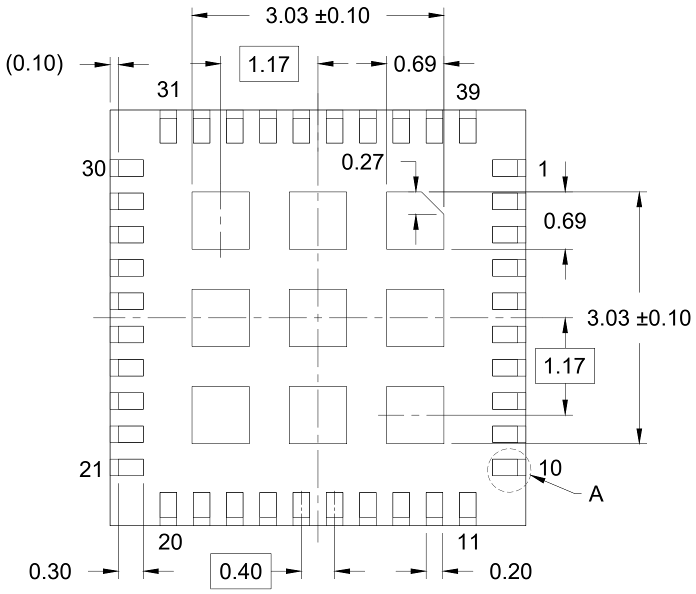
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for reference only.

# Package Outline Drawing

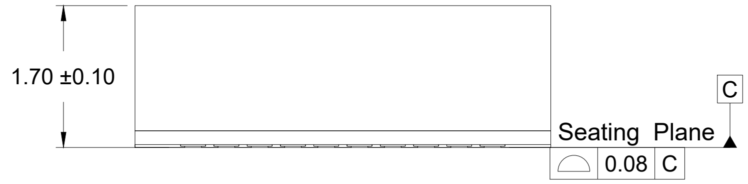
Package Code: LTG40D1
40-LGA 5.0 x 5.0 x 1.70 mm Body, 0.40 mm Pitch
PSC-4864-01, Revision: 03, Date Created: May 26, 2023



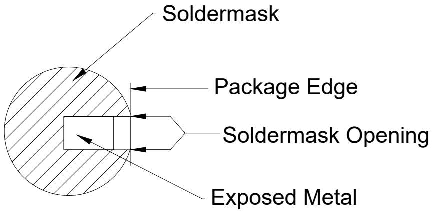
TOP VIEW



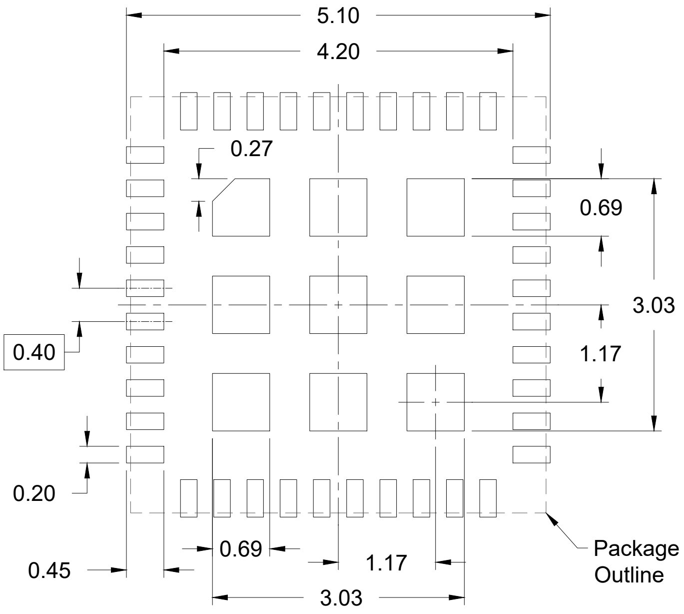
BOTTOM VIEW



SIDE VIEW



Detail A



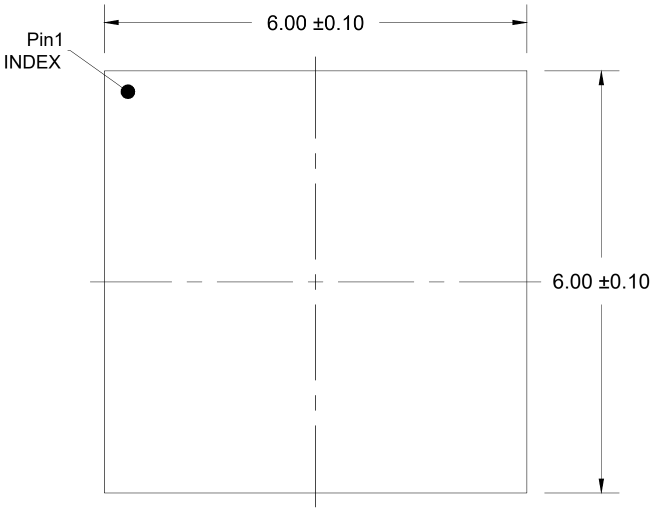
RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

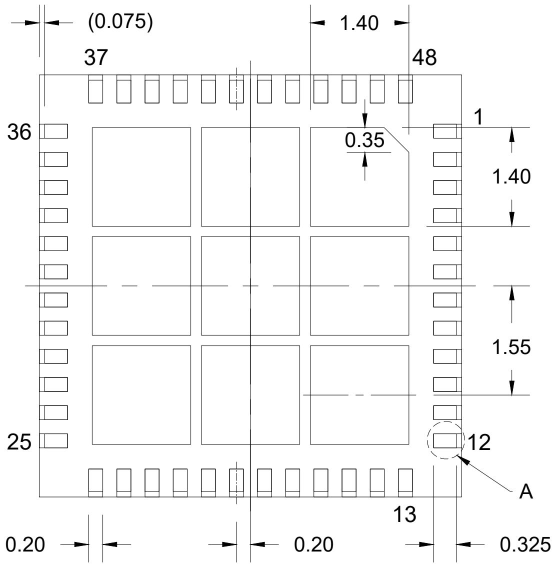
1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

# Package Outline Drawing

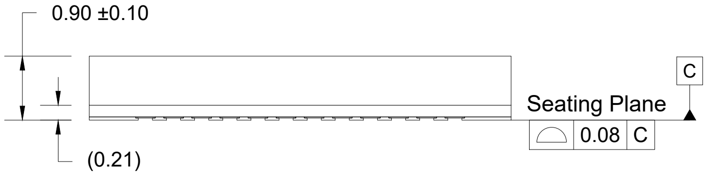
Package Code: LGV48D1
48-LGA 6.0 x 6.0 x 0.90 mm Body, 0.4mm Pitch
PSC-4943-01, Revision: 02, Date Created: May 26, 2023



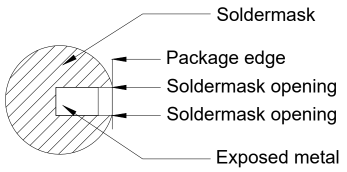
TOP VIEW



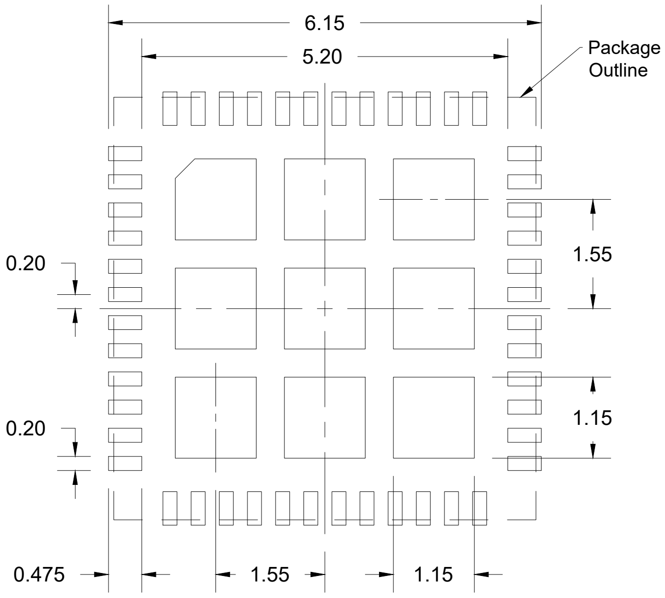
BOTTOM VIEW



SIDE VIEW



Detail A



(PCB Top View)
(Lead pad - NSMD Design; Thermal pad - SMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for reference only.

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

© 2025 Renesas Electronics Corporation. All rights reserved.