RH4Z2501 Datasheet

IO-Link transceiver with integrated protection

The RH4Z2501 is a line driver/level shifter IC for IO-Link communication with integrated protection. It addresses the IO-Link device physical layer for sensors and actuator systems. The IC can also be used as single channel master.

For device configuration and status reading, an OWI communication interface is available.

The output drivers allow push-pull operation, with a maximum R_{DSON} of less than 2.5Ω for all operational temperatures.

The RH4Z2501 is designed in a powerful CMOS mixed-signal technology that allows short supply voltage peaks up to 60V.

Applications

The RH4Z2501 acts as a universal cable driver.

The RH4Z2501 can support IO-Link communications as a physical-layer transceiver (PHY) for IO-Link devices and IO-Link masters.

- 24V line driver/level shifter.
- IO-Link-compliant devices.
- IO-Link-compliant masters.

Features

- Voltage supply range from 9V to 36V.
- Over-voltage peak robustness of ±60V.
- Configurable driver output current 50mADC to 400mADC.
- R_{DSON} of less than 2.5Ω.
- Adjustable driver slew rate.
- Integrated Wake-up detection.
- MCU assisted Wake-up generation (typ. 700mA).
- OWI digital communication and calibration interface.
- Integrated Linear Voltage Regulators 3.3V and 5V.
- Ambient Temperature range -40°C to 125°C.
- Glitch filter for receiver.
- Integrated protection:
  - ±1.25kV/2.5A (peak) surge protection for L+, CQ, GND/L- (8/20 µs pulse acc. IEC 61000-4-5).
  - Reverse polarity protection for L+, CQ, GND/L-
- On-chip diagnostics:
  - Over temperature detection.
  - Supply voltage monitor.
  - Broken chip detection.

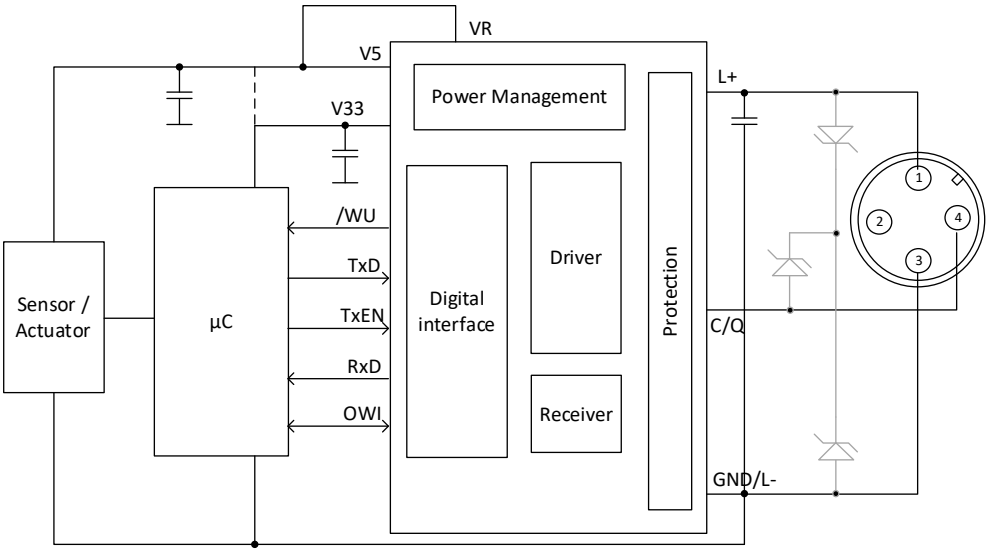

Figure 1. Typical Application Diagram

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1. Overview

1.1 Block Diagram

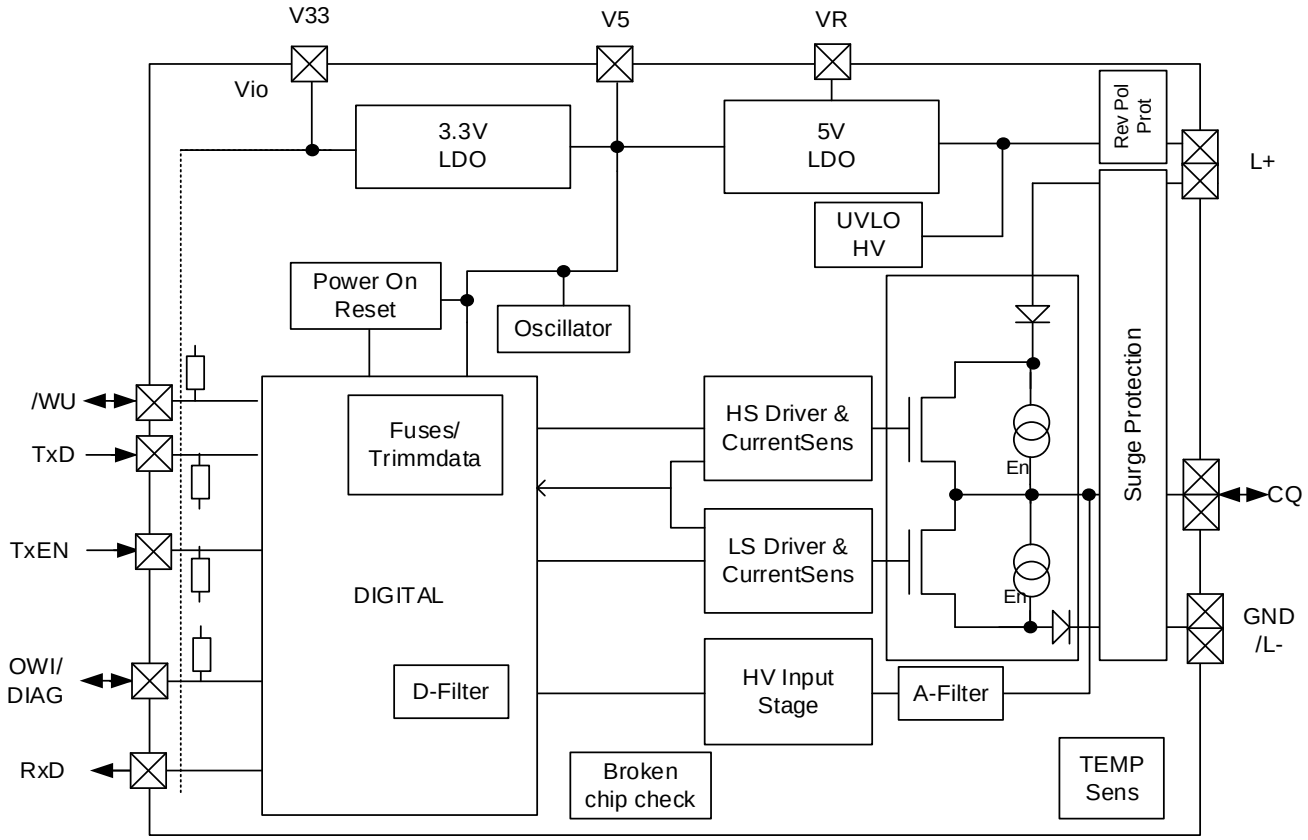

Figure 2. Block Diagram

1.2 Ordering Information

Table 1. Part Number Description

Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
RH4Z2501BJ3GNM#HD0	3mm × 3mm DFN12	MSL1	Tape & Reel	-40°C to 125°C
RH4Z2501BJ3GNM#HD1	3mm × 3mm DFN12 with Surge Protection disabled by default	MSL1	Tape & Reel	-40°C to 125°C
RH4Z2501BJ8GBM#HD0	Wafer Level Chip Scale Package	MSL1	Tape & Reel	-40°C to 125°C
RH4Z2501BJ8GBM#HD1	Wafer Level Chip Scale Package with Surge Protection disabled by default	MSL1	Tape & Reel	-40°C to 125°C

1.3 Pin Configuration

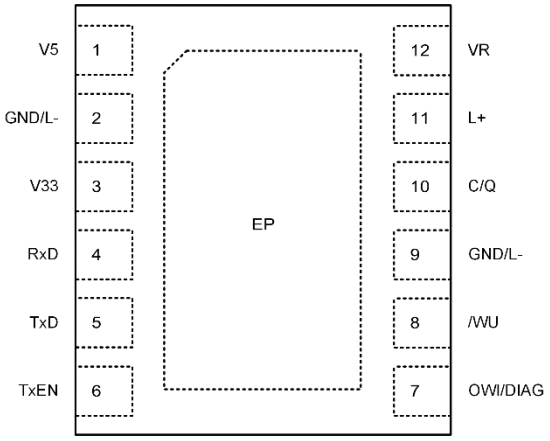

Figure 3. DFN 12 Pin Layout (Top View)

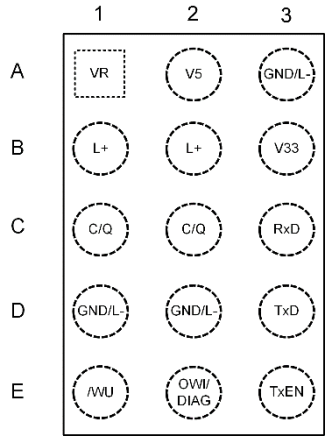

Figure 4: WCSP15 Pin Layout (Top View)

1.4 Pin Description

Table 2. Pin Description

PIN		Name	Type	Function
DFN12	WLCSP15			
1	A2	V5	5V Power supply input/output	5V must be present for normal operation. Add a 1µF blocking capacitor on this pin to GND, see section 3.1 for details.
2, 9	A3, D1, D2	GND/L-	Ground	Ground pins, all GND pins must be connected.
3	B3	V33	3V3 Power supply output	Defines the logic level of the pins, for a 5V logic level, connect this pin to 5V. Add a 1µF blocking capacitor on this pin to GND.
4	C3	RxD	Digital output	C/Q receiver output (the default RxD is inverse of C/Q).
5	D3	TxD	Digital input	C/Q driver logic level (the default C/Q output level is inverse of TxD).
6	E3	TxEN	Digital input	C/Q driver enable input. Drive TxEN high to enable C/Q driver.
7	E2	OWI/DIAG	Digital input/output Internal pull-up	Communication pin used for the One Wire and the Diagnostic interfaces.
8	E1	/WU	Digital input/output Internal pull-up	The default is Wake Up indication output (master configuration: high current selection input).
10	C1, C2	C/Q	Analog input/output	C/Q transceiver input/output. RxD logic level is by default the opposite of C/Q. When TxEN is high, the output driver is enabled. The logic level is by default the opposite of TxD.
11	B1, B2	L+	Supply voltage	Power supply using a 100nF capacitor as close as possible to the pad. The pin is typically connected to the IO-link supply voltage.
12	A1	VR	Analog output	Regulator output. See section 3.1 for possible configurations.
		EP	Exposed Pad	DFN-bottom plate: Recommendation is to connect to GND/L-, Pad to be used for heat dissipation and additional EMC robustness.

1.5 Absolute Maximum Ratings

Table 3. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum[1]	Units
T_J	Junction temperature		-40	175	°C
T_S	Storage temperature		-40	150	°C
	Latch-up	Tested per JESD78E; Class 2, Level A	-100	100	mA
V_{L+_MAX}	Maximum allowed for voltage supply	Continuous	-36	36	V
		100µs peak duration	-60	60	V
V_{CQ}		Continuous	-36	36	V
		100µs peak duration	-60	60	V
V_{SUP_MAX}	Voltage at supply pins	V5, V33	-0.3	6	V
V_{IF_MAX}	Voltage at digital interface pins	RxD, TxD, /WU, OWI	-0.3	V33+0.3	V
V_{VR_MAX}	Voltage at VR pin			20	V
	Continuous Power Dissipation	DFN12 (de-rate above 70°C with 24.1mW/°C)		1931	mW
	Continuous Power Dissipation	WLCSP (de-rate above 70°C with 20.2mW/°C)		1614	mW

1. CAUTION: Do not operate at or near the maximum ratings for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

1.6 Thermal Information

Table 4. θJA According to Package

Thermal Resistance (Typical)	θ_{JA} (°C/W)
12Ld 3×3 DFN Package[1, 2]	41.5
WLCSP 15 Package [1, 3]	50

1. θ_{JA} is simulated under 125°C ambient temperature in free air with the component mounted on a high-effective thermal conductivity test board. Used standard is JESD51-2A.
2. 3×2 thermal vias configuration used.
3. 3×5 thermal micro vias configuration used (one under each solder ball).

1.7 Recommended Operating Conditions

Table 5. Recommended Operating Conditions

Symbol	Parameter	Minimum	Typical	Maximum	Units
L+	Power supply voltage	9	–	36	V
T_A	Ambient temperature	-40	–	125	°C
T_J	Junction temperature	-40		150	°C
V5		4.5		5.5	V
V33		Internally regulated 3.3V		5.5	V

1.8 Electrical Specifications

The following electrical specifications are valid for the recommended operating conditions as specified in Table 5 unless otherwise noted.

Table 6. Electrical Specification

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
IC Supply						
	Under-voltage shutdown	L+ rising		8.0	9	V
		L+ falling	7	7.9		V
		Hysteresis		0.1		V
	Under-voltage warning	L+ rising		16.3	18	V
		L+ falling	14	15.6		V
		Hysteresis		0.8		V
	Over-voltage warning	L+ rising	30	32.3		V
		L+ falling		33.1	36	V
		Hysteresis		0.8		V
	L+ quiescent supply current	V5 = VR, Driver disabled		1.2	1.65	mA
		V5 = VR, Push Pull		1.8	2.5	mA
	V5 supply current	Driver disabled		0,85		mA
		Push Pull		1,4		mA
	V5 under-voltage (Power-on Reset)	V5 rising (reset release)	3.0	3.65	4.0	V
		V5 falling (reset assert)	3.0	3.8	4.0	V
		Hysteresis	0.1	0.17		V
	V5 supply voltage		4.5	5.0	5.5	V
	V33 supply voltage		3.0	3.3	3.6	V
5V Linear Regulator						
V5	Regulator output		4.75	5	5.25	V
	Load regulation	L+ = 24V, 1mA < IL < 50mA			2	%
	Line regulation	9V…36V IL = 1mA			4	mV/V
PSRR	Power supply rejection ratio	F = 100kHz, IL = 20mA		-65		dB
	Capacitance	External required capacitance		1		µF
3.3V Linear Regulator						
	Regulator output		3.13	3.3	3.47	V
	Load regulation	1mA < IL < 50mA			1	%
PSRR	Power supply rejection ratio			-65		dB
	Capacitance	External required capacitance		1		µF
C/Q Driver						
R_{OH}	C/Q driver on resistance	High side enabled I_{LOAD} = -200mA		1	2.5	Ω
R_{OL}		Low side enabled I_{LOAD} = 200mA				
	C/Q load current	Programmable	50		400	mA
	C/Q load current limitation	Internally actively limited	100[1]		135%	%
	Overload detection	Overload detection before current limiting		-10		%
	Slew rate	Programmable	20		140	V/µs
T_{PLH}, T_{PHL}	Driver propagation delay	C_L 3nF, 18V to 36V, 120V/µs, 200mA, push pull/PNP mode		450	750	ns
T_{SKEW}	Driver propagation delay skew	T_{PLH}-T_{PHL}		50		ns
	Difference of rise and fall time	T_{RISE}-T_{FALL}		20		ns
T_{PZH}, T_{PZL}	Driver enable delay	C_L = 3nF, R_L = 2kΩ, 18..36V, 120V/µs, 200mA		450	750	ns
T_{PHZ}, T_{PLZ}	Driver disable delay	C_L = 3nF, R_L = 2kΩ, 18..36V, 120V/µs, 200mA			4	µs
	C/Q input resistance			950		kΩ
	Weak pull-up current			0.5	1	mA
	Weak pull-down current			0.5	1	mA
	Master current sink	Programmable 3mA, 6mA, 9mA, V_{CQ} > 5V	-10		20	%

[1] For the 50mA range the lower limit is 90%

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
C/Q Receiver						
V_{IN}	Input voltage range		V_{L+}-36V		36V	V
V_{TH}	Input high threshold	L+ >= 18V	11	11.8	12.5	V
		L+ < 18V	60	72	80	% of L+
V_{TL}	Input low threshold	L+ >= 18V	9	9.8	10.5	V
		L+ < 18V	50	60	68	% of L+
V_{HYST}	Input hysteresis	L+ >= 18V		2		V
		L+ < 18V		12		% of L+
	Input capacitance	Driver disabled f = 100kHz		200		pF
	L-H propagation delay	AFilter = 0, DFilter = off		180	300	ns
		AFilter = 1, DFilter = off		570	1000	ns
	H-L propagation delay	AFilter = 0, DFilter = off		250	400	ns
		AFilter = 1, DFilter = off		690	1000	ns
	Receiver skew	AFilter = 0, DFilter = off		50		ns
		AFilter = 1, DFilter = off		100		ns
/WU Detection						
T_{WU_MIN}	Wake-up min pulse width	C_{LOAD} = 3nF	45		75	µs
T_{WU_MAX}	Wake-up max pulse width	C_{LOAD} = 3nF	85		115	µs
Thermal Management						
	Thermal shutdown	Temperature rising		165		°C
		Temperature falling		150		°C
	Thermal warning	Temperature rising		140		°C
		Temperature falling		125		°C
Pads						
V_{IO}	IO-Voltage		2.97	3.3	5.5	V
V_{IL}	Logic input voltage low	TxEN, TxD, /WU, OWI			0.25×V_{IO}	V
V_{IH}	Logic input voltage high	TxEN, TxD, /WU, OWI	0.75×V_{IO}			V
R_{PD_Tx}	Input leakage	TxEN, TxD	70	100	130	kΩ
V_{OL}	Output voltage low	I_{OUT} = -4mA (RxD, /WU)			0.4	V
V_{OH}	Output voltage high	I_{OUT} = 4mA (RxD)	V_{IO}-0.6			V
R_{PU_WU}	Pull-up resistance	/WU pad	5		10	kΩ
V_{OL}	Output voltage low	I_{OUT} = -1.5 mA (OWI)			0.6	V
R_{PU_OWI}	Pull-up resistance	OWI	10	15	20	kΩ
I_{Max_OWI}	Max output current	OWI	2		6	mA
OWI timing						
t_{OWI_START}	Minimum T_{LOW} time to detect a start condition		4			µs
t_{OWI_BIT}	OWI bit time		15		11114	µs
t_{OWI_0}	Duty ratio bit '0'		0.125	0.25	0.375	t_{OWI_BIT}
t_{OWI_1}	Duty ratio bit '1'		0.625	0.75	0.875	t_{OWI_BIT}
t_{OWI_STOP}	Hold time STOP condition	$t_{OWI\_BIT\_L}$ is the bit period of the last valid bit	3	250		$t_{OWI\_BIT\_L}$
$t_{OWI\_BIT\_DEV}$	Bit time deviation	Duration of most recent bit versus previous bit duration	0.5	1.0	2.0	t_{OWI_BIT}
ESD tolerance						
	ESD protection (L+, CQ)	IEC-61000-4-2- contact discharge		+/-4		kV
		HBM (Human Body Model)		+/-4		kV
	ESD protection all pins	HBM (Human Body Model)		+/-2		kV
		CDM (Charged Device Model)		+/-750		V
	Surge protection (L+, CQ, GND)	IEC 61000-4-5, 500Ω, 8/20µs surge		+/-1.25		kV

1. All devices 100% production tested at TA = +25ºC. Limits over operating temperature range are guaranteed by design.
2. Currents out of the device are negative. Currents into the device are positive.
3. Not production tested. Guaranteed by design.

2. Typical Performance Curves

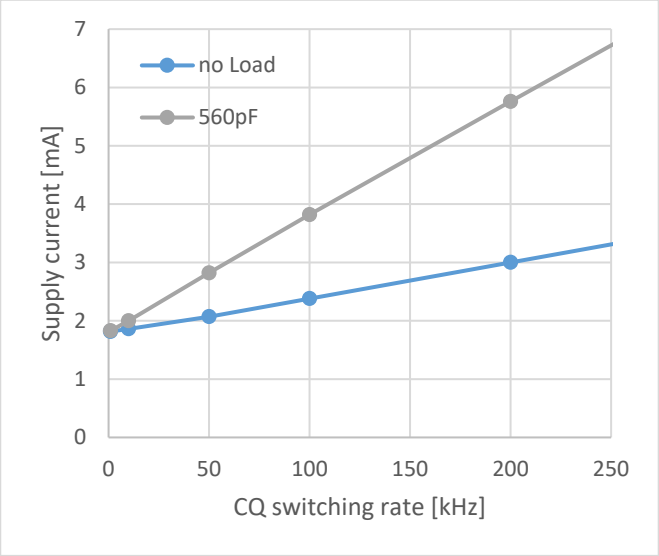

Figure 5. Current Consumption vs. Switching Rate

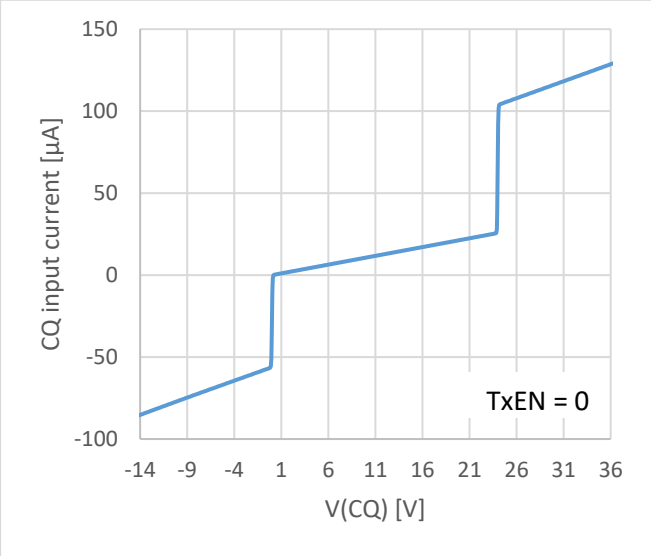

Figure 6. C/Q Input Current Driver Disabled

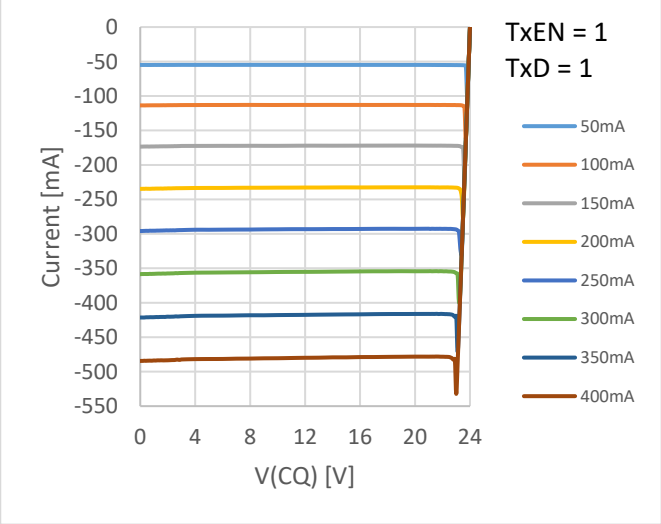

Figure 7. C/Q Driver High Side Current vs. V(CQ)

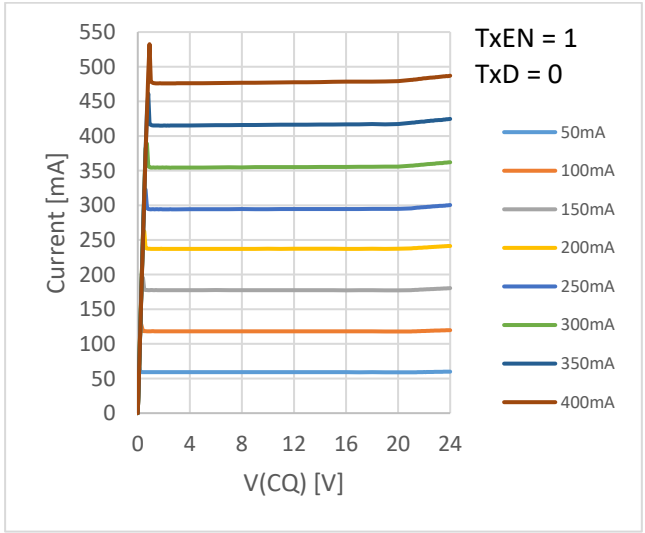

Figure 8. C/Q Driver Low Side Current vs. V(CQ)

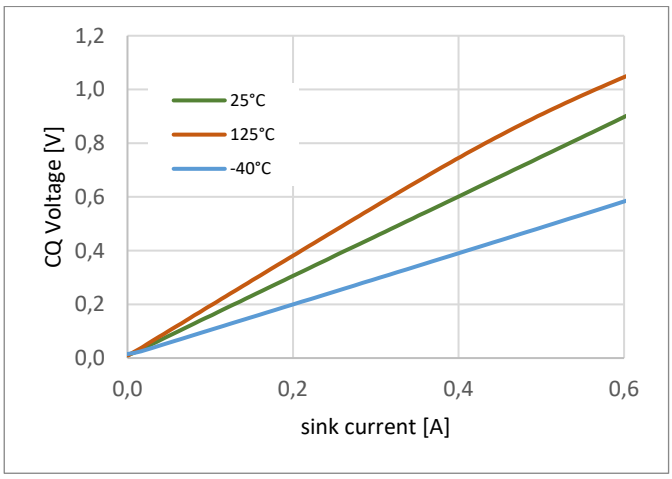

Figure 9. C/Q Driver Low Voltage vs. Sink Current

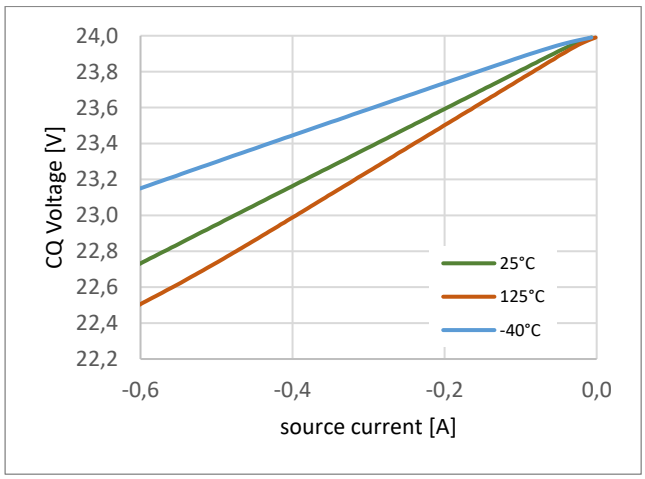

Figure 10. C/Q Driver High Voltage vs. Source Current

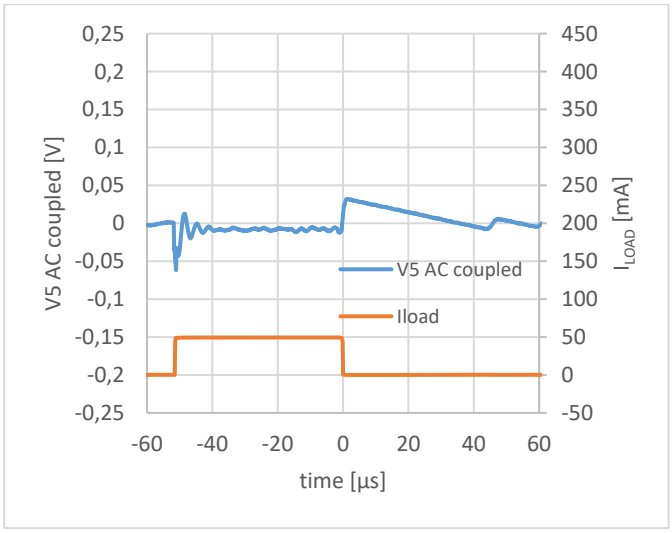

Figure 11. V5 LDO Transient Load Response

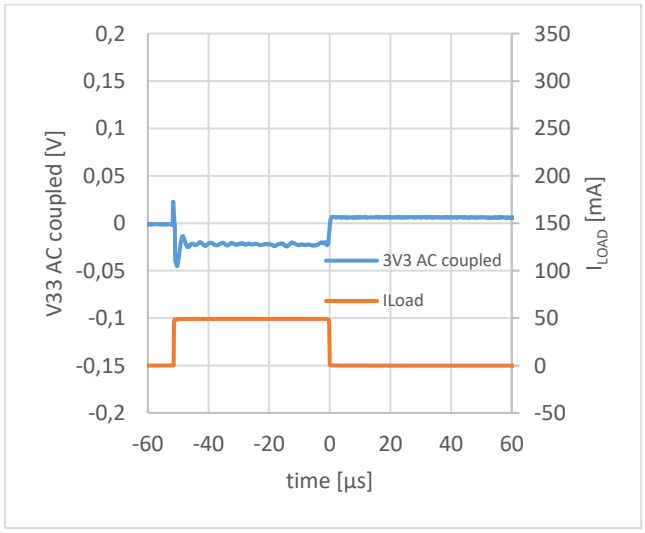

Figure 12. V33 LDO Transient Load Response

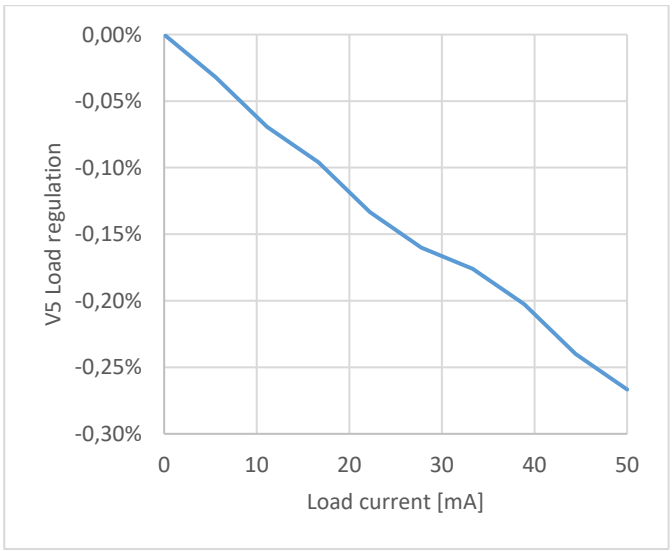

Figure 13. V5 Load Regulation

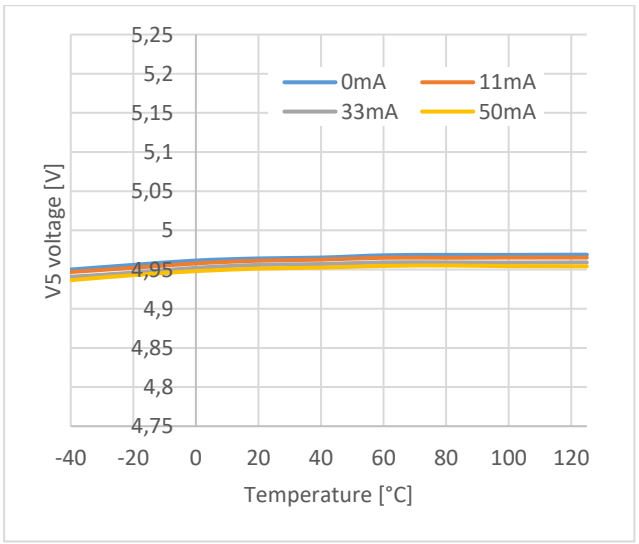

Figure 14. V5 Output Voltage vs. Temperature

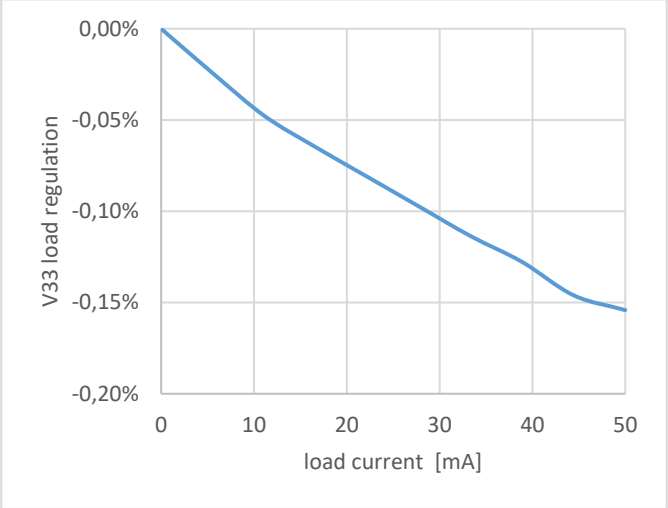

Figure 15. V33 Load Regulation

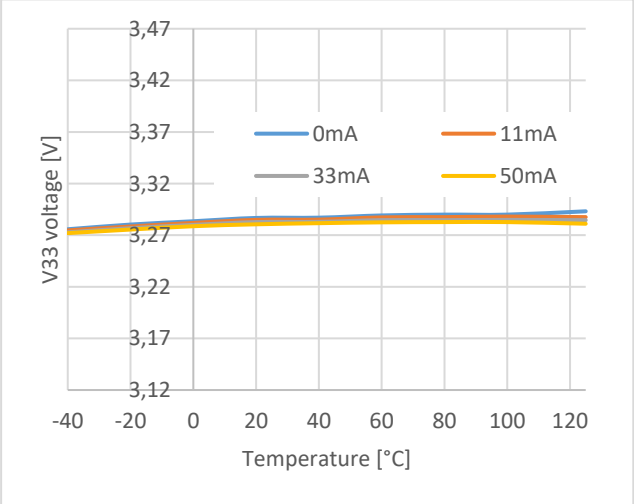

Figure 16. V33 Output Voltage vs. Temperature

3. Detailed Description

3.1 Linear Regulators

There are different configuration options to generate the 5V supply.

3.1.1. Internal 5V Linear Regulator

The device is equipped with two internal LDOs that are able to generate both 5V and 3.3V rails.

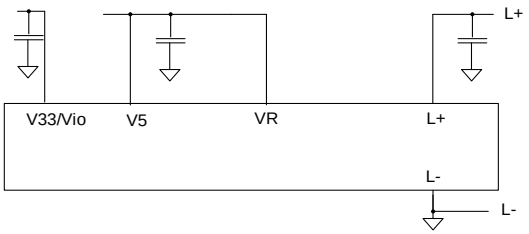

Figure 17. Internal V5 LDO

Connecting the internal regulator output (VR pin) and the 5V pin generates the 5V supply using the internal low drop-out regulator. It can provide up to 50mA current. When higher currents are required either use an NPN transistor or an external converter. Consider the LDO power dissipation for optimal thermal performance, see section 3.1.5.

3.1.2. Using an External NPN Transistor

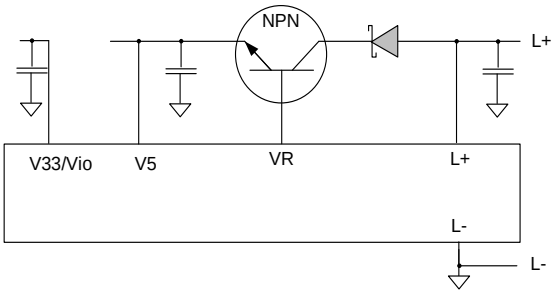

Figure 18. External NPN Transistor

Using an external NPN transistor improves thermal performance of the device allowing a higher current supply. Make sure to place a diode on the collector of the NPN transistor to ensure the reverse polarity protection.

3.1.3. Using an External Step-Down Regulator

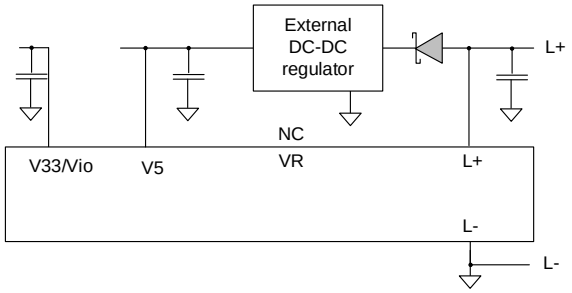

Figure 19. External DC-DC Regulator

3.1.4. 3.3V Regulator (IO Voltage)

The 3.3V regulator defines the logic level. Connect the V33 pin with the V5 pin to operate at 5V logic levels.

3.1.5. Thermal Considerations

When using internal supply capabilities of the PHY, the internal LDOs and the driver can generate more power than the package for the device can safely dissipate. It is important to ensure that the driver and LDO loading is smaller than the package can dissipate.

Total power dissipation for the device is calculated using the equations displayed in Table 7.

Table 7. Power Dissipation Equations

Equation	Description
$P_{CQ} = I_{CQ(max)}^2 \times R_{on}$	P_{CQ} is the power generated in the C/Q driver.
$P_{V5} = (V_{L+} - 5V) \times I_{V5}$	P_{V5} is the power generated by the 5V LDO.
$P_{V33} = 1.7V \times I_{V33}$	P_{V33} is the power generated by the 3.3V LDO.
$P_{Dev} = V_{L+(max)} \times I_{L+(max)}$	P_{Dev} is the power consumed by the device without driver and LDOs but including switching current consumption.
$P_{PD/PU} = V_{CQ(max)} \times I_{PD(max)}$ or $(V_{L+} - V_{CQ})_{(max)} \times I_{PU(max)}$	$P_{PU/PD}$ is the power generated by C/Q pull-up/pull-down current source/sink.
$P_{TOTAL} = P_{CQ} + P_{V5} + P_{V33} + P_{Dev} + P_{PU/PD}$	P_{TOTAL} is the sum of the above calculated powers.

3.2 C/Q Driver

3.2.1. Driver Enable/Disable

The C/Q driver is enabled when TxEN is set to ‘High’ and disabled when it is set to ‘Low’.

Table 8 lists the C/Q driver output modes according to TxEN and TxD signals.

Table 8. C/Q Driver Output Modes

TXEN	TXD	C/Q Output			
		OFF	NPN Mode	PNP Mode	Push-Pull Mode
L	X	Z	Z	Z	Z
H	L	Z	Z	H	H
H	H	Z	L	Z	L

1. X = Not to be considered, Z = High impedance; H = High, L = Low

3.2.2. Overcurrent Protection

The C/Q driver can sense an overload condition. If an overload situation occurs (either high side or low side drivers) and remains for longer than the blanking time (“blankTim”), a driver fault condition is detected, resulting in overload (“overLoad") and interrupt (“overLoadInt”) status bits being set.

If the auto-retry bit (“autoRetryEn”**)** is enabled (default):

- The C/Q driver is disabled for the duration of the auto-retry off time (“autoRetryTim”). After this time, the driver is automatically re-enabled.
  If the overload condition remains for longer than the blanking time, the C/Q driver stays disabled and the auto-retry timer restarts.
- The “overLoad" status bit is set if the overload condition remains for longer than the blanking time and remains set during the auto-retry off time.
- The driver is re-enabled once the “overLoad" status bit is cleared for longer than the blanking time indicating that the overload situation is gone.

The overload status is re-checked at either of the following cases:

- The driver is disabled again, and the “overLoad" status bit remains set.
- The driver stays enabled and the “overLoad" status bit is cleared.

The intention is to avoid permanent toggling of the “overLoad" status bit.

If the auto-retry bit (“autoRetryEn”**)** is disabled:

- The C/Q driver remains active until a thermal shutdown event occurs.
- The status bit is set after the blanking time. The status bit is cleared when the overload condition is gone.

Overload can only occur when TxEN is ‘High’ and “disCShut” bit is set to 0. When TxEN is ‘Low’ (receive only mode) or “disCShut” is 1, the Overload bit and lock condition is cleared.

3.2.3. Low Voltage Detection

3.2.3.1. Under-Voltage Warning

The IC returns a warning if a low voltage condition is detected at the L+ pin.

When the L+ supply voltage drops below the warning voltage, the following bits are set:

- The under-voltage warning interrupt “uvWarnInt” (if enabled) is raised.
- the under-voltage warning status bit “uvWarn” is set.

This status bit is cleared once the L+ voltage rises above the warning release threshold voltage.

3.2.3.2. Under-Voltage Shutdown

The C/Q driver automatically switches off if the L+ supply drops below the shutdown voltage.

When the L+ supply voltage drops below the shutdown voltage, the following bits are set:

- The shutdown interrupt “uvShutInt “(if enabled) is raised.
- the Shutdown status bit “cqShut” is set (under-voltage warning bit remains set).
- the C/Q driver switches off.

The driver is enabled and status bit is cleared when the L+ Voltage rises above the shutdown voltage.

3.2.4. Thermal Protection

A thermal warning is generated if the device exceeds 140°C. The “TempWarn” bit in the status register bit is cleared when the temperature drops below 125°C. The device continues to operate up to 165°C, above that the device’s driver is disabled. A temperature drops of 15°C enables the driver to operate again.

3.3 Receiver Threshold

The C/Q driver voltage thresholds are defined in the IO-link specification if $L+$>=18V. If $L+$<18V, the thresholds are calculated according to an L+ ratio (refer to V_{TH} and V_{TL} values in Table 6).

3.4 Wake-Up Detection

In transmit mode (TxEN=1), the IC can detect the IO-Link specific wake-up request (WURQ) of the IO-Link master. In WURQ, the master overdrives the devices output level for a determined period. The IC detects that event which physically occurs in two ways:

- A current overload (either of High side driver or Low side driver) in the driver output for a certain period.
- A contradiction of the TxD and RxD lines of the device between T_{WU_MIN} and T_{WU_MAX} period (Master pull-down, Slave driver high-Z) when transmitter is enabled

The IC configuration register (“wuMode”) defines if “overload”, “contradiction”, or both events are chosen for the WURQ detection. If a WURQ is detected, the /WU pin is pulled low until TxEN is released.

The wake-up prevention logic avoids generating false wake-up alarms, which can occur when larger capacitances are connected on the /CQ pin. After TxD toggle or driver enable, the Wake-up signal generation is prevented for the duration of the blanking time.

3.5 Wake-Up Generation

3.5.1. Master Mode

In master mode, the external MCU generates a WakeUp pulse by forcing /WU pin to low (which selects the high-power mode) and activating TxEN for 80µs with TxD in the opposite direction of RxD.

When “masterMode” bit is set to 1:

- The /WU pin is an input with activated pull-up resistor.
- When the /WU pin is pulled to low the driver is switched to high power mode and fastest slew-rate, a current >600mA is applied when TxEN is enabled.

Figure 20 displays how to generate a Wake-Up pulse (masterMode bit set to 1).

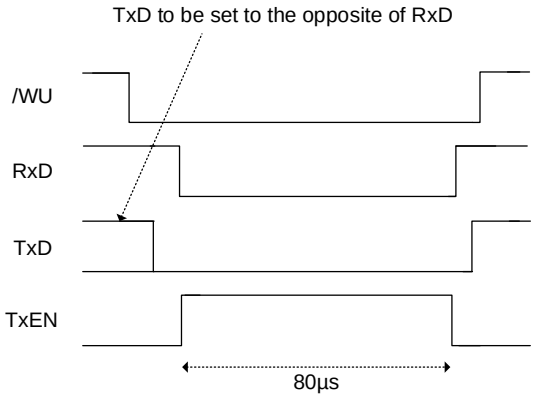

Figure 20. /WU Signal Procedure

3.5.2. Device Mode

In device mode, it is the RH4Z2501 which generates the pulse to wake-up the external MCU from its sleep mode.

3.5.3. Used Pin

Both /WU and OWI/DIAG pins can be used by the external MCU to transmit or receive the WakeUp signal. The OWI/DIAG pin can be used if sparing 1 GPIO of the external MCU is needed.

3.6 Protection

3.6.1. Surge Protection

The device embeds an integrated surge protection circuit capable of withstanding ±1.25kV (500 Ω) of IEC 61000-4-5 surge events. This circuit protects the L+, C/Q, and L- pins from pulses that can happen between any of these pins with positive or negative surge voltage.

3.6.2. Reverse Polarity Protection

Reverse polarity protection circuitry protects the devices against accidental reverse polarity connections to the L+, C/Q, and L- pins. The maximum voltage between any of the pins must not exceed ± 60V DC.

3.6.3. Broken Chip Detection

The chip die is surrounded by a metal wire made to detect a package or die crack during production testing. The conductivity of that metal wire is checked via a dedicated circuitry by its diagnostic function, see Table 11.

4. OWI Interface

The chip has a one-wire digital interface (OWI). This interface is used to configure the device and read out status information. It combines a simple and easy protocol adaptation with a cost-saving pin sharing.

The pin used for OWI communication is also used as an interrupt output. It is necessary that only one device is connected to the GPIO pin of the host controller configured as “N-Channel open drain” at a time. Limitations are the following:

- When DIAG output is asserted, disable the OWI communication.
- The DIAG output can only indicate an interrupt when OWI is in idle mode. If OWI communication is used, the DIAG signal is delayed until OWI returns to idle.

4.1 OWI Protocol

The OWI protocol is defined as follows:

- Idle state
  During inactivity of the bus, the OWI line is pulled up to the IO supply voltage V_{IO} by an internal resistor.
- Start condition
  When the OWI line is in idle mode, a ‘Low’ pulse with a minimum width of $t_{OWI\_START} \geq 4\mu s$ followed by a ‘High’ indicates a start condition. Every request must be initiated by a start condition sent by the OWI master. A master can generate a start condition only when the OWI line is in idle mode.
- Valid data
  Data is transmitted in bytes (8 bits) starting with the most significant bit (MSB). Transmitted bits are recognized after a start condition at every transition from ‘Low’ to ‘High’ at the OWI line. The value of the transmitted bit depends on the duty ratio between the high phase and the ‘High’/’Low’ period (bit period, t_{OWI_BIT}). A duty ratio greater than 1/8 and less than 3/8 is detected as 0; a duty ratio greater than 5/8 and less than 7/8 is detected as 1. The bit period of consecutive bits must not increase to more than 1.5 times the previous bit period or decrease to less than half of the previous bit period otherwise it is detected as a stop condition.

OWI protocol timing and parameters are specified in Figure 21 and Table 6.

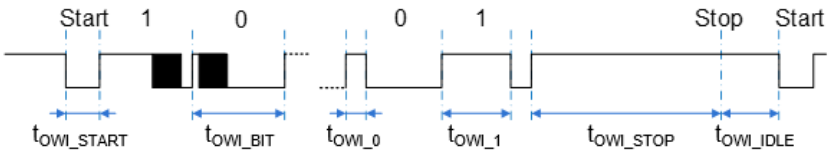

Figure 21. OWI Timing Diagram

4.2 OWI Commands Structure

The RH4Z2501 is always considered as the OWI Slave and the external MCU as OWI Master. The 7bit OWI Slave (no family address required) address is set to 0x55. Note that the OWI communication is not CRC checked.

There is an automatic increment of address pointer to write multiple registers in a short time period.

4.2.1. OWI Write Command

Below are the bit sequences and command structures to perform a write command:

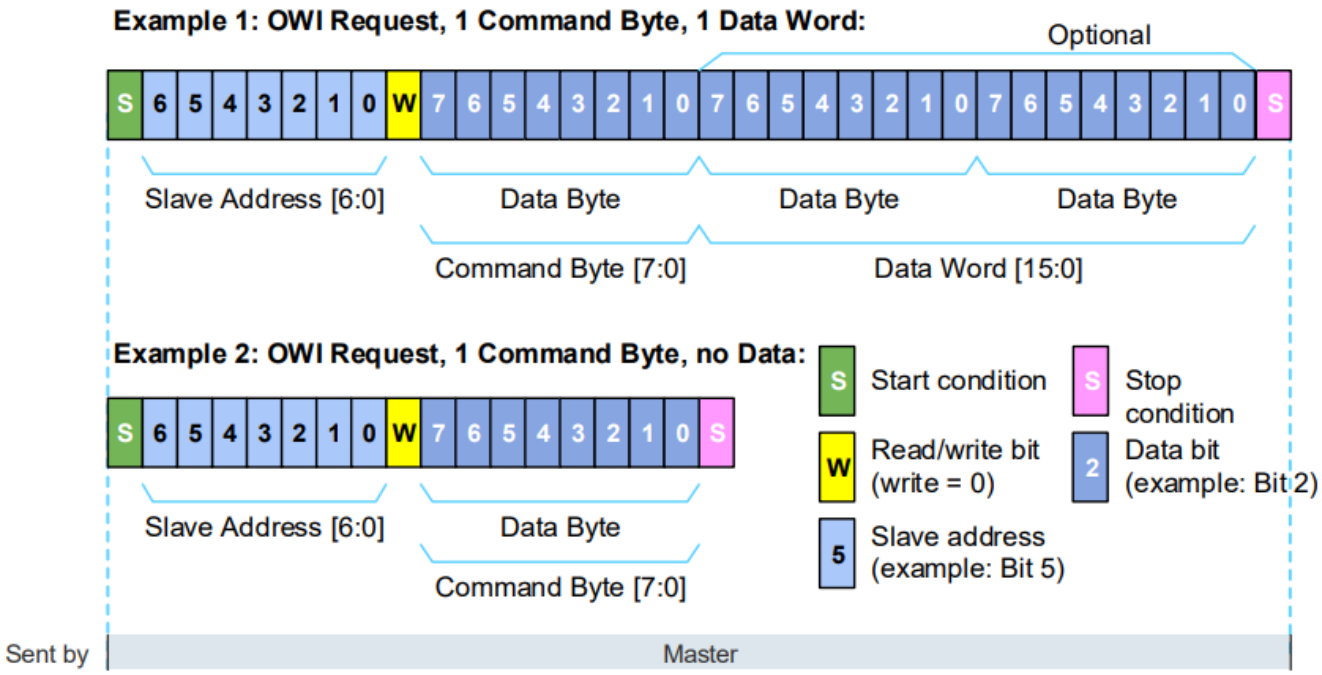

Figure 22. OWI Command Request

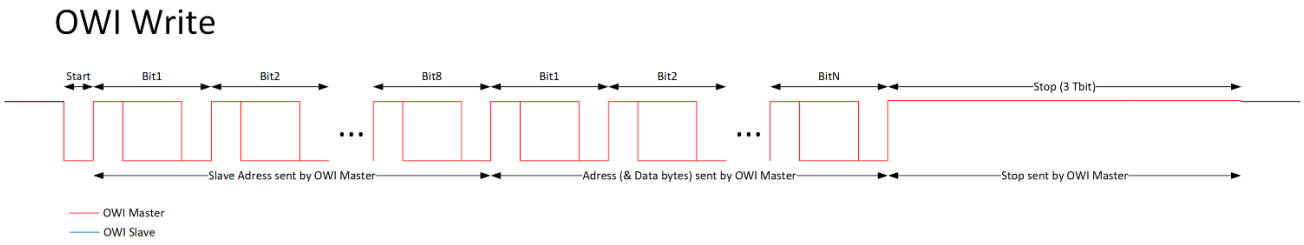

Figure 23: OWI Write Command Chronogram

4.2.2. OWI Read Command

Below are the bit sequences and command structures to perform a read command:

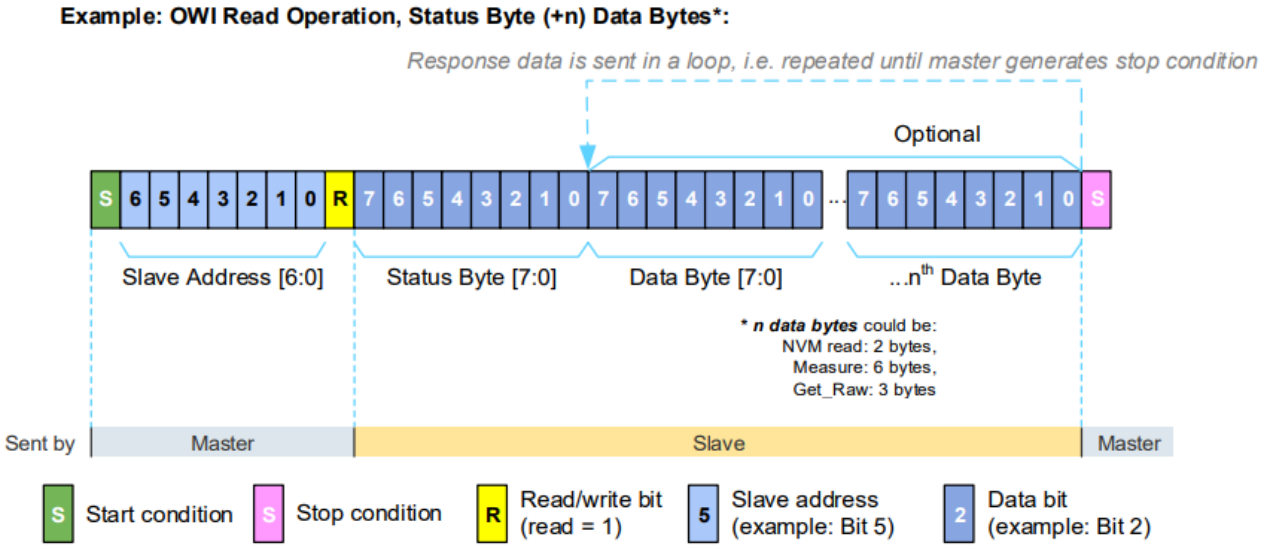

Figure 24. OWI Response by OWI Master

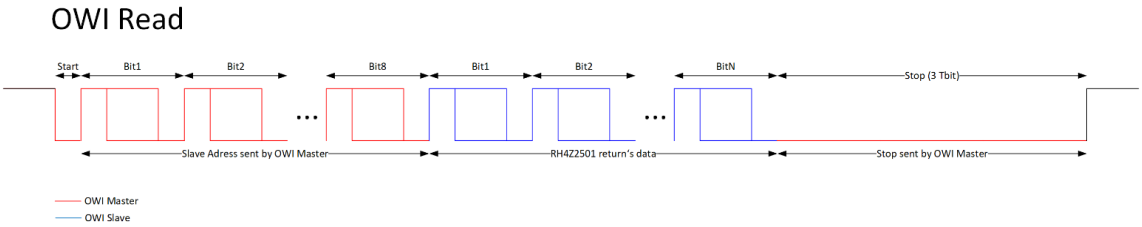

Figure 25: OWI Read Command Chronogram

5. Register Map

Table 9. Register Mapping

Name	Addr	Typ	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IRQ_Status	0x00	R/Rst	uvShutInt	thShutInt	thWarnInt	uvWarnInt	ovWarnInt	wurqInt	overLoadInt	porInt
Status	0x01	R	cqLogic	cqShut	thWarn	uvWarn	ovWarn	wurq	overLoad	bcc
IRQ_Enable	0x02	R/W	uvShutIntEn	thShutIntEn	thWarnIntEn	uvWarnIntEn	ovWarnIntEn	wurqIntEn	overLoadIntEn	reserved
comParam	0x03	R/W	slewRateEn	slewRate			currLim			
comCtrl1	0x04	RW	digFiltSel		anaFiltEn	cqInvert	pullUpEn	pullDownEn	lshsEn	
comCtrl2	0x05	RW	swRst	autoRetryEn	autoRetryTim		blankTim		wuMode	
alarm	0x06	RW	0	disSurgeProt	reserved	disDebounce	disLdo	disCShut	disTShut	disVShut
Master	0x07	RW	0	0	0	0	0	currSinkSel		masterMode
icVersion	0x08	R	0	0	0	0	0	0	0	1

5.1 IRQ_Status

The register bits are set by an interrupt event. The content of this register stays until the register is read.

Table 10. Register IRQ_Status Description

Command	IRQ_Status (00h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	uvShutInt	thShutInt	thWarnInt	uvWarnInt	ovWarnInt	wurqInt	overLoadInt	porInt
Access	Read clears all	Read clears all	Read clears all	Read clears all	Read clears all	Read clears all	Read clears all	Read clears all
Default Value	0	0	0	0	0	0	0	1

Bit	Function	Description
7	uvShutInt	Under-voltage shutdown interrupt • 1: The voltage on L+ fell below shutdown threshold since the last register read. • 0: The voltage on L+ stayed above shutdown threshold.
6	thShutInt	Thermal shutdown interrupt • 1: The junction temperature exceeded thermal shutdown threshold since the last register read. • 0: No thermal shutdown occurred.
5	thWarnInt	Thermal warning interrupt • 1: The junction temperature exceeded thermal warning threshold since the last register read. • 0: No thermal warning occurred.
4	uvWarnInt	Under-voltage warning interrupt • 1: The voltage on L+ happened to fall below under-voltage warning threshold since the last register read. • 0: The voltage on L+ stayed above under-voltage warning threshold
3	ovWarnInt	Over-voltage warning interrupt • 1: The voltage on L+ exceeded over-voltage warning threshold since the last register read. • 0: The voltage on L+ stayed below over-voltage warning threshold.
2	wurqInt	Wake-up interrupt

Bit	Function	Description
		• 1: A wake-up event was detected since the last register read. • 0: No wake-up event detected.
1	overLoadInt	Overload interrupt • 1: The C/Q driver current exceeded the overload condition longer than the blanking time since last register read. • 0: The C/Q driver current stayed within the limits.
0	porInt	Power-on reset (not mask able) • 1: A power-on reset happened since the last readout. • 0: No power-on reset happened.

5.2 Status

The register bits shows the current status of the device. This register is read-only.

Table 11. Register Status Description

Command	Status (01h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	cqLogic	cqShut	thWarn	uvWarn	ovWarn	wurq	overLoad	bcc
Access	Readonly	Readonly	Readonly	Readonly	Readonly	Readonly	Readonly	Readonly
Default Value	0	0	0	0	0	0	0	0

Bit	Function	Description
7	cqLogic	Logic level on RxD pin. • 1: RxD pin is high. • 0: RxD pin is low.
6	cqShut	C/Q driver in shutdown (thermal or under-voltage shutdown condition). • 1: Shutdown due to under-voltage condition or thermal temperature exceeding limit. • 0: C/Q driver not in shutdown.
5	thWarn	Thermal warning. • 1: The junction temperature exceeded the thermal warning threshold. • 0: The temperature is below the thermal warning condition.
4	uvWarn	Under-voltage warning. • 1: The voltage on L+ is below under-voltage warning threshold. • 0: The voltage on L+ is above under-voltage warning threshold.
3	ovWarn	Over-voltage warning • 1: The voltage on L+ is above over-voltage warning threshold. • 0: The voltage on L+ is below over-voltage warning threshold.
2	wurq	Wake-up signal • 1: A wake-up event was detected. This bit is cleared when TxEN is low. • 0: No wake-up event detected.
1	overLoad	Overload detected. • 1: The C/Q driver is in overload condition. • 0: The C/Q driver is within the limits.
0	bcc	Broken chip information (bit is set/cleared in the start-up phase) • 0: Device satisfactory.

5.3 IRQ_Enable

The register bits enable or mask interrupt events.

Table 12. Register IRQ_Enable Description

Command	IRQ_Enable (02h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	uvShutIntEn	thShutIntEn	thWarnIntEn	uvWarnIntEn	ovWarnIntEn	wurqIntEn	overLoadIntEn	Reserved
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	1	1	1	1	1	0	1	1

Bit	Function	Description (**Bold** font indicates the default setting)
7	uvShutIntEn	Under-voltage shutdown interrupt enable. • **1: Interrupt signaling of under-voltage shutdown on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal an under-voltage shutdown condition.
6	thShutIntEn	Thermal shutdown interrupt enable. • **1: Interrupt signaling of thermal shutdown on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal a thermal shutdown condition.
5	thWarnIntEn	Thermal warning interrupt enable. • **1: Interrupt signaling of thermal warning on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal a thermal warning condition.
4	uvWarnIntEn	Under-voltage warning interrupt enable. • **1: Interrupt signaling of under-voltage warning on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal an under-voltage warning condition.
3	ovWarnIntEn	Over-voltage warning interrupt enable. • **1: Interrupt signaling of over-voltage warning on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal an over-voltage warning condition.
2	wurqIntEn	Wake-up interrupt enable. • 1: Interrupt signaling of a wake-up detection on OWI/DIAG pin is enabled. • **0: OWI/DIAG pin does not signal a wake-up detection.**
1	overLoadIntEn	Overload interrupt enable. • **1: Interrupt signaling of an overload condition on OWI/DIAG pin is enabled.** • 0: OWI/DIAG pin does not signal an overload condition.
0	Reserved	Not used

5.4 comParam

The register bits configure the driver parameters.

Table 13. Register comParam Description

Command	comParam (03h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	slewRateEn	slewRate			Reserved			
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	1	1	1	0	0	0	1	1

Bit	Function	Description (**Bold** font indicates the default setting)
7	slewRateEn	Enable slew rate. • **1: Slew rate is regulated.** • 0: Slew rate regulation is disabled.
6 **5** **4**	slewRate	Value of slew rate (default 120V/µs). • 000: 20V/µs • 001: 30V/µs • 010: 40V/µs • 011: 60V/µs • 100: 80V/µs • 101: 100V/µs • **110: 120V/µs (default)** • 111: 140V/µs
3	Reserved	0
2 **1** **0**	currLim	Value of current limit. • 000: 50mA • 001: 100mA • 010: 150mA • **011: 200mA (default)** • 100: 250mA • 101: 300mA • 110: 350mA • 111: 400mA

5.5 comCtrl1

The register bits configure the transceiver parameters.

Table 14. Register comCtrl1 Description

Command	comCtrl1 (04h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	digFiltSel		anaFiltEn	cqInvert	pullUpEn	pullDownEn	lshsOn	
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	0	0	1	0	0	0	1	1

Bit	Function	Description (**Bold** font indicates the default setting)
7 **6**	digFiltSel	Digital deglitch filter. • **00: Disable digital filter function.** • 01: Digital 200ns filter (COM3). • 10: Digital 1.6µs filter (COM2). • 11: Digital 13µs filter (COM1).
5	anaFiltEn	Analog (slow) deglitch filter. • **1: Enable filter function.** • 0: Disabled filter function.
4	cqInvert	C/Q Invert enable/disable. • 1: The C/Q driver logic follows the TX input logic (if driver is enabled). RX logic follows the C/Q driver/receiver logic. • **0: The C/Q driver logic is the inverse of the TX input logic (if driver is enabled). RX logic is the inverse of the C/Q driver/receiver logic.**
3	pullUpEn	Weak Pull-up current source. • **0: No pull-up current source.** • 1: A pull-up current source is activated on CQ pin.
2	pullDownEn	Weak pull-down current source. • **0: No pull-down current source.** • 1: A pull-down current sink is activated on CQ pin.
1 **0**	lshsEn	C/Q Driver mode • 00: C/Q driver is disabled regardless of TxEN, the driver is high impedance. • 01: PNP operation. • 10: NPN operation. • **11: Push-Pull mode.**

5.6 comCtrl2

The register bits configure the transceiver parameters.

Table 15. Register comCtrl2 Description

Command	comCtrl2 (05h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	swRst	autoRetryEn	autoRetryTim		blankTim		wuMode	
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	0	1	0	0	0	0	1	1

Bit	Function	Description (**Bold** font indicates the default setting)
7	swRst	Software reset • 1: Trigger a reset, all registers are set to their default state. Status is cleared, IRQ is de-asserted. • **0: Normal operation.**
6	autoRetryEn	Auto-retry enable • **1: Fixed off-time functionality is enabled. C/Q driver is disabled for a fixed time after an overcurrent or thermal fault occurs. The driver is re-enabled automatically after the fixed off-delay.** • 0: Fixed off-time functionality is disabled. The driver is re-enabled after temperature falls below the thermal hysteresis.
5 **4**	autoRetryTim	Auto-retry fixed off-time Set the autoRetryTim to select the fixed driver off-time after a fault was generated when auto-retry functionality is enabled (autoRetryEn = 1). The driver is re-enabled automatically after the fixed off-delay. • **00: Fixed off-time is 50ms.** • 01: Fixed off-time is 100ms. • 10: Fixed off-time is 200ms. • 11: Fixed off-time is 500ms.
3 **2**	blankTim	Blanking time Minimum blanking time to signal a current limit. • **00: 128µs.** • 01: 500µs. • 10: 1ms. • 11: 5ms.
1 **0**	wuMode	Wake-up detection Turn on both OVL and RX/TX wakeup detection mechanisms (wuMode = 11) for stable Wakeup detection. • 00: No Wake-up detection. • 01: Enable Wake-up detection by OVL condition. • 10: Enable Wake-up detection by RX/TX mismatch. • **11: Enable Wake-up detection by OVL condition or RX/TX mismatch.**

5.7 alarm

The register bits configure the transceiver parameters.

Table 16. Register Alarm Description

Command	alarm (06h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	reserved	disSurgeProt	reserved	disDebounce	disLDO	disCShut	disTShut	disVShut
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	0	0	0	0	0	0	0	0

Bit	Function	Description (**Bold** font indicates the default setting)
7	reserved	Set to 0
6	disSurgeProt	Surge protection. • 1: Surge protection disabled. • **0: Surge protection enabled.**
5	reserved	Set to 0
4	disDebounce	Debouncing filter for thermal and voltage monitor. • 1: Debouncing filter disabled. • **0: Debouncing filter enabled.**
3	disLDO	Disable 3.3V LDO. • 1: 3.3V LDO disabled. • **0: 3.3V LDO enabled.**
2	disCShut	Disable driver detection&shutdown of driver in overload condition. • 1: Driver shut-down disabled. • **0: Driver shut-down enabled/possible.**
1	disTShut	Disable shut-down of driver for over-temperature condition. • 1: Thermal shut-down disabled. • **0: Thermal shut-down enabled/possible.**
0	disVShut	Disable shut-down of driver for under-voltage condition • 1: Under-voltage shut-down disabled. • **0: Under-voltage shut-down enabled/possible.**

5.8 Master

The register bits configure the transmitter for master mode operation.

Table 17. Register Master Description

Command	Master (07h)							
Bit Position	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Function	reserved	reserved	reserved	reserved	reserved	CurrSinkSel		MasterMode
Access	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write	Read/Write
Default Value	0	0	0	0	0	0	0	0

Bit	Function	Description
7	Reserved	
6	Reserved	
5	Reserved	
4	Reserved	
3	Reserved	
2 **1**	CurrSinkSel	• **00: No current sink.** • 01: 3mA current sink. • 10: 6mA current sink. • 11: 9mA current sink.
0	MasterMode	Set the device to master mode. • 1: the device is able to generate a wake-up pulse. A low on WU pin sets highest slew rate and min 500mA current; TxD defines high side or low side driver; TxEN controls the pulse length. • **0: /WU pin is used as output to signal a wake-up pulse detection.**

6. Package Outline Drawings

The package outline drawings are available below:

6.1 DFN12

Package Outline Drawing Package Code: NCG12P1 12DFN 3.0 x 3.0 x 0.75 mm Body 0.5 mm Pitch (renesas.com)

6.2 15-DSBGA

Package Outline Drawing Package Code: AHG15D1 1.61 x 2.41 x 0.6 mm Body, 0.4mm Pitch (renesas.com)

7. Glossary

Term	Definition
ADC	Analog to Digital Converter
C/Q	connection for communication (C) or switching (Q)
CRC	Cyclic Redundancy Check
DC	Direct Current
DC-DC	Direct Current to Direct Current
DFN	Dual Flat no Leads Package
ESD	Electro-Static Discharge
GPIO	General Purpose Input Output
HBM	Human Body Model
IC	Integrated Circuit
IEC	Internation Electrotechnical Commission
IO	Input Output
IRQ	Interrupt Request
LDO	Low Drop Out
MCU	Microcontroller
MSB	Most Significant Bit
NPN	Negative-Positive-Negative
PNP	Positive-Negative-Positive
OVL	Over-Voltage Level
OWI	One Wire Interface
PHY	Physical Layer
WCSP	Wafer Level Chip Scale Package
WURQ	Wake-Up Request

8. Revision History

Revision	Date	Description
1.3	Dec.11.24	Added MSL information.
1.2	Aug.28.24	Added Exposed Pad (EP) description.
1.1	Jun.25.24	Added Wakeup detection setting recommendation.
1.0	Jun.08.23	Initial release

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