Product Introduction

Concept

The market of instrument clusters on automotive requires various kinds of unit, such as from traditional instrument clusters to graphical instrument clusters.

The RH850/D1x series microcontroller focuses on instrument clusters for automotive.

The RH850/D1x series can cover wide range of instrument clusters.

Major differences in the series are functionality of graphics.

Then, it is possible to choose products in RH850/D1x series by graphics functionality of instrument clusters.

In addition, other functionality, such as standard peripherals and instrument cluster specific peripherals, has very high compatibility.

Therefore, RH850/D1x series makes easy to develop platform by reducing software development costs.

In addition, there are several features, such as internal Video RAM, for reduce BOM costs.

Function Overview

- RH850/D1L (1/2)

Series Name			D1L1	D1L2	D1L2H
Memory	Code Flash		2 MB	4 MB	
	Local RAM (LRAM)		256 KB	512 KB	
	Retention RAM (RRAM)		16 KB		
	Data Flash		64 KB		
	Video RAM (VRAM) with Video RAM wrapper		—	144 KB	
External memory interfaces	Serial Flash Memory I/F (SFMA)	Bus width	4-bit	4-bit	8-bit
		Mode	SDR	SDR, DDR	SDR, DDR
		Max. clock	40 MHz	SDR: 120 MHz, DDR: 80 MHz	SDR: 120 MHz, DDR: 80 MHz
CPU	CPU System		G3M		
	CPU frequency		120 MHz		
	Floating Point Unit (FPU)		Provided		
	Memory Protection Unit (MPU)		Provided		
	Memory caches	Instruction cache	8 KB/4-way associative		
		Non-CPU system memories	—	16 KB/4-way associative	
DMA			16 channels		
Operating clock	Main Oscillator (MainOSC)		8 to 16 MHz		
	Low Speed Internal Oscillator (LS IntOSC)		typ. 240 kHz		
	High Speed Internal Oscillator (HS IntOSC)		typ. 8 MHz		
	Sub Oscillator (SubOSC)		typ. 32.768 kHz		
	Spread-spectrum PLL0		max. 480 MHz		
	PLL1		fixed to 480 MHz		
I/O port			103	103	126
A/D Converter (ADCE)			16 channels, 12 bit resolution		
Timer	Timer Array Unit B (TAUB)		3 units (16 bit resolution, 16 channels/unit)		
	Timer Array Unit J (TAUJ)		1 unit (32 bit resolution, 4 channels/unit)		
	Operating System Timer (OSTM)		2 units (32 bit resolution, 1 channel/unit)		
	Alway-On-Area Timer (AWOT)		1 unit (32 bit resolution, 1 channel/unit)		
	Real-Time Clock (RTCA)		Provided		
	Window Watchdog Timer A (WDTA)		2 units		
	PWM Generators with Diagnostic		1 unit (12 bit resolution, 24 PWM generators, 12 with diagnostic capability)		
Communication interfaces	Clocked Serial Interface G (CSIG)		4 channels		
	Clocked Serial Interface H (CSIH)		2 channels		
	CAN Interface (RS-CAN)		3 channels (total 192 message buffers)*1		
	CAN Interface (RS-CANFD)		3 channels (total 192 message buffers)*1		
	LIN/UART Interface (RLIN3)		4 channels		
	I^2C Interface (RIIC)		2 channels		
External interrupts	Maskable		11		
	Non-maskable (NMI)		1		
Audio	Sound Generator (SG)		5 units		
	PCM-PWM Converter (PCMP)		1 unit		
	I^2S Interface (SSIF)		2 units (1 channel/unit)		

- RH850/D1L (2/2)

Series Name			D1L1	D1L2	D1L2H
Video and Graphics	Video Output	Channels	—	1 channel (480 × 320 pixels, 10 MHz pixel clock, RGB666, 4 layers)	
		I/F	—	LVTTL	
		RLE decoding	—	Provided	
		Sprite layer	—	3 × 16 sprites for 3 output layers	
		Timing Controller (TCON)	—	3 programmable signals	7 programmable signals
Other functions	LCD Bus I/F (LCBI)		18 bit output, max. 10 MHz		
	Clock Monitors (CLMA)		for MainOSC, LS IntOSC, HS IntOSC, SSCG0, PLL1		
	Data CRC (DCRA)		Provided		
	Power-On-Clear (POC)		Provided		
	Intelligent Stepper Motor Driver (ISM), incl. zero point detection for each channel		1 unit, 6 channels		
	Error Correction Coding (ECC)		for Code Flash, Data Flash, Local RAM, Retention RAM, RS-CAN RAM, Caches tag/data RAMs	for Code Flash, Data Flash, Local RAM, Retention RAM, Video RAM, RS-CAN RAM, Caches tag/data RAMs	
	Intelligent Cryptographic Unit (ICU-S2)		Provided		
	On-Chip debug (OCD)		Provided		
	Boundary Scan		Provided		
Voltage supply*2	Internal logic	AWO*3	3.3 V, 5 V via on-chip voltage regulator		
		ISO*3	3.3 V, 5 V via on-chip voltage regulator		
	I/O buffers	GPIO*3	3.3 V, 5 V		
	A/D Converter supplies		nominal 3.3 V, 5 V		
Package	Type		QFP	QFP	QFP
	Pins		144	144	176
	pin/ball pitch		0.5 mm	0.5 mm	0.5 mm

Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

Note 2. The supply voltages are given as nominal values. Refer to data sheet **Section 1.5.11, Supply Voltage** for detail specification of electrical values.

Note 3. AWO: Always-On-Area
ISO: Isolated-Area
GPIO: General purpose I/O port

- RH850/D1M (1/3)

Series Name:			D1M1_		D1M1H_			
			3.75M	5M	3.75M	5M	D1M1A	D1M1-V2
Memory	Code Flash		3.75 MB	5 MB	3.75 MB	5 MB	4 MB	4 MB
	Local RAM (LRAM)		512 KB					
	Retention RAM (RRAM)		16 KB					
	Data Flash		64 KB					
	Video RAM (VRAM) with Video RAM wrapper		1.55 MB				2 × 1.2 MB	1.55 MB
External memory interfaces	SDRAM I/F	Bus width	—		32-bit			—
		Mode	—		SDR-SDRAM (SDRA)			—
		Max. clock	—		100 MHz		120 MHz	—
	Serial Flash Memory I/F 0/2 (SFMA0/2)	Bus width	SFMA0: 8bit, SFMA2: 4bit					SFMA0: 8bit
		Mode	SDR, DDR					
		Max. clock	SDR: 120 MHz, DDR: 80 MHz					
	Serial Flash Memory I/F 1 (SFMA1)	Bus width	—				8 bits	
		Mode	—				SDR, DDR	
		Max. clock	—				40 MHz	
	HyperBus I/F 1 (HYPB)	Bus width	—				8 bits	
		Mode	—				DDR	
		Max. clock	—				80 MHz	
	OCTA Flash I/F (OCTA)	Bus width	—				8 bits	
		Mode	—				DDR	
		Max. clock	—				80 MHz	
	NAND Flash I/F (NFMA)	Bus width	—				8 bits	—
		Mode	—				ONFi 1.0 [mode 0 and 1]	—
		Max. clock	—				20 MHz	—
CPU	CPU System		G3M					
	CPU frequency		160 MHz		200 MHz		240 MHz	160 MHz
	Floating Point Unit (FPU)		Provided					
	Memory Protection Unit (MPU)		Provided					
	Memory caches	Instruction cache	8 KB/4-way associative					
		Non-CPU system memories	16 KB/4-way associative					
DMA			16 channels					
Operating clock	Main Oscillator (MainOSC)		8 to 16 MHz					
	Low Speed Internal Oscillator (LS IntOSC)		typ. 240 kHz					
	High Speed Internal Oscillator (HS IntOSC)		typ. 8 MHz					
	Sub Oscillator (SubOSC)		typ. 32.768 kHz					
	Spread-spectrum PLL0		max. 480 MHz				max. 960 MHz	
	PLL1		max. 480 MHz					
I/O port			126				127	
A/D Converter (ADCE)			16 channels, 12 bit resolution					

- RH850/D1M (2/3)

Series Name:			D1M1_		D1M1H_		D1M1A	D1M1-V2
			3.75M	5M	3.75M	5M		
Timer	Timer Array Unit B (TAUB)		3 units (16 bit resolution, 16 channels/unit)					
	Timer Array Unit J (TAUJ)		1 unit (32 bit resolution, 4 channels/unit)					
	Operating System Timer (OSTM)		2 units (32 bit resolution, 1 channel/unit)					
	Alway-On-Area Timer (AWOT)		1 unit (32 bit resolution, 1 channel/unit)					
	Real-Time Clock (RTCA)		Provided					
	Window Watchdog Timer A (WDTA)		2 units					
	PWM Generators with Diagnostic		1 unit (12 bit resolution, 24 PWM generators, 12 with diagnostic capability)					
Communica-tion interfaces	Clocked Serial Interface G (CSIG)		4 channels					
	Clocked Serial Interface H (CSIH)		2 channels					
	CAN Interface (RS-CAN)		3 channels (total 192 message buffers)*1				3 channels (total 192 message buffers)*1	
	CAN Interface (RS-CANFD)		—				3 channels (total 192 message buffers)*1	
	LIN/UART Interface (RLIN3)		4 channels					
	I^2C Interface (RIIC)		2 channels					
	Ethernet AVB MAC (ETNB)		1 channel (Media Access Controller for up to 100 Mbps, with Audio Video Bridging)					
External interrupts	Maskable		11					
	Non-maskable (NMI)		1					
Audio	Sound Generator (SG)		5 units					
	PCM-PWM Converter (PCMP)		1 unit					
	I^2S Interface (SSIF)		2 units (1 channel/unit)					
Video and Graphics	Video Output 0 (VO0)	Resolution	1024 ×1024 pixels				1280 × 1024 pixels	1024 × 1024 pixels
		Color format	RGB888					
		Max. pixel clock	30 MHz				48 MHz LVTTL, 34 MHz OpenLDI, 30 MHz VODDR	30 MHz LVTTL
		Layers	4					
		I/F	LVTTL				LVTTL, OpenLDI, VODDR	LVTTL
		Predistortion	Warping Engine (VOWE)					
		Timing Controller (TCON)	7 programmable signals					
		Video output data control	Video Output Checker (VOCA), 2 CRC checker (DISCOM)					

- RH850/D1M (3/3)

Series Name:			D1M1_		D1M1H_		D1M1A	D1M1-V2
			3.75M	5M	3.75M	5M		
Video and Graphics	Video Output 1 (VO1)	Resolution	—				1280 × 1024 pixels	—
		Color format	—				RGB888	—
		Max. pixel clock	—				40 MHz SerialRGB, 30 MHz VODDR	—
		Layers	—				4	—
		I/F	—				SerialRGB, VODDR	—
		Predistortion	—				—	—
		Timing Controller (TCON)	—				—	—
		Video output data control	—				Video Output Checker (VOCA) 2 CRC checker (DISCOM)	—
	Video Outputs shared features	RLE decoding	Provided for background layers				Provided for all layers	
		Sprite layer	3 × 16 spiites				4 × 16 sprites	
	Video Input (VI)	Channels	1 channel					
		Resolution	1024 × 1024 pixels					
		Pixel clock	30 MHz					
		Color formats	RGB666, ITU656					
		I/F	LVTTL					
	Graphics Processing Unit		2D Graphics Processing Unit (GPU2D), 80 MHz operation clock		2D Graphics Processing Unit (GPU2D), 100 MHz operation clock		2D Graphics Processing Unit (GPU2D), 120 MHz operation clock	2D Graphics Processing Unit (GPU2D), 80 MHz operation clock
	JPEG Unit (JCUA)		Provided					
Other functions	LCD Bus I/F (LCBI)		18 bit output, max. 10 MHz		—			18 bit output, max. 10 MHz
	Clock Monitors (CLMA)		for MainOSC, LS IntOSC, HS IntOSC, SSCG0, PLL1, Video Input pixel clocks					
	Data CRC (DCRA)		Provided					
	Power-On-Clear (POC)		Provided					
	Intelligent Stepper Motor Driver (ISM), incl. zero point detection for each channel		1 unit, 6 channels					
	Error Correction Coding (ECC)		for Code Flash, Data Flash, Local RAM, Retention RAM, Video RAM, RS-CAN RAM, Caches tag/data RAMs					
	Intelligent Cryptographic Unit (ICU-S2)		Provided					
	On-Chip debug (OCD)		Provided					
	Boundary Scan		Provided					
Voltage supply*2	Internal logic	AWO*3	3.3 V, 5 V via on-chip voltage regulator					
		ISO*3	3.3 V via on-chip voltage regulator					
	I/O buffers	GPIO*3	3.3 V, 5 V					
		SDR-SDRAM	—		3.3 V			
	A/D Converter supplies		nominal 3.3 V, 5 V					
Package	Type		HLQFP		BGA			LQFP
	Pins		176		272			176
	pin/ball pitch		0.5 mm		1.0 mm			0.5 mm

Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

Note 2. The supply voltages are given as nominal values. Refer to data sheet **Section 1.5.11, Supply Voltage** for detail specification of electrical values.

Note 3. AWO: Always-On-Area
ISO: Isolated-Area
GPIO: General purpose I/O port

- RH850/D1M (1/2)

Series Name			D1M2_		D1M2H_	
			3.75M	5M	3.75M	5M
Memory	Code Flash		3.75 MB	5 MB	3.75 MB	5 MB
	Local RAM (LRAM)		512 KB			
	Retention RAM (RRAM)		16 KB			
	Data Flash		64 KB			
	Video RAM (VRAM) with Video RAM wrapper		2 × 1.55 MB			
External memory interfaces	SDRAM I/F	Bus width	16-bit		32-bit	
		Mode	DDR2-SDRAM I/F (SDRB)			
		Max. clock	240 MHz			
	Serial Flash Memory I/F (SFMA)	Bus width	8 bit			
		Mode	SDR, DDR			
		Max. clock	SDR: 120 MHz, DDR: 80 MHz			
CPU	CPU System		G3M			
	CPU frequency		240 MHz			
	Floating Point Unit (FPU)		Provided			
	Memory Protection Unit (MPU)		Provided			
	Memory caches	Instruction cache	8 KB/4-way associative			
		Non-CPU system memories	32 KB/4-way associative			
DMA			16 channels			
Operating clock	Main Oscillator (MainOSC)		8 to 16 MHz			
	Low Speed Internal Oscillator (LS IntOSC)		typ. 240 kHz			
	High Speed Internal Oscillator (HS IntOSC)		typ. 8 MHz			
	Sub Oscillator (SubOSC)		typ. 32.768 kHz			
	Spread-spectrum PLL0		480 MHz			
	PLL1		fixed to 480 MHz			
	PLL2		max. 480 MHz			
I/O port			159	159	199	199
A/D Converter (ADCE)			20 channels, 12 bit resolution			
Timer	Timer Array Unit B (TAUB)		3 units (16 bit resolution, 16 channels/unit)			
	Timer Array Unit J (TAUJ)		1 unit (32 bit resolution, 4 channels/unit)			
	Operating System Timer (OSTM)		2 units (32 bit resolution, 1 channel/unit)			
	Alway-On-Area Timer (AWOT)		1 unit (32 bit resolution, 1 channel/unit)			
	Real-Time Clock (RTCA)		Provided			
	Window Watchdog Timer A (WDTA)		2 units			
	PWM Generators with Diagnostic		1 unit (12 bit resolution, 24 PWM generators, 12 with diagnostic capability)			
Communication interfaces	Clocked Serial Interface G (CSIG)		4 channels			
	Clocked Serial Interface H (CSIH)		2 channels			
	CAN Interface (RS-CAN)		3 channels (total 192 message buffers)			
	CAN Interface (RS-CANFD)		3 channels (total 192 message buffers)			
	LIN/UART Interface (RLIN3)		4 channels			
	I^2C Interface (RIIC)		2 channels			
	Ethernet AVB MAC (ETNB)		1 channel (Media Access Controller for up to 100 Mbps, with Audio Video Bridging)			
	Media Local Bus (MLBB)		—		1 channel (50 Mbps)	

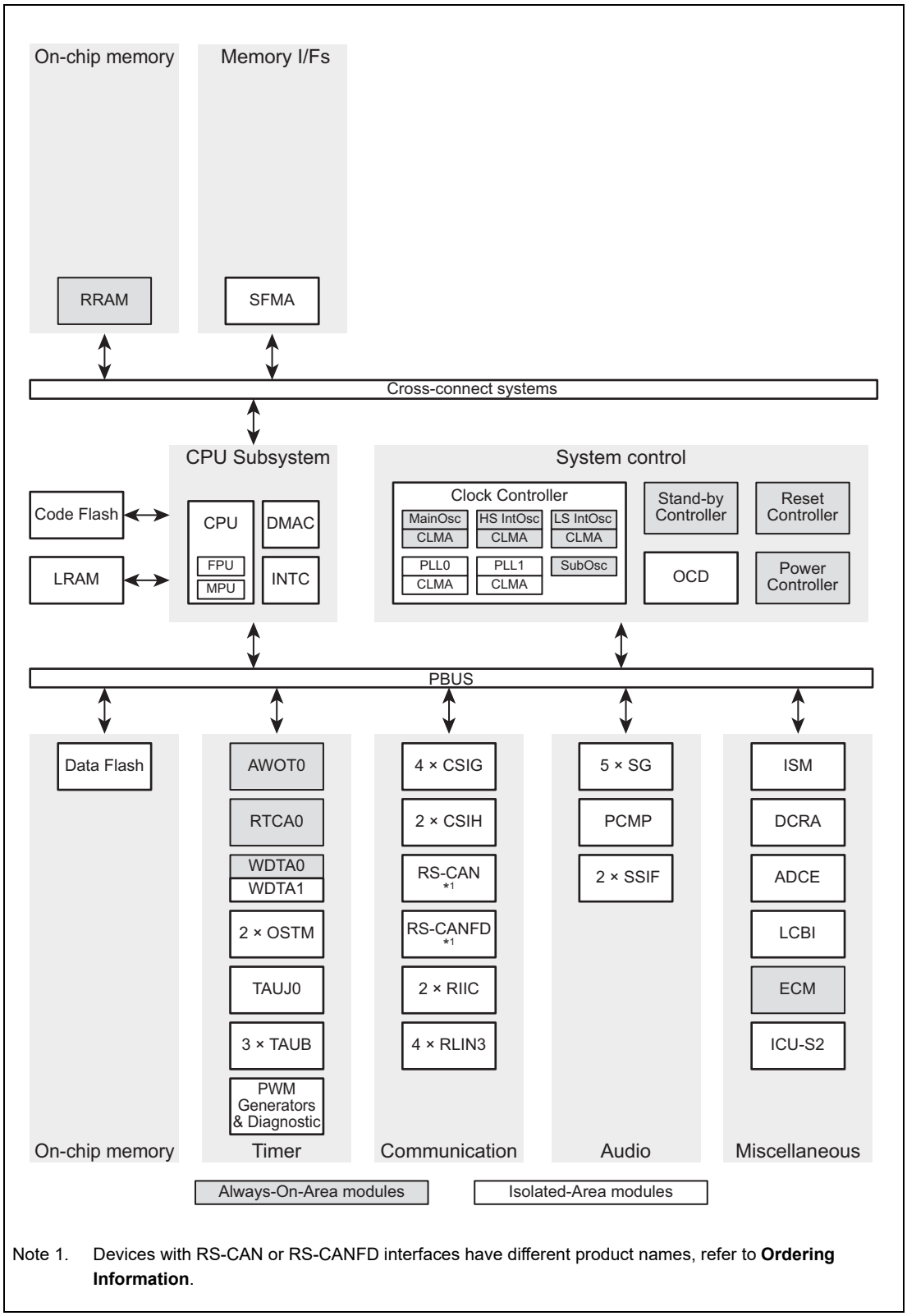
- RH850/D1M (2/2)

Series Name			D1M2_		D1M2H_	
			3.75M	5M	3.75M	5M
External interrupts	Maskable		11			
	Non-maskable (NMI)		1			
Audio	Sound Generator (SG)		5 units			
	PCM-PWM Converter (PCMP)		1 unit			
	I^2S Interface (SSIF)		2 units (1 channel/unit)			
Video and Graphics	Video Output (VO)	Channels	2 channels (1280 × 1024 pixels, 48 MHz pixel clock, RGB888, 4 layers)			
		I/F	LVTTL for both channels, single RSDS selectable for channel 0 or 1			
		Predistortion	Warping Engine (VOWE) for video channel 0			
		RLE decoding	Provided for each video channel			
		Sprite layer	3 × 16 sprites for 3 output layers			
		Timing Controller (TCON)	7 programmable signals			
	Video Input (VI)	Channels	1 channel		2 channels	
		Resolution	1024 × 1024 pixels			
		Pixel clock	48 MHz			
		Color formats	RGB888, ITU656			
		I/F	LVTTL		LVTTL for both channels, single MIPI CSI-2 for channel 0	
	Graphics Processing Unit		2D Graphics Processing Unit (GPU2D), 240 MHz operation clock			
	JPEG Unit (JCUA)		Provided			
	Video output data control		Video Output Checker (VOCA) 2 CRC checker (DISCOM) for each video channel			
Other functions	LCD Bus I/F (LCBI)		—			
	Clock Monitors (CLMA)		for MainOSC, LS IntOSC, HS IntOSC, SSCG0, PLL1, Video Input pixel clocks			
	Data CRC (DCRA)		Provided			
	Power-On-Clear (POC)		Provided			
	Intelligent Stepper Motor Driver (ISM), incl. zero point detection for each channel		1 unit, 4 channels		1 unit, 6 channels	
	Error Correction Coding (ECC)		for Code Flash, Data Flash, Local RAM, Retention RAM, Video RAM, RS-CAN RAM, Caches tag/data RAMs			
	Intelligent Cryptographic Unit (ICU-S2)		Provided			
	On-Chip debug (OCD)		Provided			
	Boundary Scan		Provided			
Voltage supply*1	Internal logic	AWO*2	3.3 V, 5 V via on-chip voltage regulator			
		ISO*2	1.25 V			
	I/O buffers	GPIO*2	3.3 V, 5 V			
		SDR-SDRAM	—			
		DDR2-SDRAM	1.8 V			
	A/D Converter supplies		nominal 3.3 V, 5 V			
Package	Type		BGA		BGA	
	Pins		376		484	
	pin/ball pitch		1.0 mm		1.0 mm	

Note 1. The supply voltages are given as nominal values. Refer to data sheet **Section 1.5.11, Supply Voltage** for detail specification of electrical values.

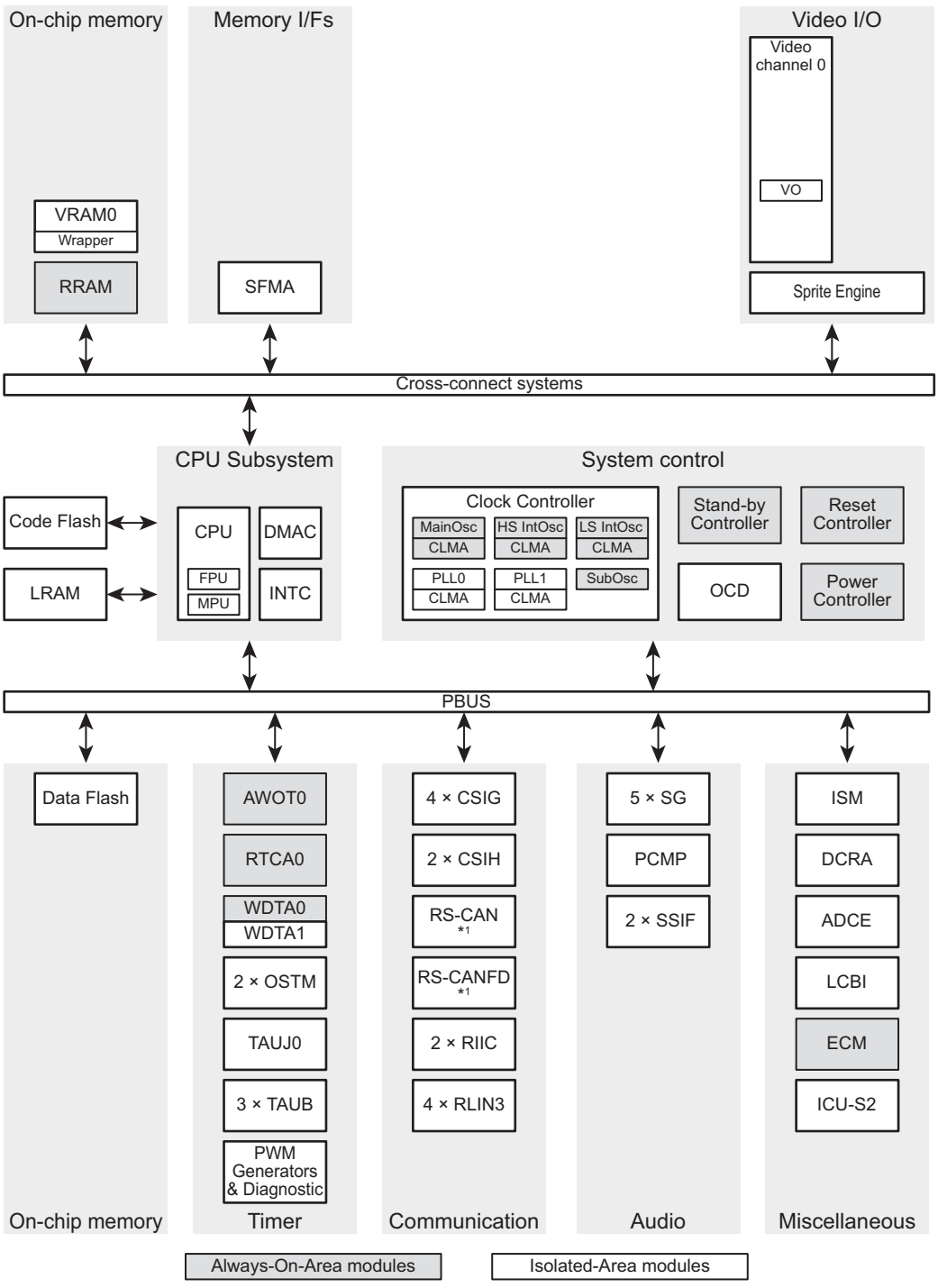
Note 2. AWO: Always-On-Area
ISO: Isolated-Area
GPIO: General purpose I/O port

Block Diagram



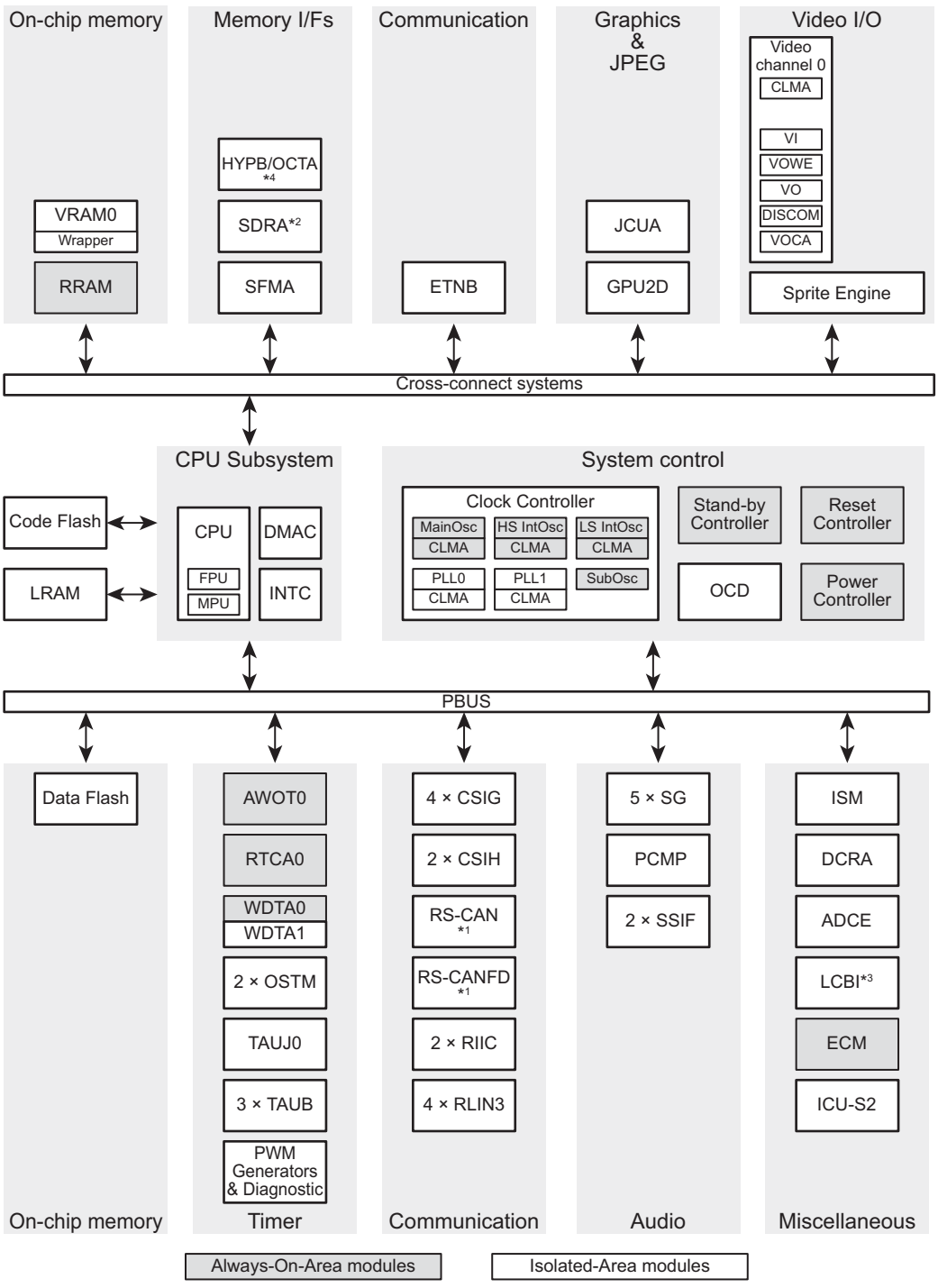
Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

D1L1 Block Diagram



Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

D1L2(H) Block Diagram



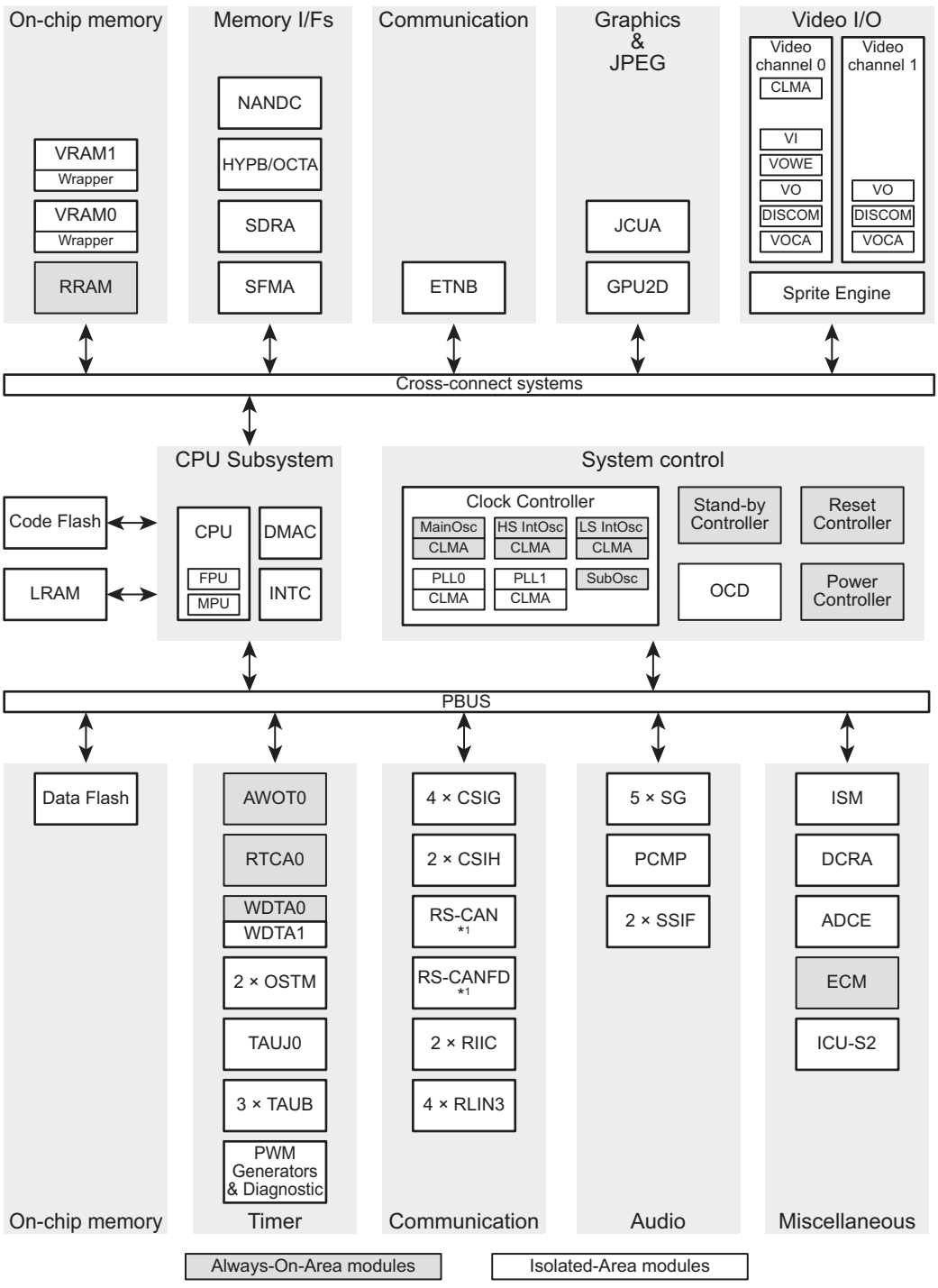
Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

Note 2. These modules are not available for the D1M1 devices.

Note 3. The LCBI module is not available for the D1M1H devices.

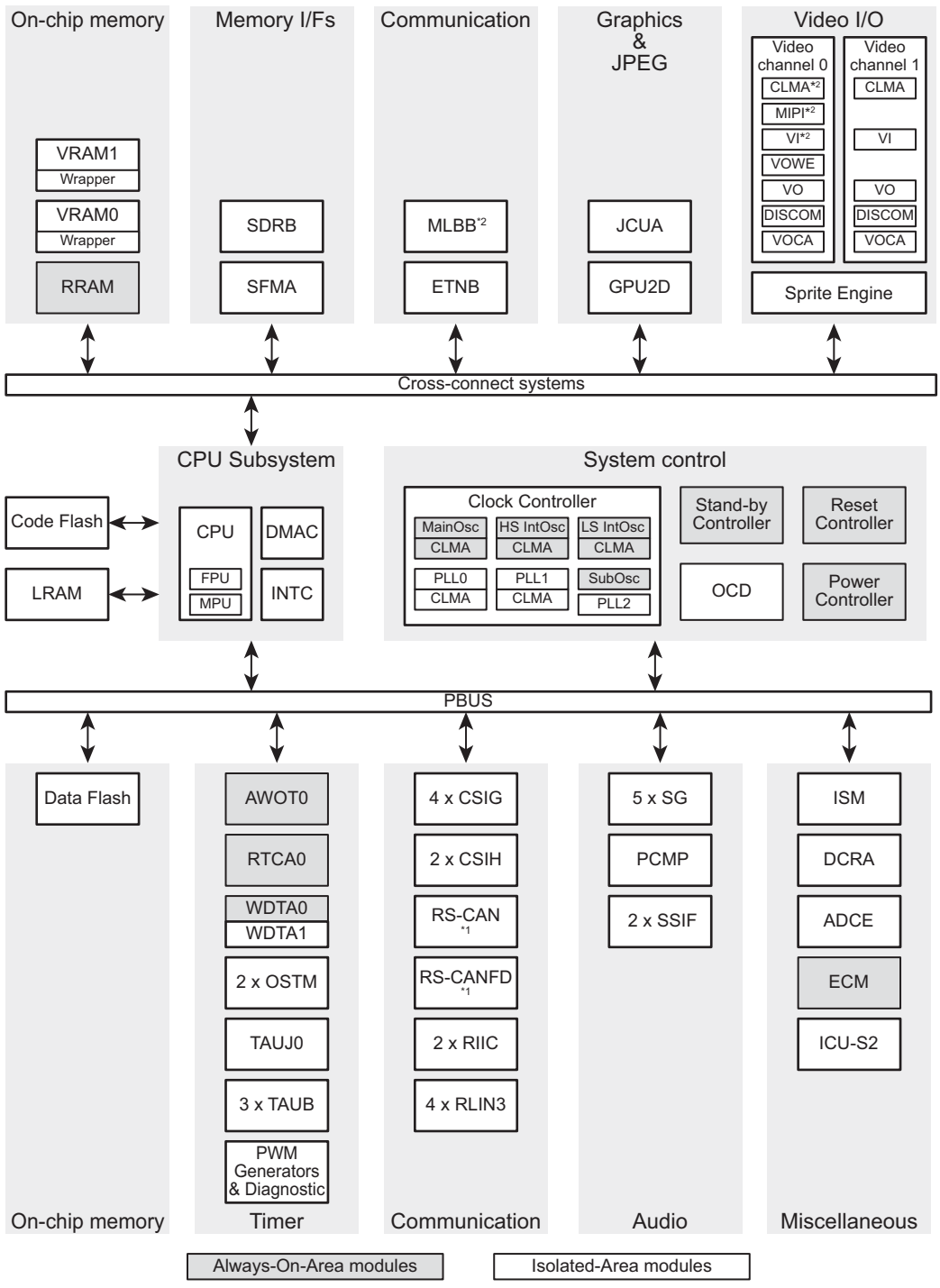
Note 4. These modules are not available for the D1M1(H) devices.

D1M1(H)/D1M1-V2 Block Diagram



Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

D1M1A Block Diagram



Note 1. Devices with RS-CAN or RS-CANFD interfaces have different product names, refer to **Ordering Information**.

Note 2. These modules are not available for the D1M2 devices.

D1M2(H) block diagram

Ordering Information

Series Name	Part Number	Renesas Order Code	Remarks
D1L1	R7F701401		D1L1 with RS-CAN I/F
	R7F701421		D1L1 with RS-CANFD I/F
D1L2	R7F701402		D1L2 with RS-CAN I/F
	R7F701422		D1L2 with RS-CANFD I/F
D1L2H	R7F701403		D1L2H with RS-CAN I/F
	R7F701423		D1L2H with RS-CANFD I/F
D1M1_3.75M	R7F701404		D1M1 with 3.75 MB Code Flash and RS-CAN I/F
D1M1_5M	R7F701405		D1M1 with 5 MB Code Flash and RS-CAN I/F
D1M1H_3.75M	R7F701406		D1M1H with 3.75 MB Code Flash and RS-CAN I/F
D1M1H_5M	R7F701407		D1M1H with 5 MB Code Flash and RS-CAN I/F
D1M2_3.75M	R7F701408		D1M2 with 3.75 MB Code Flash and RS-CAN I/F
	R7F701428		D1M2 with 3.75 MB Code Flash and RS-CANFD I/F
D1M2_5M	R7F701410		D1M2 with 5 MB Code Flash and RS-CAN I/F
	R7F701430		D1M2 with 5 MB Code Flash and RS-CANFD I/F
D1M2H_3.75M	R7F701411		D1M2H with 3.75 MB Code Flash and RS-CAN I/F
	R7F701431		D1M2H with 3.75 MB Code Flash and RS-CANFD I/F
D1M2H_5M	R7F701412		D1M2H with 5 MB Code Flash and RS-CAN I/F
	R7F701432		D1M2H with 5 MB Code Flash and RS-CANFD I/F
D1M1A	R7F701441		D1M1A with 4 MB Code Flash and RS-CAN I/F
	R7F701461		D1M1A with 4 MB Code Flash and RS-CANFD I/F
D1M1-V2	R7F701442		D1M1-V2 with 4 MB Code Flash and RS-CAN I/F
	R7F701462		D1M1-V2 with 4 MB Code Flash and RS-CANFD I/F

Pin Map

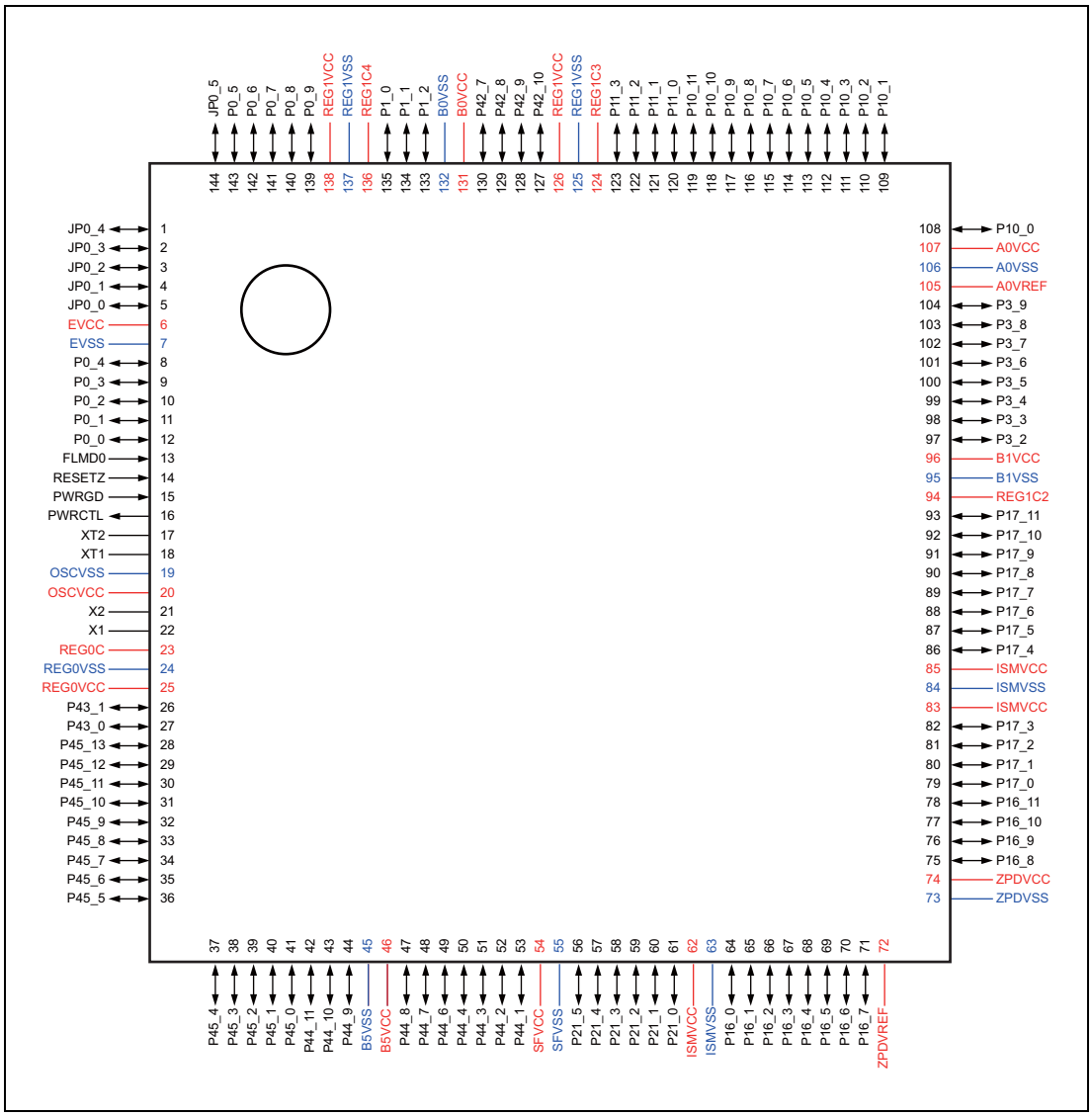


Figure A.1 D1L1(R7F701401) / D1L2 (R7F701402) (Top View)

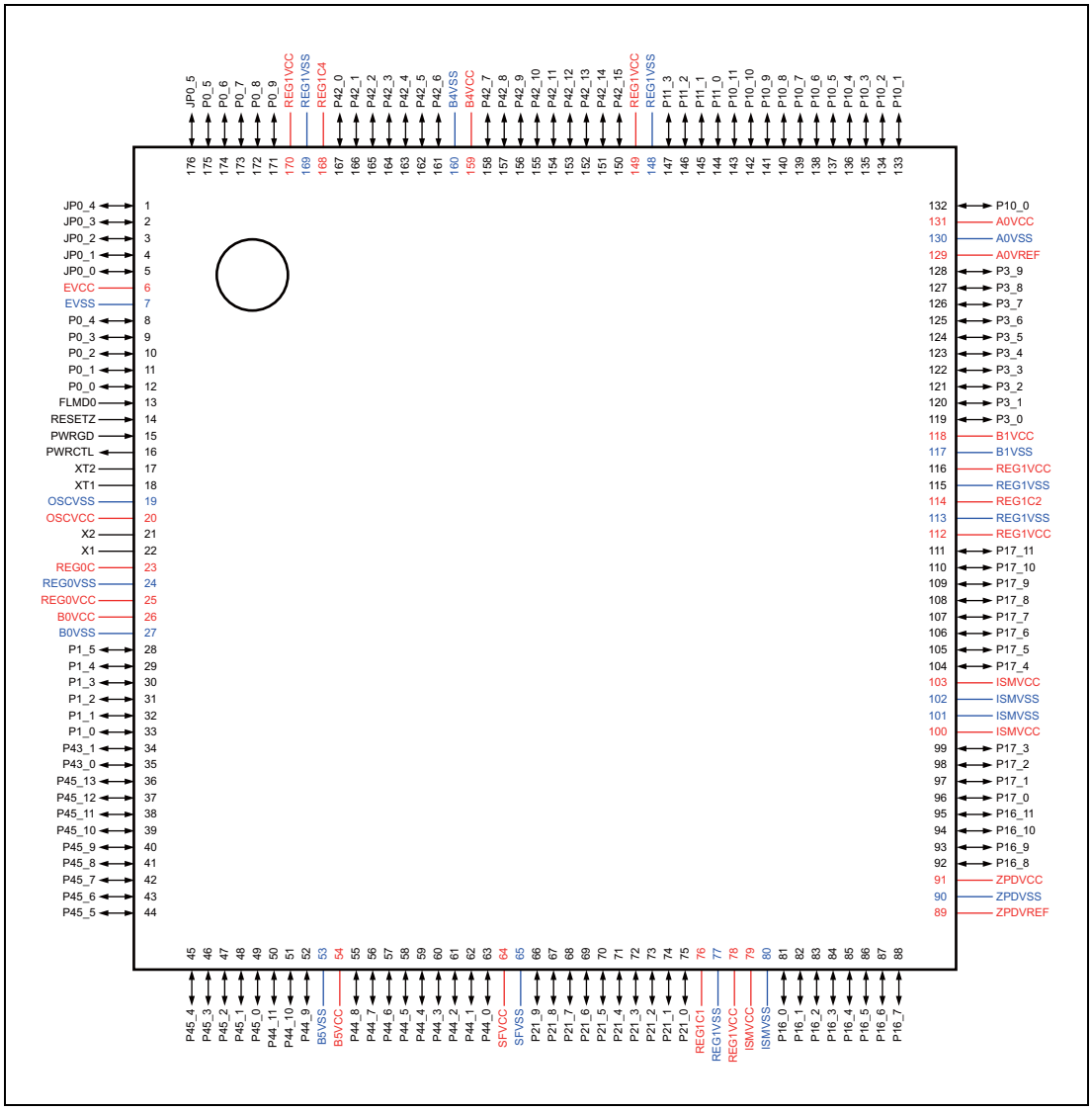


Figure B.2 D1L2H (R7F701403) / D1M1 (R7F701404/R7F701405) (Top View)

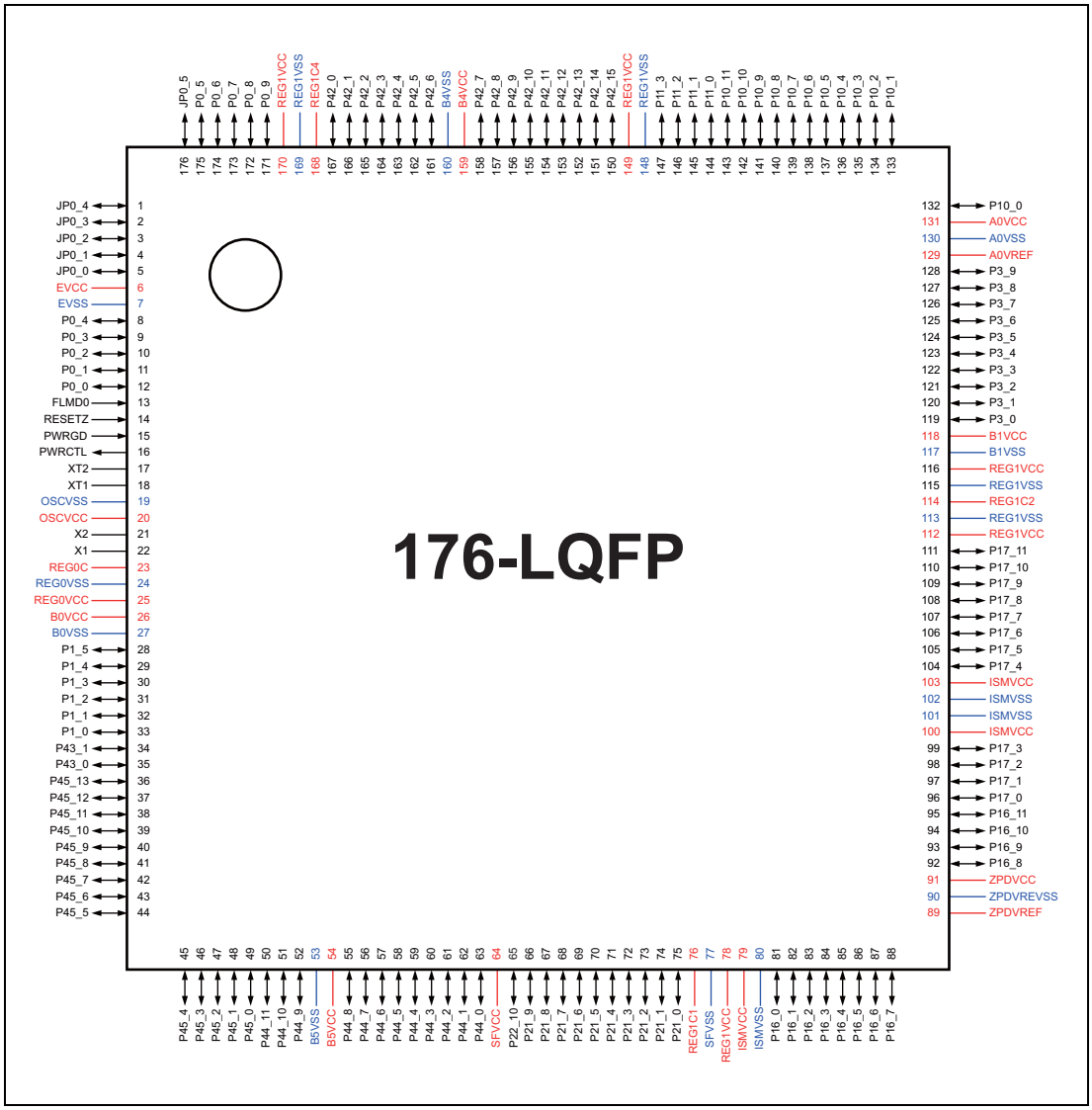


Figure C.3 D1M1-V2 (R7F701442) (Top View)

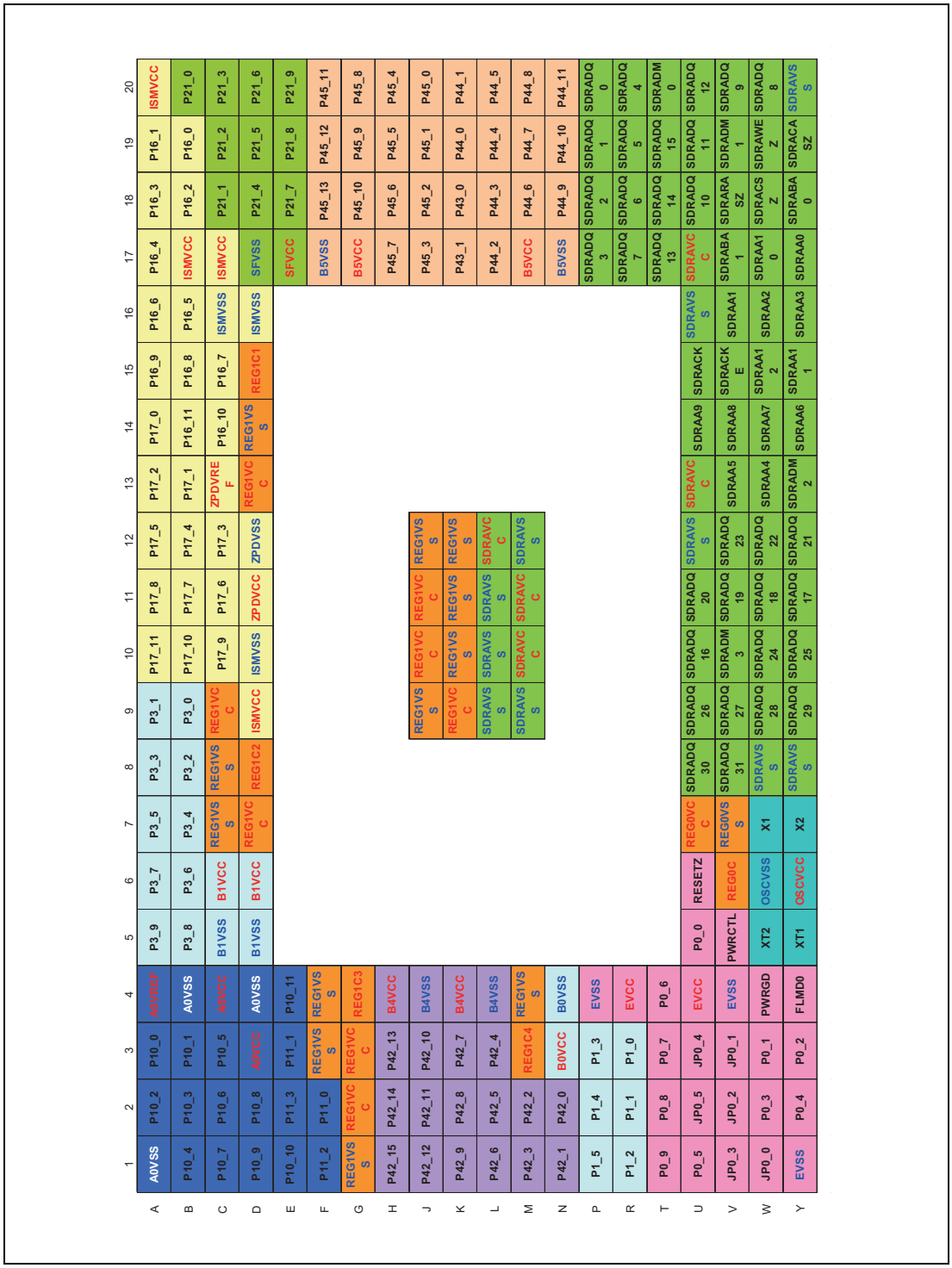


Figure D.4 D1M1H (R7F701406/R7F701407) (Top View)

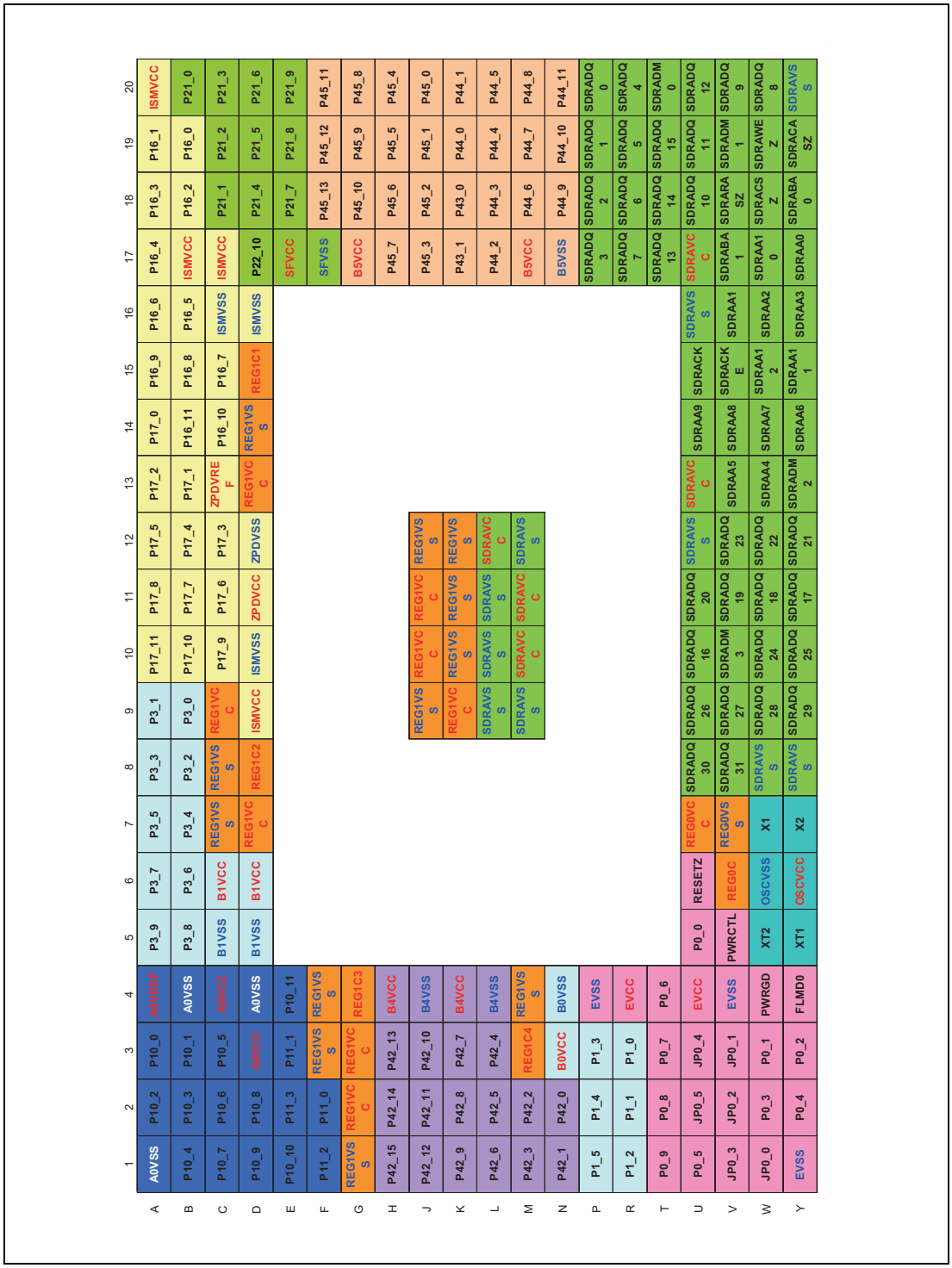


Figure E.5 D1M1A (R7F701441) (Top View)

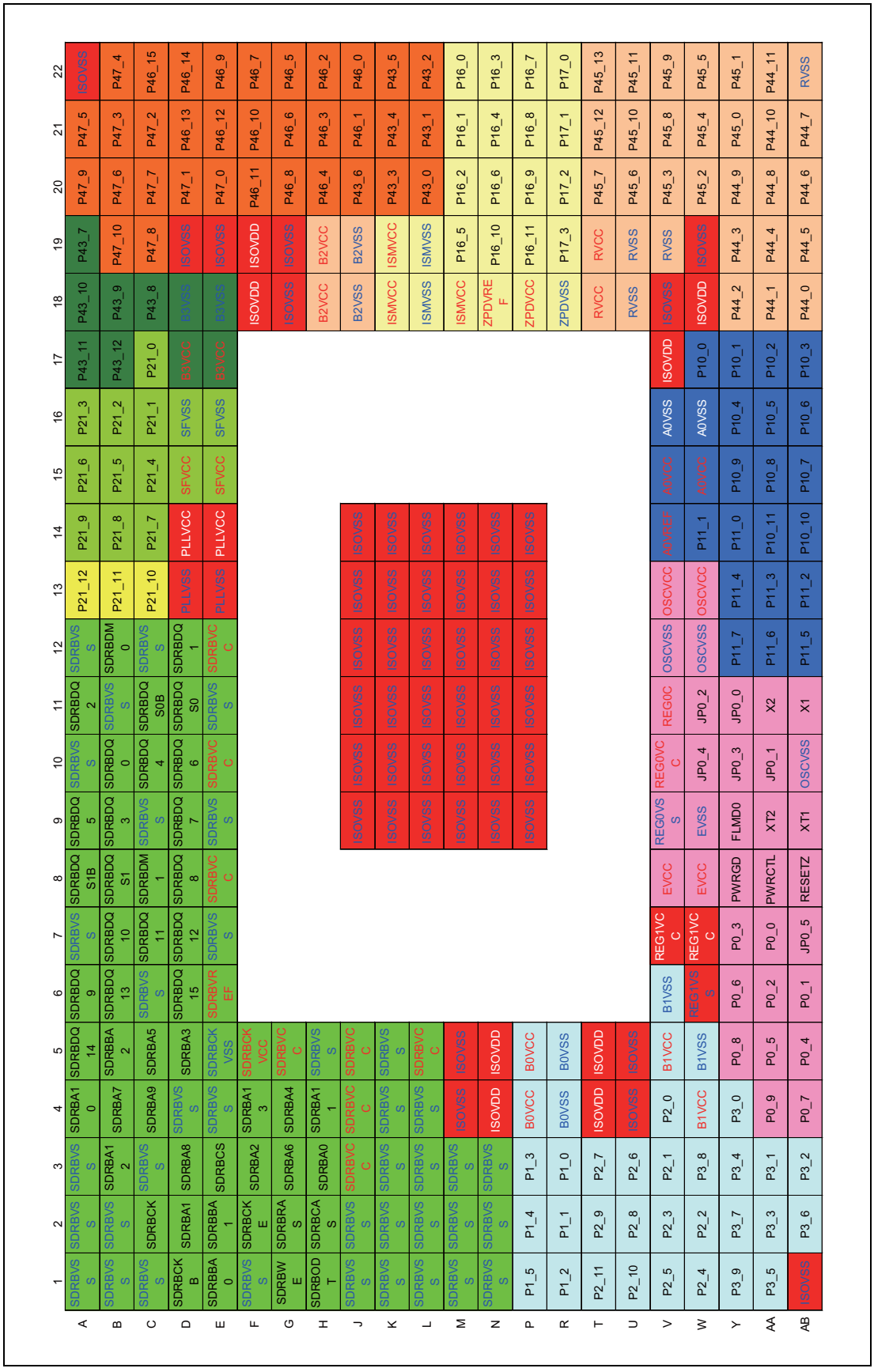


Figure F.6 D1M2 (R7F701408/R7F701410) (Top View)

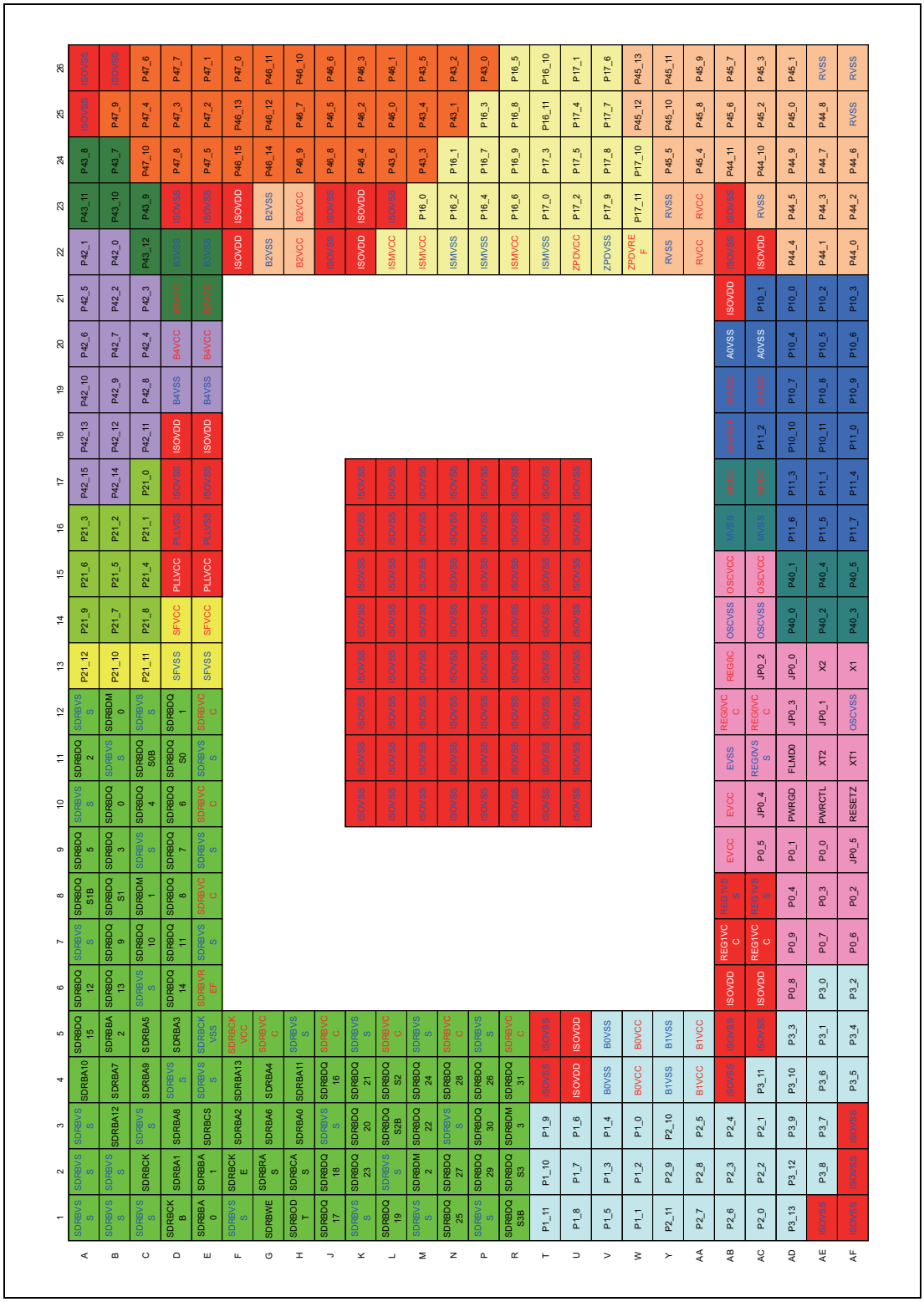


Figure G.7 D1M2H (R7F701412/R7F701411) (Top View)

Product Lineup

The RH850/D1x device family comprises several family members. An overview with the pin and package information is given in the following table:

	Family Member	Package
RH850/D1L1	R7F701401	QFP144
	R7F701421	
RH850/D1L2	R7F701402	QFP144
	R7F701422	
RH850/D1L2H	R7F701403	LQFP176
	R7F701423	
RH850/D1M1	R7F701404 / R7F701405	HLQFP176
RH850/D1M1H	R7F701406 / R7F701407	PBGA272
RH850/D1M2	R7F701408 / R7F701410	PBGA376
	R7F701428 / R7F701430	
RH850/D1M2H	R7F701411 / R7F701412	PBGA484
	R7F701431 / R7F701432	
RH850/D1M1A	R7F701441 / R7F701461	PBGA272
RH850/D1M1-V2	R7F701442 / R7F701462	LQFP176

Terms for Temperature

This specification describes a class of powerful devices that self-heating depend on the usage and thereby needed current consumption. Therefore this specification is based on two data for temperature:

- T_j: TJ or alternative T_j

is the chip junction temperature in [°C].

- Ta: TA or alternative Ta

is the ambient temperature (according to JEDEC standard JESD51-2A) in [°C] For details about the coherence between T_j and Ta see **Section 2.1, Junction-to-Ambient Resistance**.

Section 1 Electrical Specifications

1.1 Pin Groups

1.1.1 Power Supply Pins

Information about the power supply pin naming and the power supply schemes, i.e. the power supply pins and the modules they supply are provided in the "*User's Manual*" in section "*Power Supply*".

In this section the detailed distribution of dedicated power supply pins for certain I/O modules is provided. This covers different power supply pins that are indicated by different supply pin naming or different prefix. It covers also the supply of I/O modules that are supplied by several power supply pins that differ only for the suffix.

Pins having different suffix but same naming with same prefix are connected among each other but may have slightly different characteristic to parts of the I/O module. This is especially valid for devices with BGA packages, where the bonding between the die and the balls does not differ for the suffix. Nevertheless the electrical specification for each I/O pin does refer to a special power supply pin pair indicated by the complete naming including the suffix.

CAUTION

As not denoted otherwise this document neglects suffixes for power supply pins with same functions that can be treat as equal.

This document provides in the following sections;

- **Section 1.4, Absolute Maximum Ratings**
- **Section 1.5, General Operating Conditions**
- **Section 1.6, General IO Characteristic**

the voltage ranges of the power supply pins and port pins.

There the alias XyVCCn is often used to keep the operating condition description generic. Depending on the pin group supply the alias has to be replaced by the port buffer power.

1.1.2 Port Pins

A port buffer consists out of an output and input buffer with special features. Below abbreviation is used for the following port buffer tables.

1.1.2.1 Output Table Abbreviations

(1) Buffer Power Supply

Describes to which power supply pin pair the pin is connected.

(2) IOHold

The availability of this function to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty. In IOHOLD mode the I/O buffer maintains the level and drive strength it was in before entering this mode.

(3) Output

There exist different output buffer types.

- GP: General purpose output buffer.
  - Used for all general purpose I/O functions.
  - Provides frequency control option.
- HS: High speed output buffer.
  - High speed capability mainly used for SFMA.
- HD: High drivability output buffer.
  - With high drive capability that is mainly used to drive stepper motors.
- SSTL_18: DDR2-SDRAM output buffer
  - Used for DDR2-SDRAM interface.
  - SSTL_18 is compliant with JEDEC specification (JESD79-2F).
    - DRAM driver strength is corresponding to only “reduced strength”.
- RSDS: RSDS output buffer.
  - Low voltage differential buffer for RSDS video output.
- MLB: MediaLB output buffer.
  - MediaLB output buffer for MLB50 interface.
- AN: Analog output buffer.
  - Output buffer used w/ analog input buffer for A/D Converter.

The characteristic of each type is described in **Section 1.6, General IO Characteristic**.

The availability of the buffers to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the buffer is in addition initial activated by RESET an “R” or “L” is used instead of the “x”.

The “L” is used if the output direction of an output buffer is initial active low “R” is used instead of the “x”.

(4) Open Drain

The availability of the open drain emulation to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the open drain emulation is in addition initial activated by RESET an “R” is used instead of the “x”.

1.1.2.2 Input Table Abbreviations

(1) TriState

While this feature is active the input and output buffers are disabled (all PODCn_m = 1, PIBCn_m = 0). The ports enter high impedance status (HiZ). Thus these ports can be left unconnected, if they are not used.

A “R” in this column indicates that the output and input/output port is initial disabled by RESET and enters high impedance status (HiZ).

A “x” indicates that the feature is programmable during operation.

(2) Input

The characteristic of each type is described in **Section 1.6, General IO Characteristic** and can be selected by port control registers.

- CMOS1
- (LV)TTL
- Schmitt1
- Schmitt2
- Schmitt4
- SSTL_18
  - Used for DDR2-SDRAM interface.
  - SSTL_18 is compliant with JEDEC specification (JESD79-2F).
- MLB
- HS
- MIPI-CSI2

Not all input characteristics are available for each input port.

The availability of the input characteristic to each pin is marked with “x” in the associated column. For pins without this functionality the field is empty.

In case the input characteristic is in addition initial activated by RESET an “R”

is used instead of the “x”.

(3) Resistor

For input pins an internal pull-up (PU) and pull-down (PD) resistor can be selected. The availability is marked with “x” and “R” in the same meaning as above.

(4) Reset State

The output level status in case of active MCU reset.

“Z” means high impedance (output not driven).

“L” means low level (actively driven output).

(5) Drive Control

For output pins the drivability can be selected by PDSCn registers (=0 low speed, =1 high speed). In case the output drivability can be selected for a port it is indicated by “x” marking.

1.1.3 Pin Information for D1L1

Table 1.1 Pin Information for D1L1

Pin	Buffer Power Supply	Output								Open Drain	Tri State	Input									Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	AN	SSTL_18			CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
RESETZ	EV_{CC}	×								×					×									L	
FLMD0	EV_{CC}													×							×	R		Z	
PWRCTL	EV_{CC}	×																						L	
PWRGD	EV_{CC}													x										Z	
JP0_0	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_1	EV_{CC}	×								×	×					×					×	×		L	×*2
JP0_2	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_3	EV_{CC}	×								×	×					R	×				×	×		Z	
JP0_4	EV_{CC}	×								×	×					R	×				×	R		Z	
JP0_5	EV_{CC}	×								×	×					×					×	×		Z	×*2
P0	EV_{CC}	×	×							×	×			R		×	×				×	×	×	Z	×
P1	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P3	$B1V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P10	$A0V_{CC}$							×		×	×	×										×		Z	
P11	$A0V_{CC}$							×		×	×	×										×		Z	
P16	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P17	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P21(D1L1)	SFV_{CC}		×							×	×	×									×	×		Z	
P42	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P43(D1L1)	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P44	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P45	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×

Note 1. P16/P17 are driven by selection1 capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

1.1.4 Pin Information for D1L2, D1L2H

Table 1.2 Pin Information for D1L2, D1L2H

Pin	Buffer Power Supply	Output								Open Drain	Tri State	Input									Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	AN	SSTL_18			CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
$\overline{\text{RESET}}$	EV_{CC}	×								×					×									L	
FLMD0	EV_{CC}													×							×	R		Z	
PWRCTL	EV_{CC}	×																						L	
PWRGD	EV_{CC}													×										Z	
JP0_0	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_1	EV_{CC}	×								×	×					×					×	×		L	×*2
JP0_2	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_3	EV_{CC}	×								×	×					R	×				×	×		Z	
JP0_4	EV_{CC}	×								×	×					R	×				×	R		Z	
JP0_5	EV_{CC}	×								×	×					×					×	×		Z	×*2
P0	EV_{CC}	×	×							×	×			R		×	×				×	×	×	Z	×
P1	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P3	$B1V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P10	$A0V_{CC}$							×		×	×	×										×		Z	
P11	$A0V_{CC}$							×		×	×	×										×		Z	
P16	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P17	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P21	SFV_{CC}			×						×	×		×								×	×		Z	
P42	D1L2: $B0V_{CC}$ D1L2H: $B4V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P43	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P44	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P45	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×

Note 1. P16/P17 are driven by selection1 capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

1.1.5 Pin Information for D1M1, D1M1H

Table 1.3 Pin Information for D1M1, D1M1H

Pin	Buffer Power Supply	Output										Input									Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	AN	SSTL_18	Open Drain	Tri State	CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
$\overline{\text{RESET}}$	EV_{CC}	×								×					×									L	
FLMD0	EV_{CC}													×							×	R		Z	
PWRCTL	EV_{CC}	×																						L	
PWRGD	EV_{CC}													×										Z	
JP0_0	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_1	EV_{CC}	×								×	×					×					×	×		L	×*2
JP0_2	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_3	EV_{CC}	×								×	×					R	×				×	×		Z	
JP0_4	EV_{CC}	×								×	×					R	×				×	R		Z	
JP0_5	EV_{CC}	×								×	×					×					×	×		Z	×*2
P0	EV_{CC}	×	×							×	×			R		×	×				×	×	×	Z	×
P1	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P3	$B1V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P10	$A0V_{CC}$							×		×	×	×										×		Z	
P11	$A0V_{CC}$							×		×	×	×										×		Z	
P16	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P17	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P21	SFV_{CC}			×						×	×		×								×	×		Z	
P42	$B4V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P43	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P44	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P45	$B5V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
SDRAA12 to SDRAA0*3	SDRAVCC			×							×	×												L	
SDRABA1 to SDRABA0*3	SDRAVCC			×							×	×												L	
SDRACK*3	SDRAVCC			×							×	×												L	
SDRACKE*3	SDRAVCC			×							×	×												L	
SDRACS*3	SDRAVCC			×							×	×												L	
SDRACAS*3	SDRAVCC			×							×	×												L	
SDRARAS*3	SDRAVCC			×							×	×												L	
SDRAWE*3	SDRAVCC			×							×	×												L	
SDRADM3 to SDRADM0*3	SDRAVCC			×							×	×												L	
SDRADQ31 to SDRADQ0*3	SDRAVCC			×							×	×												Z	

Note 1. P16/P17 are driven by selection1 capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

Note 3. SDRA only valid for D1M1H

1.1.6 Pin Information for D1M2, D1M2H

Table 1.4 Pin Information for D1M2, D1M2H (1/2)

Pin	Buffer Power Supply	Output								Open Drain	Tri State	Input									Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	AN	SSTL_18			CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
RESET	EV_{CC}	×								×					×									L	
FLMD0	EV_{CC}													×							×	R		Z	
PWRCTL	EV_{CC}	×																						L	
PWRGD	EV_{CC}													×										Z	
JP0_0	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_1	EV_{CC}	×								×	×					×					×	×		L	×*2
JP0_2	EV_{CC}	×								×	×			R		×	×				×	×		Z	
JP0_3	EV_{CC}	×								×	×					R	×				×	×		Z	
JP0_4	EV_{CC}	×								×	×					R	×				×	R		Z	
JP0_5	EV_{CC}	×								×	×					×					×	×		Z	×*2
P0	EV_{CC}	×	×							×	×			R		×	×				×	×	×	Z	×
P1	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P2	$B0V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P3	$B1V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P10	$A0V_{CC}$							×		×	×	×										×		Z	
P11	$A0V_{CC}$							×		×	×	×										×		Z	
P16	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P17	$ISMV_{CC}$				×					×	×	×		R		×							×	L*1	×
P21_0 to P21_9	SFV_{CC}			×						×	×		×							×	×	×		Z	
P21_10 to P21_12	SFV_{CC}					×				×	×		×							×	×	×		Z	
P40	MV_{CC}	×	×							×	×	×							×		×	×		Z	×
P42	$B4V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P43_0 to P43_6	$B2V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P43_7 to P43_12	$B3V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P44	RV_{CC}	×	×				×			×	×	×									×	×		Z	×
P45	RV_{CC}	×	×				×			×	×	×									×	×		Z	×
P46	$B2V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
P47	$B2V_{CC}$	×	×							×	×	×		R		×					×	×	×	Z	×
SDRBA0 to SDRBA13	$SDRBV_{CC}$								×															L	
SDRBBA0 to SDRBBA3	$SDRBV_{CC}$								×															L	
SDRBCK	$SDRBCKV_{CC}$								×															L	
SDRBCKB	$SDRBCKV_{CC}$								×															L	
SDRBCKE	$SDRBV_{CC}$								×															L	
SDRBODT	$SDRBV_{CC}$								×															L	
SDRBCS	$SDRBV_{CC}$								×															H	
SDRBCAS	$SDRBV_{CC}$								×															H	
SDRBRAS	$SDRBV_{CC}$								×															H	
SDRBWE	$SDRBV_{CC}$								×															H	
SDRBDM0 to SDRBDM3	$SDRBV_{CC}$								×															H	

Table 1.4 Pin Information for D1M2, D1M2H (2/2)

Pin	Buffer Power Supply	Output								Open Drain	Tri State	Input									Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	AN	SSTL_18			CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
SDRBDQ0 to SDRBDQ31	$SDRBV_{CC}$								×									×						Z	
SDRBDQS0 to SDRBDQS3	$SDRBV_{CC}$								×									×						Z	
SDRBDQS0B to SDRBDQS3B	$SDRBV_{CC}$								×									×						Z	

Note 1. P16/P17 are driven by selection1 capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

1.1.7 Pin Information for D1M1A, D1M1-V2

Table 1.5 Pin Information for D1M1A, D1M1-V2

Pin	Buffer Power Supply	Output									Open Drain	Tri State	Input								Resistor			Reset State	Drive Control
		GP (slow)	GP (fast)	HS	HD	MLB	RSDS	Open LDI	AN	SSTL_18			CMOS1	HS	Schmitt1	Schmitt2	Schmitt4	TTL	SSTL_18	mipi-CSI2	MLB	PU	PD	IO-Hold		
$\overline{\text{RESET}}$	EV_{CC}	×									×					×									L	
FLMD0	EV_{CC}														×							×	R		Z	
PWRCTL	EV_{CC}	×																							L	
PWRGD	EV_{CC}														×										Z	
JP0_0	EV_{CC}	×									×	×			R		×	×				×	×		Z	
JP0_1	EV_{CC}	×									×	×					×					×	×		L	×*2
JP0_2	EV_{CC}	×									×	×			R		×	×				×	×		Z	
JP0_3	EV_{CC}	×									×	×					R	×				×	×		Z	
JP0_4	EV_{CC}	×									×	×					R	×				×	R		Z	
JP0_5	EV_{CC}	×									×	×					×					×	×		Z	×*2
P0	EV_{CC}	×	×								×	×			R		×	×				×	×	×	Z	×
P1	$B0V_{CC}$	×	×								×	×	×		R		×					×	×	×	Z	×
P3	$B1V_{CC}$	×	×								×	×	×		R		×					×	×	×	Z	×
P10	$A0V_{CC}$								×		×	×	×										×		Z	
P11	$A0V_{CC}$								×		×	×	×										×		Z	
P16	$ISMV_{CC}$				×						×	×	×		R		×							×	L*1	×
P17	$ISMV_{CC}$				×						×	×	×		R		×							×	L*1	×
P21, P22	SFV_{CC}			×							×	×		×								×	×		Z	
P42	$B4V_{CC}$	×	×								×	×	×		R		×					×	×	×	Z	×
P43	$B5V_{CC}$	×	×								×	×	×		R		×					×	×	×	Z	×
P44	$B5V_{CC}$	×	×								×	×	×		R		×					×	×	×	Z	×
P45	$B5V_{CC}$	×	×					×			×	×	×		R		×					×	×	×	Z	×
SDRAA12 to SDRAA0*3	SDRAVCC			×								×	×												L	
SDRABA1 to SDRABA0*3	SDRAVCC			×								×	×												L	
SDRACK*3	SDRAVCC			×								×	×												L	
SDRACKE*3	SDRAVCC			×								×	×												L	
SDRACS*3	SDRAVCC			×								×	×												L	
SDRACAS*3	SDRAVCC			×								×	×												L	
SDRARAS*3	SDRAVCC			×								×	×												L	
SDRAWE*3	SDRAVCC			×								×	×												L	
SDRADM3 to SDRADM0*3	SDRAVCC			×								×	×												L	
SDRADQ31 to SDRADQ0*3	SDRAVCC			×								×	×												Z	

Note 1. P16/P17 are driven by selection1 capability at Reset State.

Note 2. JP0_1/JP0_5 has JPDSC. However, AC/DC spec cover slow mode only.

Note 3. SDRA only valid for D1M1A.

1.2 Classification of Testing

Besides testing the specified parameters directly or indirectly at mass production state there is also the method of special product characterization and design simulation. Such parameters are marked in the classification tag column “CT” of each electrical parameter table with the associated classification tag.

Table 1.6 Parameter Classifications

Classification Tag		
Abbr	**Tag Name**	**Tag Description**
PC	Product Characterization	Those parameters are achieved by device characterization by measuring a statistically relevant sample size across process variations.
DS	Design Simulation	Those parameters are derived from simulations.

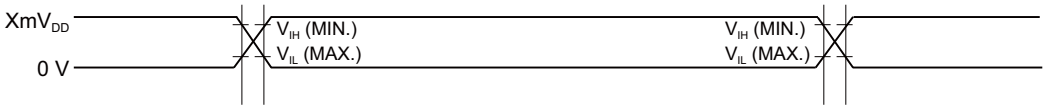
1.3 General Measurement Conditions

As not otherwise denoted the general measurement condition for testing are

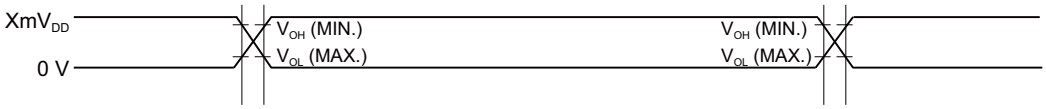
Condition: T_J = –40 to +T_{Jmax}
VSS = OSCVSS = REGnVSS = PLLVSS = EVSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = MVSS = RVSS = SDRBVSS = SDRAVSS = SFVSS = ISOVSS = 0 V

1.3.1 AC Characteristic Measurement Condition

(1) AC Test Input Measurement Points



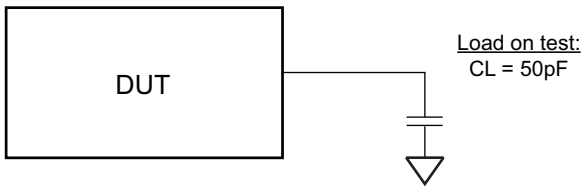
(2) AC Test Output Measurement Points



CAUTIONS

1. If not other denoted output timings are not valid for open drain setting.
2. If not other denoted input timings are valid for CMOS1 level.
   - Using the Schmitt 1/2/4 input characteristics results in a different delay time. If Schmitt 1/2/4 is used, the difference of the propagation delay timing to CMOS1 has to be added. For port input propagation delay timing please refer to Port Input Characteristics.
   - For special AC test conditions (i.e DDR2SDRAM,RSDS,MIPI-CSI2), please refer to the individual sections and check under which test conditions the individual AC specifications are valid.

(3) Load Conditions



NOTES

1. As not otherwise denoted the standard load condition for testing is
   - 1 nF for Intelligent stepper motor driver (HD type)
   - 50 pF for all lower speed port buffer (GP type in slow mode)
   - 30 pF for video and SFMA (D1L1) I/O ports. (GP type in fast mode)
   - 15 pF for high speed port buffers (HS type).
2. For critical AC timing specifications (mostly of interfaces with crucial round- trip delay calculations), please refer to the individual sections and check under which test conditions the individual AC specifications are valid.

1.4 Absolute Maximum Ratings

1.4.1 Definition of Absolute Maximum Ratings

Absolute maximum ratings are values of voltage, current, temperature, power dissipation etc., which must not be exceeded at any time, otherwise deterioration or destruction of the device may take place. Maximum values and limits given in this document should be taken into consideration anytime when using the device.

(1) Maximum Temperature Ratings

Specifies the absolute maximum limitation of operating and storage temperature.

NOTE

The device's function is not guaranteed outside of the specified maximum temperature ratings.

(2) Maximum Voltage Ratings

Specifies the absolute maximum limitation of supply and input voltages.

NOTE

The device's function is not guaranteed outside of the specified operating range and below the specified maximum voltage ratings.

(3) Maximum Current Ratings

Specifies the absolute maximum limitation of input and output currents.

1.4.2 Thermal Characteristics

Table 1.7 Thermal Characteristics

Parameter	Symbol	Condition	T_{Jmin}	TYP.	T_{Jmax}	Unit
Storage temperature	T_{STGB}	D1L1	–55		150	°C
		D1L2	–55		150	
		D1L2H	–55		150	
		D1M1	–55		150	
		D1M1H	–55		150	
		D1M2	–55		150	
		D1M2H	–55		150	
		D1M1A	–55		150	
		D1M1-V2	–55		150	
Operating temperature	T_{OPR}	D1L1	–40		150	°C
		D1L2	–40		150	
		D1L2H	–40		150	
		D1M1	–40		150	
		D1M1H	–40		150	
		D1M2	–40		150	
		D1M2H	–40		150	
		D1M1A	–40		150	
		D1M1-V2	–40		150	

1.4.3 Supply Voltages

Condition: T_j = –40 to +T_{Jmax}
REG0VSS = OSCVSS = EVSS = REG1VSS = ISOVSS = PLLVSS = BnVSS = RVSS = MVSS = SFVSS = SDRBVSS = SDRAVSS = ISMVSS = ZPDVSS = A0VSS = 0 V

Table 1.8 VCC / VDD Data

Parameter	Symbol*1,*2	Condition	Ratings	Unit
Always-On-Area	REG0VCC		–0.5 to 6.5	V
	OSCVCC		–0.5 to 6.5	V
	EVCC		–0.5 to 6.5	V
System	REG1VCC (D1M1(H)/D1M1A/D1M1-V2)		–0.5 to 4.6 V	V
	REG1VCC (D1M2(H)/D1Lx)		–0.5 to 6.5 V	V
	ISOVDD		–0.5 to 1.8	V
	PLLVCC		–0.5 to 6.5	V
Internal voltage regulator Ports	REG0C, REG1C*3		–0.5 to 1.8	V
	B0VCC		–0.5 to 6.5	V
	B1VCC		–0.5 to 6.5	V
	B2VCC		–0.5 to 6.5	V
	B3VCC		–0.5 to 6.5	V
	B4VCC		–0.5 to 6.5	V
	B5VCC		–0.5 to 6.5	V
	RVCC		–0.5 to 4.6	V
	MVCC		–0.5 to 4.6	V
	SFVCC (D1Mx/D1L2)		–0.5 to 4.6	V
	SFVCC (D1L1)		–0.5 to 6.5	V
	SDRBVCC / SDRBCKVCC		–0.5 to 2.3	V
	SDRAVCC / SDRACKVCC		–0.5 to 4.6	V
Stepper Motor Controller, Zero point detection circuit	ISMVCC		–0.5 to 6.5	V
	ZPDVCC		–0.5 to 6.5	V
	ZPDVREF	ZPDVREF<=ZPDVCC ZPDVREF<=ISMVCC	–0.5 to 6.5	V
A/D Converter	A0VCC	A0VCC>=ISOVDD	–0.5 to 6.5	V
	A0VREF	A0VREF<= A0VCC	–0.5 to 6.5	V

Note 1. As long as not otherwise noted this specification does not differ between pins with different suffix for the symbol.

Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.

Note 3. These pins are for special use only and should not be used for other connections than specified. Pins are operated with the internal generated core voltage.

Table 1.9 VSS Data

Parameter	Symbol[*1,*2]	Condition	Ratings	Unit
Always-On-Area	REG0VSS	reference ground potential	0	V
	OSCVSS		–0.5 to 0.5	V
	EVSS		–0.5 to 0.5	V
System	REG1VSS		–0.5 to 0.5	V
	ISOVSS		–0.5 to 0.5	V
	PLLVSS		–0.5 to 0.5	V
Ports	B0VSS		–0.5 to 0.5	V
	B1VSS		–0.5 to 0.5	V
	B2VSS		–0.5 to 0.5	V
	B3VSS		–0.5 to 0.5	V
	B4VSS		–0.5 to 0.5	V
	B5VSS		–0.5 to 0.5	V
	RVSS		–0.5 to 0.5	V
	MVSS		–0.5 to 0.5	V
	SFVSS		–0.5 to 0.5	V
	SDRBVSS		–0.5 to 0.5	V
	SDRAVSS		–0.5 to 0.5	V
Stepper Motor Controller, Zero point detection circuit	ISMVSS		–0.5 to 0.5	V
	ZPDVSS		–0.5 to 0.5	V
A/D Converter	A0VSS		–0.5 to 0.5	V

Note 1. As long as not otherwise noted this specification does not differ between pins with different suffix for the symbol.

Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.

1.4.4 Port Voltage

Condition: T_j = –40 to +T_{Jmax}

Table 1.10 Port Input Voltage

Parameter		Symbol[*1,*2]	Condition	Ratings	Unit
Input voltage	Pins supplied by EVCC	V_{I0}	V_{I0} < EVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by BnVCC	V_{I1}	V_{I1} < BnVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by RVCC	V_{I2}	V_{I2} < RVCC + 0.5 V	–0.5 to 4.6	V
	Pins supplied by MVCC	V_{I3}	V_{I3} < MVCC + 0.5 V	–0.5 to 4.6	V
	Pins supplied by SFVCC	V_{I4}	V_{I4} < SFVCC + 0.5 V (D1Mx/D1L2)	–0.5 to 4.6	V
			V_{I4} < SFVCC + 0.5 V (D1L1)	–0.5 to 6.5	V
	Pins supplied by SDRBVCC	V_{I5}	V_{I5} < SDRBVCC + 0.5 V	–0.5 to 2.3	V
	Pins supplied by SDRAVCC	V_{I5}	V_{I5} < SDRAVCC + 0.5 V	–0.5 to 4.6	V
	Pins supplied by ISMVCC	V_{I6}	V_{I6} < ISMVCC + 0.5 V	–0.5 to 6.5	V
	Pins supplied by A0VCC	V_{I7}	V_{I7} < A0VCC + 0.5 V	–0.5 to 6.5	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The symbol reflects all supplies within D1x. Therefore not each symbol is available for each product.

1.4.5 Port Currents

The port currents describe the allowed currents that can be sourced from / sunken into a port pin respectively a port pin supply group.

Condition: T_j = –40 to +T_{Jmax}
REG0VSS = OSCVSS = EVSS = REG1VSS = ISOVSS = PLLVSS = BnVSS = RVSS = MVSS = SFVSS = SDRBVSS = ISMVSS = ZPDVSS = A0VSS = 0 V

CAUTION

The currents in the customer's application must not exceed the absolute maximum current ratings as specified in **Table 1.11, Low Level Output Current** and **Table 1.12, High Level Output Current** below.

For the calculation of the total power dissipation of a device (Ptot) also the power consumption of the IO pins (PIO) has to be considered. PIO is dependent on the customer's application. Therefore, it has to be taken care that with the resulting PIO the Ptot does not exceed the given limits of T_{Jmax}.

Table 1.11 Low Level Output Current (1/2)

Parameter	Symbol[*1]	Condition	Average	MAX.	Unit
Pins supplied by EVSS	IOL0	1pin	—	10	mA
		Sum of all absolute IOL0 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B0VSS	IOL1	1pin	—	10	mA
		Sum of all absolute IOL1 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B1VSS	IOL2	1pin	—	10	mA
		Sum of all absolute IOL2 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B2VSS	IOL3	1pin	—	10	mA
		Sum of all absolute IOL3 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B3VSS	IOL4	1pin	—	10	mA
		Sum of all absolute IOL4 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B4VSS	IOL5	1pin	—	10	mA
		Sum of all absolute IOL5 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by B5VSS	IOL6	1pin	—	10	mA
		Sum of all absolute IOL6 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by SDRBVSS	IOL7b	1pin	—	10	mA
		Sum of all absolute IOL7b of pins supplied by same supply pin pair	—	60	mA
Pins supplied by SDRAVSS	IOL7a	1 pin	—	10	mA
		Sum of all absolute IOL7a of pins supplied by same supply pin pair	—	60	mA
Pins supplied by RVSS	IOL8	1 pin	—	10	mA
		Sum of all absolute IOL8 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by MVSS	IOL9	1 pin	—	10	mA
		Sum of all absolute IOL9 of pins supplied by same supply pin pair	—	60	mA

Table 1.11 Low Level Output Current (2/2)

Parameter	Symbol[*1]	Condition	Average	MAX.	Unit
Pins supplied by SFVSS	IOL10	1 pin	—	10	mA
		Sum of all absolute IOL10 of pins supplied by same supply pin pair	—	60	mA
Pins supplied by ISMVSS (PDSCn = 0)	IOL11	1 pin	—	10	mA
		Sum of all absolute IOL11 of pins supplied by same supply pins	—	60	mA
Pins supplied by ISMVSS (PDSCn = 1)	IOL11	1 pin (T_j = –40°C)	52	60	mA
		1 pin (T_j = 25°C)	39	45	mA
		1 pin (T_j = 125°C)	32	40	mA
		1 pin (T_j = 150°C)	30	38	mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = –40°C)	441		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 25°C)	351		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 125°C)	288		mA
		Sum of all absolute IOL11 of pins supplied by all supply pins (T_j = 150°C)	270		mA
Pins supplied by A0VSS	IOL12	1 pin	—	10	mA
		Sum of all absolute IOL12 of pins supplied by same supply pin pair	—	60	mA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Table 1.12 High Level Output Current (1/2)

Parameter	Symbol*1	Condition	Average	Peak	Unit
Pins supplied by EVCC	IOH0	1 pin	—	–10	mA
		Sum of all absolute IOH0 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B0VCC	IOH1	1 pin	—	–10	mA
		Sum of all absolute IOH1 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B1VCC	IOH2	1 pin	—	–10	mA
		Sum of all absolute IOH2 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B2VCC	IOH3	1 pin	—	–10	mA
		Sum of all absolute IOH3 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B3VCC	IOH4	1 pin	—	–10	mA
		Sum of all absolute IOH4 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B4VCC	IOH5	1 pin	—	–10	mA
		Sum of all absolute IOH5 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by B5VCC	IOH6	1 pin	—	–10	mA
		Sum of all absolute IOH6 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by SDRBVCC	IOH7b	1 pin	—	–10	mA
		Sum of all absolute IOH7b of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by SDRAVCC	IOH7a	1 pin	—	–10	mA
		Sum of all absolute IOH7a of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by RVCC	IOH8	1 pin	—	–10	mA
		Sum of all absolute IOH8 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by MVCC	IOH9	1 pin	—	–10	mA
		Sum of all absolute IOH9 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by SFVCC	IOH10	1 pin	—	–10	mA
		Sum of all absolute IOH10 of pins supplied by same supply pin pair	—	–60	mA
Pins supplied by ISMVCC (PDSCn = 0)	IOH11	1 pin	—	–10	mA
		Sum of all absolute IOH11 of pins supplied by same supply pins	—	–60	mA

Table 1.12 High Level Output Current (2/2)

Parameter	Symbol*1	Condition	Average	Peak	Unit
Pins supplied by ISMVCC (PDSCn = 1)	IOH11	1 pin (T_j = –40°C)	–52	–60	mA
		1 pin (T_j = 25°C)	–39	–45	mA
		1 pin (T_j = 125°C)	–32	–40	mA
		1 pin (T_j = 150°C)	–30	–38	mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = –40°C)	–441		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 25°C)	–351		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 125°C)	–288		mA
		Sum of all absolute IOH11 of pins supplied by all supply pins (T_j = 150°C)	–270		mA
Pins supplied by A0VCC	IOH12	1 pin	—	–10	mA
		Sum of all absolute IOH12 of pins supplied by same supply pin pair	—	–60	mA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.5 General Operating Conditions

1.5.1 Requirements for External Power Supply Connections

The customer has to ensure a low resistive connection of all XyVSS pins on the PCB. This specification denotes ground supply pins as:

- VSS = OSCVSS = PLLVSS = REGnVSS = EVSS = BnVSS = ISMVSS = ZPDVSS = A0VSS = MVSS = RVSS = SDRBVSS = SDRAVSS = ISOVSS = 0 V

The customer has to ensure a low resistive connection of all same XyVCC pins on the PCB. This specification denotes power supply pins as:

- REGnVCC, REG0C, OSCVCC, PLLVCC, EVCC, BnVCC, RVCC, MVCC, SFVCC, ISMVCC, A0VCC, A0VREF, ZPDVCC, ZPDVREF, SDRBVCC, SDRAVCC

1.5.2 Power Area Definition:

- AWO = Powered
  - REG0VCC = Powered
  - EVCC = Powered
- ISO = powered
  - ISOVDD = Powered
  - REG1VCC = Powered
  - PLLVCC = Powered

NOTE

"Powered" means to supply a voltage according to supply voltage range specified in **Section 1.5.11, Supply Voltage**.

1.5.3 Power-Up/-Down Ramp (RH850/D1M1A, D1M1(H), D1M1-V2, D1Lx)

For a proper start-up (power-up) and switch-off (power-down) of the device it is mandatory that the customer applies an ext. system supply voltage (XyVCC), with a ramp that is equal or slower than specified below.

- XyVCC means each power domain

Table 1.13 Power-up Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC ramp-up time	T_{pupr0}	0 V to 3.1 V	0.00		500	V/ms
REG1VCC ramp-up time		0 V to 3.1 V	0.00		400	V/ms
POC0RESET release to PWRCTL assert					100	µs
OSCVCC ramp-up after or equal REG0VCC	T_{puosc}	0 V to 3.0 V	0.0			µs
A0VCC/A0VREF ramp-up before REG1VCC	T_{pud1}	0 V to 3.0 V	0.0			µs
REG1VCC ramp-up after PWRCTL	T_{pud3}	0 V to 3.0 V	0.0			µs
SDRAVCC ramp-up after REG1VCC	T_{pud4}	0 V to 3.0 V	0.0			µs
A0VCC/BnVCC/ISMVCC/SFVCC/ZPDVCC ramp-up after REG0VCC	T_{pudio}	0 V to 3.0 V	0.0			µs
PWRGD ramp-up after REG1VCC	T_{pgdu}	Low to High	0.0			µs
Power-up delay (release timing of ISORES)	T_{pudly}	POC0RES			0.8 (HS IntOSC)	ms
		except POC0RES			0.5 (HS IntOSC)	ms
					1.2 (LS IntOSC)	ms
PWRGD pulse width	T_{wpg}		10.0			µs
PWRCTL assert from wake-up trigger receive	T_{pctl}		10.0		100	µs

Table 1.14 Power-down Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC shutdown time	T_{pdpr0}	3.0 V to 0 V	0.00		500	V/ms
REG1VCC shutdown time		3.0 V to 0 V	0.00		400	V/ms
OSCVCC shutdown before REG0VCC	T_{pdosc}	3.0 V to 0 V	0.0			µs
A0VCC/A0VREF shutdown from PWRCTL	T_{pdd1}	3.0 V to 0 V	0.0			µs
REG1VCC shutdown after PWRCTL	T_{pdd3}	3.0 V to 0 V	0.0			µs
SDRAVCC shutdown before REG1VCC	T_{pdd4}	3.0 V to 0 V	–10.0			ms
A0VCC/BnVCC/ISMVCC/SFVCC/ZPDVCC shutdown before REG0VCC	T_{pddio}	3.0 V to 0 V	–10.0			ms

When PWRGD become to fail (low), then internal reset asserted. But, REG1VCC need to keep >2.7v during following period.

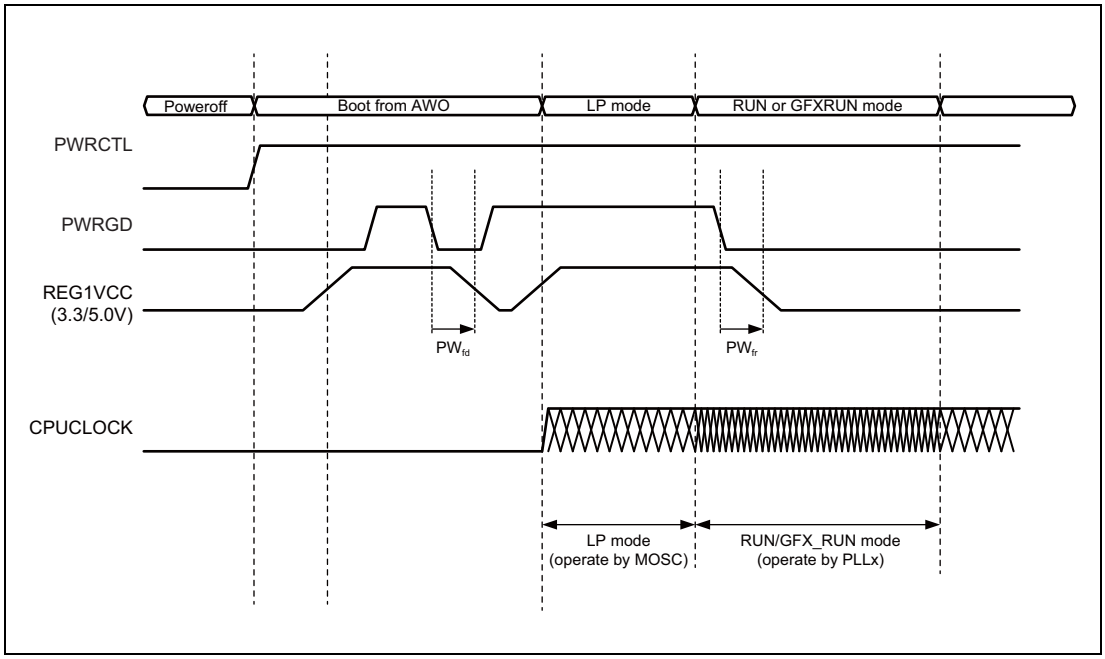


Figure 1.1 PWRGD/REG1VCC Failure

Table 1.15 Power Supply Failure

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PWRGD shutdown to REG1VCC fail	PW_{fr}	LP/RUN mode	0			µs
	PW_{fd}	Except LP/ RUN mode	0			µs

Note: PWRGD shutdown to REG1VCC fail is not relevant in case D1M1(H)/D1M1A/D1Lx successfully entered the deep-stop mode. For this case please refer to **Figure 1.5**.

Table 1.16 Power Supply Ripple Specs

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ripple of all supply	R_{rpl}		–10		10	%
Maximum rating of all slope	R_{slp}				100	V/s

1.5.4 Power-Up/-Down Ramp (RH850/D1M2(H))

For a proper start-up (power-up) and switch-off (power-down) of the device it is mandatory that the customer applies an ext. system supply voltage (XyVCC), with a ramp that is equal or slower than specified below.

- XyVCC means each power domain

Table 1.17 Power-up Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC ramp-up time	T_{pupr0}	0 V to 3.1 V	0.00		500	V/ms
POC0RESET release to PWRCTL assert					100	µs
OSCVCC ramp-up after or equal REG0VCC	T_{puosc}	0 V to 3.0 V	0.0			µs
A0VCC/A0VREF ramp-up before ISOVDD	T_{pud1}	0 V to 3.0 V	0.0			µs
ISOVDD ramp-up after PWRCTL	T_{pud2}	0 V to 1.15 V	0.0			µs
PLLVCC/REG1VCC ramp-up after PWRCTL	T_{pud3}	0 V to 3.0 V	0.0			µs
SDRBVCC ramp-up start after ISOVDD is stable*2	T_{pud4}	0 V to 1.7 V	0.0			µs
A0VCC/BnVCC/ISMVCC/SFVCC/RVCC/MVCC/ ZPDVCC ramp-up after REG0VCC	T_{pudio}	0 V to 3.0 V	0.0			µs
PWRGD ramp-up after ISOVDD	T_{pgdu}	Low to High	0.0			µs
Power-up delay (release timing of ISORES)	T_{pudly}	POC0RES, ISOPWRES			41	ms
		except POC0RES, ISOPWRES			17*1	ms
PWRGD pulse width	T_{wpg}		10.0			µs
PWRCTL assert from wake-up trigger receive	T_{pctl}		10.0		100	µs

Note 1. It depends on PWRGD_CNT register setting (default = 17 ms).
Note 2. SDRBVCC need start supply after the ISOVDD rampup to 1.15 V

Table 1.18 Power-down Restrictions

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REG0VCC/EVCC shutdown time	T_{pdpr0}	3.1 V to 0 V	0.00		500	V/ms
OSCVCC shutdown before REG0VCC	T_{pdosc}	3.0 V to 0 V	0.0			µs
A0VCC/A0VREF shutdown from ISOVDD	T_{pdd1}	3.0 V to 0 V	0.0			µs
ISOVDD shutdown after PWRCTL	T_{pdd2}	1.15 V to 0 V	0.0			µs
PLLVCC/REG1VCC shutdown after PWRCTL	T_{pdd3}	3.0 V to 0 V	0.0			µs
SDRBVCC shutdown before ISOVDD	T_{pdd4}	1.7 V to 0 V	–10.0			ms
A0VCC/BnVCC/ISMVCC/SFVCC/RVCC/MVCC/ ZPDVCC shutdown before REG0VCC	T_{pddio}	3.0 V to 0 V	–10.0			ms
PWRGD shutdown after PWRCTL deassertion	T_{pgdd}	High to Low	0.0			ms

When PWRGD become to fail (low), then internal reset asserted. But, ISOVDD need to keep >1.15v during following period.

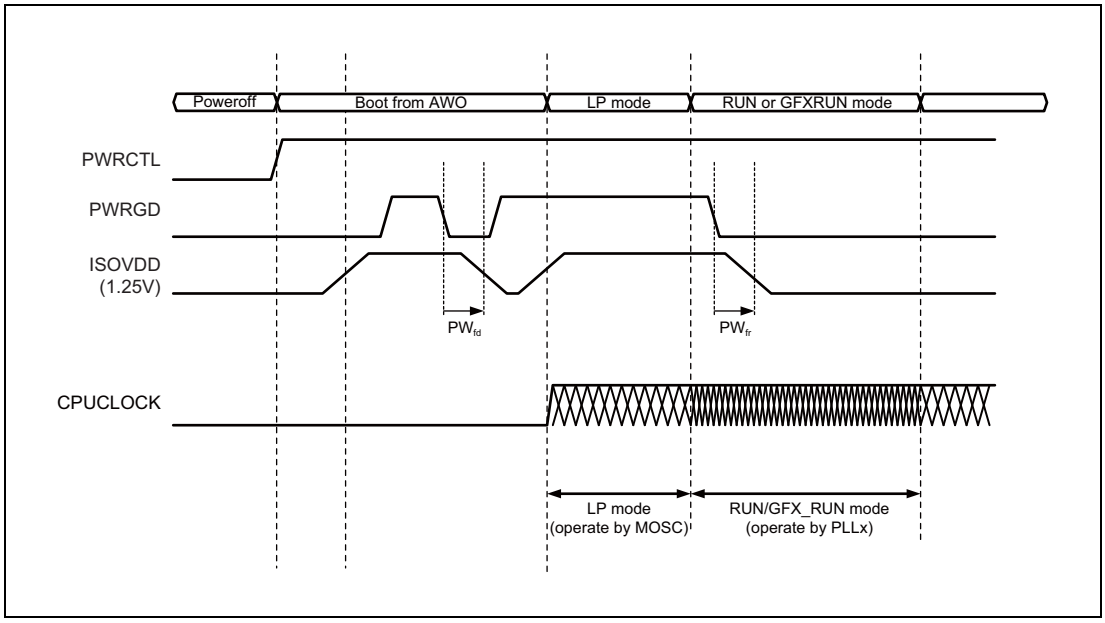


Figure 1.2 PWRGD/ISOVDD Failure

Table 1.19 Power Supply Failure

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PWRGD shutdown to ISOVDD fail	PW_{fr}	LP/RUN mode	100			µs
	PW_{fd}	Except LP/ RUN mode	700			µs

Note:
- When PW_{fr} / PW_{fd} timing is not kept (i.e. below 100 µs / 700 µs) the following 3 items may occur during this unintended power drop; 1) Write access to AWO-area may write incorrect value to AWO macro, 2) Write access to RRAM might invalidate RRAM data content, 3) The Debugger (OCD) might be disconnected.This is detectable by the reset cause “Power-On-Clear 0 reset” (POC0RES), after that the MCU shall re-setup AWO area macros and invalidated RRAM content same as for a regular POC0RES (i.e. reset caused by AWO power fail).
- PWRGD shutdown to ISOVDD fail is not relevant in case D1M2(H) successfully entered the deep-stop mode. For this case please refer to **Figure 1.8**.

Table 1.20 Power Supply Ripple Specs

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Ripple of all supply	R_{rpl}		–10		10	%
Maximum rating of all slope	R_{slp}				100	V/s

1.5.5 Power-Up/Down Sequences of External Supply Voltages (RH850/D1M1A, D1M1(H), D1M1-V2, D1Lx)

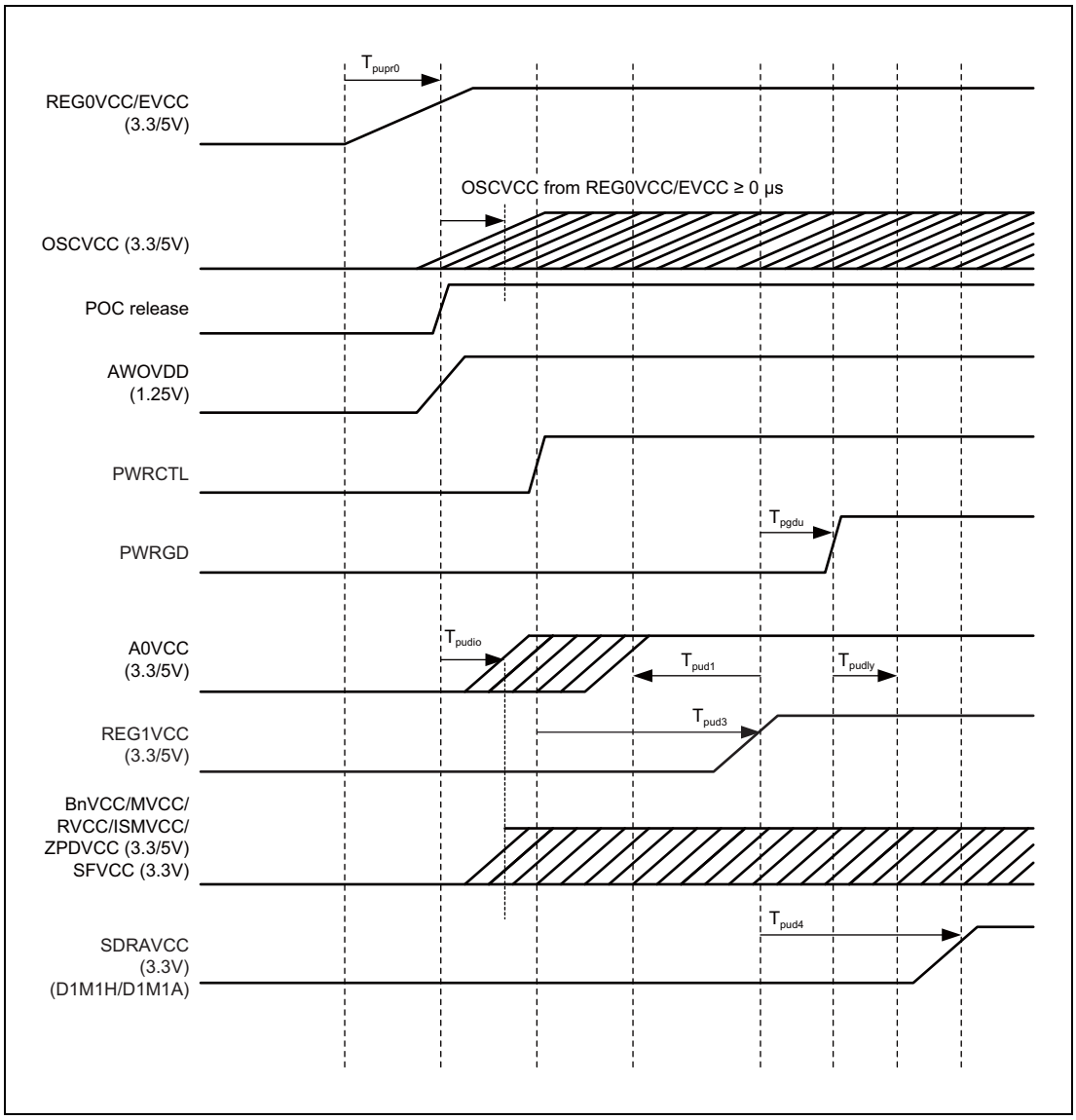


Figure 1.3 Power-up Sequence

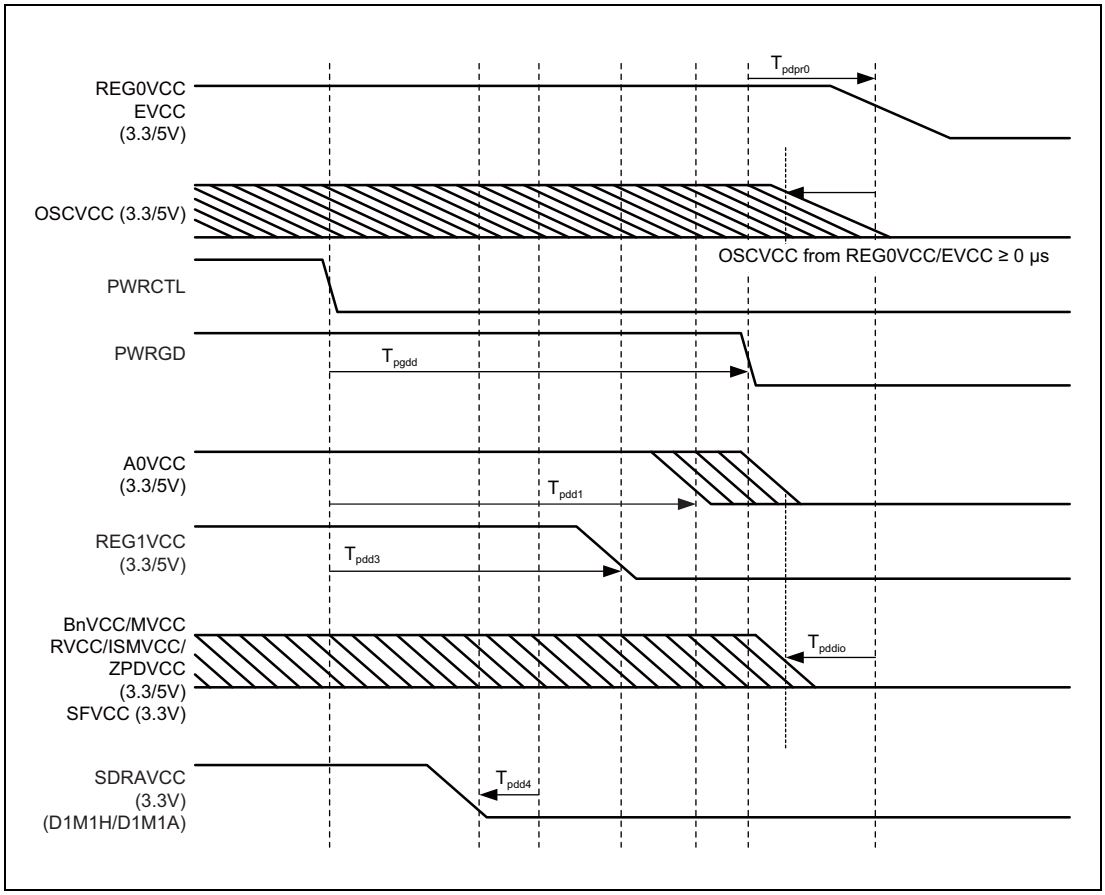


Figure 1.4 Power-down Sequence

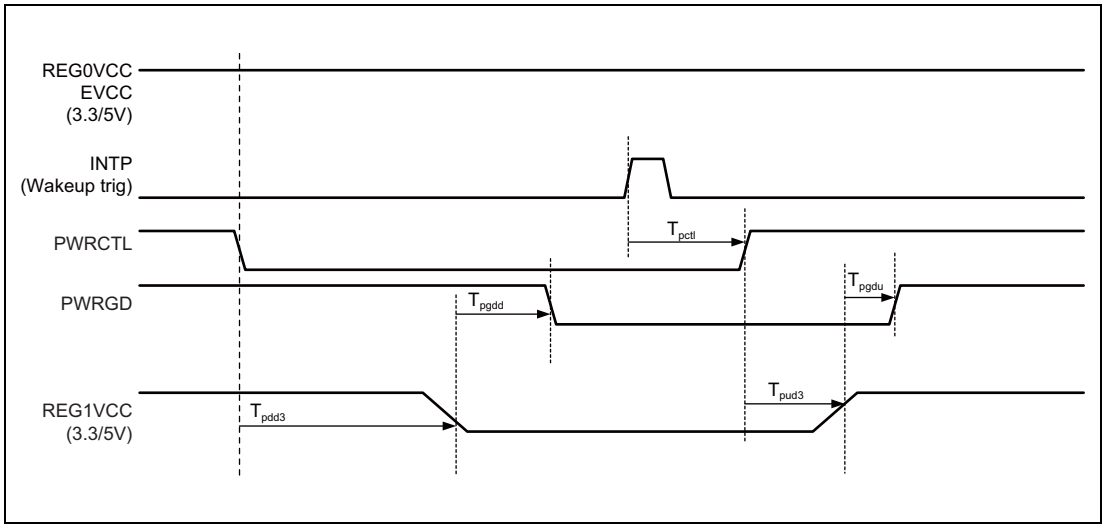


Figure 1.5 DeepSTOP Enter/Exit Sequence

NOTE

- When REG0VCC is supplied, it is possible to supply REG1VCC, regardless of the PWRCTL signal state.
- In case of successful DeepSTOP entry (when MCU has set PWRCTL = L), there is no restriction for PWRGD shutdown timing. Because of that a value for the parameter T_{pgdd} is not specified.

Please refer to the **Section 1.14.8, Stand-by Current Consumption (RH850/D1Lx,D1Mx)** and consider the leakage currents of active domain for this case.

1.5.6 Power-Up/Down Sequences of External Supply Voltages (RH850/D1M2(H))

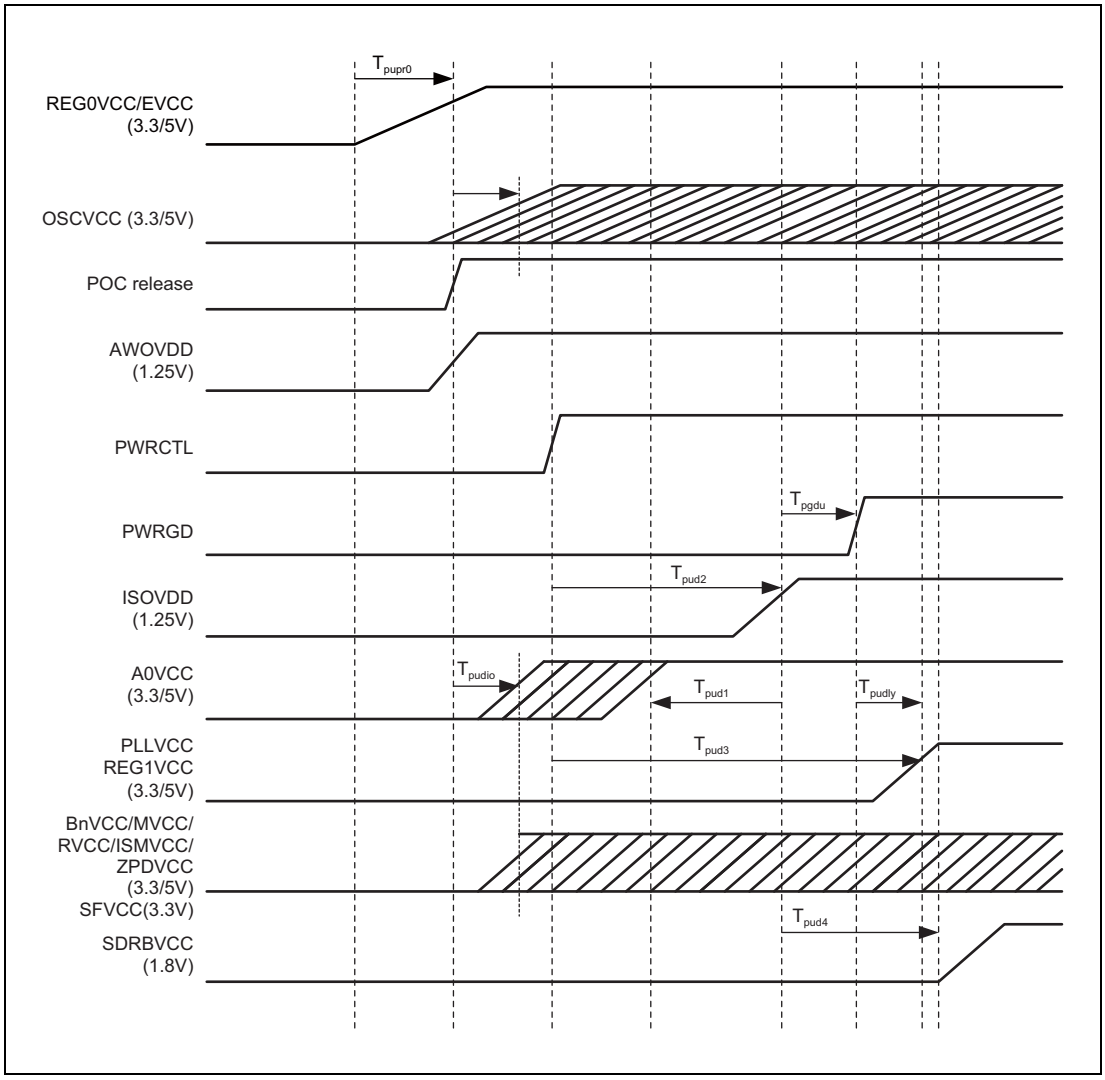


Figure 1.6 Power-up Sequence

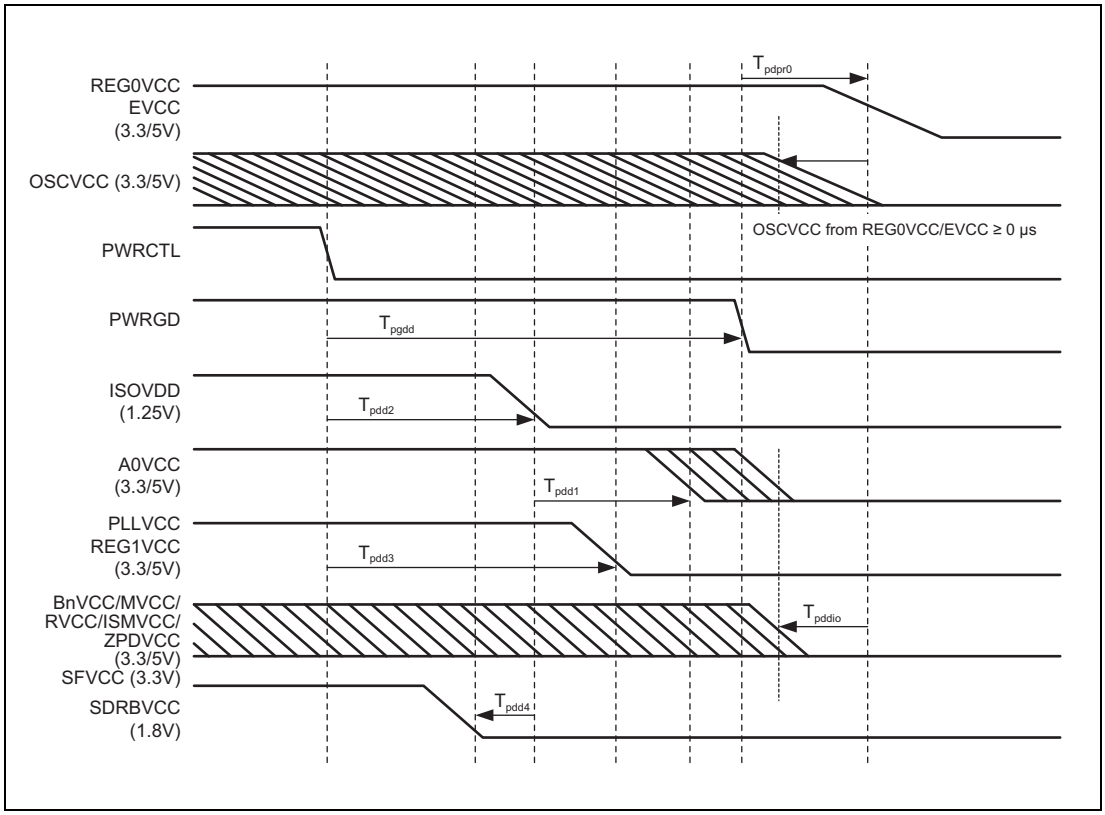


Figure 1.7 Power-down Sequence

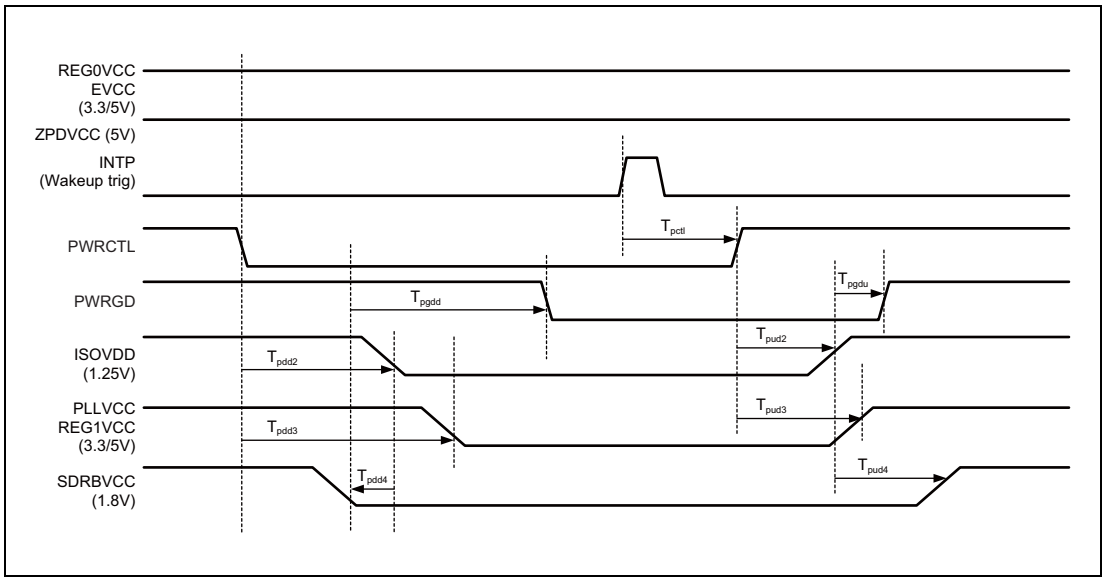


Figure 1.8 DeepSTOP Enter/Exit Sequence

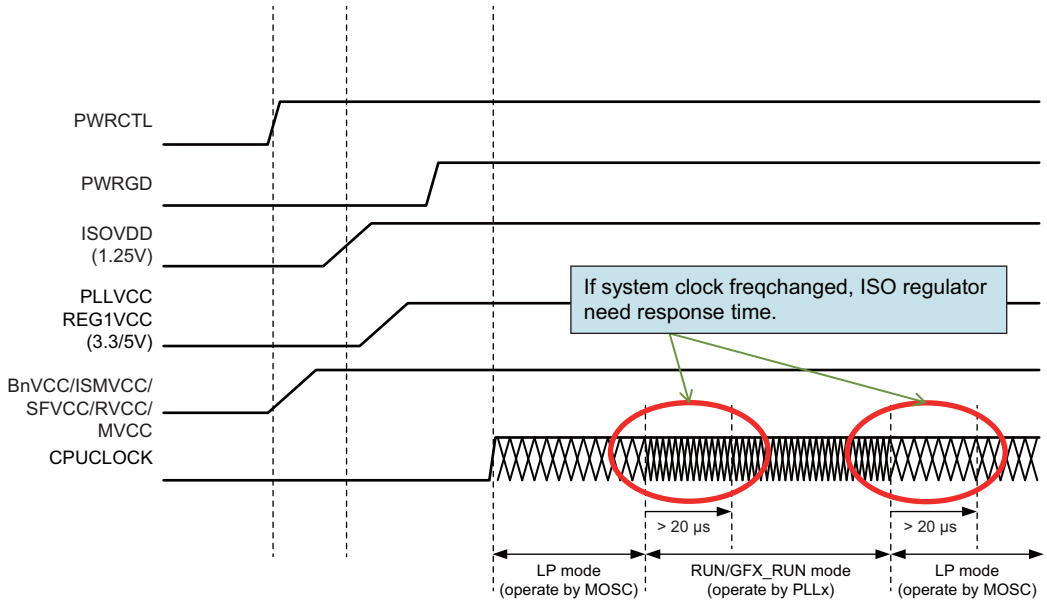
NOTE

- When REG0VCC is supplied, it is possible to supply ISOVDD, PLLVCC and REG1VCC, regardless of the PWRCTL signal state.
- In case of successful DeepSTOP entry (when MCU has set PWRCTL = L), there is no restriction for PWRGD shutdown timing. Because of that a value for the parameter T_{pgdd} is not specified.

Please refer to the **Section 1.14.8, Stand-by Current Consumption (RH850/D1Lx,D1Mx)** and consider the leakage currents of active domain for this case.

1.5.7 Clock Source Change Behavior

D1x must keep the blank time when PLL on/off switching (more than 20 µs).



Note: Changing of one or all of this clock tree registers below must not be done again within a period of 20 µs after last change.

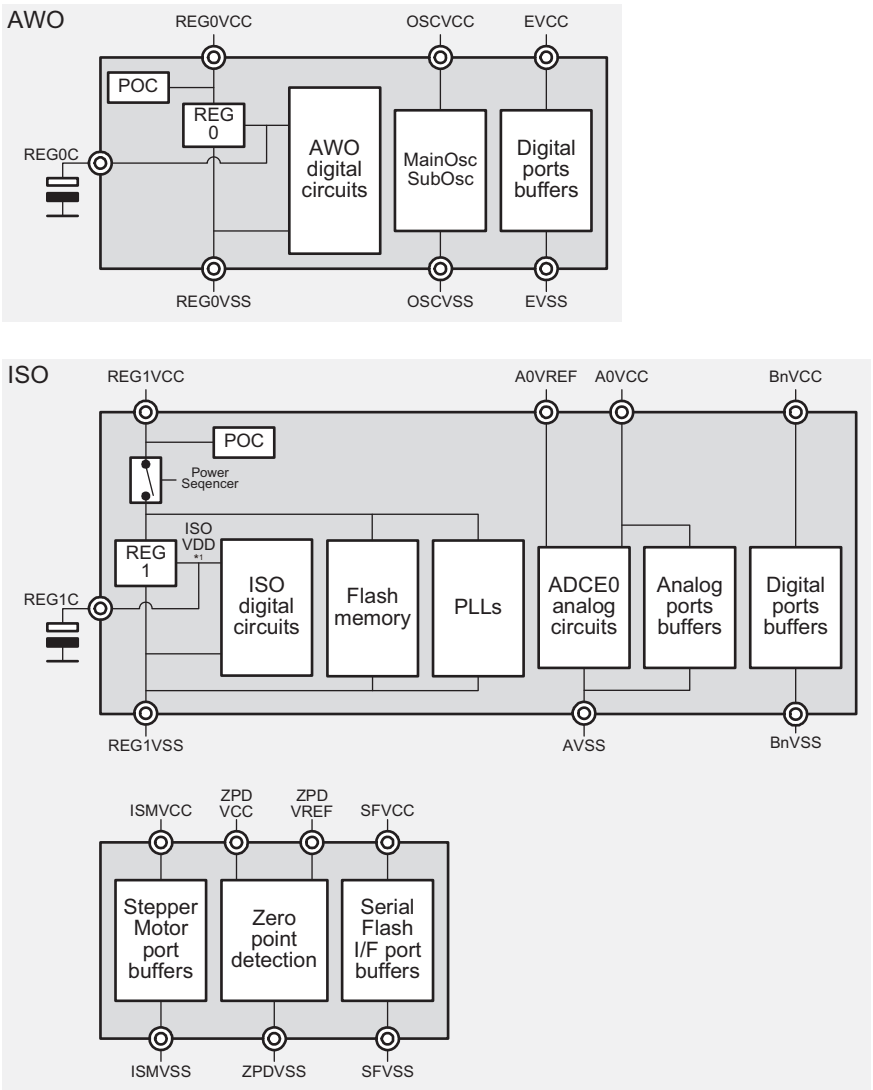
a) stop mask change of CKSC_IPLL0S_CTL
b) stop mask change of CKSC_IPLL1S_CTL
c) clock selector change of CKSC_ICPUCLKS_CTL
d) clock divider change of CKSC_ICPUCLKD_CTL
e) stop mask change of CKSC_ISDRBS_CTL
f) PLL0 dis-/enable trigger of PLL0E
g) PLL1 dis-/enable trigger of PLL1E

Figure 1.9 Power-down Sequence

1.5.8 Core Voltage Supplies (RH850/D1Lx)

The core voltage supply has to be provided to the AWO and to the ISO area separately.

AWO area and ISO are utilizing one on-chip regulator each. (AWO:REG0VCC, ISO:REG1VCC).



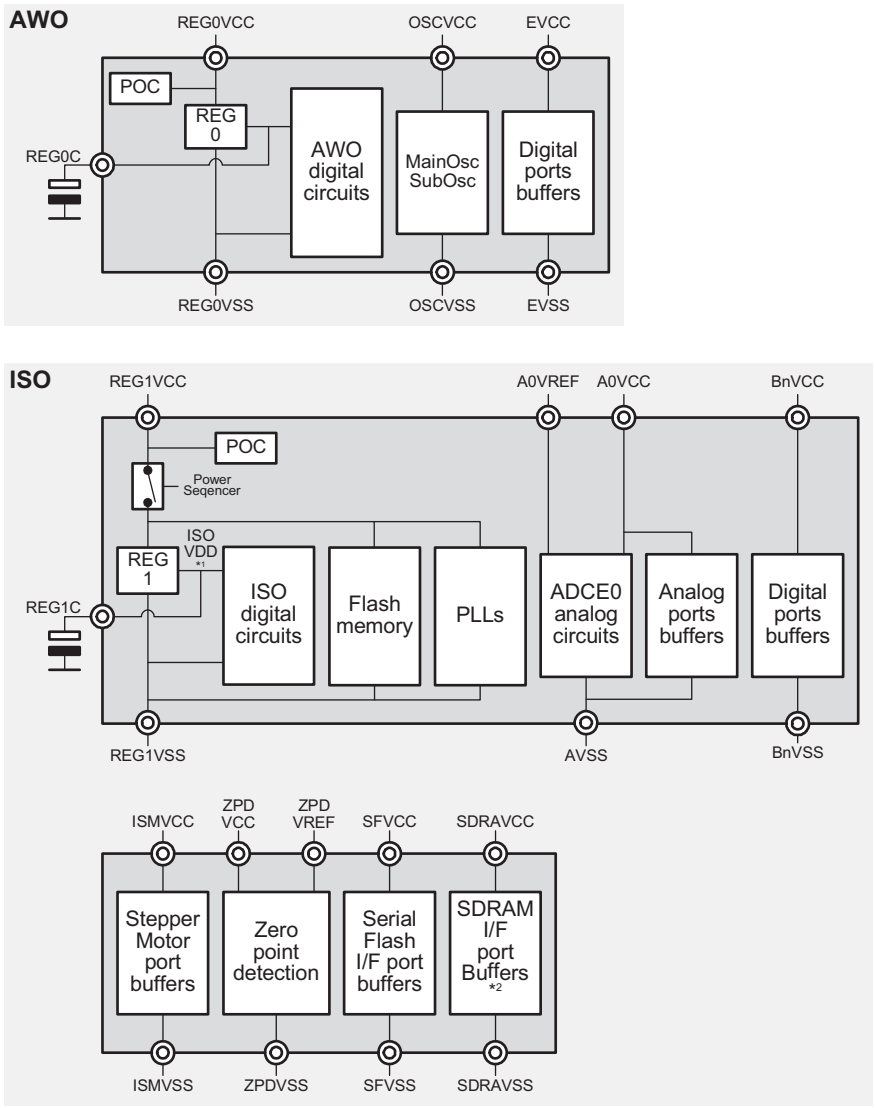
Note 1. ISOVDD is also input to the A/D Converter channel 20 for supply voltage monitoring purposes.

Figure 1.10 Voltage Supply D1Lx

1.5.9 Core Voltage Supplies (RH850/D1M1A, D1M1(H), D1M1-V2)

The core voltage supply has to be provided to the AWO and to the ISO area separately.

AWO area and ISO are utilizing one on-chip regulator each. (AWO: REG0VCC, ISO:REG1VCC).



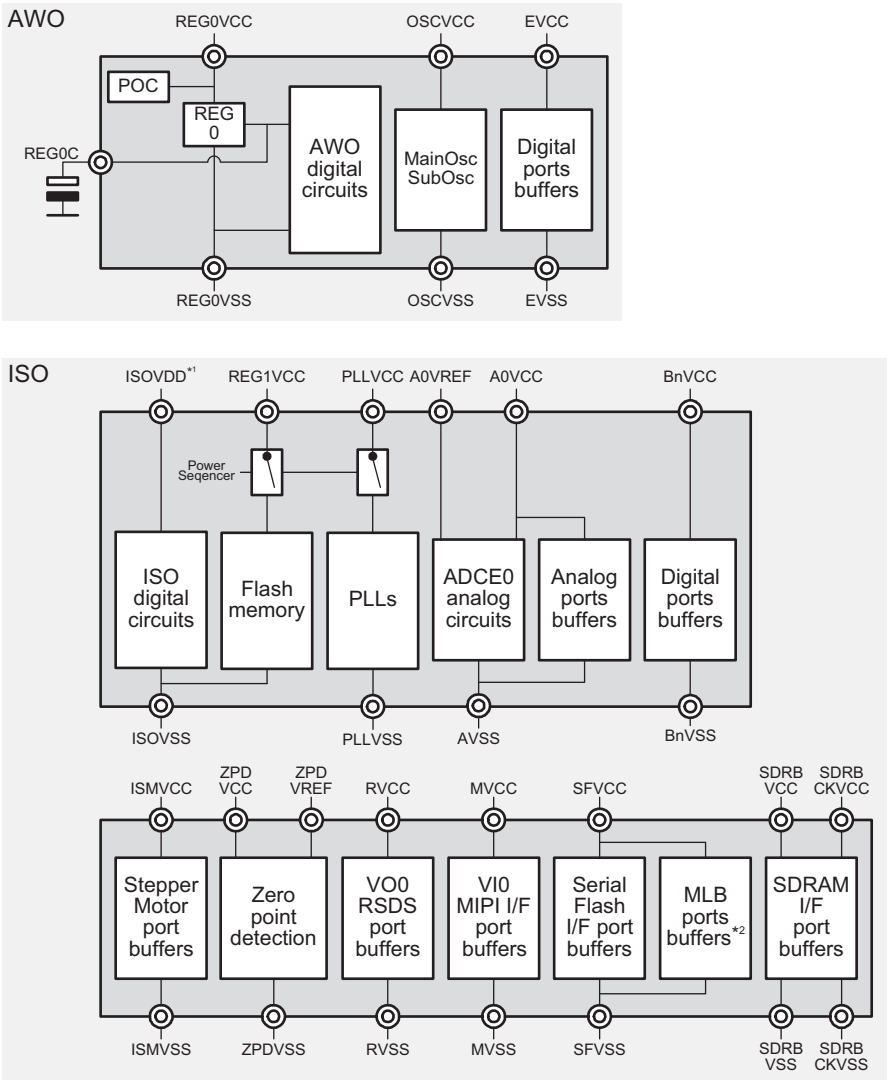
Note 1. ISOVDD is also input to the A/D Converter channel 20 for supply voltage monitoring purposes.
Note 2. SDRAVCC is only valid for D1M1A/D1M1H.

Figure 1.11 Voltage Supply D1M1A, D1M1(H), D1M1-V2

1.5.10 Core Voltage Supplies (RH850/D1M2(H))

The core voltage supply has to be provided to the AWO and to the ISO area separately.

AWO area is utilizing one on-chip regulator each. (AWO: REG0VCC). And, ISO area is supply from external regulator (ISOVDD).



Note 1. ISOVDD is also input to the A/D Converter channel 20 for supply voltage monitoring purposes.
Note 2. MLB is only for D1M2H

Figure 1.12 Voltage Supply D1M2(H)

1.5.11 Supply Voltage

Condition: T_j = –40 to +T_{Jmax}

Table 1.21 VCC Data

Parameter	PO[*1]	Symbol[*2]	Condition	MIN.	TYP.	MAX.	Unit
System	No	REG0VCC[*3]		2.7		5.5	V
	Yes	REG1VCC	D1Lx/D1M2(H)	2.7		5.5	V
			D1M1(H), D1M1A, D1M1-V2	2.7		3.6	V
	Yes	OSCVCC		2.7		5.5	V
	Yes	PLLVCC		2.7		5.5	V
	Yes	ISOVDD		1.15		1.35	V
Ports	No	EVCC[*7]		2.7		5.5	V
	Yes	BnVCC		2.7		5.5	V
	Yes	SFVCC	D1Mx/D1L2	2.7		3.6	V
			D1L1	2.7		5.5	V
	Yes	MVCC	D1M2H	2.7		3.6	V
	Yes	RVCC	D1M2(H)	2.7		3.6	V
	Yes	ISMVCC		2.7		5.5	V
A/D Converter[*5]	Yes	A0VCC[*6]		2.7		5.5	V
	Yes	A0VREF[*6]		2.7		5.5	V
SDRAM	Yes	SDRBVCC	D1M2(H)	1.7		1.9	V
		SDRAVCC	D1M1H, D1M1A	3.0		3.6	V
ZPD Comparator[*5]	Yes	ZPDVCC[*6]		2.7[*4]		5.5	V
	Yes	ZPDVREF[*6]		0		5.5	V

Note 1. PO = Power Off possibility: Under certain conditions some power supply pins are allowed to be unprovided in low power operating modes. This column informs about the principle allowance (Yes/No). However the details of supply voltage dependencies have to be obtained.

Note 2. As long as not other noted this specification does not differ between pins with different suffix for the symbol.

Note 3. Full device operation is only available, when the supply voltage is above the POC0 threshold voltage. The device may stop operation due to a $\overline{\text{RESET}}$ condition generated by the POC0, if the supply voltage drops below the POC0 threshold voltage.

Note 4. ZPD operation only 4.5 to 5.5 V

Note 5. 2.7 to 3.0 V range only specified DC characteristics.

Note 6. D1x should be keep this relation: A0VCC ≥ ISOVDD (ISOVDD is generated by REG1VCC (Except D1M2(H)), A0VREF ≤ A0VCC, ZPDVREF ≤ ZPDVCC, ZPDVREF ≤ ISMVCC

Note 7. EVCC should be kept same voltage level with REG0VCC.

1.5.12 Overload Condition (Injected Current)

The overload condition describes the behaviour in case of current injection to the port pins.

Condition: T_j = –40°C to +T_{Jmax}, XyVCC = 3.0 to 5.5 V

Table 1.22 Overload Current

Parameter		Symbol	Condition		Ratings*1	Unit
Overload Current*2 V_{IN} > VCC V_{IN} < VSS	Pins supplied by EVCC	I_{INJPM} I_{INJNM}	1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pins supplied by B0VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by B1VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} +I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by B2VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by B3VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by B4VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by RVCC		1 pin		±0	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|0|	mA
	Pin supplied by B5VCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by MVCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by SFVCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by ISMVCC		1 pin		±2	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3		|50|	mA
	Pin supplied by A0VCC		1 pin		±3	mA
			Sum of all absolute I_{INJPM} + I_{INJNM} of pins supplied as a group*3	D1M2(H), D1M1A, D1M1-V2	|20|	mA
				D1M1(H), D1Lx	|10|	mA

Note 1. The total current may be limited further by the total power dissipation.

Note 2. Be sure not to exceed the absolute maximum ratings (Max. value) of each supply voltage.

Note 3. The total overload current must be within the output current.

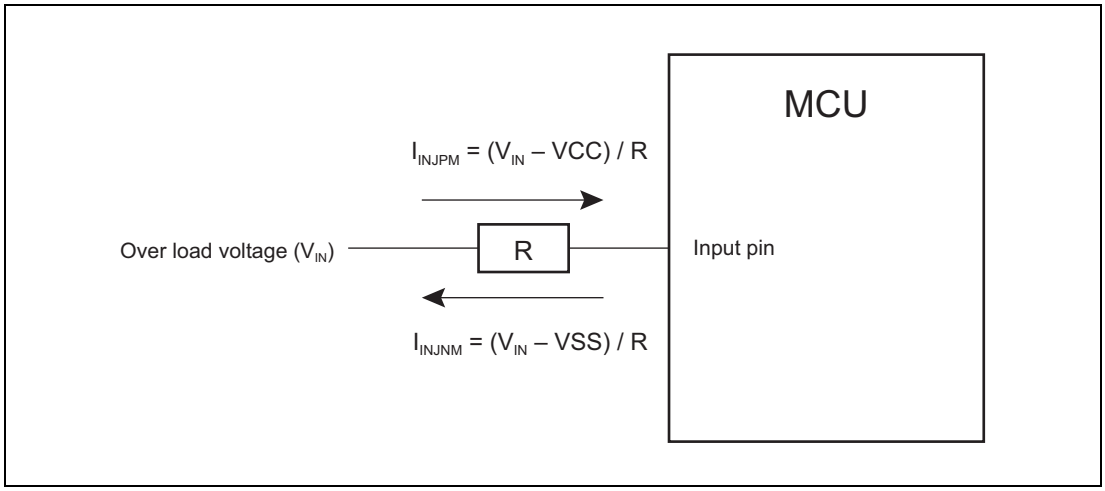


Figure 1.13 Definition of I_{INJPM} and I_{INJNM}

1.5.13 Operating Conditions

1.5.13.1 CPU Clock

Table 1.23 CPU Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1M2(H), D1M1A					240	MHz
D1M1H	*1				200	MHz
D1M1, D1M1-V2	*1				160	MHz
D1L1/D1L2(H)	*1				120	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

1.5.13.2 Module Clock

(1) APB Modules Clock

All modules (macros) that are connected though APB peripheral bus, and D1M2(H) has 3 type APB bus clocks.

(a) C_ISO_PCLK

Basically D1M2(H) uses synchronous APB bus clock with CPU clock

Table 1.24 C_ISO_PCLK Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1L1	f_{max},APB*1				60	MHz
D1L2(H)	f_{max},APB*1				60	MHz
D1M1(H), D1M1-V2	f_{max},APB*1				80	MHz
D1M2(H), D1M1A	f_{max},APB*1				60	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

(b) CLKJIT

Communication macro uses fixed frequency CLKJIT clock. It asynchronous with CPU clock and use SSC (Spread Spectrum Clocking).

Table 1.25 CLKJIT Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1x:	f_{max},JIT*1				80	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

(c) CLKFIX

Audio and timer macro uses fixed frequency CLKFIX clock. It asynchronous with CPU clock and use non-SSC (Spread Spectrum Clocking).

Table 1.26 CLKFIX Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1x:	f_{max},FIX				80	MHz

(2) XC bus Modules Clock

All modules (macros) that are connected though the multi layer bus, such as GPU2D engine, VDCE, ETNB, MLBB, JCUA, SDR-SDRAM and DDR2-SDRAM controller, SFMA, VRAMn, Retention RAM.

Table 1.27 XC Modules Clock Frequency

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
D1L1	f_{max},XC bus*1				60	MHz
D1L2(H)	f_{max},XC bus*1				60	MHz
D1M1H	f_{max},XC bus*1				100	MHz
D1M1, D1M1-V2	f_{max},XC bus*1				80	MHz
D1M2(H), D1M1A	f_{max},XC bus				120	MHz

Note 1. The center frequency is mentioned. SSCG margin needs to be added.

1.5.14 Oscillator Characteristics

1.5.14.1 Main Oscillator

A ceramic or crystal resonator can be connected to the main clock input pins as shown in **Figure 1.14, Recommended Main Oscillator Circuit**.

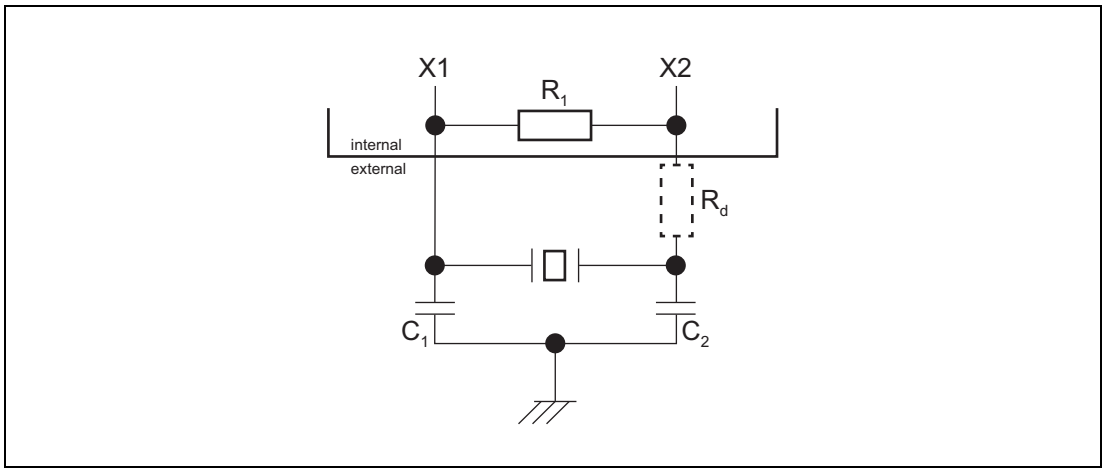


Figure 1.14 Recommended Main Oscillator Circuit

CAUTION

Values of C1, C2 and Rd depend on the used ceramic or crystal resonator and must be specified in cooperation with ceramic or crystal resonator manufacturer.

(1) Main Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}
OSCVCC = 3.0 to 5.5 V
Typ condition indicate following condition
- T_j = 25°C

Table 1.28 Main Oscillator Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
X1, X2 Oscillator Frequency		f_{OSC}		7.2		16	MHz
Oscillator stabilization time	DS	T_{OST}*1				6.0	ms
Main oscillator operation current	PC	I_{DDMOSC}	OSCVCC = 5.0 V, f_{OSC} = 8 MHz CL = 8 pF, AMPSEL = 11_B*4		340	500*2	µA
			OSCVCC = 5.0 V, f_{OSC} = 8 MHz CL = 8 pF, AMPSEL = 10_B		500	600*2	µA
			OSCVCC = 3.3 V, f_{OSC} = 8 MHz CL = 8 pF, AMPSEL = 10_B		170	300*3	µA
			OSCVCC = 5.0 V, f_{OSC} = 8 MHz CL = 8 pF, AMPSEL = 01_B		800	1200*2	µA
			OSCVCC = 3.3 V, f_{OSC} = 8 MHz CL = 8 pF, AMPSEL = 01_B		360	550*3	µA
			OSCVCC = 5.0 V, f_{OSC} = 16 MHz CL = 8 pF, AMPSEL = 00_B		1100	1700*2	µA
			OSCVCC = 3.3 V, f_{OSC} = 16 MHz CL = 8 pF, AMPSEL = 00_B		510	700*3	µA

Note 1. T_{OST} depends on the external crystal. Shorter timing might be found by evaluation.
Note 2. OSCVCC set to 5.5 V for MAX. value.
Note 3. OSCVCC set to 3.6 V for MAX. value.
Note 4. OSCVCC operation at 3.3 V is prohibited at AMPSEL=11_B.

1.5.14.2 Sub Oscillator

A crystal resonator can be connected to the sub clock input pins as shown in **Figure 1.15, Recommended Sub Oscillator Circuit**.

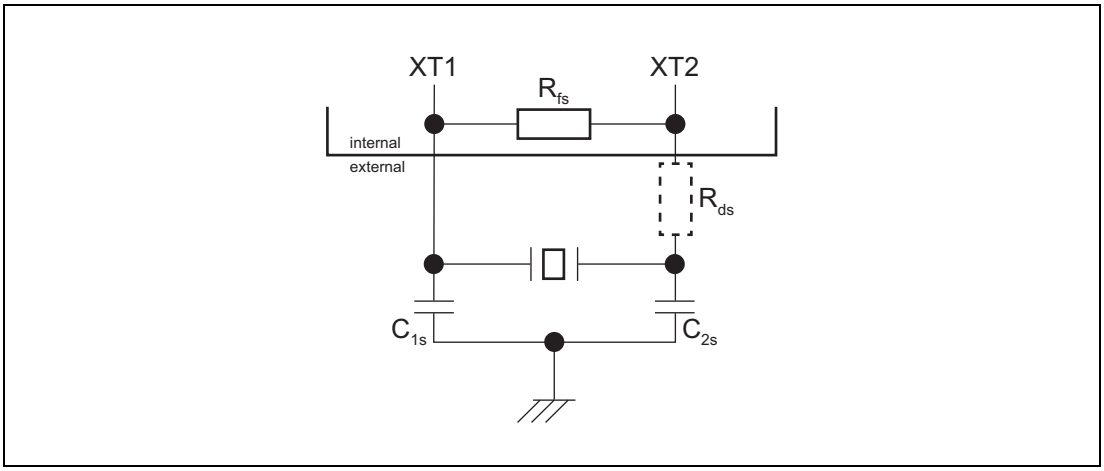


Figure 1.15 Recommended Sub Oscillator Circuit

CAUTION

Values of C_{1s}, C_{2s} and R_{ds} depend on the used crystal and must be specified in cooperation with crystal manufacturer.

(1) Sub Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}

Table 1.29 Sub Oscillator Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
XT1,XT2 Oscillator Frequency		f_{SOSC}		32	32.768	35	kHz
Sub oscillator stabilization time		T_{SOST}*1				2.0	s
Current	PC	I_{DDSOSC}			2		µA

Note 1. T_{SOST} depends on the external crystal. Shorter timing might be found by evaluation.

1.5.14.3 Internal Oscillator Characteristics

Condition: T_j = –40°C to +T_{Jmax}

Table 1.30 Internal Oscillator (240 kHz) Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Frequency		f_{240}		220	240	260	kHz
Oscillation Stabilization Time	DS*1	$T_{240STAB}$				60	µs
Current	PC	$I_{DDLOSCL}$	REG0VCC = 5.0 V		5		µA

Note 1. Not tested in production. Specified by design.

Table 1.31 Internal Oscillator (8 MHz) Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output Frequency		f_8		7.200	8.00	8.800	MHz
Oscillation Stabilization Time	DS*1	T_{8STAB}				15	µs
Current	PC	$I_{DDLOSCH}$	REG0VCC = 5.0 V		30		µA

Note 1. Not tested in production. Specified by design.

1.5.14.4 PLL Characteristics

Table 1.32 PLL0 (D1M2(H), D1M1(H), D1Lx) Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				508	MHz
PLL output period jitter		w/o SSCG	–100.0		100.0	ps
PLL output phase jitter		w/o SSCG	–1.5		1.5	ns
PLL lock up time		w/ SSCG			800.0	µs
PLL modulation frequency		w/ SSCG	20.0		100.0	kHz
PLL frequency dithering range		Center spread	±0.82	±2	±5.9	%
		Down spread	0.82	5.0	11.80	%

Table 1.33 PLL1 (D1M2(H)) Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				960.0	MHz
PLL output period jitter			–60.0		60.0	ps
Long term jitter		Term = 1 µs	–800		800	ps
		Term = 20 µs	–2.0		2.0	ns
PLL lock up time					300.0	µs

Table 1.34 PLL1 (D1M1(H)/D1M1A/D1M1-V2/D1Lx), PLL2 Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				480.0	MHz
PLL output period jitter			–100.0		100.0	ps
Long term jitter		Term = 1 µs	–500		500	ps
		Term = 20 µs	–2.0		2.0	ns
PLL lock up time					100.0	µs

Table 1.35 PLL0 (D1M1A/D1M1-V2) PLL0 Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PLL input frequency	f_{PLLkIN}		7.2		16	MHz
PLL output frequency	$f_{PLLkCLK}$				960.0*1	MHz
PLL output period jitter		w/o SSCG	–100.0		100.0	ps
PLL lock up time		w/ SSCG			1000.0	µs
PLL modulation frequency		w/ SSCG	20.0		50.0	kHz
PLL frequency dithering range		Center spread	±0.82	±2	±5.9	%
		Down spread	0.82	5.0	11.8	%

Note 1. D1M1A at max. PLL frequency of 960 MHz (CPU = 240 MHz) does not allow center-spread.

Table 1.36 PLL0 SSCG Dithering Range for Each Settings

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Frequency dithering range	f_{dit}	Dithered frequency mode (down spread only)	SELMPERCENT = 000	0.82	1.0	1.18	%
			SELMPERCENT = 001	1.64	2.0	2.36	
			SELMPERCENT = 010	2.46	3.0	3.54	
			SELMPERCENT = 011	3.28	4.0	4.72	
			SELMPERCENT = 100	4.10	5.0	5.90	
			SELMPERCENT = 101	4.92	6.0	7.08	
			SELMPERCENT = 110	6.56	8.0	9.44	
			SELMPERCENT = 111	8.20	10.0	11.80	
		Dithered frequency mode (center spread)	SELMPERCENT = 000	Invalid			
			SELMPERCENT = 001	±0.82	±1.0	±1.18	
			SELMPERCENT = 010	Invalid			
			SELMPERCENT = 011	±1.64	±2.0	±2.36	
			SELMPERCENT = 100	Invalid			
			SELMPERCENT = 101	±2.46	±3.0	±3.54	
			SELMPERCENT = 110	±.3.28	±4.0	±4.72	
			SELMPERCENT = 111	±4.10	±5.0	±5.90	

1.5.15 Voltage Regulator Conditions

Condition: T_j = –40°C to +T_{Jmax}
REGnVCC = 2.7 to 5.5 V

Table 1.37 Voltage Regulator

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage stabilization time	t_{REG}				1	ms
Output voltage level	TV_{tole}		1.2	1.25	1.3	V
Capacitance to REGnC (n=0,1)	C_{REG}	D1L2(H), D1L1: (REG0C and REG1C) D1M2(H), D1M1(H), D1M1A, D1M1-V2: (REG0C)		0.1		µF
Capacitance to REG1C	C_{REG}	D1M1(H), D1M1A, D1M1-V2, D1L2H(optional)		0.22		µF
PSRR	C_{PSRR}				–10	db
Output tolerance of REG1VCC			–4		4	%
Equivalent series resistance for load capacitance	RVRAWO	for AWO area			50*[1]	mΩ
	RVRISO	for ISO area			50*[1]	mΩ

Note 1. All values are defined by device characterization, not tested in production.

1.6 General IO Characteristic

1.6.1 Output Port Characteristics

1.6.1.1 GP Port Buffer

(1) Frequency Control of GP Port Buffers

The maximum frequency of the GP port buffer can be controlled via register setting in the port control in two steps; fast mode and slow mode.

Effectively the frequency control option limits the slew rate, what results in a (limited) max. frequency of the buffer.

Condition: Buffer power supply: XyVCC = 2.7 to 5.5V (except RVCC, RVCC = 2.7 to 3.6V)

Table 1.38 GP Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high level		CMOS V_{OHa1}	slow mode: I_{oh} ≤ –1mA, 16pin simultaneous operation slow mode: I_{oh} ≤ –2mA, 2pin simultaneous operation	XyVCC –0.5		XyVCC	V
		CMOS V_{OHa2}	fast mode: I_{oh} ≤ –5mA, 5pin simultaneous operation	XyVCC –0.5		XyVCC	
Output voltage low level		CMOS V_{OLa1}	slow mode: I_{oh} ≤ –1mA, 16pin simultaneous operation slow mode : I_{oh} ≤ –2mA, 2pin simultaneous operation	XyVSS		XyVSS +0.4	V
		CMOS V_{OLa2}	fast mode: I_{ol} <= 5mA, 5pin simultaneous operation	XyVSS		XyVSS +0.4	
cross current in port buffer during output level switching*2		I_{Cross}				0	mA
current limit during output level switching	DS	IODL	frequency control: slow mode XyVCC = 3.0 to 5.5 V			2	mA
			frequency control: fast mode XyVCC = 3.0 to 5.5 V			5	mA
Output frequency*3	DS*4	f_{max}	frequency control: fast mode C_L = 50 pF; XyVCC = 3.0 to 5.5 V	20			MHz
			frequency control: fast mode C_L = 30 pF; XyVCC = 3.0 to 5.5 V	50			MHz
			frequency control: slow mode C_L = 50 pF; XyVCC = 3.0 to 5.5 V	8			MHz
			frequency control: slow mode C_L = 30 pF; XyVCC = 3.0 to 5.5 V	10			MHz
			frequency control: fast mode C_L = 300 pF; XyVCC = 3.0 to 5.5 V	100			kHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The cross current caused by the frequency control (slew rate limitation) must not cause a cross current during buffer level switching.

Note 3. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**

Note 4. Not tested in production. Specified by design.

1.6.1.2 AN Port Buffer

Condition: Buffer power supply (XyVCC): A0VCC = 2.7 to 5.5 V

Table 1.39 AN Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHg2}	I_{OHg2} ≤ –1 mA*2, 16pin simultaneous operation	XyVCC –0.5		XyVCC	V
Output voltage low		V_{OLg2}	I_{OLg2} ≤ 1mA*2, 16pin simultaneous operation			XyVSS +0.4	V
Output propagation delay time		t_{pdo}	C_{load} = 50 pF			22	ns
			C_{load} = 30 pF			13	ns
Output rise/fall time		t_{rfo}	C_{load} = 50 pF			33	ns
			C_{load} = 30 pF			22	ns
Maximum output frequency*3	DS	f_{maxo}	C_{load} = 50 pF	8			MHz
			C_{load} = 30 pF	10			MHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified

Note 2. A port output current might affect the A/D Converter accuracy on neighbor pins. For details see **Section 1.8.1, Analog/Digital Converter (ADCE)**.

Note 3. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.

1.6.1.3 HS Port Buffer

The HS port buffer are used at serial Flash-.

Condition: Buffer power supply (XyVCC): SFVCC = 2.7 to 3.6 V (D1Mx, D1L2), SDRAVCC = 3.0 to 3.6 V (D1M1H/D1M1A)

Table 1.40 HS Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHb2}	I_{OH} ≤ –2 mA, 8 pin simultaneous operation	XyVCC –1.0		XyVCC	V
		V_{OHb1}	I_{OH} = –100 µA, 8 pin simultaneous operation	XyVCC –0.2		XyVCC	
Output voltage low		V_{OLb2}	I_{OL} ≤ 1.6 mA, 8 pin simultaneous operation	XyVSS		XyVSS +0.4	V
		V_{OLb1}	I_{OL} = 100 µA, 8 pin simultaneous operation	XyVSS		XyVSS +0.2	
Output frequency*2	DS*3		D1M2: SFVCC ≥ 3.0 V D1M1x/D1L2: SFVCC ≥ 3.12 V D1M1H, D1M1A: SDRAVCC ≥ 3.0 V			120	MHz
			D1M2: SFVCC < 3.0 V D1M1x/D1L2: SFVCC < 3.12 V D1M1H, D1M1A: SDRAVCC < 3.0 V			80	MHz
Target impedance	DS*3		D1M1A/D1M1-V2: ≥ 3.0 V, DSCTRL.xx[1:0]*4 = 00_B		25.0		Ω
			D1M1A/D1M1-V2: ≥ 3.0 V, DSCTRL.xx[1:0]*4 = 01_B		33.0		Ω
			D1M1A/D1M1-V2: ≥ 3.0 V, DSCTRL.xx[1:0]*4 = 10_B		50.0		Ω
			D1M1A/D1M1-V2: ≥ 3.0 V, DSCTRL.xx[1:0]*4 = 11_B		100.0		Ω

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition** with a load condition of C_L = 15 pF.

Note 3. Not tested in production. Specified by design.

Note 4. Please refer to Users Manual for each bit field of DSCTRL.xx[1:0] (xx = P22_10_DS, P21_9_1_DS, P21_0_DS, SDRDSA, SDRDSD3, SDRDSD2, SDRDSD1, SDRDSD0, SDRDSC). And, DSCTRL.xx cover the AC characteristics, if circuit impedance is matched.

1.6.1.4 MLB Port Buffer

The MLB port buffer are used at Media Local Bus-.

Condition: Buffer power supply (XyVCC): SFVCC = 3.0 to 3.6 V (D1M2(H))

Table 1.41 MLB Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHb2}	I_{OH} ≤ –6mA, 2 pin simultaneous operation	XyVCC –1.0		XyVCC	V
		V_{OHb1}	I_{OH} = –100 µA	XyVCC –0.5		XyVCC	
Output voltage low		V_{OLb2}	I_{OL} ≤ 6 mA, 2 pin simultaneous operation	XyVSS		XyVSS +0.4	V
		V_{OLb1}	I_{OL} = 100 µA	XyVSS		XyVSS +0.4	
Output frequency*2	DS*3			50			MHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition** with a load condition of C_L = 40pF.

Note 3. Not tested in production. Specified by design.

1.6.1.5 HD Port Buffer

The stepper motor driver (SMD) is a bi-directional I/O buffer with the same buffer like the GP buffers but with a high current output buffer and an additional zero point detection path.

A output frequency up to 32 kHz is possible if the SMDIO is used with the GP Output path (Selection0).

Stepper Motor Driver mode (Selection1) the buffer have to provide the full drivability of the specified current output in the ISMVCC = 4.75 V to 5.25 V supply range. Outside this supply range no current is specified for this mode. Refer to **Figure 1.16, Output Current Diagram of SMDIO Buffer (valid only at Ta = –40°C)**."

NOTE

Selection 0/1 is the Stepper Motor Driver output buffers selection and corresponds to the register PDSC[17:16].PDSCn_m = 0/1 setting.

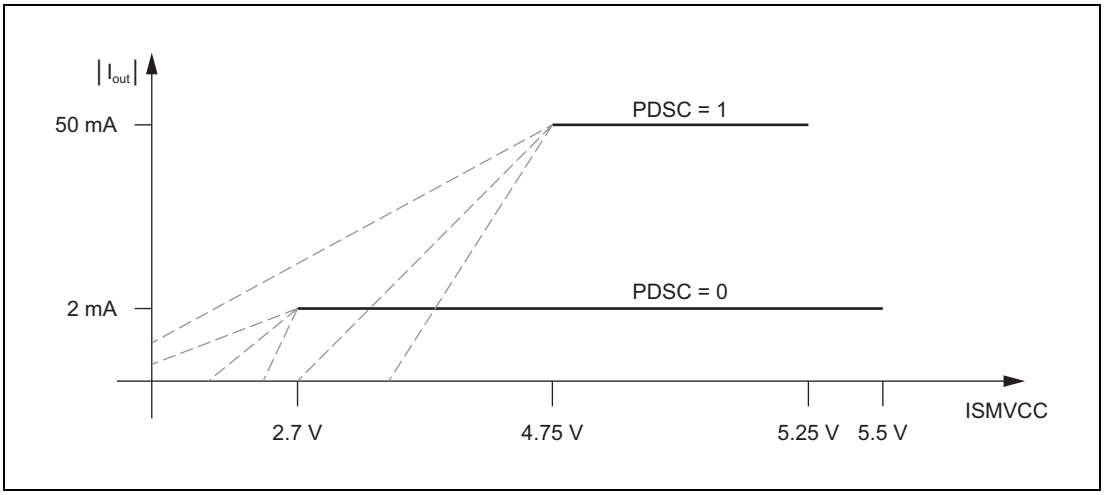


Figure 1.16 Output Current Diagram of SMDIO Buffer (valid only at Ta = –40°C)

The output voltage and current of the SMDIO buffer are shown in the below **Figure 1.17, Output Voltage and Current of the SMD Function**. The cross current through the buffer is visible. It is caused by the two output transistors that are kept open simultaneously for a specific time while the output level is switched. Opening both transistors is necessary in order to control the slew rate. It is also necessary since the inductance of the stepper motor induces a reverse current that would be discharged through the protection diodes, if the transistor is not open.

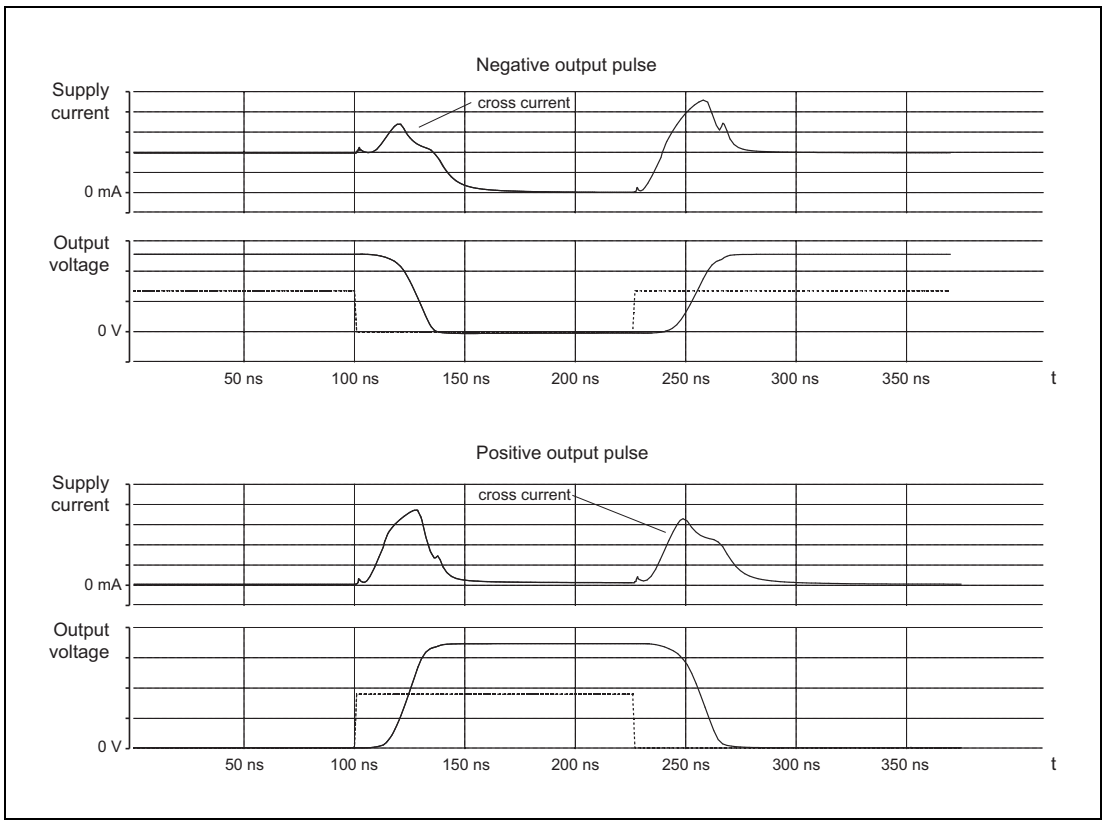


Figure 1.17 Output Voltage and Current of the SMD Function

CAUTION

- Buffer power supply (XyVCC):
  - Selection0: ISMVCCn = 2.7 to 5.5 V
  - Selection1: ISMVCCn = 4.75 to 5.25 V

NOTE

Selection 0/1 is the Stepper Motor Driver output buffers selection and corresponds to register setting in port control macro.

Table 1.42 HD Output Buffer Characteristic

Parameter*1	CT	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output voltage high		V_{OHd2}	(Selection0)	I_{OHd2} ≤ –2 mA	XyVCC –0.5		XyVCC	V
		V_{OHd3}	(Selection1) XyVCC = 4.75 to 5.25 V	I_{OHd3} = –52 mA T_J = –40°C	XyVCC –0.48*9		XyVCC	V
				I_{OHd3} = –45 mA T_J = –40°C	XyVCC –0.5			
		V_{OHd4}		I_{OHd4} = –39 mA T_J = 25°C				
		V_{OHd5}		I_{OHd5} =-32 mA T_J = 125°C				
		V_{OHd6}		I_{OHd6} = –30 mA T_J = 150°C				
Output voltage low		V_{OLd2}	(Selection0)	I_{OLd2} ≤ 2 mA	XyVSS		XyVSS +0.5	V
		V_{OLd3}	(Selection1) XyVCC = 4.75 to 5.25 V	I_{Old3} = 52 mA T_J = –40°C	XyVSS		XyVSS +0.52*9	V
				I_{Old3} = 45 mA T_J = –40°C			XyVSS +0.5	
		V_{OLd4}		I_{Old4} = 39 mA T_J = 25°C				
		V_{OLd5}		I_{Old5} = 32 mA T_J = 125°C				
		V_{OLd6}		I_{Old6} = 30 mA T_J = 150°C				
Output voltage deviation*2	DS*3	VDEV*4	(Selection1)				50	mV
Output slew rate*6	DS*3	t_{RFd}		10% - 90%	12		70	ns
Peak cross current*7	DS*3	I_{CROSS}*4					50	mA
Output pulse width*8	DS*3	t_{MO}d			125			ns
Output pulse length deviation*8	DS*3	t_{SMDEV}*4			–10	5	45	ns
Output resistance		R_{OSM}	(Selection1) XyVCC = 4.75 to 5.25 V	T_J = –40°C	5		11.6	Ω
				T_J = 25°C			15.4	Ω
				T_J = 125°C			18.8	Ω
				T_J = 150°C			21	Ω
Output frequency	DS*3	f_{OSMDIO}	(Selection0)	I_O = 3mA C_{load} = 50 pF		32		kHz
	DS*3	f_{OSMDIO}	(Selection1)	C_{load} = 50 pF		128		kHz

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. Output voltage deviation defines the difference of the outputs levels of the same stepper motor. VDEV = max (| VOHx – VOHy | , | VOLx – VOLy |) @ IOHx = IOHy, IOLx = IOLy. x and y denote any combination of two pins of a four pin group that is used for one stepper motor. The output voltage deviation is not tested, but specified by design.

Note 3. Not tested in production. Specified by design.

Note 4. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The output voltage deviation is not tested, but specified by design.

Note 5. The slew rate control generates a cross current in the output stage to control the energy of the external inductive load. The cross current flows only during the output transition time t_{RF}. It flows in addition to the output current. The cross current is not tested, but derived from simulation.

Note 6. The output buffer cannot generate high or low pulses shorter than this time, because of its slew rate control system. This value is not tested, but derived from simulation.

Note 7. The slew rate control function causes a deviation of output pulse time compared to the ideal selected output

pulse setting. This value is not tested, but derived from simulation.

Note 8. Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.

Note 9. RH850/D1L2(H) Ver.1 does not support this specification.

1.6.1.6 RSDS/OpenLDI Port Buffer

Condition: Buffer power supply (XyVCC): RVCC(D1M2(H)) = 3.0 to 3.6 V, B5VCC(D1M1A) = 3.0 to 3.6V
RSDS: *According to National Semiconductor RSDS "Intra-panel" Interface Spec Rev.1.0 May 2003*
LVDS: *According to ANSI EIA/TIA-644-A FEBRUARY 2001*

Table 1.43 Differential LVDS Mode for RSDS (D1M2(H))

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Output Voltage		Vod	R_L=100Ω	100	200	600	|mV|
Offset Voltage		V_{OS}	R_L = 100Ω C_L = 5 pF	0.5	1.2	1.5	V
Change of VOS between complementary output states		dV_{OS}				35	mV
Change of VOD between complementary output states		dV_{OD}				35	mV
RSDS driver current Irsds		Irsds		1	2	6	mA
RSDS driver speed		f_{RSDS}				50	MHz

Table 1.44 Differential LVDS Mode for OpenLDI (D1M1A)

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Differential Output Voltage		Vod	R_L=100Ω	250.0	350.0	450.0	|mV|
Offset Voltage		V_{OS}		1.125	1.250	1.375	V
Change of VOS between complementary output states		dV_{OS}				50.0	mV
Change of VOD between complementary output states		dV_{OD}				50.0	mV
LVDS driver speed		f_{LVDS}				280.0	MHz

In **Figure 1.19** the signaling for single ended and differential output is shown.

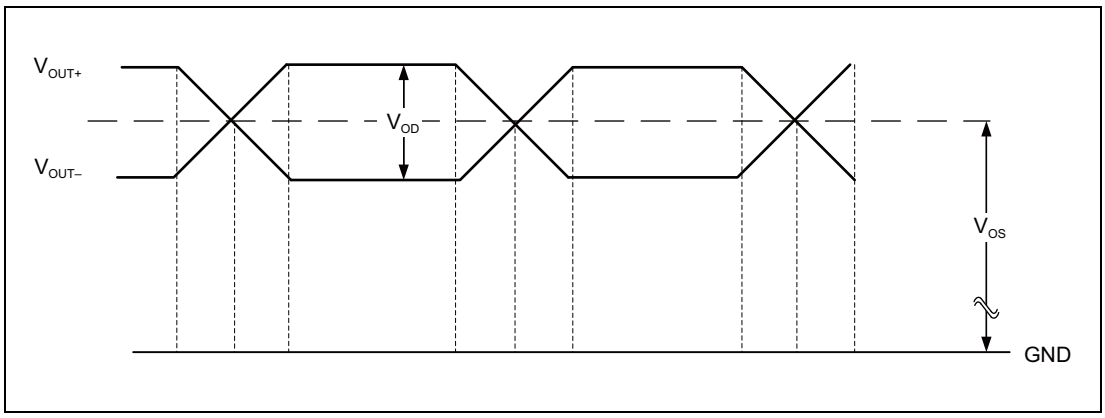


Figure 1.18 Output Signaling of the RSDS/LVDS Buffer

In **Figure 1.19** the test circuit for offset voltage (VOS) and differential output voltage (VOD) is shown.

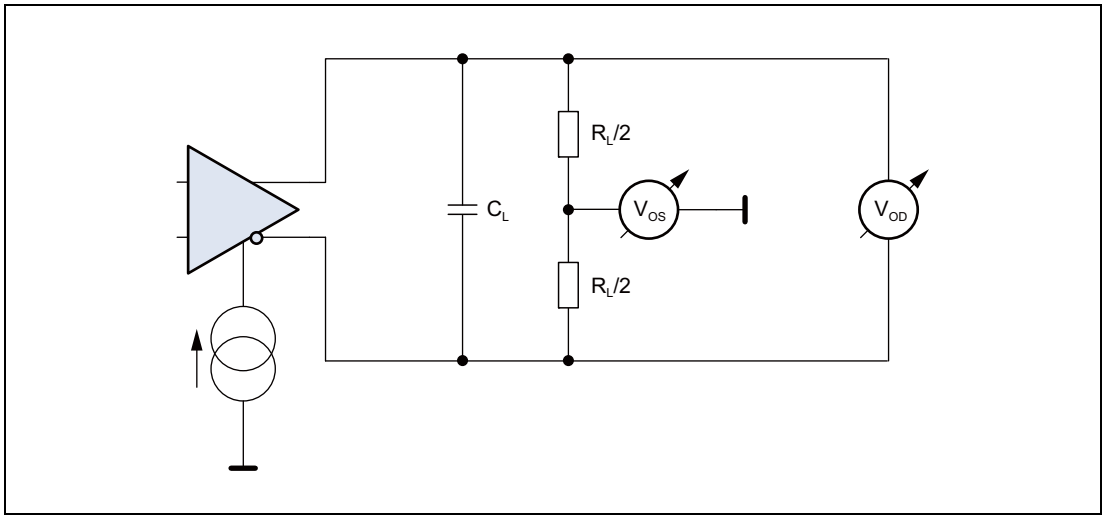


Figure 1.19 VOD and VOS Test Circuit

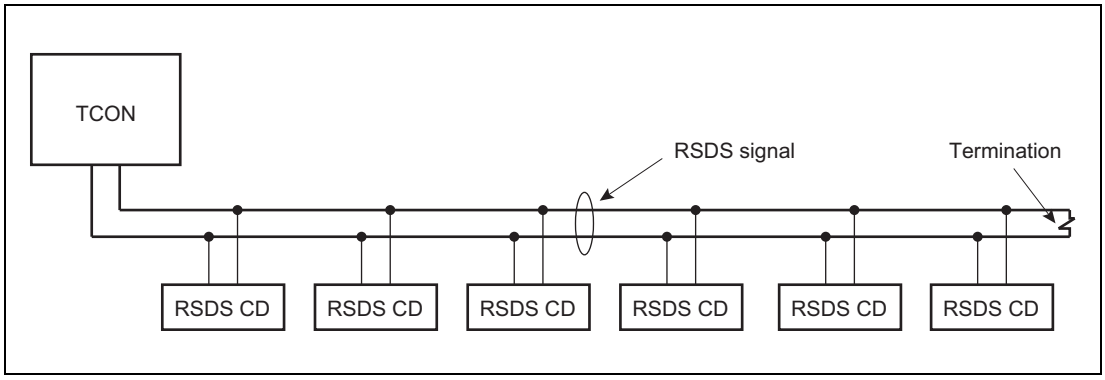


Figure 1.20 RSDS Bus Topology

RSDS bus is terminated at the far end with a nominal termination of 100Ω. The interconnecting media is a balanced coupled pair with nominal (unloaded) differential impedance of 100Ω.

1.6.1.7 DDR2-SDRAM Port Buffer

Condition: Buffer power supply (XyVCC): SDRBVCC = 1.7 to 1.9 V.
According to *DDR2-SDRAM specification of JEDEC STANDARD 79-2F "JESD79-2F"*[3]

Table 1.45 DDR2-SDRAM Buffer Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input Reference voltage		SDRBVREF	a, b	0.49 × SDRBVCC	0.50 × SDRBVCC	0.51 × SDRBVCC	V
Leak current		Ileak				1	µA
Slew rate		SRo		1.5		4.5	V/ns
Output minimum source current		I_{OH}	SDRBVCC – PAD = 300 mV	5.16		14.31	mA
Output minimum sink current		I_{OL}	PAD = 300 mV	5.16		14.31	mA
ODT tolerance		R_{ODT}	ODT = 75Ω*4	60	75	90	Ω
			ODT = 150Ω	120	150	180	Ω

Note 1. The value of SDRBVREF may be selected by the user to provide optimum noise margin in the system. Typically the value of SDRBVREF is expected to be about 0.5 × SDRBVCC of the transmitting device and SDRBVREF is expected to track variations in SDRBVCC.

Note 2. Peak to Peak ac noise on SDRBVREF may not exceed ±2% SDRBVREF(dc).

Note 3. DDR-SDRAM buffer specification is correspond to JEDEC specification (only correspond to "reduced strength")

Note 4. The D1M2(H) always use R_{ODT} = 75Ω.

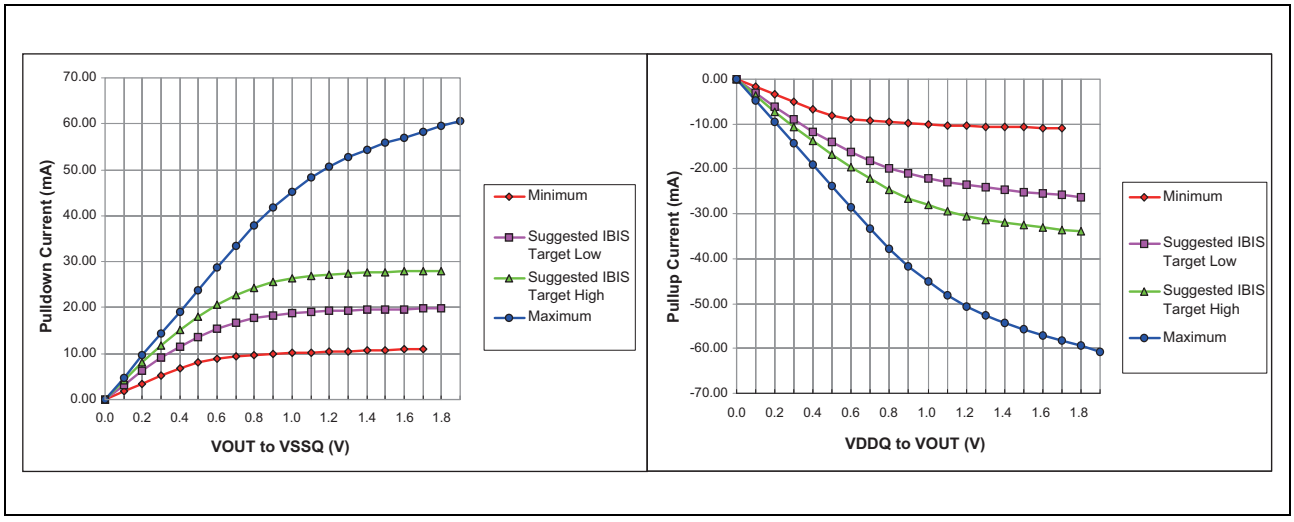


Figure 1.21 DDR2-SDRAM Default Pull-up Characteristics for Reduced Strength Driver

1.6.2 Port Input Characteristics

1.6.2.1 CMOS1

Condition: Buffer power supply: XyVCC

Table 1.46 CMOS1 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa1}	CMOS XyVCC = 2.7 to 5.5 V	0.65 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa1}	CMOS XyVCC = 2.7 to 5.5 V	–0.3		0.35 × XyVCC	V
Input propagation delay time	DS	$t_{pdi,c1}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF			3.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.2 Schmitt1

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.47 Schmitt1 Input Characteristic

Parameter*1	CT	Symbol	Condition*2		MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa2}	Schmitt1 XyVCC = 2.7 to 5.5 V	for FLMD0	0.68 × XyVCC		XyVCC +0.3	
				except FLMD0	0.7 × XyVCC			
Input voltage low		V_{ILa2}	Schmitt1 XyVCC = 2.7 to 5.5 V		–0.3		0.3 × XyVCC	
Input hysteresis		V_{Ha1}	Schmitt1		0.3			V
Input propagation delay time	DS	$t_{pdi,s1}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF				5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.3 Schmitt2

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.48 Schmitt2 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa}	Schmitt2 XyVCC = 2.7 to 5.5 V	0.75 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa}	Schmitt2 XyVCC = 2.7 to 5.5 V	–0.3		0.25 × XyVCC	V
Input hysteresis		V_{Ha2}	Schmitt2	0.2 × VCC			V
Input propagation delay time	DS	$t_{pdi,s2}$	XyVCC = 2.7 to 5.5 V C_{load} = 0.4 pF			5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

NOTE

The Schmitt2 input characteristic is to be used for the $\overline{\text{RESET}}$ input of the device.

1.6.2.4 Schmitt4

Condition: Buffer power supply: XyVCC
For different input timing of Schmitt trigger buffer see **Section 1.3.1, AC Characteristic Measurement Condition**.

Table 1.49 Schmitt4 Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa4}	Schmitt4 XyVCC = 2.7 to 5.5 V	0.80 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa4}	Schmitt4 XyVCC = 2.7 to 5.5 V	–0.3		0.50 × XyVCC	V
Input hysteresis		V_{Ha4}	Schmitt4	0.1			V
Input propagation delay time	DS	$t_{pdi,s4}$	XyVCC = 2.7 to 5.5 V C_{load}=0.4 pF			5.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.5 (LV)TTL

Condition: Buffer power supply: XyVCC

Table 1.50 (LV)TTL Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHLTa1}	LVTTL XyVCC = 3.0 to 3.6 V	2.0		XyVCC +0.3	V
Input voltage high		V_{IHTa1}	TTL XyVCC = 3.6 to 5.5 V	2.2		XyVCC +0.3	V
Input voltage low		V_{ILLTa1}	LVTTL XyVCC = 3.0 to 3.6 V	–0.3		0.8	V
Input voltage low		V_{ILTa1}	TTL XyVCC = 3.6 to 5.5 V	–0.3		0.8	V
Input propagation delay time	DS	$t_{pdi\text{-}c1}$	XyVCC = 3.0 to 5.5 V			4.0	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.6 MLB

Condition: Buffer power supply (XyVCC): SFVCC=3.0 to 3.6 V

Table 1.51 MLB Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa1}	XyVCC = 3.0 to 3.6 V	1.8		XyVCC +0.3	V
Input voltage low		V_{ILa1}	XyVCC = 3.0 to 3.6 V	–0.3		0.7	V
Input propagation delay time	DS	$t_{pdi\text{-}c1}$	XyVCC = 3.0 to 3.6 V C_{load} = 0.4 pF			1.5	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.7 HS

Condition: Buffer power supply (XyVCC): SFVCC (D1Mx, D1L2 = 2.7 to 3.6 V)

Table 1.52 HS Input Characteristic

Parameter*1	CT	Symbol	Condition*2	MIN.	TYP.	MAX.	Unit
Input voltage high		V_{IHa1}	XyVCC = 2.7 to 3.6 V	0.65 × XyVCC		XyVCC +0.3	V
Input voltage low		V_{ILa1}	XyVCC = 2.7 to 3.6 V	–0.3		0.35 × XyVCC	V
Input propagation delay time	DS	$t_{pdi\text{-}c1}$	XyVCC = 2.7 to 3.6 V C_{load} = 0.4 pF			2	ns

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified

Note 2. The alias XyVCC in the condition is used instead of the operating voltage range for the related port group. By no means it extends the operating range of the related supply voltage. The exceeding condition will be meaningless.

1.6.2.8 MIPI-CSI2

Condition: Buffer power supply (XyVCC): MVCC = 3.0 to 3.6 V

Table 1.53 MIPI-CSI2 Differential Input Characteristic

Parameter*1	Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
HS-RX	Common-mode Voltage	Vcmrx(dc)		70		330	mV
	Differential input high threshold	Vidth				70	mV
	Differential input low threshold	Vidtl		–70			mV
	Differential input impedance	Zid		80	100	125	Ω
LP-RX	Logic1 input voltage	Vihlp		880			mV
	Logic0 input voltage	Villp				550	mV
	Input hysteresis	Vhyst		25			mV

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.6.2.9 Pull-Up and Pull-Down Resistors

Table 1.54 Pull-up and Pull-down Resistor Characteristic

Parameter*1	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Pull-Up resistor		R_{PU}		20	40	120	kΩ
Pull-Down resistor		R_{PD}		20	40	120	kΩ
Pull-Up resistor		R_{PU}	only FLMD0	4		44	kΩ
Pull-Down resistor		R_{PD}	only FLMD0	4		50	kΩ

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.6.3 IO Input Leakage Current

Condition: T_j = –40°C to T_{Jmax}
Buffer power supply: XyVCC.
Typ condition indicate following condition
- Each VCC set to 5.0V
- T_j = 25°C
- Device: maximum condition

Table 1.55 Input leakage Current for Each Power Domain

Parameter*1	Domain	Symbol	Condition	MIN.	TYP.	MAX.	Unit
input leakage current (high level)	EVCC B0VCC B1VCC B2VCC B3VCC B4VCC B5VCC SFVCC(D1L1) A0VCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–0.5	–0.1		µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC		0.1	+0.5	µA
input leakage current (high level)	ISMVCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–0.6	–0.1		µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC		0.1	+0.5	µA
input leakage current (high level)	SFVCC(D1M2)	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–2			µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC			+2	µA
input leakage current (high level)	RVCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–3			µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC			+3	µA
input leakage current (high level)	MVCC	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–0.5			µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC			+0.5	µA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

Table 1.56 Input Leakage Current for SFVCC of P21_[9:0] (D1M1x/D1L2)

Parameter*1	Domain	Symbol	Condition	MIN.	TYP.	MAX.	Unit
input leakage current (high level)	SFVCC (D1M1x/ D1L2)	$I_{inLeakH}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC	–2			µA
input leakage current (low level)		$I_{inLeakL}$	1 pin supplied by XyVCC XyVSS ≤ Vi ≤ XyVCC			+20	µA

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.6.4 I/O Capacitance

Table 1.57 IO Buffer Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SDRBx	CIO	f = 1 MHz			7.0	pF
P21_x, SDRAx					5.0	pF
P40 (D1M2(H))					9.0	pF
P44/P45 (D1M2(H))					9.0	pF
Other					8.0	pF

Table 1.58 Input Buffer Capacitance

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input buffer capacitance	CI	f = 1 MHz			8.0	pF

1.7 General Module Operating Conditions

1.7.1 $\overline{\text{RESET}}$

Condition: AWO = powered
EVCC = 2.7 to 5.5 V, CL = Max.100 pF
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**

Table 1.59 Reset AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width*1		t_{WRSL} (in RUN/HALT mode)		10			µs
		t_{WRSL} (in deepstop mode)		25			µs
$\overline{\text{RESET}}$ pulse rejection*2	DS	t_{WRRJ}		100			ns

Note 1. This signal low time is needed to ensure that the internal $\overline{\text{RESET}}$ is activated.

Note 2. The $\overline{\text{RESET}}$ input incorporates an analog filter. Pulses shorter than this minimum will be ignored. Not tested in production.

NOTE

Reset pulses shorter than the given value may not be recognized by the device, they do not cause undefined states of the device.

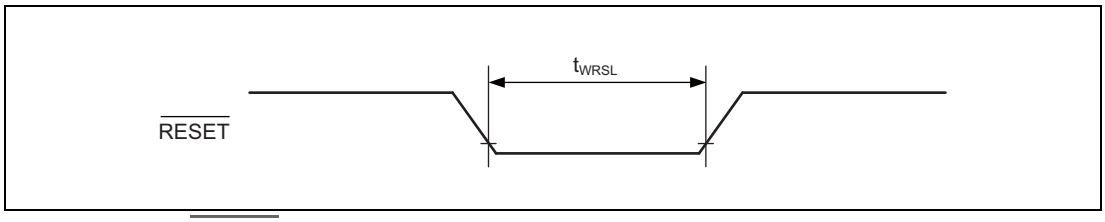


Figure 1.22 $\overline{\text{RESET}}$ Timing

1.7.2 Interrupt Timing

Condition: AWO = powered, ISO = powered
EVCC = 2.7 to 5.5V, BnVCC = 2.7 to 5.5V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.60 Interrupt AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI high-level width*1		t_{NIH}		10			µs
NMI low-level width*1		t_{NIL}		10			µs
NMI pulse rejection*2	DS*3	t_{NIRJ}		50			ns
I_{NTPn}*4 high-level width*1		t_{ITH}	except D1M1A/D1M1-V2*5	24			µs
			D1M1A/D1M1-V2	10			µs
I_{NTPn}*4 low-level width*1		t_{ITL}	except D1M1A/D1M1-V2*5	24			µs
			D1M1A/D1M1-V2	10			µs
I_{NTPn}*4 pulse rejection*2	DS*3	t_{ITRJ}		50			ns

Note 1. Pulses longer than this value will pass the input filter.
Note 2. Pulses shorter than this value do not pass the input filters.
Note 3. Characteristic is not tested in production.
Note 4. n = 10...0.
Note 5. 24 µs is for when high speed internal oscillator is configured to stop in DEEPSTOP (ROSCSTPM.ROSCSTPMSK = 0_B). Other case is 10 µs.

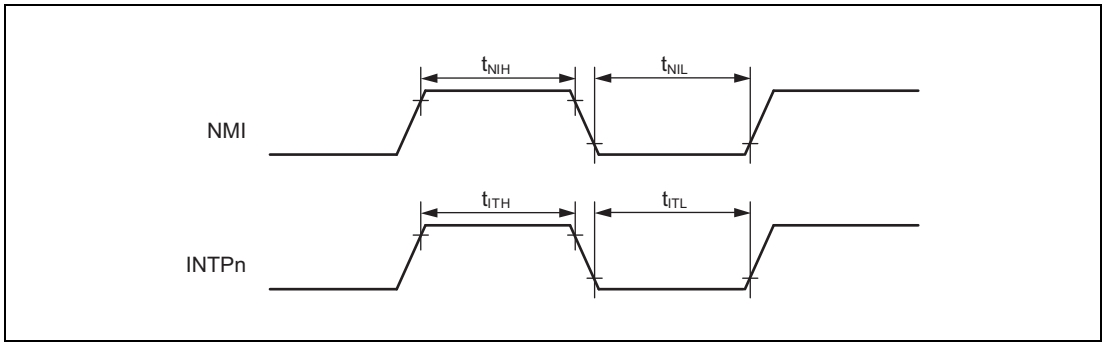


Figure 1.23 Interrupt Timing

NOTE

Interrupt timing is generated by analog delay elements. Delay characteristics have a wide range in production.

1.7.3 System Pins Timing

The below specification is valid for all system pins:

- FLMD0, FLMD1, MODE0, MODE1, PWRGD, JP0_4.

Instead of using the names of the system pins the term SYSPIN is used.

These system pins SYSPIN incorporate an analog noise filter within the input signal path:

Condition: AWO = powered,
EVCC = 2.7 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.61 System Pins AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SYSPIN high-level width*1		t_{SPH}		10			µs
		t_{SPHGD}	PWRGD	10			µs
SYSPIN low-level width*1		t_{SPL}		10			ns
		t_{SPLGD}	PWRGD	10			µs
SYSPIN pulse rejection*2	DS*3	t_{SPRJ}		50			ns

Note 1. Pulses longer than this value will pass the input filter.
Note 2. Pulses shorter than this value do not pass the input filters.
Note 3. Characteristic is not tested in production.

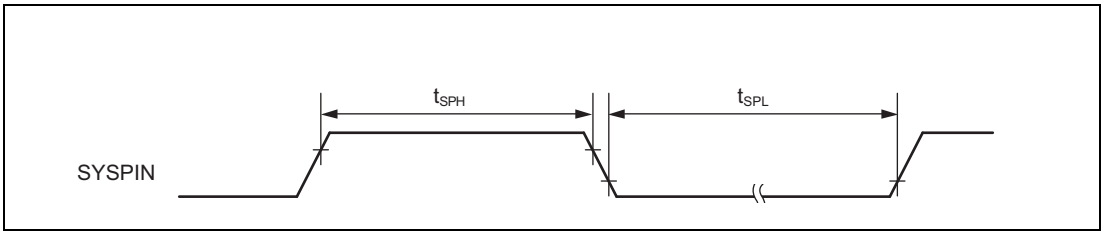


Figure 1.24 System Pins Timing

NOTE

System Pins timing is generated by analog delay elements. Delay characteristics have a wide range in production. System pins need hold time of 1 µs from FLMD0 determined.

1.7.4 Clock-Output Function

Condition: AWO = powered
EVCC = 2.7 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**. The input timings are valid if the digital filter is bypassed.

Table 1.62 Clock Output Mode via GPIO Buffer

Parameter	CT	Symbol	Pin mode	Condition	MIN.	TYP.	MAX.	Unit
Clock output period time (CSCXFOUT)		t_{clkout}			50			ns
CSCXFOUT high/low-level width		t_{FPH}/t_{FPL}	CSCXFOUTP (FOUT)	N = 1 or even value, drive strength = fast	t_{clkout} × 0.4			ns
				N = odd value (N ≥ 3), drive strength = fast	t_{clkout} × ((N – 1) / 2N) – 10			ns
				N = 1 or even value, drive strength = slow	t_{clkout} × 0.5 – 25			ns
				N = odd value (N ≥ 3), drive strength = slow	t_{clkout} × ((N – 1) / 2N) – 25			ns

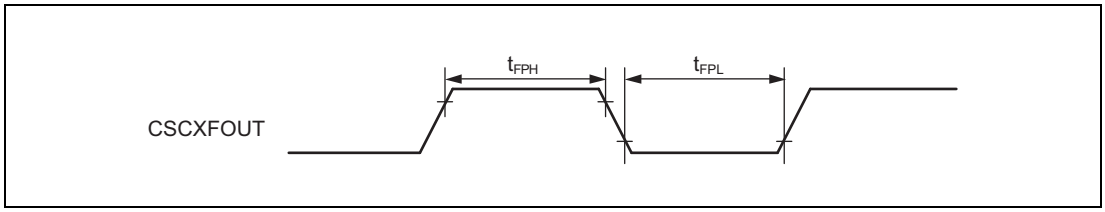


Figure 1.25 Clock Output Function Timing (CSCXFOUT)

1.7.5 ECM ERROUT

Table 1.63 ECM ERROUT AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High/low pulse width		t_{ECMHNB} / t_{ECMLNB}		2 × t_{SYNC}*1 + 5			ns

Note 1. t_{SYNC} is TAUB or OSTM operation clock cycle.

1.7.6 General Digital Noise Filter (DNF) Specification

(1) Minimum Pulse Rejection Width

Minimum pulse rejection width means that this is the minimum pulse width that will definitely be suppressed or in other words, ext. signal pulses with a longer width might pass the filter.

$$t_{wDNF(min)} = (s-1) \times \frac{1}{f_s}$$

(2) Maximum Pulse Rejection Width

Maximum pulse rejection width means that this is the maximum pulse width that can be suppressed or in other words, ext. signal pulses with a longer width will definitely pass the filter.

$$t_{wDNF(max)} = (s) \times \frac{1}{f_s}$$

NOTE

Ext. signal pulses with a width between $t_{wDNF(min)}$ and $t_{wDNF(max)}$ may be suppressed or pass the filter.

(3) Minimum Delay Time

Minimum delay time is the minimum time that ext. signals need to propagate through the DNF, i.e. it is the path delay of the DNF.

$$t_{dDNF(min)} = (s-1) \times \frac{1}{f_s} + 2\left(\frac{1}{f_{DNFATCKI}}\right)$$

(4) Maximum Delay Time

Maximum delay time is the maximum time that ext. signals need to propagate through the DNF, i.e. it is the path delay of the DNF.

$$t_{dDNF(max)} = (s) \times \frac{1}{f_s} + 3\left(\frac{1}{f_{DNFATCKI}}\right)$$

(5) Formula Explanation

s is the number of sampling times (s = 2..5), depending on setting of register bit DNFAnCTL.DNFAnNFSTS;

fs is the sampling clock The sampling clock is derived from the DNF module input clock (DNFATCKI) as follows:

$$f_S = \frac{f_{DNFATCKI}}{PRS}$$

$f_{DNFATCKI}$ is the DNF module clock

PRS is the prescaler (PRS = 1, 2, 4, ..., 128), depending on the setting of register bit DNFAnCTL.DNFAnPRS;

NOTES

1. Please consider the register settings of the DNF while using the above mentioned formulas.
2. There is also a filter bypass available for each DNF. This should be used for high-speed application of the module function.

1.8 Analog Module Operating Conditions

1.8.1 Analog/Digital Converter (ADCE)

Condition: AWO = powered, ISO = powered

Table 1.64 ADC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Reference Voltages		A0VREF		2.7		A0VCC	V
Analog input voltage		V_{AIN}		0		A0VREF	V
Resolution				10		12	bit
A/D Converter system frequency	DS	f_{ADCLK}		8		40	MHz
Conversion time		t_{CONV}		1.15			µs
Overall Error*1	PC	TOE	10-bit mode, A0VCC = 4.5 to 5.5 V			±1	LSB
			10-bit mode, A0VCC = 3.6 to 4.5 V			±1.5	LSB
			10-bit mode, A0VCC = 2.7 to 3.6 V			±2	LSB
			12-bit mode, A0VCC = 4.5 to 5.5 V			±4	LSB
			12-bit mode, A0VCC = 3.6 to 4.5 V			±6	LSB
			12-bit mode, A0VCC = 2.7 to 3.6 V			±8	LSB
Conversion result for positive overload condition	PC		A0VREF = A0VCC ≤ AIN	4015 – |TOE| (12-bit mode) 1003 – |TOE| (10-bit mode)		4095 (12-bit mode) 1023 (10-bit mode)	LSB
Analog input pull-down resistance				350	500	650	kΩ
Analog supply current during normal operation	PC	I_{AVCC}				3.0	mA
Analog supply current during power-down	PC	I_{AVCCPD}			1		µA
Analog reference supply current	PC	I_{A0VREF}	During normal operation		500	1000	µA

Note 1. Not include quantization error.

Table 1.65 Self-diagnosis Characteristic

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Accuracy of self-diagnosis	TESH0SN	12-bit mode	Diagnosis voltage = A0VREF	4015 – |TOE|*1,*2		4095*1,*2	LSB
			Diagnosis voltage = 2/3 × A0VREF	2651 – |TOE|*1,*2	2731	2811 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/2 × A0VREF	1968 – |TOE|*1,*2	2048	2128 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/3 × A0VREF	1285 – |TOE|*1,*2	1365	1445 + |TOE|*1,*2	LSB
			Diagnosis voltage = A0VSS	0		80 + |TOE|*1,*2	LSB
	TESH0SN	10-bit mode	Diagnosis voltage = A0VREF	1003 – |TOE|*1,*2		1023*1,*2	LSB
			Diagnosis voltage = 2/3 × A0VREF	663 – |TOE|*1,*2	683	703 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/2 × A0VREF	492 – |TOE|*1,*2	512	532 + |TOE|*1,*2	LSB
			Diagnosis voltage = 1/3 × A0VREF	321 – |TOE|*1,*2	341	361 + |TOE|*1,*2	LSB
			Diagnosis voltage = A0VSS	0		20 + |TOE|*1,*2	LSB
Accuracy degradation of self-diagnosis on current injection	TESH0SND	Positive current injection = 0.1 mA		0		200	LSB
		Negative current injection = –0.1 mA		–100		0	LSB

Note: Not include quantization error

Note 1. For a reliable detection of the ADC faults it is necessary that the conversion voltage doesn't exceed the conversion range.

Note 2. The injected current during ADC self-diagnosis when A0VCC = 5 V has to be limited to 0.1 mA and no injected current is allowed during ADC self-diagnosis when A0VCC = 3.3 V or in 10-bit mode. Accuracy degradation shown in **Table 1.65** is measured on injected ±0.1 mA current to measurement pins.

CAUTION

Please be aware that the accuracy of the A/D Converter input channel is influenced by a exceeding voltage drop to the AVSS and AVCC power supply lines. This exceeding voltage drop is caused by a higher sum of total current that flows at adjacent digital pins with disabled A/D Converter input functionality (depending on number of switching digital output pins, load capacitance, sum of overload current, timing gap between IO output switching and sampling of A/D Converter input channel).

1.8.1.1 Equivalent Circuit of A/D Converter Input Pin

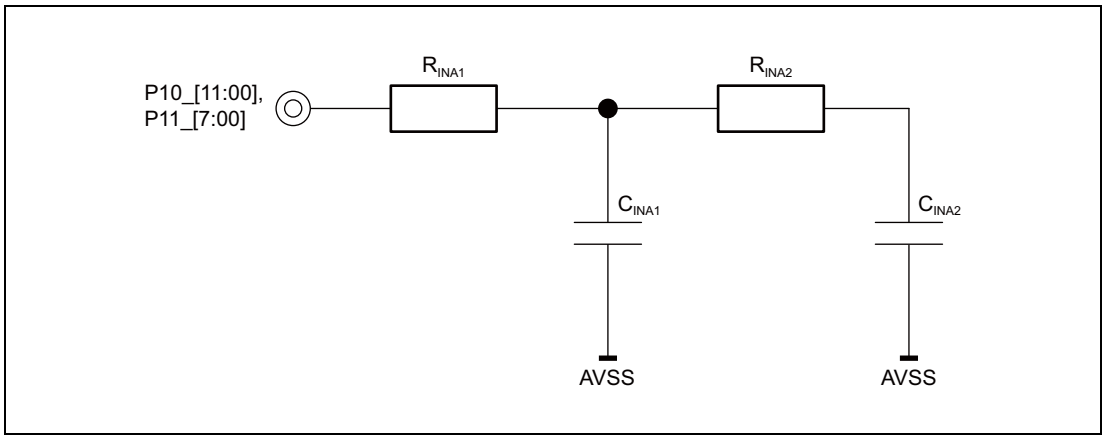


Figure 1.26 Equivalent Circuit of A/D Converter Input Pin - 2nd-order Model

Table 1.66 Analog Input Equivalent Circuit

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Analog input equivalent circuit resistance	DS*1	R_{INA1}			2.5		kΩ
		R_{INA2}			1.1		kΩ
Analog input equivalent circuit capacitance	DS*1	C_{INA1}			3.5		pF
		C_{INA2}			0.5		pF

Note 1. Not tested in production. Specified by design.

1.8.1.2 External Circuit on ADC Inputs

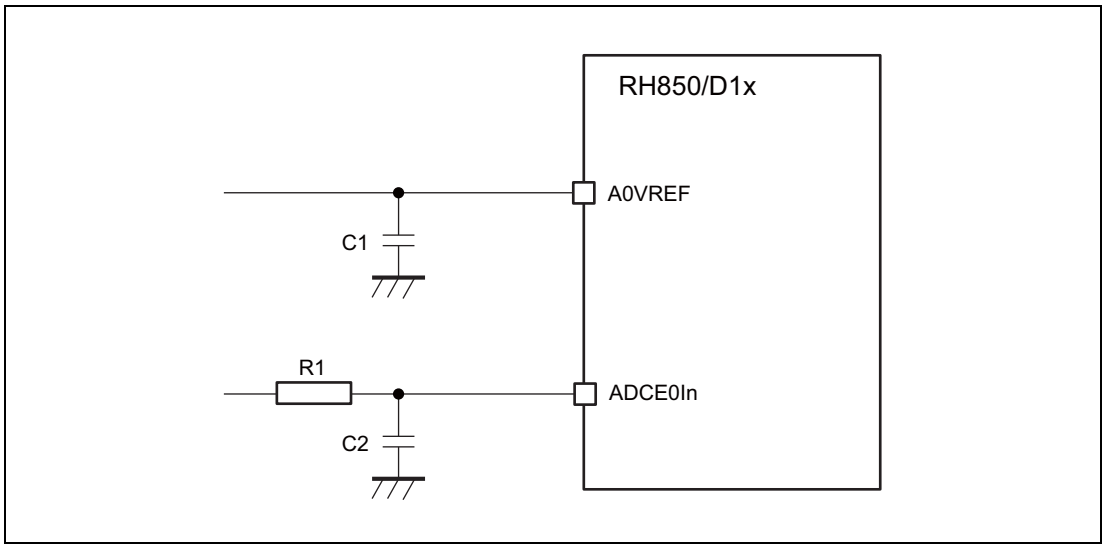


Figure 1.27 External Circuit on ADC Inputs

The external circuit on ADC input depends the input condition of user (filter condition). The characteristic of ADC is improved while R is small and C is large (about 0.1 µF). If R is large, ADC conversion error is occurred by dropping the voltage inputted ADCE0Im terminal. If C is small ADC input terminal cannot endure noise.

Component	Value
R1	10 kΩ
C1	100 nF
C2	10 nF

As guide line for the calculation of the external capacitor the formula based on the internal equivalent capacitance and the ADC resolution of the corresponding AD-converter channel can be used:

$C_{external} = C_{IN} \times 2$ ADC resolution

$C_{external}$: External capacitor

C_{IN}: Equivalent input capacitance (≈ CINA1 + CINA2)

1.8.1.3 A/D Converter Trigger Timing

Condition: The input incorporates a digital noise filter (DNF) in the input signal path. The filter function can be bypassed. If not bypassed the DNF filters all pulses that are shorter than the given high- and low-level width. Longer pulses are passed.

Table 1.67 ADCE0TRGn AC Characteristic

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCE0TRGn input high-level width	DS	t_{WADTH}	filtered (DNF)*1	t_{dDNF}(max) + 2 × t_{SYNC} + 5*2			ns
			filter-bypassed*3	2 × t_{SYNC} + 5			ns
ADCE0TRGn input low-level width		t_{WADTL}	filtered (DNF)	t_{dDNF}(max) + 2 × t_{SYNC} + 5*2			ns
			filter-bypassed	2 × t_{SYNC} + 5			ns
ADCE0TRGn input pulse rejection		t_{ADTRJ}	filtered (DNF)	t_{dDNF}(min) + t_{SYNC} + 5			ns
			filter-bypassed	t_{SYNC} + 5			ns

Note 1. Please consider the following SFR bit of the filter control module for selecting the filtered input signal: FCLA0CTLn.FCLA0BYPSn = 0

Note 2. 2 × t_{SYNC} is the delay time due to the synchronization of the input signal of the A/D Converter Trigger with the module clock of the A/D Converter module (t_{SYNC} = one module clock cycle).Note: Please consider the correct module clock of the A/D Converter

Note 3. Please consider the following SFR bit of the filter control module for selecting the filter-bypassed input signal: FCLA0CTLn.FCLA0BYPSn = 1

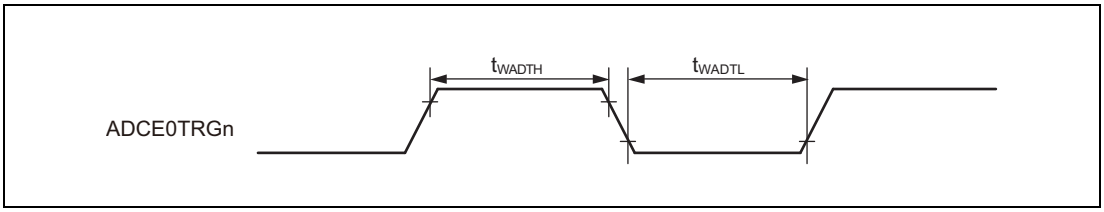


Figure 1.28 ADCE0TRGn Input Timing

1.8.1.4 How to Read A/D Converter Characteristics Table

This section describes the meanings of the terms peculiar to the A/D converter.

(1) Resolution

The minimum analog input voltage that can be identified, i.e. the ratio of the analog input voltage to 1 digital output is called 1 LSB (Least Significant Bit). The ratio of 1 LSB to the full scale is expressed as %FSR (Full Scale Range). %FSR is the ratio, in percentage, of the range in which an analog input voltage can be converted, and is expressed as follows regardless of the resolution.

1%FSR = (Maximum value of analog input voltage that can be converted - Minimum value of analog input voltage that can be converted) /100

= (AVrefp – AVrefm) /100

At a resolution of 10 bits the relation between 1 LSB and %FSR is as follows:

1 LSB = $1 / 2^{10}$

= 1 / 1,024

= 0.098 %FSR

At a resolution of 12 bits the relation between 1 LSB and %FSR is as follows:

1 LSB = $1 / 2^{12}$

= 1 / 4,096

= 0.024 %FSR

The accuracy is determined by the total error, regardless of the resolution.

(2) Total Error

This is the maximum value of the difference between the actually measured value and the theoretical value.

It is the total of the zero-scale error, full-scale error, linearity error, and a combination of these errors.

The total error shown in the characteristics table does not include the quantization error.

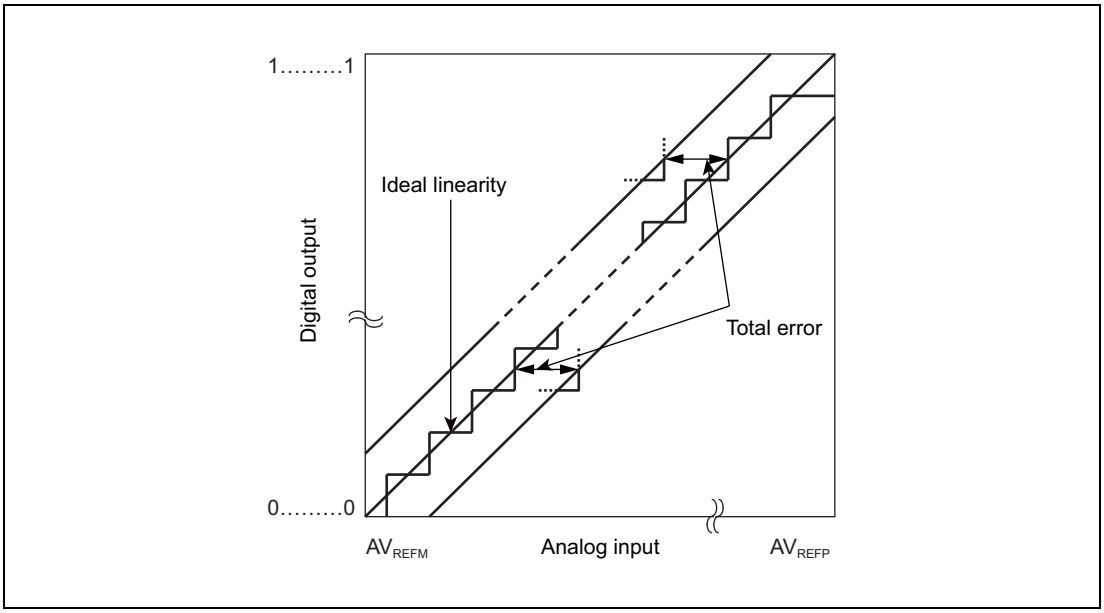


Figure 1.29 Total Error

(3) Quantization Error

This is the error of ±1/2 LSB that always occurs when an analog value is converted into a digital value. Because the A/D converter converts an analog input voltage in a range of ±1/2 LSB into the same digital code, the quantization error is unavoidable.

Note that this error is not included in the total error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

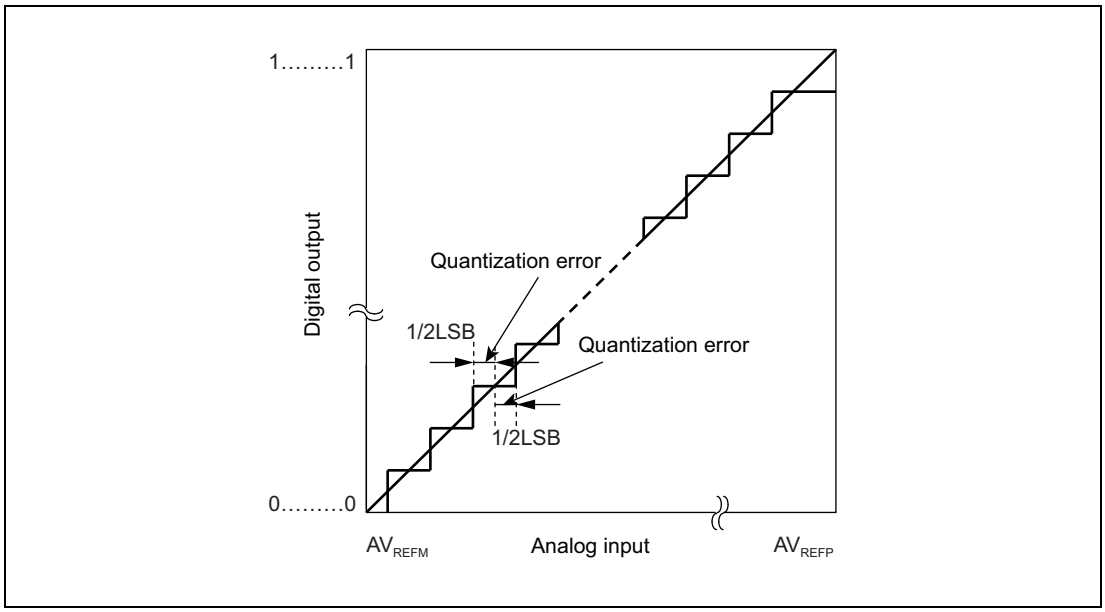
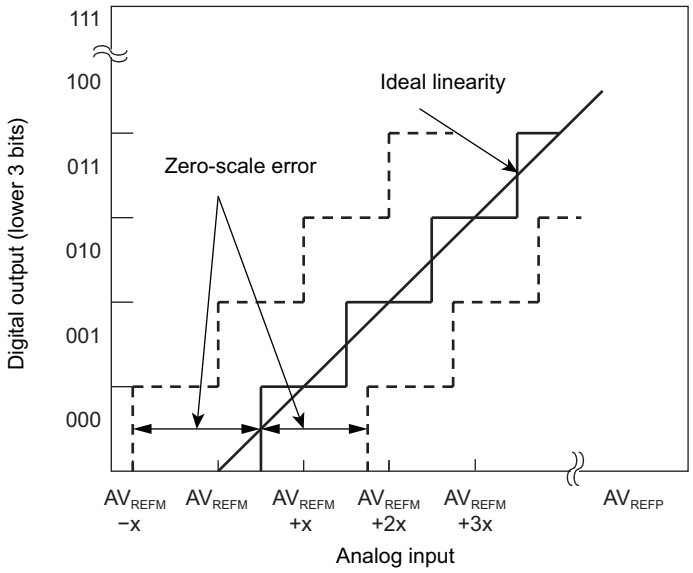


Figure 1.30 Quantization Error

(4) Zero-scale Error

This is the difference between the actually measured value of the analog input voltage and the theoretical value (1/2 LSB) when the digital output changes from 0…000 to 0…001.

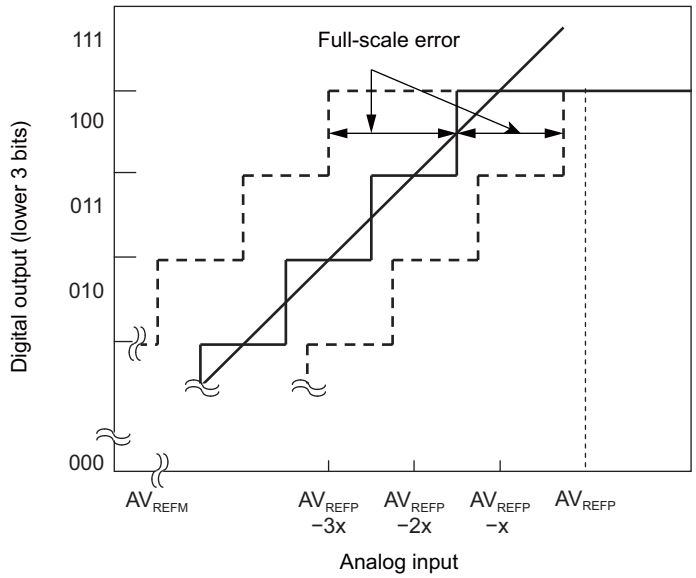


Note: x: voltage equivalent to 1 LSB
$x = (AV_{refp} - AV_{refm}) \times 1\ LSB$

Figure 1.31 Zero-scale Error

(5) Full-scale Error

This is the difference between the actually measured value of the analog input voltage and the theoretical value (full scale – 3/2 LSB) when the digital output changes from 1…110 to 1…111.



Note: x: voltage equivalent to 1 LSB
$x = (AV_{refp} - AV_{refm}) \times 1\ LSB$

Figure 1.32 Zero-scale Error

(6) Differential Linearity Error

Ideally, the width at which a specific code is output is 1 LSB. The differential linearity error is the difference between the actually measured value of the width at which a specific code is output and the ideal value.

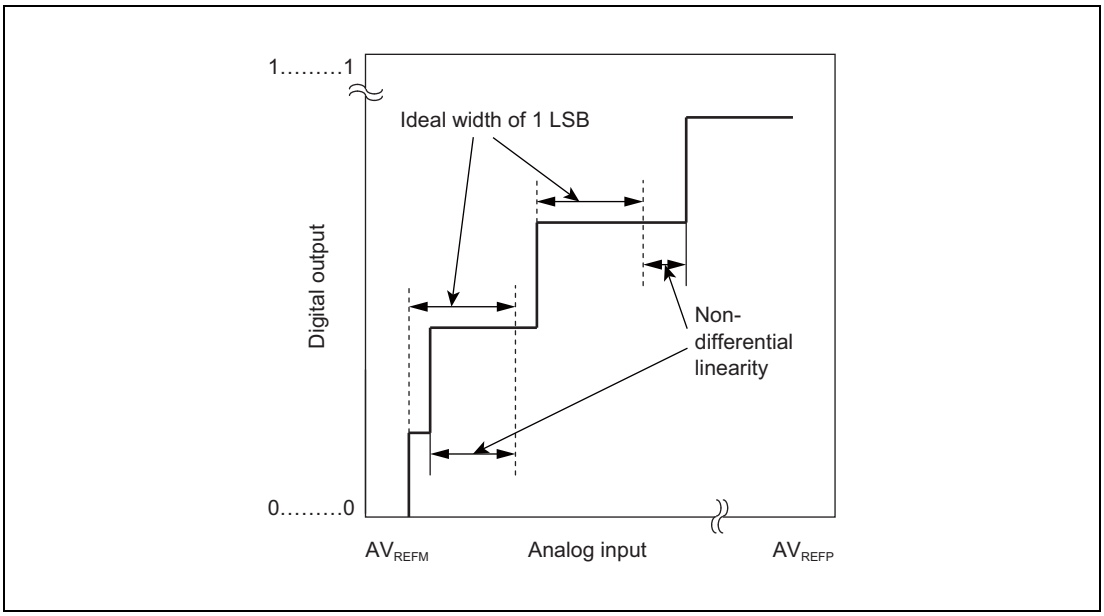


Figure 1.33 Differential Linearity Error

(7) Integral Linearity Error

This indicates the degree to which the conversion characteristic shifts from the ideal linearity, and indicates the maximum value of the difference between the actually measured value and the ideal linearity where the zero-scale error and full-scale error are 0.

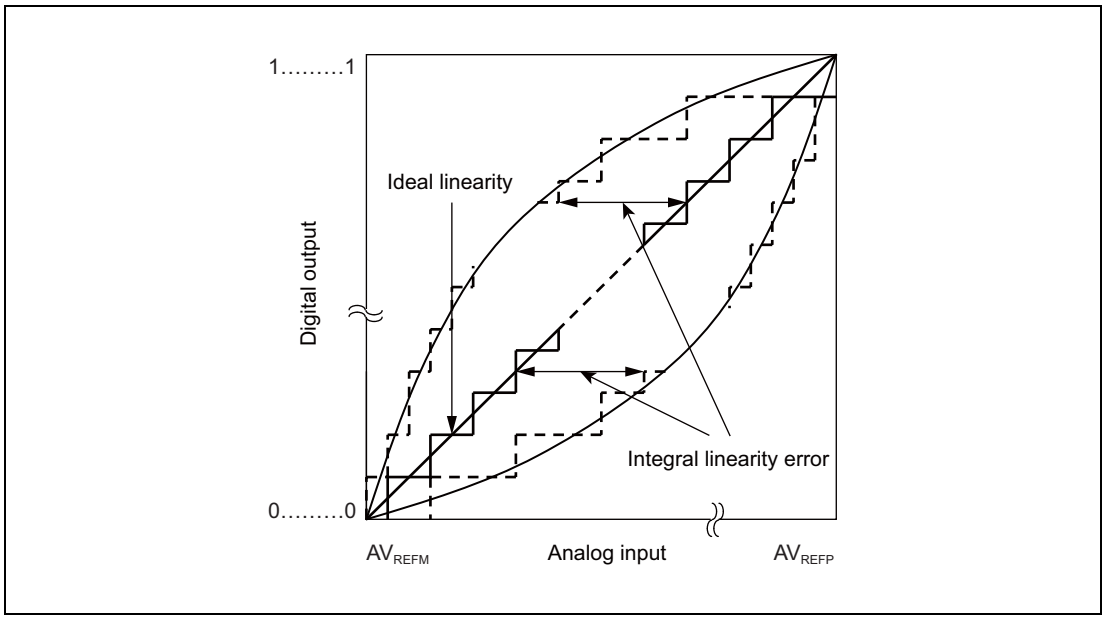


Figure 1.34 Integral Linearity Error

(8) Conversion Time

This is the time from when an analog voltage is input until digital output is produced.

The conversion time in the characteristics table includes sampling time.

(9) Sampling Time

This is the time during which the analog switch is on to input the analog voltage to the sample & hold circuit.

(10) A/D Start Time

This is the time from the A/D conversion trigger to the start of A/D conversion.

1.8.2 POC Characteristic

1.8.2.1 POC Characteristic on AWO

Condition: AWO = powered
REG0VCC = 2.7 to 5.5 V

CAUTIONS

1. The POC ensures that the devices stops operation ($\overline{\text{RESET}}$ condition) when the device is outside the operation voltage range, under the condition that the supply voltage slope on REG0VCC is ≤500V/ms.
2. Full device operation is only available, when the supply voltage is above the maximum threshold voltage. The device may stop operation due to reset condition generated by POC, if the supply voltage drops below the given max threshold voltage.

Table 1.68 POC Characteristic on AWO

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection threshold voltage		V_{POC0}	Power-on(Rise)	2.8	2.95	3.1	V
			Power-down(Fall)	2.8	2.9	3.0	V
POC threshold voltage hysteresis	DS*1	V_{POC0H}			2		mV
Response time at power up	DS*1	ts_{POC0R}	At power on(Rise) $V_{POC0ramp}$ = 0.00 to 0.5V/ms			2	ms
			At power on(Rise) $V_{POC0ramp}$ = 0.5 to 500V/ms			6.3	ms
			At power on(Rise) $V_{POC0ramp}$ = 0.00 to 20V/ms			2	ms
			At power on(Rise) $V_{POC0ramp}$ = 20 to 500V/ms			5	ms
Response time at power-down		ts_{POC0F}	$V_{POC0ramp}$ = 0.00 to 500V/ms			5	µs
POC0 supply voltage ramp*2	DS*1	$V_{POC0ramp}$		0.00		500	V/ms
POC minimum pulse width	DS*1	t_{POC0W}		0.2			ms
POC noise rejection width	DS*1	t_{POC0RJ}				30	ns

Note 1. Not tested in production. Specified by design.

Note 2. Up to the specified maximum POC0 supply voltage down ramp the POC0 ensures that the devices stops operation and enters a defined state (i.e. $\overline{\text{RESET}}$ condition).

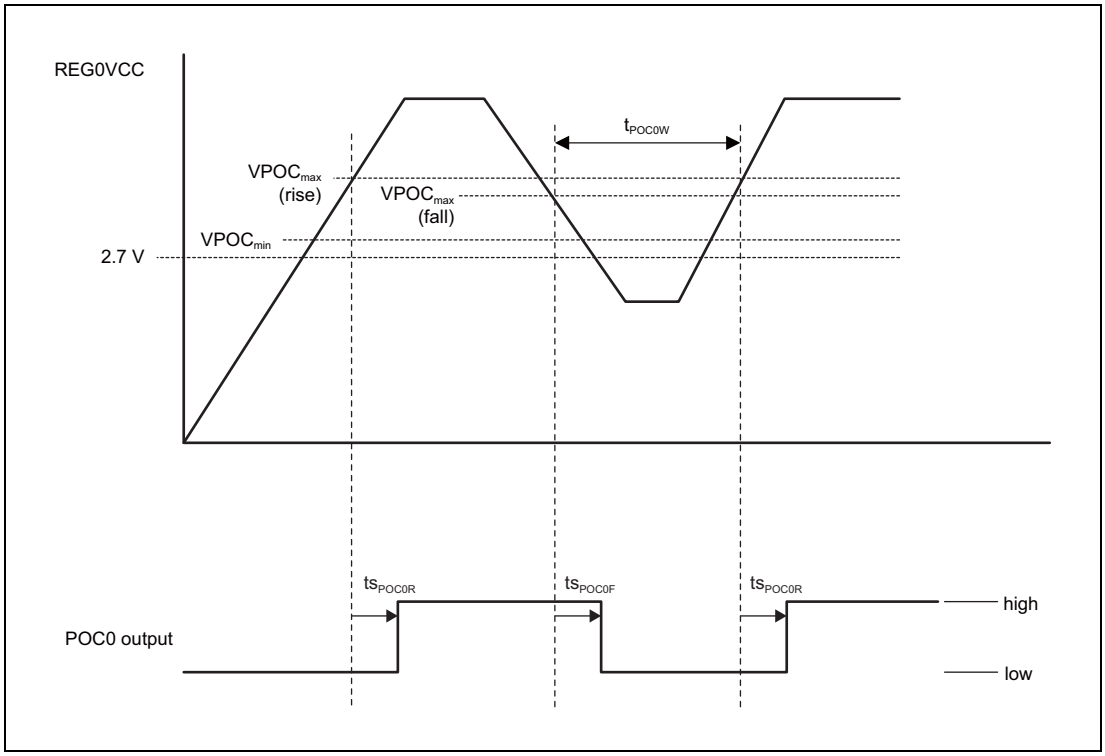


Figure 1.35 POC0 Timing

1.8.2.2 POC Characteristic on ISO (D1M1(H)/D1M1A/D1Lx)

Condition: AWO = powered, ISO = powered
REG1VCC = 2.7 to 5.5 V

CAUTION

The POC ensures that the ISO stops operation when the device is outside the operation voltage range, under the condition that the supply voltage slope on REG1VCC is ≤400V/ms.

Table 1.69 POC Characteristic on ISO

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
POC detection threshold voltage		V_{POC1}	Power-on(Rise)	2.8	2.95	3.1	V
			Power-down(Fall)	2.8	2.9	3.0	V
POC threshold voltage hysteresis	DS*1	V_{POC1H}			2		mV
Response time at power up	DS*1	ts_{POC1R}	At power on(Rise) $V_{POC1ramp}$ = 0.00 to 0.5V/ms			2	ms
			At power on(Rise) $V_{POC1ramp}$ = 0.5 to 400V/ms			6.3	ms
			At power on(Rise) $V_{POC1ramp}$ = 0.00 to 20V/ms			2	ms
			At power on(Rise) $V_{POC1ramp}$ = 20 to 400V/ms			5	ms
Response time at power-down		ts_{POC1F}	$V_{POC1ramp}$ = 0.00 to 400V/ms			5	µs
POC1 supply voltage ramp*2	DS*1	$V_{POC1ramp}$		0.00		400	V/ms
POC minimum pulse width	DS*1	t_{POC1W}		0.2			ms
POC noise rejection width	DS*1	t_{POC1RJ}				30	ns

Note 1. Not tested in production. Specified by design.

Note 2. Up to the specified maximum POC1 supply voltage down ramp the POC1 ensures that the devices stops operation and enters a defined state (i.e. $\overline{\text{RESET}}$ condition).

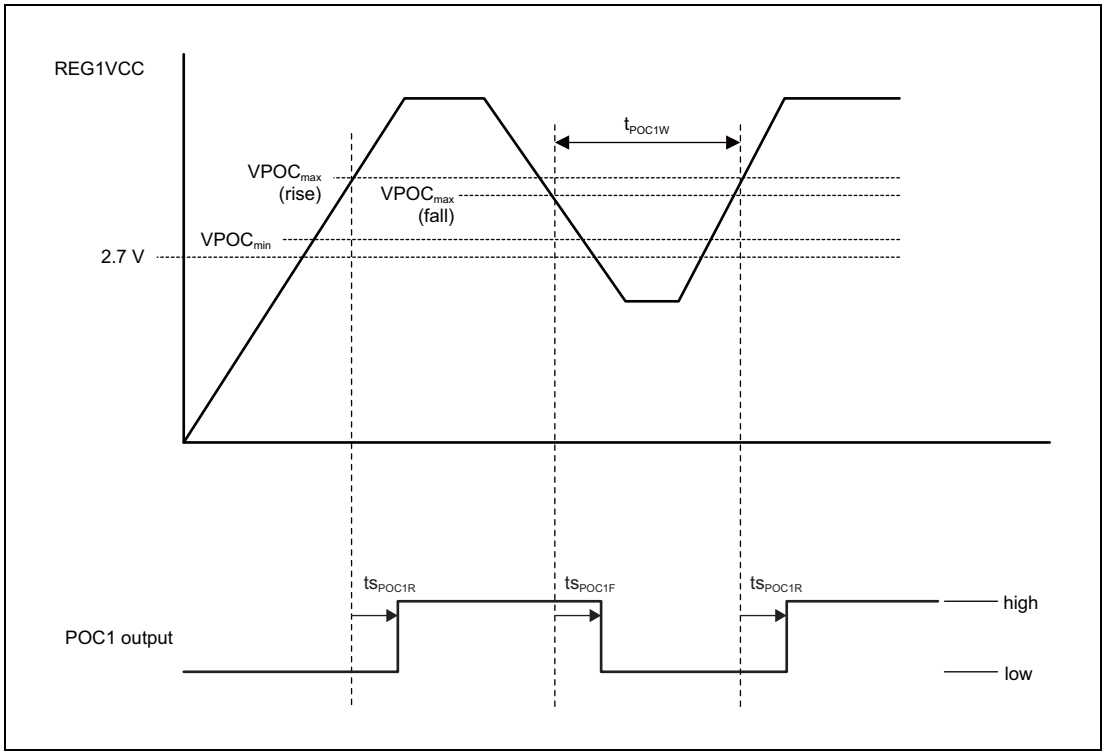


Figure 1.36 POC1 Timing

1.8.3 Zero Point Detection (ZPD)

The ZPD input path is an analog connection from the pad of a stepper motor driver (SMD) buffer to the ZPD module by-passing the digital input path of the general purpose input function of the SMD buffer.

Condition: AWO = powered, ISO = powered
ZPDVCC =4.5 to 5.5 V

Table 1.70 DC Characteristics Stepper Motor Driver Zero Point Detection

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Accuracy of ZPD comparator		Vth, ZPD	Internal reference, $V_{ZPD} \leq 350$ mV	–20		20	mV
		Vth, ZPD	Internal reference, $V_{ZPD} \geq 450$ mV	–30		30	mV
		Vth, ZPD	$V_{ZPD} = 0.2 \times$ ZPDVREF	–20		20	mV
Ext. ZPD reference voltage range		$ZPDV_{REF}$		0		5	V
Input pulse width[*1]	DS[*2]	t_{PW}		2			µs
Comparator output delay		t_{ZPDD}				1	µs
Dynamic current of ZPDVCC		I_{ZPDVCC}				2.0	mA

Note 1. The input pulse should have a minimum pulse width (TPW) to be detected properly. Shorter pulses may be ignored.

Note 2. Not tested in production. Specified by design.

NOTES

1. Six independent stepper motor channels (consisting of four SMD pins) can be measured by the ZPD.
2. For each stepper motor channel, 4 different inputs (SMD pins) can be selected for the ZPD.
3. Each stepper motor channel can be compared to 1 out of 3 reference voltages. Two of the reference voltages are generated based on Internal BGR and one is feed externally by a dedicated reference voltage port pin $ZPDV_{REF}$.
4. Each reference voltage(V_{ZPD}) is as follows.
   - Selection by ISMnGZPDCTL.ISMnGGRV1[3:0]
     – 100, 150, 215, 230, 235, 245, 250, 350, 450, 480, 500, 550, 650, 750, and 850 mV
   - Selection by ISMnGZPDCTL.ISMnGGRV2[3:0]
     – 150, 215, 225, 235, 245, 350, 450, 470, 480, 490, 500, 550, 650, 750, and 850 mV
5. The measurement itself is done by analogue comparators of the ZPD.
6. Each stepper motor channel has its own comparator.
7. For the timing of the ZPD function refer to **Figure 1.37, Timing of ZPD Function**.

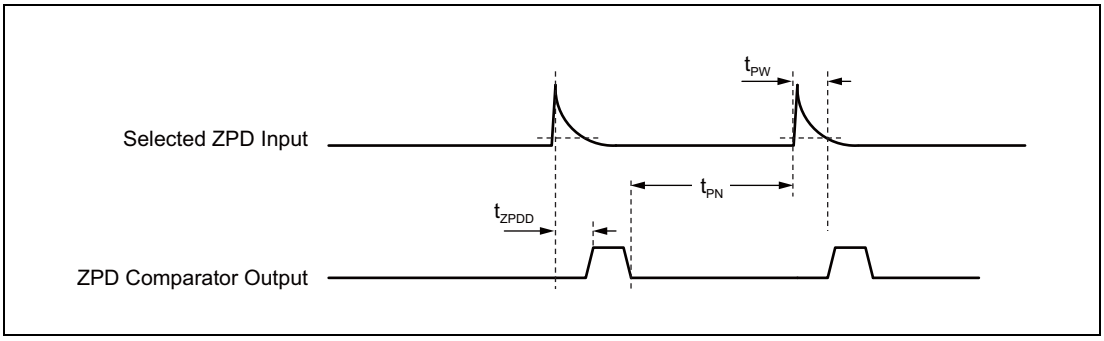


Figure 1.37 Timing of ZPD Function

Table 1.71 ZPDVREF Voltage Dividing Resistances

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage dividing resistance		R1			R2 × 4		kΩ
		R2			8		kΩ
Deviation of resistances		R_{dev}		–20		20	%

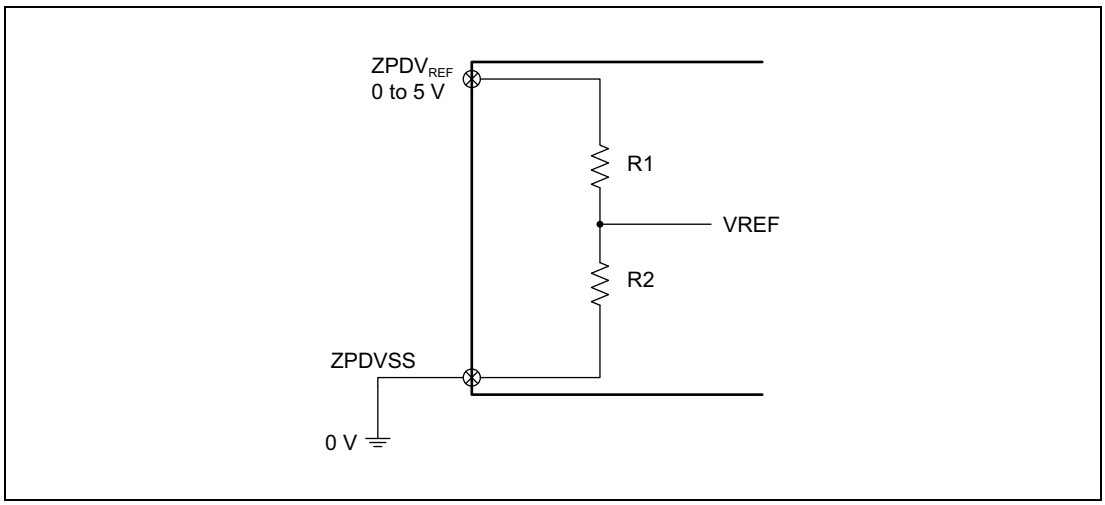


Figure 1.38 ZPD VREF Resistances

1.8.4 Temperature Sensor

Condition: AWO = powered, ISO = powered
REG1VCC = 3.0 to 5.5 V

Table 1.72 Temperature Sensor Specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Temperature detect Accuracy		Tj = –40 to 25°C	–10.0		10	°C
		Tj = 25 to 150°C	–5		5	°C
Stability time of output voltage			6.0			µs
Return time from Standby state					200.0	µs
Operation current					200.0	µA
Standby current					25.0	µA

1.9 Timer Module Operating Condition

1.9.1 Timer TAUB/TAUJ Timing

Table 1.73 Timer TAUB/TAUJ AC Specification*1

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUx high/low-level width	t_{TAUHNB} / t_{TAULNB}	filtered (DNF)	$t_{dDNF(max)}$ + 2 × t_{SYNC} + 5*2,*3			ns
		filter-bypassed	2 × t_{SYNC} + 5			ns
TAUx pulse rejection	t_{TAURJ}	filtered (DNF)	$t_{dDNF(min)}$ + t_{SYNC} + 5*2			ns
		filter-bypassed	t_{SYNC} + 5			ns

Note 1. The external input incorporates a digital noise filter (DNF). Using a filter control macro this DNF can be placed into the input signal path. The filter control macro can also be used to bypass the DNF.

Note 2. Please refer to **Section 1.7.6, General Digital Noise Filter (DNF) Specification**.

Note 3. 2 × t_{SYNC} is the delay time due to the synchronization of the input signal of the Timer TAUx with the macro clock of the Timer TAUx (t_{SYNC} = one macro clock cycle)

1.10 Serial Interface Module Operating Condition

1.10.1 LIN / UART Interface

Table 1.74 LIN / UART AC Specification

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate UART	t_{UARTR}		0.3		1000.0	Kbps
Transfer rate LIN	t_{LIN}		1		115.2	Kbps
UART/LIN RX pulse rejection	t_{UARTRJ}		$t_{PCLK} \times 2^{PRS}$			ns

Note: PRS is the RLIN3/UART clock prescaler division value, set in the macro register. Please refer the prescaler function in Users Manual.

1.10.2 Synchronous Interface CSIG

1.10.2.1 Master Mode

Table 1.75 Master Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock output cycle time	t_{KCYM}		100.0			ns
Clock output high level width	t_{KWHM}		0.5 × t_{KCYM} – 10.0			ns
Clock output low level width	t_{KWLM}		0.5 × t_{KCYM} – 10.0			ns
Data input setup time	t_{SSIM}	filtered (DNF)	29 + $t_{dDNFSI(max)}$			ns
		filter-bypassed	29			ns
Data input hold time	t_{HSIM}	filtered (DNF)	0 – $t_{dDNF(max)}$			ns
		filter-bypassed	0			ns
Data output delay max time	t_{DSOM}				5.0	ns
Data output delay min time	t_{HSOM}		–20			ns
Ready / Busy input signal (CSIGnRY) setup time	t_{SRYI}	filtered (DNF)	2 × t_{KCY} + $t_{dDNF(max)}$ + 16.6			ns
		filter-bypassed	2 × t_{KCY} + 16.6			ns
Ready / Busy input signal (CSIGnRY) high level width	t_{WRYI}	filtered (DNF)	t_{KCY} + $t_{dDNFRY(max)}$ – 5			ns
		filter-bypassed	t_{KCY} – 5			ns

(1) [CSIGnSC / CSIGnSO] Output Pins and [CSIGnSI] Input Pin in Master Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

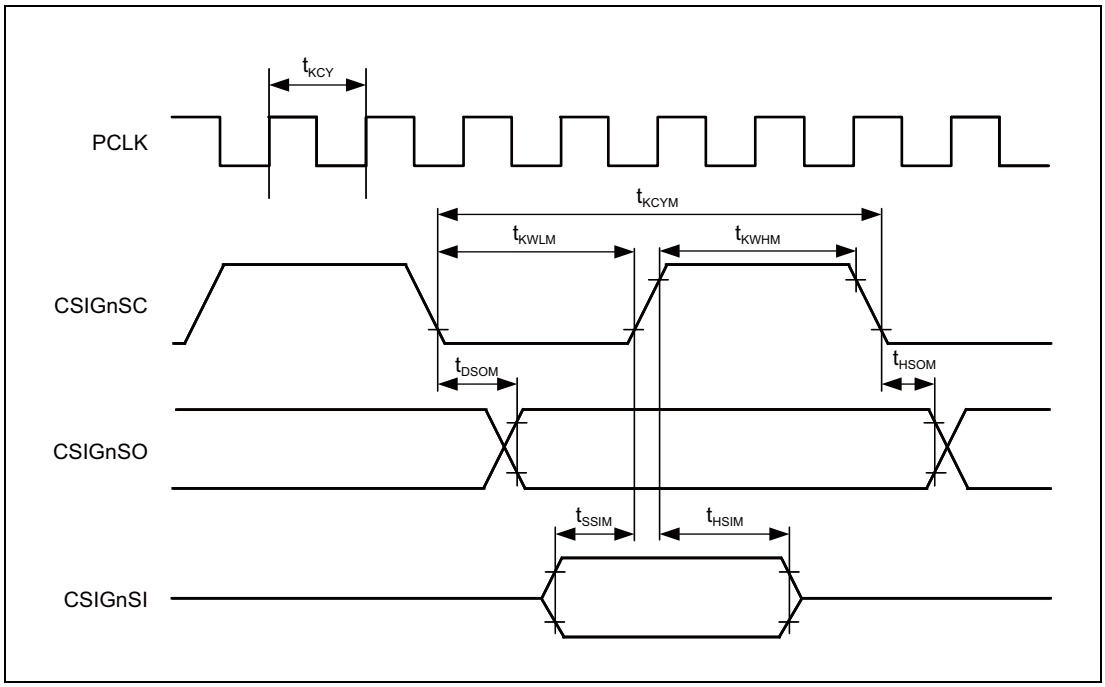


Figure 1.39 CSIGn Master Mode Timing (a)

(2) [CSIGnSC / CSIGnSO] Output Pins and [CSIGnSI] Input Pin in Master Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

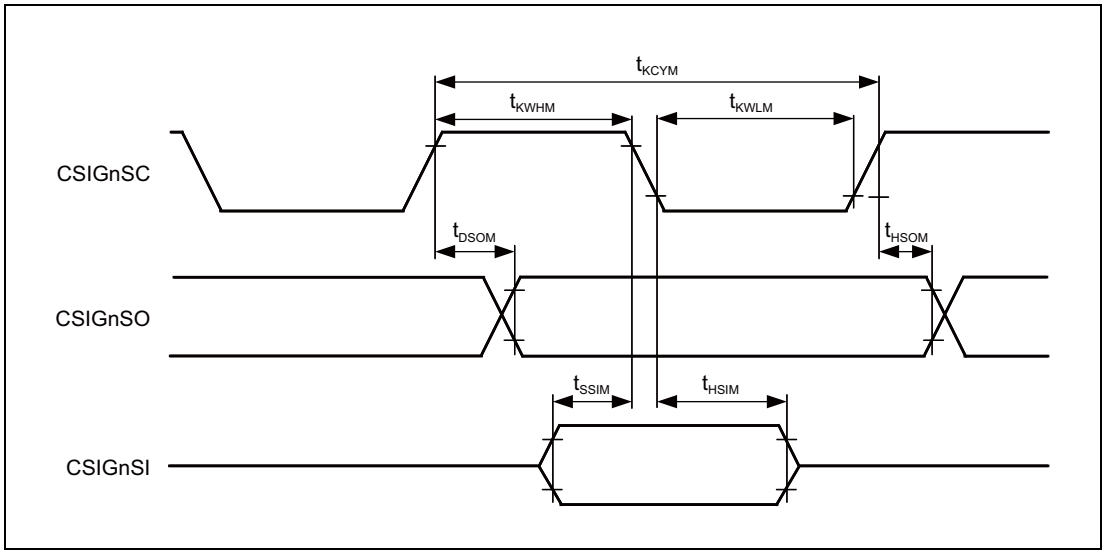


Figure 1.40 CSIGn Master Mode Timing (b): Inverted Clock2

(3) [CSIGnSC] Output Pin and [CSIGnRY] Input Pin in Master Mode

Note: Settings: CSIGnCTL1.CSIGnSIT=0, CSIGnCTL1.CSIGnHSE=1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

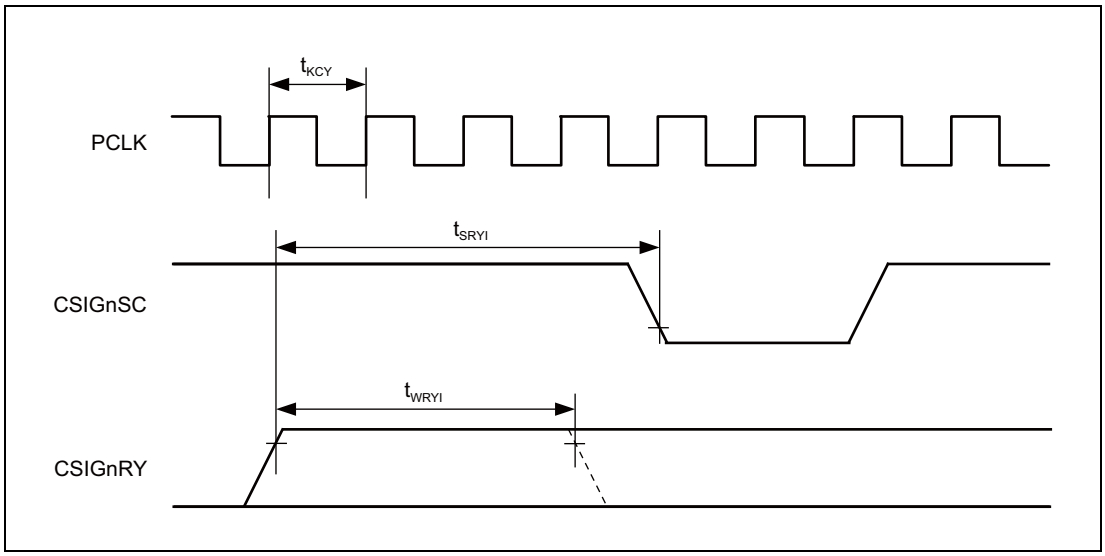


Figure 1.41 CSIGn Master Mode Timing (c): Ready / Busy Input Signal (CSIGnRY)

(4) [CSIGnSC] Output Pin and [CSIGnRY] Input Pin in Master Mode

Note: Settings: CSIGnCTL1.CSIGnSIT=0, CSIGnCTL1.CSIGnHSE=1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

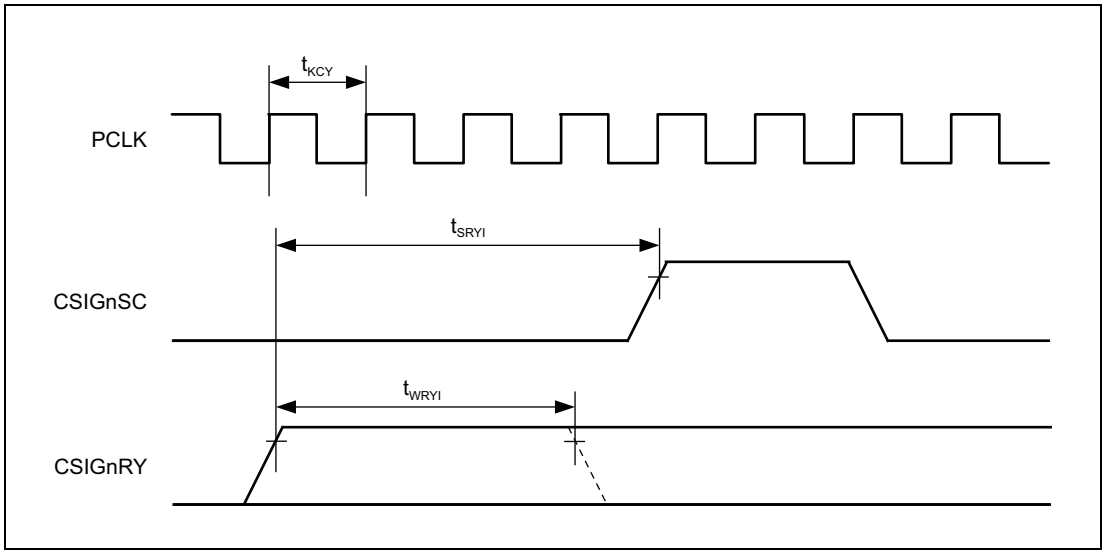


Figure 1.42 CSIGn Master Mode Timing (d): Ready / Busy Input Signal (CSIGnRY) - Inv.Clock

(5) [CSIGnSC / CSIGnDCS] Input Pins in Master Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

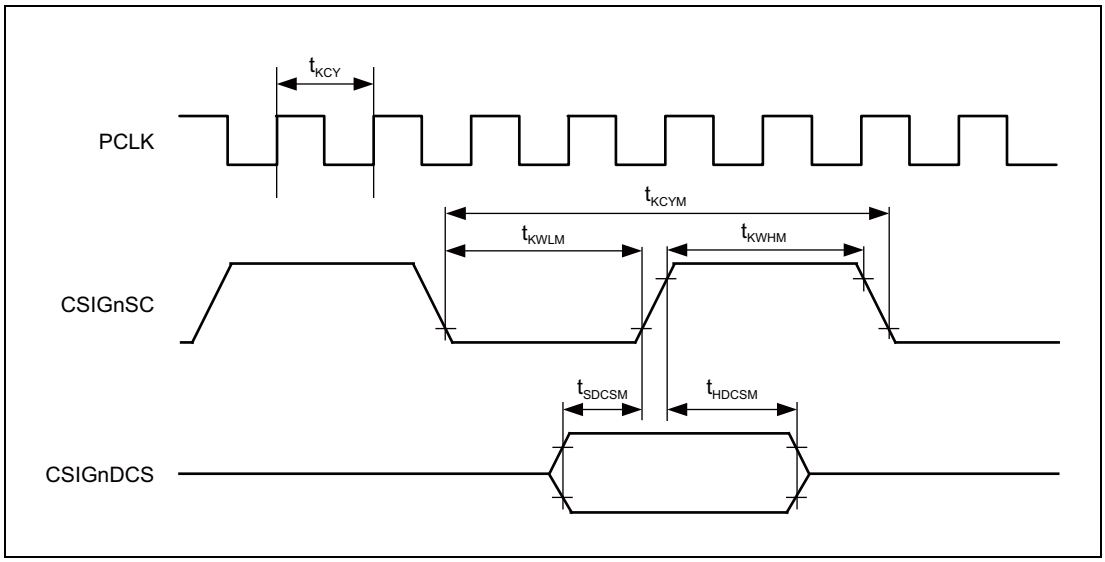


Figure 1.43 CSIGn Master Mode Timing (e): Data Consistency Check (CSIGnDCS)

(6) [CSIGnSC / CSIGnDCS] Input Pins in Master Mode

Note: Settings: CSIGnCTL1.CSIGnDCS=1, CSIGnCTL1.CSIGnCKR=0 (consider CSIGnCFG0.CSIGnDAP bit)

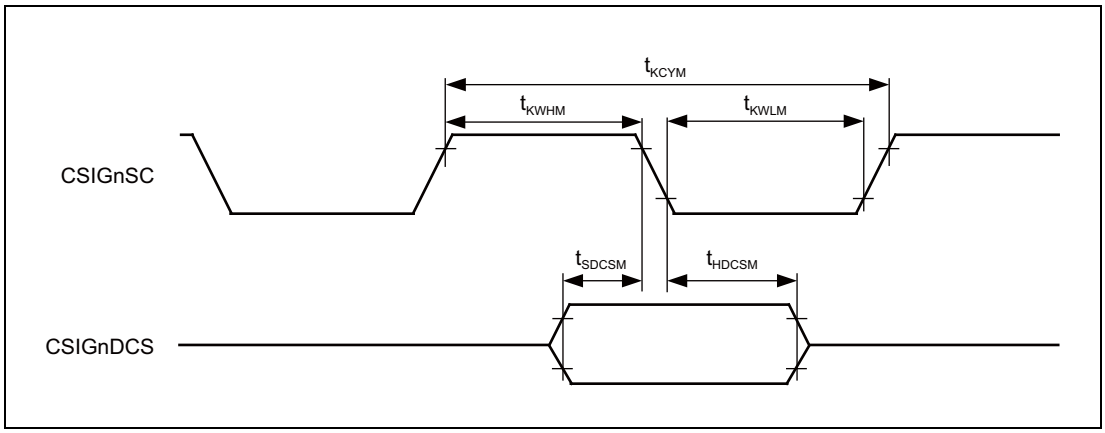


Figure 1.44 CSIGn Master Mode Timing (f): Data Consistency Check (CSIGnDCS) - Inverted Clock

1.10.2.2 Slave Mode

Table 1.76 Slave Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock input cycle time	t_{KCYM}	filtered (DNF)	$8 \times t_{dDNFSCI(max)}$			ns
		filter-bypassed	75			ns
Clock input high level width	t_{KWHS}	filtered (DNF)	$4 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	32.5			ns
Clock input low level width	t_{KWLS}	filtered (DNF)	$4 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	32.5			ns
Data input setup time	t_{SSIS}	filtered (DNF)	$7 + t_{dDNFSCI(min)} - t_{dDNFSI(max)}$			ns
		filter-bypassed	7.5			ns
Data input hold time	t_{HSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{KCY}$			ns
Data output delay time	t_{DSOS}	filtered (DNF)			$35 + t_{dDNFSCI(max)}$	ns
		filter-bypassed			35	
Slave select control input signal setup time	t_{SSSIS}	filtered (DNF)	$0.5 \times t_{KCYS} + t_{dDNFSCI(min)} - t_{dDNFSI(max)} - 7$			ns
		filter-bypassed	$0.5 \times t_{KCYS} - 5$			ns
Slave select control input signal hold time	t_{HSSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{CKYS} - 5$			ns
Ready / Busy output signal (CSIG0RY) output delay time	t_{DRYO}	filtered (DNF)			$35 + t_{KCY} + t_{dDNFSCI(max)}$	ns
		filter-bypassed			$35 + t_{KCY}$	ns

(1) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

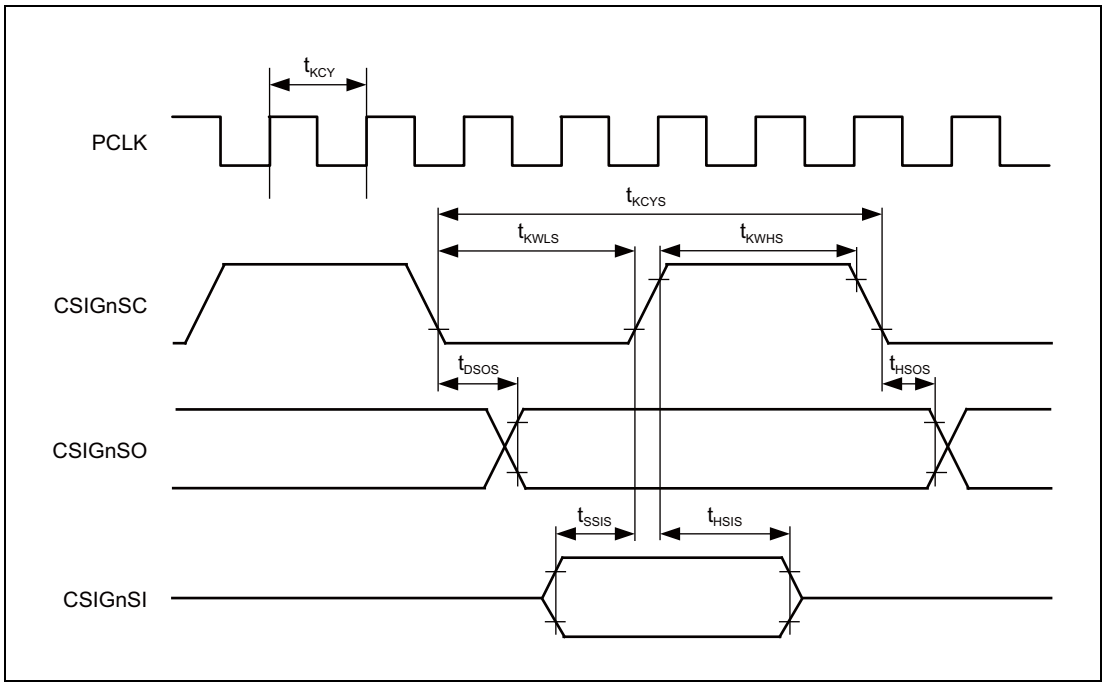


Figure 1.45 CSIGn Slave Mode Timing (a)

(2) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Setting: CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

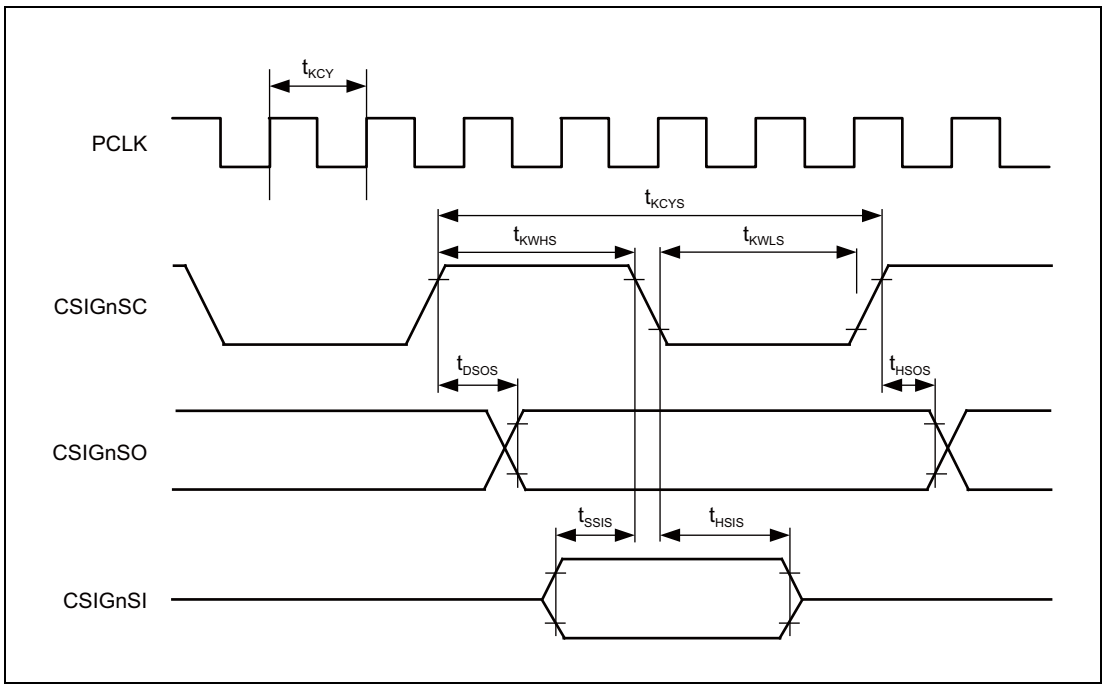


Figure 1.46 CSIGn Slave Mode Timing (b) - Inverted Clock

(3) [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnSSE = 1, CSIGnCTL1.CSIGnCKR=0 (consider CSIGnCFG0.CSIGnDAP bit)

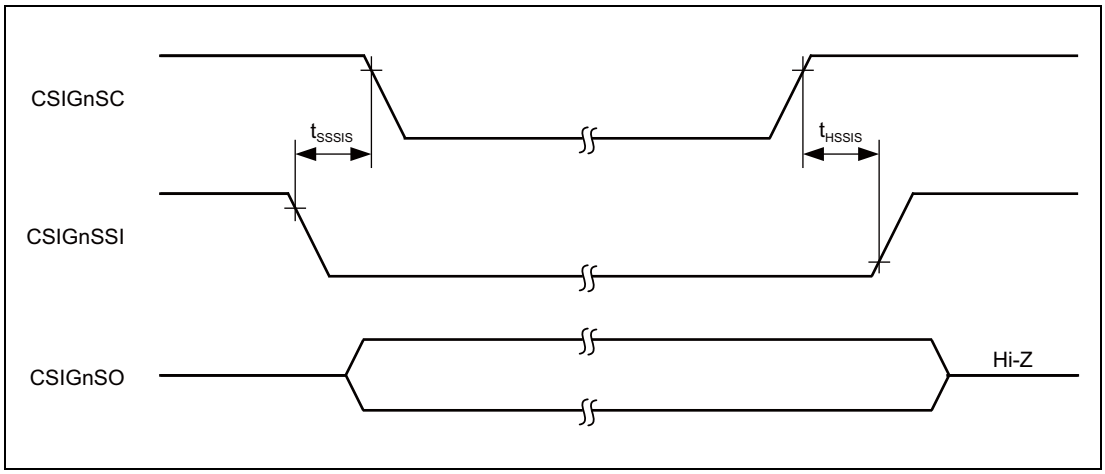


Figure 1.47 CSIGn Slave Mode Timing (c): Slave Select Ctrl Input (CSIGnSSI)

(4) [CSIGnSC / CSIGnSSI] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnSSE = 1, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

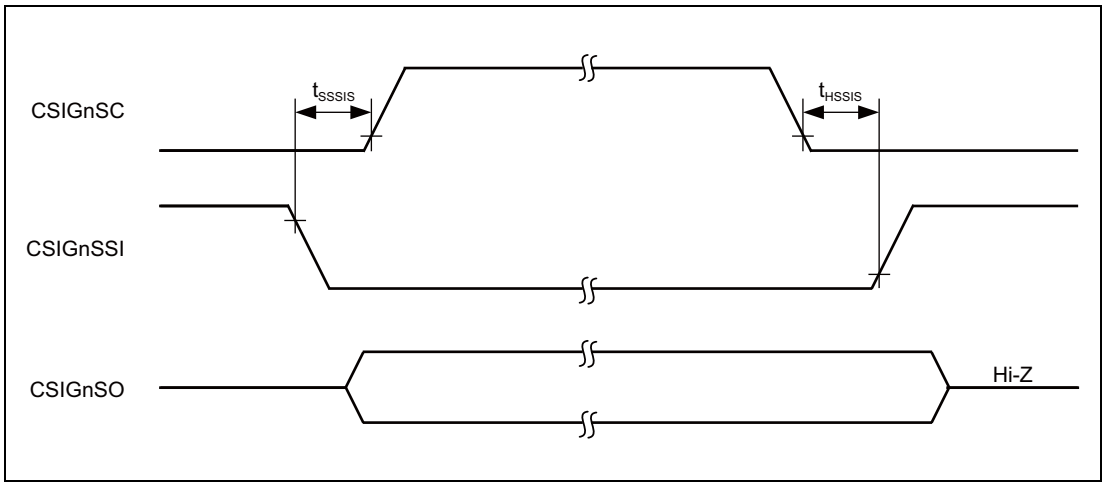


Figure 1.48 CSIGn Slave Mode Timing (d): Slave Select Ctrl Input (CSIGnSSI) - Inverted Clock

(5) [CSIG0SC] Input Pin and [CSIG0RY] Output Pin in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

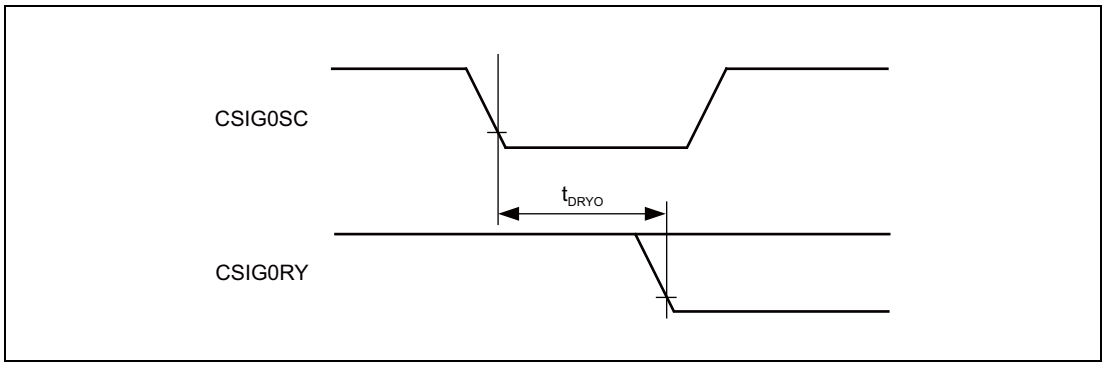


Figure 1.49 CSIGn Slave Mode Timing (e): Ready / Busy Output Signal (CSIGnRY)

(6) [CSIG0SC] Input Pin and [CSIG0RY] Output Pin in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

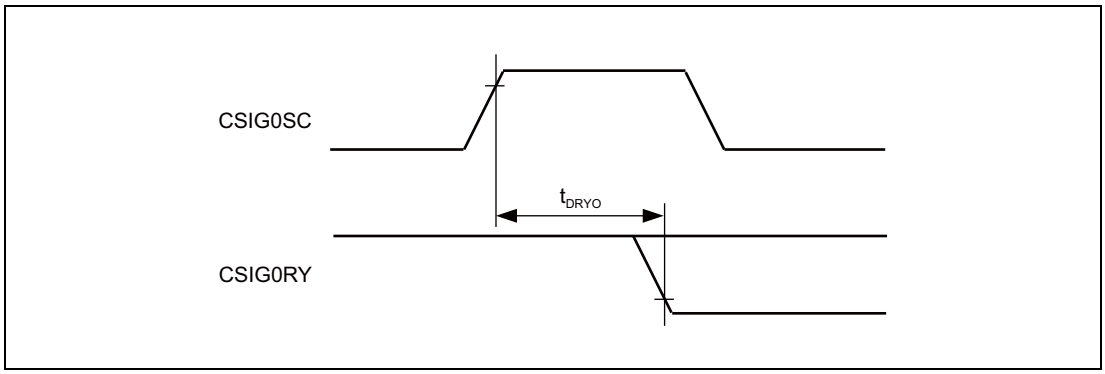


Figure 1.50 CSIGn Slave Mode Timing (f): Ready / Busy Output Signal (CSIGnRY) - Inverted Clock

(7) [CSIGnSO] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

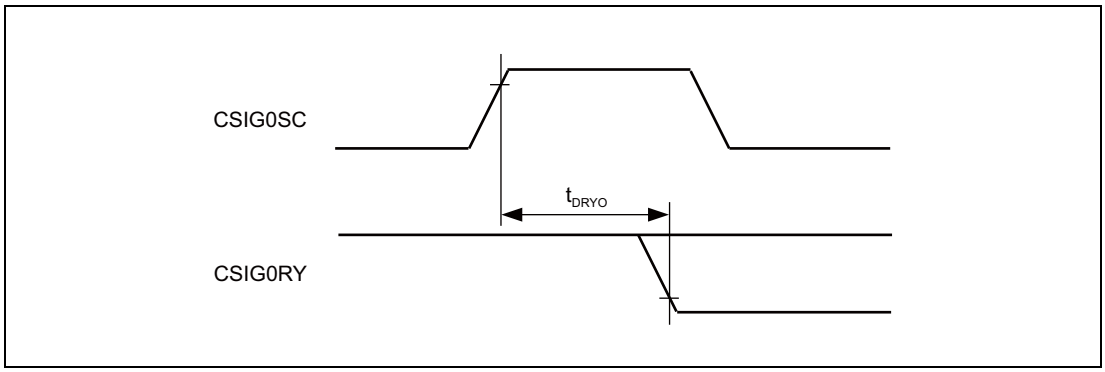


Figure 1.51 CSIGn Slave Mode Timing (g): Ready / Busy Output Signal (CSIGnRY)

(8) [CSIG0SC] Output Pin and [CSIGnSC / CSIGnSI] Input Pins in Slave Mode

Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 1 (consider CSIGnCFG0.CSIGnDAP bit)

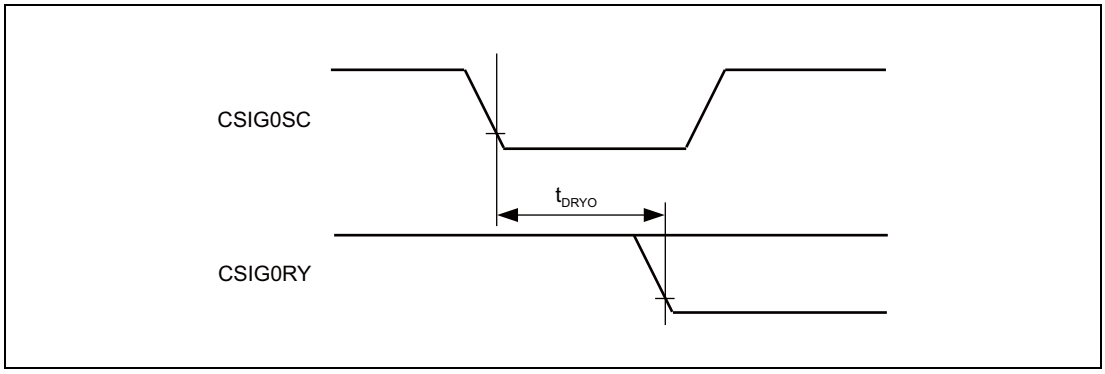


Figure 1.52 CSIGn Slave Mode Timing (h): Ready / Busy Output Signal (CSIGnRY) - Inverted Clock

(9) [CSIGnSC, CSIGnDCS] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

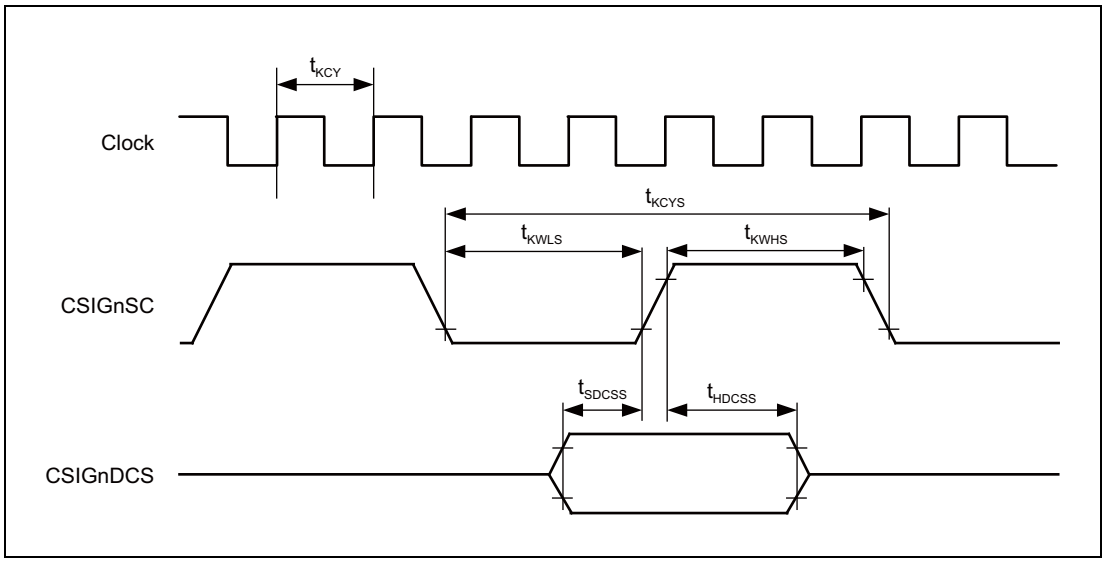


Figure 1.53 CSIGn Slave Mode Timing (h): Data Consistency Check (CSIGnDCS).CSIGnDAP bit)

(10) [CSIGnSC, CSIGnDCS] Input Pins in Slave Mode

Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 0 (consider CSIGnCFG0.CSIGnDAP bit)

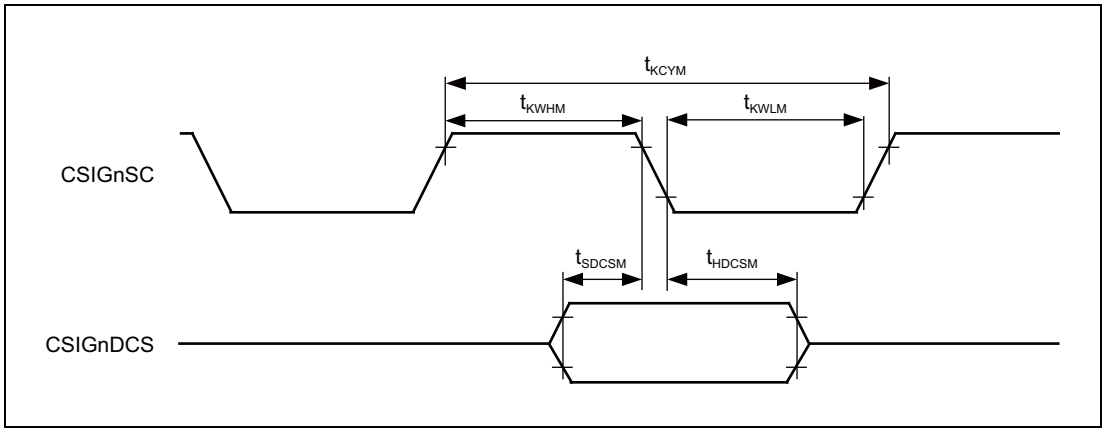
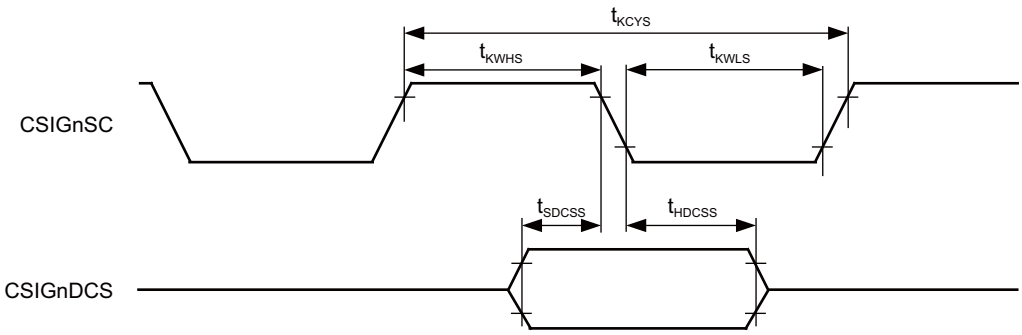
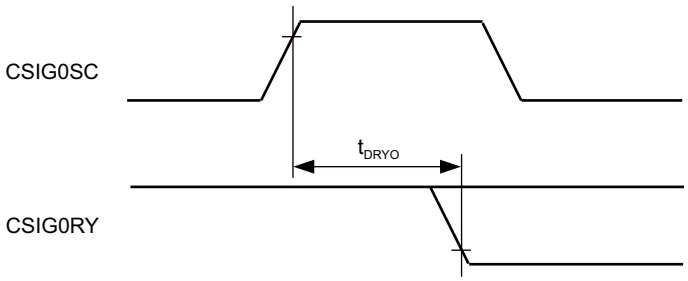


Figure 1.54 CSIGn Slave Mode Timing (i): Data Consistency Check (CSIGnDCS).CSIGnDAP bit) - Inverted Clock



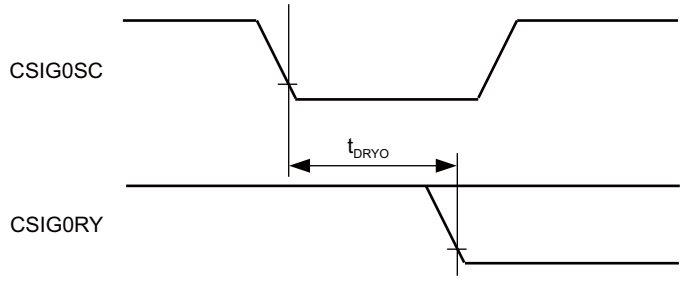
Note: Settings: CSIGnCTL1.CSIGnDCS = 1, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.55 Slave Mode Wave Form6



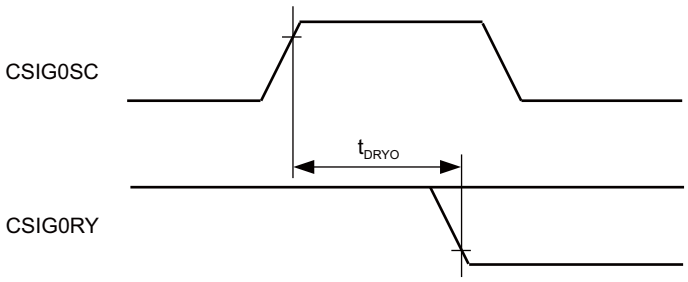
Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.56 Slave Mode Wave Form7



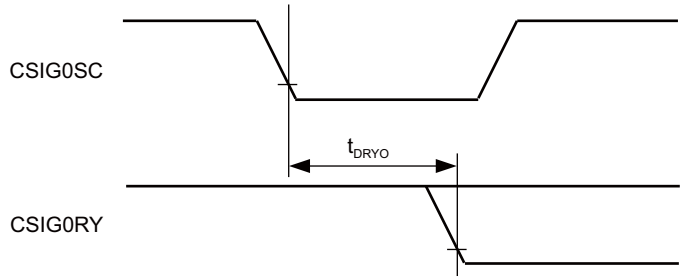
Note: Settings: CSIG0CFG0.CSIG0CKP = 0, CSIGnCTL1.CSIGnCKR = 0
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.57 Slave Mode Wave Form8



Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 0
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.58 Slave Mode Wave Form9



Note: Settings: CSIG0CFG0.CSIG0CKP = 1, CSIGnCTL1.CSIGnCKR = 1
(consider CSIGnCFG0.CSIGnDAP bit)

Figure 1.59 Slave Mode Wave Form10

1.10.3 Synchronous Interface CSIH

1.10.3.1 Master Mode

Table 1.77 Master Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock output cycle time	t_{KCYM}		50.0			ns
Clock output high level width	t_{KWHM}		$0.5 \times t_{KCYM} - 10.0$			ns
Clock output low level width	t_{KWLM}		$0.5 \times t_{KCYM} - 10.0$			ns
Data input setup time	t_{SSIM}	filtered (DNF)	$17 + t_{dDNFSI(max)}$*1			ns
		filter-bypassed	17*2			ns
Data input hold time	t_{HSIM}	filtered (DNF)	$0 - t_{dDNF(max)}$			ns
		filter-bypassed	0			ns
Data output delay max time	t_{DSOM}				5.0	ns
Data output delay min time	t_{HSOM}		–10			ns
Ready / Busy input signal (CSIHnRY) setup time	t_{SRYI}	filtered (DNF)	$2 \times t_{KCY} + t_{dDNF(max)} + 16.6$			ns
		filter-bypassed	$2 \times t_{KCY} + 16.6$			ns
Ready / Busy input signal (CSIHnRY) high level width	t_{WRYI}	filtered (DNF)	$t_{KCY} + t_{dDNFRY(max)} - 5$			ns
		filter-bypassed	$t_{KCY} - 5$			ns
CSS signal (CSIHnCSS) inactive width	t_{WSCSB}		$CSIDLE \times t_{KCY} - 5$			ns
CSS signal (CSIHnCSS) setup time	t_{SSCSB0}	CSIHnDAP=0	$CSSETUP \times t_{KCY} - 24$			ns
		CSIHnDAP=1	$(CSSETUP + 0.5) \times t_{KCY} - 24$			ns
CSS signal (CSIHnCSS) hold time	t_{HSCSB0}	CSIHnSIT=0	$CSHOLD \times t_{KCY} - 3$			ns
		CSIHnSIT=1	$(CSHOLD + 0.5) \times t_{KCY} - 3$			ns

Remark: CSIDLE: setting value of CSIHnCFGx.CSIHnIDx0-2
CSSETUP: setting value of CSIHnCFGx.CSIHnSPx3-0
CSHOLD: setting value of CSIHnCFG0-7.CSIHnHDx3-0

Note 1. In case of version 1 samples of RH850/D1L2(R7F701402), the value is 30 + $t_{dDNFSI(max)}$.

Note 2. In case of version 1 samples of RH850/D1L2(R7F701402), the value is 30.

Timing waveforms are same as master mode of CSIH (except CSS).

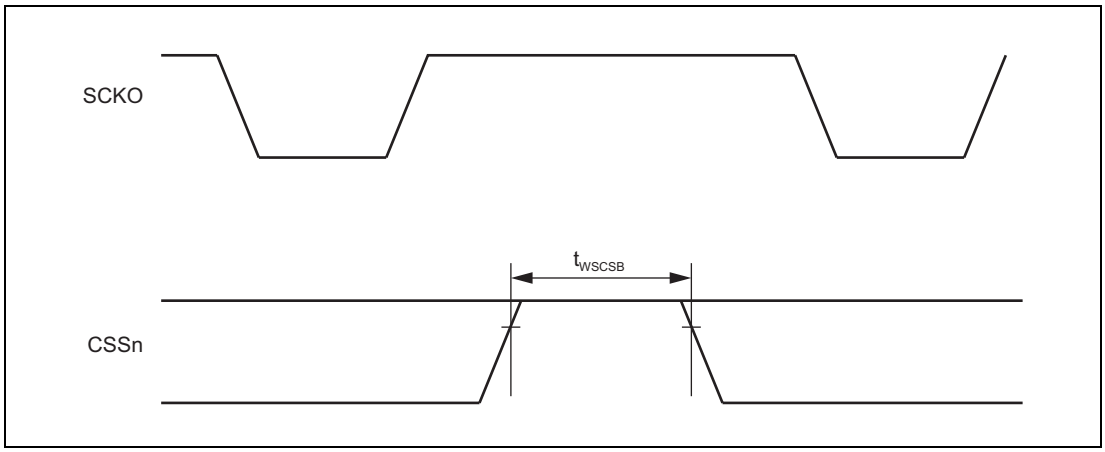
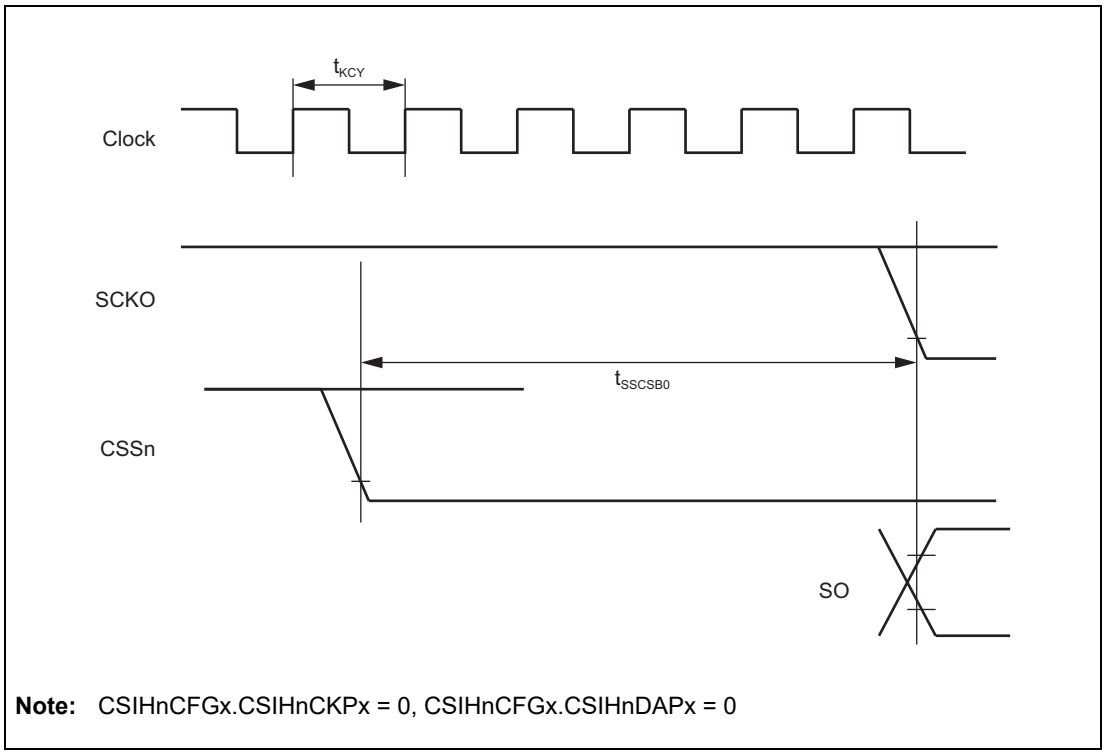
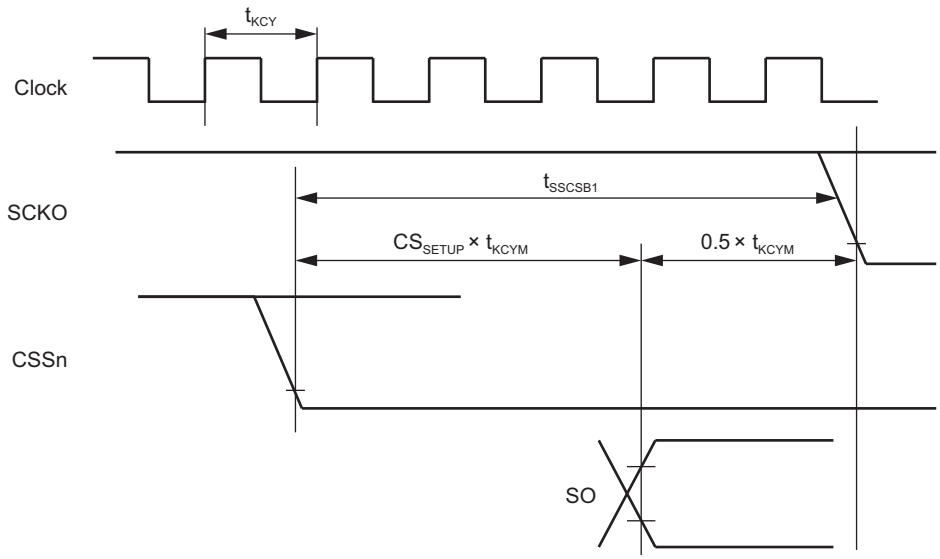


Figure 1.60 CSIH Master Mode Wave Form1



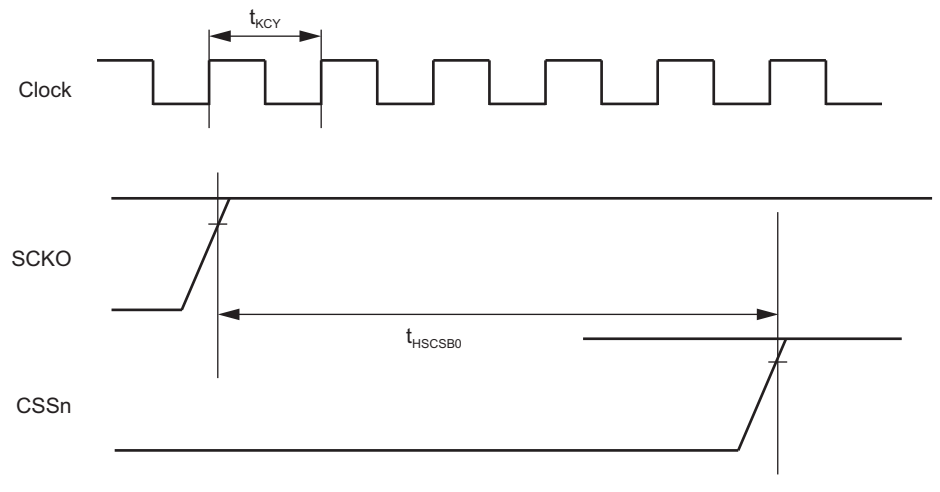
Note: CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.61 CSIH Master Mode Wave Form2



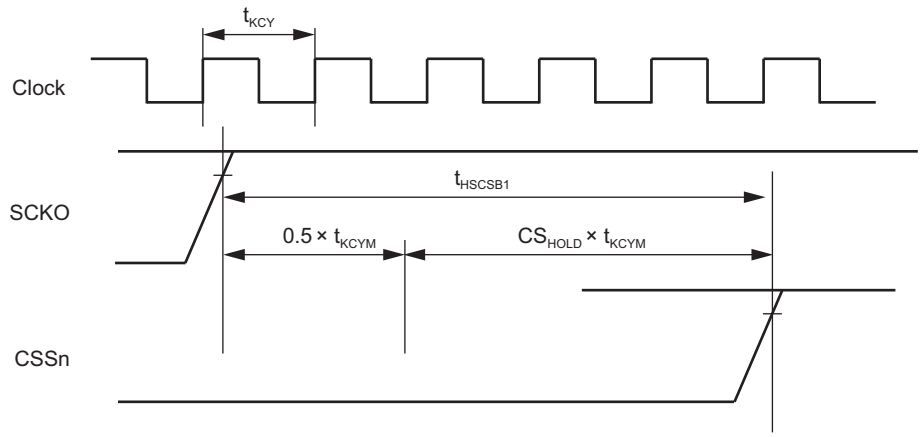
Note: CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 1

Figure 1.62 CSIH Master Mode Wave Form3



Note: CSIH0CTL1.CSIH0SIT = 0, CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.63 CSIH Master Mode Wave Form4



Note: CSIH0CTL1.CSIH0SIT = 1, CSIHnCFGx.CSIHnCKPx = 0, CSIHnCFGx.CSIHnDAPx = 0

Figure 1.64 CSIH Master Mode Wave Form5

1.10.3.2 Slave Mode

Table 1.78 Slave Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
PCLK frequency	t_{KCYf}				80	MHz
PCLK cycle time	t_{KCY}		12.5			ns
Clock input cycle time	t_{KCYM}	filtered (DNF)	$6 \times t_{dDNFSCI(max)}$			ns
		filter-bypassed	75			ns
Clock input high level width	t_{KWHS}	filtered (DNF)	$3 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	35			ns
Clock input low level width	t_{KWLS}	filtered (DNF)	$3 \times t_{dDNFSCI(max)} - 5$			ns
		filter-bypassed	35			ns
Data input setup time	t_{SSIS}	filtered (DNF)	$7 + t_{dDNFSCI(min)} - t_{dDNFSI(max)}$			ns
		filter-bypassed	7.5			ns
Data input hold time	t_{HSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{KCY}$			ns
Data output delay time	t_{DSOS}	filtered (DNF)			$32.5 + t_{dDNFSCI(max)}$	ns
		filter-bypassed			32.5	
Slave select control input signal setup time	t_{SSSIS}	filtered (DNF)	$0.5 \times t_{KCYS} + t_{dDNFSCI(min)} - t_{dDNFSI(max)} - 7$			ns
		filter-bypassed	0.5 x tKCYS – 5			ns
Slave select control input signal hold time	t_{HSSIS}	filtered (DNF)	$7 + t_{KCY} + t_{dDNFSCI(max)} - t_{dDNFSI(min)}$			ns
		filter-bypassed	$7.5 + t_{CKYS} - 5$			ns
Ready / Busy output signal (CSIH0RY) output delay time	t_{DRYO}	filtered (DNF)			$32.5 + t_{KCY} + t_{dDNFSCI(max)}$	ns
		filter-bypassed			$32.5 + t_{KCY}$	ns

Timing waveforms are same as slave mode of CSIG.

1.10.4 FLSCI3

Table 1.79 FLSCI3 AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	t_{FLSCI3}				2000.0	Kbps

1.10.5 I²C Bus Interface

Condition: AWO = powered, ISO = powered
BnVDD = 3.0 to 5.5 V, RVCC=3.0 to 3.6 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.
The input timings are valid if the digital filter is bypassed.
The current I²C implementation complies with the I²C bus format (*Philips 1995 update Ver.2.1, Rev. June 5, 1996*). High speed (HS) mode is not supported.

Table 1.80 I²C AC Characteristics

Parameter	CT	Symbol	Normal Mode		Fast-speed Mode		Unit
			MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency	DS	f_{CLK}	0	100	0	400	kHz
Bus-free time (between stop/start conditions)		t_{BUF}	4.7	—	1.3	—	µs
Hold time[*1]		$t_{HD:STA}$	4.0	—	0.6	—	µs
SCLn clock low-level width		t_{LOW}	4.7	—	1.3	—	µs
SCLn clock high-level width		t_{HIGH}	4.0	—	0.6	—	µs
Setup time for start/restart conditions		$t_{SU:STA}$	4.7	—	0.6	—	µs
Data hold time CBUS compatible master		$t_{HD:DAT}$	5.0	—	-	—	µs
Data hold time I²C mode			0[*2]	3.45[*3]	0[*2]	0.9[*3]	µs
Data setup time		$t_{SU:DAT}$	250		100[*4]		ns
STOP condition setup time		$t_{SU:STO}$	4.0		0.6		µs
Noise suppression[*5]		t_{SP}				t_{IICLK}[*6]	ns
Capacitive load of each bus line		C_b		400		400	pF

Note 1. At the start condition, the first clock pulse is generated after the hold time

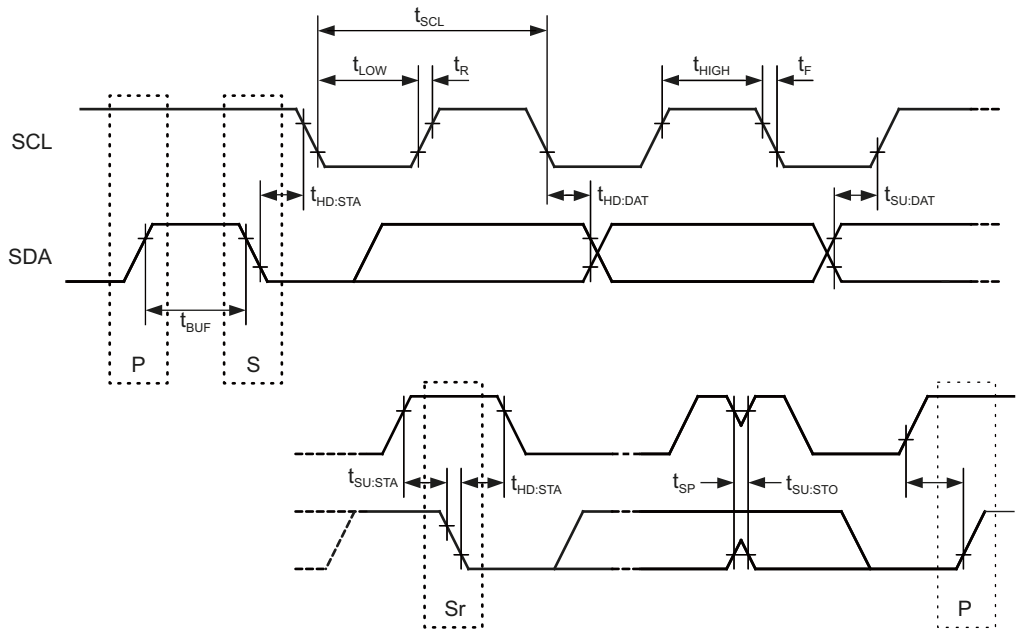
Note 2. The system requires a minimum of 300ns hold time internally for the SDA signal (at VIHmin of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

Note 3. If the system does not extend the SCL0 signal low hold time (tlow), only the maximum data hold time ($t_{HD:DAT)}$ needs to be satisfied.

Note 4. The fast-speed-mode IIC bus can be used in a normal-mode IIC bus system.
In this case, set the fast-speed-mode IIC bus so that it meets the following conditions:
- If the system does not extend the SCL0n signal's low state hold time: $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCL0n signal's low state hold time:
Transmit the following data bit to the SDA0 line prior to releasing the SCL0 line
($t_{Rmax.} + t_{SU:DAT} = 1000 + 250 = 1250$ ns: Normal mode IIC bus specification).

Note 5. Noise suppression is only available in Fast-speed mode.

Note 6. t_{IICLK} is the period of the IICLK supplied by the clock controller.



Note 1. P: Stop condition
S: Start condition
Sr: Restart condition

Note 2. Rise and Fall time depend on the actual load of the signal and the selected output current limit. For a capacitive load the time can be roughly calculated from:
(t_R = VOH / IOH × CL),
(t_F = VOH / IOL × CL)

Figure 1.65 I^2C Timing Waveform

1.10.6 SSIF (Serial Sound Interface)

Table 1.81 Audio Clock Input Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
External ACK inputs	t_{ACKI}	DNF used	100		1000	ns
		DNF not used	20		1000	ns
External ACK outputs	t_{ACKO}		41.667		531.25	ns

Table 1.82 IIS Master Mode Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK output cycle time	t_o	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SCK high width	t_{HC}		0.45 × t_o		0.55 × t_o	ns
SCK low width	t_{LC}		0.45 × t_o		0.55 × t_o	ns
SCK outputs rise time	t_{RC}				30	ns
SDO/WS outputs delay time	t_{DTR}		–5		30	ns
SDI input setup time	t_{SR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns
SDI input hold time	t_{HTR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns

Table 1.83 IIS Slave Mode Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
SCK input cycle time	t_i	DNF used	200		64000	ns
		DNF not used	80		64000	ns
SCK high width	t_{HC}		0.45 × t_i		0.55 × t_i	ns
SCK low width	t_{LC}		0.45 × t_i		0.55 × t_i	ns
SCK inputs rise time	t_{RC}				30	ns
SDO outputs delay time	t_{DTR}		–5		30	ns
SDI/WS input setup time	t_{SR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns
SDI/WS input hold time	t_{HTR}	filtered (DNF)	25 + $t_{DNFSDI(max)}$			ns
		filter-bypassed	25			ns

1.10.7 PCM-PWM Converter (PCMP)

Table 1.84 PCM-PWM Converter Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output frequency of High-speed PWM	f_{PWMOP}		10		60	kHz
Output period time	f_{PWMOP}		16.67			µs
Output time difference for each PWM outputs	t_{ANOD}, t_{BNOD}		–10.0		10.0	ns

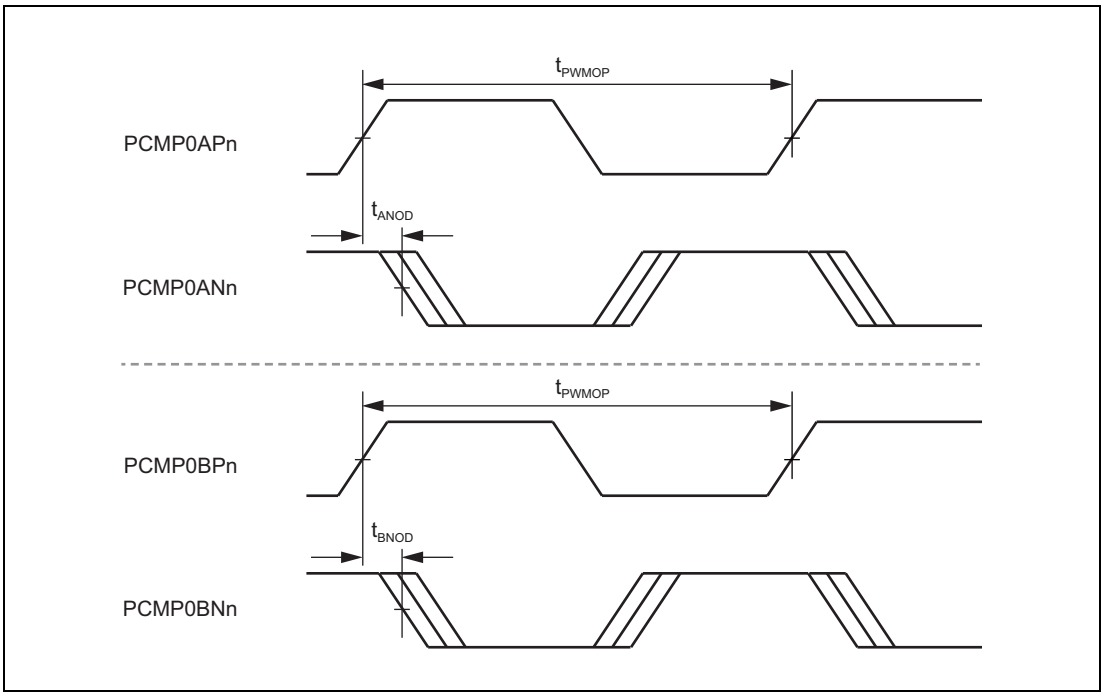


Figure 1.66 PCM-PWM Timing Waveform

1.10.8 Media Local Bus Interface (MLBB)

Table 1.85 Media Local Bus Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clk operation frequency	f_mck	256 Fs	11.264			MHz
		512 Fs			25.6	MHz
		1024 Fs	45.056		51.2	MHz
MLBCLK rise/fall time	f_mckfr	256/512 Fs			3.0	ns
		1024 Fs			1.0	ns
MLBCLK high/low time	f_mckhl	256 Fs	30.0			ns
		512 Fs	14.0			ns
		1024 Fs	6.1			ns
MLBSIG/MLBDAT input setup time to MLBCLK falling	t_dsmcf		1.0			ns
MLBSIG/MLBDAT input hold time from MLBCLK low	t_dhmcf		2.0			ns
MLBSIG/MLBDATA output delay time from MLBCLK rising	t_delay		0.0		8.0	ns
MLBSIG/MLBDATA output Hi-Z time from MLBCLK low	t_mcfdz		0.0		8.0	ns

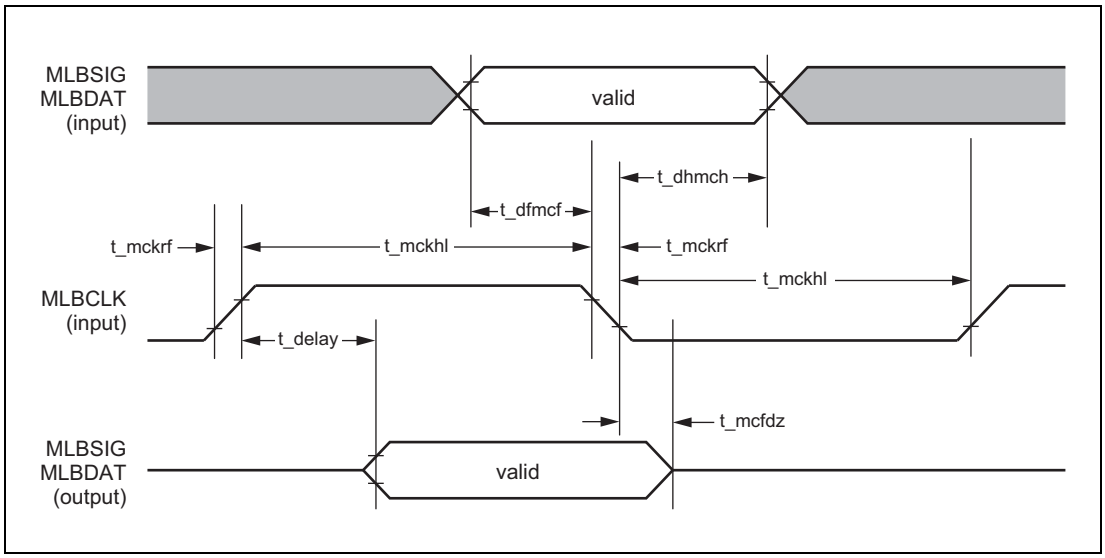


Figure 1.67 Media Local Bus Timing Waveform

1.10.9 Ethernet Media Independent Interface (ETNB)

Table 1.86 Media Local Bus Interface Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RX_CLK/TX_CLK frequency	mickf	100 Mbps		25.0		MHz
		10 Mbps		2.5		MHz
Input data setup	miids		10.0			ns
Input data hold	miidh		10.0			ns
Output data delay	miod		0.0		25.0	ns

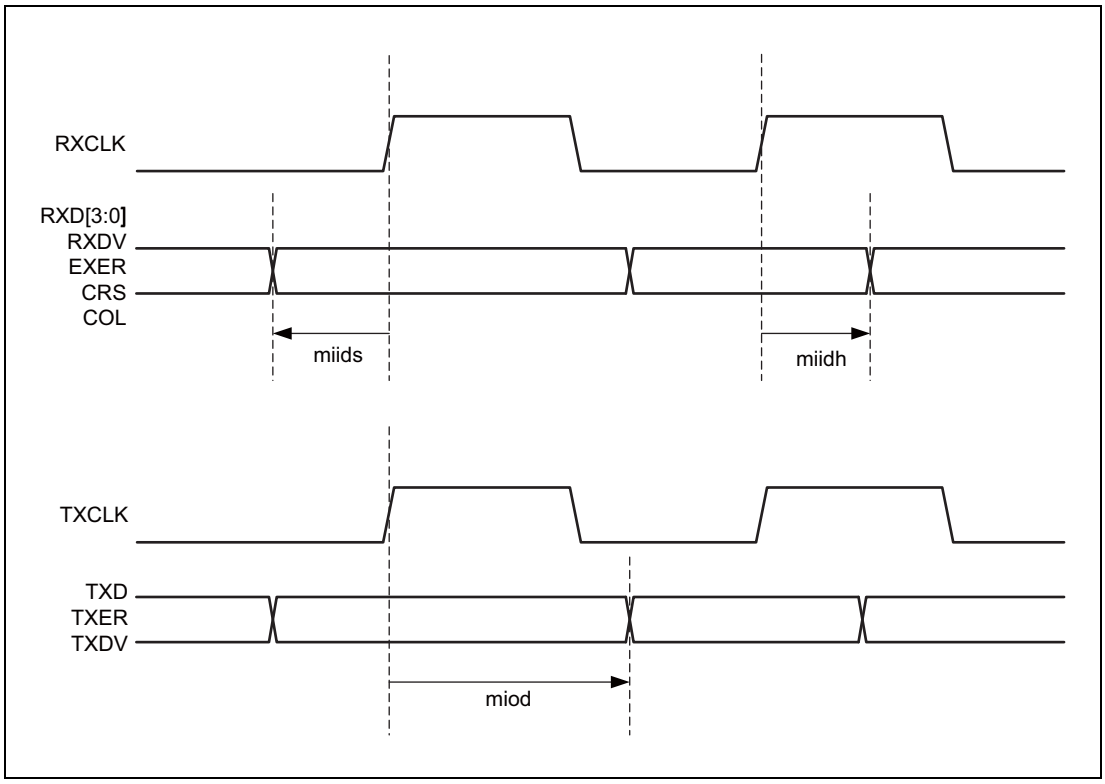


Figure 1.68 Ethernet Media Independent Interface Timing Waveform

1.10.10 RS-CAN Interface

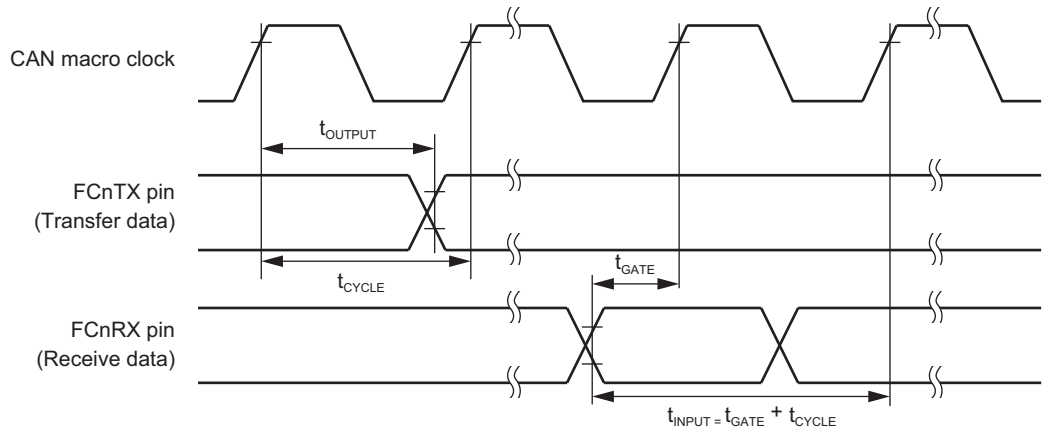
Condition: AWO = powered, ISO = powered
EVDD = 3.0 to 5.5 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition**.
The input timings are valid if the digital filter is bypassed.

Table 1.87 CAN AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	DS	t_{FCNn}	Regular CAN			1000	Kbps
Internal delay time		t_{INTDEL}	Regular CAN			37.5	ns
CAN Node Delay time		t_{NODE}	t_{CYCLE} = 62.5 ns, regular CAN			100	ns

NOTE

The CAN module of this device is conform to ISO 11898-1. Additionally it is tested according to CAN Conformance Specification (i.e. ISO16845).



Note: CAN node delay time (t_{NODE})
= INPUT delay time (t_{INPUT}) + Output delay time (t_{OUTPUT})
Internal delay time (t_{INTDEL})
= Internal gate delay time (t_{GATE}) + Output delay time (t_{OUTPUT})

Figure 1.69 CAN Interface Waveform

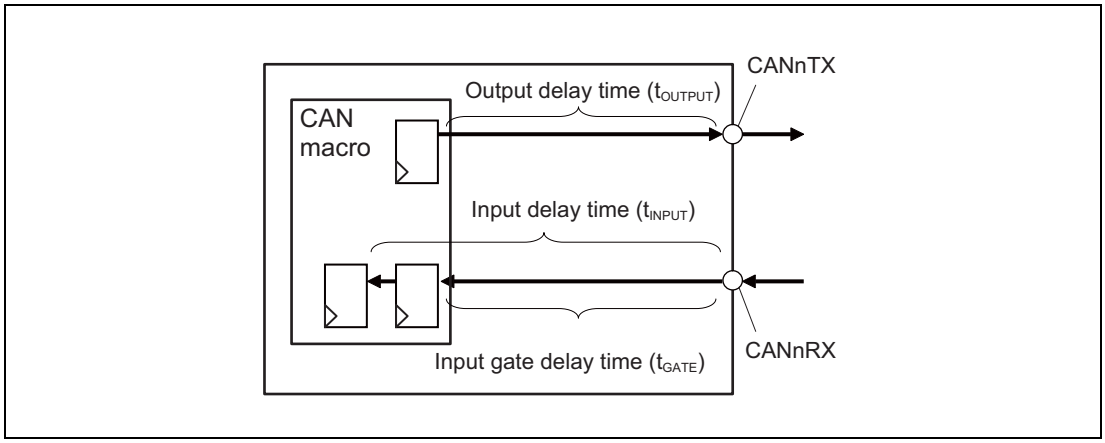


Figure 1.70 CAN Delay Time Definition

1.10.11 CAN-FD Interface

Table 1.88 CAN-FD AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate	DS	t_{FCNn}			8000	Kbps
CAN-FD Node Delay time		t_{NODE}			50	ns

Note: CAN node delay time (t_{NODE})
= INPUT delay time (t_{INPUT}) + Output delay time (t_{OUTPUT})

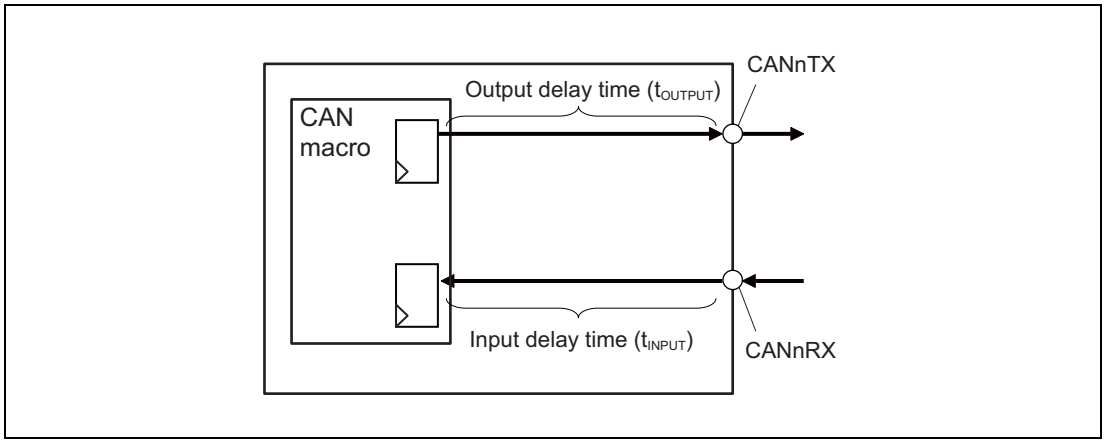


Figure 1.71 CAN-FD Delay Time Definition

1.10.12 Debug Connection

1.10.12.1 NEXUS Interface

Table 1.89 NEXUS Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK Cycle width	TDCKW		50.0			ns
DCUTDI setup time (vs DCUTCK rise edge)	TSDI		40.0			ns
DCUTDI hold time (vs DCUTCK rise edge)	THDI		3.0			ns
DCUTMS setup time (vs DCUTCK rise edge)	TSMS		40.0			ns
DCUTMS hold time (vs DCUTCK rise edge)	THMS		3.0			ns
DCUTDO Delay time (vs DCUTCK fall edge)	TDDO		0.0		23.0	ns
$\overline{\text{DCURDY}}$ Delay time (vs DCUTCK fall edge)	TRDYZ		0.0		23.0	ns

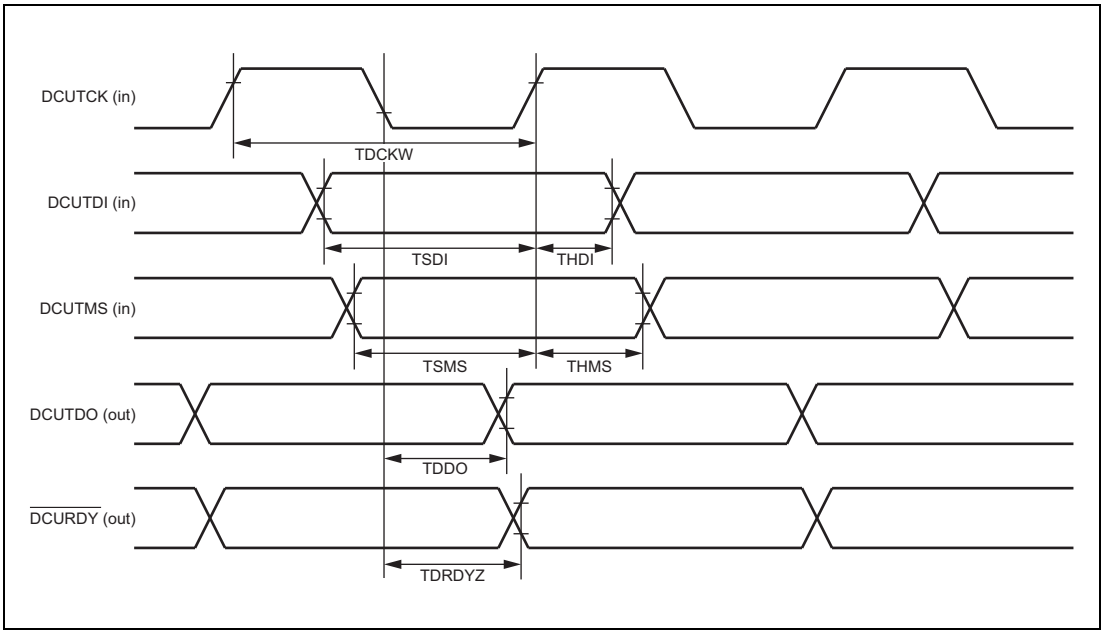


Figure 1.72 NEXUS Interface Wave Form

1.10.12.2 LPD 4pin Interface

Table 1.90 LPD 4pin Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time	t_{LPDCKW}		30			ns
LPDCLK high/low width	$t_{LPDCKWH}$/ $t_{LPDCKWL}$		$t_{LPDCKW/2}$ × 0.9		$t_{LPDCKW/2}$	ns
LPDIO setup time (to LPDCLK rise)	t_{LPDSU}		t_{LPDCKW} − 19			ns
LPDIO hold time (to LPDCLK rise)	t_{LPDH}		11.0			ns
LPDCLKO cycle time	$t_{LPDCKOW}$		t_{LPCKW}		t_{LPCKW}	ns
LPDCLKO high/low width	$t_{LPDCKOWH}$/ $t_{LPDCKOWL}$		$t_{LPDCKWH}$		$t_{LPDCKWH}$	ns
LPDCLKO rise/fall time	$t_{LPDCKOr}$/ $t_{LPDCKOf}$	EVCC = 3.0 to 3.6 V			10.0	ns
		EVCC = 4.5 to 5.5 V			5.0	ns
LPDO output delay (to LPDCLKO rise)	t_{LPDOD}		0		$t_{LPDCKW/2}$ − 3	ns

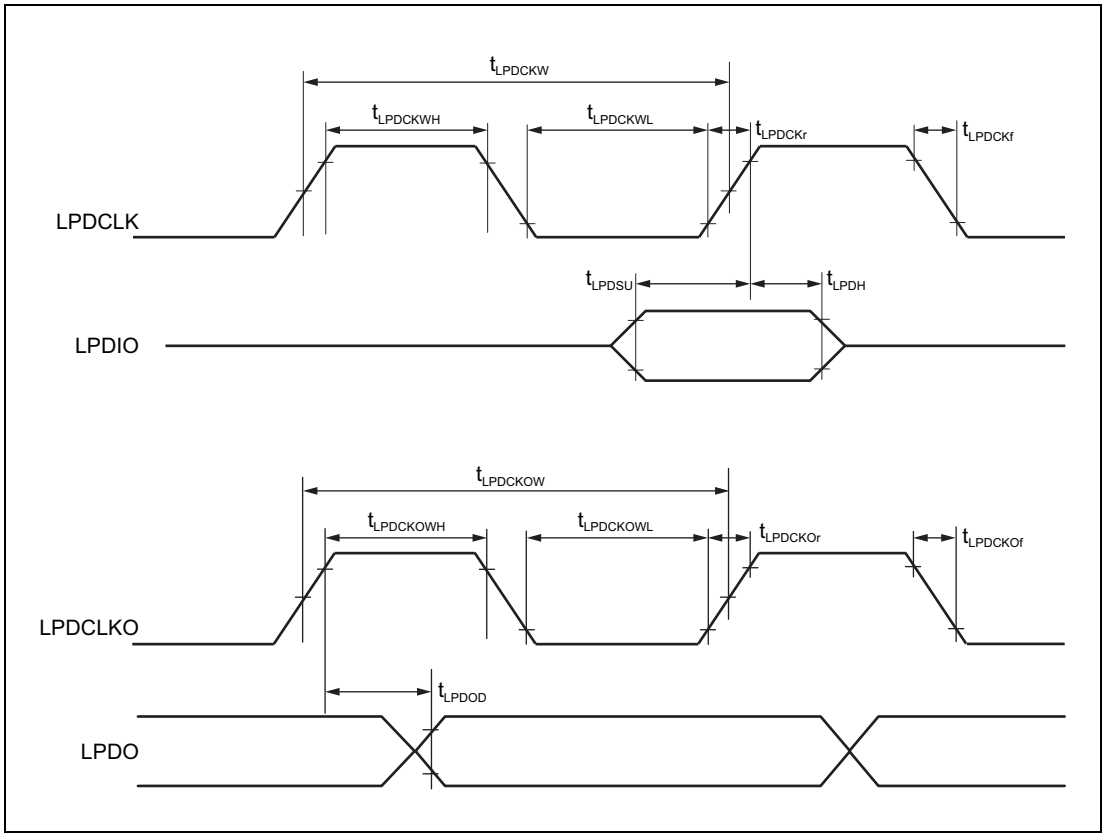


Figure 1.73 LPD 4pin Interface Wave Form

1.10.12.3 LPD 1pin Interface

Table 1.91 LPD 1pin Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD Baud rate					2	Mbps

1.10.12.4 Trace Interface

Table 1.92 Trace Interface

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MCKO cycle time	t_{MCKW}		8.3			ns
MCKO high / low level width	t_{MCKWH}/ t_{MCKWL}		$t_{MCKW/2}$ – 1.3			ns
MDO output delay	t_{MDOD}		0.2		3.5	ns
$\overline{MSEO0}$ / $\overline{MSEO1}$ output delay	t_{MSED}		0.2		3.5	ns
$\overline{EVTO}$ output delay	t_{EVTOD}		0.2		4.0	ns
$\overline{EVTI}$ low level width	t_{EVTI}		2 × t_{MCKW}			ns
$\overline{MSYNC}$ low level width	t_{MSYNC}		2 × t_{MCKW}			ns
Rising / Falling time	t_{OR}/t_{OF}				1.3	ns

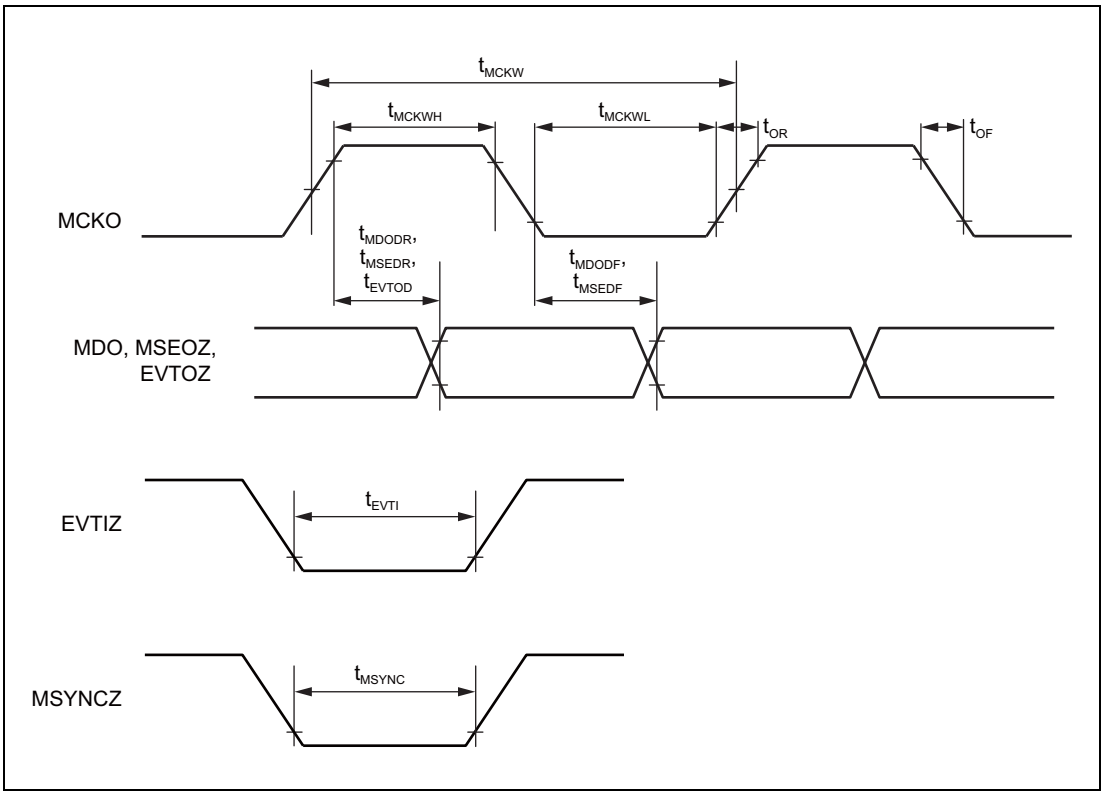


Figure 1.74 Trace Interface Wave Form

1.11 Memory Interface Operating Conditions

1.11.1 Serial Flash Memory Interface (SFMA)

Table 1.93 SFMA AC Characteristics (D1M2(H)/D1M1(H)/D1M1A/D1M1-V2/D1L2(H))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK frequency	f_{CK}				DDR mode: 80 SDR mode:120	MHz
CLK cycle	t_{CK}		DDR mode: 12.5 SDR mode: 8.3			ns
CLK high width	t_{CKH}		0.45		0.55	t_{CK}
CLK low width	t_{CKL}		0.45		0.55	t_{CK}
Chip select signal output setup*2	t_{CSS}		–1.0		7.0	ns
		for P45_1 of D1M1A	–1.0		14.0	ns
Data input setup time*1,*2	t_{DIS}		2.0			ns
		SFVCC = 3.2 to 3.4 V, only D1M2(H)	1.9			ns
Data input hold time*1,*2	t_{DIH}		1.5			ns
Data output valid time*2	t_{DOV}		2.3		4.75@CL = 15 pF 4.4@CL = 10 pF	ns
Clock to output low impedance	t_{LZ}		0.0		8.0	ns
Phase shift control step	t_{PSS}		t_{PHCYC}*3 – 0.1		t_{PHCYC}*3 + 0.1	ns
t_{DIS} delay range whole temperature*4	t_{DIS_T}		–600		600	ps
t_{DIH} delay range whole temperature*4	t_{DIH_T}		–600		600	ps
Data input setup/hold window for 1 device at one temperature	$t_{\Delta DISH}$				150.0	ps

Note 1. $CKDLY_{RX} = 000_B$, if $CKDLY_{RX}$ change to other value, it calculate by following formula.
- $t_{DIS} = 2.0 – (CKDLY_{RX} \times t_{PHCYC} + 0.1)$
- $t_{DIH} = 1.5 + CKDLY_{RX} \times t_{PHCYC} + 0.1$
  - i.e) $CKDLY_{RX} = 010_B$, $t_{PHCYC} = 1.04$ ns: $t_{DIS} = –0.18$ ns, $t_{DIH} = 3.68$ ns

Note 2. $f_{PHCLK}/f_{B\varphi} = 2$: $CKDLY_{OC} = 010_B$, $f_{PHCLK}/f_{B\varphi} = 3$: $CKDLY_{OC} = 011_B$, $f_{PHCLK}/f_{B\varphi} = 4$: $CKDLY_{OC} = 101_B$

Note 3. t_{PHCYC} is cycle time of phase shift clock (f_{PHCLK})

Note 4. t_{DIS_T} and t_{DIH_T} show the deviation of delay spec from room temperature (25°C).
- i.e) $CKDLY_{RX} = 000_B$
  - $t_{DIS(max)} = 2.0$ ns: $t_{DIS(min)} = 0.8$ ns

Table 1.94 SFMA AC Characteristics for P42 pin group (D1M1A/D1M1-V2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK frequency	f_{CK}	w/ –6% down-spread			DDR mode: 40 SDR mode: 40	MHz
CLK cycle	t_{CK}	w/ –6% down-spread	DDR mode: 25 SDR mode: 25			ns
CLK high width	t_{CKH}		0.45		0.55	t_{CK}
CLK low width	t_{CKL}		0.45		0.55	t_{CK}
Chip select signal output setup*2	t_{CSS}		–1.0		9.0	ns
Data input setup time*1,*2	t_{DIS}		6.0			ns
Data input hold time*1,*2	t_{DIH}		1.0			ns
Data output valid time*2	t_{DOV}		3.0		8.0	ns
Clock to output low impedance	t_{LZ}		0.0		8.0	ns
Phase shift control step	t_{PSS}		t_{PHCYC}*3 × 1 – 0.3		t_{PHCYC}*3 × 1 + 0.3	ns

Note 1. $CKDLY_{RX} = 000_B$
Note 2. $CKDLY_{TS} = 01_B$
Note 3. tP_{HCYC} is cycle time of phase shift clock (f_{PHCLK})

Table 1.95 SFMA AC Characteristics (D1L1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK frequency	f_{CK}				SDR: 40	MHz
CLK cycle	t_{CK}		SDR: 25			ns
CLK high width	t_{CKH}		0.45		0.55	t_{CK}
CLK low width	t_{CKL}		0.45		0.55	t_{CK}
Chip select signal output setup	t_{CSS}		0.0		18	ns
Data input setup time	t_{DIS}		9.0			ns
Data input hold time	t_{DIH}		1.0			ns
Data output valid time	t_{DOV}		2.0		10.0	ns
Output disable timing	t_{ODS}		0.0		8.0	ns

Note: t_{DOV} spec specify by DLYOn = 1.

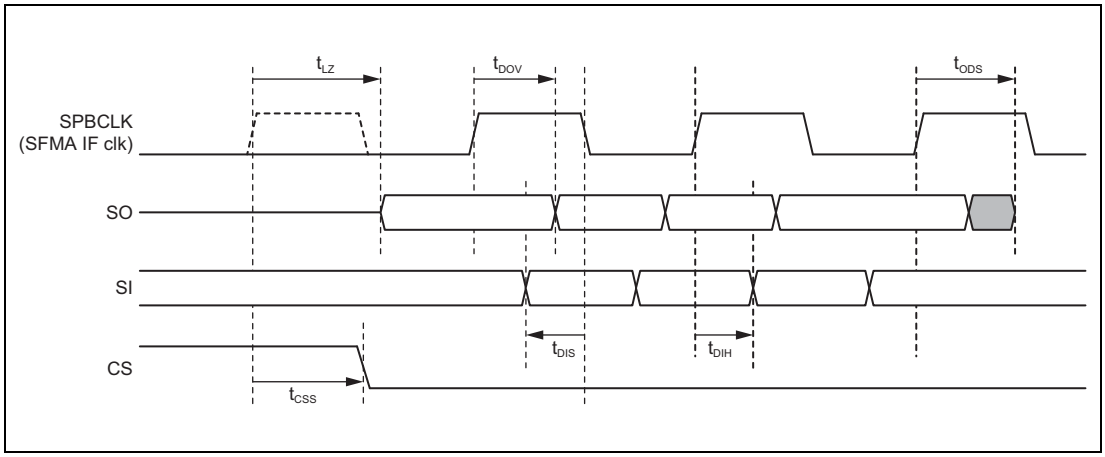


Figure 1.75 SFMA Wave Form

1.11.2 HyperBus/OctaBus Interface

Table 1.96 HYPB/OCTA AC Characteristics (D1M1A/D1M1-V2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK frequency	f_{CK}	w/ –6% down-spread			80	MHz
CLK cycle	t_{CK}	w/ –6% down-spread	12.5			ns
CLK high width	t_{CKH}		0.45		0.55	t_{CK}
CLK low width	t_{CKL}		0.45		0.55	t_{CK}
Chip select signal output setup	t_{CSS}		–1.0		7.0	ns
Data input setup time	t_{DIS}		–1.5		1.5	ns
Data input hold time	t_{DIH}		–1.5		1.5	ns
Data output valid time	t_{DOV}		$t_{CK/4 - 1.2}$		$t_{CK/4 + 1.2}$	ns
Clock to output low impedance (DQ/DQS)	t_{LZ}		–1.0		5.0	ns
DQS flight time	t_{CKDS}		1.0		8.0	ns

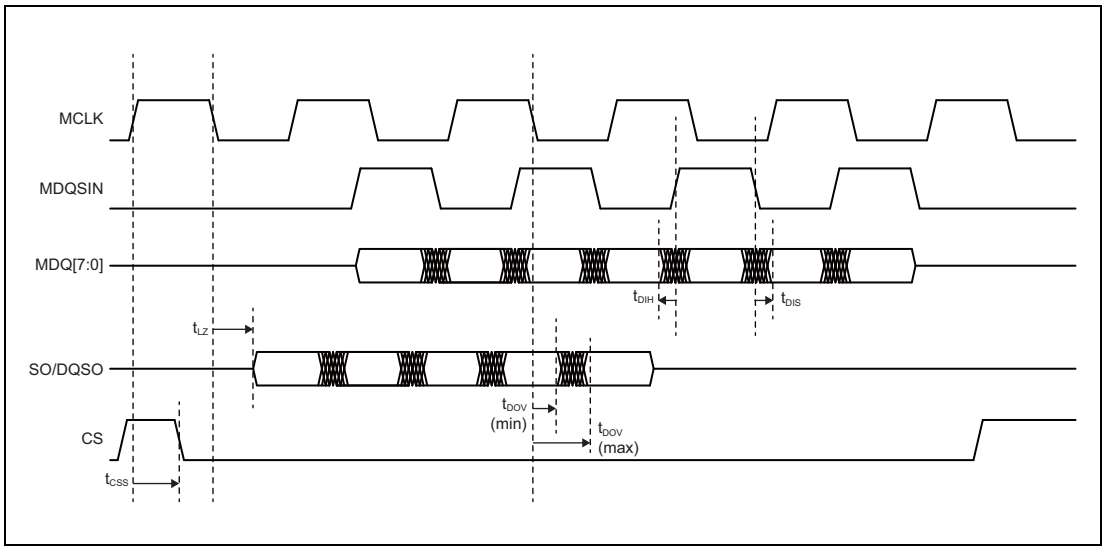


Figure 1.76 HYPB/OCTA Waveforms

1.11.3 DDR2-SDRAM Interface

Table 1.97 DDR2-SDRAM AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MCK cycle period	t_{CK} (avg)		4.167		4.167	ns
MCK high cycle width	t_{CH} (abs)		0.43		0.57	t_{CK}
MCK low cycle width	t_{CL} (abs)		0.43		0.57	t_{CK}
Address/Command setup time	t_{IS}		890			ps
Address/Command hold time	t_{IH}		950			ps
Pulse width of Address/Command signals	t_{IPW}		0.65			t_{CK}
Write latency	W_L		C_L–1			t_{CK}
1st DQS rising edge from Write command (write)	t_{WDQSS}		–0.20		0.20	t_{CK}
MDQS negedge setup time from MCK (write)	t_{WDSS}		0.25			t_{CK}
MDQS posedge setup time from MCK (write)	t_{WDSH}		0.25			t_{CK}
high pulse width of MDQS (write)	t_{WDQSH}		0.35		0.65	t_{CK}
low pulse width of MDQS (write)	t_{WDQSL}		0.35		0.65	t_{CK}
MDQS preamble width (write)	t_{WPRE}		0.35			t_{CK}
MDQS postamble width (write)	t_{WPST}		0.40			t_{CK}
MDQ/MDM setup time from MDQS (write)	t_{WDS}		460			ps
MDQ/MDM hold time from MDQS (write)	t_{WDH}		460			ps
MDQ/MDM pulse width (write)	t_{WDIPW}		0.37			t_{CK}
Read latency	R_L		C_L			t_{CK}
MDQS skew from MCK (read)	t_{RDQSCK}		–530		1430	ps
MDQS high pulse width (read)	t_{RQSH}		0.35		0.65	t_{CK}
MDQS low pulse width (read)	t_{RQSL}		0.35		0.65	t_{CK}
MDQS preamble width (read)	t_{RPRE}		0.90			t_{CK}
MDQS postamble width (read)	t_{RPST}		0.40			t_{CK}
MDQ skew from MDQS (read)	t_{RDQSQ}				410	ps
MDQ hold time from MDQS (read)	t_{RQH}		0.38			t_{CK}

Note: CL: CAS Latency

1.11.4 SDR-SDRAM Interface

Table 1.98 SDR-SDRAM AC Characteristics (D1M1H)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK cycle	t_{CK}		9.4			ns
CLK high/low level width	t_{CH} / t_{CL}		0.40		0.60	t_{CK}
Command/Address output delay	t_{Ad}		1.0		7.0	ns
Data-out high-Z time	t_{HZ}				7.0	ns
Data-out low-Z time	t_{LZ}		1.0			ns
Write data output delay	t_{WDO}		2.0		7.0	ns
Read data input setup time	t_{RDIS}		3.0			ns
Read data input hold time	t_{RDIH}		2.0			ns
Round Trip Time of read data	t_{RTT}		0.5		1.4	ns

Table 1.99 SDR-SDRAM AC Characteristics (D1M1A)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CLK cycle	t_{CK}		8.333			ns
CLK high/low level width	t_{CH} / t_{CL}		0.40		0.60	t_{CK}
Command/Address output delay	t_{Ad}		0.8		6.5	ns
Data-out high-Z time	t_{HZ}				6.5	ns
Data-out low-Z time	t_{LZ}		0.8			ns
Write data output delay	t_{WDO}		0.8		6.3	ns
Read data input setup time	t_{RDIS}		1.5			ns
Read data input hold time	t_{RDIH}		2.5			ns
Round Trip Time of read data	t_{RTT}		0.5		1.4	ns

1.11.5 NAND Flash Interface

Table 1.100 NANDC AC Characteristics (D1M1A)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Minimum command cycle	t_{CYC}				50	ns
Output signals delay	t_{OD}		0		3	ns
Rise-fall delay data of each output signals	t_{RFD}		0		3	ns
Read data setup time from NAND_RE# rise	t_{SD}		15.0			ns
Read data hold time from NAND_RE#rise	t_{HD}		10.0			ns

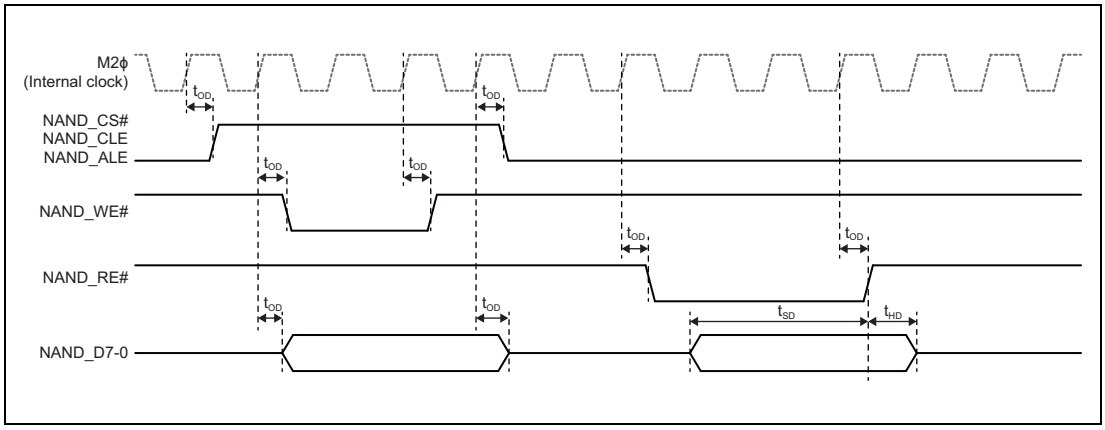


Figure 1.77 NANDC Waveforms

1.12 Graphic Module Operating Conditions

1.12.1 Video Interface Timing

1.12.1.1 Video Output Timing

Condition: AWO = powered, ISO = powered
BnVCC = 3.0 to 3.6 V, RVCC = 3.0 to 3.6 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition** with load condition of 30 pF.

Table 1.101 Video Output AC Characteristics - LVTTL Mode (D1M2(H), D1M1(H), D1M1-V2)

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Pixel clock frequency (DCLK)	DS	f_{DCLK}	48 MHz for D1M2(H) (max. DCLK frequency)*1			52	MHz
			30 MHz for D1M1(H) (max. DCLK frequency)*1			32	MHz
			For D1M1-V2 (serial RGB) (max. DCLK frequency)			40	MHz
Pixel clock period		t_{DCLK}	$1/f_{DCLK}$				ns
Pixel clock duty cycle		$DCLK_{duty}$		40.0	50.0	60.0	%
Output data valid time		t_{OV}				4.0	ns
Output data hold time		t_{OH}		–2.0			ns
SYNP signal output valid time		t_{SOV}				4.0	ns
SYNP signal output hold time		t_{SOH}		–2.0			ns

Note 1. VO0EXCLKI: Clock source for DCLK can also be input from external via pin. MAX. value include SSCG (±5%) margin.

Table 1.102 Video Output AC Characteristics (D1L2)

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Pixel clock frequency (DCLK)	DS	f_{DCLK}	10 MHz (max. DCLK frequency)*1			10	MHz
Pixel clock period		t_{DCLK}		$1/f_{DCLK}$			ns
Pixel clock duty cycle		$DCLK_{duty}$		40	50	60	%
Output data valid time		t_{OV}				15	ns
Output data hold time		t_{OH}		0			ns
SYNP signal output valid time		t_{SOV}				15	ns
SYNP signal output hold time		t_{SOH}		0			ns

Note 1. VO0EXCLKI: Clock source for DCLK can also be input from external via pin.

Table 1.103 Video Output AC Characteristics - LVTTL Mode (D1M1A)

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Pixel clock frequency (DCLK)	DS	f_{DCLK}	LVTTL, Serial RGB			48	MHz
			VO-DDR			30	MHz
Pixel clock period		t_{DCLK}		$1/f_{DCLK}$			ns
Pixel clock duty cycle		$DCLK_{duty}$		40.0	50.0	60.0	%
Output data valid time		t_{OV}				2.0	ns
Output data hold time		t_{OH}		–2.0			ns
SYNP signal output valid time		t_{SOV}				2.0	ns
SYNP signal output hold time		t_{SOH}		–2.0			ns

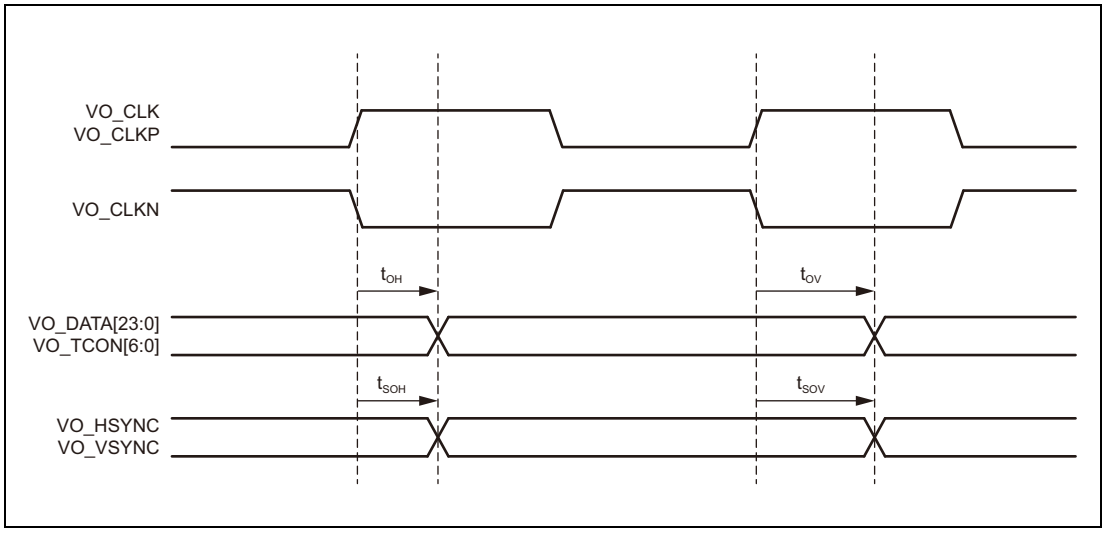


Figure 1.78 Video Output AC Characteristics - LVTTL Mode

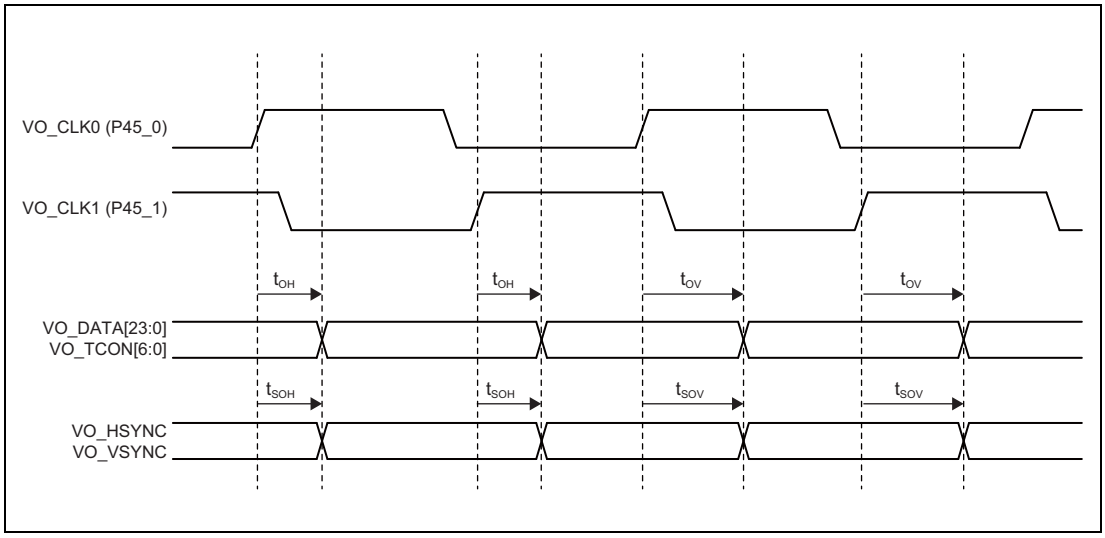


Figure 1.79 Video Output AC Characteristics - VO-DDR

1.12.1.2 Video Output Interface (RSDS)

Table 1.104 RSDS Interface AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output clock frequency	t_{CK}				50	MHz
Output clock cycle	t_{CYC}		20			ns
Output clock high-width/low-width	RCHP/RCLP		7.5			ns
Output data setup time to edge of RSCK	RSTU		4.3 + PHS × t_{CYC}/4			ns
Output data hold time to edge of RSCK	RHLD		0.2 – PHS × t_{CYC}/4			ns
Output Sync setup time	SPSTU			0.5		t_cyc
Output Sync hold time	SPHLD			0.5		t_cyc

Note: PHS = RPHSL[1:0] of RSDSCFG register

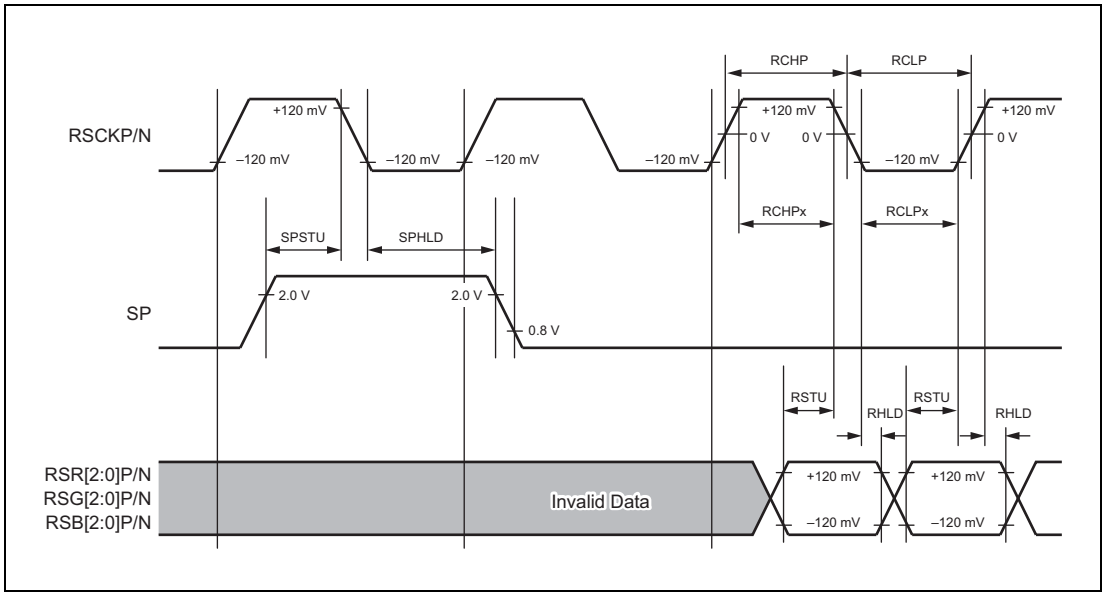


Figure 1.80 RSDS Timing Figure

1.12.1.3 Video Output Interface (OpenLDI)

Table 1.105 OpenLDI Interface AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Output clock frequency	t_{CK}				34.29	MHz
Output data cycle	t_{CYC}		29.17			ns
Output clock high-width/low-width	RCHP/RCLP		$t_{CYC} \times 0.4$		$t_{CYC} \times 0.6$	ns
Output data position0	t_{RIP0}		$-t_{SKM}$	0	t_{SKM}	ns
Output data position1	t_{RIP1}		$t_{CYC/7} - t_{SKM}$	$t_{CYC/7}$	$t_{CYC/7} + t_{SKM}$	ns
Output data position2	t_{RIP2}		$2 \times t_{CYC/7} - t_{SKM}$	$2 \times t_{CYC/7}$	$2 \times t_{CYC/7} + t_{SKM}$	ns
Output data position3	t_{RIP3}		$3 \times t_{CYC/7} - t_{SKM}$	$3 \times t_{CYC/7}$	$3 \times t_{CYC/7} + t_{SKM}$	ns
Output data position4	t_{RIP4}		$4 \times t_{CYC/7} - t_{SKM}$	$4 \times t_{CYC/7}$	$4 \times t_{CYC/7} + t_{SKM}$	ns
Output data position5	t_{RIP5}		$5 \times t_{CYC/7} - t_{SKM}$	$5 \times t_{CYC/7}$	$5 \times t_{CYC/7} + t_{SKM}$	ns
Output data position6	t_{RIP6}		$6 \times t_{CYC/7} - t_{SKM}$	$6 \times t_{CYC/7}$	$6 \times t_{CYC/7} + t_{SKM}$	ns
Output data skew margin	t_{SKM}		—	—	0.5	ns

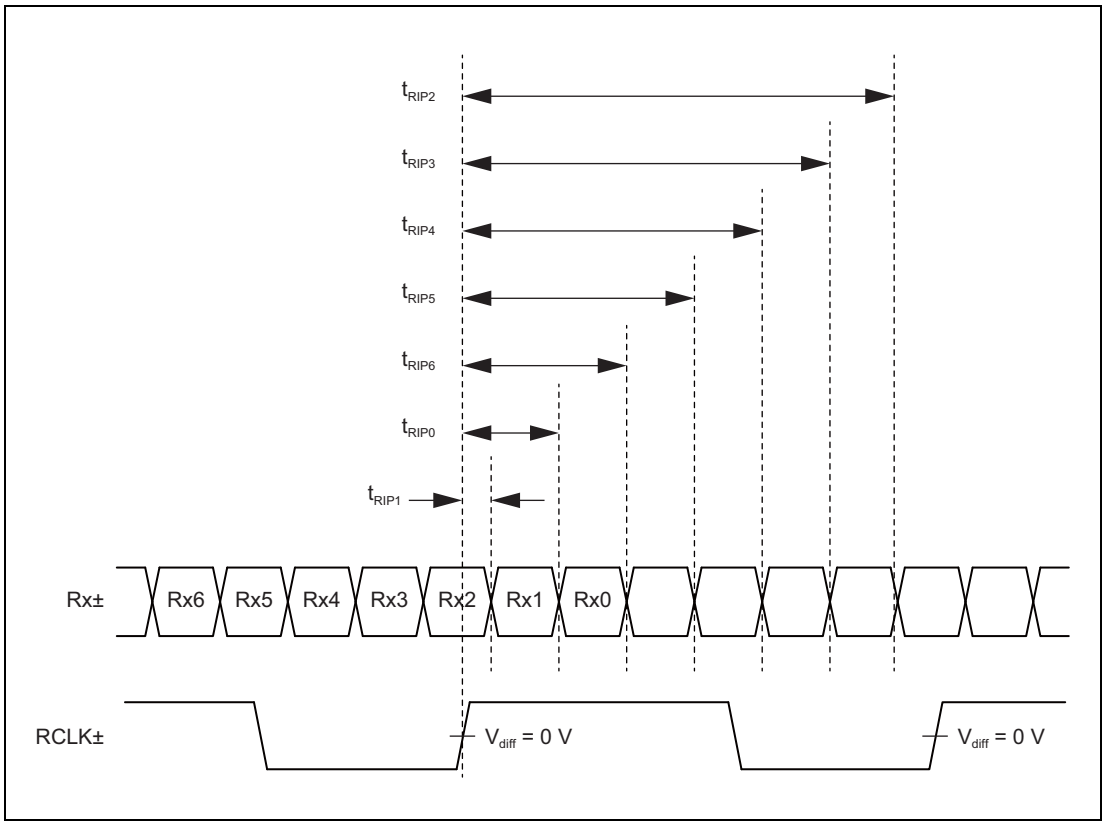


Figure 1.81 OpenLDI Interface AC Characteristics

1.12.1.4 Video Input Timing

Condition: AWO = powered, ISO = powered
BnVCC = 2.7 to 3.6 V, RVCC = 2.7 to 3.6 V
Measurement according to **Section 1.3.1, AC Characteristic Measurement Condition** with load condition of 30 pF.

Table 1.106 Video Input AC Characteristics

Parameter	CT	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input clock period	DS	t_{CKI}	D1M2(H)	20			ns
			D1M1(H), D1M1A, D1M1-V2	33.3			ns
Input clock duty ratio		CKI_{duty}	$(t_{CKIH} + t_{CKIF})/ t_{CKI}$ or $(t_{CKIL} + t_{CKIR})/ t_{CKI}$	40	50	60	%
Input clock rise time		t_{CKIR}				5	ns
Input clock fall time		t_{CKIF}				5	ns
VI_DATA[23:0], VI_HSYNC, VI_VSYNC setup time		t_{VIS}		3.1			ns
VI_DATA[23:0], VI_HSYNC, VI_VSYNC hold time		t_{VIH}		1			ns

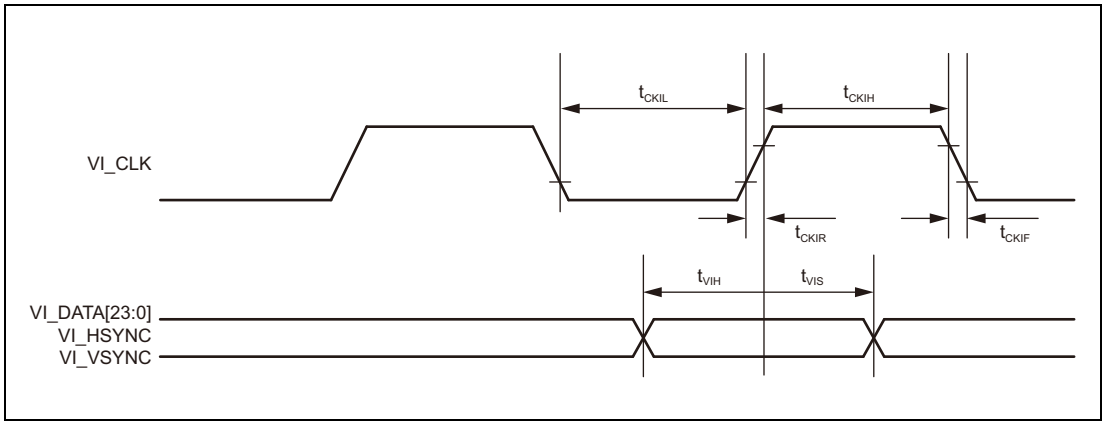


Figure 1.82 Video Input AC Characteristics

1.12.1.5 Video Input Interface (MIPI-CSI2)

Table 1.107 MIPI-CSI 2 Interface AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input clock frequency	t_{CK}				240	MHz
Input clock cycle	t_{CYC}		4.167			ns
Input data setup time to edge of t_{CK}	Tsu		0.2			t_{CYC}
Input data hold time to edge of t_{CK}	Thld		0.2			t_{CYC}

1.12.1.6 LCD Bus Interface (LCBI)

Table 1.108 RAM Operation Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time (transfer period)	t_{CYCr}*1	slow mode	CYC_{slow} × T – 5			ns
		fast mode	CYC_{fast} × T – 5			ns
Address setup time (WRITE mode: A0 falling to CSZ&WRZ falling) (READ mode: A0 falling to CSZ&RDZ falling)	t_{ASr}	slow mode	(TIAD + TIDW + 2) × T			ns
		fast mode	0			ns
Address hold time (WRITE mode: WRZ rising to A0&CSZ rising) (READ mode: RDZ rising to A0&CSZ rising)	t_{AHr}	slow mode	(TIDZ + 1) × T – 10			ns
		fast mode				
WRITE strobe LOW pulse width	t_{WRZLr}	slow mode	(TIWR + 1) × T – 10			ns
		fast mode				
WRITE strobe HIGH pulse width	t_{WRZHr}	slow mode	(TIAD + TIDW + TIDZ + 3) × T – 10			ns
		fast mode	(TIDZ + 1) × T – 10			ns
READ strobe LOW pulse width	t_{RDZLr}	slow mode	((TIRD + 1) × T – 10			ns
		fast mode				
READ strobe HIGH pulse width	t_{RDZHr}	slow mode	(TIAD + TIDW + TIDZ + 3) × T – 10			ns
		fast mode	(TIDZ + 1) × T – 10			ns
Data output setup time (WRITE mode) D[17:0] to CSZ&WRZ falling	t_{DOSr}	slow mode			(TIDW + 1) × T	ns
		fast mode			0	ns
Data output hold time (WRITE mode) WRZ rising to D[17:0]	t_{DOHr}	slow mode	(TIDZ + 1) × T – 10			ns
		fast mode				
Data input setup time (READ mode) D[17:0] to CSZ&RDZ rising	t_{DISr}	slow mode	50.0			ns
		fast mode				
Data input hold time (READ mode) D[1:0] from CSZ&RDZ rising	t_{DIHr}	slow mode	1 × T			ns
		fast mode	1 × T			
Output disable Time (WRITE mode to READ mode) D[17:0] Hi-Z to RDZ falling	t_{ODr}	slow mode	(TIAD + TIDW + 2) × T			ns
		fast mode	0.0			ns

Note 1. The parameters CYCslow respectively CYCfast, as well as the parameter T are set as described in *the UM Section 36.3.1.2, Transfer Speed*.
Where the transfer period CYCr (depending on slow or fast mode named CYCslow or CYCfast) corresponds to the settings of the LCBInBCYC register.
Likewise the time for one step of a transfer period T corresponds to the settings of the LCBInCKSEL register, means the PCLK divider setting.

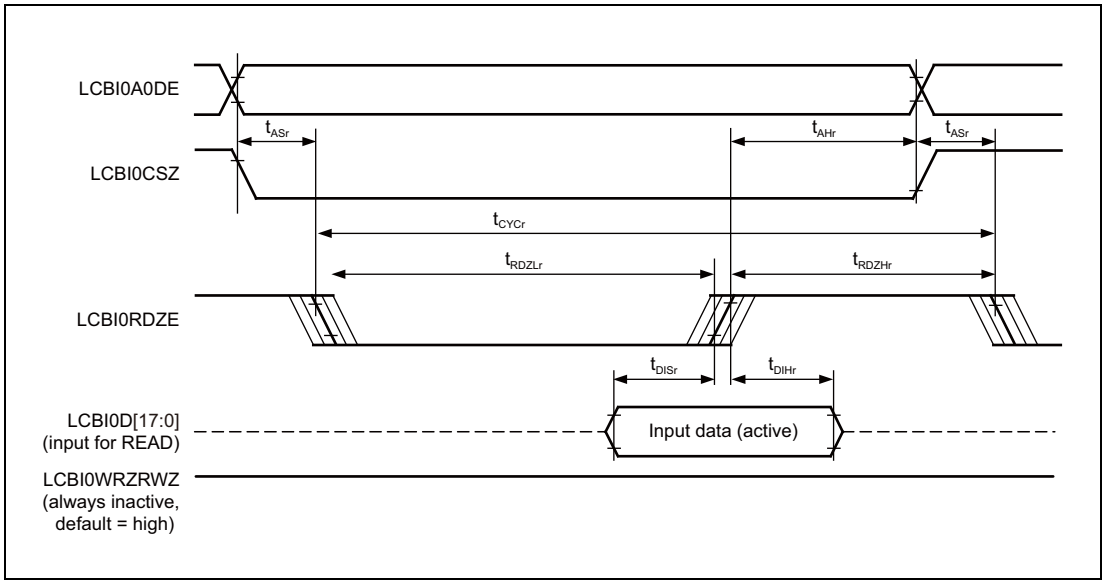


Figure 1.83 LCD Bus Interface RAM Operation Mode (READ)

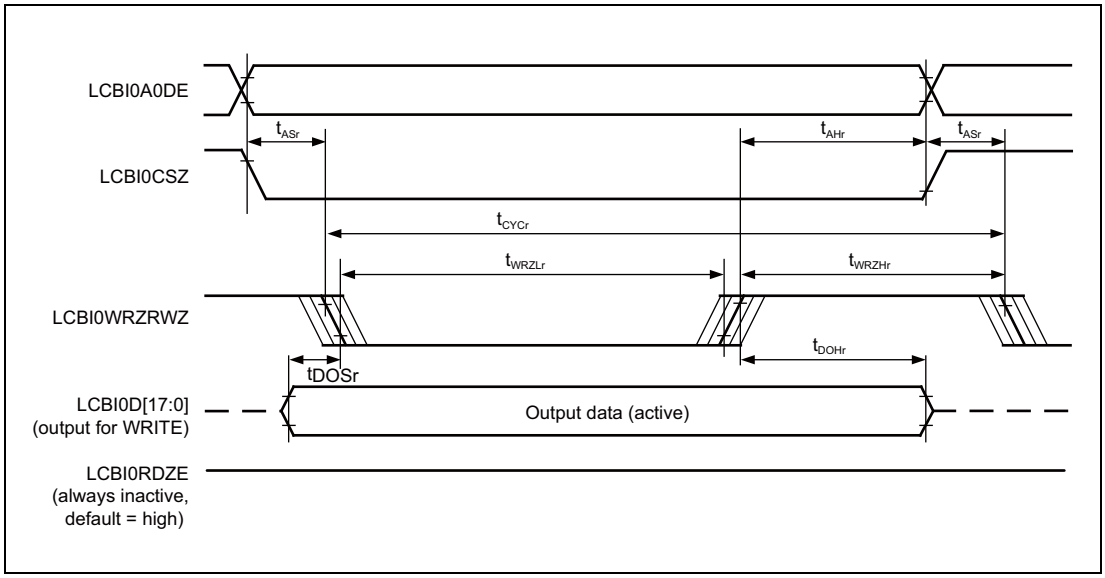


Figure 1.84 LCD Bus Interface RAM Operation Mode (WRITE)

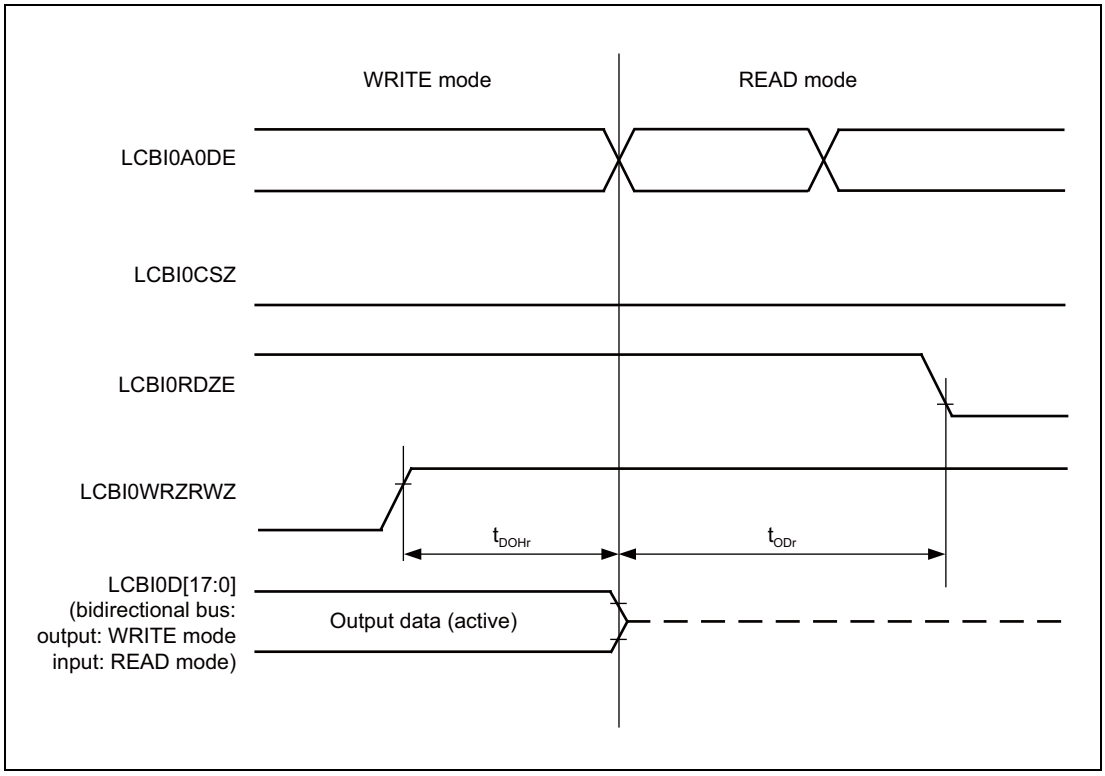


Figure 1.85 LCD Bus Interface RAM Operation Mode (WRITE/READ switch)

Table 1.109 E-type Operation Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Cycle time (transfer period)	t_{CYCe}	slow mode	CYC_{slow} × T – 5			ns
		fast mode	CYC_{fast} × T – 5			ns
Address setup time (A0 falling to CSZ&E falling)	t_{ASe}	slow mode	(TMAD + TMDW + 2) × T			ns
		fast mode	0			ns
Address hold time (WRZ rising to A0&CSZ rising)	t_{AHe}	slow mode	(TMDZ + 1) × T – 10			ns
		fast mode				
Enable control signal LOW pulse width	t_{ENRLe}/ t_{ENWLe}	slow mode	(TMED + 1) × T – 10			ns
		fast mode				
Enable control signal HIGH pulse width	t_{ENRHe}/ t_{ENWHe}	slow mode	(TMAD + TMDW + TMDZ + 3) × T – 10			ns
		fast mode	(TMDZ + 1) × T – 10			ns
Data output setup time (WRITE mode) D[17:0]&WRZ to E falling	t_{DOSe}	slow mode			(TMDW + 1) × T	ns
		fast mode			0	ns
Data output hold time (WRITE mode) E rising to D[17:0]	t_{DOHe}	slow mode	(TMDZ + 1) × T – 10			ns
		fast mode				
Data input setup time (READ mode) D[17:0] to CSZ&E rising	t_{DISe}	slow mode	50.0			ns
		fast mode				
Data input hold time (READ mode) D[1:0] from CSZ&E rising	t_{DIHe}	slow mode	1 × T			ns
		fast mode	1 × T			ns
Output disable Time (WRITE mode to READ mode) D[17:0] Hi-Z to E falling	t_{ODe}	slow mode	(TMAD + TMDW + 2) × T			ns
		fast mode	0.0			ns

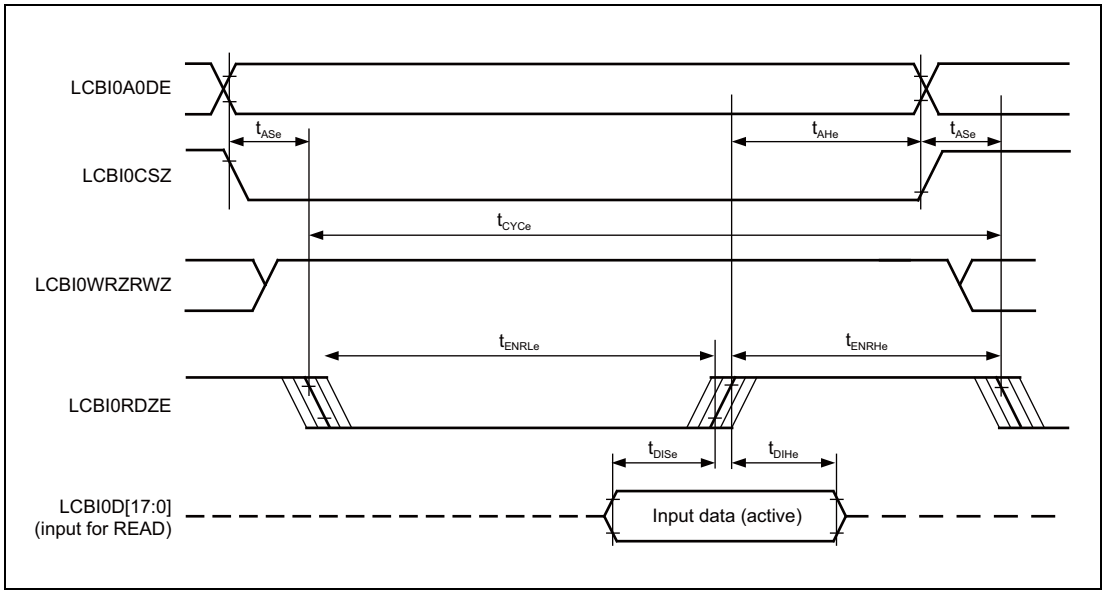


Figure 1.86 LCD Bus Interface E-type Operation Mode (READ)

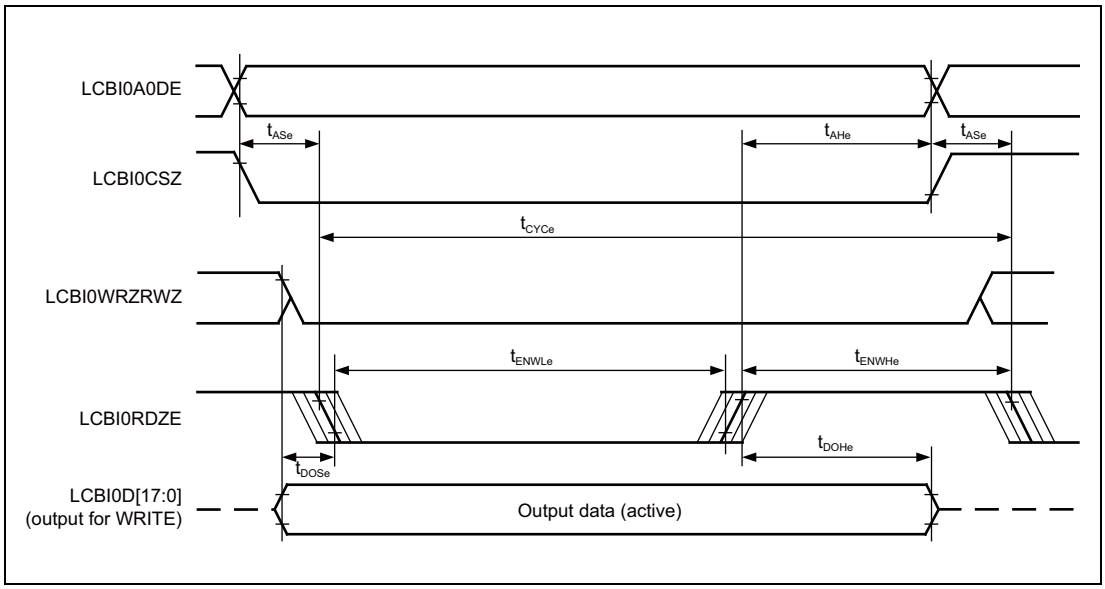


Figure 1.87 LCD Bus Interface E-type Operation Mode (WRITE)

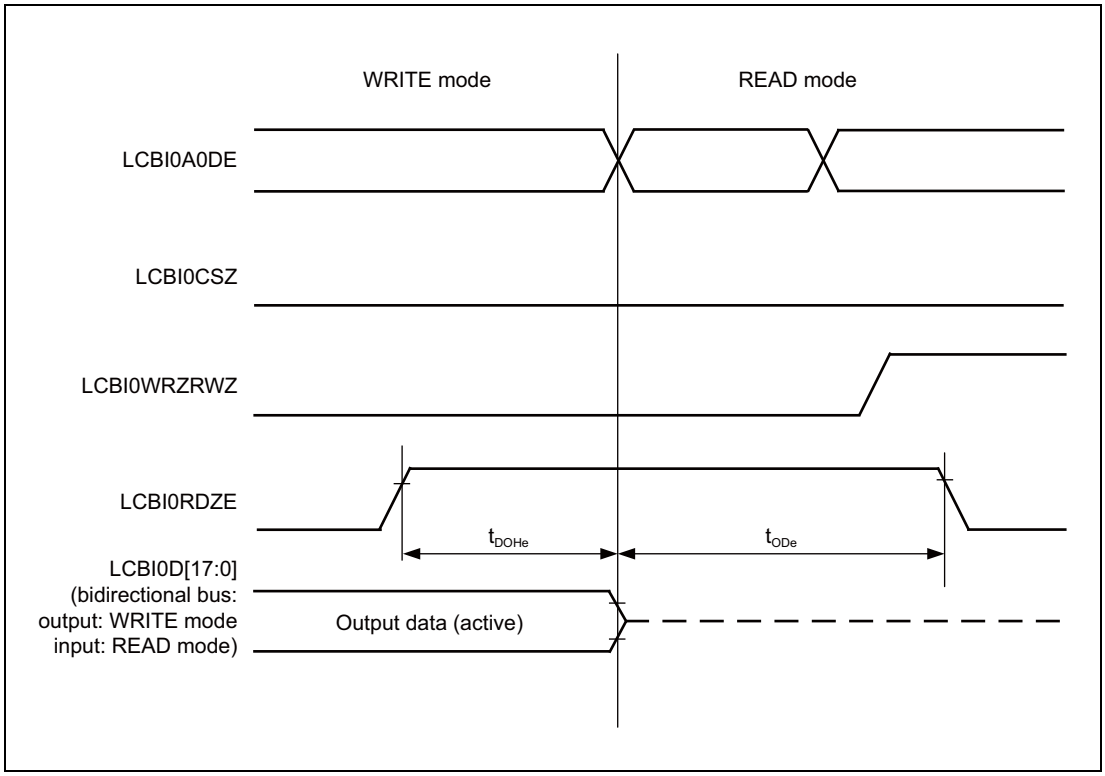


Figure 1.88 LCD Bus Interface E-type Operation Mode (WRITE/READ switch)

Table 1.110 TFT Operation Mode AC Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TFT pixel data clock frequency	f_{DCLKt}				10	MHz
TFT pixel data clock period	t_{DCLK}		$1/f_{DCLKt} - 5 =$ CYC × T – 5			ns
TFT pixel data clock high/low level width	t_{DCLKLt}/ t_{DCLKHt}		$t_{DCLKt/2} - 10$			ns
Address setup time (A0 falling to RDZE falling)	t_{ASt}		(TFDCD + 1) × T			ns
Address hold time (RDZE rising to A0 rising)	t_{AHt}		–10.0			ns
Horizontal synchronization signal setup time ($\overline{HSYNC}$ falling to RDZE falling)	t_{HSYSt}		(TFDCH + 1) × T			ns
Horizontal synchronization signal hold time (RDZE rising to $\overline{HSYNC}$ rising)	t_{HSYHt}		–10.0			ns
Vertical synchronization signal setup time ($\overline{VSYNC}$ falling to RDZA falling)	t_{VSYSt}		(TFDHV + 1) × T			ns
Vertical synchronization signal hold time (RDZE rising to $\overline{VSYNC}$ rising)	t_{VSYHt}		–10.0			ns
Data output hold time (D[17:0] to RDZE falling)	t_{DOSt}				(TFDCD + 1) × T	ns
Data output hold time (RDZE rising to D[17:0])	t_{DOHt}		–10.0			ns

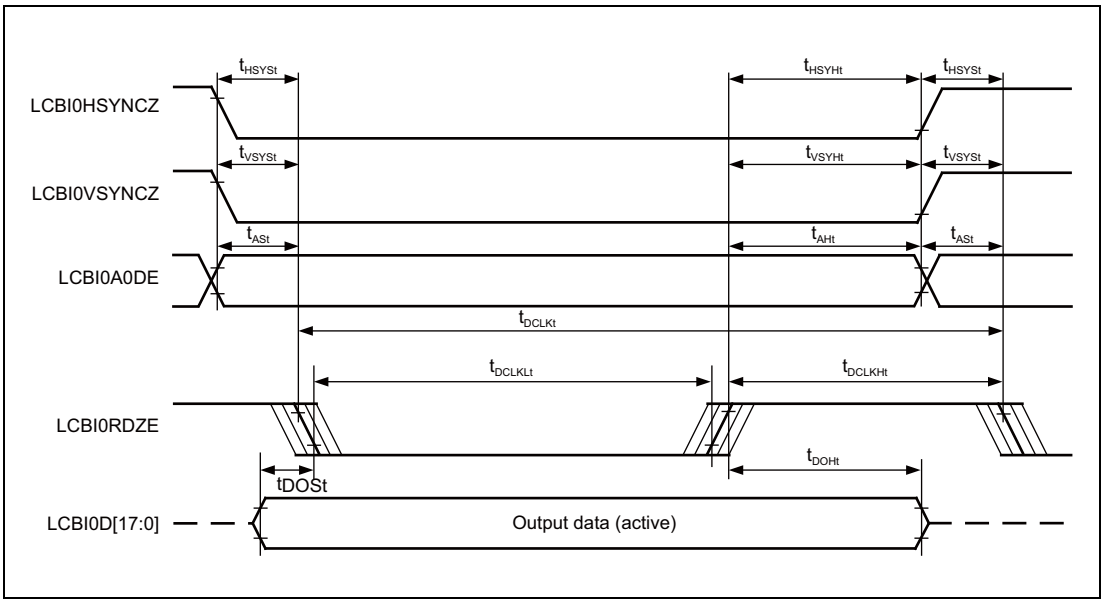


Figure 1.89 LCD Bus Interface TFT Operation Mode (WRITE/READ switch)

1.13 Flash Characteristics

1.13.1 Code Flash

The code flash memory is shipped in the erase state. If the code flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: T_j = –40°C to $+T_{Jmax}$
AWO = powered, ISO = powered

Table 1.111 Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		60	MHz
Operation voltage (actual supply voltage is equal to REG1VCC)	V_{dd}		2.7		5.5	V
Number of rewrites	CWRT	Data retention of 20 years	1000.0			times
Programming temperature (Ta)	TPRG		–40.0		105.0	°C

Note: Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Table 1.112 Timing Characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz P/E < 100 times	256 B		2	6	ms
			8 KB		50	90	ms
			32 KB		200	360	ms
			128 KB		800	1440	ms
		f_{PCLK} ≥ 20 MHz P/E ≥ 100 times	256 B		2.4	7.2	ms
			8 KB		60	108	ms
			32 KB		240	432	ms
			128 KB		960	1728	ms
Erase Time		f_{PCLK} ≥ 20 MHz P/E < 100 times	8 KB		50	120	ms
			32 KB		200	480	ms
			128 KB		800	1750	ms
		f_{PCLK} ≥ 20 MHz P/E ≥ 100 times	8 KB		60	144	ms
			32 KB		240	576	ms
			128 KB		960	2100	ms

1.13.2 Data Flash

The data flash memory is shipped in the erased state. If the data flash memory is read where it has not been written after erasure (no write condition), an ECC error is generated, resulting in the occurrence of an exception.

Condition: T_j = –40°C to +T_{Jmax}
AWO = powered, ISO = powered

Table 1.113 Basic Characteristics

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}		4		60	MHz
Operation voltage (actual supply voltage is equal to REG1VCC)	V_{dd}		2.7		5.5	V
Number of rewrites	CWRT	Data retention of 20 years	125 k			times
		Data retention of 3 years	250 k			times
Programming temperature (Ta)	TPRG		–40.0		105.0	°C

Note: Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Table 1.114 Timing Characteristics

Parameter	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.3	1.7	ms
			64 B		4.8	13	ms
Erase Time		f_{PCLK} ≥ 20 MHz	64 B		3	10	ms
			32 KB		1.6	5.2	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30	µs
			64 B			100	µs

1.14 Power Supply Current

1.14.1 Operation Current Consumption (RH850/D1L1)

Condition: T_j = –40°C to + T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0V
Clock setting:
CPU: 120 MHz, AXI: 60 MHz, APB: 60 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.115 Dynamic Current (D1L1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of $REG0V_{CC}$	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of $REG1V_{CC}$	$I_{OREG1VCC}$	REG1VCC = 3.0 to 5.5 V			70	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.116 Static Current (D1L1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of $REG0V_{CC}$	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of $REG1V_{CC}$	$I_{SREG1VCC}$	REG1VCC = 3.0 to 5.5 V			75	mA

1.14.2 Operation Current Consumption (RH850/D1L2(H))

Condition: T_j = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0V
Clock setting:
CPU: 120 MHz, AXI: 60 MHz, APB: 60 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.117 Operation Current (D1L2(H))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of REG0V_{CC}	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of REG1V_{CC}	$I_{OREG1VCC}$	REG1VCC = 3.0 to 5.5 V			105	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.118 Static Current (D1L2(H))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of REG0V_{CC}	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of REG1V_{CC}	$I_{SREG1VCC}$	REG1VCC = 3.0 to 5.5 V			115	mA

1.14.3 Operation Current Consumption (RH850/D1M1 (HLQFP176))

Condition: T_j = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
CPU: 160 MHz, AXI: 80 MHz, APB: 80 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.119 Operation Current (D1M1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of REG0V_{CC}	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of REG1V_{CC}	$I_{OREG1VCC}$	REG1VCC = 3.0 to 3.6 V			145	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.120 Static Current (D1M1)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of REG0V_{CC}	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of REG1V_{CC}	$I_{SREG1VCC}$	REG1VCC = 3.0 to 3.6 V			260	mA

1.14.4 Operation Current Consumption (RH850/D1M1H (BGA))

Condition: T_j = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
CPU: 200 MHz, AXI: 100 MHz, APB: 50 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.121 Operation Current (D1M1H)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of REG0V_{CC}	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of REG1V_{CC}	$I_{OREG1VCC}$	REG1VCC = 3.0 to 3.6 V			170	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.122 Static Current (D1M1H)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of REG0V_{CC}	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of REG1V_{CC}	$I_{SREG1VCC}$	REG1VCC = 3.0 to 3.6 V			260	mA

1.14.5 Operation Current Consumption (RH850/D1M1A)

Condition: T_j = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
CPU: 240 MHz, AXI: 120 MHz, APB: 60 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.123 Operation Current (D1M1A)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of REG0V_{CC}	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of REG1V_{CC}	$I_{OREG1VCC}$	REG1VCC = 3.0 to 3.6 V			205	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.124 Static Current (D1M1A)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of REG0V_{CC}	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of REG1V_{CC}	$I_{SREG1VCC}$	REG1VCC = 3.0 to 3.6 V			310	mA

1.14.6 Operation Current Consumption (RH850/D1M1-V2)

Condition: T_j = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
CPU: 160 MHz, AXI: 80 MHz, APB: 80 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.125 Operation Current (D1M1-V2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of REG0V_{CC}	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of REG1V_{CC}	$I_{OREG1VCC}$	REG1VCC = 3.0 to 3.6 V			165	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.126 Static Current (D1M1-V2)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of REG0V_{CC}	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of REG1V_{CC}	$I_{SREG1VCC}$	REG1VCC = 3.0 to 3.6 V			150	mA

1.14.7 Operation Current Consumption (RH850/D1M2(H))

Condition: Tj = –40°C to +T_{Jmax}
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
CPU: 240 MHz, AXI: 120 MHz, APB: 60 MHz
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
Please apply both dynamic and static current for total current of each domain.
AWO = powered, ISO = powered

Table 1.127 Operation Current (D1M2(H))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of $REG0V_{CC}$	$I_{OREG0VCC}$	REG0VCC = 3.0 to 5.5 V			2	mA
Operation Current of $REG1V_{CC}$	$I_{OREG1VCC}$	REG1VCC = 3.0 to 5.5 V			22	mA
Operation Current of $ISOV_{DD}$	$I_{OISOVDD}$	ISOVDD = 1.15 to 1.35 V			230	mA
Operation Current of $PLLV_{CC}$	$I_{OPLLVCC}$	PLLVCC = 3.0 to 5.5 V			12	mA
Operation Current of SDRBVcc	$I_{OSDRBVCC}$	SDRBVCC = 1.7 to 1.9 V			230	mA

Remark: OSCVCC current depend on frequency and external logics for Main oscillator. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Table 1.128 Static Current (D1M2(H))

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Static Current of $REG0V_{CC}$	$I_{SREG0VCC}$	REG0VCC = 3.0 to 5.5 V			3	mA
Static Current of $REG1V_{CC}$	$I_{SREG1VCC}$	REG1VCC = 3.0 to 5.5 V			3	mA
Static Current of $ISOV_{DD}$	$I_{SISOVDD}$	ISOVDD = 1.15 to 1.35 V			420	mA
Static Current of $PLLV_{CC}$	$I_{SPLLVCC}$	PLLVCC = 3.0 to 5.5 V			3	mA
Static Current of SDRBVcc	$I_{SSDRBVCC}$	SDRBVCC = 1.7 to 1.9 V			20	mA

1.14.8 Stand-by Current Consumption (RH850/D1Lx,D1Mx)

Condition: T_j = –40°C to 85°C
Vss = OSCVss = REGnVss = EVss = ISOVss = PLLVss = BnVss = RVss = MVss = SFVss = ISMVss = ZPDVss = SDRAVss =SDRBVss = A0Vss = 0 V
Clock setting:
f_{RL}: On
IO current: The input/output current is mainly part of the special application use case and not covered in this “Power supply current”. Excluded from this are some currents that need to be considered separately.
AWO = powered, ISO = Off.
Typ condition indicate following condition
- Each VCC set to 5.0 V
- T_j = 25°C
- Device = center condition

Table 1.129 Stand-by Current

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation Current of $OSCV_{CC}$	I_{OSCVCC}	f_{XT}: On, f_X: Off			4	µA
		f_{XT}: On, f_X: Off, Each VCC set to 5.0 V, T_j = 25°C			2	µA
		f_{XT}: Off, f_X: On[*1] Each VCC set to 5.0 V, T_j = 25°C			340	µA
		f_{XT}: Off, f_X: Off Possible to turn off			1	µA
Operation Current of $REG0V_{CC}$	$I_{REG0VCC}$	f_{XT}: On, f_X: Off, T_j = 85°C			430	µA
		f_{XT}: On, f_X: Off, Each VCC set to 5.0 V, T_j = 25°C		40		µA
		f_{XT}: Off, f_X: On, T_j = 85°C			800	µA
		f_{XT}: Off, f_X: On, Each VCC set to 5.0 V, T_j = 25°C		70		µA
		f_{XT}: Off, f_X: Off, f_{RL}: On, f_{RH}: Off, Tj = 40°C, Each VCC set to 5.0 V, all peripheral stop			90	µA
Leakage Current of $PLLV_{CC}$	I_{PLLVCC}	Possible to turn off		0.3	0.5	µA
Leakage Current of $REG1V_{CC}$	$I_{REG1VCC}$	Possible to turn off		2	3	µA
Leakage Current of $A0V_{CC}$	I_{A0VCC}	D1M2(H), D1L2(H) Possible to turn off — TSN never activated		0.1	1.0	µA
		D1M2(H), D1L2(H) Possible to turn off — TSN was activated			25.0	µA
		D1M1(H), D1M1A, D1L1 Possible to turn off		0.1	1.0	µA
Leakage Current of $A0V_{REF}$	I_{A0VREF}	Possible to turn off < $A0V_{CC}$		0.1	1	µA
Operation Current of EV_{CC}	I_{EVCC}	T_j = 85°C		1	20	µA
		Each VCC set to 5.0 V, T_j = 25°C			1	µA
Leakage Current of ZPDVCC/ZPDVREF	I_{ZPDVCC}	Possible to turn off		0.1	2	µA

Note 1. Main oscillator current depend on frequency (AMPSEL setting) and external logics. Detail specs please refer to **Section 1.5.14.1, Main Oscillator**.

Section 2 Package

2.1 Junction-to-Ambient Resistance

The simplest method to determine the actual chip temperature is to use the single resistance metric of θja. The following equation may be used:

$$Tj = Ta + (Ptot \times \theta ja)$$

- Tj: is the chip junction temperature in [°C]
- Ta: is the ambient temperature (according to JEDEC standard JESD51-2A) in [°C]
- Ptot: is the total power consumption (refer to section DC characteristic) in [W]
- θja is the thermal resistance between junction and ambient in [°C/W]

This simple metric considers the test board properties in a natural convection environment. The thermal resistance is derived from a defined test fixture (JEDEC) or simulation of such test fixture using a 3D simulation with a detailed model. Since real application is usually quite different from this environment, the error in determining the maximum Tj can be quite big. The amount of deviation depends entirely on the application and can easily reach >30%.

A sufficient margin to Tjmax must be applied, considering the simulation error.

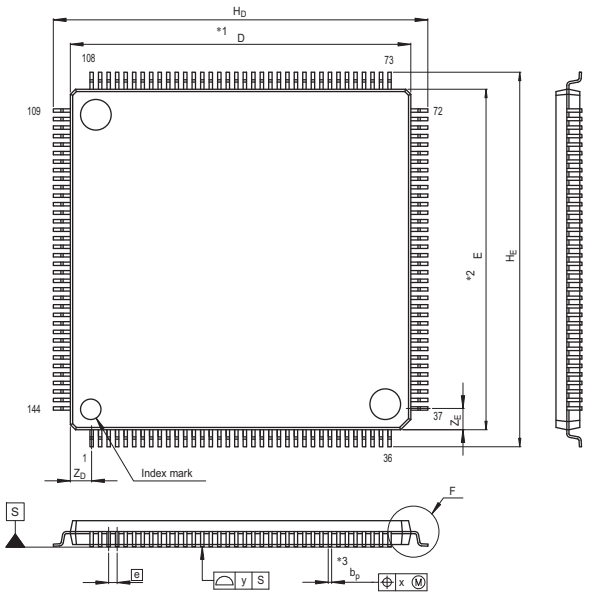
Table 2.1 Thermal resistance – Junction-to-ambient resistance

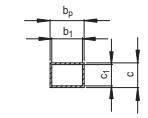
Device	Symbol	Condition	Package	Value	Unit
D1L1 (R7F701401)	θja	JEDEC	QFP144	37.1	°C/W
D1L2 (R7F701402)	θja	JEDEC	QFP144	35	°C/W
D1L2H (R7F701403)	θja	JEDEC	LQFP176	35	°C/W
D1M1 (R7F701404/R7F701405)	θja	JEDEC	HLQFP176	15	°C/W
D1M1H (R7F701406/R7F701407)	θja	JEDEC	PBGA272	22	°C/W
D1M2 (R7F701408/R7F701410)	θja	JEDEC	PBGA376	17	°C/W
D1M2H (R7F701412/R7F701411)	θja	JEDEC	PBGA484	15	°C/W
D1M1A (R7F701441)	θja	JEDEC	PBGA272	18.9	°C/W
D1M1-V2 (R7F701442)	θja	JEDEC	LQFP176	29.2	°C/W

2.2 Device Packages

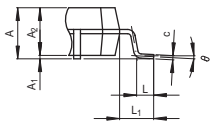
2.2.1 D1L2/D1L1 Devices (R7F01401/R7F701402)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP144-20x20-0.50	PLQP0144KA-A	144P6Q-A / FP-144L / FP-144LV	1.2g





Terminal cross section



Detail F

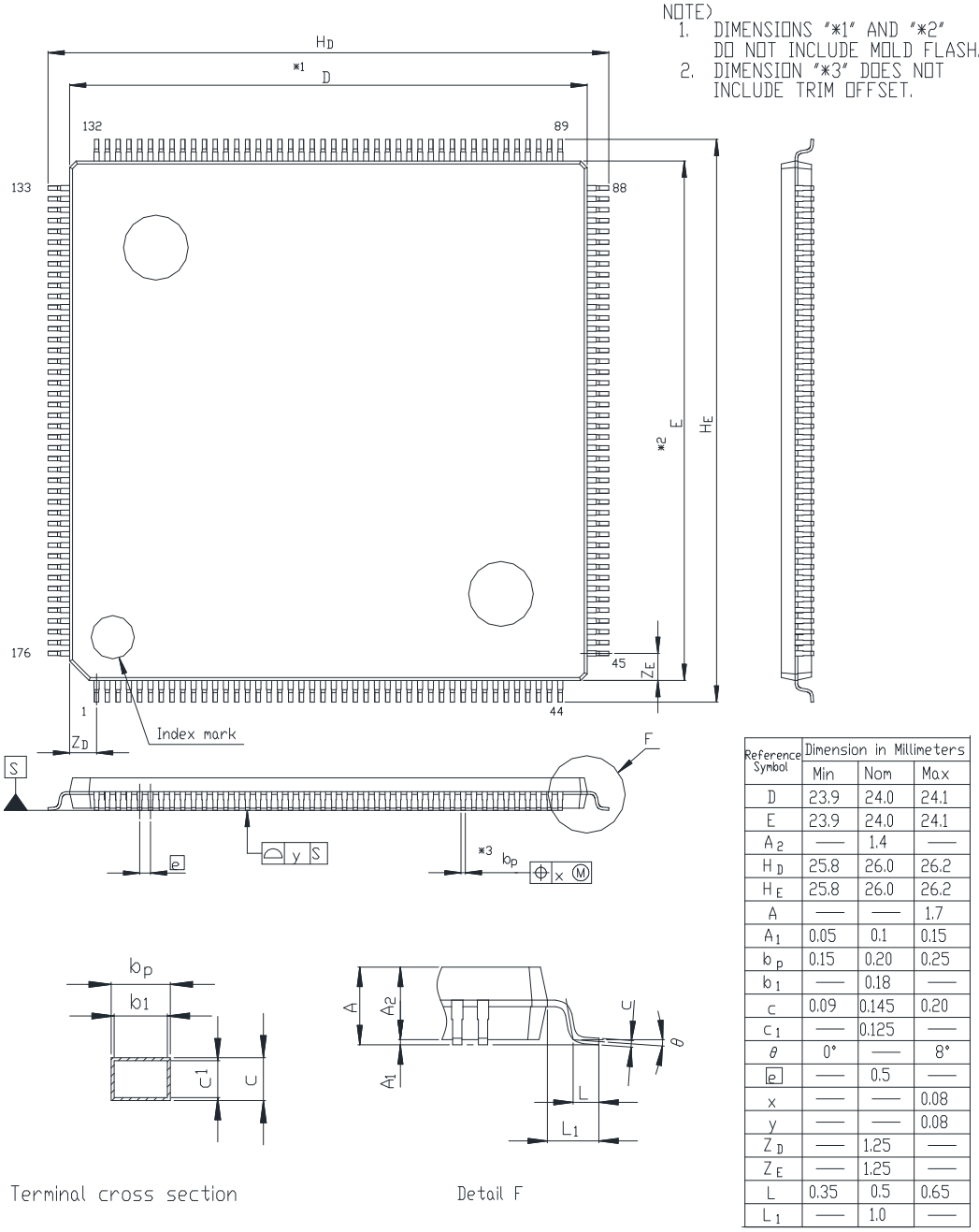
NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	19.9	20.0	20.1
E	19.9	20.0	20.1
A_2	—	1.4	—
H_D	21.8	22.0	22.2
H_E	21.8	22.0	22.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.17	0.22	0.27
b_1	—	0.20	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.10
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.1 144-pin Plastic QFP, 0.5 mm Pin-pitch

2.2.2 D1L2H/D1M1-V2 Devices (R7F701403/R7F701442)

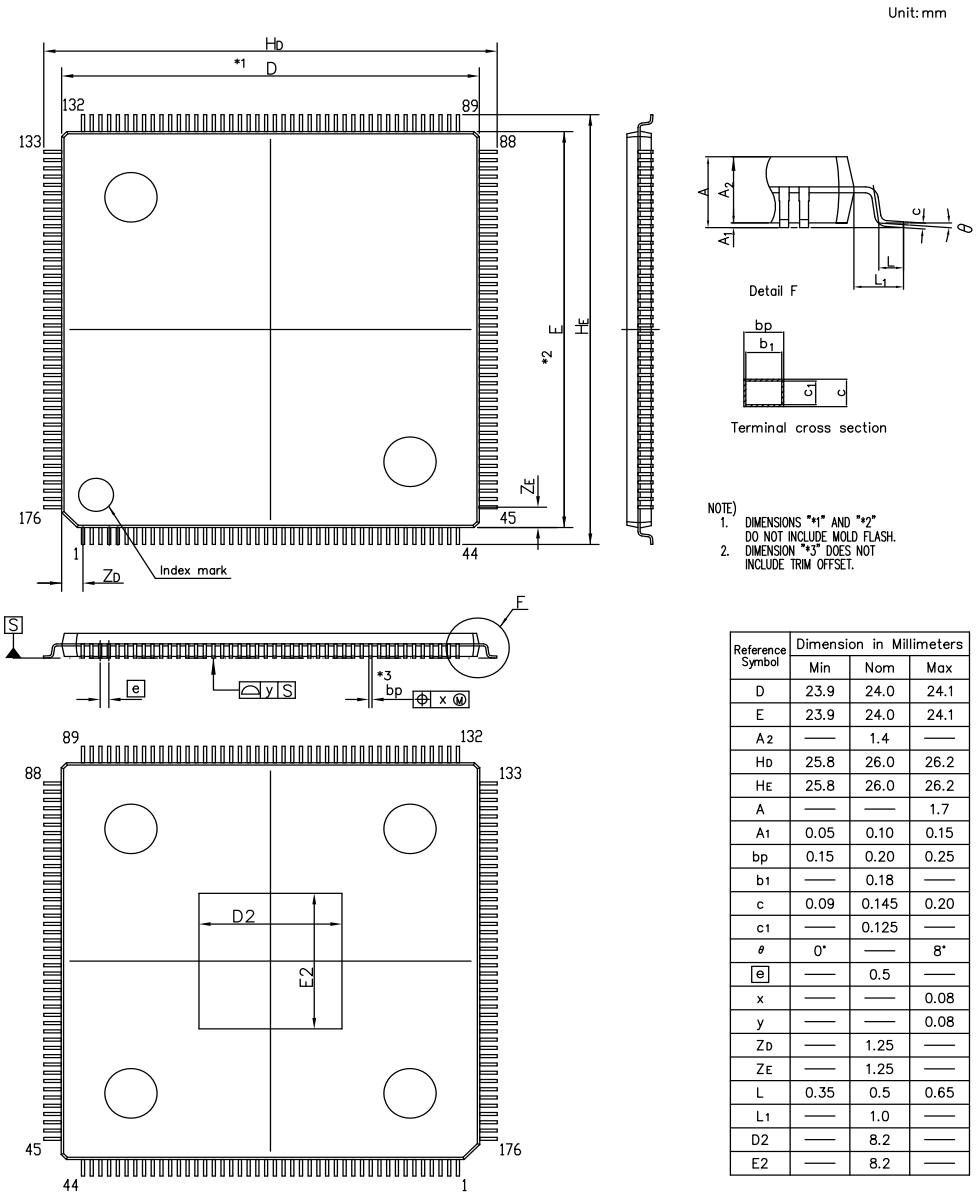
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 2.2 176-pin Plastic QPF, 0.5 mm Pin-pitch

2.2.3 D1M1 Devices (R7F701404/R7F701405)



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.10	0.15
bp	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—
D2	—	8.2	—
E2	—	8.2	—

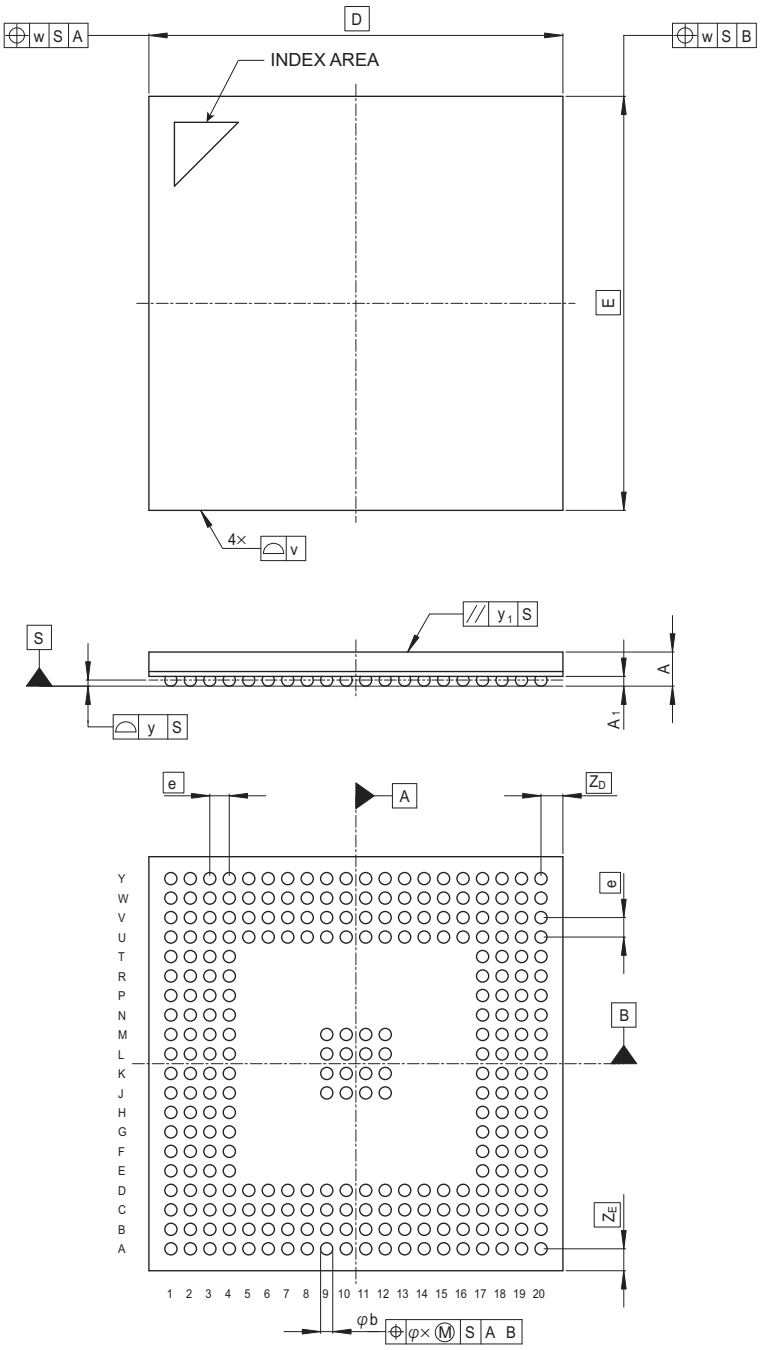
Note 1. The exposed die pad is internally (inside of the package) connected.

Note 2. The exposed die pad must either be connected to GND on the PCB or must be left unconnected on the PCB. It is recommended to connect the exposed die pad to GND on the PCB.

Figure 2.3 176-pin Plastic QPF, 0.5 mm Pin-pitch with Exposed Pad

2.2.4 D1M1H/D1M1A Devices (R7F701406/R7F701407/R7F701441)

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-BGA272-21x21-1.00	PRBG0272FA-A	BP-272/BP-272V	1.3g

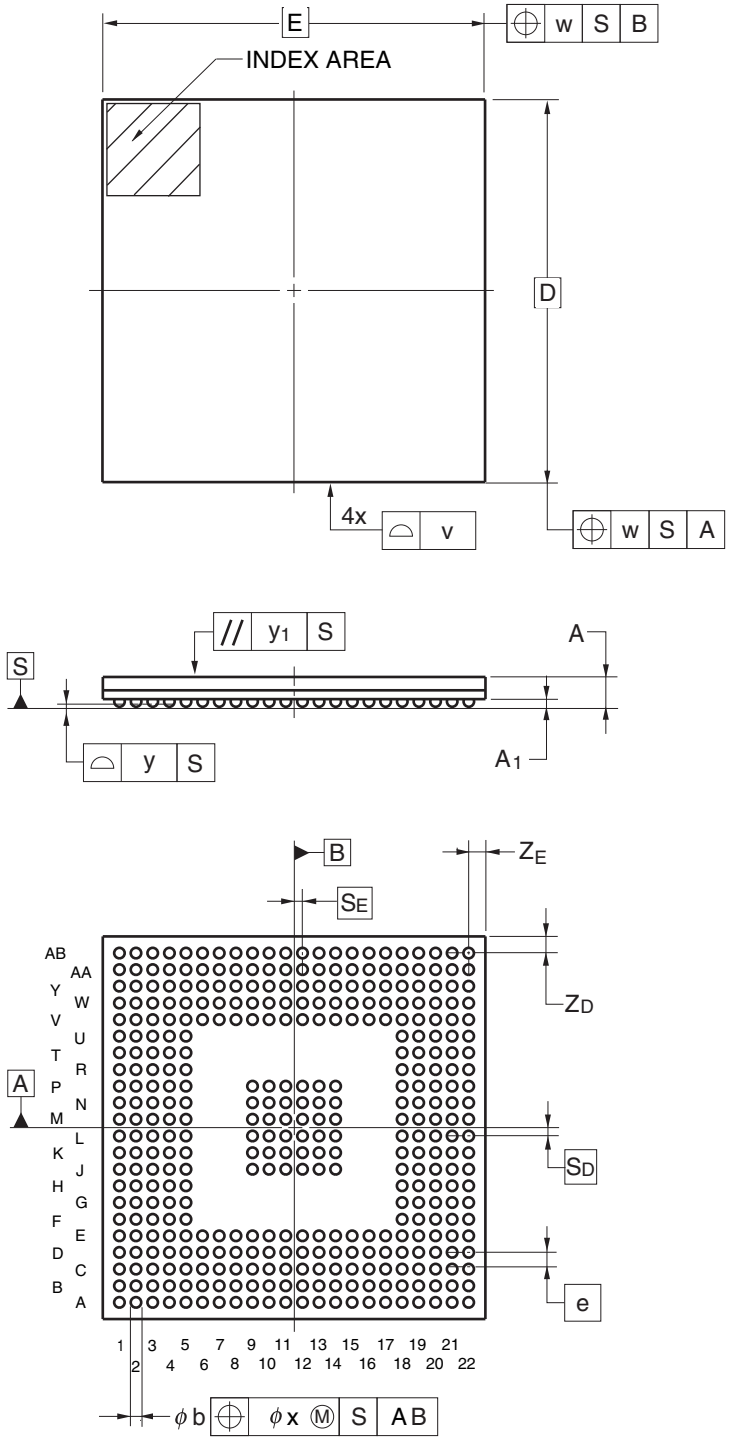


Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	21.0	—
E	—	21.0	—
v	—	—	0.20
w	—	—	0.30
A	—	—	2.10
A_1	0.36	0.46	0.56
e	—	1.00	—
b	0.53	0.63	0.73
x	—	—	0.10
y	—	—	0.15
y_1	—	—	0.35
S_D	—	—	—
S_E	—	—	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure 2.4 272-pin Plastic BGA, 1.0 mm Ball-pitch, 19 × 19 mm^2 Size

2.2.5 D1M2 Devices (R7F701408/R7F701410)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-BGA376-23x23-1.00	PRBG0376FB-A	T376F1-100-KNJ	-

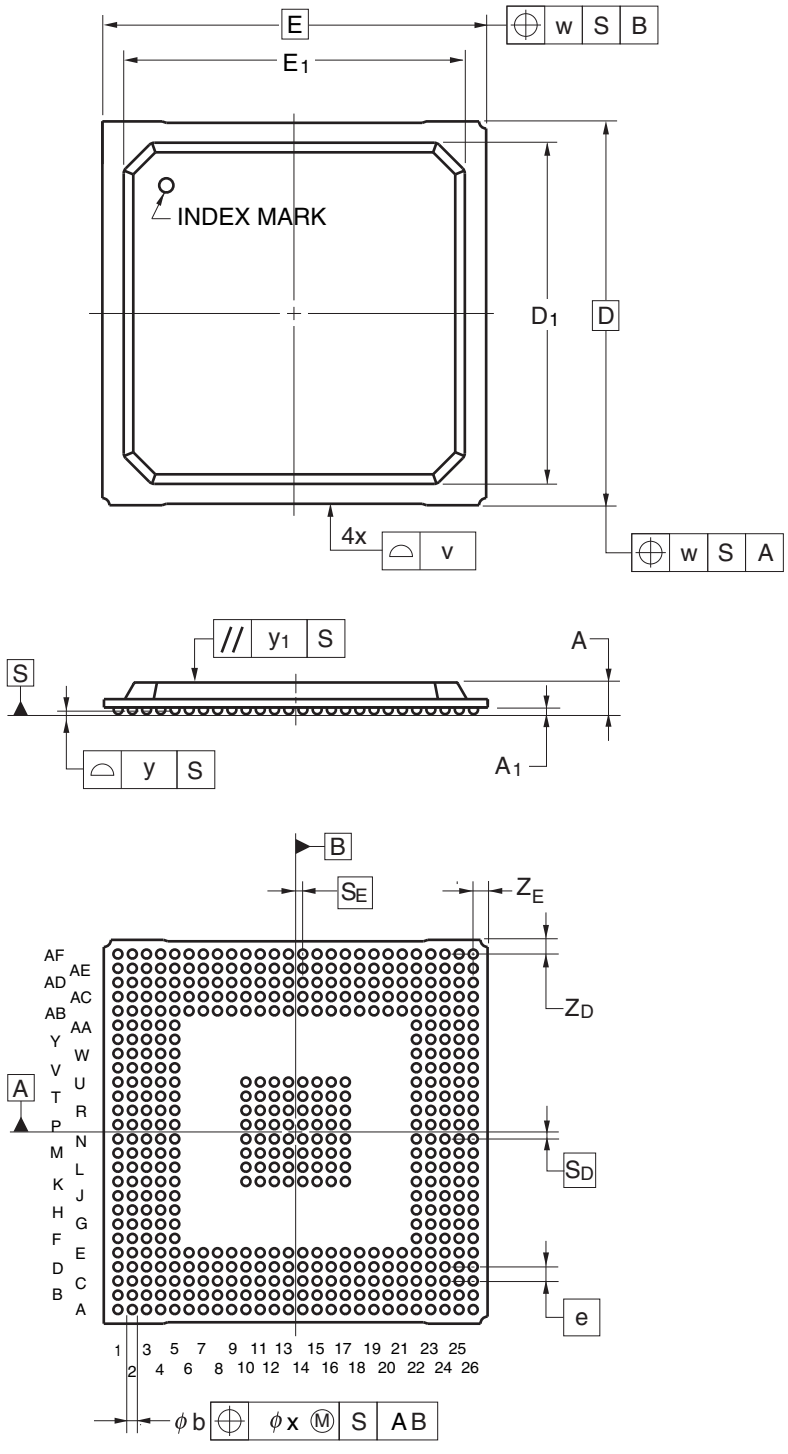


Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	23.00	—
E	—	23.00	—
v	—	—	0.15
w	—	—	0.30
A	—	—	2.10
A_1	0.36	0.46	0.56
e	—	1.00	—
b	0.53	0.63	0.73
x	—	—	0.15
y	—	—	0.15
y_1	—	—	0.35
S_D	—	0.50	—
S_E	—	0.50	—
Z_D	—	1.00	—
Z_E	—	1.00	—

Figure 2.5 376-pin Plastic BGA, 1.0 mm Ball-pitch, 23 × 23 mm^2 Size

2.2.6 D1M2H Devices (R7F701412/R7F701411)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-BGA484-27x27-1.00	PRBG0484FF-A	T484F1-100-MNW	-



Referance Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	27.00	—
E	—	27.00	—
v	—	—	0.20
w	—	—	0.30
A	—	—	2.60
A_1	0.36	0.46	0.56
e	—	1.00	—
b	0.53	0.63	0.73
x	—	—	0.15
y	—	—	0.15
y_1	—	—	0.35
S_D	—	0.50	—
S_E	—	0.50	—
Z_D	—	1.00	—
Z_E	—	1.00	—
D_1	—	24.00	—
E_1	—	24.00	—

Figure 2.6 484-pin Plastic BGA, 1.0 mm Ball-pitch, 27 × 27 mm^2 Size

REVISION HISTORY	RH850/D1L/D1M Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 28, 2015	—	First Edition issued
1.10	Jul 31, 2015	All	Unit unified: µsec → µs
		All	Unit unified: msec → ms
		All	Unit unified: nsec → ns
		Product Introduction	
		1	RH850/D1M2: Notice corrected (R7F701408 → R7F701408 and R7F701410, R7F701410 → R7F701411 and R7F701412)
		3	• RH850/D1L: Note 2 corrected
		5, 6	• RH850/D1M: ISO corrected, Note 2 corrected
		10	Figure of D1M2(H) block diagram: Video channel 0 corrected
		17	Terms for Temperature: Description corrected
		Section 1 Electrical Specifications	
		22	1.1.3 Pin Information for D1L1: Section title corrected
		22	Table 1.1 Pin Information for D1L1: Table tittle corrected, output buffer of GP corrected, “HS” column for input buffer added
		23	Table 1.2 Pin Information for D1L2, D1L2H: “HS” column for input buffer added, “×” mark of the “CMOS1” column (P21) for input buffer deleted
		24	Table 1.3 Pin Information for D1M1, D1M1H: “HS” column for input buffer added, “×” mark of the “CMOS1” column (P21) for input buffer deleted
		25, 26	Table 1.4 Pin Information for D1M2, D1M2H: “HS” column for input buffer added, “×” marks of the “CMOS1” column (P21_0 to P21_9, P21_10 to P21_12) for input buffer deleted
		32	Table 1.6 VCC / VDD Data: Symbol and ratings of the system corrected, symbol of the internal voltage regulator corrected, remark corrected (Remark → Note 3)
		40	Table 1.11 Power-up Restrictions: Parameter column corrected
		42	Table 1.15 Power-up Restrictions: Parameter column corrected, Note 2 added
		42	Table 1.16 Power-down Restrictions: Parameter column corrected
		46	Figure 1.6 Power-up Sequence: Corrected (ZPDVCC drawing deleted, BnVCC/MVCC/RVCC/ISMVCC(3.3/5V)SFVCC(3.3V) → BnVCC/MVCC/RVCC/ISMVCC/ZPDVCC(3.3/5V)SFVCC(3.3V))
		47	Figure 1.7 Power-down Sequence: Corrected (ZPDVCC drawing deleted, BnVCC/MVCC/RVCC/ISMVCC(3.3/5V)SFVCC(3.3V) → BnVCC/MVCC/RVCC/ISMVCC/ZPDVCC(3.3/5V)SFVCC(3.3V))
		49	Figure 1.10 Voltage Supply D1Lx: Figure title corrected
		50	Figure 1.11 Voltage Supply D1M1(H): Figure title corrected
		51	Figure 1.12 Voltage Supply D1M2(H): Figure title corrected, Note 2 corrected
		56	(2) XC bus Modules Clock: Description corrected (DDR2-SDRAM → SDR-SDRAM and DDR2-SDRAM)
		58	Table 1.26 Main Oscillator Characteristics: TYP. and MAX. value of I_{DDMOSC} corrected, unit of I_{DDMOSC} corrected, condition and spec of I_{DDMOSC} added, Note 2 and Note 3 added
		61	Table 1.30 PLL0 Characteristics: PLLVCC and ISOVDD deleted
		61	Table 1.31 PLL1 (D1M2(H)) Characteristics: PLLVCC and ISOVDD deleted
		61	Table 1.32 PLL1(D1M1/D1Lx), PLL2 Characteristics: PLLVCC and ISOVDD deleted
		62	Table 1.33 Voltage Regulator: Corrected, Note 1 added
		63	(1) Frequency Control of GP Port Buffers: Condition corrected
		63	Table 1.34 GP Output Buffer Characteristic: Condition of the output voltage high level corrected, condition of the output voltage low level corrected
		64	1.6.1.2 AN Port Buffer: Heading level corrected
		64	1.6.1.3 HS Port Buffer: Heading level corrected
		64	Table 1.36 HS Output Buffer Characteristic: Condition of the output frequency corrected (D1M1/D1L2: SFVCC ≥ 3.12 V → D1M1/D1L2: SFVCC ≥ 3.15 V, D1M1H: SDRAVCC ≥ 3.0V added, SFVCC ≤ 3.12 V → SFVCC < 3.15 V)

Rev.	Date	Description	
		Page	Summary
1.10	Jul 31, 2015	65	1.6.1.4 MLB Port Buffer: Heading level corrected
		65	1.6.1.5 HD Port Buffer: Heading level corrected
		65	Figure 1.16 Output Current Diagram of SMDIO Buffer (valid only at Ta = –40°C): Corrected (5 mA → 2mA)
		67	Table 1.38 HD Output Buffer Characteristic: Value of V_{OHd2} and V_{OLd2} corrected (I_{OHd2} ≤ –1 mA → I_{OHd2} ≤ –2 mA, I_{OLd2} ≤ 1 mA → I_{OLd2} ≤ 2 mA)
		68	1.6.1.6 RSDS Port Buffer: Heading level corrected, description corrected (Figure E.5 →Figure 1.19)
		70	1.6.1.7 DDR2-SDRAM Port Buffer: Heading level corrected
		70	Table 1.40 DDR2-SDRAM Buffer Characteristics: Note 4 added
		—	1.6.4 Overload Condition: Deleted
		—	1.6.5 Input Leakage Current at Overload Condition for Analog Buffer: Deleted
		76	Table 1.52 IO Buffer Capacitance: MAX. value corrected
		76	Table 1.53 Input Buffer Capacitance: MAX. value corrected
		77	Table 1.54 Reset AC Characteristic: Corrected
		78	Table 1.55 Interrupt AC Characteristics: MIN. value corrected
		79	Table 1.56 System Pins AC Characteristics: MIN. value of t_{SPRJ} corrected
		79	1.7.3 System Pins Timing: NOTE corrected
		80	Table 1.57 Clock Output Mode via GPIO Buffer: Condition of t_{FPH}/t_{FPL} corrected, t_{FPH} row deleted
		80	Table 1.58 ECM ERROUT AC Characteristic: Added
		81	(2) Maximum Pulse Rejection Width: Formula corrected
		81	(4) Maximum Delay Time: Formula corrected
		83	Table 1.59 ADC Characteristic: MIN. and MAX. value of the conversion result for positive overload condition corrected
		94	Table 1.63 POC Characteristic on AWO: Condition of ts_{POC0R} and ts_{POC0F} corrected
		96	Table 1.64 POC Characteristic on ISO: Condition of ts_{POC1R} and ts_{POC0F} corrected
		99	Table 1.67 Temperature Sensor Specification: Value and unit of the temperature detect accuracy corrected
		100	Table 1.68 Timer TAUB/TAUJ AC Specification*1: MIN. value of t_{TAURJ} corrected
		105	Table 1.71 Slave Mode AC Characteristics: MIN. value of t_{KWHS} and t_{KWLS} corrected, MAX. value of t_{DSOS} and t_{DRYO} corrected
		117	Table 1.73 Slave Mode AC Characteristics: MIN. value of t_{KWHS} and t_{KWLS} corrected, MAX. value of t_{DSOS} and t_{DRYO} corrected
		118	Table 1.75 I^2C AC Characteristics: Unit of f_{CLK} corrected (KHz → kHz)
		121	Table 1.79 PCM-PWM Converter Characteristics: Unit of f_{PWMOP} corrected (KHz → kHz)
		124	1.10.10 RS-CAN Interface: NOTE corrected
		127	1.10.12.2 LPD 4pin Interface: MIN. value of $t_{LPDCKOWH}$/$t_{LPDCKOWL}$ corrected
		129	Table 1.84 SFMA AC Characteristics (D1M2/D1M1/D1L2): Corrected
		130	Figure 1.75 SFMA Wave Form: error corrected (HSFI IF clk → SFMA IF clk)
		131	Table 1.87 SDR-SDRAM AC Characteristics (D1M1H): MIN. value of t_{CK} corrected
		132	Table 1.88 Video Output AC Characteristics - LVTTL Mode(D1Mx): MIN. value of t_{OH} and t_{SOH} corrected, MAX. value of f_{DCLK}, t_{DCLK}, t_{OV} and t_{SOV} corrected, Note 1 corrected
		132	Table 1.89 Video Output AC Characteristics (D1L2): MIN. value of t_{OH} and t_{SOH} corrected, MAX. value of f_{DCLK}, t_{OV} and t_{SOV} corrected, Note 1 corrected
		134	Table 1.90 RSDS Interface AC Characteristics: MIN. value of RCHP/RCLP, RSTU and RHLD corrected, TYP. value of SPSTU and SPHLD corrected, unit of SPSTU and SPHLD corrected
		135	Table 1.91 Video Input AC Characteristics: MIN. value of t_{VIS} and t_{VIH} corrected, MAX. value of t_{CKIR} and t_{CKIF} corrected
		135	Table 1.92 MIPI-CSI 2 Interface AC Characteristics: MIN. value of t_{CYC}, Tsu and Thld corrected, unit of t_{CYC} corrected

Rev.	Date	Description	
		Page	Summary
1.10	Jul 31, 2015	136	Table 1.93 RAM Operation Mode AC Characteristics: t_{AHr}, t_{WRZLr}, t_{RDZLr}, t_{DOHr} and t_{DISr} corrected (separate specs for “slow mode” and “fast mode” → common spec for “slow mode” and “fast mode”), unit of t_{CYCr} corrected
		139	Table 1.94 E-type Operation Mode AC Characteristics: t_{AHe}, t_{ENRLe}/t_{ENWLe}, t_{DOHe}, t_{DISe}, corrected (separate specs for “slow mode” and “fast mode” → common spec for “slow mode” and “fast mode”), unit of t_{CYCe} and t_{DIHe} corrected
		145	Table 1.100 Dynamic Current (D1L1): MAX. value of $I_{OREG1VCC}$ corrected
		145	Table 1.101 Static Current (D1L1): MAX. value of $I_{SREG1VCC}$ corrected
		149	Table 1.108 Operation Current (D1M2(H)): MAX. value of $I_{OSDRBVCC}$ corrected
		149	Table 1.109 Static Current (D1M2(H)): MAX. value of $I_{SSDRBVCC}$ corrected
		150	Table 1.110 Stand-by Current: MAX. value of $I_{REG0VCC}$ corrected, leakage Current of ZPDVCC/APDVREF added
		Section 2 Package	
		151	Table 2.1 Thermal resistance – Junction-to-ambient resistance: Value of the D1L1 (R7F701401) corrected
1.20	Feb 04, 2016	1	Product Introduction: Description of “Notice” deleted
		4	Function Overview, RH850/D1M: CAN Interface (RS-CANFD) corrected
		29	(3) Load Conditions: NOTES corrected
		53	Table 1.20 Overload Current: Ratings for “Pin supplied by RVCC” corrected
		61	Table 1.30 PLL0 Characteristics: MIN. and MAX. value for “PLL frequency dithering range” corrected
		63	1.6.1.1 GP Port Buffer, (1) Frequency Control of GP Port Buffers: Description corrected
		64	Table 1.35 AN Output Buffer Characteristic: Note 2 corrected
		68	Table 1.39 Differential LVDS Mode: MIN., TYP. and MAX. of Irsds corrected
		71	Table 1.42 Schmitt1 Input Characteristic: MIN. value of V_{IHa2} corrected
		74	Table 1.49 Pull-up and Pull-down Resister Characteristic: MAX. value of R_{PU}, R_{PD} and R_{PU} corrected
		75	Table 1.51 Input Leakage Current for SFVCC of P21_[9:0] (D1M1/D1L2): MIN. value of $I_{inLeakH}$, and MAX. value of $I_{inLeakL}$ corrected
		77	1.7.1 $\overline{\text{RESET}}$: Condition corrected
		77	Table 1.54 Reset AC Characteristic: Symbol and MIN. value for “RESET low-level width” corrected, *1 added, Note 3 deleted
		83	1.8.1 Analog/Digital Converter (ADCE): Section title corrected
		87	1.8.1.3 A/D Converter Trigger Timing: Description corrected
		96	Table 1.64 POC Characteristic on ISO: Condition for ts_{POC1R} corrected, symbol and condition for “Response time at power-down” corrected
		99	Table 1.67 Temperature Sensor Specification: MAX. value for “Standby current” corrected
		105	Table 1.71 Slave Mode AC Characteristics: MIN. value (filter-bypassed) of t_{KCYM}, t_{KWHS} and t_{KWLS} corrected
		129	Table 1.84 SFMA AC Characteristics (D1M2/D1M1/D1L2): Condition and MIN. value of t_{DIS} added, MIN. value of t_{DOV} corrected, spec. for “Data input setup/hold window for 1 device at one temperature” added
		129	Table 1.85 SFMA AC Characteristics (D1L1): MIN. and MAX. value of t_{CSS}, t_{DIS}, t_{DIH}, t_{DOV} and t_{ODS} corrected
		143	Table 1.96 Basic Characteristics: MAX. value of f_{PCLK} corrected
		145	Table 1.100 Dynamic Current (D1L1): MAX. value of $I_{OREG1VCC}$ corrected
		145	Table 1.101 Static Current (D1L1): MAX. value of $I_{SREG1VCC}$ corrected
		150	Table 1.110 Stand-by Current: Spec in “Operation current of REG0VCC” added, spec. for I_{A0VCC} corrected
		154	2.2.4 D1M1 Devices (R7F701404/R7F701405): Figure 2.4 176-pin Plastic QPF, 0.5 mm Pin-pitch with Exposed Pad added
2.00	Dec 14, 2018	Product Introduction	
		1	Product Introduction: Notice added
		4 to 9	RH850/D1M (Table): Changed by additional line-up (D1M1A)

Rev.	Date	Description	
		Page	Summary
2.00	Dec 14, 2018	13	D1M1A Block Diagram: Added
		15	Ordering Information: D1M1A added
		19	Figure E.5 D1M1A (R7F701441) (Top View): Added
		22	Product Lineup: D1M1A added
		Section 1 Electrical Specifications	
		25	1.1.2.2, (2) Input: Description of SSTL_18 added
		27	Table 1.1 Pin Information for D1L1: GP(fast) added, PD register for JP0_4 pin changed
		28	Table 1.2 Pin Information for D1L2, D1L2H: GP(fast) added, PD register for JP0_4 pin changed
		29	Table 1.3 Pin Information for D1M1, D1M1H: GP(fast) added, PD register for JP0_4 pin changed
		30, 31	Table 1.4 Pin Information for D1M2, D1M2H: GP(fast) added, PD register for JP0_4 pin changed
		32	1.1.7 Pin Information for D1M1A: Added, PD register for JP0_4 pin changed
		37	1.4.2 Thermal Characteristics: Condition of T_{STGB} and T_{OPRT} changed by addtional line-up (D1M1A)
		38	Table 1.7 VCC / VDD Data: Line-up of REG1VCC changed
		46	1.5.3 Power-Up/-Down Ramp (RH850/D1M1A, D1M1(H), D1Lx): Line-up for section title changed
		46	Table 1.12 Power-up Restrictions: T_{pud4} added, MAX. value on T_{pudly} changed, Note 1 deleted
		46	Table 1.13 Power-down Restrictions: T_{pdd4} added, parameter on T_{pdd1} changed, MIN. value and unit on T_{pddio} changed
		47	Table 1.14 Power Supply Failure: Line-up for note changed, D1M1A added.
		48	Table 1.17 Power-down Restrictions: MIN. value and unit on T_{pdd4}, T_{pddio} and T_{pgdd} changed
		50	1.5.5 Power-Up/Down Sequences of External Supply Voltages (RH850/D1M1A, D1M1H-V2, D1Lx): Line-up for section title changed
		50	Figure 1.3 Power-up Sequence: Line-up of SDRAVCC changed
		51	Figure 1.4 Power-down Sequence: Line-up of SDRAVCC, and T_{pdd1} spec changed
		56	1.5.9 Core Voltage Supplies (RH850/D1M1A, D1M1(H)): Line-up for section title changed
		56	Figure 1.11 Voltage Supply D1M1A, D1M1(H)): Figure title changed by additional line-up (D1M1A)
		58	Table 1.20 VCC Data: Condition (Line-up) of REG1VCC and SDRAVCC, changed
		59	Table 1.21 Overload Current: Condition (Line-up) for “Pin supplied by A0VCC”, changed
		61	Table 1.22 CPU Clock Frequency: Line-up (D1M1A) of parameter, added
		61	Table 1.23 C_ISO_PCLK Modules Clock Frequency: Line-up (D1M1A) of parameter, added
		62	Table 1.26 XC Modules Clock Frequency: Line-up (D1M1A) of parameter, added
		64	Table 1.27 Main Oscillator Characteristics: Condition of I_{DDMOSC} added, symbol name of Note 1, Note 4 added
		65	Table 1.28 Sub Oscillator Characteristics: Note 1 added for T_{SOST}
		67	Table 1.31 PLL0 (D1M2(H), D1M1(H), D1Lx) Characteristics: • Table title changed (added line-up) • Symbol for PLL input frequency and PLL output frequency, added • MAX. value for PLL input frequency and PLL output frequency, corrected • Condition for PLL output period jitter and PLL output phase jitter, corrected
		67	Table 1.32 PLL1 (D1M2(H)) Characteristics: • Symbol for PLL input frequency and PLL output frequency, added • MAX. value for PLL input frequency, corrected
		67	Table 1.33 PLL1 (D1M1(H)/D1M1A/D1Lx), PLL2 Characteristics • Table title changed (added line-up) • Symbol for PLL input frequency and PLL output frequency, added • MAX. value for PLL input frequency, corrected
		67	Table 1.34 PLL0 (D1M1A) PLL0 Characteristics: Added

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2.00	Apr 14, 2017	68	Table 1.35 PLL0 SSCG Dithering Range for Each Settings: Added
		69	Table 1.36 Voltage Regulator: Condition (Line-up) for C_{REG}, changed
		72	1.6.1.3 HS Port Buffer: Condition (Line-up) changed
		72	Table 1.39 HS Output Buffer Characteristic: Condition for “Output frequency” amended, Note 4. added, and line-up added
		76	1.6.1.6 RSDS/OpenLDI Port Buffer: Section title changed, description of RSDS and LVDS added, condition changed
		76	Table 1.42 Differential LVDS Mode for RSDS (D1M2(H)): Table title changed
		76	Table 1.43 Differential LVDS Mode for OpenLDI (D1M1A): Added
		82	Table 1.51 HS Input Characteristic: Condition corrected
		83	Table 1.54 Input leakage Current for Each Power Domain: Domain of $I_{inLeakL}$ corrected (A0VCC added)
		83	Table 1.55 Input Leakage Current for SFVCC of P21_[9:0] (D1M1x/D1L2): Line-up for table title and domain, corrected
		91	Table 1.63 ADC Characteristic: Parameter (analog input pull-down resistance) corrected, and Note 2 added
		104	1.8.2.2 POC Characteristic on ISO (D1M1(H)/D1M1A/D1Lx): Line-up for section title changed
		129	Table 1.83 PCM-PWM Converter Characteristics: Symbol for “output time difference for each PWM outputs”, corrected
		137	Table 1.88 SFMA AC Characteristics (D1M2(H)/D1M1(H)/D1M1A/D1L2(H)): • Line-up for tabel title changed • Note 1 and Note 2 corrected, Note 4 added
		138	Table 1.89 SFMA AC Characteristics for P42 pin group (D1M1A): Added
		139	Figure 1.75 SFMA Wave Form: Corrected
		140	1.11.2 HyperBus/OctaBus Interface: Added
		141	Table 1.93 SDR-SDRAM AC Characteristics (D1M1H): MIN. value of t_{CK} corrected
		142	Table 1.94 SDR-SDRAM AC Characteristics (D1M1A): Added
		142	1.11.5 NAND Flash Interface: Added
		143	Table 1.96 Video Output AC Characteristics - LVTTL Mode (D1M2(H), D1M1(H)): • Line-up for table title changed • Parameter, symbol, condition, and unit for t_{DCLK}, corrected • Symbol and MIN. value for $DCLK_{duty}$, corrected • Parameter for t_{OV}, t_{OH}, t_{SOV}, t_{SOH} corrected
		143	Table 1.97 Video Output AC Characteristics (D1L2): • Symbol for “Pixel clock duty cycle” amended • Parameter of t_{ov}, amended
		143	Table 1.98 Video Output AC Characteristics - LVTTL Mode (D1M1A): Added
		144	Figure 1.79 Video Output AC Characteristics - VO-DDR: Added
		146	12.2.1.3 Video Output Interface (OpenLDI): Added
		148	Table 1.103 RAM Operation Mode AC Characteristics: Note 1 for t_{CYCr}, added
		161	1.14.5 Operation Current Consumption (RH850/D1M1A): Added
		163	Table 1.122 Stand-by Current: Condition of I_{A0VCC} corrected
		Section 2 Package	
		164	Table 2.1 Thermal resistance — Junction-to-ambient resistance: Added D1M1A
		141	Table 1.93 SDR-SDRAM AC Characteristics (D1M1H): MIN. value for t_{CK} changed
		167	Figure 2.3 176-pin Plastic QPF, 0.5 mm Pin-pitch with Exposed Pad: Note added
		168	2.2.4 D1M1H/D1M1A Devices (R7F701406/R7F701407/R7F701441): “D1M1A” added
2.10	Nov 30, 2017	Product Introduction	
		1	Product Introduction: Notice deleted
		3	RH850/D1L (2/2): Operating ambient temperature deleted
		4 to 6	RH850/D1M (1/3) to RH850/D1M (3/3): D1M1-V2 information added
		9	RH850/D1M (2/2): Operating ambient temperature deleted

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2.10	Nov 30, 2017	12	D1M1(H)/D1M1-V2 Block Diagram: “HYPB/OCTA” added into the Memory I/Fs, Note 4 added, figure title changed
		13	D1M1A Block Diagram: Modified (SDRB→SDRA, “PLL2” in the clock controller deleted)
		15	Ordering Information: Modified (RS-CAN→RS-CANFD (D1M2_3.75M, D1M2_5M), D1M1-V2 information added)
		18	Figure D.4 D1M1-V2 (R7F701442) (Top View): Added
		23	Product Lineup: RH850/D1M1-V2 information added
		Section 1 Electrical Specifications	
		25	1.1.2.1 Output Table Abbreviations, (2) IOHold: Description added
		28	Table 1.1 Pin Information for D1L1: Note 1 and Note 2 added
		29	Table 1.2 Pin Information for D1L2, D1L2H: Modified (P46→P45, Note 1 and Note 2 added)
		30	Table 1.3 Pin Information for D1M1, D1M1H: Note 1 to Note 3 added
		31, 32	Table 1.4 Pin Information for D1M2, D1M2H: Note 1 and Note 2 added
		33	1.1.7 Pin Information for D1M1A, D1M1-V2: Section title changed
		33	Table 1.5 Pin Information for D1M1A, D1M1-V2: Table title changed, Note 1 to Note 3 added
		38	1.4.2 Thermal Characteristics: T_{Jmin} value of “Storage temperature” changed, D1M1-V2 information added
		39	Table 1.7 VCC / VDD Data: Symbol (product name) of system changed
		47	1.5.3 Power-Up/-Down Ramp (RH850/D1M1A, D1M1(H), D1M1-V2, D1Lx): Section title changed
		47	Table 1.12 Power-up Restrictions: Parameter of T_{pgdu} changed, Power-up delay information changed
		49	Table 1.16 Power-up Restrictions: Power-up delay information changed
		49	Table 1.17 Power-down Restrictions: MIN. value modified
		51	1.5.5 Power-Up/Down Sequences of External Supply Voltages (RH850/D1M1A, D1M1(H), D1M1-V2, D1Lx): Section title changed
		51	Figure 1.3 Power-up Sequence: T_{pud3} end point change, rise timing and signal of “REG1VCC (3.3/5V)” changed
		52	Figure 1.4 Power-down Sequence: Signal modified (PLLVCC,REG1VCC (3.3/5V)→REG1VCC (3.3/5V))
		52	Figure 1.5 DeepSTOP Enter/Exit Sequence: Signal modified (PLLVCC,REG1VCC (3.3/5V)→REG1VCC (3.3/5V))
		57	1.5.9 Core Voltage Supplies (RH850/D1M1A, D1M1(H), D1M1-V2): Section title changed
		57	Figure 1.11 Voltage Supply D1M1A, D1M1(H), D1M1-V2: Figure title and Note 2 changed
		59	Table 1.20 VCC Data: Condition for REG1VCC changed
		60	Table 1.21 Overload Current: Condition for “Pin supplied by A0VCC” changed
		62	Table 1.22 CPU Clock Frequency: *1 (Note 1) for “D1M2(H), D1M1A” deleted, Parameter changed
		62	Table 1.23 C_ISO_PCLK Modules Clock Frequency: Parameter changed
		63	Table 1.26 XC Modules Clock Frequency: Parameter changed
		68	Table 1.33 PLL1 (D1M1(H)/D1M1A/D1M1-V2/D1Lx), PLL2 Characteristics: Table title changed
		68	Table 1.34 PLL0 (D1M1A/D1M1-V2) PLL0 Characteristics: Table title changed, value of MIN. and TYP. for “PLL frequency dithering range” modified
		70	Table 1.36 Voltage Regulator: Condition of C_{REG} changed
		73	Table 1.39 HS Output Buffer Characteristic: Condition for “Output frequency” and “Target impedance” changed, Note 4 modified
		77	Figure 1.18 Output Signaling of the RSDS/LVDS Buffer: Figure title changed
		92	Table 1.63 ADC Characteristic: Note 2 (*2) deleted
		114	Table 1.75 Slave Mode AC Characteristics: MIN. value of t_{SSIS}, t_{HSIS}, t_{SSSIS} and t_{HSSIS} modified
		126	Table 1.77 Slave Mode AC Characteristics: MIN. value of t_{SSIS}, t_{HSIS}, t_{SSSIS} and t_{HSSIS} modified

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2.10	Nov 30, 2017	138	Table 1.88 SFMA AC Characteristics (D1M2(H)/D1M1(H)/D1M1A/D1M1-V2/D1L2(H)): Table title changed, MAX. value of t_{CSS} modified, information for “Chip select signal output setup” added
		139	Table 1.89 SFMA AC Characteristics for P42 pin group (D1M1A/D1M1-V2): Table title changed, conditions of f_{CK} and t_{CK}, added, parameter modified, Note 1 and Note 2 modified, Note 4 deleted
		139	Figure 1.75 SFMA Wave Form: Arrow for t_{ODS} changed, CS timing added
		140	Table 1.91 HYPB/OCTA AC Characteristics (D1M1A/D1M1-V2): Table title changed, conditions of f_{CK} and t_{CK}, added, MAXl. value of t_{CSS} modified
		140	Figure 1.76 HYPB/OCTA Waveforms: “t_{CSS}” for CS timing added
		143	Table 1.96 Video Output AC Characteristics - LVTTL Mode (D1M2(H), D1M1(H), D1M1-V2): Table title changed, condition for “Pixel clock frequency (DCLK)” modified
		146	Table 1.100 OpenLDI Interface AC Characteristics: Table titile modified, unit of t_{CYC}, RCHP/RCLP, t_{RIP0} to t_{RIP6} and t_{SKM} modified
		162	11.14.6 Operation Current Consumption (RH850/D1M1-V2): Added
		165	Table 2.1 Thermal resistance – Junction-to-ambient resistance: D1M1-V2 information added
		167	2.2.2 D1L2H/D1M1-V2 Devices (R7F701442): Section title changed
2.20	Dec 14, 2018	Product Introduction	
		4	RH850/D1M (1/3): Mode of “Serial Flash Memory I/F 1 (SFMA1)” modified
		Section 1 Electrical Specifications	
		38	1.4.2 Thermal Characteristics (Table 1.7 Thermal Characteristics): Table number and title added
		46	1.5.1 Requirements for External Power Supply Connections: Description modified
		47	Table 1.13 Power-up Restrictions: Parameter of T_{pudio}, modified
		47	Table 1.13 Power-up Restrictions: MIN. value of T_{pctl}, modified
		47	Table 1.14 Power-down Restrictions: Parameter of T_{pddio}, modified
		49	Table 1.17 Power-up Restrictions: Parameter of T_{pudio}, modified
		49	Table 1.17 Power-up Restrictions: MIN. value of T_{pctl}, modified
		49	Table 1.18 Power-down Restrictions: Parameter of T_{pddio}, modified
		55	Figure 1.9 Power-down Sequence: Modified (IOVCC → BnVCC/ISMVCC/SFVCC/RVCC/MVCC)
		59	Table 1.13 VCC Data: Note 6 modified
		87	Table 1.60 Interrupt AC Characteristics: Spec. of t_{ITH} modified
		87	Table 1.60 Interrupt AC Characteristics: Spec. of t_{ITL} modified
		87	Table 1.60 Interrupt AC Characteristics: Note 5 added
		95	1.8.1.2 External Circuit on ADC Inputs: Calculation formula modified
		135	1.10.12.1 NEXUS Interface (Table 1.89 NEXUS Interface): Table title and number, added
		136	1.10.12.2 LPD 4pin Interface (Table 1.90 LPD 4pin Interface): Table title and number, added
		137	1.10.12.3 LPD 1pin Interface (Table 1.91 LPD 1pin Interface): Table title and number, added
		137	1.10.12.4 Trace Interface (Table 1.92 Trace Interface): Table title and number, added
		139	Figure 1.75 SFMA Wave Form: Modified
		142	Table 1.94 SDR-SDRAM AC Characteristics (D1M1A): MAX. value of t_{Ad}, modified
		147	Table 1.106 Video Input AC Characteristics: Spec. of t_{CKI} modified
		155	Table 1.111 Basic Characteristics: MIN. value of f_{PCLK}, modified
		155	Table 1.111 Basic Characteristics: Parameter of V_{dd}, modified
		156	Table 1.113 Basic Characteristics: MIN. value of f_{PCLK}, modified
		156	Table 1.113 Basic Characteristics: Parameter of V_{dd}, modified

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2.20	Dec 14, 2018	Section 2 Package	
		167	Figure 2.2 176-pin Plastic QPF, 0.5 mm Pin-pitch: Modified
		169	Figure 2.4 272-pin Plastic BGA, 1.0 mm Ball-pitch, 19 × 19 mm^2 Size: Index data added

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Renesas Electronics Corporation
TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852 2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338

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