RH850/F1H PREMIUM (100 pin Version)

RENESAS MCU

R01DS0275EJ0100
Rev.1.00
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Product Introduction

Concept

The RH850/F1x microcontroller focus on low power and low cost for the body application.

The device is a high-end microcontroller with a 32-bit RH850G3M core for car body control. The features of this device are the low power consumption, the high processing power and the variable peripheral function.

In particular, Low power consumption is achieved by supporting wide stand-by control and the power supply insulation using the port polling, stand-by control of AD conversion and LIN communication which considered body control application.

This device supports the security and safety function. And the local area network has been strengthened by upgrading each module of CAN, LIN master/slave.

Function overview

Refer to *the RH850/F1H PREMIUM 100 pin Version User's manual: Hardware*.

Block diagram

Refer to *the RH850/F1H PREMIUM 100 pin Version User's manual: Hardware*.

Pin map

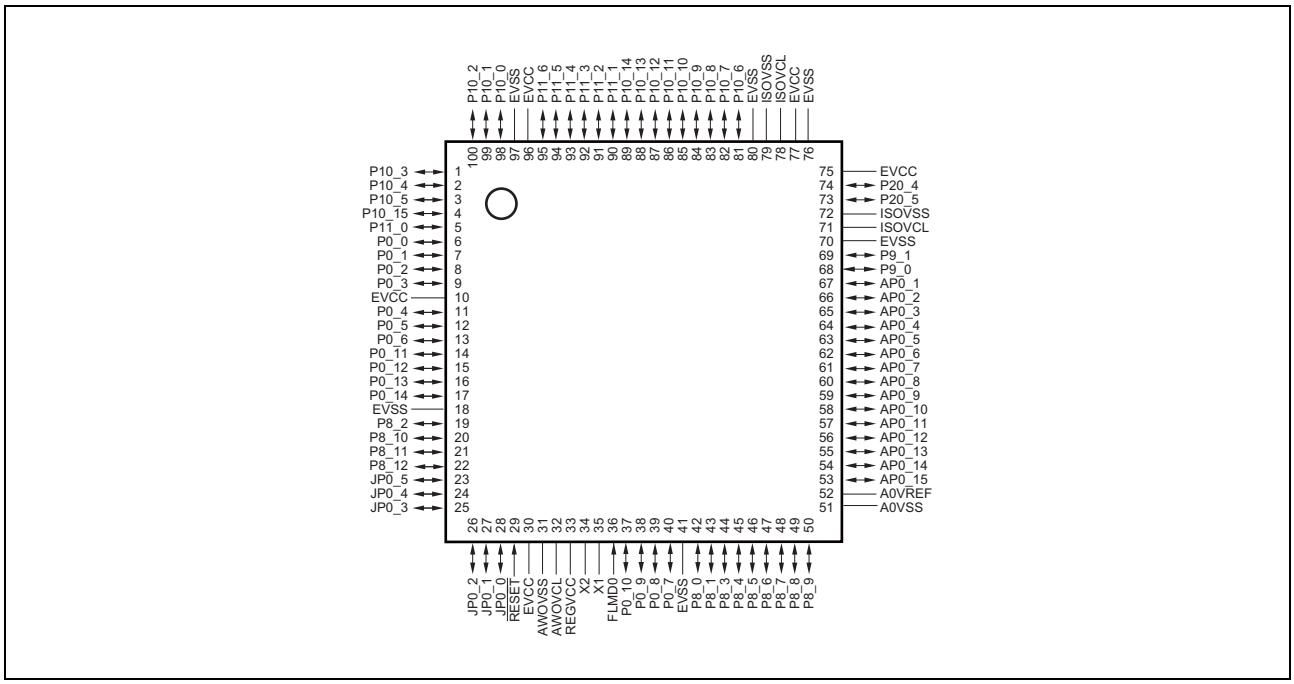


Figure 1.1 Pin Connection Diagram (100 pin QLFP)

Product Lineup

Pin Count	Memory						Product Name		Line Name
	Code Flash	CPU1 (Core #1)	CPU2 (Core #2)	Global Memory			Operating Temperature(Ta)		
		Local RAM	Local RAM	Data Flash	Global RAM	Retention RAM (RRAM)	–40°C to +105°C Caution	-40°C to +125°C Caution	
100 pin	3 MB	256 KB	128 KB	64 KB	64 KB	64 KB	R7F7015303AFP	Not provided	PREMIUM
	4 MB	256 KB	128 KB	64 KB	64 KB	64 KB	R7F7015313AFP	Not provided	

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj (**Section 1.2.4, Temperature Condition**) and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

Section 1 Electrical Specifications (Preliminary)

1.1 Overview

The electrical spec of this device is guaranteed by the following operational condition. But, this condition is different depends on each characteristics, so refer to each chapter for more detail.

1.1.1 Pin Groups

1.1.1.1 100 pin

Symbol	Pin Group Supplied by	Related Pins/Ports
Pg R	REGVCC, AWOVSS	X1, X2
Pg E	EVCC, EVSS	Related ports: JP0, P0, P8, P9, P10, P11, P20 Related pins: RESET, FLMD0
Pg A0	A0VREF, A0VSS	Related port: AP0

1.1.2 General Measurement Conditions

1.1.2.1 Common Conditions

Power supply

- REGVCC = EVCC = VPOC*1 to 5.5 V
- A0VREF = 3.0 V to 5.5 V
- AWOVSS = ISOVSS = EVSS = A0VSS = 0 V

Capacitance on internal regulator

- CAWOVCL: 0.1 µF +/– 30%
- CISOVCL: 0.1 µF +/– 30% per pin
- Operating temperature
  Ta:
  –40 to 105 °C
  Tj:
  –40 to 130°C

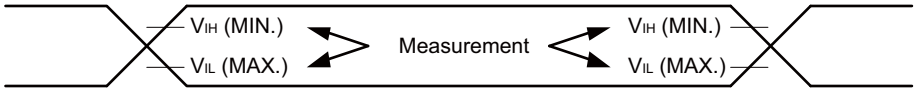
Load conditions

- CL = 30 pF

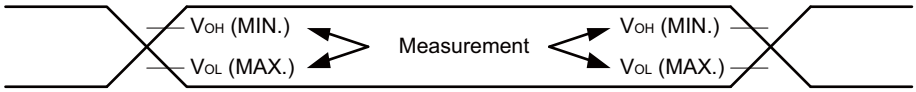
Note 1. “VPOC” means POC (power on clear) detection voltage. For more detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

1.1.2.2 AC Characteristic Measurement Condition

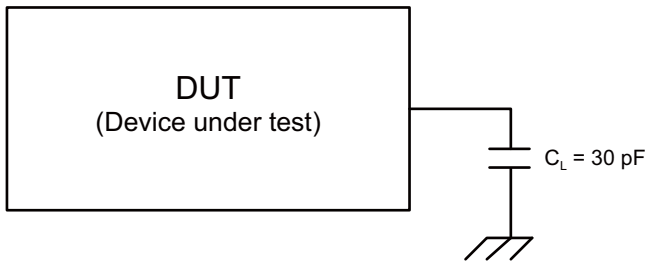
AC test input measurement points



AC test output measurement points



Load conditions



CAUTION

If the load capacitance exceeds 30 pF due to the circuit configuration, it is recommended to insert a buffer in order to reduce capacitance till less than 30 pF.

1.2 Absolute Maximum Ratings

CAUTIONS

1. **Do not directly connect the output (or input/output) pins to each other, power supply and ground.**
2. **Even momentarily exceeding the absolute maximum rating for just one item creates a threat of failure in the reliability of the products. That is, the absolute maximum ratings are the levels that raise a threat of physical damage to the products. Be sure to use the products only under conditions that do not exceed the ratings. The quality and normal operation of the product are guaranteed under the standards and conditions given as DC and AC characteristics.**
3. **When designing an external circuit ensure that the connections do not conflict with the port state of this device.**

1.2.1 Supply Voltages

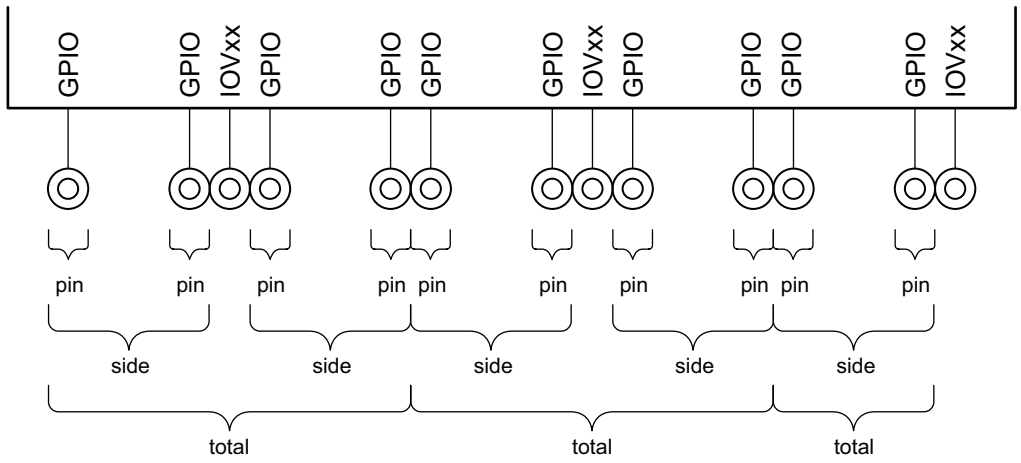
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
System supply voltage	REGVCC		–0.5		6.5	V
	AWOVSS		–0.5		0.5	V
	ISOVSS		–0.5		0.5	V
Port supply voltage	EVCC		–0.5		6.5	V
	EVSS		–0.5		0.5	V
A/D-converter supply voltage	A0VREF		–0.5		6.5	V
	A0VSS		–0.5		0.5	V

1.2.2 Port Voltages

Item	Pin Group*1	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	PgR	VI		–0.5		REGVCC + 0.5 (Do not exceed 6.5 V)	V
	PgE			–0.5		EVCC + 0.5 (Do not exceed 6.5 V)	V
	PgA0			–0.5		A0VREF + 0.5 (Do not exceed 6.5 V)	V

Note 1. The characteristics of the alternative-function pins are the same as those of the port pins unless otherwise specified.

1.2.3 Port Current



Definition of the condition

- **Per pin:** Output current of one GPIO
- **Per side:** Total output current of all GPIO pins on one side of one IOVxx
- **Total:** Total output current of both sides of one IOVxx

Note:

- **GPIO:** General-purpose I/O pin (JP0, P0, P8, P9, P10, P11, P20, AP0)
- **IOVxx:** Power supply pin for I/O pins (EVCC/EVSS, A0VREF/A0VSS)

1.2.3.1 100 pin

Table 1.1 Port Current (100 pin)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level output current	IOH	PgE	Per pin			–10	mA
			Per side (total of P9_0, P9_1)			–48	mA
			Per side (total of P20_4, P20_5)			–48	mA
			Per side (total of P0_0 to P0_3)			–40	mA
			Per side (total of JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12)			–48	mA
			Per side (total of JP0_0 to JP0_2)			–48	mA
			Per side (total of P0_7 to P0_10, P8_0, P8_1, P8_3 to P8_7)			–48	mA
			Per side (total of P8_8, P8_9)			–48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_6)			–48	mA
			Per side (total of P10_0 to P10_2)			–30	mA
			Per side (total of P10_3 to P10_5)			–30	mA
			Per side (total of P10_15, P11_0)			–48	mA
			Total (EVCC)			–60	mA
High level output current	IOH	PgA0	Per pin			–10	mA
			Total (A0VREF)			–48	mA
Low level output current	IOL	PgE	Per pin			10	mA
			Per side (total of P9_0, P9_1)			48	mA
			Per side (total of P20_4, P20_5)			48	mA
			Per side (total of P0_0 to P0_6, P0_11 to P0_14)			48	mA
			Per side (total of JP0_0 to JP0_5)			48	mA
			Per side (total of P8_0, P8_1, P8_3 to P8_7)			48	mA
			Per side (total of P8_8, P8_9)			48	mA
			Per side (total of P10_6 to P10_14, P11_1 to P11_2)			48	mA
			Per side (total of P11_3 to P11_6)			48	mA
			Per side (total of P10_0 to P10_2)			30	mA
			Per side (total of P10_3 to P10_5)			30	mA
			Per side (total of P10_15, P11_0)			48	mA
			Total (EVCC)			60	mA
Low level output current	IOL	PgA0	Per pin			10	mA
			Total (A0VREF)			48	mA

1.2.4 Temperature Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Storage temperature	Tstg		–55		170	°C
Junction temperature	Tj		–40		130	°C

1.3 Capacitance

Condition: REGVCC = EVCC = A0VREF = AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, Ta = 25°C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input capacitance	CI*1	f = 1 MHz 0 V for non measurement pins			10	pF
Input/Output capacitance	CIO*2				10	pF

Note 1. CI: Capacitance between the input pin and ground

Note 2. CIO: Capacitance between the input/output pin and ground

1.4 Operational Condition

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
CPU clock frequency	f_{CPUCLK}	for CPU1 PLL mode (Fixed frequency mode) SSCG mode (Dithered frequency mode)			120	MHz
		for CPU2				
Peripheral clock frequency	f_{CKSCLK_AWDTA}	for WDTA0			240*2	kHz
	f_{CKSCLK_ATAUJ}	for TAUJ0			40	MHz
	f_{CKSCLK_AADCA}	for ADCA0			40	MHz
	f_{CKSCLK_IPERI1}	for TAUD0			80	MHz
		for TAUJ1				
	f_{CKSCLK_IPERI2}	for TAUB0			60	MHz
		for PWM-diag				
	f_{CKSCLK_ILIN}	for RLIN2n			60	MHz
		for RLIN3n				
	f_{CKSCLK_ICAN}	for RS-CANn (pclk)			80	MHz
	$f_{CKSCLK\_ICANOSC}$	for RS-CANn (clk_xincan)			24	MHz
	f_{CKSCLK_ICSI}	for CSIG0			80	MHz
		for CSIHn				
	f_{RL}	for WDTA1			240*2	kHz
		for WDTA2				
	$f_{CPUCLK2}$	for OSTMn			60	MHz
	$f_{PPLLCLK}$				80	MHz
	$f_{CPUCLK4}$	for RIIC			30	MHz
	f_{EMCLK}	for LPS			8	MHz
Power supply range	REGVCC	REGVCC = EVCC	VPOC*3		5.5	V
	EVCC					
	A0VREF		3.0		5.5	V

Note 1. For clock specification of peripherals, refer to *Section 11, Clock Controller*, in the *RH850/F1H PREMIUM 100 pin Version User's Manual: Hardware*.

Note 2. This frequency depends on the internal oscillator (LS IntOSC).

Note 3. "VPOC" means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on). For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**. In addition, the guaranteed operation in DC characteristic. And AC characteristic is guaranteed when more than 3.0 V. When the power supply voltage is VPOC to 3.0 V, the device does not malfunction.

1.5 Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %, CISOVCL: 0.1 µF +/– 30 %,
Ta = –40 to 105 °C

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
MainOSC frequency	f_{MOSC}	Crystal/Ceramic	8		24	MHz
MainOSC Current consumption	I_{MOSC}	Crystal/Ceramic After stabilization		1.9*2	2.3*2	mA
MainOSC oscillation start point	V_{MOSCSP}	Crystal/Ceramic	VPOC			V
MainOSC oscillation operating point	V_{MOSCOP}	Crystal/Ceramic		0.5xREGVCC*2		V
MainOSC oscillation amplitude	$V_{MOSCAMP}$	Crystal/Ceramic	0.4xREGVCC–0.2*2			V
MainOSC oscillation stabilization time	t_{MSTB}	Crystal/Ceramic		*1		ms

Note 1. Oscillator stabilization time is time until being set (“1”) in MOSCS.MOSCCLKACT bit after MOSCE.MOSCENTRG bit is written “1”, and depends on the setting value of MOSCST register and EMCLK (8 MHz/240 kHz). Please decide appropriate oscillation stabilization time by matching test with resonator and oscillation circuit.

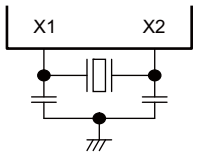
Note 2. This is reference value.

CAUTION

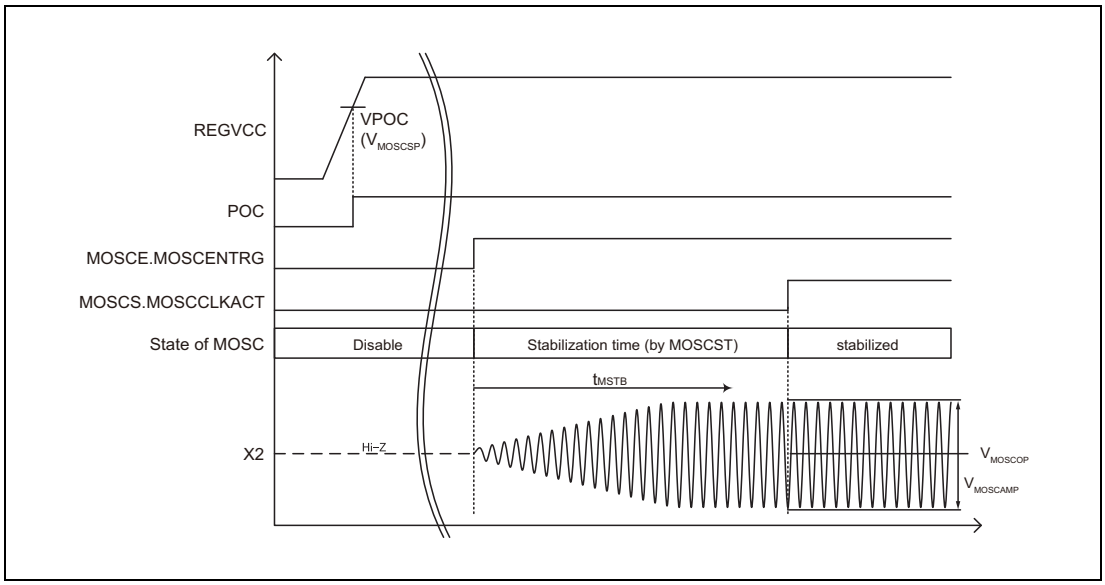
The oscillation stabilization time differs according the matching with the external resonator circuit. It is recommended to determine the oscillation stabilization time by an oscillator matching test.

NOTE

Recommended oscillator circuit is shown below.



MainOSC



1.6 Internal Oscillator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105 °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LS IntOSC frequency	f_{RL}		220.8	240	259.2	kHz
HS IntOSC frequency	f_{RH}		7.36	8	8.64	MHz
		Ta = 25°C	7.6	8	8.4	MHz
HS IntOSC Current consumption	I_{RH}	After stabilization			25*1	µA
HS IntOSC oscillation stabilization time	t_{RHSTB}				54.4	µs

Note 1. This is reference value.

1.7 PLL Characteristics

1.7.1 PLL0 (for CPU) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105 °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input frequency	$f_{SSCGICLK}$			8		24	MHz
Output frequency	f_{SSCGP}	PLL mode		25		120	MHz
	f_{SSCGS}	SSCG mode		25		120	MHz
Modulation frequency	f_{MOD}			20		100	kHz
Frequency dithering range*4	f_{DIT}			±0.82	±1.0	±1.18	%
				±1.64	±2.0	±2.36	%
				±2.46	±3.0	±3.54	%
				±3.28	±4.0	±4.72	%
				±4.1	±5.0	±5.9	%
Output period jitter*1	t_{CPJS}	pr = 4*2		–150		150	ps
		pr = 8*2		–200		200	ps
		pr = 16*2		–300		300	ps
Lock time*3	t_{LCKSP}	PLL mode	PLL0ST = 0000 $0AA0_H$	314.9	340	369.6	µs
	t_{LCKS}	SSCG mode	PLL0ST = 0000 $1B80_H$	814.9	880	956.6	µs

Note 1. This is reference value.

Note 2. The following parameters are set by PLL0C register.
- pr: PLL0C.PLL0P2-0 bits

Note 3. Lock time is time until being set (“1”) in PLL0S.PLL0CLKACT bit after PLL0E.PLL0ENTRG bit is written “1”.

Note 4. “Frequency dithering range” is set by PLL0ADJ[2:0] bits of PLL0C registers.

1.7.2 PLL1 (for Peripheral) Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105 °C, CL = 30 pF

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Input frequency	$f_{PLLICLK}$			8		24	MHz
Output frequency	f_{PLL}			25		80	MHz
Output period jitter*1	t_{CPJP}	PLL1C.OUTBSEL = 0	par = 4*2	–150		150	ps
			par = 6*2 [($f_{PLLICLK}$ / mr × nr) = 480 MHz]	–150		150	ps
			par = 6*2 [($f_{PLLICLK}$ / mr × nr) < 480 MHz]	–200		200	ps
			par = 8*2	–250		250	ps
			par = 16*2	–300		300	ps
		PLL1C.OUTBSEL = 1	($f_{PLLICLK}$ / mr × nr) = 480 MHz	–150		150	ps
			($f_{PLLICLK}$ / mr × nr) < 480 MHz	–200		200	ps
Long term jitter*1	t_{LTJ}		term = 1 µs	–500		500	ps
			term = 10 µs	–1		1	ns
			term = 20 µs	–2		2	ns
Lock time*3	t_{LCKP}			104.0	112.3	122.1	µs

Note 1. This is reference value.

Note 2. The following parameters are set by PLL1C register.
- par: PLL1C.PA2-0 bits
- mr: PLL1C.M1-0 bits
- nr: PLL1C.N5-0 bits

Note 3. Lock time is time until being set (“1”) in PLL1S.PLL1CLKACT bit after PLL1E.PLL1ENTRG bit is written “1”.

1.8 Power Management Characteristics

1.8.1 Regulator Characteristics

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, Ta = –40 to 105 °C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Input voltage	REGVCC		VPOC*1		5.5	V
Normal operation voltage	V_{OP}	AWOVCL pin, ISOVCL pin	1.10	1.25	1.35	V
Limited operation voltage	V_{LOP}	AWOVCL pin, ISOVCL pin	1.35		1.43*3	V
Regulator output voltage	V_{RO}	AWOVCL pin, ISOVCL pin	1.15	1.25	1.35	V
Capacitance	CAWOVCL	AWOVCL pin	0.07	0.1	0.13	µF
	CISOVCL	ISOVCL pin	0.07	0.1	0.13	µF
Equivalent series resistance for load capacitance	RVRAWO	for CAWOVCL			40*2	mΩ
	RVRISO	for CISOVCL			40*2	mΩ
Inrush current during power-on					200*2	mA

Note 1. “VPOC” means POC (power on clear) detection voltage (typ. 2.95 V@at power-on, typ. 2.9 V@after (except) power-on).
For detail, refer to **Section 1.8.2, Voltage Detector (POC, LVI, VLVI, CVM) Characteristics**.

Note 2. This is reference value.

Note 3. Reliability restrictions from 1.35 V to 1.43 V.

1.8.2 Voltage Detector (POC, LVI, VLVI, CVM) Characteristics

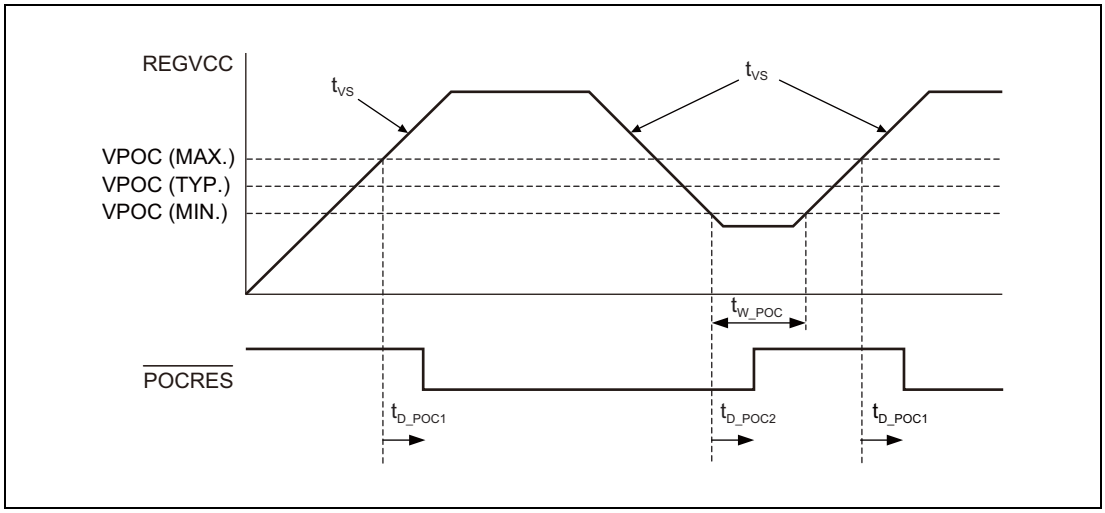
Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105 °C, CL = 30 pF

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Detection voltage (REGVCC)	VPOC	POC	At power-on (Rise)		2.8	2.95	3.1	V
			After power-on (Fall)		2.8	2.9	3.0	V
	VLVI0	LVI	Rise		3.87	4.0	4.13	V
			Fall		3.9	4.0	4.1	V
	VLVI1		Rise		3.57	3.7	3.83	V
			Fall		3.6	3.7	3.8	V
	VLVI2		Rise		3.37	3.5	3.63	V
			Fall		3.4	3.5	3.6	V
	VVLVI	VLVI			1.8	1.9	2.0	V
Detection voltage (AWOVCL, ISOVCL)	VCVMH	CVM	High voltage		1.40	1.50	1.60	V
	VCVML*8		Low voltage		1.1	1.15	1.20	V
Response time	t_{D_POC1}*6	POC	At power-on (Rise)	*1			2	ms
				*2			6.3	ms
			After power-on (Rise)	*3			2	ms
				*4			5	ms
	t_{D_POC2}*7		After power-on (Fall)	*5			5	µs
	t_{D_LVI}	LVI					2	ms
	t_{D_VLVI}	VLVI		*3			2	ms
				*4			5	ms
	t_{D_CVM}	CVM			0.2		10	µs
Setup time	t_{S_LVI}	LVI	LVICNT0,1 bits are set to 1 (except 00_B), then LVI is ready to operate				80	µs
REGVCC minimum width	t_{W_POC}	POC			0.2			ms
	t_{W_LVI}	LVI			0.2			ms
	t_{W_VLVI}	VLVI			0.2			ms

Note 1. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms
Note 2. Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms
Note 3. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 20 V/ms
Note 4. Voltage slope (t_{VS}): 20 V/ms < t_{VS} ≤ 500 V/ms
Note 5. Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 500 V/ms
Note 6. t_{D_POC1} is the time from detection voltage to release of reset signal.
Note 7. t_{D_POC2} is the time from detection voltage to occurrence of reset signal.
Note 8. The CVM monitors the internal voltage regulator output to ensure that AWOVCL/ISOVCL is upper than specified minimum level.

Caution: A detection of the voltage AWOVCL or ISOVCL outside the specified level of VCVMH and VCVML is not ensured by CVM.

<POC>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VPOC (TYP.)
VPOC (MIN.)
tW_POC
POCRES
tD_POC1
tD_POC2
tD_POC1

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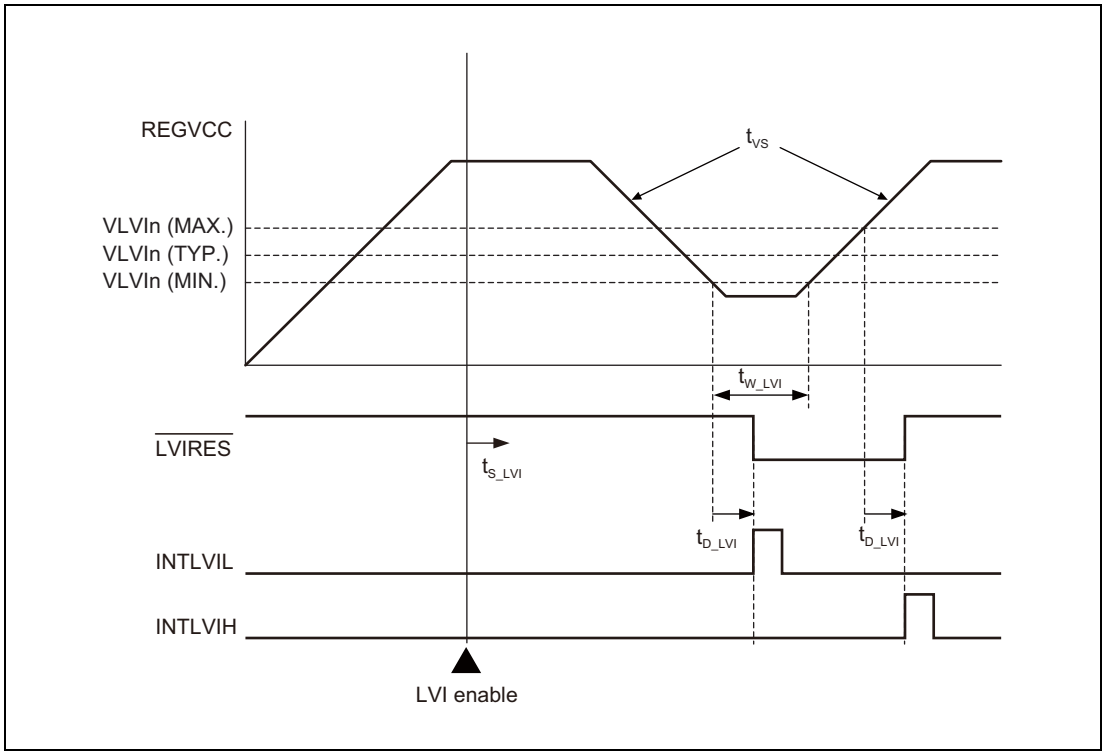
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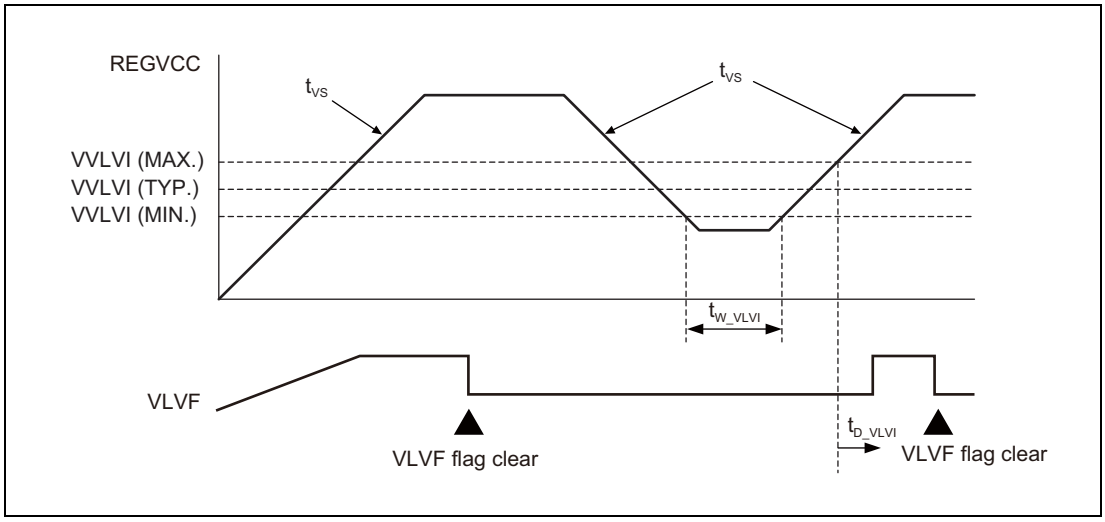
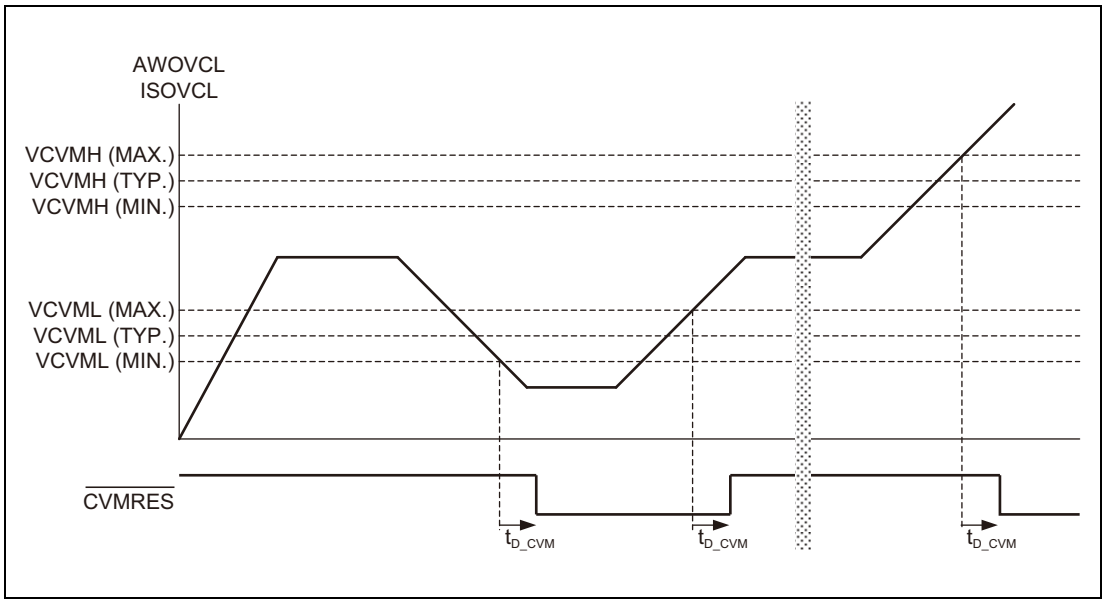
VLVIn (MIN.)
tW_LVI
LVIRES
tS_LVI
tD_LVI
tD_LVI
INTLVIL
INTLVIH
LVI enable

<VLVI>


REGVCC
t_{VS}
t_{VS}
VVLVI (MAX.)
VVLVI (TYP.)
VVLVI (MIN.)
t_{W_VLVI}
VLVF
VLVF flag clear
t_{D_VLVI}
VLVF flag clear

<CVM>

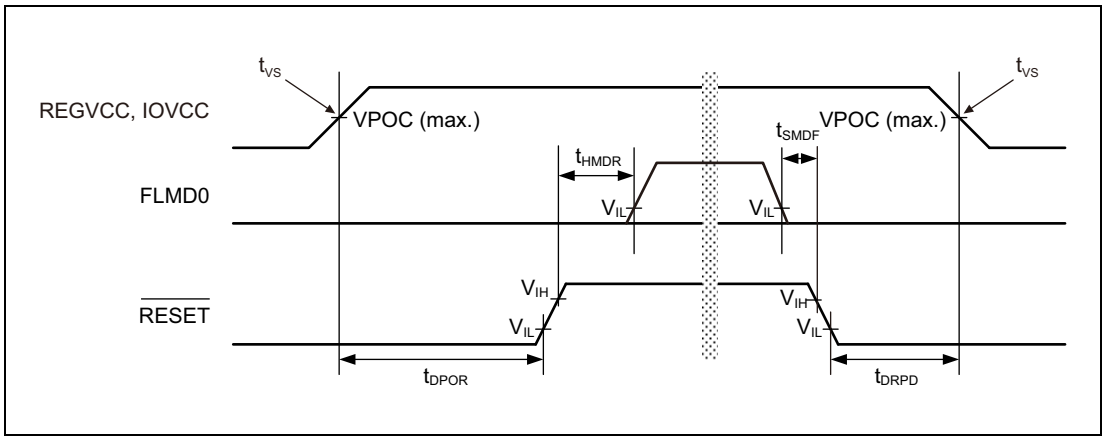

AWOVCL
ISOVCL
VCVMH (MAX.)
VCVMH (TYP.)
VCVMH (MIN.)
VCVML (MAX.)
VCVML (TYP.)
VCVML (MIN.)
$\overline{CVMRES}$
t_{D_CVM}
t_{D_CVM}
t_{D_CVM}

1.8.3 Power Up/Down Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105 °C, CL = 30 pF

Table 1.2 In case the $\overline{\text{RESET}}$ pin is used (except Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 hold time (vs $\overline{\text{RESET}}$ ↑)	t_{HMDR}		1			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↓)	t_{SMDF}		0*2			µs
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC and A0VREF.

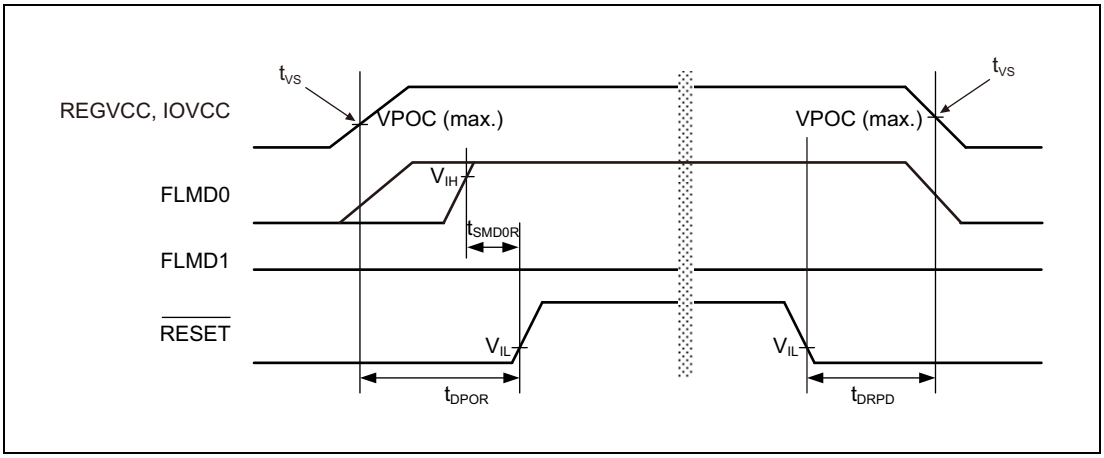
Note 2. When the $\overline{\text{RESET}}$ and FLMD0 pin input low level at same time (t_{SMDF} = 0µs) in the device entries on-chip debug mode and operates self-programming, following pins have a possibility to unstable level output for less than 23ns.

P10_0, P0_0, P10_5, P8_1

So, when the device was used in the device entries on-chip debug mode and operates self-programming, please input low level in FLMD0 before $\overline{\text{RESET}}$ pin input.

Table 1.3 In case the $\overline{\text{RESET}}$ pin is used (for Serial programming mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*1 ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGVCC ↓ and IOVCC*1 ↓ delay time	t_{DRPD}		0			ms



Note 1. IOVCC means EVCC and A0VREF.

Table 1.4 Boundary scan mode in case of using $\overline{\text{RESET}}$ pin

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*1)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC ↑ to $\overline{\text{RESET}}$ ↑ delay time	t_{DPOR}	Voltage slope (t_{VS}):0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0, FLMD1, MODE0, MODE1 setup time (vs $\overline{\text{RESET}}$ ↑)	t_{SMD0R}		1			ms
$\overline{\text{RESET}}$ ↓ to REGCC ↓ and IOVCC ↓ delay time	t_{DRPD}		0			ms
$\overline{\text{DCUTRST}}$ input delay time (vs $\overline{\text{RESET}}$ ↑)	t_{DRTRST}		1			ms
$\overline{\text{RESET}}$ hold time (vs $\overline{\text{DCUTRST}}$ ↓)	t_{HRTRST}		0			ms

Note 1. IOVCC means EVCC and A0VREF.

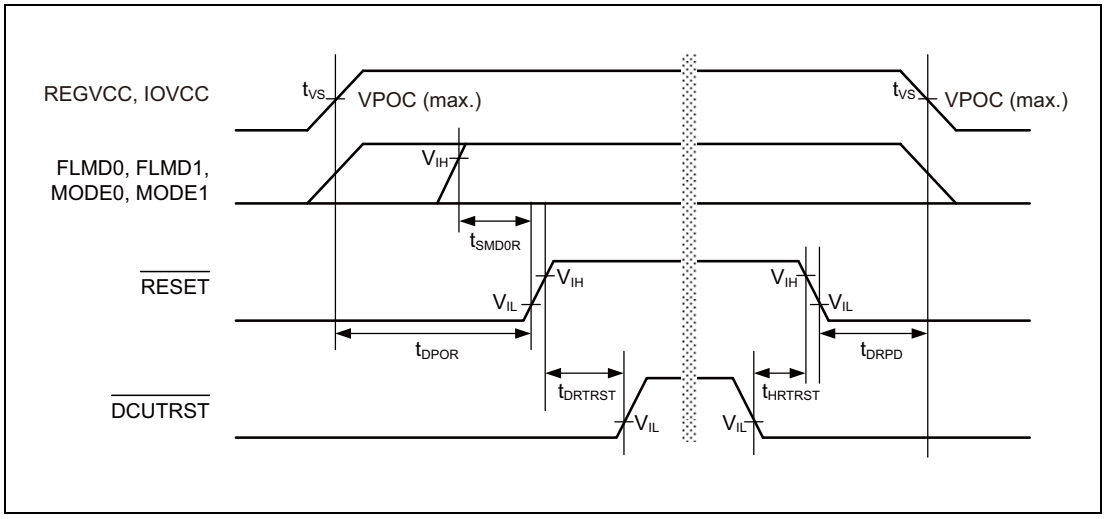
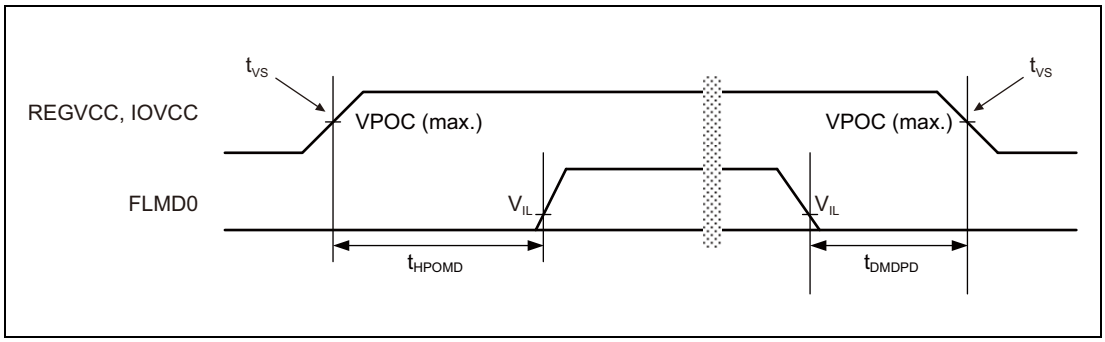


Table 1.5 In case the $\overline{\text{RESET}}$ pin is not used and fixed to high level by pull-up*1

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Voltage slope (REGVCC and IOVCC*2)	t_{VS}		0.02 (= 50 ms/V)		500 (= 2 µs/V)	V/ms
REGVCC ↑ and IOVCC*2 ↑ to FLMD0 hold time	t_{HPOMD}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms	2			ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms	6.3			ms
FLMD0 ↓ to REGVCC ↓ and IOVCC*2 ↓ delay time	t_{DMDPD}		1			µs

Note 1. This operating condition is available only in normal operation mode (include self-programming mode). When the device is used in except single chip mode, please use the $\overline{\text{RESET}}$ pin.

Note 2. IOVCC means EVCC and A0VREF.



1.8.4 CPU Reset Release Timing

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1µF +/– 30 %, CISOVCL: 0.1µF +/–30 %,
Ta = –40 to 105 °C, CL = 30 pF

Table 1.6 In case the $\overline{\text{RESET}}$ pin is not used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
REGVCC ↑ to CPU reset release*1	t_{DPCRR}	Voltage slope (t_{VS}): 0.02 V/ms ≤ t_{VS} ≤ 0.5 V/ms			2.58	ms
		Voltage slope (t_{VS}): 0.5 V/ms < t_{VS} ≤ 500 V/ms			8.38	ms

Note 1. This is reference value.

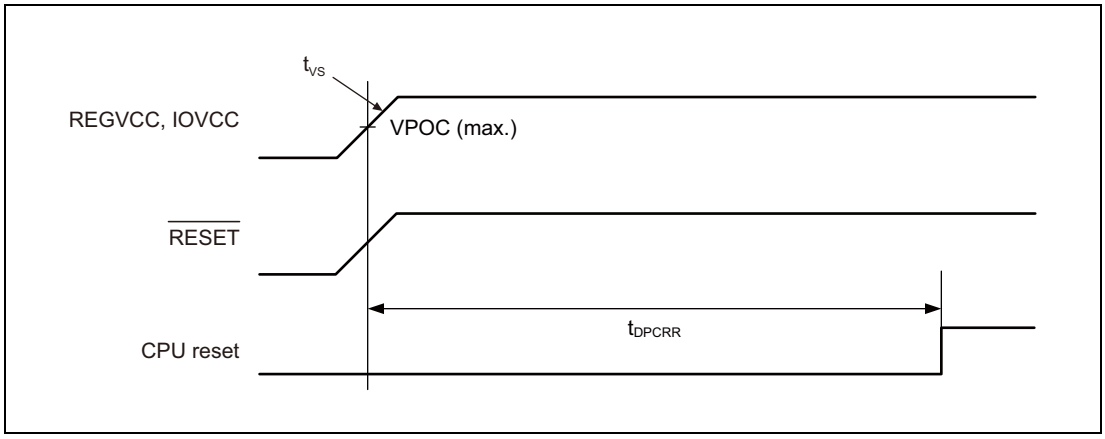
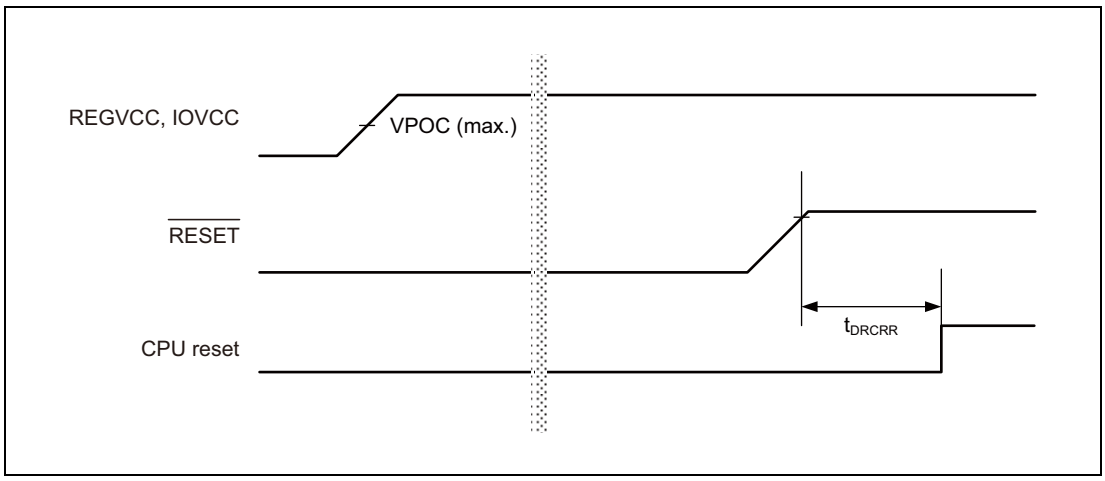


Table 1.7 In case the $\overline{\text{RESET}}$ pin is used

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ ↑ to CPU reset release*1	t_{DRCRR}				14*2	µs

Note 1. This is reference value.

Note 2. At least t_{DPCRR} time is necessary reaching from VPOC (max) even if power up sequence is kept shown on **Section 1.8.3, Power Up/Down Timing**.



1.9 Pin Characteristics

Condition: Some of the conditions mentioned in this chapter can be selected by software and described in the hardware user's manual.

(1/2)

Pin Name	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
$\overline{\text{RESET}}$	—	—	√	—	—	—	—	—	—[*4]
FLMD0	—	√	—	—	—	—	—	√	√
JP0_0	—	—	—	√	√	—	Slow	√	√
JP0_1	—	—	—	√	—	—	Slow/Fast	√	√
JP0_2	—	—	—	√	√	—	Slow	√	√
JP0_3	—	—	—	√	√	—	Slow	√	√
JP0_4	—	—	—	√	√	—	Slow	√	√
JP0_5	—	—	—	√	—	—	Slow/Fast	√	√
P0_0	—	√	—	√	—	—	Slow	√	√
P0_1	—	√	—	√	—	—	Slow	√	√
P0_2	—	√	—	√	—	—	Slow/Fast[*2]	√	√
P0_3	—	√	—	√	—	—	Slow/Fast[*2]	√	√
P0_4	—	√	—	√	—	—	Slow	√	√
P0_5	—	√	—	√	—	—	Slow/Fast[*3]	√	√
P0_6	—	√[*1]	—	√	—	—	Slow/Fast[*3]	√	√
P0_7	—	√	—	√	—	—	Slow/Fast	√	√
P0_8	—	—	—	√	—	—	Slow	√	√
P0_9	—	√	—	√	—	—	Slow	√	√
P0_10	—	—	—	√	—	—	Slow	√	√
P0_11	—	√	—	√	—	—	Slow	√	√
P0_12	—	√	—	√	—	—	Slow	√	√
P0_13	—	√	—	√	—	—	Slow/Fast	√	—
P0_14	—	—	—	√	—	—	Slow/Fast	√	—
P8_0	—	—	—	√	—	—	Slow	√	√
P8_1	—	—	—	√	—	—	Slow	√	√
P8_2	—	—	—	√	—	—	Slow	√	√
P8_3	—	—	—	√	—	—	Slow	√	√
P8_4	—	—	—	√	—	—	Slow	√	√
P8_5	—	—	—	√	—	—	Slow	√	√
P8_6	—	—	—	√	—	—	Slow	√	√
P8_7	—	—	—	√	—	—	Slow	√	—
P8_8	—	—	—	√	—	—	Slow	√	—
P8_9	—	—	—	√	—	—	Slow	√	—
P8_10	—	—	—	√	—	—	Slow	√	—
P8_11	—	—	—	√	—	—	Slow	√	—
P8_12	—	—	—	√	—	—	Slow	√	—
P20_4	—	√	—	√	—	—	Slow	√	—
P20_5	—	—	—	√	—	—	Slow	√	—
P9_0	—	—	—	√	—	—	Slow	√	—
P9_1	—	—	—	√	—	—	Slow	√	—
P10_0	—	√	—	√	√	—	Slow/Fast	√	√
P10_1	—	—	—	√	√	—	Slow/Fast[*3]	√	√
P10_2	—	√	—	√	√	—	Slow/Fast[*3]	√	√
P10_3	—	√	—	√	—	—	Slow/Fast	√	√
P10_4	—	√	—	√	√	—	Slow/Fast	√	√
P10_5	—	—	—	√	√	—	Slow/Fast	√	√

(2/2)

Pin Name	Port Input Buffer Function						Port Output Drive Strength Mode	Other Port Function	
	CMOS	SHMT1	SHMT2	SHMT4	TTL	Analog		Pull-up	Pull-down
P10_6	—	√	—	√	—	—	Slow/Fast	√	√
P10_7	—	—	—	√	—	—	Slow/Fast	√	√
P10_8	—	—	—	√	—	—	Slow/Fast	√	√
P10_9	—	√	—	√	—	—	Slow/Fast	√	√
P10_10	—	√	—	√	—	—	Slow/Fast	√	√
P10_11	—	√	—	√	—	—	Slow/Fast	√	√
P10_12	—	√	—	√	—	—	Slow/Fast	√	√
P10_13	—	√	—	√	—	—	Slow/Fast	√	√
P10_14	—	√	—	√	—	—	Slow/Fast	√	√
P10_15	—	√	—	√	—	—	Slow/Fast	√	√
P11_0	—	—	—	√	—	—	Slow/Fast	√	√
P11_1	—	√	—	√	—	—	Slow/Fast	√	√
P11_2	—	—	—	√	—	—	Slow/Fast*3	√	√
P11_3	—	√	—	√	—	—	Slow/Fast*3	√	√
P11_4	—	—	—	√	—	—	Slow/Fast	√	√
P11_5	—	√	—	√	—	—	Slow/Fast	√	—
P11_6	—	√	—	√	—	—	Slow/Fast*3	√	—
AP0_1	√	—	—	—	—	ADC	Slow	—	√*1
AP0_2	√	—	—	—	—	ADC	Slow	—	√*1
AP0_3	√	—	—	—	—	ADC	Slow	—	√*1
AP0_4	√	—	—	—	—	ADC	Slow	—	√*1
AP0_5	√	—	—	—	—	ADC	Slow	—	√*1
AP0_6	√	—	—	—	—	ADC	Slow	—	√*1
AP0_7	√	—	—	—	—	ADC	Slow	—	√*1
AP0_8	√	—	—	—	—	ADC	Slow	—	√*1
AP0_9	√	—	—	—	—	ADC	Slow	—	√*1
AP0_10	√	—	—	—	—	ADC	Slow	—	√*1
AP0_11	√	—	—	—	—	ADC	Slow	—	√*1
AP0_12	√	—	—	—	—	ADC	Slow	—	√*1
AP0_13	√	—	—	—	—	ADC	Slow	—	√*1
AP0_14	√	—	—	—	—	ADC	Slow	—	√*1
AP0_15	√	—	—	—	—	ADC	Slow	—	√*1

Note 1. Pull-down resistor for ADC diagnostic purpose. Control via ADC self-diagnostic register.

Note 2. Supports Cload: 100 pF, it can be set for CSIH0SO and CSIH0SC with fast mode

Note 3. Supports Cload: 50 pF, it can be set for CSIHnSO and CSIHnSC with fast mode. (n = 1 to 2)

Note 4. At a power-on clear reset, an on-chip pull-down resistor at the $\overline{\text{RESET}}$ pin is enabled until the flash sequence is completed.

Caution: Regarding external pull-up resistor of $\overline{\text{RESET}}$ pin, please connect less than 6.6 kΩ.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105 °C, CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
High level input voltage	VIH	CMOS		0.65 ×IOVCC		IOVCC + 0.3	V
		SHMT1 (except FLMD0 pin)		0.7 × IOVCC		IOVCC + 0.3	V
		SHMT1 (FLMD0 pin)*3		0.66 × EVCC		EVCC + 0.3	V
		SHMT2		0.75 × IOVCC		IOVCC + 0.3	V
		SHMT4		0.8 × IOVCC		IOVCC + 0.3	V
		TTL	EVCC = VPOC to 3.6 V	2.0		EVCC + 0.3	V
			EVCC = 3.6 V to 5.5 V	2.2		EVCC + 0.3	V
Low level input voltage	VIL	CMOS		–0.3		0.35 × IOVCC	V
		SHMT1		–0.3		0.3 × IOVCC	V
		SHMT2		–0.3		0.25 × IOVCC	V
		SHMT4		–0.3		0.5 × IOVCC	V
		TTL		–0.3		0.8	V
Input hysteresis for Schmitt	VH	SHMT1		0.3			V
		SHMT2		0.2 × IOVCC			V
		SHMT4		0.1			V
Input leakage current	ILIH	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9, P20 pin, VI = EVCC*2				0.5	µA
		P10, P11 pin, VI = EVCC				0.5	µA
		AP0 pin, VI = A0VREF*2				0.5	µA
	ILIL	$\overline{\text{RESET}}$, FLMD0, JP0, P0, P8, P9, P20 pin, VI = 0 V*2				–0.5	µA
		P10, P11 pin, VI = 0 V*2				–0.5	µA
		AP0 pin, VI = 0 V*2				–0.5	µA
Internal pull-up resistance	RU	except FLMD0 pin, VI = 0 V		20	40	100	kΩ
		FLMD0, VI = 0 V*3		4	12	36	kΩ
Internal pull-down resistance	RD	except FLMD0 pin, VI = IOVCC		20	40	100	kΩ
		FLMD0, VI = EVCC		4	12	36	kΩ
High level output voltage	VOH	Fast mode					
			IOH = –5 mA (6 pins)*4	IOVCC – 1.0			V
			IOH = –3 mA (10 pins)*4	IOVCC – 1.0			V
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
		Slow mode					
			IOH = –1 mA (16 pins)*4	IOVCC – 0.5			V
			IOH = –0.1 mA (16 pins)*4	IOVCC – 0.5			V
Low level output voltage	VOL	Fast mode					
			IOL = 5 mA (6 pins)*4			0.4	V
			IOL = 3 mA (10 pins)*4			0.4	V
			IOL = 1 mA (16 pins)*4			0.4	V
		Slow mode					
			IOL = 1 mA (16 pins)*4			0.4	V
Rise/Fall time	t_{KRP}/t_{KFP}	Fast mode (except below pins)*5	CL = 30 pF			7	ns
			CL = 50 pF			12	ns
			CL = 100 pF			24	ns
		Fast mode (P0_5, P0_6, P10_1, P10_2, P11_2, P11_3, P11_6)*6	CL = 50 pF			6	ns
		Fast mode (P0_2, P0_3)*6	CL = 100 pF			6.15	ns
		Slow mode*5	CL = 30 pF			37	ns
			CL = 50 pF			62	ns
			CL = 100 pF			124	ns

(2/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Output frequency	f_O	Fast mode	CL = 30 pF			40	MHz
		Slow mode	CL = 30 pF			10	MHz
			CL = 50 pF			6	MHz
			CL = 100 pF			3	MHz

Note 1. “IOVCC” means the pins are assigned to the power supply (EVCC and A0VREF).

Note 2. Not select the analog input function of ADC0.

Note 3. When the internal pull-up resistor of FLMD0 pin is applied by FLMDCNT register, please connect 86 kΩ or more as external pull-down resistor.

Note 4. The number of pin indicates simultaneous ON.

Note 5. Measurement point: 0.1 × IOVCC to 0.9 × IOVCC

Note 6. Measurement point: 0.2 × IOVCC to 0.8 × IOVCC

1.9.1 Output Current

1.9.1.1 100 pin

Table 1.8 Output Current (100 pin)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
High level output current	IOH	PgE	Per side	P9_0, P9_1			–11	mA
				P20_4, P20_5			–18	mA
				P0_0 to P0_3			–12	mA
				JP0_3 to JP0_5, P0_4 to P0_6, P0_11 to P0_14, P8_2, P8_10 to P8_12			–30	mA
				JP0_0 to JP0_2			–14	mA
				P0_7 to P0_10, P8_0 to P8_1, P8_3 to P8_7			–28	mA
				P8_8, P8_9			–10	mA
				P10_6 to P10_14, P11_1 to P11_6			–30	mA
				P10_0 to P10_2			–15	mA
				P10_3 to P10_5			–15	mA
				P10_15, P11_0			–30	mA
			Total (EVCC)				–60	mA
		PgA0	Total (A0VREF)				–16	mA
Low level output current	IOL	PgE	Per side	P9_0, P9_1			11	mA
				P20_4, P20_5			18	mA
				P0_0 to P0_6, P0_11 to P0_14			30	mA
				JP0_0 to JP0_5, P8_2, P8_10 to P8_12			20	mA
				P0_7 to P0_10			11	mA
				P8_0, P8_1, P8_3 to P8_7			10	mA
				P8_8, P8_9			10	mA
				P10_6 to P10_14, P11_1 to P11_2			30	mA
				P11_3 to P11_6			30	mA
				P10_0 to P10_2			15	mA
				P10_3 to P10_5			15	mA
				P10_15, P11_0			30	mA
			Total (EVCC)				60	mA
		Pg A0	Total (A0VREF)				16	mA

Note 1. For detail of the definition of “side” and “total”, refer to **Section 1.2.3, Port Current**.

1.10 Power Supply Currents

Condition: REGVCC, EVCC and A0VREF total current. But, the I/O buffer is stopped.

Item	Symbol	Condition				MIN.	TYP.*1	MAX.	Unit
		CPU1/CPU2	PLL	Ta	Peripheral				
RUN mode current	IDDR1	RUN (120 MHz)	RUN	–40 to 125°C	Run(#1)		82	144	mA
				25°C	Stop(#1)		70		mA
RUN mode current (During data/code flash programming)	IDDR3	RUN (120 MHz)	RUN	–40 to 125°C	Run(#2)		94	161	mA
HALT mode current	IDDH	RUN	RUN	–40 to 125°C	Run(#3)		47	115	mA
STOP mode current	IDDS	Stop	Stop	–40 to 85°C	Stop(#2)		0.75	15	mA
				105°C	Stop(#2)			25	mA
				125°C	Stop(#2)			42	mA
DeepSTOP mode current	IDDDS	Power off	Power off	–40 to 85°C	Stop(#3)		50	540	µA
				105°C	Stop(#3)			950	µA
				125°C	Stop(#3)			1600	µA
Cyclic RUN mode current	IDDCR	RUN (HS IntOSC)	Stop	–40 to 85°C	Run(#4)		4	25	mA
				105°C	Run(#4)			40	mA
				125°C	Run(#4)			72	mA
Cyclic STOP mode current	IDDCS	Stop	Stop	–40 to 85°C	Run(#5)		2	22	mA
				105°C	Run(#5)			38	mA
				125°C	Run(#5)			70	mA

Note 1. The condition of “TYP.” shows the specification with the following conditions. Also, the value is just for reference only. RUN mode current of TYP condition shows the value when ICUMB is stop.
- Ta = 25°C
- REGVCC = EVCC = A0VREF = 5.0 V
- AWOVSS = EVSS = A0VSS = 0 V

Caution: It must be ensured that the junction temperature in the Ta range remains below Tj≤130°C and does not exceed its limit under application conditions (thermal resistance, power supply current, peripheral current (if not included in power supply current), port output current and injection current).

(1/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
AWO	MainOSC	Run	Run	Run	Stop	Stop	Run	Stop	Stop
	HS IntOSC	Run	Run	Run	Run	Stop	Run	Stop	Stop
	LPS	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	RRAM	Read / Write	Read / Write	No access	Fetch	No access	Read/Write	No access	No access
	WDTA0	Stop	Stop	Stop	Stop	Stop	Stop	Stop	Stop
	TAUJ0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	RTCA0	Run	Run	Run	Run (LS IntOSC)	Run (LS IntOSC)	Stop	Stop	Stop
	CLMA0	Run	Run	Run	Run	Stop	Stop	Stop	Stop
	CLMA1	Run	Run	Run	Stop	Stop	Stop	Stop	Stop
	ADCA0	Run	Run	Run	Stop	Stop	Stop	Stop	Stop

(2/2)

Power Domain	Function	Run					Stop		
		(#1)	(#2)	(#3)	(#4)	(#5)	(#1)	(#2)	(#3)
ISO	CPU1 (PE1)	Run (PLL)	Run (PLL)	Halt (PLL)	Run (HS IntOSC)	Stop	Run (PLL)	Stop	Power off
	CPU2 (PE2)	Run (PLL)	Run (PLL)	Halt (PLL)	Stop	Stop	Run (PLL)	Stop	
	ICUMB	Run	Run	Stop	Stop	Stop	Stop	Stop	
	DMA	Run	Run	Run	Stop	Stop	Stop	Stop	
	PLL0	Run	Run	Run	Stop	Stop	Run	Stop	
	PLL1	Run	Run	Run	Stop	Stop	Run	Stop	
	Code Flash (FLI0)	Fetch	No access	No access	No access	No access	Fetch	No access	
	Code Flash (FLI1)	Stop	No access	No access	No access	No access	Fetch	No access	
	Code Flash (FLI2)	Fetch	No access	No access	No access	No access	Fetch	No access	
	Data Flash	Read	Write / Erase	No access	No access	No access	Read	No access	
	LRAM (PE1)	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	LRAM (PE2)	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	GRAM	Read / Write	Read / Write	No access	No access	No access	Read/Write	No access	
	OSTMn	Run	Run	Run	Stop	Stop	Stop	Stop	
	WDTAn	Stop	Stop	Stop	Stop	Stop	Stop	Stop	
	TAUD0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUB0	Run	Run	Run	Stop	Stop	Stop	Stop	
	TAUJ1	Run	Run	Run	Stop	Stop	Stop	Stop	
	PWM-diag	Run	Run	Run	Stop	Stop	Stop	Stop	
	RLIN3n	Run (115.2kbps)	Run (115.2kbps)	Run (115.2kbps)	Stop	Stop	Stop	Stop	
	RLIN2n	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	RS-CANn	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CSIG0	Run	Run	Run	Stop	Stop	Stop	Stop	
	CSIHn	Run	Run	Run	Stop	Stop	Stop	Stop	
	RIIC0	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	KR	Wait	Wait	Wait	Stop	Stop	Stop	Stop	
	CLMA2	Run	Run	Run	Stop	Stop	Stop	Stop	

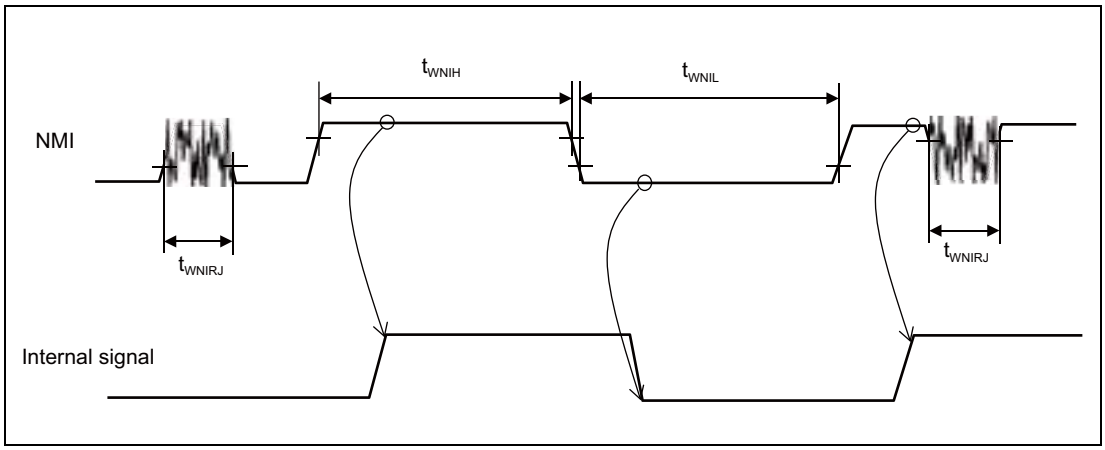
1.11 Interrupt Timing

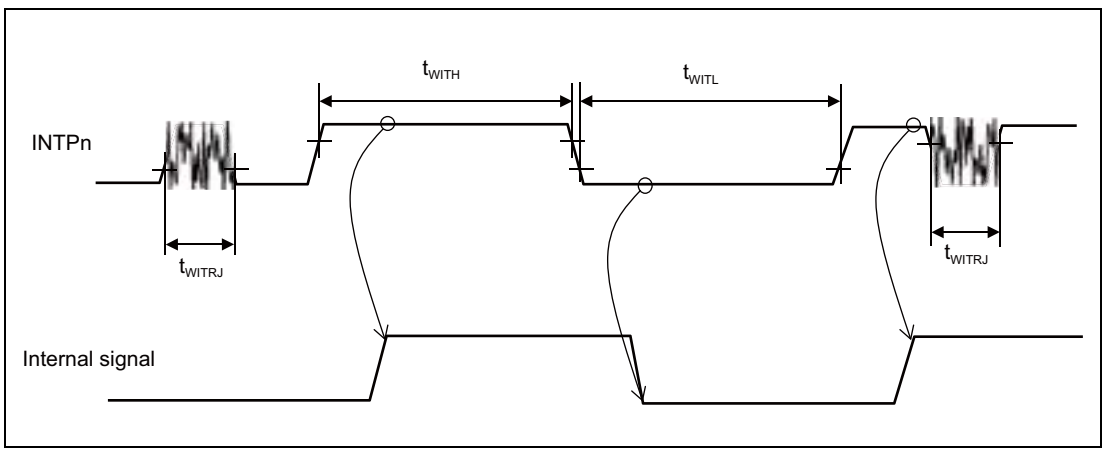
Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
NMI input high / low level width*1	t_{WNIH} / t_{WNIL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
NMI pulse rejection*2	t_{WNIRJ}		100			ns
INTPn input high / low level width*1	t_{WITH} / t_{WITL}	Edge detection mode	600			ns
		Level detection mode (EMCLK is operated by HS IntOSC)	756			ns
		Level detection mode (EMCLK is operated by LS IntOSC)	5.13			µs
INTPn pulse rejection*2	t_{WITRJ}		100			ns

Note 1. NMI and INTPn input width is needed to ensure that the internal interrupt signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





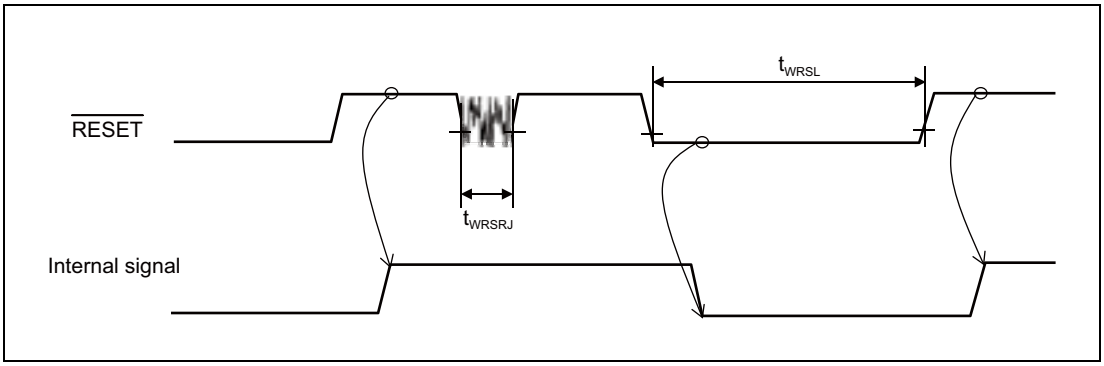
1.12 $\overline{\text{RESET}}$ Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{RESET}}$ input low level width*1	t_{WRSL}	*3	0.6			µs
		*4	5.0			µs
		*5	600			µs
$\overline{\text{RESET}}$ pulse rejection*2	t_{WRSRJ}		0.1			µs

Note 1. $\overline{\text{RESET}}$ input width is needed to ensure that the internal reset signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.

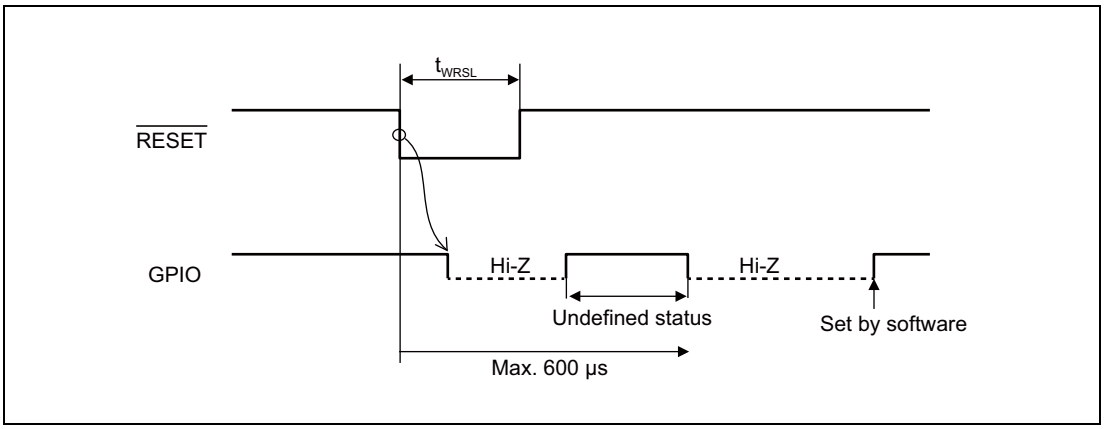


Note 3. After $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600µs will become Hi-z. (figure (a))

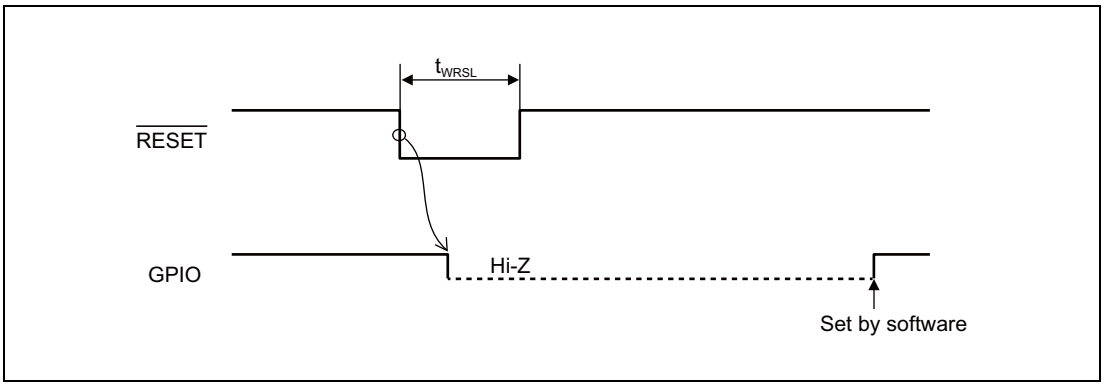
Note 4. If during RUN mode or HALT mode, after $\overline{\text{RESET}}$ is asserted GPIO pin will become Hi-z. For other modes, after $\overline{\text{RESET}}$ is asserted there will be a period where GPIO output could become an undefined status and after 600us will become Hi-z. (figure (a) and (b))

Note 5. GPIO output states will become Hi-z after $\overline{\text{RESET}}$ is asserted. (figure (b))

(a) In case of either
t_{WRSL} < 5 µs, any mode or
t_{WRSL} < 600 µs, any mode except for RUN and HALT mode.



(b) In case of either
5 µs ≤ t_{WRSL}, RUN and HALT mode or
600 µs ≤ t_{WRSL}, any mode.

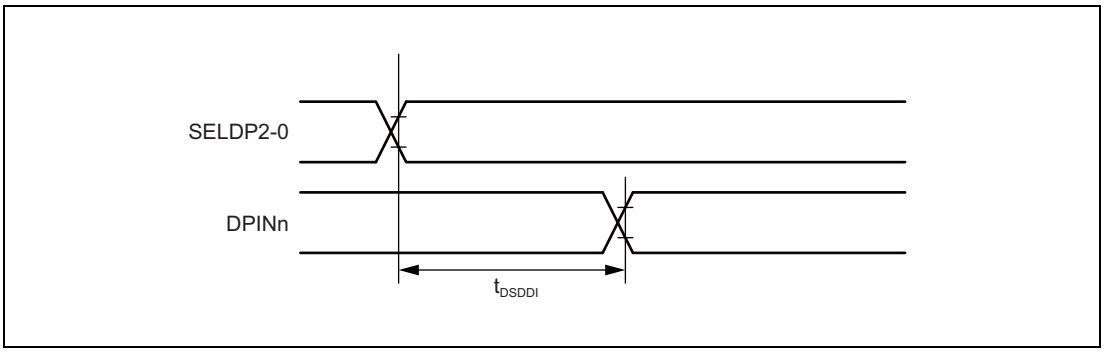


1.13 Low Power Sampler (DPIN Input) Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DPINn input delay time (vs SELDP2-0)	t_{DSDDI}				150	ns

Note 1. n = 7 to 0



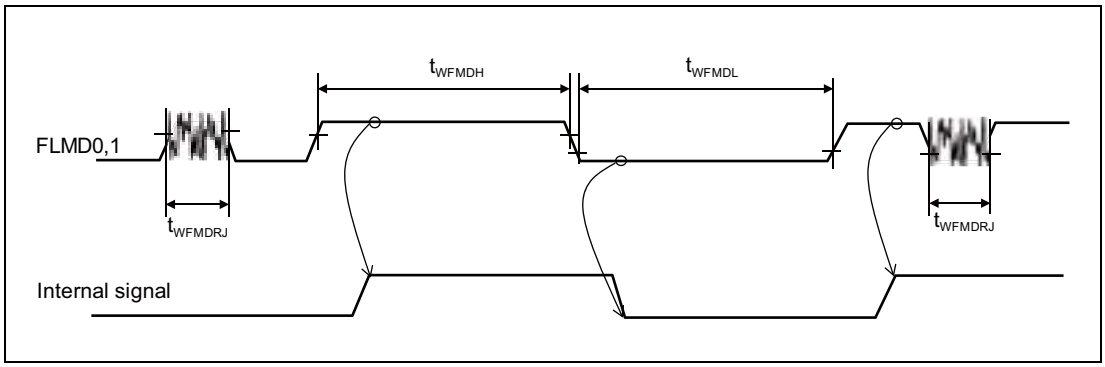
1.14 Mode Timing

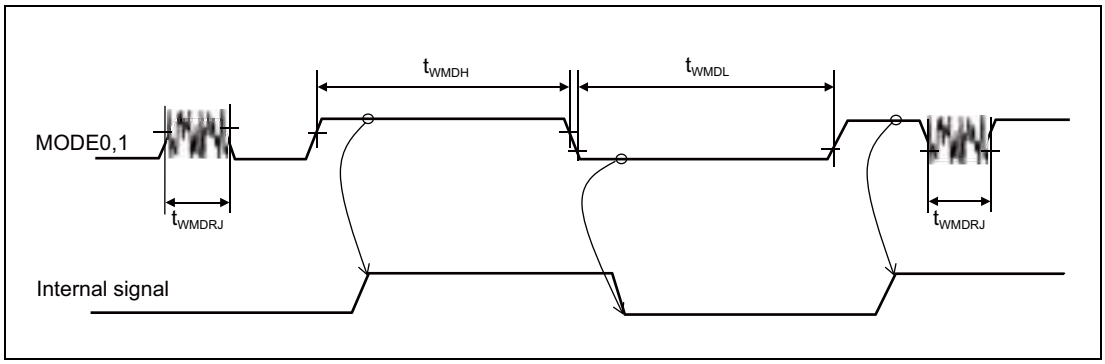
Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0,1 input high / low level width*1	t_{WFMDH} / t_{WFMDL}		600			ns
FLMD0, 1 pulse rejection*2	t_{WFMDRJ}		100			ns
MODE0,1 input high / low level width*1	t_{WMDH} / t_{WMDL}		600			ns
MODE0, 1 pulse rejection*2	t_{WMDRJ}		100			ns

Note 1. FLMD0,1 and MODE0,1 input width is needed to ensure that the internal mode signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





1.15 Timer Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105°C, CL = 30 pF

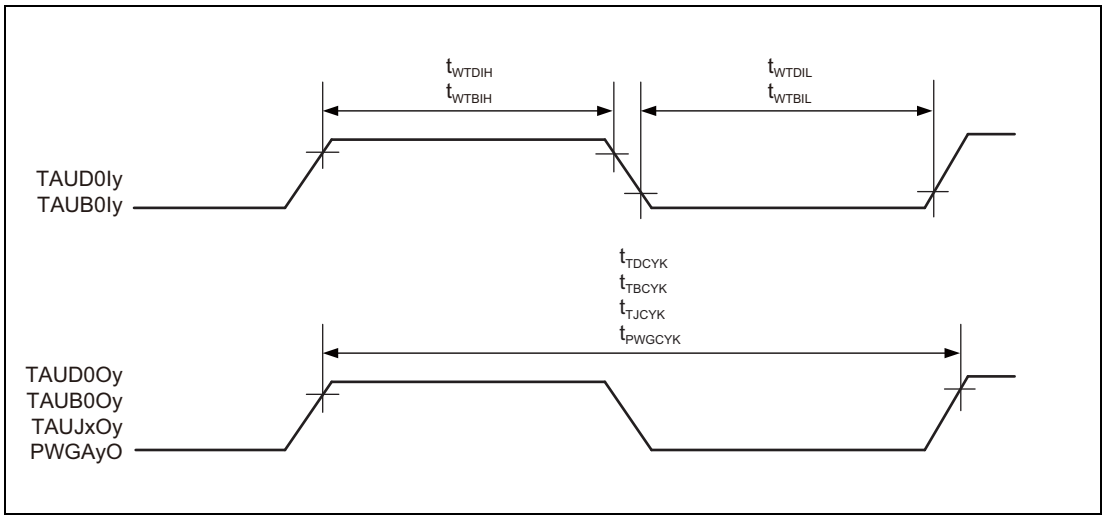
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
TAUD0Iy input high/low level width (y = 0 to 15)	t_{WTDIH}/ t_{WTDIL}		n × Tsamp + 20[*1, *2]			ns
TAUD0Oy output cycle (y = 0 to 15)	t_{TDCYK}	Slow mode			10	MHz
TAUB0Iy input high/low level width (y = 0 to 15)	t_{WTBIH}/ t_{WTBIL}		n × Tsamp + 20[*1, *2]			ns
TAUB0Oy output cycle (y = 0 to 15)	t_{TBCYK}	Slow mode			10	MHz
TAUJxIy input high/low level width[*3] (x = 0, 1, y = 0 to 3)	t_{WTJIH}/ t_{WTJIL}		600			ns
TAUJxIy pulse rejection[*4]	t_{WTIJRJ}		100			ns
TAUJxOy output cycle (x = 0, 1, y = 0 to 3)	t_{TJCYK}	Slow mode			10	MHz
PWGAyO output cycle (y = 0 to 14)	t_{PWGCYK}	Slow mode			10	MHz

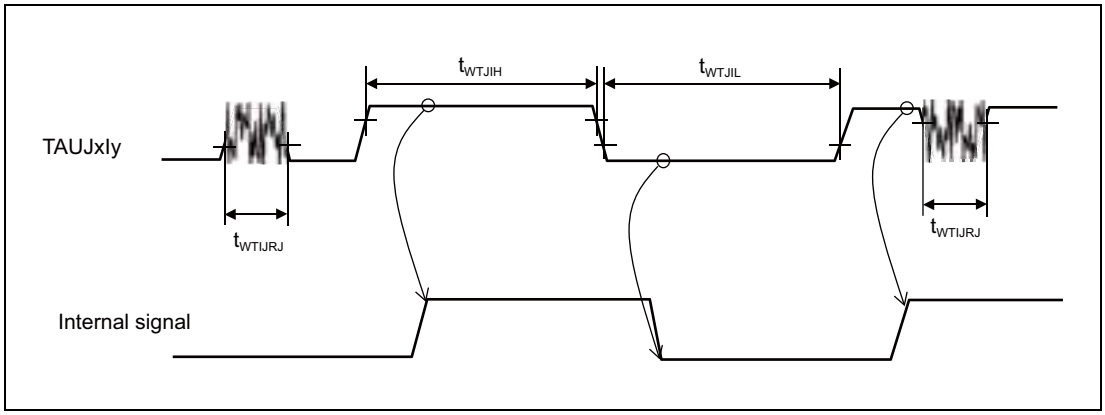
Note 1. n: Sampling number of the digital noise filter for each input.
Tsamp: Sampling time of the digital noise filter for each input.

Note 2. Input more than 1 count clock width of each timer counter channel.

Note 3. TAUJxIy input width is needed to ensure that the internal timer input signal is activated.

Note 4. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.





1.16 RLIN2 / RLIN3 Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RLIN3 transfer rate		LIN specification	1		20	kbps
		LIN extended baudrate	1		115.2*1	kbps
		UART function			1.5	Mbps
RLIN2 transfer rate		LIN specification	1		20	kbps

Note 1. The LIN extended baudrate is not part of the LIN standard specification.

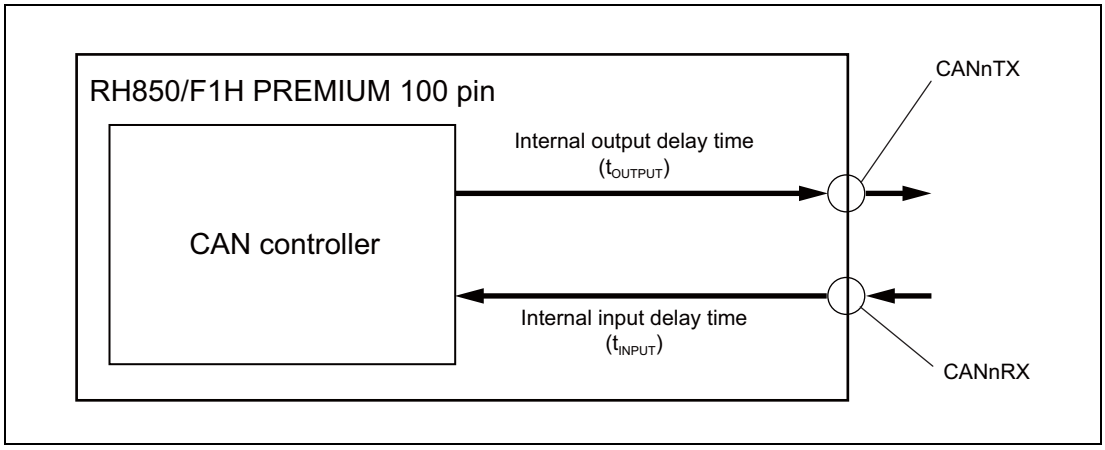
1.17 RS-CAN / RS-CANFD Timing

1.17.1 RS-CAN / RS-CANFD (Classical CAN Mode) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					1	Mbps
Internal delay time*1	t_{NODE}				100	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})

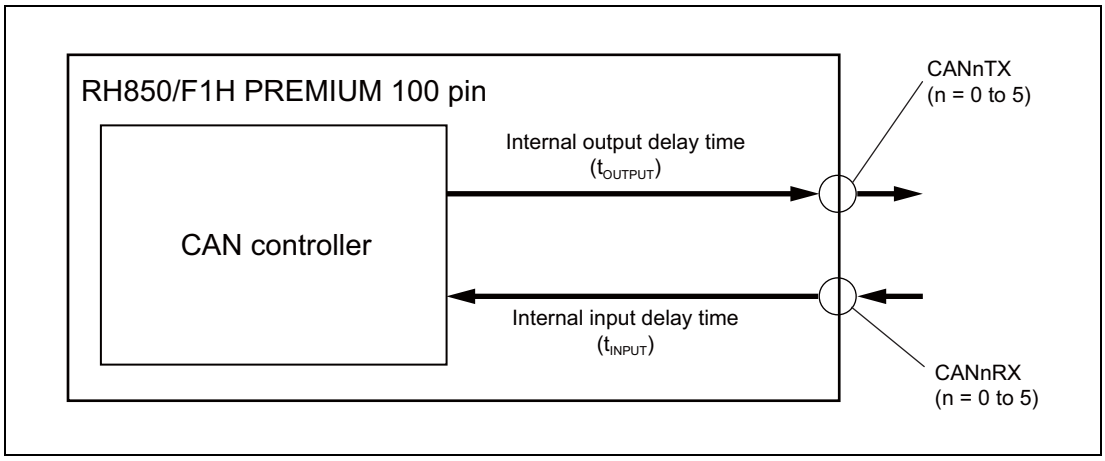


1.17.2 RS-CANFD (CAN-FD Mode) Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30%, CISOVCL: 0.1uF +/–30%,
Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Transfer rate					5	Mbps
Internal delay time*1	t_{NODE}				50	ns

Note 1. t_{NODE} = Internal input delay time (t_{INPUT}) + Internal output delay time (t_{OUTPUT})



1.18 CSI Timing

1.18.1 CSIG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Table 1.9 CSIG Timing (Master Mode)

<Output driver strength>

CSIG0SO, CSIG0SC (output): Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYG0}		12.5 (max. 80 MHz)			ns
CSIG0SC cycle time	t_{KCYMG0}		100			ns
CSIG0SC high level width	t_{KWHMG0}		0.5 × t_{KCYMG0} – 10			ns
CSIG0SC low level width	t_{KWLMG0}		0.5 × t_{KCYMG0} – 10			ns
CSIG0SI setup time (vs CSIG0SC)	t_{SSIMG0}		30			ns
CSIG0SI hold time (vs CSIG0SC)	t_{HSIMG0}		0			ns
CSIG0SO output delay (vs CSIG0SC)	t_{DSOMG0}				7	ns
CSIG0RYI setup time (vs CSIG0SC)	t_{SRYIG0}	CSIG0CTL1.CSIG0SIT = x CSIG0CTL1.CSIG0HSE = 1	2 × t_{KCYG0} + 25			ns
CSIG0RYI High level width	t_{WRYIG0}	CSIG0CTL1.CSIG0HSE = 1	t_{KCYG0} + 5			ns

Table 1.10 CSIG Timing (Slave Mode)

<Output driver strength>

CSIG0SO: Fast mode
CSIG0RYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYG0}		12.5 (max. 80 MHz)			ns
CSIG0SC cycle time	t_{KCYSG0}		200			ns
CSIG0SC high level width	t_{KWHSG0}		0.5 × t_{KCYSG0} – 10			ns
CSIG0SC low level width	t_{KWLSG0}		0.5 × t_{KCYSG0} – 10			ns
CSIG0SI setup time (vs CSIG0SC)	t_{SSISG0}		20			ns
CSIG0SI hold time (vs CSIG0SC)	t_{HSISG0}		t_{KCYG0} + 5			ns
CSIG0SO output delay (vs CSIG0SC)	t_{DSOSG0}				30	ns
CSIG0RYO output delay	t_{SRYOG0}	$t_{KCYSG0} \geq 8 \times t_{KCYG0}$			39	ns
		$t_{KCYSG0} < 8 \times t_{KCYG0}$			39 + t_{KCYG0}	ns
$\overline{\text{CSIG0SSI}}$ setup time (vsCSIG0SC)	$t_{SSSISG0}$		0.5 × t_{KCYSG0} – 5			ns
$\overline{\text{CSIG0SSI}}$ hold time (vs CSIG0SC)	$t_{HSSISG0}$		t_{KCYG0} + 5			ns

1.18.2 CSIH Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Table 1.11 CSIH Timing (Master Mode)

<Output driver strength>

CSIHnSO, CSIHnSC (output): Fast mode (CL = 100 pF@n = 0 / 50 pF@n = 1 to 2)
CSIHnCSSm: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYMHn}		100			ns
CSIHnSC high level width	t_{KWHMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSC low level width	t_{KWLMHn}		0.5 × t_{KCYMHn} – 10			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	19			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	14			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSIMHn}	SI Positive edge mode (CSIHnCTL1.CSIHnSLRS = 0)	0			ns
		SI Negative edge mode (CSIHnCTL1.CSIHnSLRS = 1)	t_{KCYHn} / 2			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOMHn}				7	ns
CSIHnRYI setup time (vs CSIHnSC)	t_{SRYIHn}	CSIHnCTL1.CSIHnSIT = x CSIHnCTL1.CSIHnHSE = 1	2 × t_{KCYHn} + 25			ns
CSIHnRYI High level width	t_{WRYIHn}	CSIHnCTL1.CSIHnHSE = 1	t_{KCYHn} + 5			ns
CSIHnCSS0-7 inactive width	$t_{WSCSBHn}$		CSIDLE × t_{KCYMHn} – 15			ns
CSIHnCSS0-7 setup time (vs CSIHnSC)	$t_{SSCSBHn0}$	CSIHnCFGx.CSIHnDAP = 0	CSSETUP × t_{KCYMHn} – 23			ns
	$t_{SSCSBHn1}$	CSIHnCFGx.CSIHnDAP = 1	(CSSETUP + 0.5) × t_{KCYMHn} – 23			ns
CSIHnCSS0-7 hold time (vs CSIHnSC)	$t_{HSCSBHn0}$	CSIHnCTL1.CSIHnSIT = 0	CSSHOLD × t_{KCYMHn} – 5			ns
	$t_{HSCSBHn1}$	CSIHnCTL1.CSIHnSIT = 1	(CSSHOLD + 0.5) × t_{KCYMHn} – 5			ns

NOTE

CSIDLE: Setting value of CSIHnCFGx.CSIHnIDx[2:0]
CSSETUP: Setting value of CSIHnCFGx.CSIHnSPx[3:0]
CSSHOLD: Setting value of CSIHnCFGx.CSIHnHDx[3:0]
x: Depends on number of the chip select signals.

CAUTION

When the serial clock level is changed during the communication (CSIHnCFGx.CSIHnCKPx) and the IDLE has a setting of 0.5 transmission clock period an inactive width time $t_{WSCSBHn}$ of "0.5 × t_{KCYMHn}" is added.

Table 1.12 CSIH Timing (Slave Mode)

<Output driver strength>

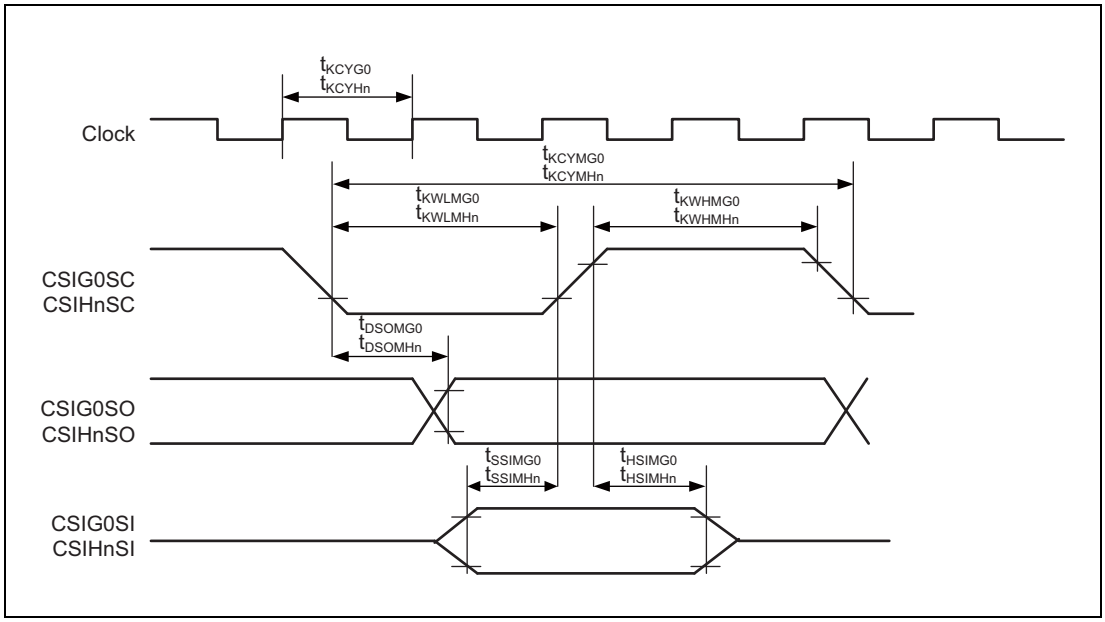
CSIHnSO, CSIHnSC (output): Fast mode
CSIHnRYO: Slow mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Macro Operation clock cycle time	t_{KCYHn}		12.5 (max. 80 MHz)			ns
CSIHnSC cycle time	t_{KCYSHn}		200			ns
CSIHnSC high level width	t_{KWHSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSC low level width	t_{KWLSHn}		$0.5 \times t_{KCYSHn} - 10$			ns
CSIHnSI setup time (vs CSIHnSC)	t_{SSISHn}		20			ns
CSIHnSI hold time (vs CSIHnSC)	t_{HSISHn}		$t_{KCYHn} + 5$			ns
CSIHnSO output delay (vs CSIHnSC)	t_{DSOSHn}				30	ns
CSIHnRYO output delay	t_{SRYOHn}	$t_{KCYSHn} \geq 8 \times t_{KCYHn}$			39	ns
		$t_{KCYSHn} < 8 \times t_{KCYHn}$			$39 + t_{KCYHn}$	ns
$\overline{\text{CSIHnSSI}}$ setup time (vs CSIHnSC)	$t_{SSSISHn}$		$0.5 \times t_{KCYSHn} - 5$			ns
$\overline{\text{CSIHnSSI}}$ hold time (vs CSIHnSC)	$t_{HSSISHn}$		$t_{KCYHn} + 5$			ns

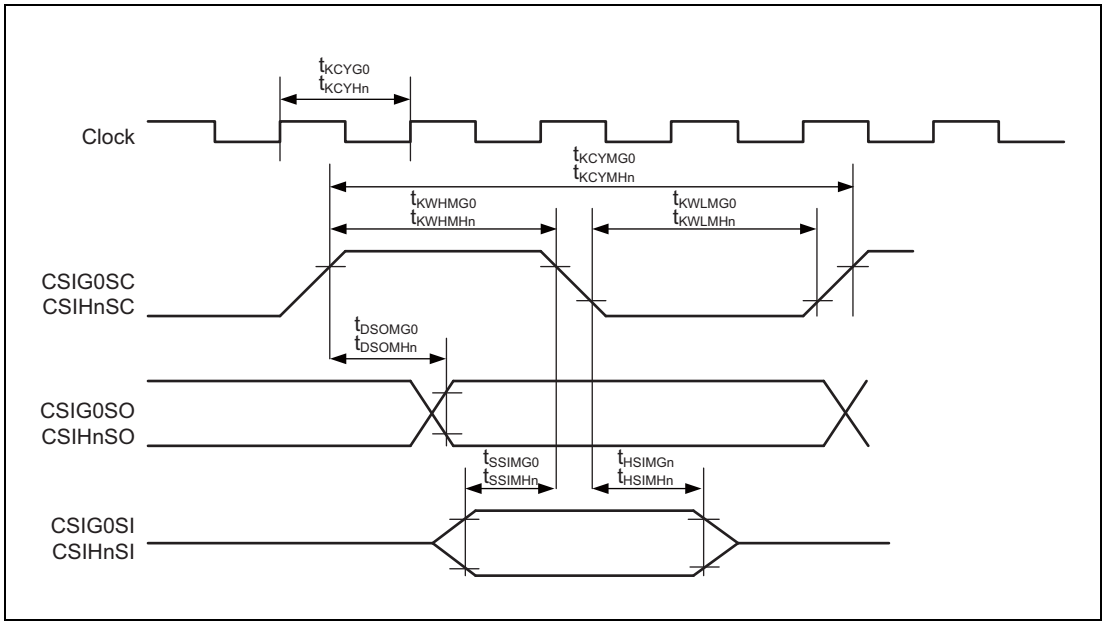
(1) SC/SI/SO

Master Mode:

- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



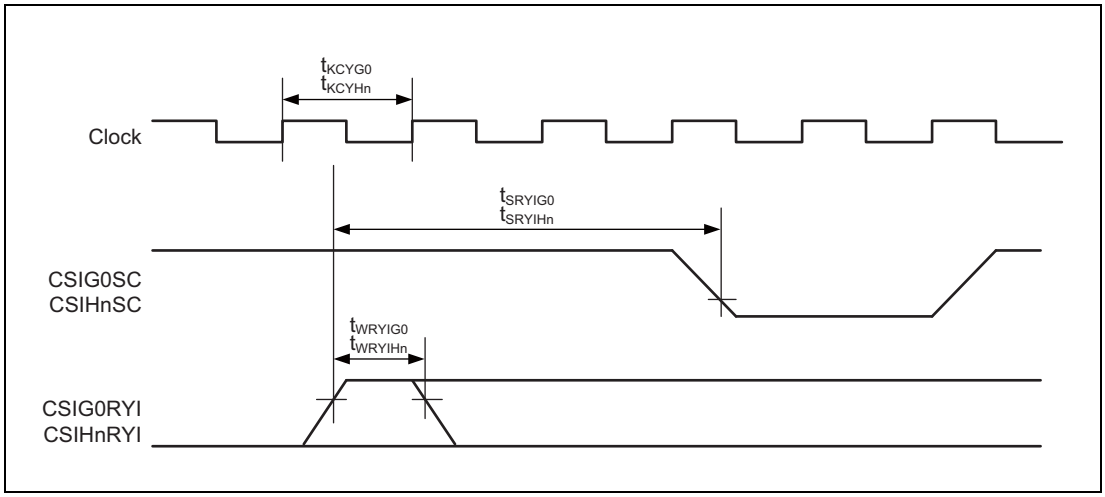
- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



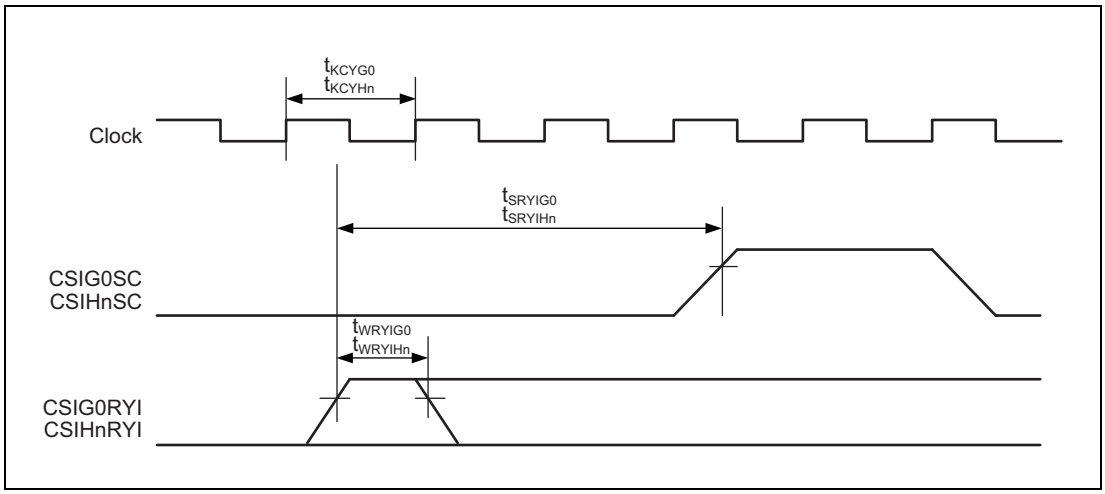
(2) RYI

CSIG: Only master mode (CSIG0CTL1: CSIG0HSE = 1, CSIG0CTL1: CSIG0SIT = 0)
CSIH: Only master mode (CSIHnCTL1: CSIHnHSE = 1, CSIHnCTL1: CSIHnSIT = 0)

- CSIG (CSIG0CTL1: CSIG0CKR = 0)
- CSIH (CSIHnCFGm: CSIHnCKPm = 0)



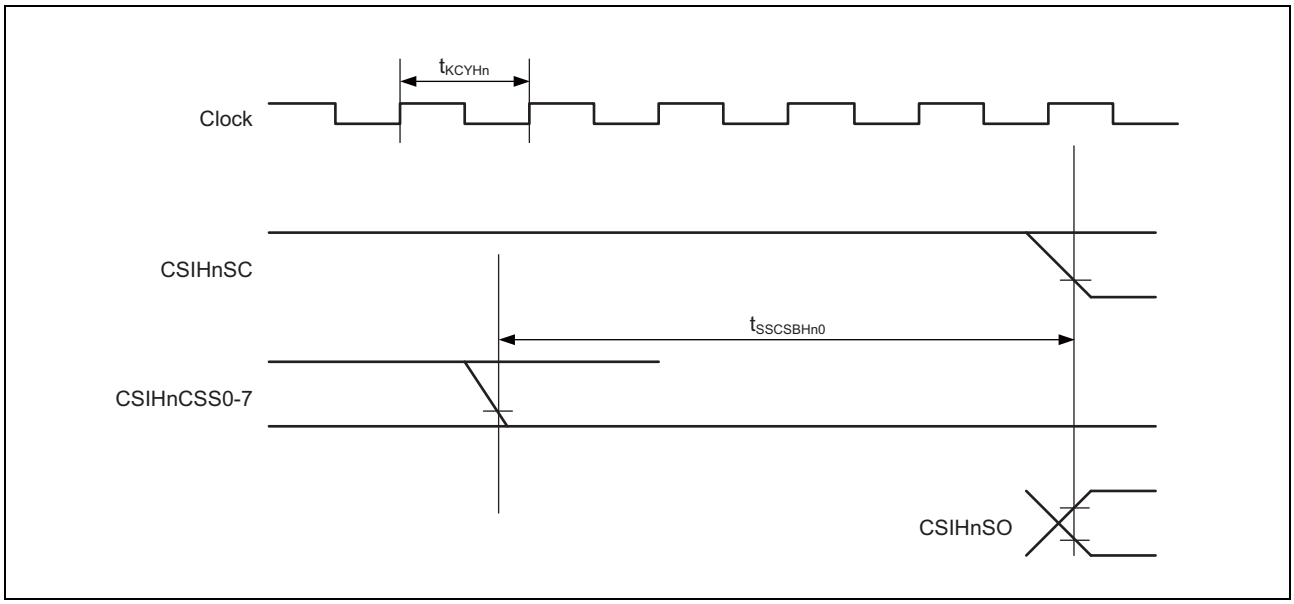
- CSIG (CSIG0CTL1: CSIG0CKR = 1)
- CSIH (CSIHnCFGm: CSIHnCKPm = 1)



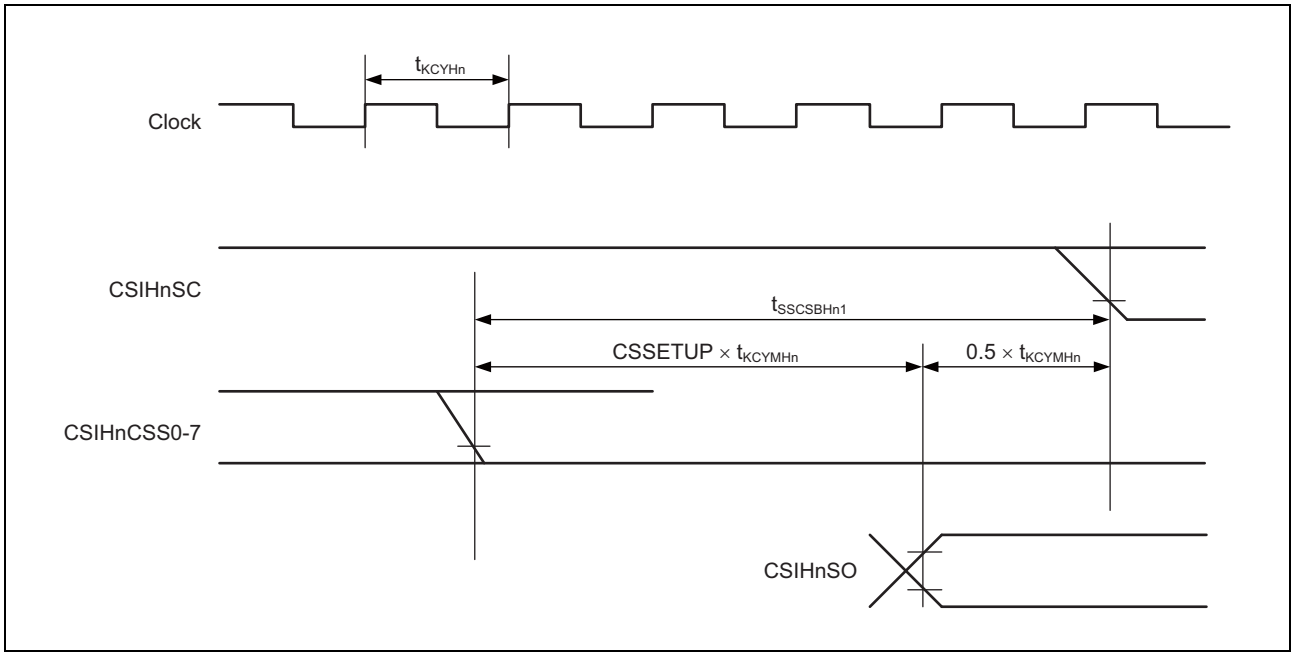
(3) CSSn

Only Master Mode (Setup Time):

- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0

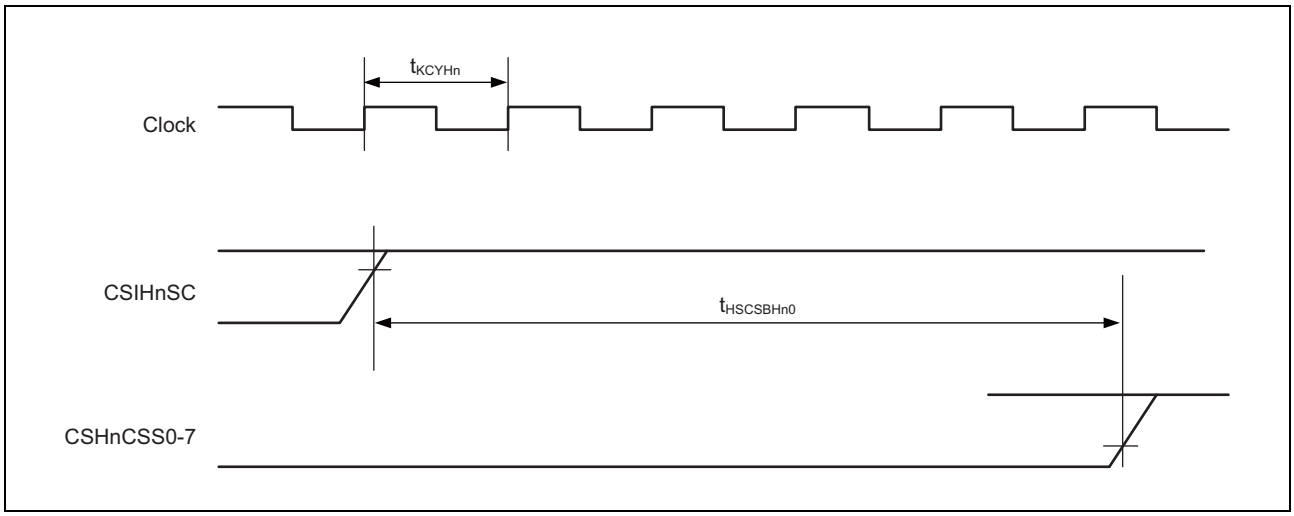


- CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 1

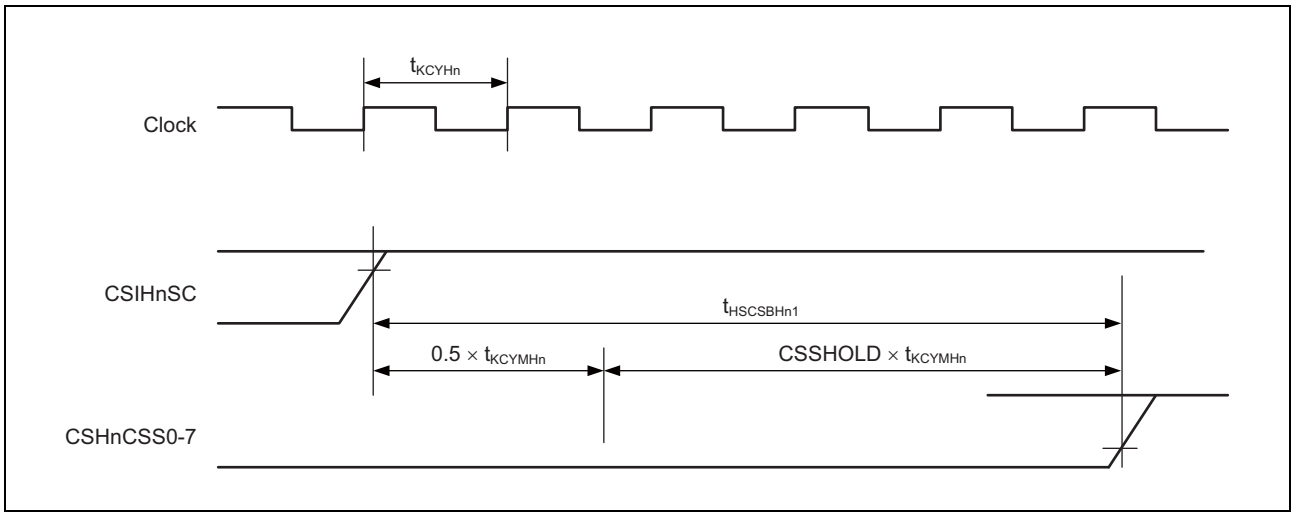


Only Master Mode (Hold Time):

- CSIHnCTL1: CSIHnSIT = 0, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



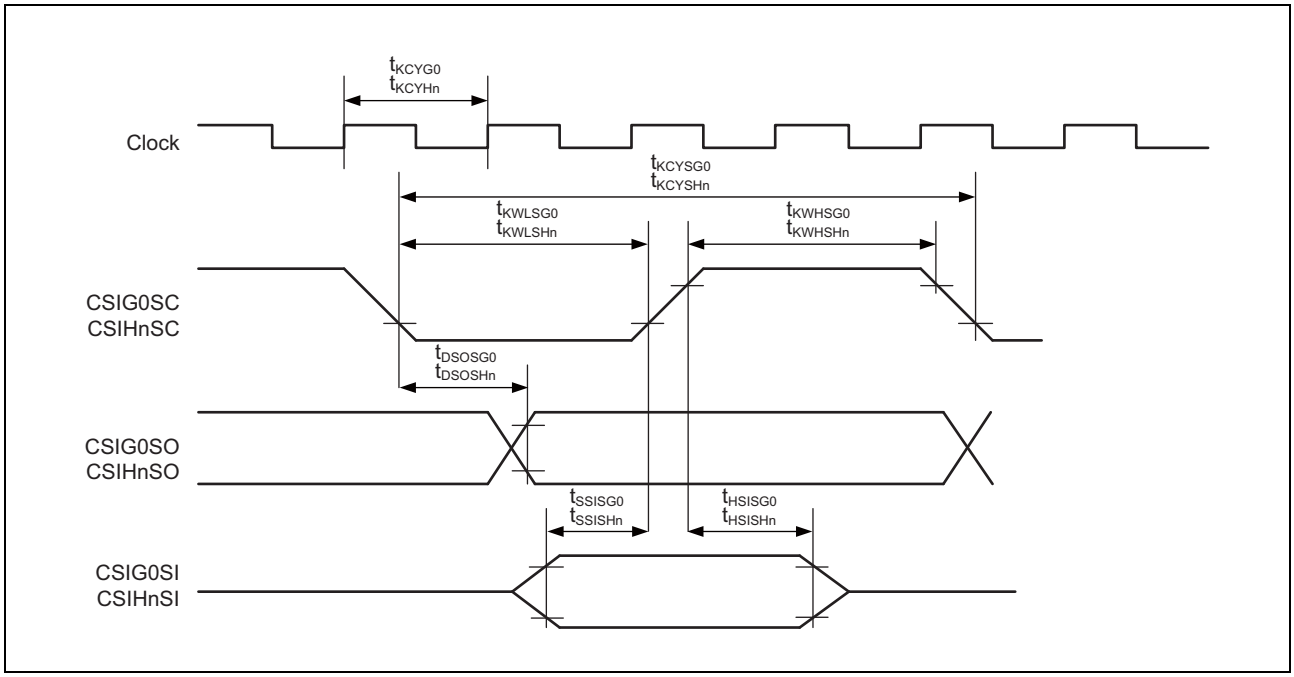
- CSIHnCTL1: CSIHnSIT = 1, CSIHnCFGm: CSIHnCKPm = 0, CSIHnCFGm: CSIHnDAPm = 0



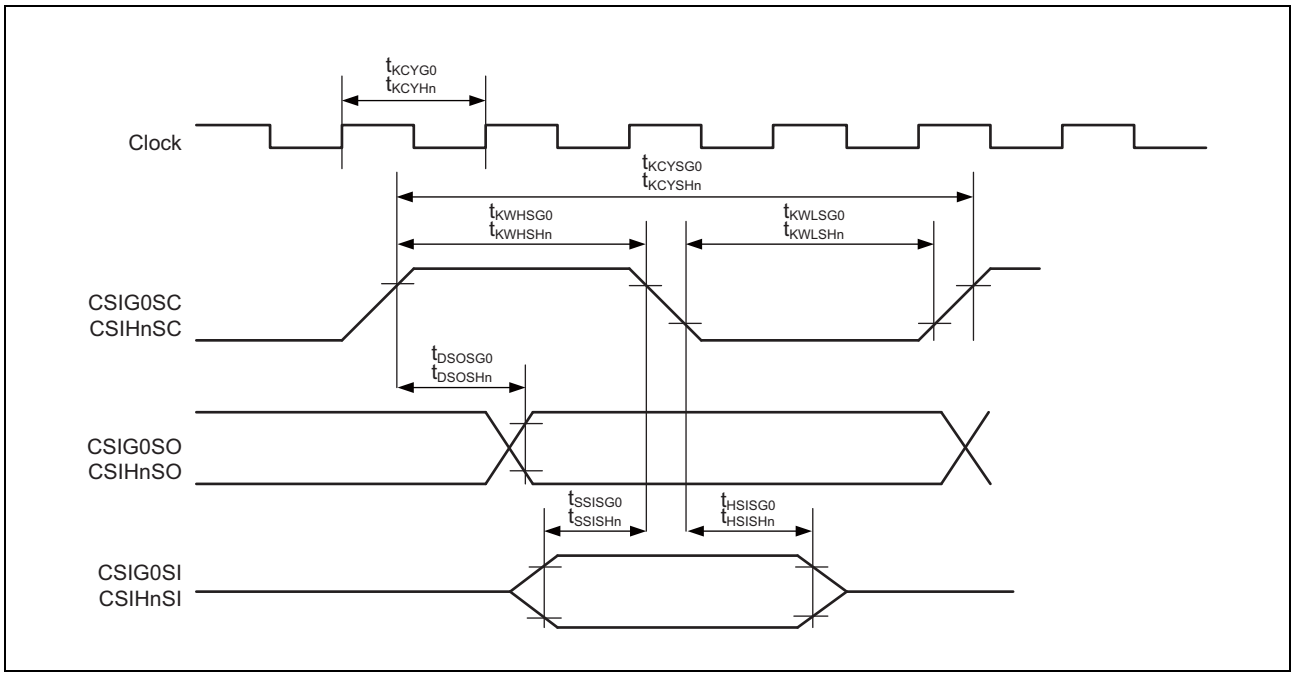
(4) SC/SI/SO

Slave Mode:

- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 0/0 or 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0 /0 or 1/1)

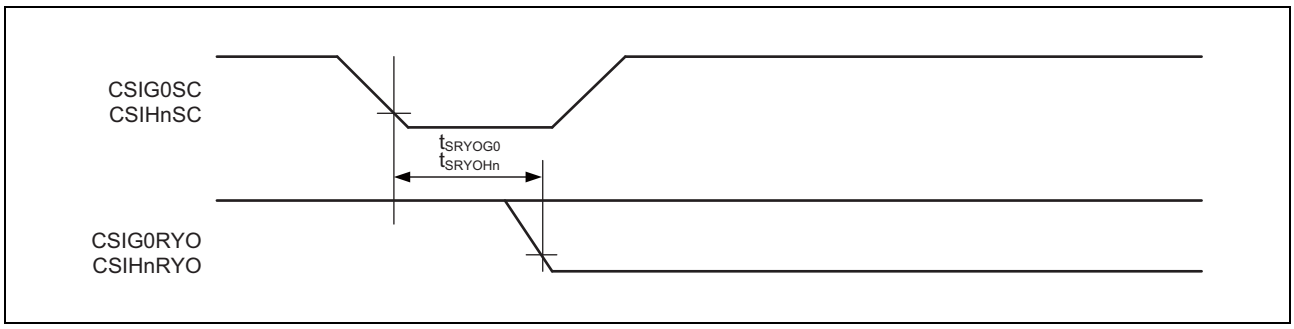


- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 1/0 or 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)

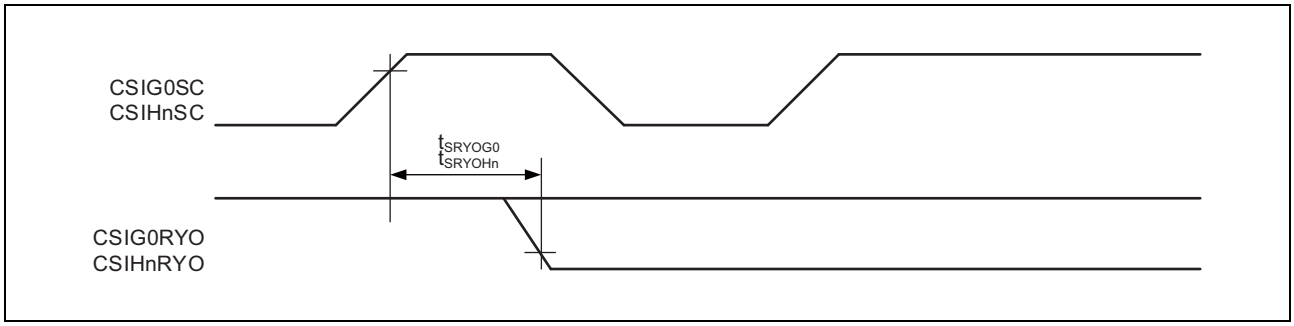


(5) RYO

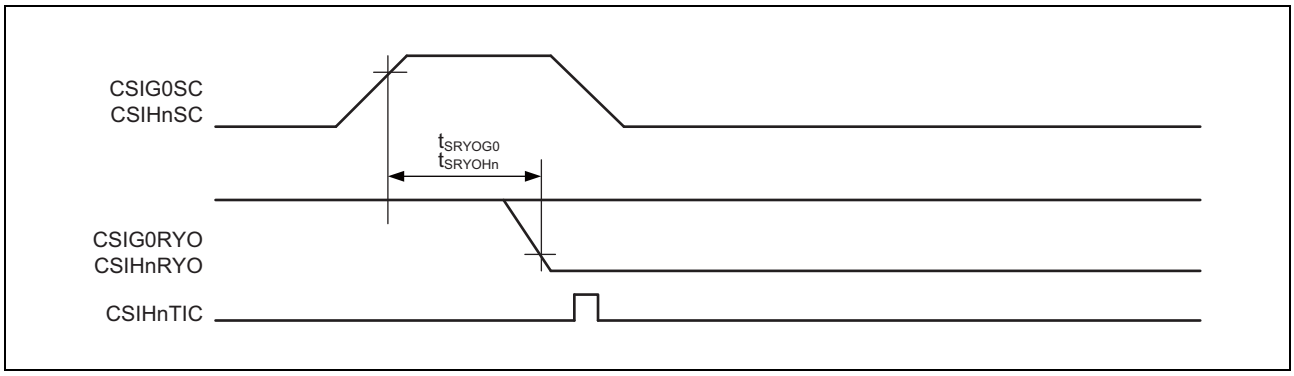
- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 0/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0)



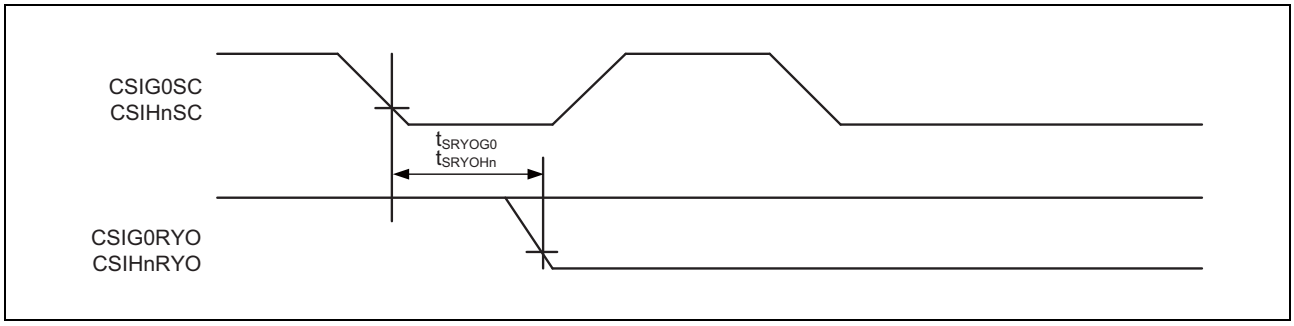
- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 0/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/1)



- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 1/0)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0)



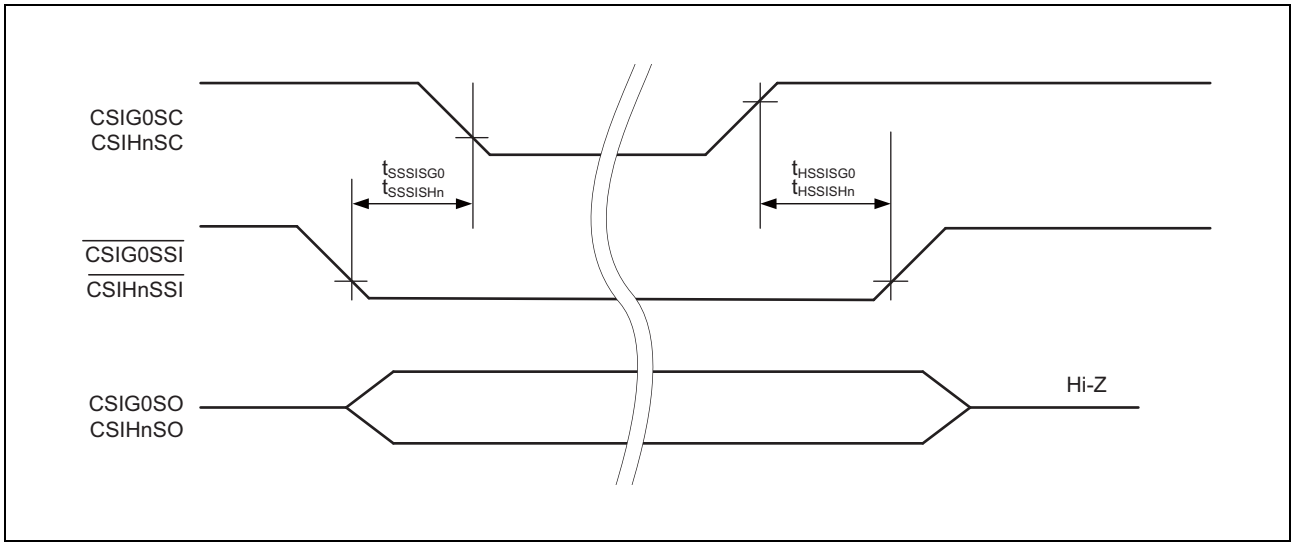
- CSIG (CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 1/1)
- CSIH (CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/1)



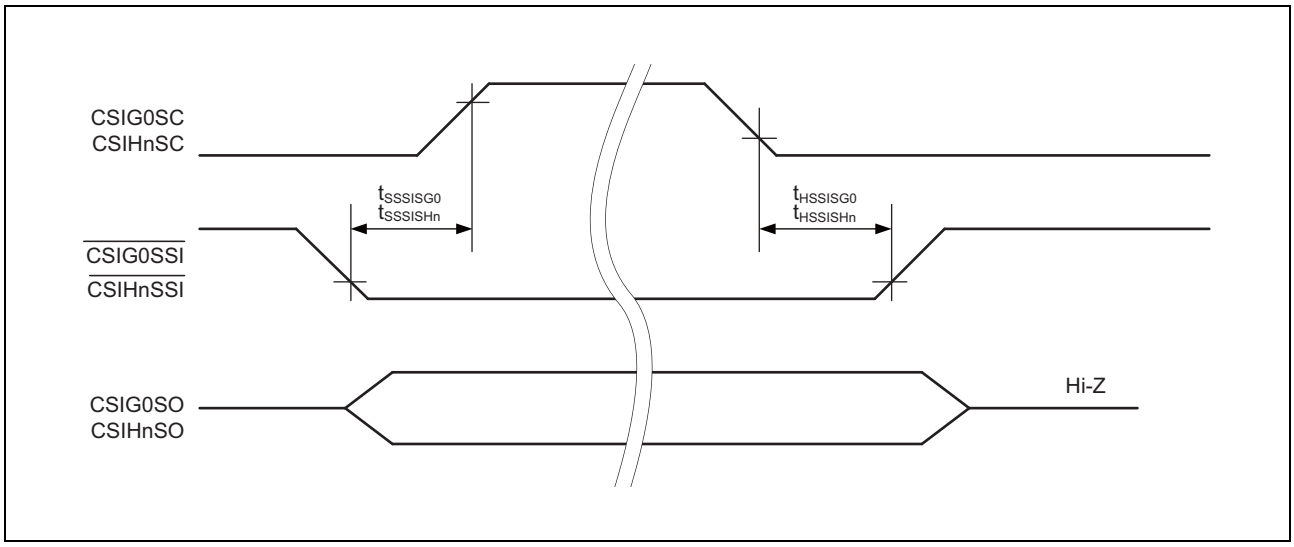
(6) SSI

Slave Mode:

- CSIG (CSIG0CTL1: CSIG0SSE=1, CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 0/0 or 1/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 0/0 or 1/1)



- CSIG (CSIG0CTL1: CSIG0SSE=1, CSIG0CTL1: CSIG0CKR / CSIG0CFG0: CSIG0DAP0 = 1/0 or 0/1)
- CSIH (CSIHnCTL1: CSIHnSSE=1, CSIHnCFGm: CSIHnCKPm / CSIHnCFGm: CSIHnDAPm = 1/0 or 0/1)



1.19 RIIC Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %, CISOVCL: 0.1 µF +/– 30 %,
Ta = –40 to 105°C

Table 1.13 RIIC Timing (Normal Mode)

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				100	kHz
Bus free time (between stop/start condition)	t_{BUF}		4.7			µs
Hold time*1	t_{HD}: STA		4.0			µs
RIIC0SCL clock low-level width	t_{LOW}		4.7			µs
RIIC0SCL clock high-level time	t_{HIGH}		4.0			µs
Setup time for start/restart condition	t_{SU}: STA		4.7			µs
Data hold time	t_{HD}: DAT	CBUS compatible master	5.0			µs
		IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		250			ns
Stop condition setup time	t_{SU}: STO		4.0			µs
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Table 1.14 RIIC Timing (Fast Mode)

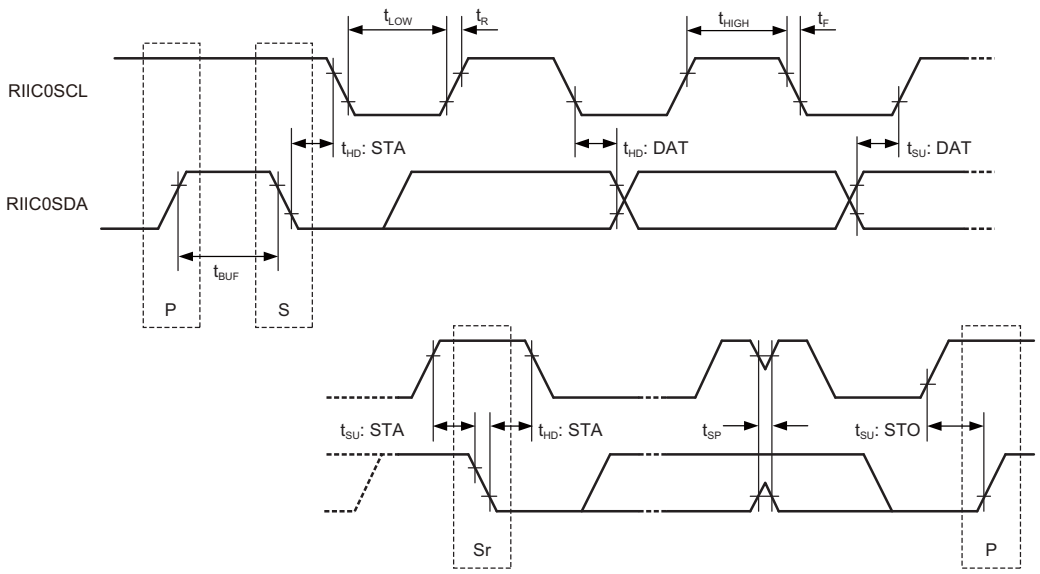
Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
RIIC0SCL clock period	f_{CLK}				400	kHz
Bus free time (between stop/start condition)	t_{BUF}		1.3			µs
Hold time*1	t_{HD}: STA		0.6			µs
RIIC0SCL clock low-level width	t_{LOW}		1.3			µs
RIIC0SCL clock high-level time	t_{HIGH}		0.6			µs
Setup time for start/restart condition	t_{SU}: STA		0.6			µs
Data hold time	t_{HD}: DAT	IIC mode	0*2			µs
Data setup time	t_{SU}: DAT		100*4			ns
Stop condition setup time	t_{SU}: STO		0.6			µs
Pulse width with spike suppressed by input filter	t_{SP}		0		50	ns
Capacitance load of each bus line	Cb				400	pF

Note 1. At the start condition, the first clock pulse Is generated after the hold time.

Note 2. The system requires a minimum of 300 ns hold time internally for the RIIC0SDA signal (at VIH min. of RIIC0SCL signal). In order to occupy the undefined area at the falling edge of RIIC0SCL.

Note 3. If the system does not extend the RIIC0SCL signal low hold time (t_{Low}), only the maximum data hold time (t_{HD}: DAT) needs to be satisfied.

Note 4. The fast mode IIC bus can be used in normal mode IIC bus system. In this case, set the fast mode IIC bus so that it meets the following conditions.
- If the system does not extend the RIIC0SCL signal's low state hold time: t_{SU}: DAT ≥ 250 ns
- If the system extends the RIIC0SCL signal's low state hold time:
Transmit the following data bit to the RIIC0SDA line prior to releasing the RIIC0SCL line (1250 ns: Normal mode IIC bus specification).



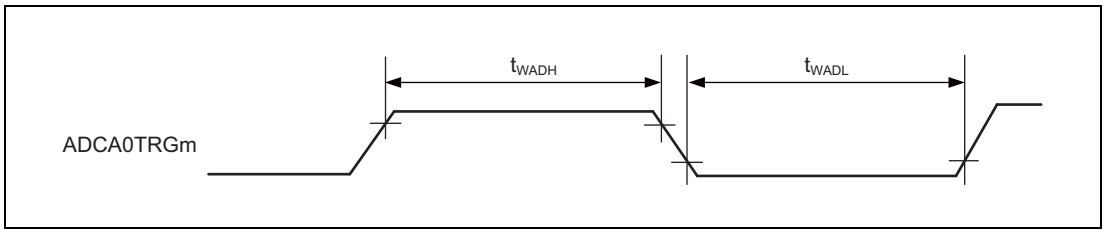
Note: P: Stop condition
S: Start condition
Sr: Restart condition

1.20 ADTRG Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
ADCA0TRGm input high / low level width	t_{WADH} / t_{WADL}		k × Tsamp + 20 *1			ns

Note 1. k: Sampling number of the digital noise filter (DNFA_xxx) for each input.
Tsamp: Sampling time of the digital noise filter (DNFA_xxx) for each input.



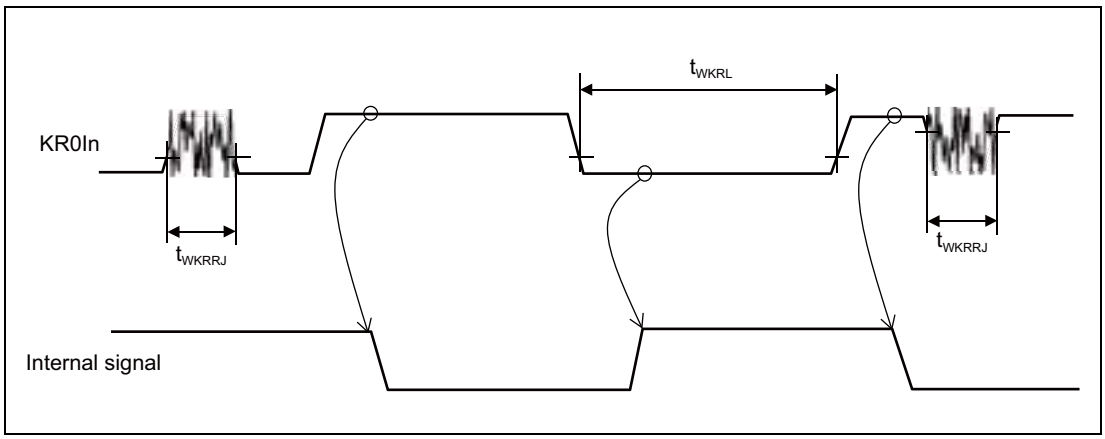
1.21 Key Return Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
KR0In input low level width*1	t_{WKRL}		600			ns
KR0In pulse rejection*2	t_{WKRRJ}		100			ns

Note 1. KR0In input width is needed to ensure that the internal key input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



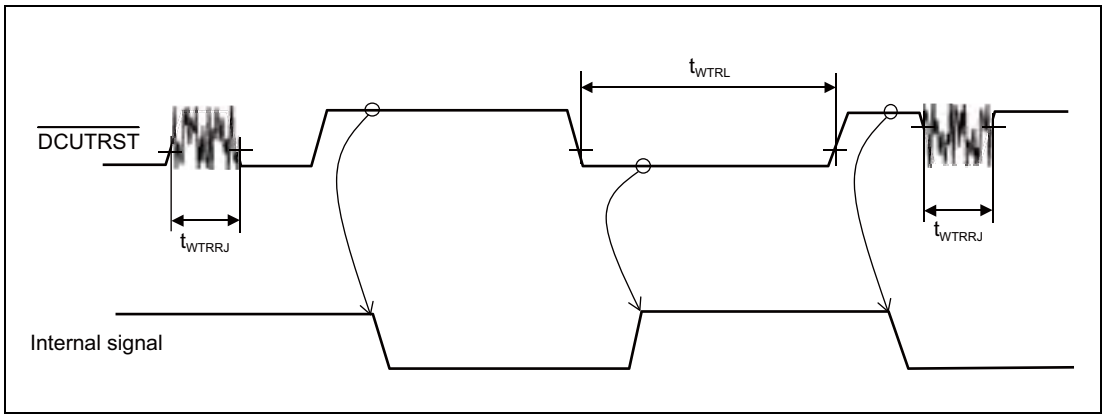
1.22 $\overline{\text{DCUTRST}}$ Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
$\overline{\text{DCUTRST}}$ input low level width*1	t_{WTRL}		600			ns
$\overline{\text{DCUTRST}}$ pulse rejection*2	t_{WTRRJ}		100			ns

Note 1. $\overline{\text{DCUTRST}}$ input width is needed to ensure that the internal DCU reset input signal is activated.

Note 2. Pulses shorter than this minimum is ignored. This is reference value. Noise such as the figure can be filtered.



1.23 Debug Interface Characteristics

1.23.1 Nexus Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1uF +/–30 %, CISOVCL: 0.1uF +/–30 %,
Ta = –40 to 105°C, CL = 30 pF

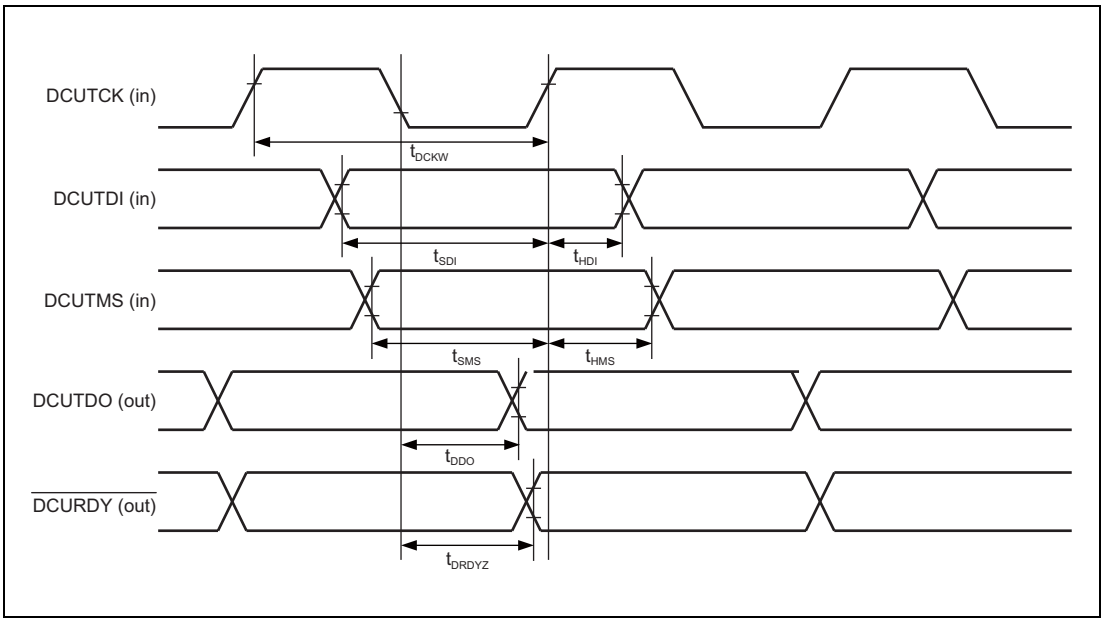
<Input buffer>

DCUTDI, DCUTCK, DCUTMS, $\overline{\text{DCUTRST}}$: TTL

<Output driver strength>

DCUTDO, $\overline{\text{DCURDY}}$: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
DCUTCK cycle width	t_{DCKW}		50			ns
DCUTDI setup time (vs DCUTC K ↑)	t_{SDI}		12			ns
DCUTDI hold time (vs DCUTCK ↑)	t_{HDI}		3			ns
DCUTMS setup time (vs DCUTCK ↑)	t_{SMS}		12			ns
DCUTMS hold time (vs DCUTCK ↑)	t_{HMS}		3			ns
DCUTDO delay time (↓ DCUTCK)	t_{DDO}		0		20	ns
$\overline{\text{DCURDY}}$ delay time (↓ DCUTCK)	t_{RDYZ}		0		20	ns



1.23.2 LPD (4 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

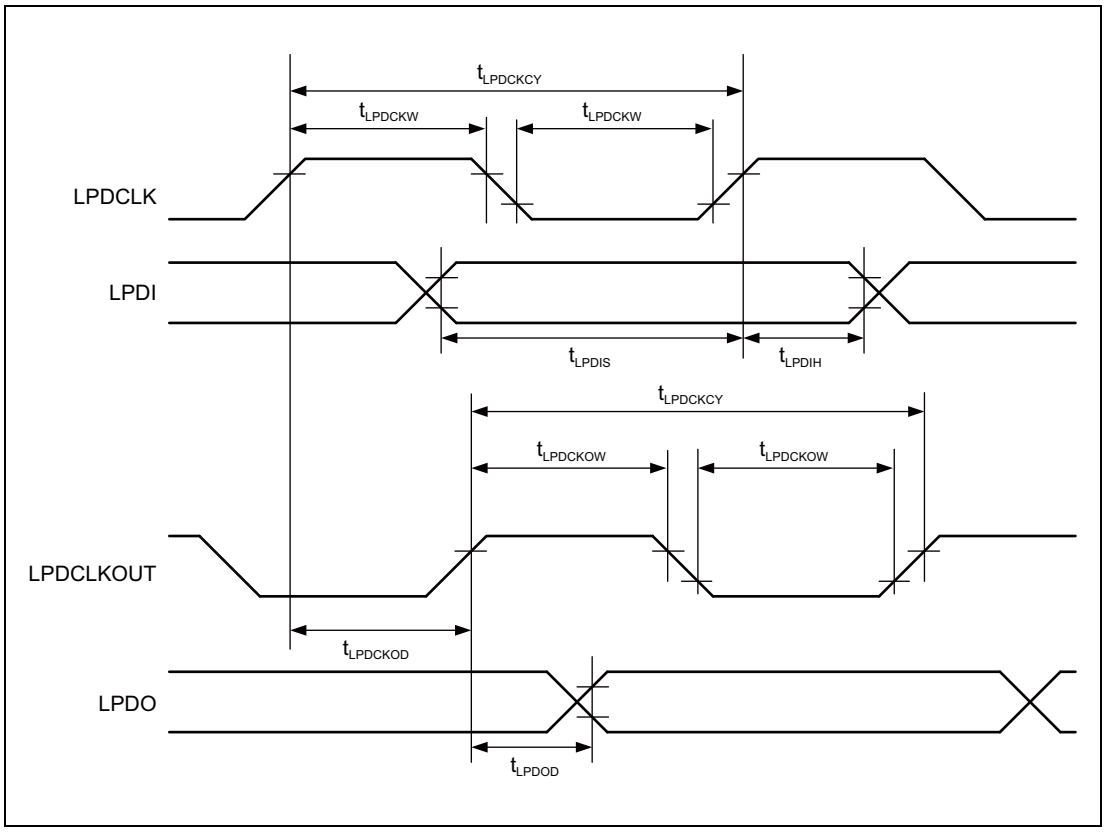
<Input buffer>

LPDCLK, LPDI: TTL

<Output driver strength>

LPDCLKOUT, LPDO: Fast mode

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPDCLK cycle time/ LPDCLKOUT cycle time	$t_{LPDCLKCY}$		83.3 (max. 12 MHz)			ns
LPDCLK High-level width / LPDCLK Low-level width	t_{LPDCKW}		0.5 × $t_{LPDCLKCY}$ – 10			ns
LPDCLKOUT High-level width / LPDCLKOUT low-level width	$t_{LPDCKOW}$		t_{LPDCKW} – 10			ns
LPDI setup time (LPDCLK ↑)	t_{LPDIS}		41			ns
LPDI hold time (LPDCLK ↑)	t_{LPDIH}		3			ns
LPDCLK to LPDCLKOUT delay time	$t_{LPDCKOD}$				44	ns
LPDO delay time (LPDCLKOUT ↑)	t_{LPDOD}		0		15	ns



1.23.3 LPD (1 pin) Interface Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 50 pF

<Input buffer>

LPDIO: TTL

<Output driver strength>

LPDIO: Fast mode

<External pull-up resistor>

LPDIO: 4.7 kΩ to 10 kΩ

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
LPD (1 pin) baud rate					2.0	Mbps

1.24 Flash Programming Characteristics

1.24.1 Code Flash

The code flash memory is shipped in the erase state. If the code flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting i the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Table 1.15 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention: 20 years*2	1000			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 1000), the device can be erased “n” times for each block. For example, when a block of 32 KB is erased after 256 bytes of writing have been performed for different addresses 128 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful ensure of the code flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.16 Programming Characteristics (1/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz CWRT < 100 times	256 B		0.4*1	6*1	ms
			8 KB		20	90	ms
			32 KB		80	360	ms
			256 KB		0.6	2.7	s
			384 KB		0.9	4.1	s
			512 KB		1.2	5.4	s
			768 KB		1.7	8.1	s
			1 MB		2.3	10.8	s
			1.5 MB		3.4	16.2	s
			2 MB		4.5	21.5	s
			3 MB		6.8	32.3	s
			4 MB		9	43	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	256 B		0.5*1	7.2*1	ms
			8 KB		24	108	ms
			32 KB		96	432	ms
			256 KB		0.7	3.3	s
			384 KB		1.1	4.9	s
			512 KB		1.4	6.5	s
			768 KB		2.1	9.8	s
			1 MB		2.7	13	s
			1.5 MB		4.1	19.5	s
			2 MB		5.4	26	s
			3 MB		8.1	39	s
			4 MB		10.8	52	s

Table 1.16 Programming Characteristics (2/2)

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Erase time		f_{PCLK} ≥ 20MHz CWRT < 100 times	8 KB		39	120	ms
			32 KB		141	480	ms
			256 KB		1.2	3.5	s
			384 KB		1.7	5.3	s
			512 KB		2.3	7	s
			768 KB		3.4	10.5	s
			1 MB		4.5	14	s
			1.5 MB		6.8	21	s
			2 MB		9	28	s
			3 MB		13.6	42	s
			4 MB		18.1	56	s
		f_{PCLK} ≥ 20 MHz CWRT ≥ 100 times	8 KB		47	144	ms
			32 KB		169	576	ms
			256 KB		1.4	4.2	s
			384 KB		2.1	6.3	s
			512 KB		2.7	8.4	s
			768 KB		4.1	12.6	s
			1 MB		5.4	16.8	s
			1.5 MB		8.1	25.2	s
			2 MB		10.8	33.6	s
			3 MB		16.2	50.4	s
			4 MB		21.6	67.2	s

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.24.2 Data Flash

The data flash memory is shipped in the erase state. If the data flash memory is read where it has not been written after ensure (no write condition), an ECC error is generated, resulting i the occurrence of an exception.

Condition: REGVCC = EVCC = VPOC to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Table 1.17 Basic Characteristics

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Operation frequency	f_{PCLK}*3		4*4		30	MHz
Number of rewrites*1	CWRT	Data retention: 20 years*2	125 k			times
		Data retention: 3 years*2	250 k			times

Note 1. The number of rewrites is the number of erasures for each block. When the number of rewrites is “n” (n = 125000), the device can be erased “n” times for each block. For example, when a block of 64 bytes is erased after 4 bytes of writing have been performed for different addresses 16 times, the number of rewrites is counted as 1. However, multiple writing to the same address is not possible with 1 erasure (overwriting prohibited).

Note 2. Retention period under average Ta = 85°C. This is the period starting on completion of a successful erasure of the code flash memory.

Note 3. f_{PCLK} = 1/4 f_{CPUCLK}: System operating frequency for internal flash.

Note 4. Only for program/erase operation.

Table 1.18 Programming Characteristics

Item	Symbol	Condition	Block Size	MIN.	TYP.	MAX.	Unit
Programming time		f_{PCLK} ≥ 20 MHz	4 B		0.16*1	1.7*1	ms
			64 KB		2.79	13.44	s
Erasure time		f_{PCLK} ≥ 20 MHz	64 B		1.7*1	10*1	ms
			64 KB		1.74	10.24	s
Blank check time		f_{PCLK} ≥ 20 MHz	4 B			30*1	µs
			64 B			100*1	µs
			64 KB			70.4	ms

Note 1. Only the processing time of the hardware. The overhead required by the software is not included.

1.24.3 Serial Programming Interface

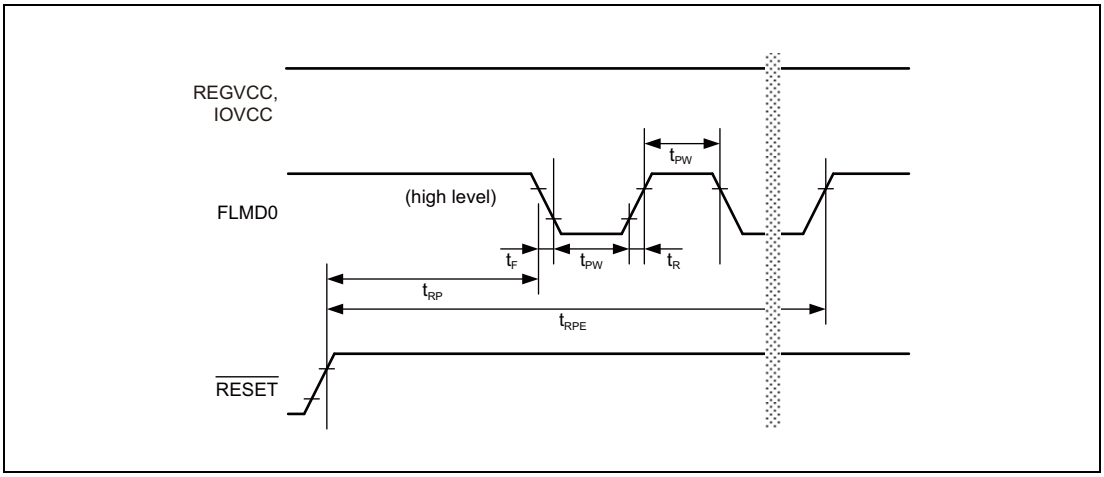
1.24.3.1 Serial Programmer Setup Timing

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLMD0 pulse input start time	t_{RP}		1.5			ms
FLMD0 pulse input end time	t_{RPE}				101.5	ms
FLMD0 low/high level width	t_{PW}		1.6			µs
FLMD0 rise time	t_R				20	ns
FLMD0 fall time	t_F				20	ns

NOTE

IOVCC: EVCC = A0VREF



1.24.3.2 FLSCI3 Interface

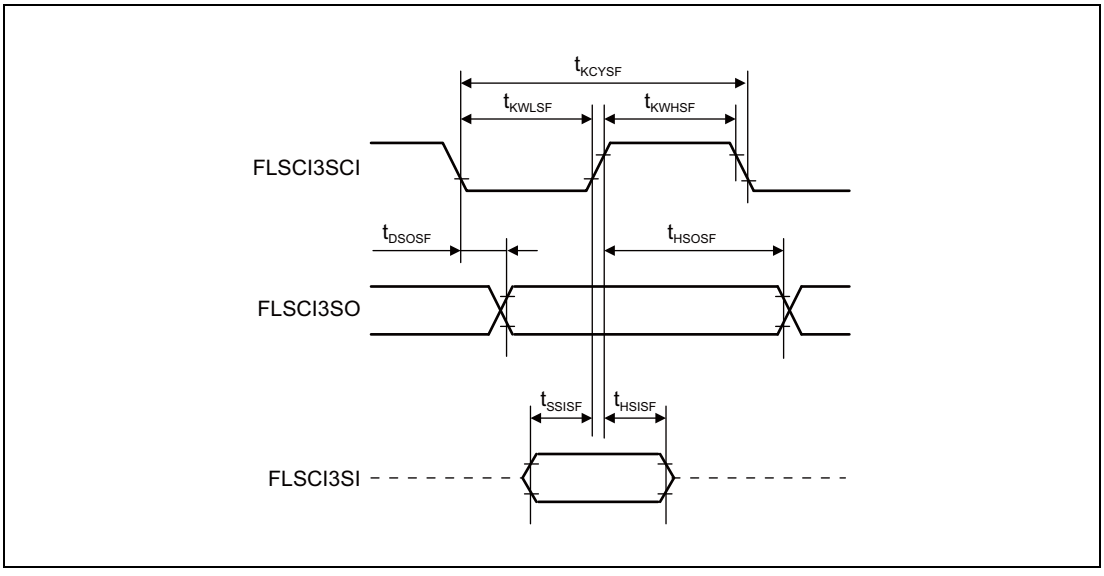
Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

Item	Symbol	Condition	MIN.	TYP.	MAX.	Unit
FLSCI3 transfer rate		1-wired UART mode			1	Mbps
		2-wired UART mode			1.5	Mbps
FLSCI3SCI cycle time	t_{KCYSF}	3-wired Clock Sync mode	200*[1]			ns
FLSCI3SCI high level width	t_{KWHSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SCI low level width	t_{KWLSF}	3-wired Clock Sync mode	t_{KCYSF} / 2 – 15			ns
FLSCI3SI setup time (vs FLSCI3SCI)	t_{SSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SI hold time (vs FLSCI3SCI)	t_{HSISF}	3-wired Clock Sync mode	55			ns
FLSCI3SO output delay (vs FLSCI3SCI)	t_{DSOSF}	3-wired Clock Sync mode Not continuous transfer (data: 1st bit)			0	ns
		3-wired Clock Sync mode Not continuous transfer (data: except 1st bit)			$-t_{KWHSF} + 3 \times t_{Pcyc} + 36$	ns
FLSCI3SO hold time (vs FLSCI3SCI)	t_{HSOSF}	3-wired Clock Sync mode	$2 \times t_{Pcyc}$			ns

Note 1. Input the external clock that is more than 6 clocks of PCLK.

NOTE

t_{Pcyc} is period of PCLK.



1.25 A/D Converter Characteristics

Condition: REGVCC = EVCC = 3.0 V to 5.5 V, A0VREF = 3.0 V to 5.5 V,
AWOVSS = ISOVSS = EVSS = A0VSS = 0 V, CAWOVCL: 0.1 µF +/– 30 %,
CISOVCL: 0.1 µF +/– 30 %, Ta = –40 to 105°C, CL = 30 pF

(1/2)

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Conversion clock	ADCLK0			8*2		40	MHz
Resolution	RES0	12-bit mode		12	12	12	bit
		10-bit mode		10	10	10	bit
Conversion time	t_{CON0}	ADCA0SMPCR.SMPT[7:0] = 12H (40 cycle) (8MHz*2 ≤ ADCLK0 ≤ 32 MHz)		1.25		5	µs
		ADCA0SMPCR.SMPT[7:0] = 18H (46 cycle) (8MHz*2 ≤ ADCLK0 ≤ 40 MHz)		1.15		5.75	µs
		ADCA0SMPCR.SMPT[7:0] = 12H (80 cycle) (8MHz*2 ≤ ADCLK0 ≤ 32 MHz)		2.5		10	µs
		ADCA0SMPCR.SMPT[7:0] = 18H (92 cycle) (8MHz*2 ≤ ADCLK0 ≤ 40MHz)		2.3		11.5	µs
Sampling time	t_{SMP}	ADCA0SMPCR.SMPT[7:0] = 12H (18 cycle) (8MHz*2 ≤ ADCLK0 ≤ 32 MHz)		0.56		2.25	µs
		ADCA0SMPCR.SMPT[7:0] = 18H (24 cycle) (8MHz*2 ≤ ADCLK0 ≤ 40 MHz)		0.6		3	µs
Analog input voltage	VAIN0SN	ADCA0Im		A0VSS		A0VSS	V
Operation current	IA0VREF				1.1	3.0	mA
STOP, DeepSTOP, Cyclic STOP current (@LPS is stopped)	IA0VREFS				1	10	µA
Set up time of self diagnosis voltage circuit	t_{BOOT}			500			ns
Set up time of self diagnosis voltage level	t_{OUT}			500			ns
Pull-down resistor for Discharge mode		ADCA0Im pins, VI = A0VREF		350	500	650	kΩ
Accuracy of Self-diagnosis function	TESH0SN	12-bit mode	Self-diagnosis voltage level = A0VREF	4015 – [TOE0]		4095	—
			Self-diagnosis voltage level = 2/3A0VREF	2651 – [TOE0]	2731	2811 + [TOE0]	—
			Self-diagnosis voltage level = 1/2A0VREF	1968 – [TOE0]	2048	2128 + [TOE0]	—
			Self-diagnosis voltage level = 1/3A0VREF	1285 – [TOE0]	1365	1445 + [TOE0]	—
			Self-diagnosis voltage level = A0VSS	0		80 + [TOE0]	—
		10-bit mode	Self-diagnosis voltage level = A0VREF	1003 – [TOE0]		1023	—
			Self-diagnosis voltage level = 2/3A0VREF	663 – [TOE0]	683	703 + [TOE0]	—
			Self-diagnosis voltage level = 1/2A0VREF	492 – [TOE0]	512	532 + [TOE0]	—
			Self-diagnosis voltage level = 1/3A0VREF	321 – [TOE0]	341	361 + [TOE0]	—
			Self-diagnosis voltage level = A0VSS	0		20 + [TOE0]	—

(2/2)

Item	Symbol	Condition			MIN.	TYP.	MAX.	Unit
Overall error*1	TOE0	12-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±4.0	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±6.0	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±8.0	LSB
		10-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±1.5	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±2.0	LSB
Integral nonlinearity error*1	ILE0	12-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±2.0	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±3.0	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±4.0	LSB
		10-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.0 V to 4.5 V	ADCA0Im			±1.5	LSB
Differential nonlinearity error*1	DLE0	12-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±3.0	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±3.0	LSB
		10-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.0 V to 4.5 V	ADCA0Im			±1.0	LSB
Zero scale error*1 (offset error)	ZSE0	12-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±3.5	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±5.5	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±7.5	LSB
		10-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±0.5	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±1.5	LSB
Full scale error*1	FSE0	12-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±3.5	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±5.5	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±7.5	LSB
		10-bit mode	A0VREF = 4.5 V to 5.5 V	ADCA0Im			±0.5	LSB
			A0VREF = 3.6 V to 4.5 V	ADCA0Im			±1.0	LSB
			A0VREF = 3.0 V to 3.6 V	ADCA0Im			±1.5	LSB

Note 1. This does not include quantization error.

Note 2. Include the oscillation accuracy of HS IntOSC.

CAUTION

When an external digital pulse is applied to AP0, P8, and P9 pins during an A/D conversion this may lead to an A/D conversion result with a larger conversion error as expected due to the coupling noise of the external digital pulse.

The same behavior may apply when the digital buffer is used as output pin. For the output port the potential degradation increases with the driven total output current of the port. In addition the conversion resolution may drop if the output current fluctuates at adjacent pins due to the coupling effect of the external circuit connected to these port pins.

1.26 Injection Currents

Table 1.19 Definition of Pin Group (100 pin)

Symbol	Power Supply for Pin Group	Pin
PgE	EVCC, EVSS	JP0, P0, P20
		P10, P11
PgE'	EVCC, EVSS	P8, P9
PgA0	A0VREF, A0VSS	AP0

Note 1. Do not apply an overvoltage on P8 and P9 pins.

1.26.1 Absolute Maximum Ratings

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJPM}	PgE	Per pin			10	mA
			total			60	mA
		PgE'	Per pin			10	mA
			Total			60	mA
		PgA0	Per pin			10	mA
			total			60	mA
Negative overload current VIN < VSS	I_{INJNM}	PgE	Per pin			–10	mA
			total			–60	mA
		PgE'	Per pin			–10	mA
			Total			–60	mA
		PgA0	Per pin			–10	mA
			total			–60	mA

CAUTIONS

1. The DC injection current (total) must satisfy the specifications of the injection current per pin.
2. In case of injected current for PgA0, TESH0SN cannot be kept. Its deviating value will increase sharply with increasing absolute value of injection current.

1.26.2 DC Characteristics for Overload Current

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Positive overload current VIN > VCC	I_{INJP}	PgE	Per pin			2	mA
			Total			50	mA
		PgE’	Per pin			3	mA
			Total			20	mA
		PgA0	Per pin			3	mA
			Total			20	mA
Negative overload current VIN < VSS	I_{INJN}	PgE	Per pin			–2	mA
			Total			–50	mA
		PgE’	Per pin			–3	mA
			Total			–20	mA
		PgA0	Per pin			–3	mA
			Total			–20	mA

NOTE

These specifications are not tested on sorting and are specified based on the device characterization.

1.26.3 DC Characteristics for Pins Influenced by Injected Current on an Adjacent Pin

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Leakage current coupling factor for positive overload current	K_{INJP}	PgE	Per pin			3.0×10^{-6}	—
		PgE’	Per pin			3.0×10^{-6}	—
		PgA0	Per pin			4.8×10^{-6}	—
Leakage current coupling factor for negative overload current	K_{INJN}	PgE	Per pin			7.5×10^{-6}	—
		PgE’	Per pin			7.5×10^{-6}	—
		PgA0	Per pin			2.6×10^{-6}	—

NOTES

1. This is reference value.
2. An overload current through a pin will cause a certain error current in the adjacent pins. This error current must be added to the respective leakage current (ILIH or ILIL) of the adjacent pins.
3. The amount of error leakage current depends on the overload current and is defined by the overload coupling factor K_{INJ}.
   The total current through a pin is:
   $| I_{total} | = |$ ILIH or ILIL $| + (| I_{INJn} | \times K_{INJn})$

1.26.4 AD Characteristics for Pins Influenced by Injected Current on an Adjacent

Item	Symbol	Condition		MIN.	TYP.	MAX.	Unit
Degradation of overall error*1	I_{INJP}	Par = 3 mA	ADCA0Im			±1.3	LSB
		Total = 20 mA	ADCA0Im			±3.8	LSB
	I_{INJN}	Par = 3 mA	ADCA0Im			±1.4	LSB
		Total = 20 mA	ADCA0Im			±4.5	LSB

Note 1. This value is the degradation by injected current on an adjacent pin. Therefore, this value is added to the specification of A/D converter's overall error defined separately as the electrical specifications.

Note 2. This is reference value.

CAUTION

When there is an increased leakage current on the analog input pins, based on currents injected into the pins adjacent to the converted channel, the effect on the ADC accuracy depends on the external analog source impedance.

[Example] Conditions: A0VREF = 5.0 V, external analog source impedance = 10 kΩ.

If there is a leakage current of 1μA by injected current, the effect on the ADC accuracy is 1 (μA) × 10 k (Ω) / 5 (V) = 0.2%FSR

1.27 Thermal Characteristics

1.27.1 Parameters

Package	Item	Symbol	Estimate	Unit	Note
100 pin LQFP	Thermal Resistance	Θja	39	°C/W	Conforming to JESD51-7 (4 layers)
	Thermal Characterization Parameter	ψjb	29		

Note: The thermal resistance depend on the usage environment.

1.27.2 Assumed Board

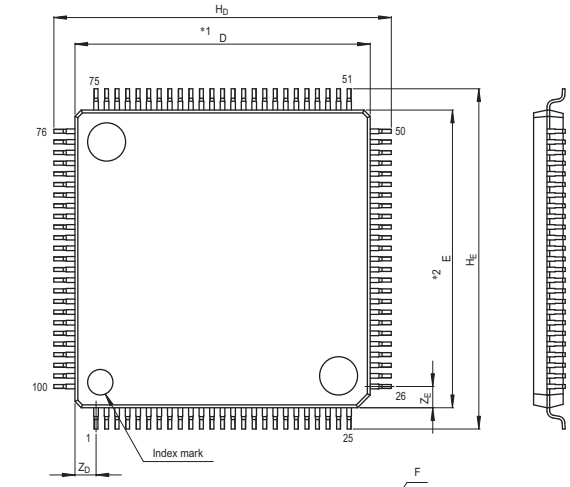
Conforming to JESD51-7 (4 layers)

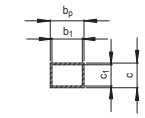
	Board size (mm)		
	X	Y	Area (mm^2)
Boad	76.2	114.3	8709.66
Remaining copper raes	Thickness of conductors		
50-95-95-50%	70-35-35-70 µm		

Section 2 Package Dimensions

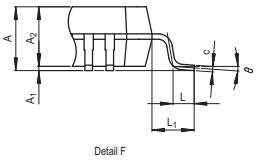
2.1 100 pin

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP100-14x14-0.50	PLQP0100KB-A	100P6Q-A / FP-100U / FP-100UV	0.6g





Terminal cross section



Detail F

NOTE)
1. DIMENSIONS "*1" AND "*2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "*3" DOES NOT INCLUDE TRIM OFFSET.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A_2	—	1.4	—
H_D	15.8	16.0	16.2
H_E	15.8	16.0	16.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.0	—
Z_E	—	1.0	—
L	0.35	0.5	0.65
L_1	—	1.0	—

REVISION HISTORY	RH850/F1H PREMIUM (100 pin Version) Datasheet

Rev.	Date	Description	
		Page	Summary
0.50	Dec 09, 2015	—	First Edition issued
0.51	May 23, 2016	15	correction of 1.8.1 Regulator Characteristics addition of Note 3
		26	correction of High level input voltage
		34	correction of note2 to 1.17 Mode Timing
		68	correction of 1.27.1 Parameters
1.00	Aug 31, 2016	3	correction of Local RAM
		15	deleted of Output voltage
		26	correction of Internal pull-up resistance correction of Internal pull-down resistance
		62	correction of Pull-down resistor for Discharge mode

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