

# RJK1211DNS

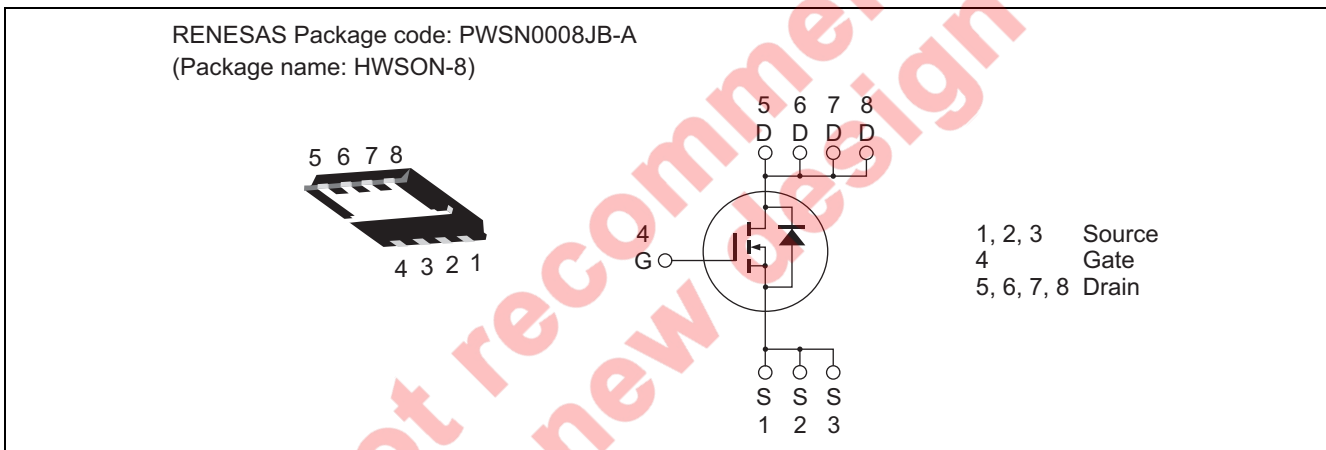
120V, 5A, 130mΩ max.  
Silicon N Channel Power MOS FET  
Power Switching

R07DS0090EJ0400  
Rev.4.00  
Apr 11, 2013

## Features

- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance  
 $R_{DS(on)} = 100\text{ m}\Omega$  typ. (at  $V_{GS} = 10\text{ V}$ )
- Pb-free
- Halogen-free

## Outline



## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

Item	Symbol	Ratings	Unit
Drain to source voltage	$V_{DSS}$	120	V
Gate to source voltage	$V_{GSS}$	+12, -5	V
Drain current	$I_D$	5	A
Drain peak current	$I_{D(pulse)}$ <sup>Note 1</sup>	15	A
Body-drain diode reverse drain current	$I_{DR}$	5	A
Avalanche current	$I_{AP}$ <sup>Note 2</sup>	3	A
Avalanche energy	$E_{AS}$ <sup>Note 2</sup>	0.77	mJ
Channel dissipation	$P_{ch}$ <sup>Note 3</sup>	10	W
Channel to case thermal impedance	$\theta_{ch-c}$ <sup>Note 3</sup>	12.5	$^\circ\text{C}/\text{W}$
Channel temperature	$T_{ch}$	150	$^\circ\text{C}$
Storage temperature	$T_{stg}$	-55 to +150	$^\circ\text{C}$

Notes: 1.  $PW \leq 10\ \mu\text{s}$ , duty cycle  $\leq 1\%$   
 2. Value at  $T_{ch} = 25^\circ\text{C}$ ,  $R_g \geq 50\ \Omega$   
 3.  $T_c = 25^\circ\text{C}$

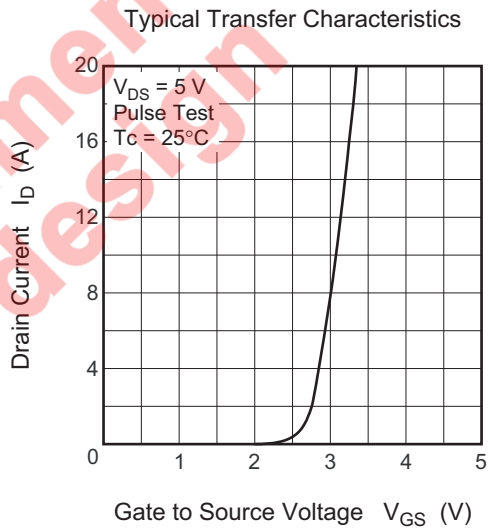
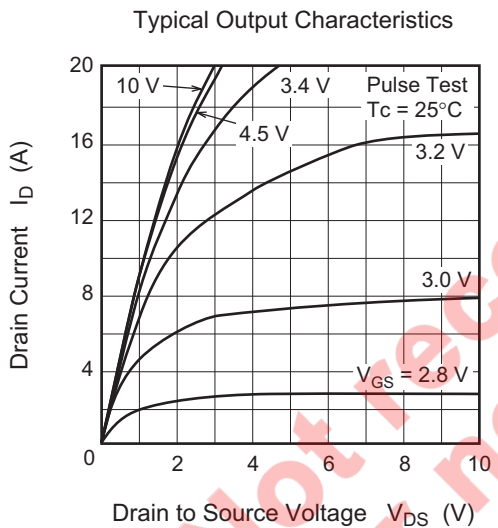
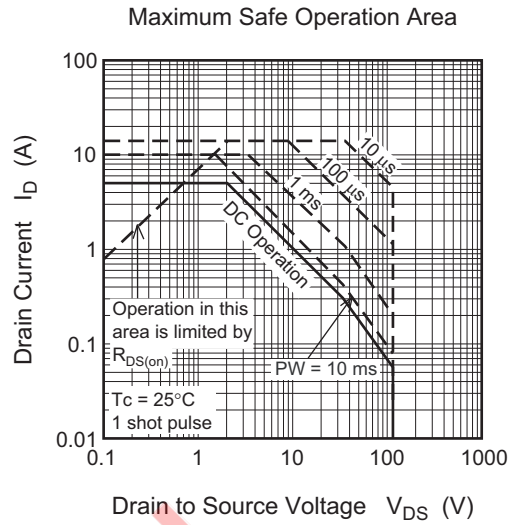
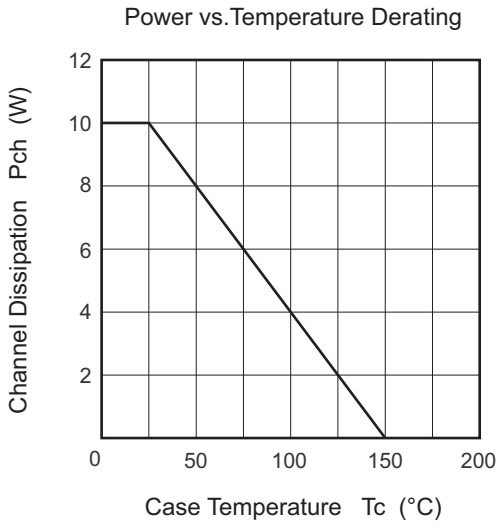
## Electrical Characteristics

(Ta = 25°C)

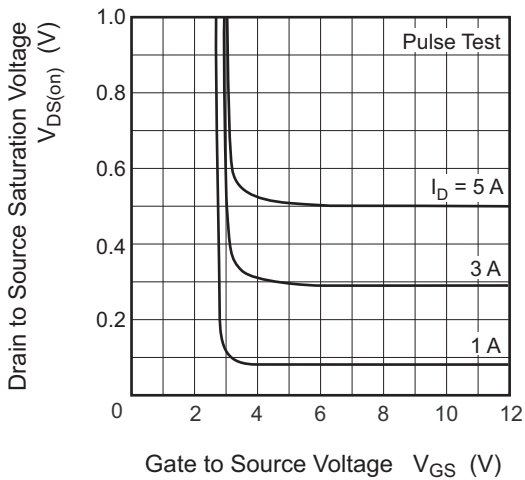
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	120	—	—	V	$I_D = 10 \text{ mA}$ , $V_{GS} = 0$
Gate to source leak current	$I_{GSS}$	—	—	$\pm 0.1$	$\mu\text{A}$	$V_{GS} = +12, -5 \text{ V}$ , $V_{DS} = 0$
Zero gate voltage drain current	$I_{DSS}$	—	—	10	$\mu\text{A}$	$V_{DS} = 120 \text{ V}$ , $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}$ , $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	100	130	$\text{m}\Omega$	$I_D = 2.5 \text{ A}$ , $V_{GS} = 10 \text{ V}$ <sup>Note4</sup>
	$R_{DS(on)}$	—	110	150	$\text{m}\Omega$	$I_D = 2.5 \text{ A}$ , $V_{GS} = 4.5 \text{ V}$ <sup>Note4</sup>
Forward transfer admittance	$ y_{fs} $	—	9.0	—	S	$I_D = 2.5 \text{ A}$ , $V_{DS} = 5 \text{ V}$ <sup>Note4</sup>
Input capacitance	$C_{iss}$	—	1070	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	$C_{oss}$	—	80	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	$C_{rss}$	—	35	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	$R_g$	—	1.7	—	$\Omega$	
Total gate charge	$Q_g$	—	8.0	—	nC	$V_{DD} = 50 \text{ V}$
Gate to source charge	$Q_{gs}$	—	3.0	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	$Q_{gd}$	—	2.0	—	nC	$I_D = 5 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	7.8	—	ns	$V_{GS} = 10 \text{ V}$ , $I_D = 2.5 \text{ A}$
Rise time	$t_r$	—	2.8	—	ns	$V_{DD} \cong 30 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	38	—	ns	$R_L = 12 \Omega$
Fall time	$t_f$	—	2.7	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	$V_{DF}$	—	0.83	1.1	V	$I_F = 5 \text{ A}$ , $V_{GS} = 0$ <sup>Note4</sup>
Body-drain diode reverse recovery time	$t_{rr}$	—	40	—	ns	$I_F = 5 \text{ A}$ , $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

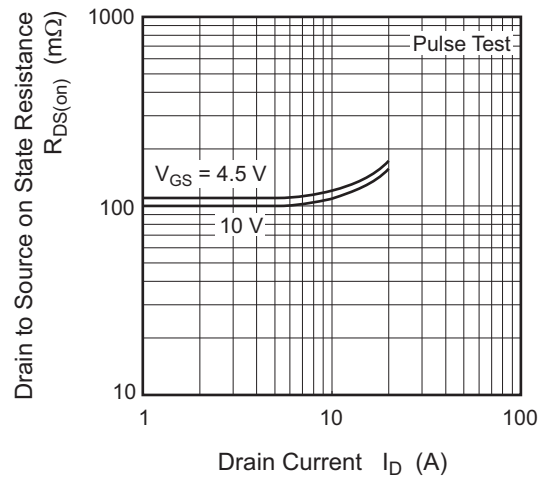
Main Characteristics



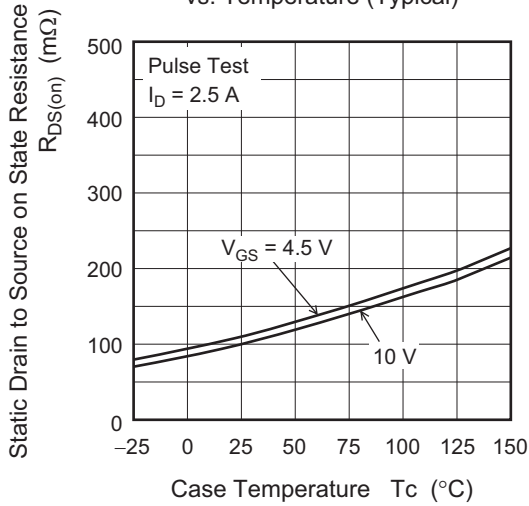
Drain to Source Saturation Voltage vs. Gate to Source Voltage



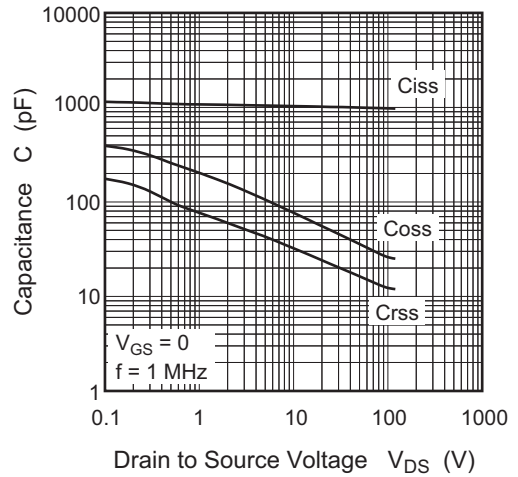
Static Drain to Source on State Resistance vs. Drain Current (Typical)



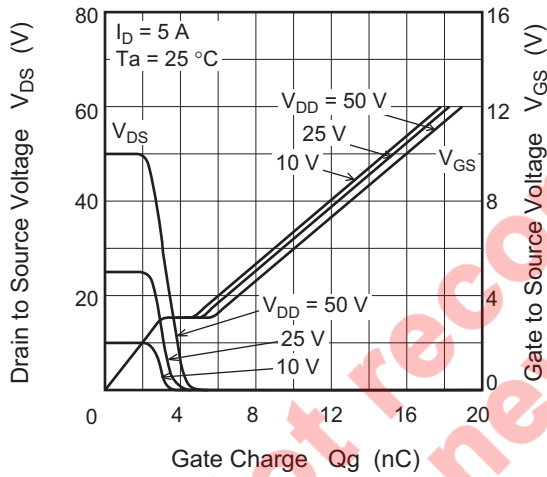
Static Drain to Source on State Resistance vs. Temperature (Typical)



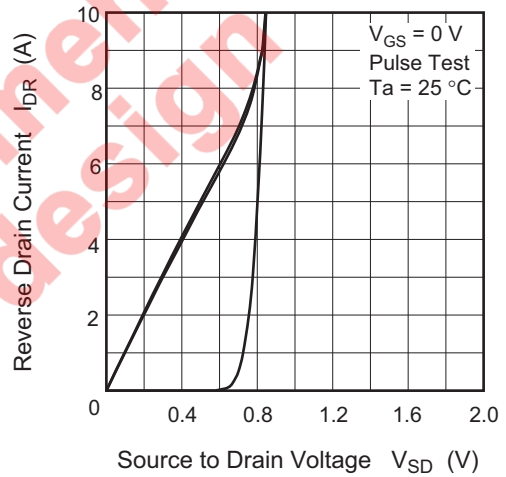
Typical Capacitance vs. Drain to Source Voltage (Typical)



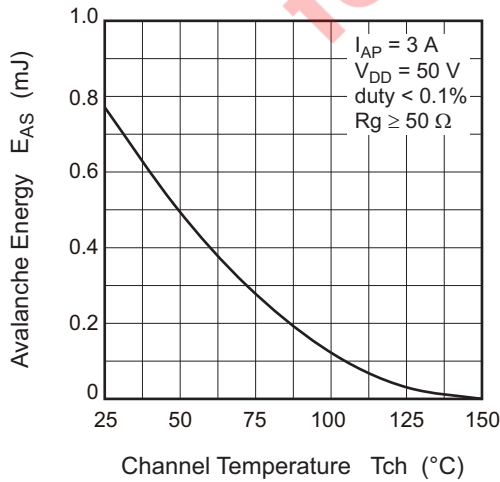
Dynamic Input Characteristics (Typical)

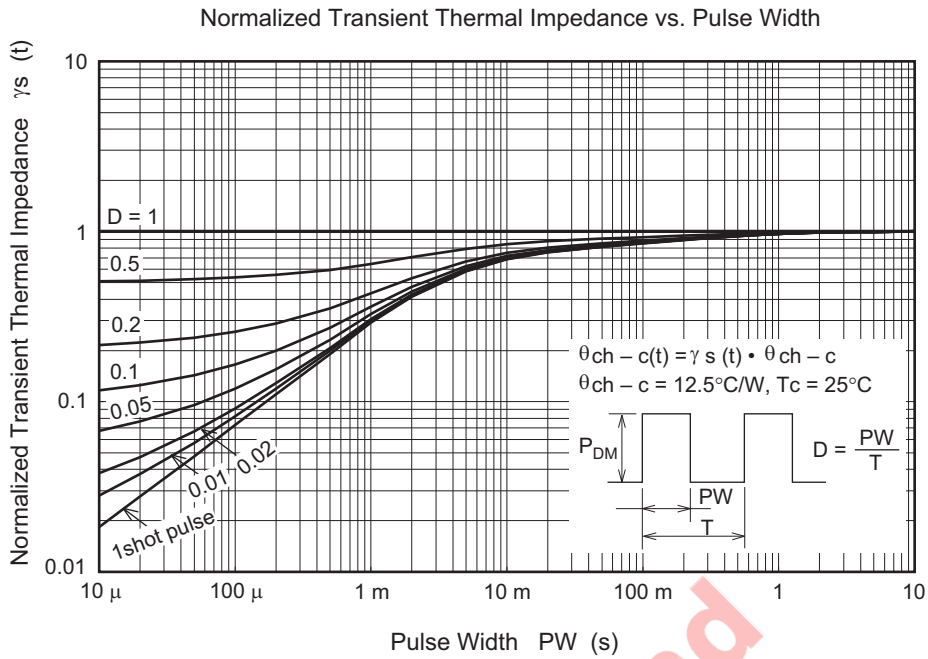


Reverse Drain Current vs. Source to Drain Voltage

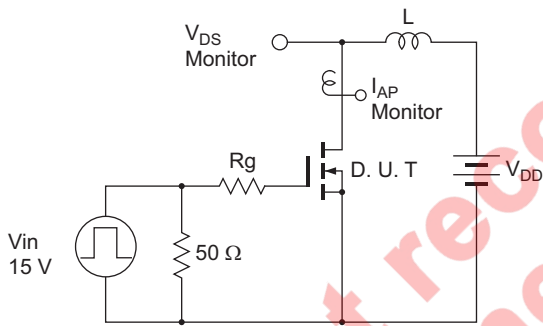


Maximum Avalanche Energy vs. Channel Temperature Derating

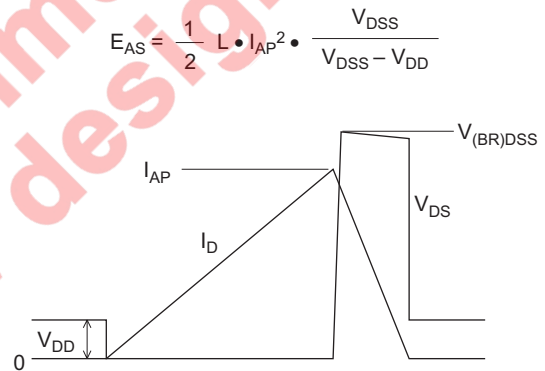




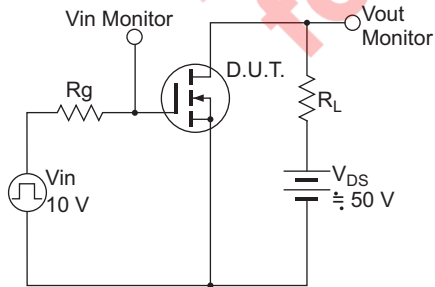
Avalanche Test Circuit



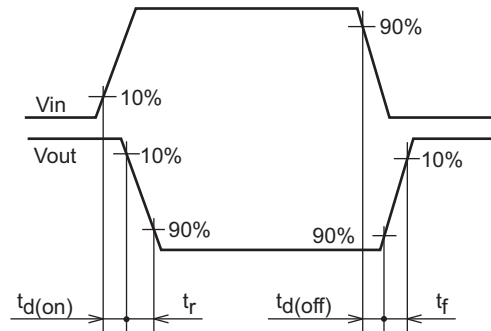
Avalanche Waveform



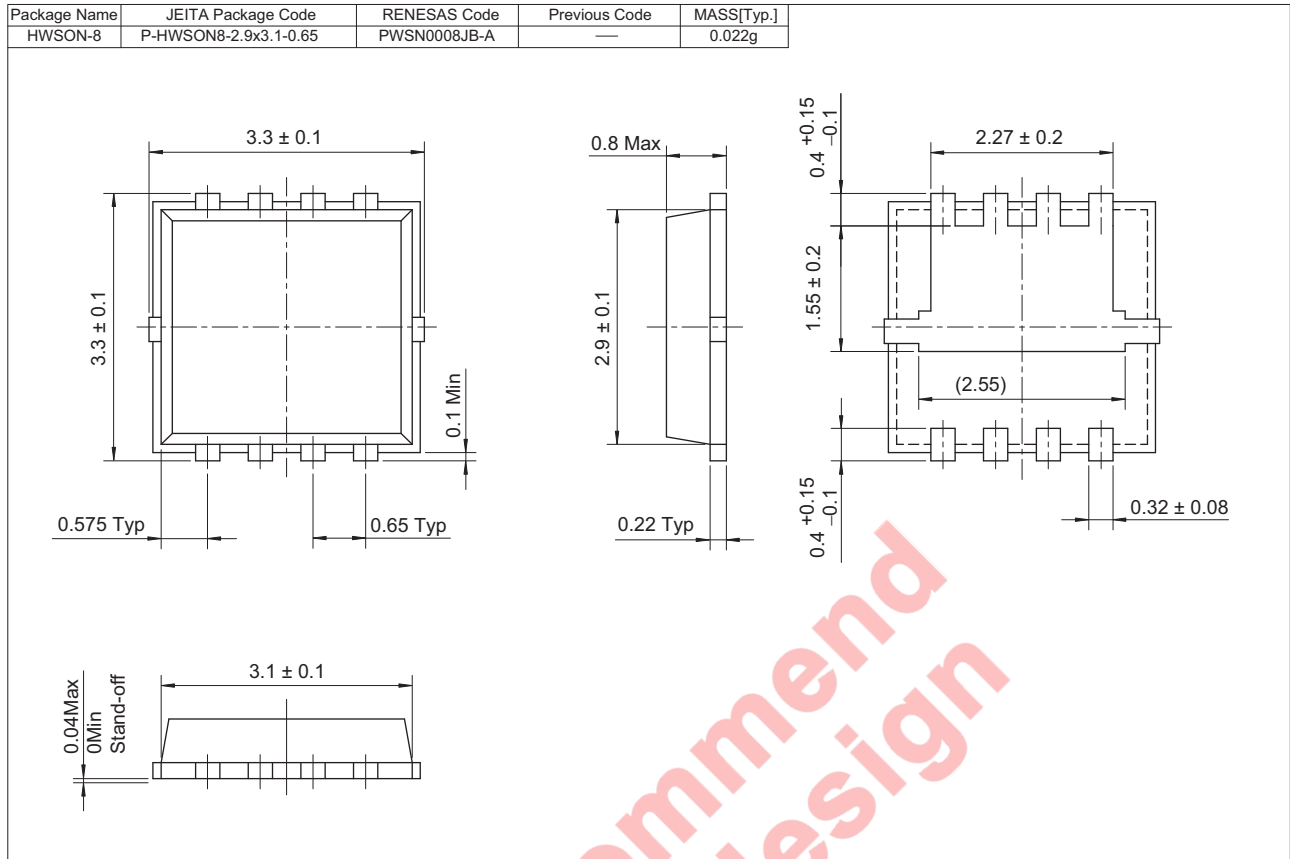
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK1211DNS-00-J5	5000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

Not recommended for new design

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