

RJK4034DJE

400V - 1.6A - MOS FET
High Speed Power Switching

R07DS0864EJ0100

Rev.1.00

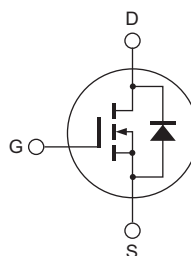
Aug 10, 2012

Features

- Low on-state resistance
 $R_{DS(on)} = 3.7 \Omega$ typ. (at $I_D = 0.8 \text{ A}$, $V_{GS} = 10 \text{ V}$, $T_a = 25^\circ\text{C}$)
- Low drive current
- High speed switching

Outline

RENESAS Package code: PRSS0003DC-A
(Package name: TO-92 Mod)



1. Source
2. Drain
3. Gate

Absolute Maximum Ratings

($T_a = 25^\circ\text{C}$)

Item	Symbol	Value	Unit
Drain to source voltage	V_{DSS}	400	V
Gate to source voltage	V_{GSS}	± 30	V
Drain current	I_D ^{Note1}	1.6	A
Drain peak current	$I_{D(pulse)}$ ^{Note2}	3.2	A
Body-drain diode reverse drain current	I_{DR} ^{Note1}	1.6	A
Body-drain diode reverse drain peak current	$I_{DR(pulse)}$ ^{Note2}	3.2	A
Channel dissipation	P_{ch} ^{Note 3}	0.9	W
Channel to ambient thermal Impedance	θ_{ch-a}	139	$^\circ\text{C/W}$
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

- Notes: 1. Limited by T_{ch} max.
2. Pulse width limited by safe operating area.
3. Value at $T_c = 25^\circ\text{C}$

Electrical Characteristics

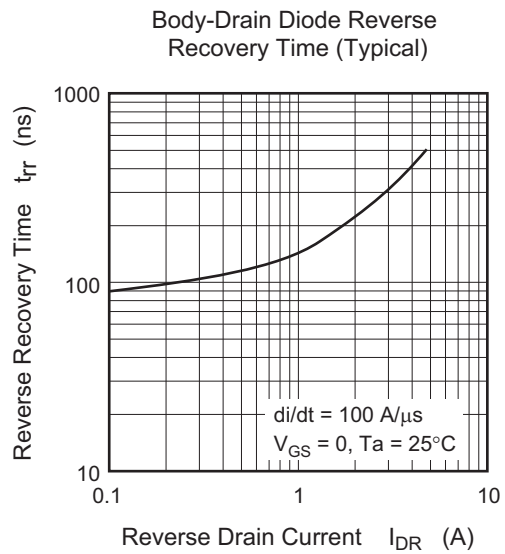
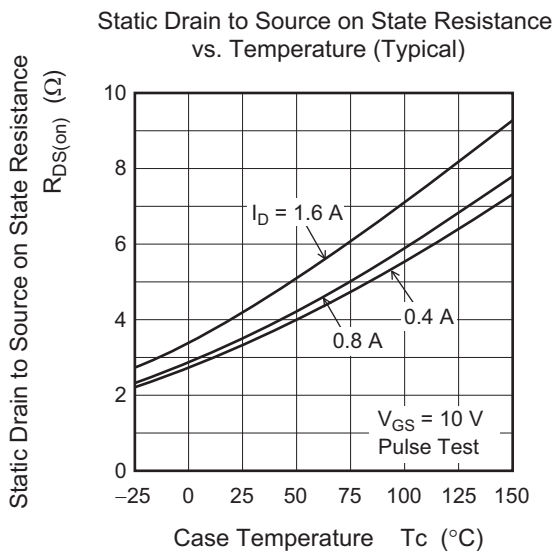
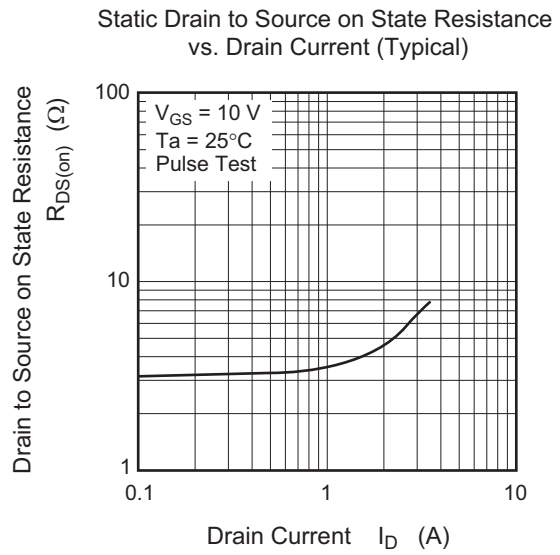
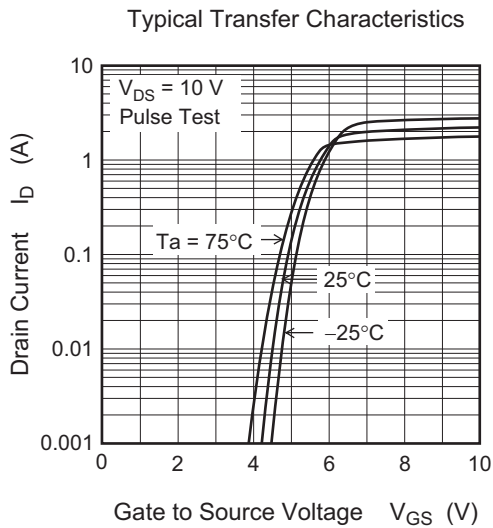
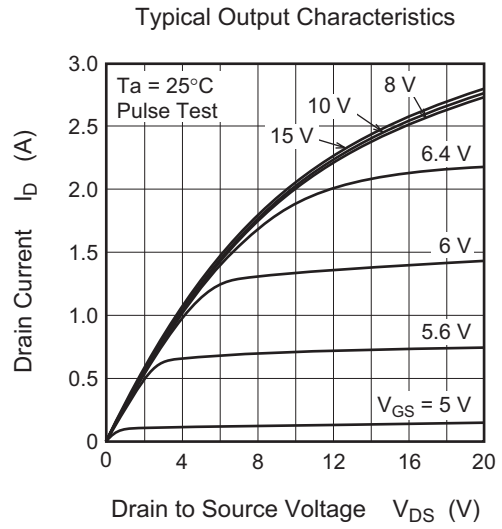
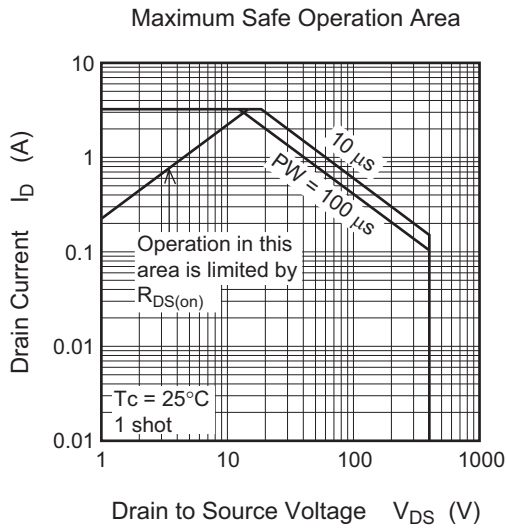
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	400	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 400 \text{ V}$, $V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}$, $V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3	—	5	V	$V_{DS} = 10 \text{ V}$, $I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	3.7	4.5	Ω	$I_D = 0.8 \text{ A}$, $V_{GS} = 10 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	117	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	C_{oss}	—	18	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	2	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	$t_{d(on)}$	—	11	—	ns	$I_D = 0.8 \text{ A}$
Rise time	t_r	—	11	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	18	—	ns	$R_L = 300 \Omega$
Fall time	t_f	—	54	—	ns	$R_g = 10 \Omega$
Total gate charge	Q_g	—	4.9	—	nC	$V_{DD} = 360 \text{ V}$
Gate to source charge	Q_{gs}	—	1.0	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.8	—	nC	$I_D = 1.6 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.87	1.45	V	$I_F = 1.6 \text{ A}$, $V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	193	—	ns	$I_F = 1.6 \text{ A}$, $V_{GS} = 0$ $di_F/dt = 100 \text{ A}/\mu\text{s}$

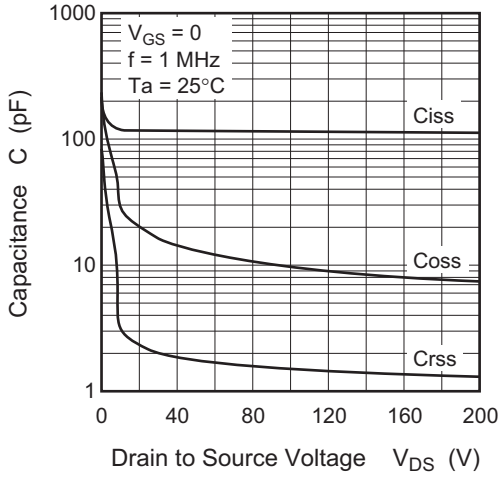
Note: 4. Pulse test

5. Since this device is equipped with high voltage FET chip ($V_{DSS} \geq 400 \text{ V}$), high voltage may be supplied. Therefore, please be sure to confirm about Electric discharge between Drain terminal and other terminal.
6. This device is sensitive to electrostatic discharge.
It is recommended to adopt appropriate cautions when handling this product.

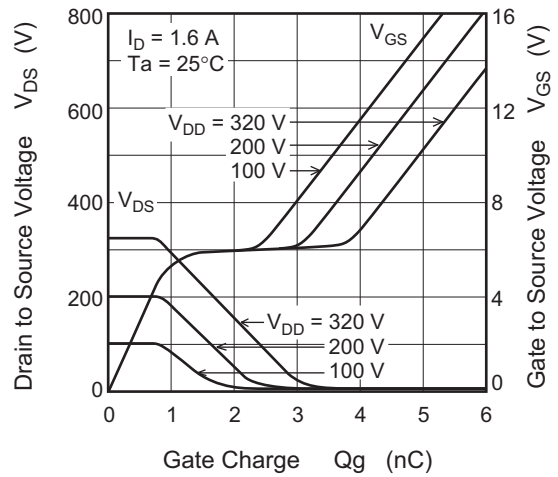
Main Characteristics



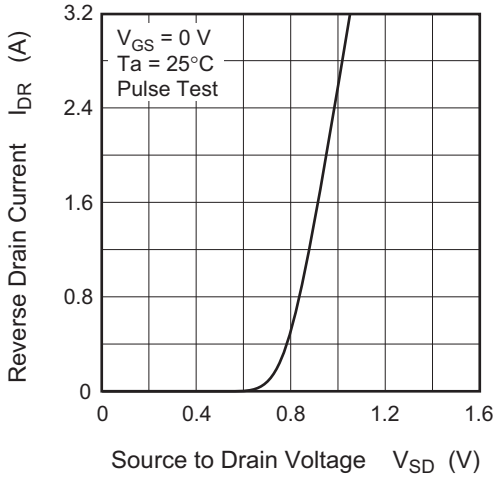
Typical Capacitance vs. Drain to Source Voltage



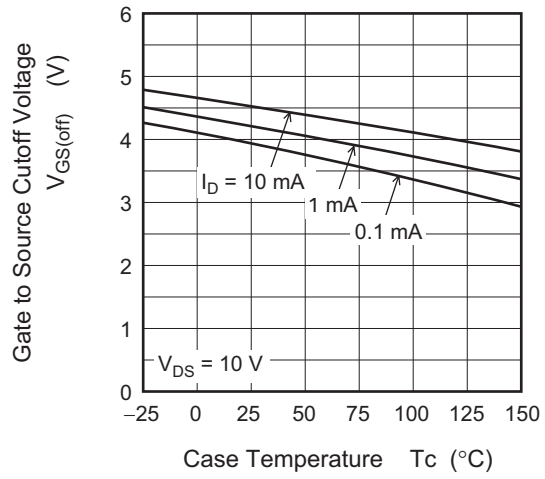
Dynamic Input Characteristics (Typical)



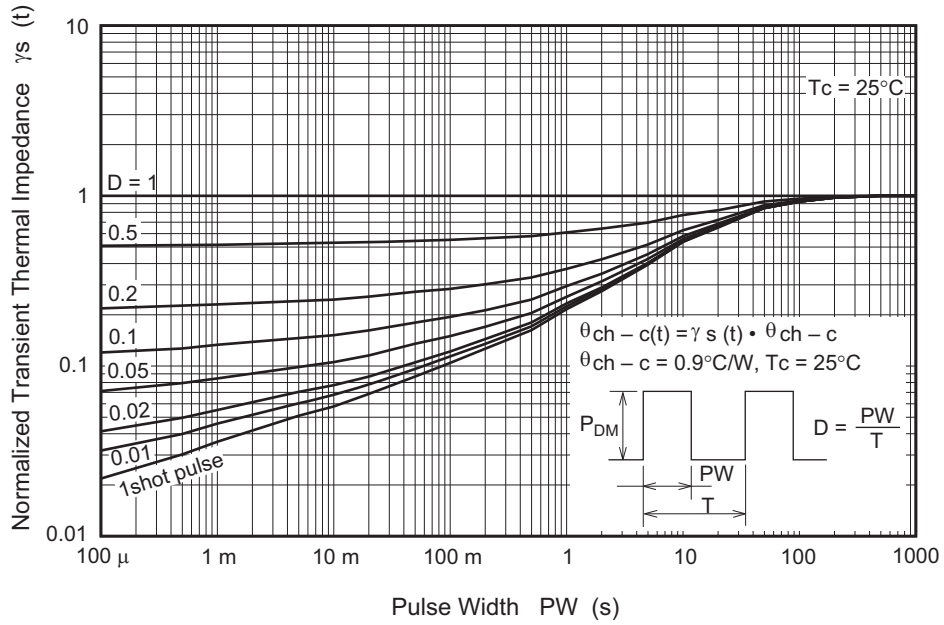
Reverse Drain Current vs. Source to Drain Voltage (Typical)



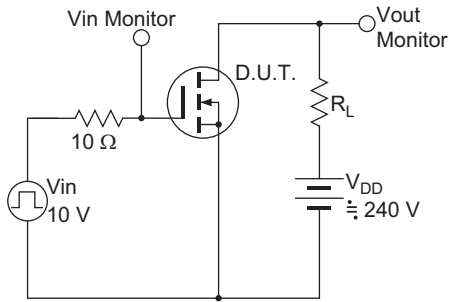
Gate to Source Cutoff Voltage vs. Case Temperature (Typical)



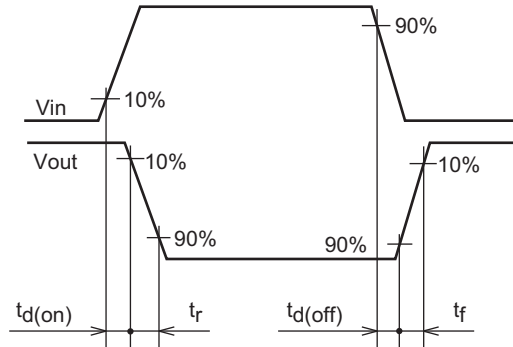
Normalized Transient Thermal Impedance vs. Pulse Width



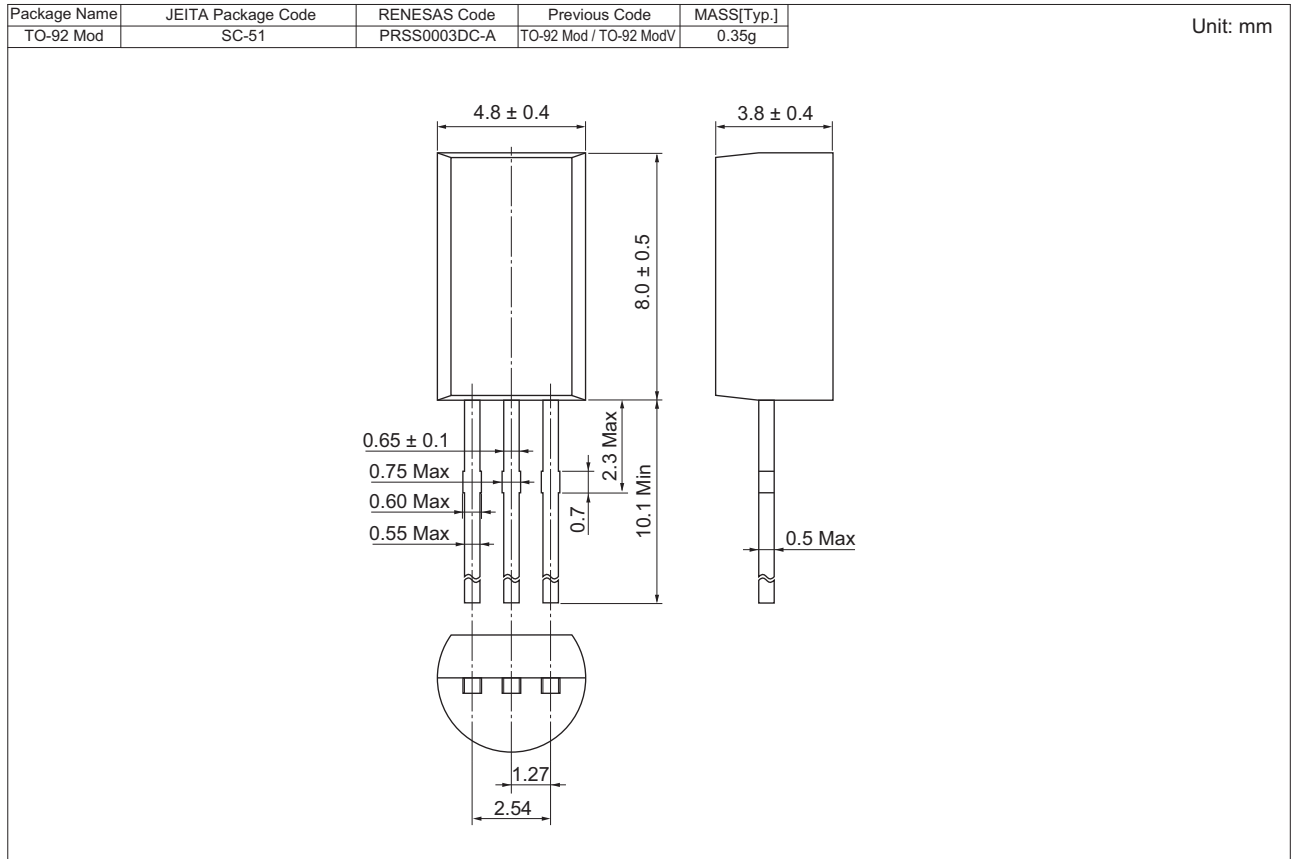
Switching Time Test Circuit



Waveform



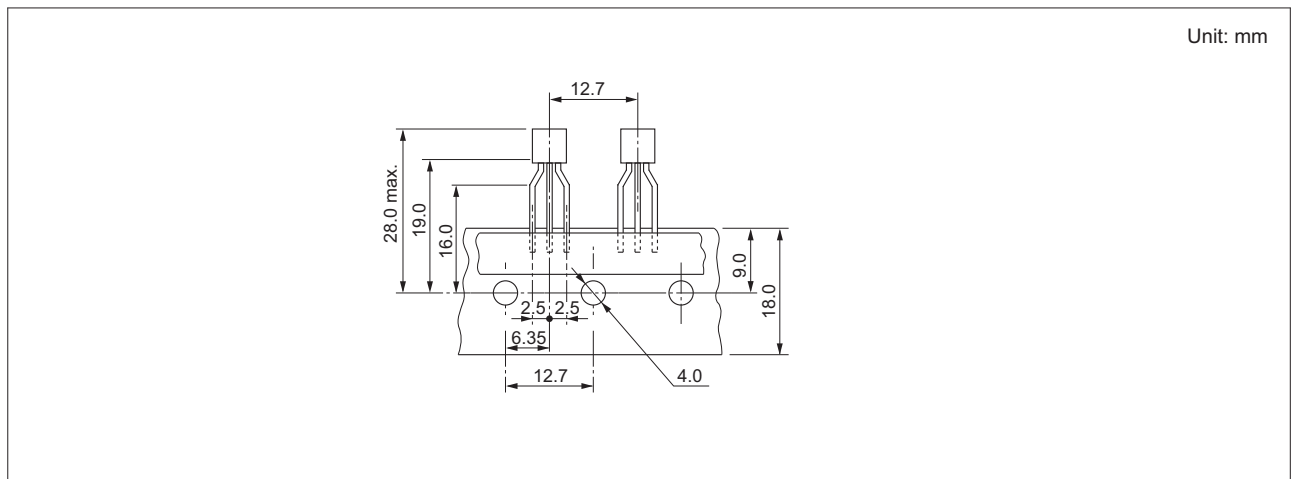
Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK4034DJE-00#Z0	2500 pcs	Taping

Note: Leads is forming applied as following figure.



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