

RL78/G22

R01DS0424EJ0110

RENESAS MCU

Rev.1.10

Jun 12, 2024

True low-power platform, 37.5- $\mu$ A/MHz operating current, 200-nA stop current, 32-/64-KB code flash memory and 4-KB RAM, up to 29 capacitive touch sensors, from 16 to 48 pins, 1.6 to 5.5 V

## 1. Outline

### 1.1 Features

Ultra-low power consumption technology

- VDD = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode
  - High-speed wakeup from the STOP mode is possible.
- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- The minimum instruction execution time can be changed from high to ultra-low speed.
  - High speed: 0.03125  $\mu$ s at 32-MHz operation with the high-speed on-chip oscillator clock
  - Ultra-low speed: 30.5  $\mu$ s at 32.768-kHz operation with the subsystem clock
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers: (8-bit register  $\times$  8)  $\times$  4 banks
- On-chip RAM: 4 KB

Code flash memory

- Code flash memory: 32 or 64 KB
- Block size: 2 KB
- Security function: Prohibition of block erase and rewriting
- On-chip debugging
- Self-programming with boot swapping and flash shield window

Data flash memory

- Data flash memory: 2 KB
- Background operation (BGO): Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator

- Selectable from among 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, and 1 MHz
- High accuracy:  $\pm 1.0\%$  (VDD = 1.8 to 5.5 V, TA = -20 to +85°C)

Middle-speed on-chip oscillator

- Selectable from among 4 MHz, 2 MHz, and 1 MHz with adjustability

Low-speed on-chip oscillator

- 32.768 kHz (typ.) with adjustability

Operating ambient temperature

- TA = -40 to +85°C (2D: Consumer applications)
- TA = -40 to +105°C (3C: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detectors (LVD0 and LVD1)

Data transfer controller (DTC)

- Transfer modes: Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

SNOOZE mode sequencer (SMS)

- Calculations and comparison of values by the commands for use in processing by the sequencer can realize intermittent operations where the RL78/G22 does not have to return to normal operation.
- Sequentially handling a total of 32 processes with the use of desired commands from among 21 different ones
- The SNOOZE mode sequencer offers operation with low power consumption without using the CPU, flash memory, and RAM.

## Event link controller (ELC)

- Event signals can be set up between specified peripheral functions.

## Serial interface

- Simplified SPI (CSI<sup>Note</sup>): 1 to 5 channels
- UART/UART (LIN-bus supported)/UARTA: 1 to 4 channels
- I<sup>2</sup>C/Simplified I<sup>2</sup>C: 2 to 6 channels

## Timers

- 16-bit timer: 8 channels
- 32-bit interval timer: 1 channel in 32-bit counter mode  
2 channels in 16-bit counter mode  
4 channels in 8-bit counter mode
- Realtime clock: 1 channel (counting of one second to 99 years, alarm interrupt, and clock correction)
- Watchdog timer: 1 channel (operates with the dedicated low-speed on-chip oscillator clock)

## A/D converter

- 8-/10-bit resolution A/D converter
- Analog input: 3 to 10 channels
- Internal reference voltage (1.48 V) and temperature sensor

## Capacitive sensing unit

- Operating voltage: V<sub>DD</sub> = 1.8 to 5.5 V
- Self-capacitance method: A single pin configures a single key, supporting up to 29 keys
- Mutual capacitance method: Matrix configuration with 8 × 8 pins, supporting up to 64 keys

## Input/output port pins

- Number of port pins: 12 to 44  
N-ch open drain I/O pins [withstand voltage of 6 V]: 0 to 4  
N-ch open drain I/O pins [withstand voltage of V<sub>DD</sub>]: 4 to 13
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

## Others

- Binary-coded decimal (BCD) correction circuit
- Key interrupt input
- Clock output/buzzer output controller

**Note** Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

**Remark** The functions mounted depend on the product. See **1.6 Outline of Functions**.

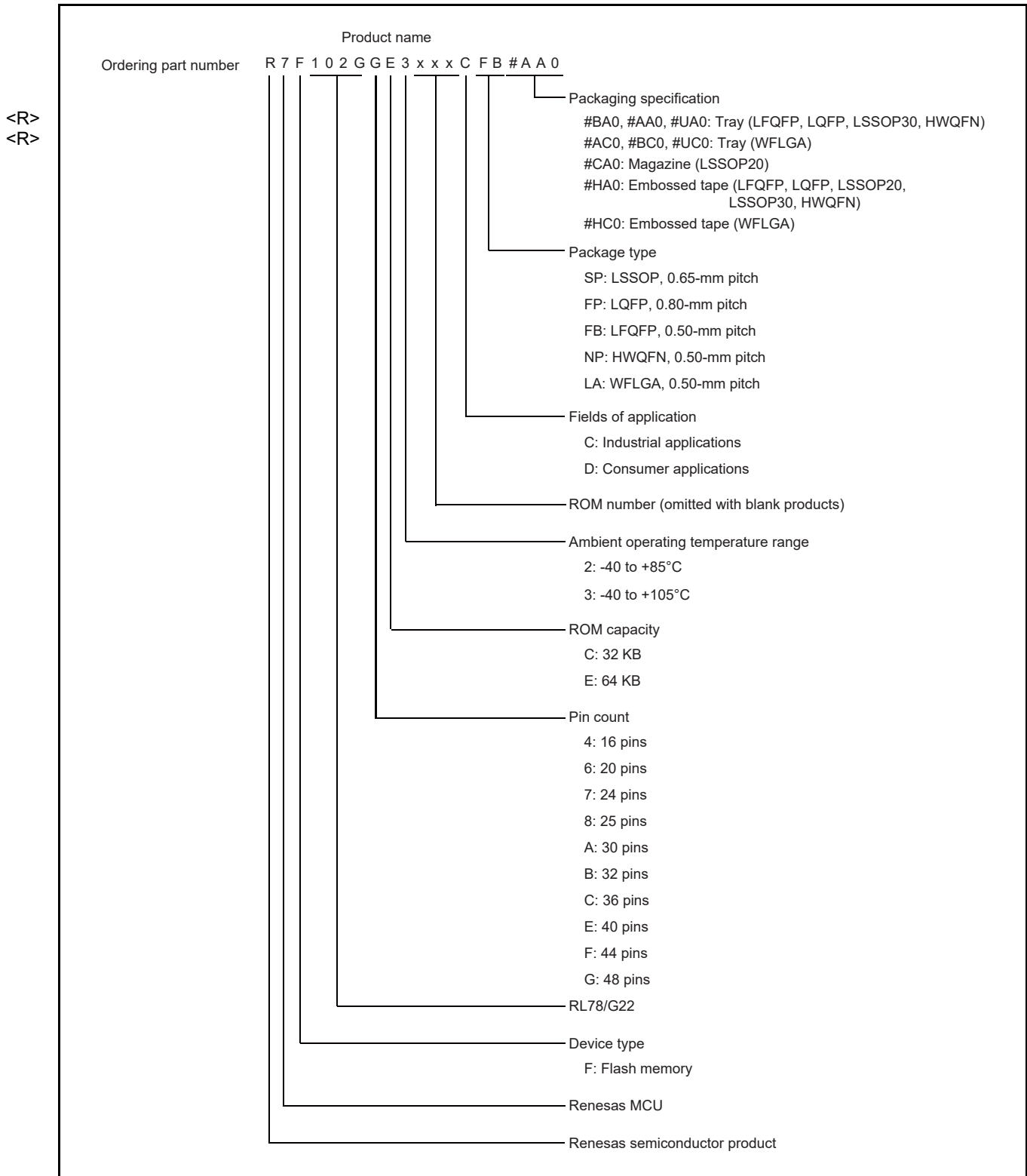
## O ROM, RAM capacities

| Flash ROM | Data flash memory | RAM  | RL78/G22  |           |           |           |           |
|-----------|-------------------|------|-----------|-----------|-----------|-----------|-----------|
|           |                   |      | 16 pins   | 20 pins   | 24 pins   | 25 pins   | 30 pins   |
| 64 KB     | 2 KB              | 4 KB | R7F102G4E | R7F102G6E | R7F102G7E | R7F102G8E | R7F102GAE |
| 32 KB     | 2 KB              | 4 KB | R7F102G4C | R7F102G6C | R7F102G7C | R7F102G8C | R7F102GAC |

| Flash ROM | Data flash memory | RAM  | RL78/G22  |           |           |           |           |
|-----------|-------------------|------|-----------|-----------|-----------|-----------|-----------|
|           |                   |      | 32 pins   | 36 pins   | 40 pins   | 44 pins   | 48 pins   |
| 64 KB     | 2 KB              | 4 KB | R7F102GBE | R7F102GCE | R7F102GEE | R7F102GFE | R7F102GGE |
| 32 KB     | 2 KB              | 4 KB | R7F102GBC | R7F102GCC | R7F102GEC | R7F102GFC | R7F102GGC |

## 1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22



&lt;R&gt; Table 1 - 1 List of Ordering Part Numbers

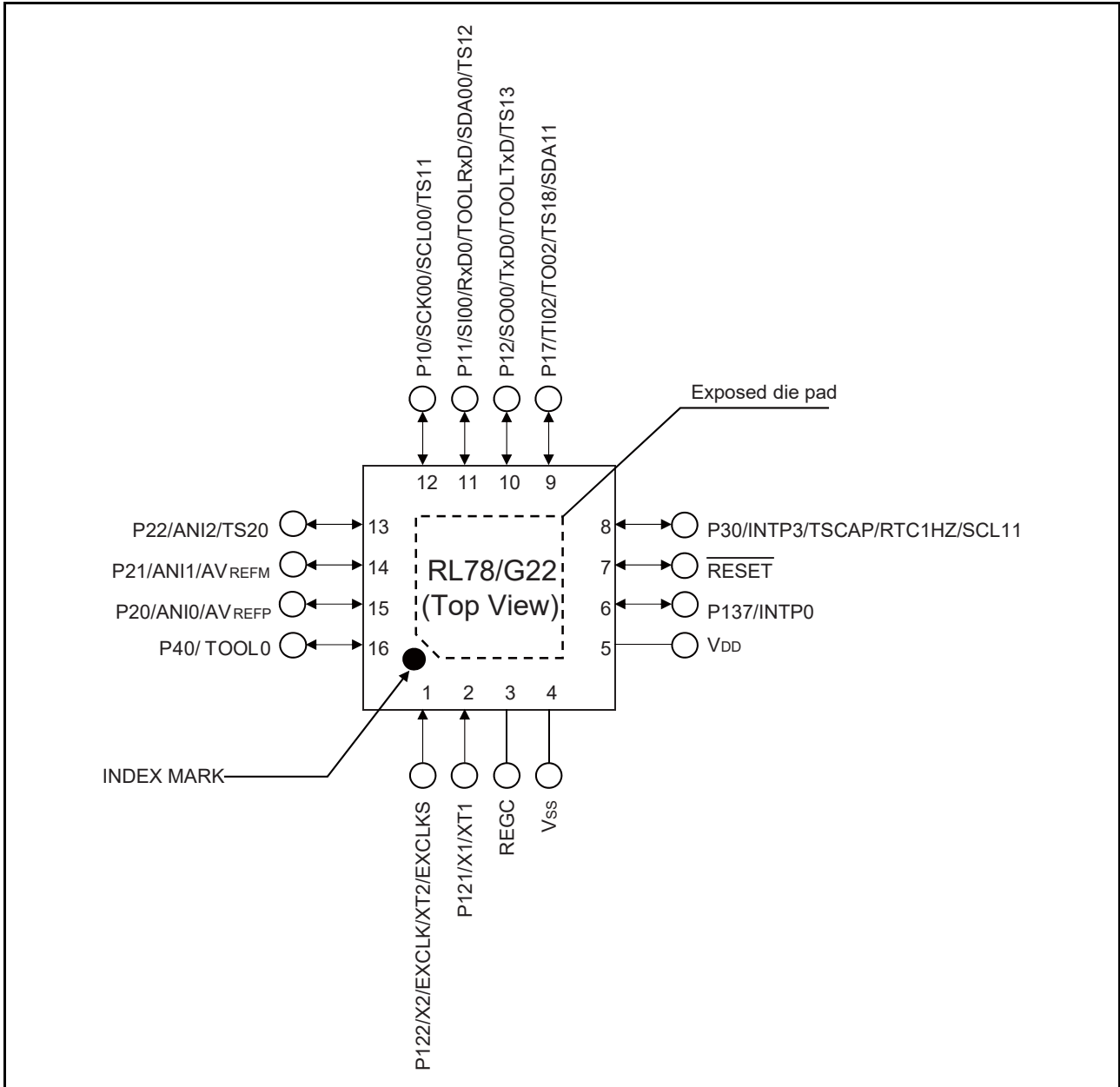
| Pin Count | Package  | Fields of Application<br>Note | Ordering Part Number         |                           | Renesas Code                 |
|-----------|--|-------------------------------|------------------------------|---------------------------|------------------------------|
|           |  |                               | Product Name                 | Packaging Specification   |                              |
| 16        | 16-pin plastic HWQFN<br>(3 × 3 mm, 0.50-mm pitch)      | C                             | R7F102G4C3CNP, R7F102G4E3CNP | #AA0, #BA0,<br>#UA0, #HA0 | PWQN0016KD-A                 |
|           |  | D                             | R7F102G4C2DNP, R7F102G4E2DNP |                           |                              |
| 20        | 20-pin plastic LSSOP<br>(4.4 × 6.5 mm, 0.65-mm pitch)  | C                             | R7F102G6C3CSP, R7F102G6E3CSP | #CA0, #HA0                | PLSP0020JB-A                 |
|           |  | D                             | R7F102G6C2DSP, R7F102G6E2DSP |                           |                              |
| 24        | 24-pin plastic HWQFN<br>(4 × 4 mm, 0.5 mm pitch)       | C                             | R7F102G7C3CNP, R7F102G7E3CNP | #AA0, #BA0,<br>#UA0, #HA0 | PWQN0024KG-A                 |
|           |  | D                             | R7F102G7C2DNP, R7F102G7E2DNP |                           |                              |
| 25        | 25-pin plastic WFLGA<br>(3 × 3 mm, 0.5 mm pitch)       | C                             | R7F102G8C3CLA, R7F102G8E3CLA | #AC0, #BC0,<br>#UC0, #HC0 | PWL0025KB-A                  |
|           |  | D                             | R7F102G8C2DLA, R7F102G8E2DLA |                           |                              |
| 30        | 30-pin plastic LSSOP<br>(7.62 mm (300), 0.65-mm pitch) | C                             | R7F102GAC3CSP, R7F102GAE3CSP | #AA0, #BA0,<br>#UA0, #HA0 | PLSP0030JB-B                 |
|           |  | D                             | R7F102GAC2DSP, R7F102GAE2DSP |                           |                              |
| 32        | 32-pin plastic HWQFN<br>(5 × 5 mm, 0.50-mm pitch)      | C                             | R7F102GBC3CNP, R7F102GBE3CNP | #AA0, #BA0,<br>#UA0, #HA0 | PWQN0032KE-A                 |
|           |  | D                             | R7F102GBC2DNP, R7F102GBE2DNP |                           |                              |
|           | 32-pin plastic LQFP<br>(7 × 7 mm, 0.80-mm pitch)       | C                             | R7F102GBC3CFP, R7F102GBE3CFP | #AA0, #BA0,<br>#UA0, #HA0 | PLQP0032GB-A<br>PLQP0032GE-A |
|           |  | D                             | R7F102GBC2DFP, R7F102GBE2DFP |                           |                              |
| 36        | 36-pin plastic WFLGA<br>(4 × 4 mm, 0.50-mm pitch)      | C                             | R7F102GCC3CLA, R7F102GCE3CLA | #BC0, #AC0,<br>#UC0, #HC0 | PWL0036KB-A                  |
|           |  | D                             | R7F102GCC2DLA, R7F102GCE2DLA |                           |                              |
| 40        | 40-pin plastic HWQFN<br>(6 × 6 mm, 0.50-mm pitch)      | C                             | R7F102GEC3CNP, R7F102GEE3CNP | #AA0, #BA0,<br>#UA0, #HA0 | PWQN0040KD-A                 |
|           |  | D                             | R7F102GEC2DNP, R7F102GEE2DNP |                           |                              |
| 44        | 44-pin plastic LQFP<br>(10 × 10 mm, 0.80-mm pitch)     | C                             | R7F102GFC3CFP, R7F102GFE3CFP | #AA0, #BA0,<br>#UA0, #HA0 | PLQP0044GC-A<br>PLQP0044GE-A |
|           |  | D                             | R7F102GFC2DFP, R7F102GFE2DFP |                           |                              |
| 48        | 48-pin plastic LFQFP<br>(7 × 7 mm, 0.50-mm pitch)      | C                             | R7F102GGC3CFB, R7F102GGE3CFB | #AA0, #BA0,<br>#UA0, #HA0 | PLQP0048KB-B<br>PLQP0048KL-A |
|           |  | D                             | R7F102GGC2DFB, R7F102GGE2DFB |                           |                              |
|           | 48-pin plastic HWQFN<br>(7 × 7 mm, 0.50-mm pitch)      | C                             | R7F102GGC3CNP, R7F102GGE3CNP | #AA0, #BA0,<br>#UA0, #HA0 | PWQN0048KC-A                 |
|           |  | D                             | R7F102GGC2DNP, R7F102GGE2DNP |                           |                              |

**Note** For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22**.

### 1.3 Pin Configuration (Top View)

#### 1.3.1 16-pin products

- 16-pin plastic HWQFN (3 × 3 mm, 0.5-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

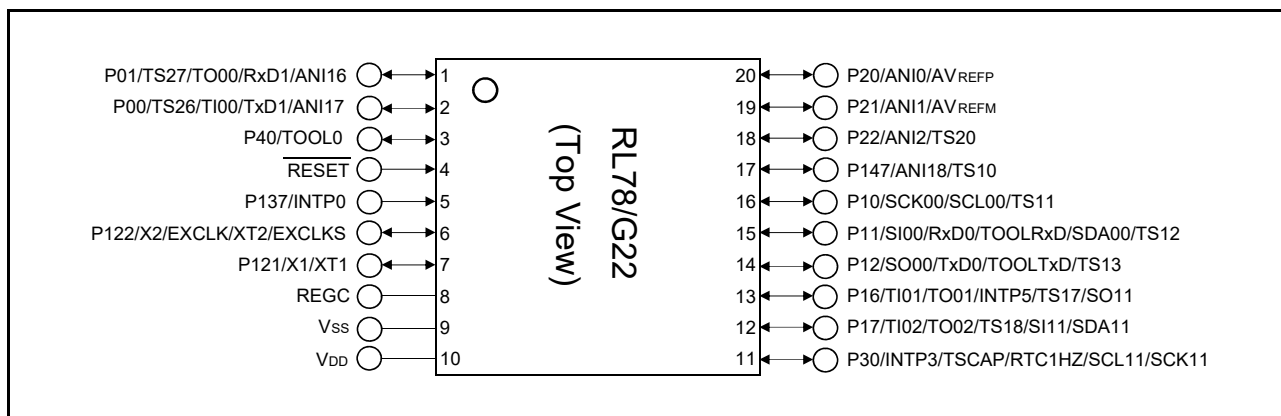
**Remark** For pin identification, see 1.4 Pin Identification.

Table 1 - 2 Multiplexed Pin Functions of the 16-pin Products

| Pin Number | I/O          | Power supply, system clock, and debugging | Analog Circuit      | HMI              |                    |                                   | Timers                 |                      | Communications Interfaces |                              |                                |
|------------|--------------|---|---------------------|------------------|--------------------|-----------------------------------|------------------------|----------------------|---------------------------|------------------------------|--------------------------------|
|            |              |   | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSU2La) | Timer array unit (TAU) | Realtime Clock (RTC) | Serial array unit (SAU)   | Serial interface IICA (IICA) | Serial interface UARTA (UARTA) |
| 16HWQFN    | Digital port |   |                     |                  |                    |                                   |                        |                      |                           |                              |                                |
| 1          | P122         | X2/XT2/EXCLK/EXCLKS                       | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 2          | P121         | X1/XT1                                    | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 3          | —            | REGC                                      | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 4          | —            | Vss                                       | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 5          | —            | Vdd                                       | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 6          | P137         | —   | —                   | INTP0            | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 7          | —            | RESET                                     | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 8          | P30          | —   | —                   | INTP3            | —                  | TSCAP                             | —                      | RTC1HZ               | SCL11                     | —                            | —                              |
| 9          | P17          | —   | —                   | —                | —                  | TS18                              | TI02/TO02              | —                    | SDA11                     | —                            | —                              |
| 10         | P12          | TOOLTxD                                   | —                   | —                | —                  | TS13                              | —                      | —                    | SO00/TxD0                 | —                            | —                              |
| 11         | P11          | TOOLRxD                                   | —                   | —                | —                  | TS12                              | —                      | —                    | SI00/RxD0/SDA00           | —                            | —                              |
| 12         | P10          | —   | —                   | —                | —                  | TS11                              | —                      | —                    | SCK00/SCL00               | —                            | —                              |
| 13         | P22          | —   | ANI2                | —                | —                  | TS20                              | —                      | —                    | —                         | —                            | —                              |
| 14         | P21          | —   | ANI1/AVREFM         | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 15         | P20          | —   | ANI0/AVREFP         | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |
| 16         | P40          | TOOL0                                     | —                   | —                | —                  | —                                 | —                      | —                    | —                         | —                            | —                              |

### 1.3.2 20-pin products

- 20-pin plastic LSSOP (4.4 × 6.5 mm, 0.65-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark** For pin identification, see 1.4 Pin Identification.

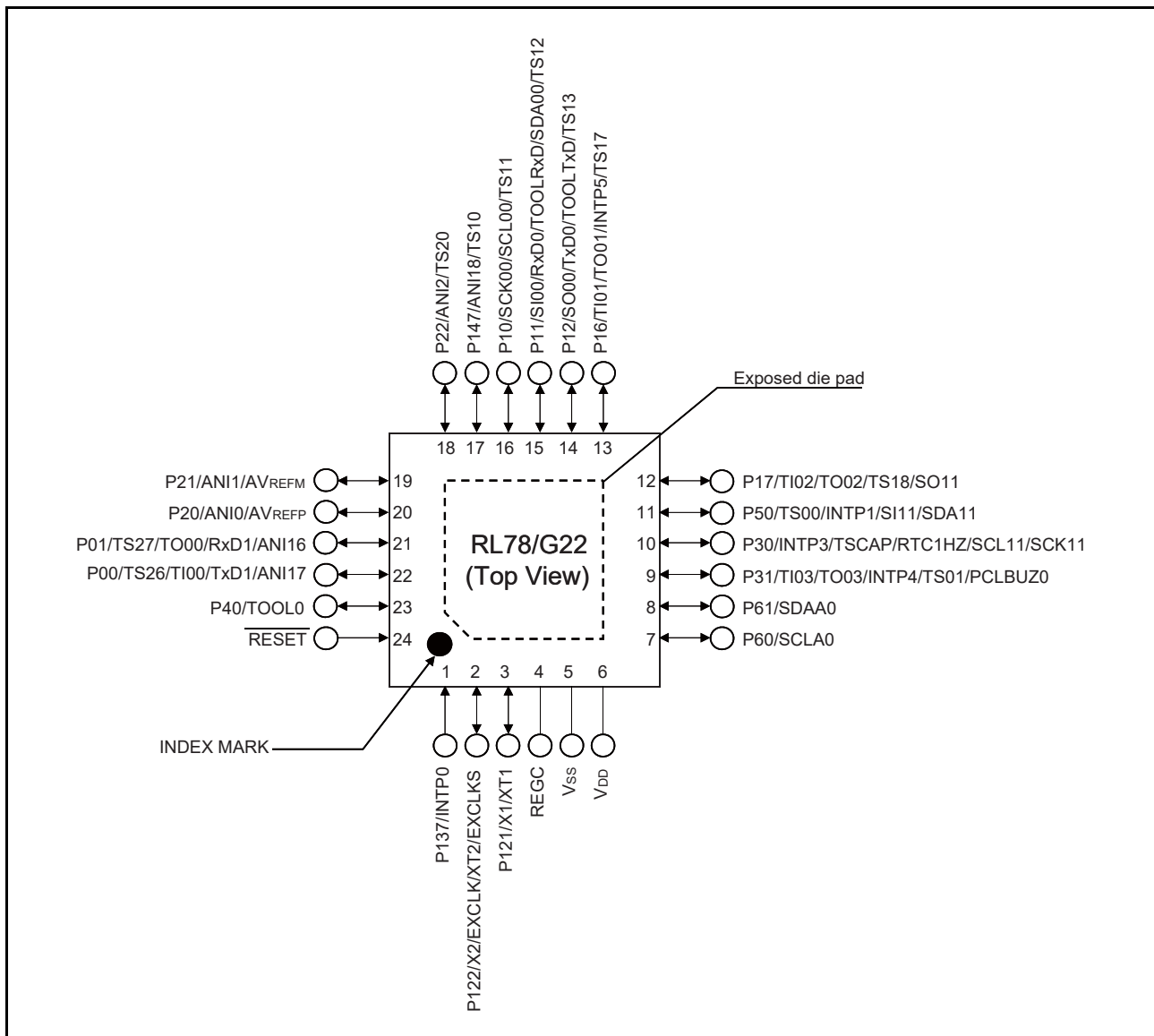


Table 1 - 3 Multiplexed Pin Functions of the 20-pin Products

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS2U2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 1          | P01  | —   | ANI16           | —                   | —                | TS27               | TO00                               | —                      | RxD1                      | —                       | —                            |
| 2          | P00  | —   | ANI17           | —                   | —                | TS26               | TI00                               | —                      | TxD1                      | —                       | —                            |
| 3          | P40  | TOOL0                                     | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 4          | —    | RESET                                     | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 5          | P137 | —   | —               | INTP0               | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 6          | P122 | X2/XT2/EXCLK/<br>EXCLKS                   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 7          | P121 | X1/XT1                                    | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 8          | —    | REGC                                      | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 9          | —    | VSS                                       | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 10         | —    | VDD                                       | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 11         | P30  | —   | —               | INTP3               | —                | TSCAP              | —                                  | RTC1HZ                 | SCK11/<br>SCL11           | —                       | —                            |
| 12         | P17  | —   | —               | —                   | —                | TS18               | TI02/TO02                          | —                      | SI11/<br>SDA11            | —                       | —                            |
| 13         | P16  | —   | —               | INTP5               | —                | TS17               | TI01/TO01                          | —                      | SO11                      | —                       | —                            |
| 14         | P12  | TOOLTxD                                   | —               | —                   | —                | TS13               | —                                  | —                      | SO00/<br>TxD0             | —                       | —                            |
| 15         | P11  | TOOLRxD                                   | —               | —                   | —                | TS12               | —                                  | —                      | SI00/RxD0/<br>SDA00       | —                       | —                            |
| 16         | P10  | —   | —               | —                   | —                | TS11               | —                                  | —                      | SCK00/<br>SCL00           | —                       | —                            |
| 17         | P147 | —   | ANI18           | —                   | —                | TS10               | —                                  | —                      | —                         | —                       | —                            |
| 18         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| 19         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 20         | P20  | —   | ANI0/<br>AVREFP | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |

### 1.3.3 24-pin products

- 24-pin plastic HWQFN (4 × 4 mm, 0.5-mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

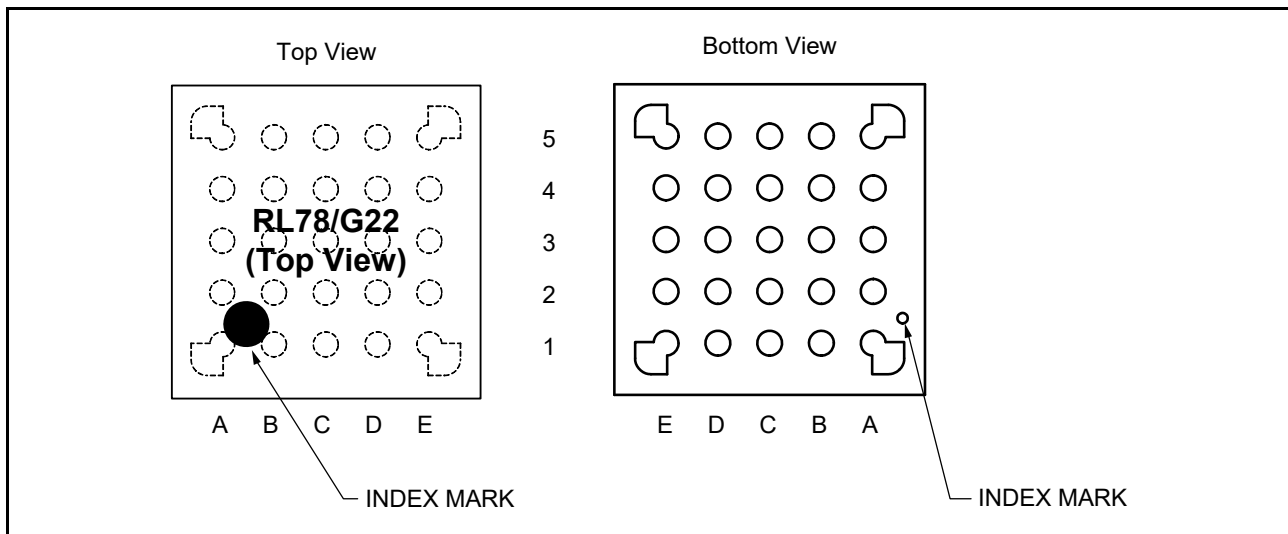
**Remark** For pin identification, see 1.4 Pin Identification.

Table 1 - 4 Multiplexed Pin Functions of the 24-pin Products

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit | HMI                 |                  |                    | Timers                            |                        | Communications Interfaces |                         |                              |
|------------|------|---|----------------|---------------------|------------------|--------------------|-----------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS02La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 1          | P137 | —   | —              | INTP0               | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 2          | P122 | X2/XT2/EXCLK/EXCLKS                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 3          | P121 | X1/XT1                                    | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 4          | —    | REGC                                      | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 5          | —    | VSS                                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 6          | —    | VDD                                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 7          | P60  | —   | —              | —                   | —                | —                  | —                                 | —                      | —                         | SCLA0                   | —                            |
| 8          | P61  | —   | —              | —                   | —                | —                  | —                                 | —                      | —                         | SDAA0                   | —                            |
| 9          | P31  | PCLBUZ0                                   | —              | INTP4               | —                | TS01               | TI03/TO03                         | —                      | —                         | —                       | —                            |
| 10         | P30  | —   | —              | INTP3               | —                | TSCAP              | —                                 | RTC1HZ                 | SCK11/SCL11               | —                       | —                            |
| 11         | P50  | —   | —              | INTP1               | —                | TS00               | —                                 | —                      | SI11/SDA11                | —                       | —                            |
| 12         | P17  | —   | —              | —                   | —                | TS18               | TI02/TO02                         | —                      | SO11                      | —                       | —                            |
| 13         | P16  | —   | —              | INTP5               | —                | TS17               | TI01/TO01                         | —                      | —                         | —                       | —                            |
| 14         | P12  | TOOLTxD                                   | —              | —                   | —                | TS13               | —                                 | —                      | SO00/TxD0                 | —                       | —                            |
| 15         | P11  | TOOLRxD                                   | —              | —                   | —                | TS12               | —                                 | —                      | SI00/RxD0/SDA00           | —                       | —                            |
| 16         | P10  | —   | —              | —                   | —                | TS11               | —                                 | —                      | SCK00/SCL00               | —                       | —                            |
| 17         | P147 | —   | ANI18          | —                   | —                | TS10               | —                                 | —                      | —                         | —                       | —                            |
| 18         | P22  | —   | ANI2           | —                   | —                | TS20               | —                                 | —                      | —                         | —                       | —                            |
| 19         | P21  | —   | ANI1/AVREFM    | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 20         | P20  | —   | ANI0/AVREFP    | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 21         | P01  | —   | ANI16          | —                   | —                | TS27               | TO00                              | —                      | RxD1                      | —                       | —                            |
| 22         | P00  | —   | ANI17          | —                   | —                | TS26               | TI00                              | —                      | TxD1                      | —                       | —                            |
| 23         | P40  | TOOL0                                     | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| 24         | —    | RESET                                     | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |

### 1.3.4 25-pin products

- 25-pin plastic WFLGA (3 × 3 mm, 0.5-mm pitch)



|   | A                        | B          | C                                  | D                          | E                                |   |
|---|--------------------------|------------|------------------------------------|----------------------------|----------------------------------|---|
| 5 | P40/TOOL0                | RESET      | P01/TS27/TO00/RxD1/ANI16           | P22/ANI2/TS20              | P147/ANI18/TS10                  | 5 |
| 4 | P122/X2/EXCLK/XT2/EXCLKS | P137/INTP0 | P00/TS26/TI00/TxD1/ANI17           | P21/ANI1/AVREFM            | P10/SCK00/SCL00/TS11             | 4 |
| 3 | P121/X1/XT1              | VDD        | P20/ANI0/AVREFP                    | P12/SO00/TxD0/TOOLTxD/TS13 | P11/SI00/RxD0/TOOLRxD/SDA00/TS12 | 3 |
| 2 | REGC                     | VSS        | P30/INTP3/TSCAP/RTC1HZ/SCL11/SCK11 | P17/TI02/TO02/TS18/SO11    | P50/TS00/INTP1/SI11/SDA11        | 2 |
| 1 | P60/SCLA0                | P61/SDAA0  | P31/TI03/TO03/INTP4/TS01/PCLBUZ0   | P16/TI01/TO01/INTP5/TS17   | P130/TS19                        | 1 |
|   | A                        | B          | C                                  | D                          | E                                |   |

**Caution** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

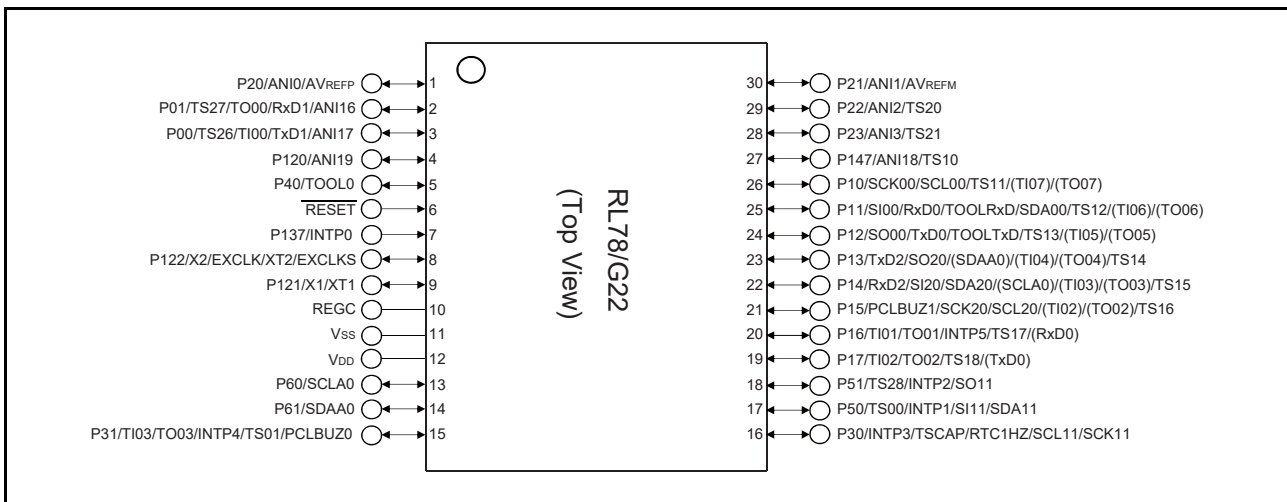
**Remark** For pin identification, see 1.4 Pin Identification.

Table 1 - 5 Multiplexed Pin Functions of the 25-pin Products

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit | HMI                 |                  |                    | Timers                            |                        | Communications Interfaces |                         |                              |
|------------|------|---|----------------|---------------------|------------------|--------------------|-----------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS/2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| A1         | P60  | —   | —              | —                   | —                | —                  | —                                 | —                      | —                         | SCLA0                   | —                            |
| A2         | —    | REGC                                      | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| A3         | P121 | X1/XT1                                    | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| A4         | P122 | X2/XT2/EXCLK/EXCLKS                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| A5         | P40  | TOOL0                                     | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| B1         | P61  | —   | —              | —                   | —                | —                  | —                                 | —                      | —                         | SDAA0                   | —                            |
| B2         | —    | VSS                                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| B3         | —    | VDD                                       | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| B4         | P137 | —   | —              | INTP0               | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| B5         | —    | RESET                                     | —              | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| C1         | P31  | PCLBUZ0                                   | —              | INTP4               | —                | TS01               | TI03/TO03                         | —                      | —                         | —                       | —                            |
| C2         | P30  | —   | —              | INTP3               | —                | TSCAP              | —                                 | RTC1HZ                 | SCK11/SCL11               | —                       | —                            |
| C3         | P20  | —   | ANI0/AVREFP    | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| C4         | P00  | —   | ANI17          | —                   | —                | TS26               | TI00                              | —                      | TxD1                      | —                       | —                            |
| C5         | P01  | —   | ANI16          | —                   | —                | TS27               | TO00                              | —                      | RxD1                      | —                       | —                            |
| D1         | P16  | —   | —              | INTP5               | —                | TS17               | TI01/TO01                         | —                      | —                         | —                       | —                            |
| D2         | P17  | —   | —              | —                   | —                | TS18               | TI02/TO02                         | —                      | SO11                      | —                       | —                            |
| D3         | P12  | TOOLTxD                                   | —              | —                   | —                | TS13               | —                                 | —                      | SO00/TxD0                 | —                       | —                            |
| D4         | P21  | —   | ANI1/AVREFM    | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| D5         | P22  | —   | ANI2           | —                   | —                | TS20               | —                                 | —                      | —                         | —                       | —                            |
| E1         | P130 | —   | —              | —                   | —                | TS19               | —                                 | —                      | —                         | —                       | —                            |
| E2         | P50  | —   | —              | INTP1               | —                | TS00               | —                                 | —                      | SI11/SDA11                | —                       | —                            |
| E3         | P11  | TOOLRxD                                   | —              | —                   | —                | TS12               | —                                 | —                      | SI00/RxD0/SDA00           | —                       | —                            |
| E4         | P10  | —   | —              | —                   | —                | TS11               | —                                 | —                      | SCK00/SCL00               | —                       | —                            |
| E5         | P147 | —   | ANI18          | —                   | —                | TS10               | —                                 | —                      | —                         | —                       | —                            |

### 1.3.5 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)



**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

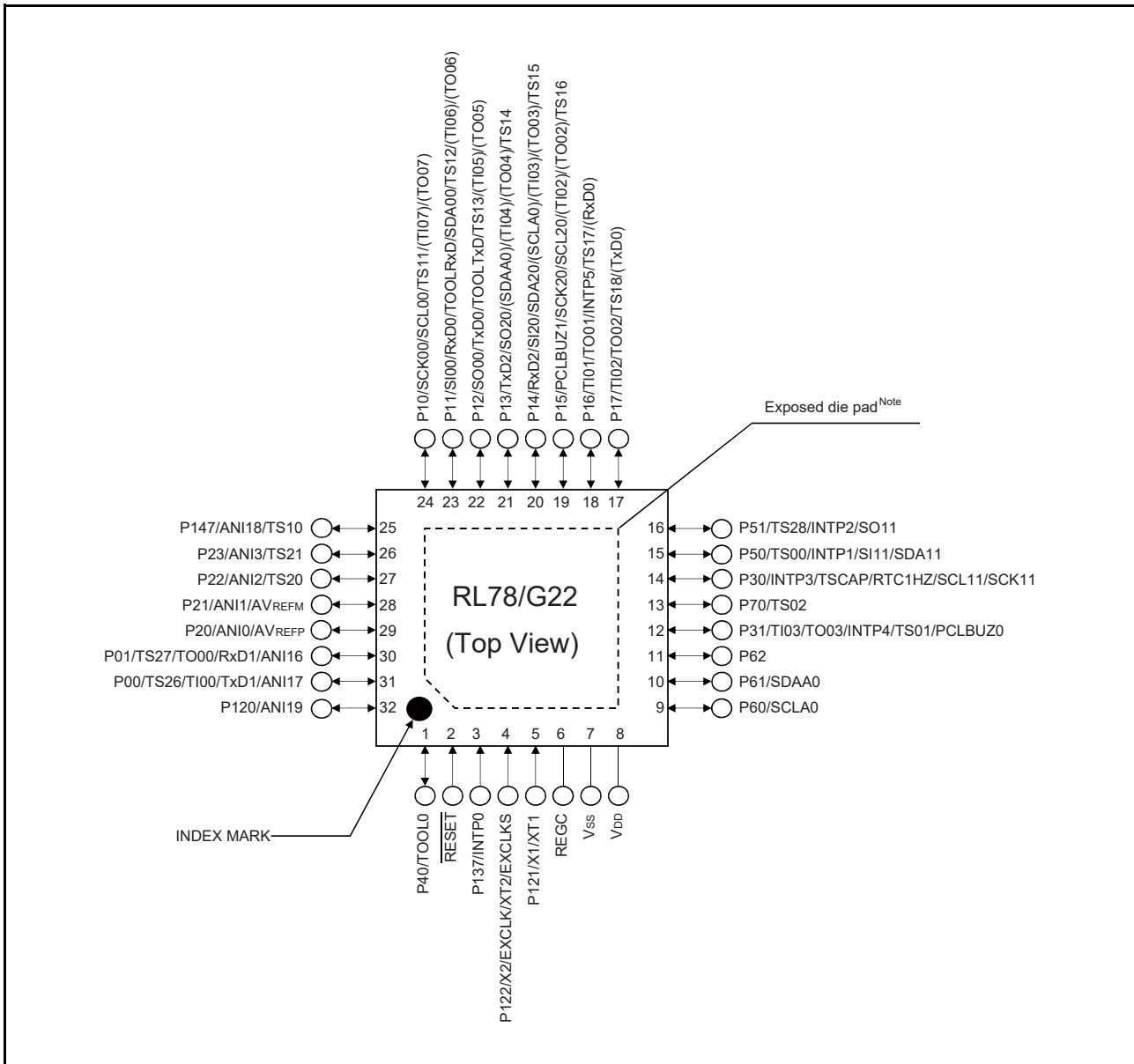
Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.

Table 1 - 6 Multiplexed Pin Functions of the 30-pin Products

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSUS2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 1          | P20  | —   | ANI0/<br>AVREFP | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 2          | P01  | —   | ANI16           | —                   | —                | TS27               | TO00                               | —                      | RxD1                      | —                       | —                            |
| 3          | P00  | —   | ANI17           | —                   | —                | TS26               | TI00                               | —                      | TxD1                      | —                       | —                            |
| 4          | P120 | —   | ANI19           | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 5          | P40  | TOOL0                                     | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 6          | —    | RESET                                     | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 7          | P137 | —   | —               | INTP0               | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 8          | P122 | X2/XT2/EXCLK/<br>EXCLKS                   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 9          | P121 | X1/XT1                                    | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 10         | —    | REGC                                      | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 11         | —    | Vss                                       | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 12         | —    | Vdd                                       | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 13         | P60  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SCLA0                   | —                            |
| 14         | P61  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SDAA0                   | —                            |
| 15         | P31  | PCLBUZ0                                   | —               | INTP4               | —                | TS01               | TI03/TO03                          | —                      | —                         | —                       | —                            |
| 16         | P30  | —   | —               | INTP3               | —                | TSCAP              | —                                  | RTC1HZ                 | SCK11/<br>SCL11           | —                       | —                            |
| 17         | P50  | —   | —               | INTP1               | —                | TS00               | —                                  | —                      | SI11/<br>SDA11            | —                       | —                            |
| 18         | P51  | —   | —               | INTP2               | —                | TS28               | —                                  | —                      | SO11                      | —                       | —                            |
| 19         | P17  | —   | —               | —                   | —                | TS18               | TI02/TO02                          | —                      | (TxD0)                    | —                       | —                            |
| 20         | P16  | —   | —               | INTP5               | —                | TS17               | TI01/TO01                          | —                      | (RxD0)                    | —                       | —                            |
| 21         | P15  | PCLBUZ1                                   | —               | —                   | —                | TS16               | (TI02)/<br>(TO02)                  | —                      | SCK20/<br>SCL20           | —                       | —                            |
| 22         | P14  | —   | —               | —                   | —                | TS15               | (TI03)/<br>(TO03)                  | —                      | SI20/RxD2/<br>SDA20       | (SCLA0)                 | —                            |
| 23         | P13  | —   | —               | —                   | —                | TS14               | (TI04)/<br>(TO04)                  | —                      | SO20/<br>TxD2             | (SDAA0)                 | —                            |
| 24         | P12  | TOOLTxD                                   | —               | —                   | —                | TS13               | (TI05)/<br>(TO05)                  | —                      | SO00/<br>TxD0             | —                       | —                            |
| 25         | P11  | TOOLRxD                                   | —               | —                   | —                | TS12               | (TI06)/<br>(TO06)                  | —                      | SI00/RxD0/<br>SDA00       | —                       | —                            |
| 26         | P10  | —   | —               | —                   | —                | TS11               | (TI07)/<br>(TO07)                  | —                      | SCK00/<br>SCL00           | —                       | —                            |
| 27         | P147 | —   | ANI18           | —                   | —                | TS10               | —                                  | —                      | —                         | —                       | —                            |
| 28         | P23  | —   | ANI3            | —                   | —                | TS21               | —                                  | —                      | —                         | —                       | —                            |
| 29         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| 30         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |

### 1.3.6 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)
- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)



**Note** The 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch) products do not have an exposed die pad.

**Caution** Connect the REGC pin to V<sub>SS</sub> via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.

**Remark 3.** It is recommended to connect an exposed die pad to V<sub>SS</sub>.

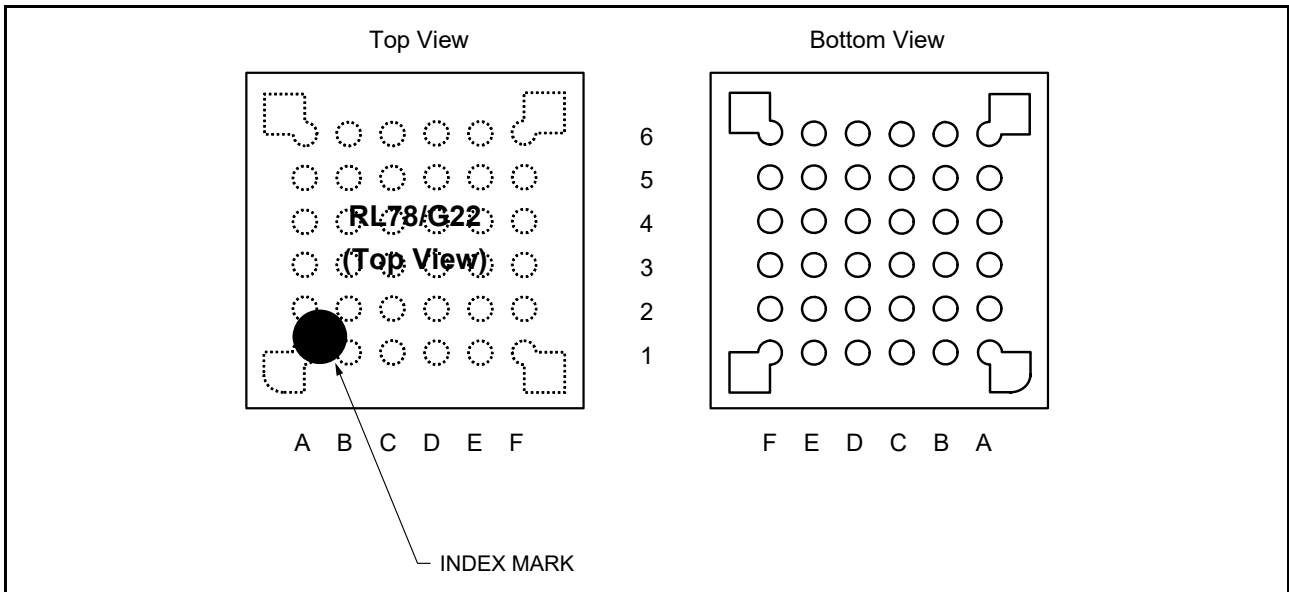


Table 1 - 7 Multiplexed Pin Functions of the 32-pin Products

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit      | HMI              |                    |                                    | Timers                 |                      | Communications Interfaces |                              |                                |
|------------|------|---|---------------------|------------------|--------------------|------------------------------------|------------------------|----------------------|---------------------------|------------------------------|--------------------------------|
|            |      |   | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSUS2La) | Timer array unit (TAU) | Realtime Clock (RTC) | Serial array unit (SAU)   | Serial interface IICA (IICA) | Serial interface UARTA (UARTA) |
| 1          | P40  | TOOL0                                     | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 2          | —    | RESET                                     | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 3          | P137 | —   | —                   | INTP0            | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 4          | P122 | X2/XT2/EXCLK/<br>EXCLKS                   | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 5          | P121 | X1/XT1                                    | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 6          | —    | REGC                                      | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 7          | —    | VSS                                       | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 8          | —    | VDD                                       | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 9          | P60  | —   | —                   | —                | —                  | —                                  | —                      | —                    | —                         | SCLA0                        | —                              |
| 10         | P61  | —   | —                   | —                | —                  | —                                  | —                      | —                    | —                         | SDAA0                        | —                              |
| 11         | P62  | —   | —                   | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 12         | P31  | PCLBUZ0                                   | —                   | INTP4            | —                  | TS01                               | TI03/TO03              | —                    | —                         | —                            | —                              |
| 13         | P70  | —   | —                   | —                | —                  | TS02                               | —                      | —                    | —                         | —                            | —                              |
| 14         | P30  | —   | —                   | INTP3            | —                  | TSCAP                              | —                      | RTC1HZ               | SCK11/<br>SCL11           | —                            | —                              |
| 15         | P50  | —   | —                   | INTP1            | —                  | TS00                               | —                      | —                    | SI11/<br>SDA11            | —                            | —                              |
| 16         | P51  | —   | —                   | INTP2            | —                  | TS28                               | —                      | —                    | SO11                      | —                            | —                              |
| 17         | P17  | —   | —                   | —                | —                  | TS18                               | TI02/TO02              | —                    | (TxD0)                    | —                            | —                              |
| 18         | P16  | —   | —                   | INTP5            | —                  | TS17                               | TI01/TO01              | —                    | (RxD0)                    | —                            | —                              |
| 19         | P15  | PCLBUZ1                                   | —                   | —                | —                  | TS16                               | (TI02)/<br>(TO02)      | —                    | SCK20/<br>SCL20           | —                            | —                              |
| 20         | P14  | —   | —                   | —                | —                  | TS15                               | (TI03)/<br>(TO03)      | —                    | SI20/RxD2/<br>SDA20       | (SCLA0)                      | —                              |
| 21         | P13  | —   | —                   | —                | —                  | TS14                               | (TI04)/<br>(TO04)      | —                    | SO20/<br>TxD2             | (SDAA0)                      | —                              |
| 22         | P12  | TOOLTxD                                   | —                   | —                | —                  | TS13                               | (TI05)/<br>(TO05)      | —                    | SO00/<br>TxD0             | —                            | —                              |
| 23         | P11  | TOOLRxD                                   | —                   | —                | —                  | TS12                               | (TI06)/<br>(TO06)      | —                    | SI00/RxD0/<br>SDA00       | —                            | —                              |
| 24         | P10  | —   | —                   | —                | —                  | TS11                               | (TI07)/<br>(TO07)      | —                    | SCK00/<br>SCL00           | —                            | —                              |
| 25         | P147 | —   | ANI18               | —                | —                  | TS10                               | —                      | —                    | —                         | —                            | —                              |
| 26         | P23  | —   | ANI3                | —                | —                  | TS21                               | —                      | —                    | —                         | —                            | —                              |
| 27         | P22  | —   | ANI2                | —                | —                  | TS20                               | —                      | —                    | —                         | —                            | —                              |
| 28         | P21  | —   | ANI1/<br>AVREFM     | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 29         | P20  | —   | ANI0/<br>AVREFP     | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |
| 30         | P01  | —   | ANI16               | —                | —                  | TS27                               | TO00                   | —                    | RxD1                      | —                            | —                              |
| 31         | P00  | —   | ANI17               | —                | —                  | TS26                               | TI00                   | —                    | TxD1                      | —                            | —                              |
| 32         | P120 | —   | ANI19               | —                | —                  | —                                  | —                      | —                    | —                         | —                            | —                              |

1.3.7 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)



|   | A  | B                                   | C  | D  | E                      | F                      |
|---|--|-------------------------------------|--|--|------------------------|------------------------|
| 6 | P60/SCLA0                                  | VDD                                 | P121/X1/XT1  | P122/X2/EXCLK/<br>XT2/EXCLKS                           | P137/INTP0             | P40/TOOL0              |
| 5 | P62  | P61/SDAA0                           | VSS  | REGC   | RESET                  | P120/ANI19             |
| 4 | P72/TS04/SO21/<br>TxDA0                    | P71/TS03/SI21/<br>SDA21/RxDA0       | P14/RxD2/SI20/<br>SDA20/(SCLA0)/<br>(TI03)/(TO03)/TS15 | P31/TI03/TO03/<br>INTP4/TS01/<br>PCLBUZ0               | P00/TS26/TI00/<br>TxD1 | P01/TS27/TO00/<br>RxD1 |
| 3 | P50/TS00/INTP1/<br>SI11/SDA11              | P70/TS02/SCK21/<br>SCL21            | P15/PCLBUZ1/<br>SCK20/SCL20/<br>(TI02)/(TO02)/TS16     | P22/ANI2/TS20  | P20/ANI0/AVREFP        | P21/ANI1/AVREFM        |
| 2 | P30/INTP3/TSCAP/<br>RTC1HZ/SCL11/<br>SCK11 | P16/TI01/TO01/<br>INTP5/TS17/(RxD0) | P12/SO00/TxD0/<br>TOOLTxD/TS13/<br>(TI05)/(TO05)       | P11/SI00/RxD0/<br>TOOLRxD/SDA00/<br>TS12/(TI06)/(TO06) | P24/ANI4/TS22          | P23/ANI3/TS21          |
| 1 | P51/TS28/INTP2/<br>SO11                    | P17/TI02/TO02/<br>TS18/(TxD0)       | P13/TxD2/SO20/<br>(SDAA0)/(TI04)/<br>(TO04)/TS14       | P10/SCK00/SCL00/<br>TS11/(TI07)/(TO07)                 | P147/ANI18/TS10        | P25/ANI5/TS23          |

**Caution** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.

Table 1 - 8 Multiplexed Pin Functions of the 36-pin Products (1/2)

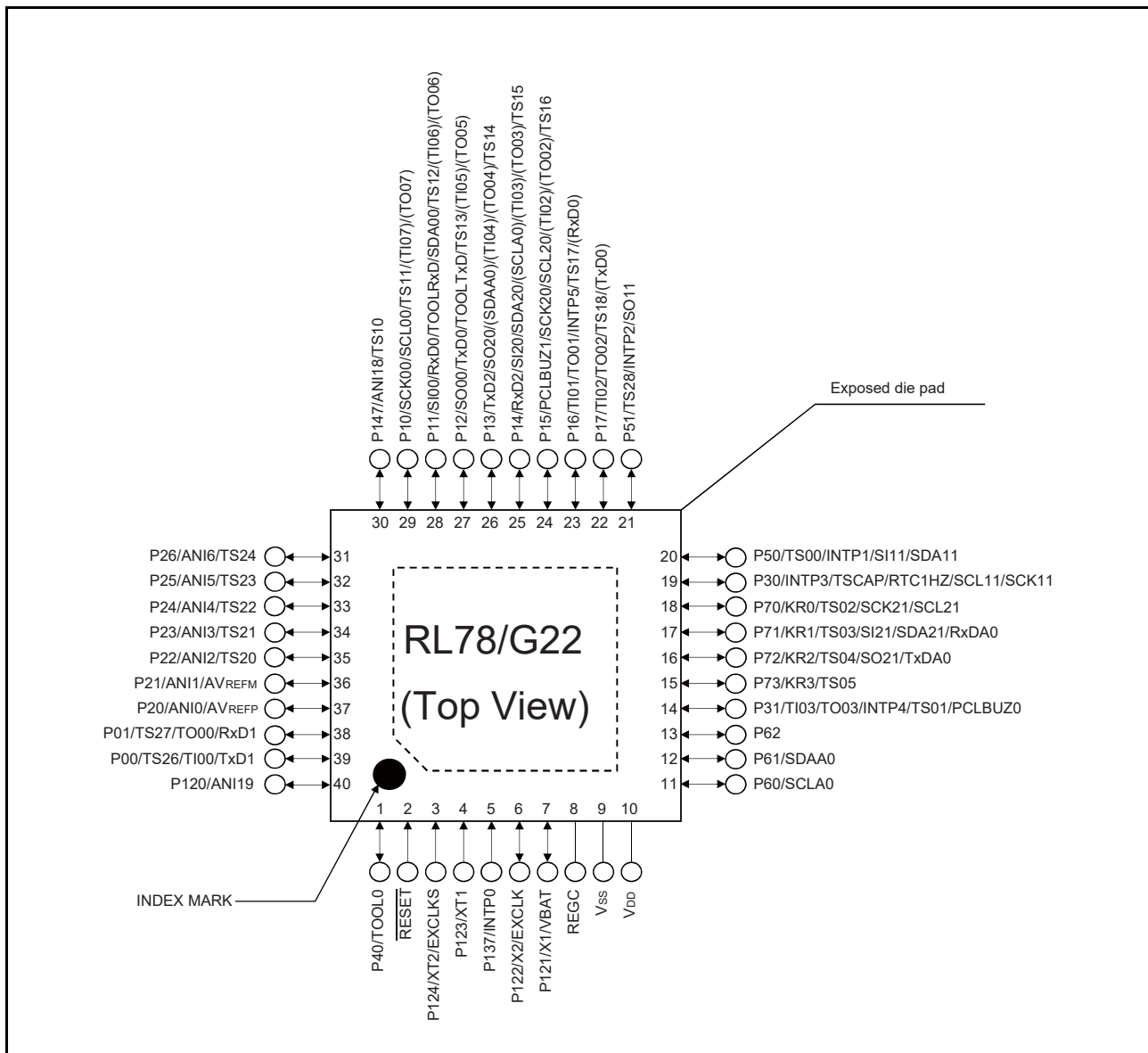
| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSUS2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| A1         | P51  | —   | —               | INTP2               | —                | TS28               | —                                  | —                      | SO11                      | —                       | —                            |
| A2         | P30  | —   | —               | INTP3               | —                | TSCAP              | —                                  | RTC1HZ                 | SCK11/<br>SCL11           | —                       | —                            |
| A3         | P50  | —   | —               | INTP1               | —                | TS00               | —                                  | —                      | SI11/<br>SDA11            | —                       | —                            |
| A4         | P72  | —   | —               | —                   | —                | TS04               | —                                  | —                      | SO21                      | —                       | TxDA0                        |
| A5         | P62  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| A6         | P60  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SCLA0                   | —                            |
| B1         | P17  | —   | —               | —                   | —                | TS18               | TI02/TO02                          | —                      | (TxD0)                    | —                       | —                            |
| B2         | P16  | —   | —               | INTP5               | —                | TS17               | TI01/TO01                          | —                      | (RxD0)                    | —                       | —                            |
| B3         | P70  | —   | —               | —                   | —                | TS02               | —                                  | —                      | SCK21/<br>SCL21           | —                       | —                            |
| B4         | P71  | —   | —               | —                   | —                | TS03               | —                                  | —                      | SI21/<br>SDA21            | —                       | RxDA0                        |
| B5         | P61  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SDAA0                   | —                            |
| B6         | —    | V <sub>DD</sub>                           | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| C1         | P13  | —   | —               | —                   | —                | TS14               | (TI04)/<br>(TO04)                  | —                      | SO20/<br>TxD2             | (SDAA0)                 | —                            |
| C2         | P12  | TOOLTxD                                   | —               | —                   | —                | TS13               | (TI05)/<br>(TO05)                  | —                      | SO00/<br>TxD0             | —                       | —                            |
| C3         | P15  | PCLBUZ1                                   | —               | —                   | —                | TS16               | (TI02)/<br>(TO02)                  | —                      | SCK20/<br>SCL20           | —                       | —                            |
| C4         | P14  | —   | —               | —                   | —                | TS15               | (TI03)/<br>(TO03)                  | —                      | SI20/RxD2/<br>SDA20       | (SCLA0)                 | —                            |
| C5         | —    | V <sub>SS</sub>                           | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| C6         | P121 | X1/XT1                                    | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| D1         | P10  | —   | —               | —                   | —                | TS11               | (TI07)/<br>(TO07)                  | —                      | SCK00/<br>SCL00           | —                       | —                            |
| D2         | P11  | TOOLRxD                                   | —               | —                   | —                | TS12               | (TI06)/<br>(TO06)                  | —                      | SI00/RxD0/<br>SDA00       | —                       | —                            |
| D3         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| D4         | P31  | PCLBUZ0                                   | —               | INTP4               | —                | TS01               | TI03/TO03                          | —                      | —                         | —                       | —                            |
| D5         | —    | REGC                                      | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| D6         | P122 | X2/XT2/EXCLK/<br>EXCLKS                   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| E1         | P147 | —   | ANI18           | —                   | —                | TS10               | —                                  | —                      | —                         | —                       | —                            |
| E2         | P24  | —   | ANI4            | —                   | —                | TS22               | —                                  | —                      | —                         | —                       | —                            |
| E3         | P20  | —   | ANI0/<br>AVREFF | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| E4         | P00  | —   | —               | —                   | —                | TS26               | TI00                               | —                      | TxD1                      | —                       | —                            |
| E5         | —    | RESET                                     | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| E6         | P137 | —   | —               | INTP0               | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| F1         | P25  | —   | ANI5            | —                   | —                | TS23               | —                                  | —                      | —                         | —                       | —                            |
| F2         | P23  | —   | ANI3            | —                   | —                | TS21               | —                                  | —                      | —                         | —                       | —                            |

Table 1 - 8 Multiplexed Pin Functions of the 36-pin Products (2/2)

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                            |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|-----------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS02La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| F3         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| F4         | P01  | —   | —               | —                   | —                | TS27               | TO00                              | —                      | RxD1                      | —                       | —                            |
| F5         | P120 | —   | ANI19           | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |
| F6         | P40  | TOOL0                                     | —               | —                   | —                | —                  | —                                 | —                      | —                         | —                       | —                            |

### 1.3.8 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (1/2)

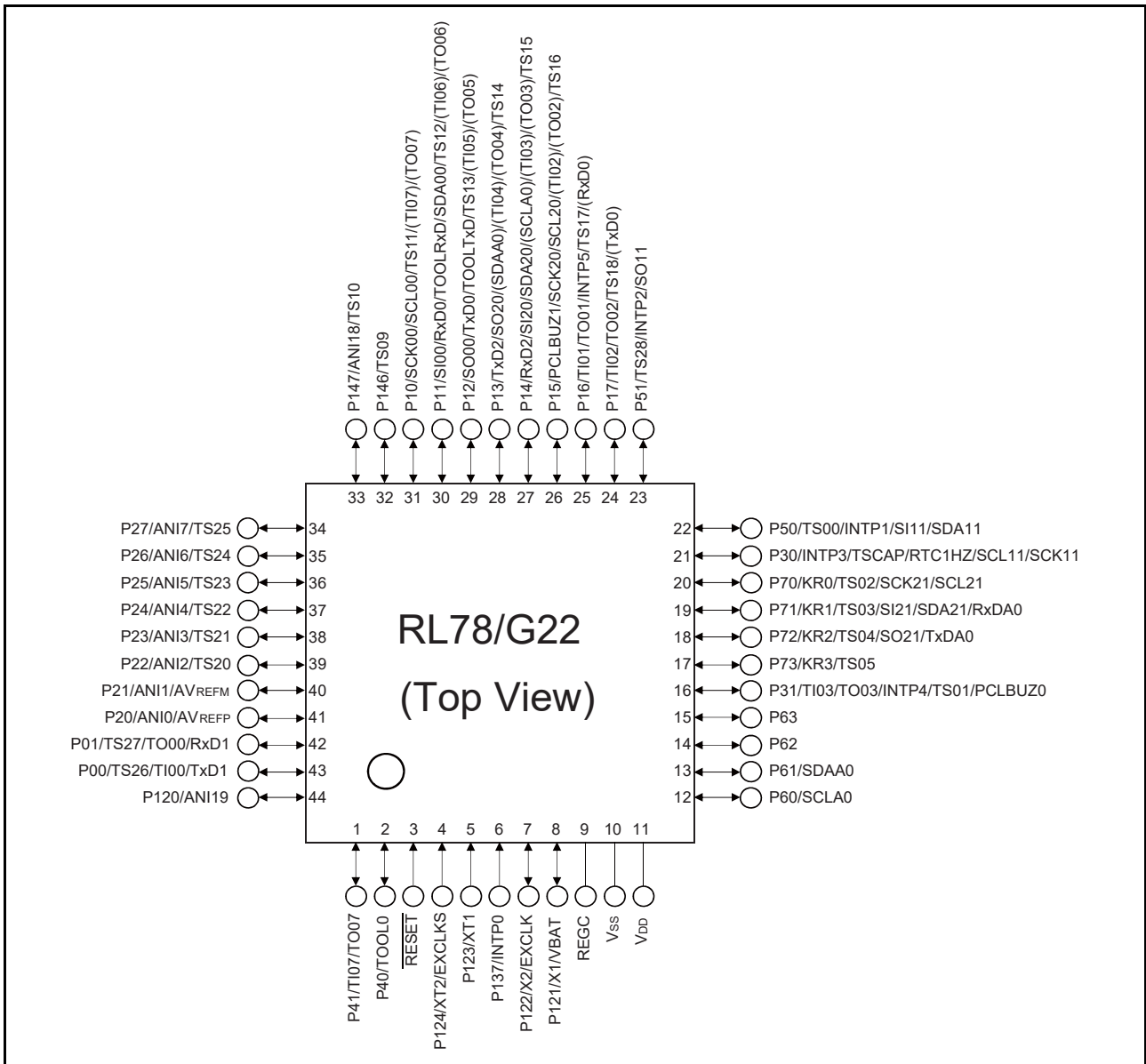
| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |                                |
|------------|------|---|----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|--------------------------------|
|            |      |   |                | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSUS2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) | Serial interface UAR1A (UAR1A) |
| 1          | P40  | TOOL0                                     | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 2          | —    | RESET                                     | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 3          | P124 | XT2/EXCLKS                                | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 4          | P123 | XT1                                       | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 5          | P137 | —   | —              | INTP0               | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 6          | P122 | X2/EXCLK                                  | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 7          | P121 | X1/VBAT                                   | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 8          | —    | REGC                                      | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 9          | —    | Vss                                       | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 10         | —    | Vdd                                       | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 11         | P60  | —   | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | SCLA0                        | —                              |
| 12         | P61  | —   | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | SDAA0                        | —                              |
| 13         | P62  | —   | —              | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            | —                              |
| 14         | P31  | PCLBUZ0                                   | —              | INTP4               | —                | TS01               | TI03/TO03                          | —                      | —                         | —                       | —                            | —                              |
| 15         | P73  | —   | —              | —                   | KR3              | TS05               | —                                  | —                      | —                         | —                       | —                            | —                              |
| 16         | P72  | —   | —              | —                   | KR2              | TS04               | —                                  | —                      | SO21                      | —                       | —                            | TxDA1                          |
| 17         | P71  | —   | —              | —                   | KR1              | TS03               | —                                  | —                      | SI21/<br>SDA21            | —                       | —                            | RxDA0                          |
| 18         | P70  | —   | —              | —                   | KR0              | TS02               | —                                  | —                      | SCK21/<br>SCL21           | —                       | —                            | —                              |
| 19         | P30  | —   | —              | INTP3               | —                | TSCAP              | —                                  | RTC1HZ                 | SCK11/<br>SCL11           | —                       | —                            | —                              |
| 20         | P50  | —   | —              | INTP1               | —                | TS00               | —                                  | —                      | SI11/<br>SDA11            | —                       | —                            | —                              |
| 21         | P51  | —   | —              | INTP2               | —                | TS28               | —                                  | —                      | SO11                      | —                       | —                            | —                              |
| 22         | P17  | —   | —              | —                   | —                | TS18               | TI02/TO02                          | —                      | (TxD0)                    | —                       | —                            | —                              |
| 23         | P16  | —   | —              | INTP5               | —                | TS17               | TI01/TO01                          | —                      | (RxD0)                    | —                       | —                            | —                              |
| 24         | P15  | PCLBUZ1                                   | —              | —                   | —                | TS16               | (TI02)/<br>(TO02)                  | —                      | SCK20/<br>SCL20           | —                       | —                            | —                              |
| 25         | P14  | —   | —              | —                   | —                | TS15               | (TI03)/<br>(TO03)                  | —                      | SI20/RxD2/<br>SDA20       | (SCLA0)                 | —                            | —                              |
| 26         | P13  | —   | —              | —                   | —                | TS14               | (TI04)/<br>(TO04)                  | —                      | SO20/<br>TxD2             | (SDAA0)                 | —                            | —                              |
| 27         | P12  | TOOLTxD                                   | —              | —                   | —                | TS13               | (TI05)/<br>(TO05)                  | —                      | SO00/<br>TxD0             | —                       | —                            | —                              |
| 28         | P11  | TOOLRxD                                   | —              | —                   | —                | TS12               | (TI06)/<br>(TO06)                  | —                      | SI00/RxD0/<br>SDA00       | —                       | —                            | —                              |
| 29         | P10  | —   | —              | —                   | —                | TS11               | (TI07)/<br>(TO07)                  | —                      | SCK00/<br>SCL00           | —                       | —                            | —                              |
| 30         | P147 | —   | ANI18          | —                   | —                | TS10               | —                                  | —                      | —                         | —                       | —                            | —                              |
| 31         | P26  | —   | ANI6           | —                   | —                | TS24               | —                                  | —                      | —                         | —                       | —                            | —                              |
| 32         | P25  | —   | ANI5           | —                   | —                | TS23               | —                                  | —                      | —                         | —                       | —                            | —                              |
| 33         | P24  | —   | ANI4           | —                   | —                | TS22               | —                                  | —                      | —                         | —                       | —                            | —                              |

Table 1 - 9 Multiplexed Pin Functions of the 40-pin Products (2/2)

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS/J2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 34         | P23  | —   | ANI3            | —                   | —                | TS21               | —                                  | —                      | —                         | —                       | —                            |
| 35         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| 36         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 37         | P20  | —   | ANI0/<br>AVREFP | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 38         | P01  | —   | —               | —                   | —                | TS27               | TO00                               | —                      | RxD1                      | —                       | —                            |
| 39         | P00  | —   | —               | —                   | —                | TS26               | TI00                               | —                      | TxD1                      | —                       | —                            |
| 40         | P120 | —   | ANI19           | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |

### 1.3.9 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.



Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (1/2)

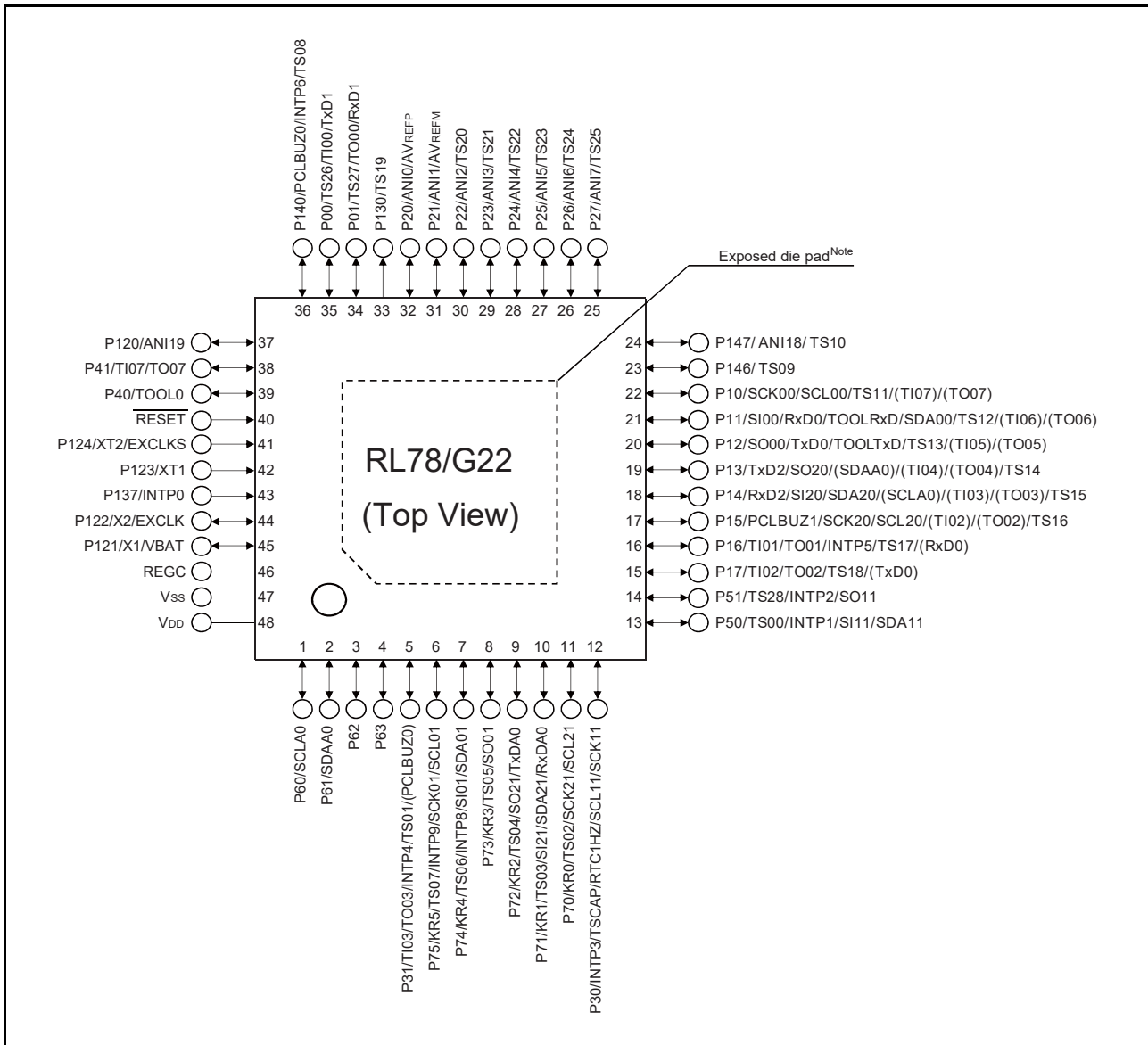
| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit | HMI                 |                  |                    | Timers                              |                        | Communications Interfaces |                         |                              |                                |
|------------|------|---|----------------|---------------------|------------------|--------------------|-------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|--------------------------------|
|            |      |   |                | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS/US2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) | Serial interface UARTA (UARTA) |
| 1          | P41  | —   | —              | —                   | —                | —                  | —                                   | TI07/TO07              | —                         | —                       | —                            | —                              |
| 2          | P40  | TOOL0                                     | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 3          | —    | RESET                                     | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 4          | P124 | XT2/EXCLKS                                | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 5          | P123 | XT1                                       | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 6          | P137 | —   | —              | INTP0               | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 7          | P122 | X2/EXCLK                                  | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 8          | P121 | X1/VBAT                                   | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 9          | —    | REGC                                      | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 10         | —    | Vss                                       | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 11         | —    | Vdd                                       | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 12         | P60  | —   | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | SCLA0                        | —                              |
| 13         | P61  | —   | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | SDAA0                        | —                              |
| 14         | P62  | —   | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 15         | P63  | —   | —              | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            | —                              |
| 16         | P31  | PCLBUZ0                                   | —              | INTP4               | —                | TS01               | —                                   | TI03/TO03              | —                         | —                       | —                            | —                              |
| 17         | P73  | —   | —              | —                   | KR3              | TS05               | —                                   | —                      | —                         | —                       | —                            | —                              |
| 18         | P72  | —   | —              | —                   | KR2              | TS04               | —                                   | —                      | SO21                      | —                       | TxDA1                        | —                              |
| 19         | P71  | —   | —              | —                   | KR1              | TS03               | —                                   | —                      | SI21/SDA21                | —                       | RxDA0                        | —                              |
| 20         | P70  | —   | —              | —                   | KR0              | TS02               | —                                   | —                      | SCK21/SCL21               | —                       | —                            | —                              |
| 21         | P30  | —   | —              | INTP3               | —                | TSCAP              | —                                   | RTC1HZ                 | SCK11/SCL11               | —                       | —                            | —                              |
| 22         | P50  | —   | —              | INTP1               | —                | TS00               | —                                   | —                      | SI11/SDA11                | —                       | —                            | —                              |
| 23         | P51  | —   | —              | INTP2               | —                | TS28               | —                                   | —                      | SO11                      | —                       | —                            | —                              |
| 24         | P17  | —   | —              | —                   | —                | TS18               | —                                   | TI02/TO02              | —                         | (TxD0)                  | —                            | —                              |
| 25         | P16  | —   | —              | INTP5               | —                | TS17               | —                                   | TI01/TO01              | —                         | (RxD0)                  | —                            | —                              |
| 26         | P15  | PCLBUZ1                                   | —              | —                   | —                | TS16               | —                                   | (TI02)/TO02            | —                         | SCK20/SCL20             | —                            | —                              |
| 27         | P14  | —   | —              | —                   | —                | TS15               | —                                   | (TI03)/TO03            | —                         | SI20/RxD2/SDA20         | (SCLA0)                      | —                              |
| 28         | P13  | —   | —              | —                   | —                | TS14               | —                                   | (TI04)/TO04            | —                         | SO20/TxD2               | (SDAA0)                      | —                              |
| 29         | P12  | TOOLTxD                                   | —              | —                   | —                | TS13               | —                                   | (TI05)/TO05            | —                         | SO00/TxD0               | —                            | —                              |
| 30         | P11  | TOOLRxD                                   | —              | —                   | —                | TS12               | —                                   | (TI06)/TO06            | —                         | SI00/RxD0/SDA00         | —                            | —                              |
| 31         | P10  | —   | —              | —                   | —                | TS11               | —                                   | (TI07)/TO07            | —                         | SCK00/SCL00             | —                            | —                              |
| 32         | P146 | —   | —              | —                   | —                | TS09               | —                                   | —                      | —                         | —                       | —                            | —                              |
| 33         | P147 | —   | ANI18          | —                   | —                | TS10               | —                                   | —                      | —                         | —                       | —                            | —                              |

Table 1 - 10 Multiplexed Pin Functions of the 44-pin Products (2/2)

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS/J2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 34         | P27  | —   | ANI7            | —                   | —                | TS25               | —                                  | —                      | —                         | —                       | —                            |
| 35         | P26  | —   | ANI6            | —                   | —                | TS24               | —                                  | —                      | —                         | —                       | —                            |
| 36         | P25  | —   | ANI5            | —                   | —                | TS23               | —                                  | —                      | —                         | —                       | —                            |
| 37         | P24  | —   | ANI4            | —                   | —                | TS22               | —                                  | —                      | —                         | —                       | —                            |
| 38         | P23  | —   | ANI3            | —                   | —                | TS21               | —                                  | —                      | —                         | —                       | —                            |
| 39         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| 40         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 41         | P20  | —   | ANI0/<br>AVREFP | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 42         | P01  | —   | —               | —                   | —                | TS27               | TO00                               | —                      | RxD1                      | —                       | —                            |
| 43         | P00  | —   | —               | —                   | —                | TS26               | TI00                               | —                      | TxD1                      | —                       | —                            |
| 44         | P120 | —   | ANI19           | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |

### 1.3.10 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)



**Note** The 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

**Caution** Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

**Remark 1.** For pin identification, see 1.4 Pin Identification.

**Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR).

Refer to **Figure 4 - 9 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G22 User's Manual.

**Remark 3.** It is recommended to connect an exposed die pad to Vss.

Table 1 - 11 Multiplexed Pin Functions of the 48-pin Products (1/2)

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                             |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTSUS2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 1          | P60  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SCLA0                   | —                            |
| 2          | P61  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | SDAA0                   | —                            |
| 3          | P62  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 4          | P63  | —   | —               | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |
| 5          | P31  | (PCLBUZ0)                                 | —               | INTP4               | —                | TS01               | TI03/TO03                          | —                      | —                         | —                       | —                            |
| 6          | P75  | —   | —               | INTP9               | KR5              | TS07               | —                                  | —                      | SCK01/<br>SCL01           | —                       | —                            |
| 7          | P74  | —   | —               | INTP8               | KR4              | TS06               | —                                  | —                      | SI01/<br>SDA01            | —                       | —                            |
| 8          | P73  | —   | —               | —                   | KR3              | TS05               | —                                  | —                      | SO01                      | —                       | —                            |
| 9          | P72  | —   | —               | —                   | KR2              | TS04               | —                                  | —                      | SO21                      | —                       | TxDA0                        |
| 10         | P71  | —   | —               | —                   | KR1              | TS03               | —                                  | —                      | SI21/<br>SDA21            | —                       | RxDA0                        |
| 11         | P70  | —   | —               | —                   | KR0              | TS02               | —                                  | —                      | SCK21/<br>SCL21           | —                       | —                            |
| 12         | P30  | —   | —               | INTP3               | —                | TSCAP              | —                                  | RTC1HZ                 | SCK11/<br>SCL11           | —                       | —                            |
| 13         | P50  | —   | —               | INTP1               | —                | TS00               | —                                  | —                      | SI11/<br>SDA11            | —                       | —                            |
| 14         | P51  | —   | —               | INTP2               | —                | TS28               | —                                  | —                      | SO11                      | —                       | —                            |
| 15         | P17  | —   | —               | —                   | —                | TS18               | TI02/TO02                          | —                      | (TxD0)                    | —                       | —                            |
| 16         | P16  | —   | —               | INTP5               | —                | TS17               | TI01/TO01                          | —                      | (RxD0)                    | —                       | —                            |
| 17         | P15  | PCLBUZ1                                   | —               | —                   | —                | TS16               | (TI02)/<br>(TO02)                  | —                      | SCK20/<br>SCL20           | —                       | —                            |
| 18         | P14  | —   | —               | —                   | —                | TS15               | (TI03)/<br>(TO03)                  | —                      | SI20/RxD2/<br>SDA20       | (SCLA0)                 | —                            |
| 19         | P13  | —   | —               | —                   | —                | TS14               | (TI04)/<br>(TO04)                  | —                      | SO20/<br>TxD2             | (SDAA0)                 | —                            |
| 20         | P12  | TOOLTxD                                   | —               | —                   | —                | TS13               | (TI05)/<br>(TO05)                  | —                      | SO00/<br>TxD0             | —                       | —                            |
| 21         | P11  | TOOLRxD                                   | —               | —                   | —                | TS12               | (TI06)/<br>(TO06)                  | —                      | SI00/RxD0/<br>SDA00       | —                       | —                            |
| 22         | P10  | —   | —               | —                   | —                | TS11               | (TI07)/<br>(TO07)                  | —                      | SCK00/<br>SCL00           | —                       | —                            |
| 23         | P146 | —   | —               | —                   | —                | TS09               | —                                  | —                      | —                         | —                       | —                            |
| 24         | P147 | —   | ANI18           | —                   | —                | TS10               | —                                  | —                      | —                         | —                       | —                            |
| 25         | P27  | —   | ANI7            | —                   | —                | TS25               | —                                  | —                      | —                         | —                       | —                            |
| 26         | P26  | —   | ANI6            | —                   | —                | TS24               | —                                  | —                      | —                         | —                       | —                            |
| 27         | P25  | —   | ANI5            | —                   | —                | TS23               | —                                  | —                      | —                         | —                       | —                            |
| 28         | P24  | —   | ANI4            | —                   | —                | TS22               | —                                  | —                      | —                         | —                       | —                            |
| 29         | P23  | —   | ANI3            | —                   | —                | TS21               | —                                  | —                      | —                         | —                       | —                            |
| 30         | P22  | —   | ANI2            | —                   | —                | TS20               | —                                  | —                      | —                         | —                       | —                            |
| 31         | P21  | —   | ANI1/<br>AVREFM | —                   | —                | —                  | —                                  | —                      | —                         | —                       | —                            |

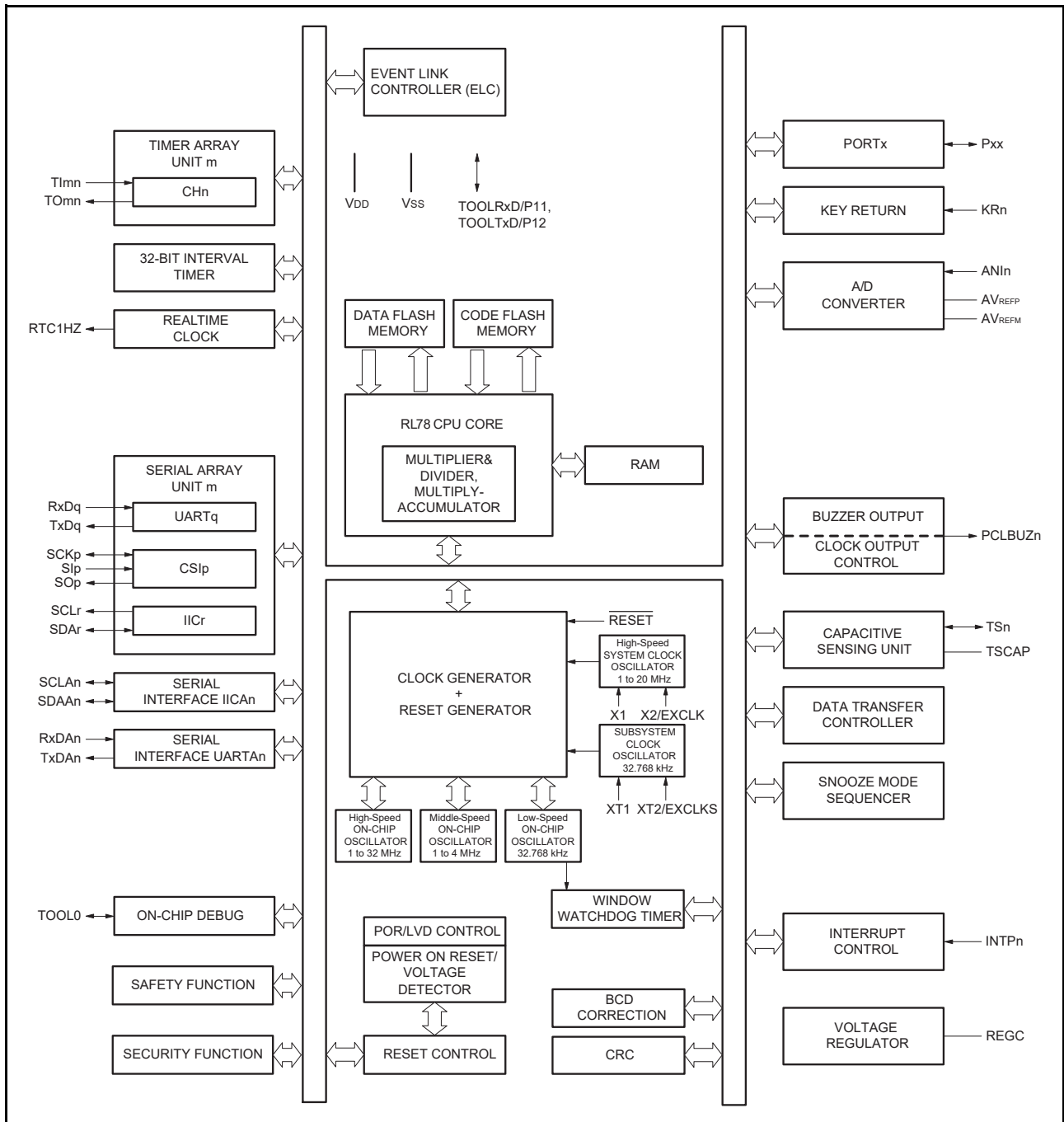
Table 1 - 11 Multiplexed Pin Functions of the 48-pin Products (2/2)

| Pin Number | I/O  | Power supply, system clock, and debugging | Analog Circuit  | HMI                 |                  |                    | Timers                              |                        | Communications Interfaces |                         |                              |
|------------|------|---|-----------------|---------------------|------------------|--------------------|-------------------------------------|------------------------|---------------------------|-------------------------|------------------------------|
|            |      |   |                 | A/D converter (ADC) | Interrupt (INTP) | Key interrupt (KR) | Capacitive sensing unit (CTS[U]2La) | Timer array unit (TAU) | Realtime Clock (RTC)      | Serial array unit (SAU) | Serial interface IICA (IICA) |
| 32         | P20  | —   | ANI0/<br>AVREFF | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 33         | P130 | —   | —               | —                   | —                | TS19               | —                                   | —                      | —                         | —                       | —                            |
| 34         | P01  | —   | —               | —                   | —                | TS27               | TO00                                | —                      | RxD1                      | —                       | —                            |
| 35         | P00  | —   | —               | —                   | —                | TS26               | TI00                                | —                      | TxD1                      | —                       | —                            |
| 36         | P140 | PCLBUZ0                                   | —               | INTP6               | —                | TS08               | —                                   | —                      | —                         | —                       | —                            |
| 37         | P120 | —   | ANI19           | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 38         | P41  | —   | —               | —                   | —                | —                  | TI07/TO07                           | —                      | —                         | —                       | —                            |
| 39         | P40  | TOOL0                                     | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 40         | —    | RESET                                     | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 41         | P124 | XT2/EXCLKS                                | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 42         | P123 | XT1                                       | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 43         | P137 | —   | —               | INTP0               | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 44         | P122 | X2/EXCLK                                  | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 45         | P121 | X1/VBAT                                   | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 46         | —    | REGC                                      | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 47         | —    | VSS                                       | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |
| 48         | —    | VDD                                       | —               | —                   | —                | —                  | —                                   | —                      | —                         | —                       | —                            |

## 1.4 Pin Identification

|                        |  |   |  |
|------------------------|--|---|--|
| ANI0 to ANI7,          |  | RxD0 to RxD2,                           |  |
| ANI16 to ANI19         | : Analog input                                     | RxDA0                                   | : Receive data                           |
| AVREFM                 | : Analog reference voltage minus                   | SCLA0,                                  |  |
| AVREFP                 | : Analog reference voltage plus                    | SCK00, SCK01,                           |  |
| EXCLK                  | : External clock input<br>(main system clock)      | SCK11, SCK20, SCK21                     | : Serial clock input/output              |
| EXCLKS                 | : External clock input<br>(subsystem clock)        | SCL00, SCL01,<br>SCL11, SCL20,<br>SCL21 | : Serial clock output                    |
| INTP0 to INTP6, INTP8, |  | SDAA0, SDA00,                           |  |
| INTP9                  | : Interrupt request from peripheral                | SDA01, SDA11,                           |  |
| KR0 to KR5             | : Key return                                       | SDA20, SDA21                            | : Serial data input/output               |
| P00, P01               | : Port 0   | SI00, SI01, SI11,                       |  |
| P10 to P17             | : Port 1   | SI20, SI21                              | : Serial data input                      |
| P20 to P27             | : Port 2   | SO00, SO01                              |  |
| P30, P31               | : Port 3   | SO11, SO20, SO21                        | : Serial data output                     |
| P40, P41               | : Port 4   | TSCAP                                   | : Touch sensor capacitance               |
| P50, P51               | : Port 5   | TI00 to TI07                            | : Timer input                            |
| P60 to P63             | : Port 6   | TO00 to TO07                            | : Timer output                           |
| P70 to P75             | : Port 7   | TOOL0                                   | : Data input/output for tool             |
| P120 to P124           | : Port 12  | TOOLRxD, TOOLTxD                        | : Data input/output for external device  |
| P130, P137             | : Port 13  | TS00 to TS28                            | : Capacitive touch sensor                |
| P140, P146, P147       | : Port 14  | TxD0 to TxD2                            | : Transmit data                          |
| PCLBUZ0, PCLBUZ1       | : Programmable clock output/buzzer<br>output       | TxDA0                                   |  |
| REGC                   | : Regulator capacitance                            | VBAT                                    | : Battery backup power supply            |
| <u>RESET</u>           | : Reset  | VDD                                     | : Power supply                           |
| RTC1HZ                 | : Realtime clock correction clock (1 Hz)<br>output | VSS                                     | : Ground                                 |
|                        |  | X1, X2                                  | : Crystal oscillator (main system clock) |
|                        |  | XT1, XT2                                | : Crystal oscillator (subsystem clock)   |

1.5 Block Diagram



**Caution 1.** The serial interface IICA is only incorporated in the 24- to 48-pin products.

**Caution 2.** The serial interface UARTA is only incorporated in the 36- to 48-pin products.

**Caution 3.** The key return function is only incorporated in the 40- to 48-pin products.

**Remark** m: Unit number, n: Channel number, p: Simplified SPI (CSI) number, q: UART number, r: Simplified I2C number, xx: Port number

## 1.6 Outline of Functions

**Caution** This outline describes the functions at the time when peripheral I/O redirection register (PIOR) is set to 00H.

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| Item   | 16-pin   | 20-pin  | 24-pin    | 25-pin    | 30-pin    | 32-pin    | 36-pin    | 40-pin                                      | 44-pin    | 48-pin    |  |
|--|--|---|-----------|-----------|-----------|-----------|-----------|---|-----------|-----------|--|
|  | R7F102G4x  | R7F102G6x   | R7F102G7x | R7F102G8x | R7F102GAx | R7F102GBx | R7F102GCx | R7F102GEx                                   | R7F102GFx | R7F102GGx |  |
| Code flash memory  | 32 or 64 KB  |   |           |           |           |           |           |   |           |           |  |
| Data flash memory  | 2 KB   |   |           |           |           |           |           |   |           |           |  |
| RAM  | 4 KB   |   |           |           |           |           |           |   |           |           |  |
| Address space  | 1 Mbyte  |   |           |           |           |           |           |   |           |           |  |
| CPU/<br>peripheral<br>hardware<br>clock<br>frequency<br>(fCLK) | Main<br>system<br>clock  | HS (high-speed main) mode: 1 to 32 MHz (V <sub>DD</sub> = 1.8 to 5.5 V)<br>HS (high-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (V <sub>DD</sub> = 1.6 to 5.5 V)<br>LS (low-speed main) mode: 1 to 24 MHz (V <sub>DD</sub> = 1.8 to 5.5 V)<br>LS (low-speed main) mode: 1 to 4 MHz <sup>Note 1</sup> (V <sub>DD</sub> = 1.6 to 5.5 V)<br>LP (low-power main) mode: 1 to 2 MHz <sup>Note 1</sup> (V <sub>DD</sub> = 1.6 to 5.5 V) |           |           |           |           |           |   |           |           |  |
|  | Subsystem<br>clock   | SUB mode: 32.768 kHz (V <sub>DD</sub> = 1.6 to 5.5 V)   |           |           |           |           |           |   |           |           |  |
| Main<br>system<br>clock  | High-<br>speed<br>system<br>clock (f <sub>MX</sub> )   | 1 to 20 MHz   |           |           |           |           |           |   |           |           |  |
|  | High-<br>speed on-<br>chip<br>oscillator<br>clock (f <sub>IH</sub> )   | 1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz  |           |           |           |           |           |   |           |           |  |
|  | Middle-<br>speed on-<br>chip<br>oscillator<br>clock (f <sub>IM</sub> )   | 1 MHz, 2 MHz, 4 MHz   |           |           |           |           |           |   |           |           |  |
| Subsystem<br>clock   | Subsystem<br>clock X<br>(f <sub>SX</sub> )   | 32.768 kHz (V <sub>DD</sub> = 2.4 to 5.5 V)   |           |           |           |           |           | 32.768 kHz (V <sub>DD</sub> = 1.6 to 5.5 V) |           |           |  |
|  | Low-speed<br>on-chip<br>oscillator<br>clock (f <sub>IL</sub> )   | 32.768 kHz (typ.)   |           |           |           |           |           |   |           |           |  |
| General-purpose<br>registers                                   | 8 bits × 32 registers (8 bits × 8 registers × 4 banks)   |   |           |           |           |           |           |   |           |           |  |
| Minimum instruction<br>execution time                          | 0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (f <sub>IH</sub> ))   |   |           |           |           |           |           |   |           |           |  |
| Instruction set  | <ul style="list-style-type: none"> <li>• Data transfer (8/16 bits)</li> <li>• Adder and subtractor/logical operation (8/16 bits)</li> <li>• Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits)</li> <li>• Multiplication and accumulation (16 bits × 16 bits + 32 bits)</li> <li>• Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc.</li> </ul> |   |           |           |           |           |           |   |           |           |  |



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| Item                               |   | 16-pin  | 20-pin  | 24-pin  | 25-pin     | 30-pin  | 32-pin   | 36-pin   | 40-pin   | 44-pin   | 48-pin   |  |
|------------------------------------|---|---|---|---|------------|---|--|--|--|--|--|--|
|                                    |   | R7F102G4x   | R7F102G6x   | R7F102G7x   | R7F102G8x  | R7F102GAx   | R7F102GBx  | R7F102GCx  | R7F102GEx  | R7F102GFx  | R7F102GGx  |  |
| I/O port                           | Total number of pins  | 12  | 16  | 20  | 21         | 26  | 28   | 32   | 36   | 40   | 44   |  |
|                                    | CMOS I/O  | 11<br>(N-ch open drain I/O [withstand voltage of VDD]: 4)   | 15<br>(N-ch open drain I/O [withstand voltage of VDD]: 5) | 17<br>(N-ch open drain I/O [withstand voltage of VDD]: 6) |            | 23<br>(N-ch open drain I/O [withstand voltage of VDD]: 10)  | 24<br>(N-ch open drain I/O [withstand voltage of VDD]: 10) | 28<br>(N-ch open drain I/O [withstand voltage of VDD]: 12) | 30<br>(N-ch open drain I/O [withstand voltage of VDD]: 12) | 33<br>(N-ch open drain I/O [withstand voltage of VDD]: 12) | 36<br>(N-ch open drain I/O [withstand voltage of VDD]: 13) |  |
|                                    | CMOS input  | 1   |   |   |            |   |  |  | 3  |  |  |  |
|                                    | CMOS output   | —   |   |   |            | 1   | —  |  | 1  |  |  |  |
|                                    | N-ch open drain I/O [withstand voltage of 6 V]  | —   |   |   | 2          |   |  | 3  |  |  | 4  |  |
| Timers                             | 16-bit timer  | 8 channels  |   |   |            |   |  |  |  |  |  |  |
|                                    | Watchdog timer  | 1 channel   |   |   |            |   |  |  |  |  |  |  |
|                                    | Realtime clock (RTC)  | 1 channel   |   |   |            |   |  |  |  |  |  |  |
|                                    | 32-bit interval timer (TML32)   | 1 channel in 32-bit counter mode,<br>2 channels in 16-bit counter mode,<br>4 channels in 8-bit counter mode |   |   |            |   |  |  |  |  |  |  |
|                                    | Timer output  | 1 channel (PWM output: 1)   | 3 channels (PWM outputs: 2 <sup>Note 2</sup> )            | 4 channels (PWM outputs: 3 <sup>Note 2</sup> )            |            | 4 channels (PWM outputs: 3 <sup>Note 2</sup> ),<br>8 channels (PWM outputs: 7 <sup>Note 2</sup> ) <sup>Note 3</sup> |  |  |  |  |  |  |
|                                    | RTC output  | 1 channel   |   |   |            |   |  |  |  |  |  |  |
| Clock output/buzzer output         | 2   |   |   |   |            |   |  |  |  |  |  |  |
|                                    | <ul style="list-style-type: none"> <li>3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (f<sub>MAIN</sub>))</li> <li>256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (f<sub>SP</sub>))</li> </ul> |   |   |   |            |   |  |  |  |  |  |  |
| 8-/10-bit resolution A/D converter | 3 channels  | 6 channels  |   |   | 8 channels |   |  | 9 channels   | 10 channels  |  |  |  |

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| Item   | 16-pin  | 20-pin   | 24-pin     | 25-pin    | 30-pin     | 32-pin    | 36-pin     | 40-pin     | 44-pin    | 48-pin     |  |
|--|---|--|------------|-----------|------------|-----------|------------|------------|-----------|------------|--|
|  | R7F102G4x   | R7F102G6x  | R7F102G7x  | R7F102G8x | R7F102GAx  | R7F102GBx | R7F102GCx  | R7F102GEx  | R7F102GFx | R7F102GGx  |  |
| Serial interfaces  | [16-pin products]   |  |            |           |            |           |            |            |           |            |  |
|  | <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified I<sup>2</sup>C: 1 channel</li> </ul>  |  |            |           |            |           |            |            |           |            |  |
|  | [20-, 24-, and 25-pin products]   |  |            |           |            |           |            |            |           |            |  |
|  | <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> </ul>  |  |            |           |            |           |            |            |           |            |  |
|  | [30- and 32-pin products]   |  |            |           |            |           |            |            |           |            |  |
| <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART (UART supporting LIN-bus): 1 channel</li> </ul>     |   |  |            |           |            |           |            |            |           |            |  |
| [36-, 40-, and 44-pin products]  |   |  |            |           |            |           |            |            |           |            |  |
| <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART (UART supporting LIN-bus): 1 channel</li> </ul>   |   |  |            |           |            |           |            |            |           |            |  |
| [48-pin products]  |   |  |            |           |            |           |            |            |           |            |  |
| <ul style="list-style-type: none"> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART: 1 channel</li> <li>• Simplified SPI (CSI): 1 channel, simplified I<sup>2</sup>C: 1 channel, UART: 1 channel</li> <li>• Simplified SPI (CSI): 2 channels, simplified I<sup>2</sup>C: 2 channels, UART (UART supporting LIN-bus): 1 channel</li> </ul> |   |  |            |           |            |           |            |            |           |            |  |
| UARTA  | —   |  |            |           |            |           | 1 channel  |            |           |            |  |
| I <sup>2</sup> C bus   | —   |  |            | 1 channel |            |           |            |            |           |            |  |
| Data transfer controller (DTC)   | 21 sources  | 23 sources   | 25 sources |           | 28 sources |           | 30 sources | 31 sources |           | 32 sources |  |
| Event link controller (ELC)  | 1   |  |            |           |            |           |            |            |           |            |  |
| SNOOZE mode sequencer (SMS)  | 1   |  |            |           |            |           |            |            |           |            |  |
| Capacitive sensing unit  | 5   | 9  | 11         | 12        | 16         | 17        | 21         | 23         | 25        | 29         |  |
| Vectored interrupt sources   | Internal  | 23   | 25         | 26        |            | 29        |            | 32         |           |            |  |
|  | External  | 2  | 3          | 5         |            | 6         |            |            | 7         | 10         |  |
| Key interrupt  | —   |  |            |           |            |           |            | 4          |           | 6          |  |
| Reset  | <ul style="list-style-type: none"> <li>• Reset by <math>\overline{\text{RESET}}</math> pin</li> <li>• Internal reset by watchdog timer</li> <li>• Internal reset by power-on-reset</li> <li>• Internal reset by voltage detectors (LVD0 and LVD1)</li> <li>• Internal reset by illegal instruction execution<sup>Note 4</sup></li> <li>• Internal reset by RAM parity error</li> <li>• Internal reset by illegal-memory access</li> </ul> |  |            |           |            |           |            |            |           |            |  |
| Power-on-reset circuit   | Detection voltage<br>• 1.50 V (typ.)  |  |            |           |            |           |            |            |           |            |  |
| Voltage detector   | LVD0  | Detection voltage<br>• Rising edge: 1.67 to 4.00 V (6 stages)<br>• Falling edge: 1.63 to 3.92 V (6 stages)   |            |           |            |           |            |            |           |            |  |
|  | LVD1  | Detection voltage<br>• Rising edge: 1.67 to 4.16 V (18 stages)<br>• Falling edge: 1.63 to 4.08 V (18 stages) |            |           |            |           |            |            |           |            |  |
| On-chip debugging  | Available   |  |            |           |            |           |            |            |           |            |  |
| Power supply voltage   | V <sub>DD</sub> = 1.6 to 5.5 V  |  |            |           |            |           |            |            |           |            |  |

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| Item                          | 16-pin  | 20-pin    | 24-pin    | 25-pin    | 30-pin    | 32-pin    | 36-pin    | 40-pin    | 44-pin    | 48-pin    |
|-------------------------------|---|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|-----------|
|                               | R7F102G4x   | R7F102G6x | R7F102G7x | R7F102G8x | R7F102GAx | R7F102GBx | R7F102GCx | R7F102GEx | R7F102GFx | R7F102GGx |
| Operating ambient temperature | TA = -40 to +85°C (2D: Consumer applications), TA = -40 to +105°C (3C: Industrial applications) |           |           |           |           |           |           |           |           |           |

- Note 1.** Ensure that the operating voltage is at least 1.8 V during overwriting of the flash memory.
- Note 2.** The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G22 User's Manual.
- Note 3.** This applies when the setting of the PIOR0 bit is 1.
- Note 4.** In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

## 2. Electrical Characteristics

This section describes the electrical characteristics of the following products.

- 2D: Consumer applications, TA = -40 to +85°C  
R7F102Gxx2Dxx
- 3C: Industrial applications, TA = -40 to +105°C  
R7F102Gxx3Cxx

**Caution 1.** RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.

**Caution 2.** For the consumer application products, the ambient operating temperature of TA = -40 to +85°C applies. Note that the characteristics of the A/D converter for each of the ranges of ambient operating temperature are described in the following sections.

2.6.1 Characteristics of the A/D converter for TA = -40 to +85°C

2.6.2 Characteristics of the A/D converter for TA = -40 to +105°C

**Caution 3.** The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product in the RL78/G22 User's Manual.

## 2.1 Absolute Maximum Ratings

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| Item                        | Symbols                  | Conditions   |  | Ratings  | Unit |
|-----------------------------|--------------------------|--|--|--|------|
| Supply voltage              | VDD                      |  |  | -0.5 to +6.5   | V    |
| REGC pin input voltage      | VIREGC                   | REGC   |  | -0.3 to +2.1<br>and -0.3 to VDD + 0.3 <sup>Note 1</sup>  | V    |
| Input voltage               | Vi1                      | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147             |  | -0.3 to VDD + 0.3 <sup>Note 2</sup>  | V    |
|                             | Vi2                      | P60 to P63 (N-ch open-drain)   |  | -0.3 to +6.5   | V    |
|                             | Vi3                      | P20 to P27, P121 to P124, P137, EXCLK, EXCLKS, RESET   |  | -0.3 to VDD + 0.3 <sup>Note 2</sup>  | V    |
| Output voltage              | VO1                      | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P130, P140, P146, P147 |  | -0.3 to VDD + 0.3 <sup>Note 2</sup>  | V    |
|                             | VO2                      | P20 to P27, P121, P122   |  | -0.3 to VDD + 0.3 <sup>Note 2</sup>  | V    |
| Analog input voltage        | VAI1                     | ANI16 to ANI19   |  | -0.3 to VDD + 0.3<br>and -0.3 to AVREFP + 0.3<br><sup>Notes 2, 3</sup>                                   | V    |
|                             | VAI2                     | ANI0 to ANI7   |  | -0.3 to VDD + 0.3<br>and -0.3 to AVREFP + 0.3<br><sup>Notes 2, 3</sup>                                   | V    |
| High-level output current   | IOH1                     | Per pin  | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147 | -40  | mA   |
|                             |                          | Total of all pins<br>-170 mA   | P00, P01, P40, P41, P120, P130, P140   | -70  | mA   |
|                             |                          |  | P10 to P17, P30, P31, P50, P51, P70 to P75, P146, P147                                       | -100   | mA   |
|                             | IOH2                     | Per pin  | P20 to P27, P121, P122   | -5   | mA   |
|                             |                          | Total of all pins  |  | -20  | mA   |
|                             | Low-level output current | IOL1   | Per pin  | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147 | 40   |
| Total of all pins<br>170 mA |                          |  | P00, P01, P40, P41, P120, P130, P140   | 70   | mA   |
|                             |                          |  | P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75, P146, P147                           | 100  | mA   |
| IOL2                        |                          | Per pin  | P20 to P27, P121, P122   | 10   | mA   |
|                             |                          | Total of all pins  |  | 20   | mA   |

**Note 1.** Connect the REGC pin to Vss via a capacitor (0.47 to 1  $\mu$ F). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

**Note 2.** This voltage must be no higher than 6.5 V.

**Note 3.** The voltage on a pin in use for A/D conversion must not exceed AVREFP + 0.3.

(Caution and Remarks are listed on the next page.)

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| Item                          | Symbols          | Conditions                       |                             | Ratings     | Unit |
|-------------------------------|------------------|----------------------------------|-----------------------------|-------------|------|
| Ambient operating temperature | TA               | In normal operation mode         | 3C: Industrial applications | -40 to +105 | °C   |
|                               |                  |                                  | 2D: Consumer applications   | -40 to +85  |      |
|                               |                  | In flash memory programming mode | 3C: Industrial applications | -40 to +105 |      |
|                               |                  |                                  | 2D: Consumer applications   | -40 to +85  |      |
| Storage temperature           | T <sub>stg</sub> |                                  |                             | -65 to +150 | °C   |

**Caution** Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

**Remark 1.** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

**Remark 2.** AVREFP refers to the positive reference voltage of the A/D converter.

**Remark 3.** The reference voltage is V<sub>SS</sub>.

## 2.2 Characteristics of the Oscillators

### 2.2.1 Characteristics of the X1 oscillator

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Resonator                               | Conditions | Min. | Typ. | Max. | Unit |
|---|---|------------|------|------|------|------|
| X1 clock oscillation allowable input cycle time <b>Note</b> | Ceramic resonator/<br>crystal resonator |            | 0.05 |      | 1    | μs   |

**Note** The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See **2.4 AC Characteristics** for instruction execution time.

**Caution** Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

### 2.2.2 Characteristics of the XT1 oscillator

(TA = -40 to +105°C, 2.4 V ≤ VDD ≤ 5.5 V (16- to 36-pin products), 1.6 V ≤ VDD ≤ 5.5 V (40- to 48-pin products), VSS = 0 V)

| Item   | Resonator         | Conditions | Min. | Typ.   | Max. | Unit |
|--|-------------------|------------|------|--------|------|------|
| XT1 clock oscillation frequency (f <sub>XT</sub> ) <b>Note</b> | Crystal resonator |            |      | 32.768 |      | kHz  |

**Note** The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. See **2.4 AC Characteristics** for instruction execution time.

### 2.2.3 Characteristics of the On-chip Oscillators

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Item   | Symbol         | Conditions                   |               |                                 | Min. | Typ.   | Max.                    | Unit |
|--|----------------|------------------------------|---------------|---------------------------------|------|--------|-------------------------|------|
| High-speed on-chip oscillator clock frequency                              | f <sub>H</sub> |                              |               |                                 | 1    |        | 32                      | MHz  |
| High-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>   |                | HIPREC = 1                   | +85 to +105°C | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V | -2.0 |        | +2.0                    | %    |
|  |                |                              |               | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V | -6.0 |        | +6.0                    | %    |
|  |                |                              | -20 to +85°C  | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V | -1.0 |        | +1.0                    | %    |
|  |                |                              |               | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V | -5.0 |        | +5.0                    | %    |
|  |                |                              | -40 to -20°C  | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V | -1.5 |        | +1.5                    | %    |
|  |                |                              |               | 1.6 V ≤ V <sub>DD</sub> ≤ 5.5 V | -5.5 |        | +5.5                    | %    |
|  |                | HIPREC = 0 <sup>Note 4</sup> |               |                                 | -15  |        | 0                       | %    |
| High-speed on-chip oscillator clock correction resolution                  |                |                              |               |                                 |      | 0.05   |                         | %    |
| Middle-speed on-chip oscillator clock frequency <sup>Note 2</sup>          | f <sub>M</sub> |                              |               |                                 | 1    |        | 4                       | MHz  |
| Middle-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup> |                |                              |               |                                 | -12  |        | +12                     | %    |
| Middle-speed on-chip oscillator clock correction resolution                |                |                              |               |                                 |      | 0.15   |                         | %    |
| Middle-speed on-chip oscillator frequency temperature coefficient          |                |                              |               |                                 |      |        | ±0.17 <sup>Note 3</sup> | %/°C |
| Low-speed on-chip oscillator clock frequency <sup>Note 2</sup>             | f <sub>L</sub> |                              |               |                                 |      | 32.768 |                         | kHz  |
| Low-speed on-chip oscillator clock frequency accuracy <sup>Note 1</sup>    |                |                              |               |                                 | -15  |        | +15                     | %    |
| Low-speed on-chip oscillator clock correction resolution                   |                |                              |               |                                 |      | 0.3    |                         | %    |
| Low-speed on-chip oscillator frequency temperature coefficient             |                |                              |               |                                 |      |        | ±0.21 <sup>Note 3</sup> | %/°C |

**Note 1.** The accuracy values were obtained in testing of this product.

**Note 2.** The listed values only indicate the characteristics of the oscillators. See **2.4 AC Characteristics** for instruction execution time.

**Note 3.** Guaranteed by characterization results.

**Note 4.** The listed condition applies when the setting of the FRQSEL3 bit is 1.



## 2.3 DC Characteristics

### 2.3.1 Characteristics of Pins

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/5)

| Item  | Symbol | Conditions   | Min.                | Typ. | Max. | Unit                 |    |
|---|--------|--|---------------------|------|------|----------------------|----|
| Allowable high-level output current <b>Note 1</b> | IOH1   | Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147 | 1.6 V ≤ VDD ≤ 5.5 V |      |      | -10.0 <b>Note 2</b>  | mA |
|   |        | Total of P00, P01, P40, P41, P120, P130, P140<br>(when duty ≤ 70% <b>Note 3</b> )                        | 4.0 V ≤ VDD ≤ 5.5 V |      |      | -55.0 <b>Note 4</b>  | mA |
|   |        |  | 2.7 V ≤ VDD < 4.0 V |      |      | -10.0                | mA |
|   |        |  | 1.8 V ≤ VDD < 2.7 V |      |      | -5.0                 | mA |
|   |        |  | 1.6 V ≤ VDD < 1.8 V |      |      | -2.5                 | mA |
|   |        | Total of P10 to P17, P30, P31, P50, P51, P70 to P75, P146, P147<br>(when duty ≤ 70% <b>Note 3</b> )      | 4.0 V ≤ VDD ≤ 5.5 V |      |      | -80.0 <b>Note 5</b>  | mA |
|   |        |  | 2.7 V ≤ VDD < 4.0 V |      |      | -19.0                | mA |
|   |        |  | 1.8 V ≤ VDD < 2.7 V |      |      | -10.0                | mA |
|   |        |  | 1.6 V ≤ VDD < 1.8 V |      |      | -5.0                 | mA |
|   |        | Total of all pins<br>(when duty ≤ 70% <b>Note 3</b> )  | 1.6 V ≤ VDD ≤ 5.5 V |      |      | -135.0 <b>Note 6</b> | mA |
|   | IOH2   | Per pin for P20 to P27, P121, P122   | 4.0 V ≤ VDD ≤ 5.5 V |      |      | -3.0 <b>Note 2</b>   | mA |
|   |        |  | 2.7 V ≤ VDD < 4.0 V |      |      | -1.0 <b>Note 2</b>   | mA |
|   |        |  | 1.8 V ≤ VDD < 2.7 V |      |      | -1.0 <b>Note 2</b>   | mA |
|   |        |  | 1.6 V ≤ VDD < 1.8 V |      |      | -0.5 <b>Note 2</b>   | mA |
|   |        | Total of all pins<br>(when duty ≤ 70% <b>Note 3</b> )  | 4.0 V ≤ VDD ≤ 5.5 V |      |      | -20.0                | mA |
|   |        |  | 2.7 V ≤ VDD < 4.0 V |      |      | -10.0                | mA |
| 1.8 V ≤ VDD < 2.7 V                               |        |  |                     |      | -5.0 | mA                   |    |
| 1.6 V ≤ VDD < 1.8 V                               |        |  |                     |      | -5.0 | mA                   |    |

**Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from the VDD pin to an output pin.

**Note 2.** The combination of these and other pins must also not exceed the value for maximum total current.

**Note 3.** The listed currents apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

• Total output current from the listed pins = (IOH × 0.7)/(n × 0.01)

Example when n = 80% and IOH = -10.0 mA

Total output current from the listed pins = (-10.0 × 0.7)/(80 × 0.01) ≈ -8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

**Note 4.** The maximum value is -30 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

**Note 5.** The maximum value is -50 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of +85 to +105°C.

**Note 6.** The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F102Gxx3xxxC) with an ambient operating temperature range of -40 to +85°C and of +85 to +105°C.

**Caution** The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.  
**P00, P10 to P15, P17, P50, P71, P72, P74, and P120**

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/5)

| Item   | Symbol  | Conditions  | Min.                | Typ. | Max.                    | Unit                   |    |
|--|---|---|---------------------|------|-------------------------|------------------------|----|
| Allowable low-level output current <sup>Note 1</sup> | IoL1  | Per pin for P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147            |                     |      | 20.0 <sup>Note 2</sup>  | mA                     |    |
|  |   | Per pin for P60 to P63  |                     |      | 15.0 <sup>Note 2</sup>  | mA                     |    |
|  |   | Total of P00, P01, P40, P41, P120, P130, P140<br>(when duty ≤ 70% <sup>Note 3</sup> )                               | 4.0 V ≤ VDD ≤ 5.5 V |      |                         | 70.0 <sup>Note 4</sup> | mA |
|  |   |   | 2.7 V ≤ VDD < 4.0 V |      |                         | 15.0                   | mA |
|  |   |   | 1.8 V ≤ VDD < 2.7 V |      |                         | 9.0                    | mA |
|  |   |   | 1.6 V ≤ VDD < 1.8 V |      |                         | 4.5                    | mA |
|  |   | Total of P10 to P17, P30, P31, P50, P51, P60 to P63, P70 to P75, P146, P147<br>(when duty ≤ 70% <sup>Note 3</sup> ) | 4.0 V ≤ VDD ≤ 5.5 V |      |                         | 80.0 <sup>Note 4</sup> | mA |
|  |   |   | 2.7 V ≤ VDD < 4.0 V |      |                         | 35.0                   | mA |
|  |   |   | 1.8 V ≤ VDD < 2.7 V |      |                         | 20.0                   | mA |
|  |   |   | 1.6 V ≤ VDD < 1.8 V |      |                         | 10.0                   | mA |
|  | Total of all pins<br>(when duty ≤ 70% <sup>Note 3</sup> ) |   |                     |      | 150.0 <sup>Note 5</sup> | mA                     |    |
|  | IoL2  | Per pin for P20 to P27, P121, P122  | 4.0 V ≤ VDD ≤ 5.5 V |      |                         | 8.5 <sup>Note 2</sup>  | mA |
|  |   |   | 2.7 V ≤ VDD < 4.0 V |      |                         | 1.5 <sup>Note 2</sup>  | mA |
|  |   |   | 1.8 V ≤ VDD < 2.7 V |      |                         | 0.6 <sup>Note 2</sup>  | mA |
|  |   |   | 1.6 V ≤ VDD < 1.8 V |      |                         | 0.4 <sup>Note 2</sup>  | mA |
|  |   | Total of all pins<br>(when duty ≤ 70% <sup>Note 3</sup> )   | 4.0 V ≤ VDD ≤ 5.5 V |      |                         | 20                     | mA |
|  |   |   | 2.7 V ≤ VDD < 4.0 V |      |                         | 20                     | mA |
|  |   |   | 1.8 V ≤ VDD < 2.7 V |      |                         | 15                     | mA |
| 1.6 V ≤ VDD < 1.8 V                                  |   |   |                     |      | 10                      | mA                     |    |

**Note 1.** Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the VSS pin.

**Note 2.** The combination of these and other pins must also not exceed the value for maximum total current.

**Note 3.** The listed currents apply when the duty cycle is no greater than 70%.

Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

• Total output current from the listed pins =  $(IoL \times 0.7)/(n \times 0.01)$

Example when n = 80% and IoL = 10.0 mA

Total output current from the listed pins =  $(10.0 \times 0.7)/(80 \times 0.01) \approx 8.7$  mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

**Note 4.** The maximum value is 40 mA in the products for industrial applications (R7F102Gxx3xxx) with an ambient operating temperature range of +85 to +105°C.

**Note 5.** The maximum value is 80 mA in the products for industrial applications (R7F102Gxx3xxx) with an ambient operating temperature range of +85 to +105°C.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/5)

| Item                | Symbol | Conditions   | Min.                                    | Typ.    | Max. | Unit    |   |
|---------------------|--------|--|---|---------|------|---------|---|
| Input voltage, high | VIH1   | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147 | Normal input buffer                     | 0.8 VDD |      | VDD     | V |
|                     | VIH2   | P01, P10, P11, P13 to P17, P41, P71  | TTL input buffer<br>4.0 V ≤ VDD ≤ 5.5 V | 2.2     |      | VDD     | V |
|                     |        |  | TTL input buffer<br>3.3 V ≤ VDD < 4.0 V | 2.0     |      | VDD     | V |
|                     |        |  | TTL input buffer<br>1.6 V ≤ VDD < 3.3 V | 1.5     |      | VDD     | V |
|                     | VIH3   | P20 to P27   |   | 0.7 VDD |      | VDD     | V |
|                     | VIH4   | P60 to P63   |   | 0.7 VDD |      | 6.0     | V |
|                     | VIH5   | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$                           |   | 0.8 VDD |      | VDD     | V |
| Input voltage, low  | VIL1   | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P140, P146, P147 | Normal input buffer                     | 0       |      | 0.2 VDD | V |
|                     | VIL2   | P01, P10, P11, P13 to P17, P41, P71  | TTL input buffer<br>4.0 V ≤ VDD ≤ 5.5 V | 0       |      | 0.8     | V |
|                     |        |  | TTL input buffer<br>3.3 V ≤ VDD < 4.0 V | 0       |      | 0.5     | V |
|                     |        |  | TTL input buffer<br>1.6 V ≤ VDD < 3.3 V | 0       |      | 0.32    | V |
|                     | VIL3   | P20 to P27   |   | 0       |      | 0.3 VDD | V |
|                     | VIL4   | P60 to P63   |   | 0       |      | 0.3 VDD | V |
|                     | VIL5   | P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$                           |   | 0       |      | 0.2 VDD | V |

**Caution** The maximum value of VIH of pins P00, P10 to P15, P17, P50, P71, P72, P74, and P120 is VDD, even in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(4/5)

| Item                               | Symbol              | Conditions   | Min.   | Typ.                                | Max. | Unit |     |
|------------------------------------|---------------------|--|--|-------------------------------------|------|------|-----|
| Output voltage, high               | VOH1                | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147 | 4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -10.0 mA   | VDD - 1.5                           |      |      | V   |
|                                    |                     |  | 4.0 V ≤ VDD ≤ 5.5 V, IOH1 = -3.0 mA  | VDD - 0.7                           |      |      | V   |
|                                    |                     |  | 2.7 V ≤ VDD ≤ 5.5 V, IOH1 = -2.0 mA  | VDD - 0.6                           |      |      | V   |
|                                    |                     |  | 1.8 V ≤ VDD ≤ 5.5 V, IOH1 = -1.5 mA  | VDD - 0.5                           |      |      | V   |
|                                    |                     |  | 1.6 V ≤ VDD < 5.5 V, IOH1 = -1.0 mA  | VDD - 0.5                           |      |      | V   |
|                                    | VOH2                | P20 to P27, P121, P122   | 4.0 V ≤ VDD ≤ 5.5 V, IOH2 = -3.0 mA  | VDD - 0.7                           |      |      | V   |
|                                    |                     |  | 2.7 V ≤ VDD < 4.0 V, IOH2 = -1.0 mA  | VDD - 0.5                           |      |      | V   |
|                                    |                     |  | 1.8 V ≤ VDD < 2.7 V, IOH2 = -1.0 mA  | VDD - 0.5                           |      |      | V   |
|                                    |                     |  | 1.6 V ≤ VDD < 1.8 V, IOH2 = -0.5 mA  | VDD - 0.5                           |      |      | V   |
|                                    | Output voltage, low | VOL1   | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120, P130, P140, P146, P147 | 4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 20.0 mA |      |      | 1.3 |
| 4.0 V ≤ VDD ≤ 5.5 V, IOL1 = 8.5 mA |                     |  |  |                                     |      | 0.7  | V   |
| 2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 3.0 mA |                     |  |  |                                     |      | 0.6  | V   |
| 2.7 V ≤ VDD ≤ 5.5 V, IOL1 = 1.5 mA |                     |  |  |                                     |      | 0.4  | V   |
| 1.8 V ≤ VDD ≤ 5.5 V, IOL1 = 0.6 mA |                     |  |  |                                     |      | 0.4  | V   |
| 1.6 V ≤ VDD ≤ 5.5 V, IOL1 = 0.3 mA |                     |  |  |                                     |      | 0.4  | V   |
| VOL2                               |                     | P20 to P27, P121, P122   | 4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 8.5 mA   |                                     |      | 0.7  | V   |
|                                    |                     |  | 2.7 V ≤ VDD < 4.0 V, IOL2 = 1.5 mA   |                                     |      | 0.5  | V   |
|                                    |                     |  | 1.8 V ≤ VDD < 2.7 V, IOL2 = 0.6 mA   |                                     |      | 0.4  | V   |
|                                    |                     |  | 1.6 V ≤ VDD < 1.8 V, IOL2 = 0.4 mA   |                                     |      | 0.4  | V   |
| VOL3                               |                     | P60 to P63   | 4.0 V ≤ VDD ≤ 5.5 V, IOL3 = 15.0 mA  |                                     |      | 2.0  | V   |
|                                    |                     |  | 4.0 V ≤ VDD ≤ 5.5 V, IOL3 = 5.0 mA   |                                     |      | 0.4  | V   |
|                                    |                     |  | 2.7 V ≤ VDD ≤ 5.5 V, IOL3 = 3.0 mA   |                                     |      | 0.4  | V   |
|                                    |                     |  | 1.8 V ≤ VDD ≤ 5.5 V, IOL3 = 2.0 mA   |                                     |      | 0.4  | V   |
|                                    |                     |  | 1.6 V ≤ VDD ≤ 5.5 V, IOL3 = 1.0 mA   |                                     |      | 0.4  | V   |

**Caution** P00, P10 to P15, P17, P50, P71, P72, P74, and P120 do not output high-level signals in the N-ch open-drain mode.

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(5/5)

| Item                        | Symbol | Conditions   | Min. | Typ. | Max. | Unit |
|-----------------------------|--------|--|------|------|------|------|
| Input leakage current, high | LIH1   | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147 |      |      | 0.5  | μA   |
|                             | LIH2   | P20 to P27, P137, $\overline{\text{RESET}}$  |      |      | 0.5  | μA   |
|                             | LIH3   | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   |      |      | 0.5  | μA   |
| Input leakage current, low  | LIL1   | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P60 to P63, P70 to P75, P120, P130, P140, P146, P147 |      |      | -0.5 | μA   |
|                             | LIL2   | P20 to P27, P137, $\overline{\text{RESET}}$  |      |      | -0.5 | μA   |
|                             | LIL3   | P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)   |      |      | -0.5 | μA   |
| On-chip pull-up resistance  | RU     | P00, P01, P10 to P17, P30, P31, P40, P41, P50, P51, P70 to P75, P120 to P122, P140, P146, P147           | 10   | 20   | 100  | kΩ   |

**Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

## 2.3.2 Characteristics of the supply current

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/4)

| Item  | Symbol           | Conditions                |  |  |  | Min.             | Typ.        | Max. | Unit |     |    |
|---|------------------|---------------------------|--|--|--|------------------|-------------|------|------|-----|----|
| Supply current<br>Note 1                                      | IDD1             | Operating mode            | HS (high-speed main) mode                                      | f <sub>IH</sub> = 32 MHz <sup>Note 2</sup>                     | Basic operation                            | VDD = 5.0 V      |             | 1.2  |      | mA  |    |
|   |                  |                           |  |  |  | VDD = 1.8 V      |             | 1.2  |      |     |    |
|   |                  |                           |  | Normal operation   | VDD = 5.0 V                                |                  | 2.7         | 4.6  | mA   |     |    |
|   |                  |                           |  |  | VDD = 1.8 V                                |                  | 2.7         | 4.6  |      |     |    |
|   |                  |                           |  | LS (low-speed main) mode                                       | f <sub>IH</sub> = 24 MHz <sup>Note 2</sup> | Normal operation | VDD = 5.0 V |      | 2.0  | 3.5 | mA |
|   |                  |                           |  |  |  |                  | VDD = 1.8 V |      | 2.0  | 3.5 |    |
|   |                  |                           | Normal operation   |  | VDD = 5.0 V                                |                  | 1.5         | 2.5  | mA   |     |    |
|   |                  |                           |  |  | VDD = 1.8 V                                |                  | 1.5         | 2.5  |      |     |    |
|   |                  |                           | f <sub>IM</sub> = 4 MHz <sup>Note 3</sup>                      |  | Normal operation                           | VDD = 5.0 V      |             | 0.4  | 0.7  | mA  |    |
|   |                  |                           |  |  |  | VDD = 1.6 V      |             | 0.4  | 0.7  |     |    |
|   |                  |                           | LP (low-power main) mode                                       | f <sub>IM</sub> = 2 MHz <sup>Note 3</sup>                      | Normal operation                           | VDD = 5.0 V      |             | 179  | 300  | μA  |    |
|   |                  |                           |  |  |  | VDD = 1.6 V      |             | 179  | 300  |     |    |
|   |                  | Normal operation          |  | VDD = 5.0 V  |  | 100              | 163         | μA   |      |     |    |
|   |                  |                           |  | VDD = 1.6 V  |  | 100              | 163         |      |      |     |    |
|   |                  | HS (high-speed main) mode |  | f <sub>MX</sub> = 20 MHz <sup>Note 4</sup> , Square wave input | Normal operation                           | VDD = 5.0 V      |             | 1.7  | 2.9  | mA  |    |
|   |                  |                           |  |  |  | VDD = 1.8 V      |             | 1.6  | 2.8  |     |    |
|   |                  | LS (low-speed main) mode  | f <sub>MX</sub> = 20 MHz <sup>Note 4</sup> , Square wave input | Normal operation   | VDD = 5.0 V                                |                  | 1.5         | 2.7  | mA   |     |    |
|   |                  |                           |  |  | VDD = 1.8 V                                |                  | 1.5         | 2.7  |      |     |    |
|   |                  |                           | Normal operation   | VDD = 5.0 V  |  | 1.7              | 3.0         | mA   |      |     |    |
|   |                  |                           |  | VDD = 1.8 V  |  | 1.7              | 3.0         |      |      |     |    |
|   |                  |                           | f <sub>MX</sub> = 10 MHz <sup>Note 4</sup> , Square wave input | Normal operation   | VDD = 5.0 V                                |                  | 0.8         | 1.5  | mA   |     |    |
|   |                  |                           |  |  | VDD = 1.8 V                                |                  | 0.8         | 1.4  |      |     |    |
|   |                  |                           | Normal operation   | VDD = 5.0 V  |  | 0.9              | 1.6         | mA   |      |     |    |
|   |                  |                           |  | VDD = 1.8 V  |  | 0.9              | 1.6         |      |      |     |    |
| f <sub>MX</sub> = 8 MHz <sup>Note 4</sup> , Square wave input | Normal operation |                           | VDD = 5.0 V  |  | 0.7  | 1.2              | mA          |      |      |     |    |
|   |                  |                           | VDD = 1.8 V  |  | 0.7  | 1.2              |             |      |      |     |    |
| Normal operation  | VDD = 5.0 V      |                           |  | 0.8  | 1.3  | mA               |             |      |      |     |    |
|   | VDD = 1.8 V      |                           |  | 0.8  | 1.3  |                  |             |      |      |     |    |

**Note 1.** The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

**Note 2.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

**Remark 1.** f<sub>H</sub>: High-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>M</sub>: Middle-speed on-chip oscillator clock frequency

**Remark 3.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 4.** The typical value for the ambient operating temperature (T<sub>A</sub>) is +25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

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| Item                     | Symbol | Conditions     |                                |  |                  |             | Min. | Typ. | Max. | Unit |
|--------------------------|--------|----------------|--------------------------------|--|------------------|-------------|------|------|------|------|
| Supply current<br>Note 1 | IDD1   | Operating mode | Subsystem clock operation mode | fsUB = 32.768 kHzNote 2,<br>Low-speed on-chip oscillator operation | Normal operation | TA = -40°C  |      | 2.9  | 4.7  | μA   |
|                          |        |                |                                |  |                  | TA = +25°C  |      | 3.1  | 4.9  |      |
|                          |        |                |                                |  |                  | TA = +50°C  |      | 3.3  | 6.3  |      |
|                          |        |                |                                |  |                  | TA = +70°C  |      | 3.6  | 9.6  |      |
|                          |        |                |                                |  |                  | TA = +85°C  |      | 4.1  | 15.2 |      |
|                          |        |                |                                |  |                  | TA = +105°C |      | 5.4  | 32.2 |      |
|                          |        |                |                                | fsUB = 32.768 kHzNote 3,<br>Square wave input                      | Normal operation | TA = -40°C  |      | 2.9  | 4.9  | μA   |
|                          |        |                |                                |  |                  | TA = +25°C  |      | 3.0  | 5.0  |      |
|                          |        |                |                                |  |                  | TA = +50°C  |      | 3.2  | 6.4  |      |
|                          |        |                |                                |  |                  | TA = +70°C  |      | 3.5  | 9.7  |      |
|                          |        |                |                                |  |                  | TA = +85°C  |      | 4.0  | 15.3 |      |
|                          |        |                |                                | fsUB = 32.768 kHzNote 3,<br>Resonator connection                   | Normal operation | TA = -40°C  |      | 2.9  | 4.9  | μA   |
|                          |        |                |                                |  |                  | TA = +25°C  |      | 3.1  | 5.3  |      |
|                          |        |                |                                |  |                  | TA = +50°C  |      | 3.3  | 6.7  |      |
|                          |        |                |                                |  |                  | TA = +70°C  |      | 3.6  | 10.2 |      |
| TA = +85°C               |        | 4.1            | 15.8                           |  |                  |             |      |      |      |      |
|                          |        | TA = +105°C    |                                | 5.5  | 33.3             |             |      |      |      |      |

**Note 1.** The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. In the subsystem clock operation mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

**Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the currents flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Remark 1.** fil: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)



(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

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| Item  | Symbol                | Conditions |  |  |             | Min. | Typ. | Max. | Unit |
|---|-----------------------|------------|--|--|-------------|------|------|------|------|
| Supply current<br><b>Note 1</b>                                 | IDD2<br><b>Note 2</b> | HALT mode  | HS<br>(high-speed main)<br>mode                              | f <sub>IH</sub> = 32 MHz <b>Note 3</b>                           | VDD = 5.0 V |      | 0.49 | 1.87 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.49 | 1.87 |      |
|   |                       |            | LS<br>(low-speed main)<br>mode                               | f <sub>IH</sub> = 24 MHz <b>Note 3</b>                           | VDD = 5.0 V |      | 0.41 | 1.46 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.40 | 1.45 |      |
|   |                       |            |  | f <sub>IH</sub> = 16 MHz <b>Note 3</b>                           | VDD = 5.0 V |      | 0.42 | 1.15 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.41 | 1.14 |      |
|   |                       |            |  | f <sub>IM</sub> = 4 MHz <b>Note 4</b>                            | VDD = 5.0 V |      | 0.08 | 0.26 | mA   |
|   |                       |            |  |  | VDD = 1.6 V |      | 0.07 | 0.25 |      |
|   |                       |            | LP<br>(low-power main)<br>mode                               | f <sub>IM</sub> = 2 MHz <b>Note 4</b>                            | VDD = 5.0 V |      | 29   | 115  | μA   |
|   |                       |            |  |  | VDD = 1.6 V |      | 29   | 115  |      |
|   |                       |            |  | f <sub>IM</sub> = 1 MHz <b>Note 4</b>                            | VDD = 5.0 V |      | 25   | 71   | μA   |
|   |                       |            |  |  | VDD = 1.6 V |      | 25   | 71   |      |
|   |                       |            | HS<br>(high-speed main)<br>mode                              | f <sub>MX</sub> = 20 MHz <b>Note 5</b> ,<br>Square wave input    | VDD = 5.0 V |      | 0.19 | 1.03 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.16 | 0.99 |      |
|   |                       |            | LS<br>(low-speed main)<br>mode                               | f <sub>MX</sub> = 20 MHz <b>Note 5</b> ,<br>Square wave input    | VDD = 5.0 V |      | 0.19 | 1.03 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.16 | 0.99 |      |
|   |                       |            |  | f <sub>MX</sub> = 20 MHz <b>Note 5</b> ,<br>Resonator connection | VDD = 5.0 V |      | 0.38 | 1.26 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.37 | 1.25 |      |
|   |                       |            |  | f <sub>MX</sub> = 10 MHz <b>Note 5</b> ,<br>Square wave input    | VDD = 5.0 V |      | 0.12 | 0.54 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.10 | 0.52 |      |
|   |                       |            |  | f <sub>MX</sub> = 10 MHz <b>Note 5</b> ,<br>Resonator connection | VDD = 5.0 V |      | 0.22 | 0.67 | mA   |
|   |                       |            |  |  | VDD = 1.8 V |      | 0.22 | 0.66 |      |
|   |                       |            | f <sub>MX</sub> = 8 MHz <b>Note 5</b> ,<br>Square wave input | VDD = 5.0 V  |             | 0.10 | 0.45 | mA   |      |
|   |                       |            |  | VDD = 1.8 V  |             | 0.09 | 0.43 |      |      |
| f <sub>MX</sub> = 8 MHz <b>Note 5</b> ,<br>Resonator connection | VDD = 5.0 V           |            | 0.20   | 0.57   | mA          |      |      |      |      |
|   | VDD = 1.8 V           |            | 0.20   | 0.56   |             |      |      |      |      |

**Note 1.** The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

**Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

**Note 3.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 4.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

**Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

**Remark 1.** f<sub>H</sub>: High-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>M</sub>: Middle-speed on-chip oscillator clock frequency

**Remark 3.** f<sub>MX</sub>: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

**Remark 4.** The typical value for the ambient operating temperature (T<sub>A</sub>) is +25°C unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

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| Item                     | Symbol         | Conditions  |                                |  | Min.        | Typ. | Max.  | Unit  |    |
|--------------------------|----------------|-------------|--------------------------------|--|-------------|------|-------|-------|----|
| Supply current<br>Note 1 | IDD2<br>Note 2 | HALT mode   | Subsystem clock operation mode | fsUB = 32.768 kHz<br>Note 3,<br>Low-speed on-chip oscillator operation | TA = -40°C  |      | 0.48  | 1.84  | μA |
|                          |                |             |                                |  | TA = +25°C  |      | 0.57  | 1.89  |    |
|                          |                |             |                                |  | TA = +50°C  |      | 0.67  | 3.19  |    |
|                          |                |             |                                |  | TA = +70°C  |      | 0.91  | 6.33  |    |
|                          |                |             |                                |  | TA = +85°C  |      | 1.69  | 12.66 |    |
|                          |                |             |                                |  | TA = +105°C |      | 3.04  | 29.93 |    |
|                          |                |             |                                | fsUB = 32.768 kHz,<br>Square wave input<br>Note 4                      | TA = -40°C  |      | 0.20  | 1.72  | μA |
|                          |                |             |                                |  | TA = +25°C  |      | 0.29  | 1.75  |    |
|                          |                |             |                                |  | TA = +50°C  |      | 0.49  | 3.75  |    |
|                          |                |             |                                |  | TA = +70°C  |      | 0.90  | 8.16  |    |
|                          |                |             |                                |  | TA = +85°C  |      | 1.41  | 14.55 |    |
|                          |                |             |                                |  | TA = +105°C |      | 2.79  | 32.65 |    |
|                          |                |             |                                | fsUB = 32.768 kHz,<br>Resonator connection<br>Note 5                   | TA = -40°C  |      | 0.21  | 1.79  | μA |
|                          |                |             |                                |  | TA = +25°C  |      | 0.33  | 2.03  |    |
|                          |                |             |                                |  | TA = +50°C  |      | 0.44  | 3.40  |    |
|                          |                |             |                                |  | TA = +70°C  |      | 0.97  | 8.65  |    |
|                          |                |             |                                |  | TA = +85°C  |      | 1.48  | 15.04 |    |
|                          |                |             |                                |  | TA = +105°C |      | 2.92  | 33.56 |    |
| IDD3                     | STOP mode      | TA = -40°C  |                                |  |             | 0.15 | 1.10  | μA    |    |
|                          |                | TA = +25°C  |                                |  |             | 0.20 | 1.10  |       |    |
|                          |                | TA = +50°C  |                                |  |             | 0.40 | 2.40  |       |    |
|                          |                | TA = +70°C  |                                |  |             | 0.80 | 5.50  |       |    |
|                          |                | TA = +85°C  |                                |  |             | 1.30 | 11.00 |       |    |
|                          |                | TA = +105°C |                                |  |             | 2.70 | 28.00 |       |    |

**Note 1.** The listed currents are the total currents flowing into VDD, including the input leakage currents flowing when the level of the input pin is fixed to VDD or VSS. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

**Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

**Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped. They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). They do not include the current flowing into the RTC, 32-bit interval timer, and watchdog timer.

**Remark 1.** fL: Low-speed on-chip oscillator clock frequency

**Remark 2.** fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)

Peripheral Functions

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Symbol                    | Conditions                       |  | Min.  | Typ.  | Max. | Unit |    |
|---|---------------------------|----------------------------------|--|---|-------|------|------|----|
| High-speed on-chip oscillator operating current       | IFIH <b>Note 1</b>        |                                  |  |   | 380   |      | μA   |    |
| Middle-speed on-chip oscillator operating current     | IFIM <b>Note 1</b>        |                                  |  |   | 20    |      | μA   |    |
| Low-speed on-chip oscillator operating current        | FIL <b>Note 1</b>         |                                  |  |   | 0.3   |      | μA   |    |
| RTC operating current                                 | IRTC <b>Notes 1, 2, 3</b> | fRTCCLK = 32.768 kHz             |  |   | 0.005 |      | μA   |    |
|   |                           | fRTCCLK = 128 Hz                 |  |   | 0.002 |      | μA   |    |
| 32-bit interval timer operating current               | IIT <b>Notes 1, 2, 4</b>  |                                  |  |   | 0.04  |      | μA   |    |
| Watchdog timer operating current                      | IWDT <b>Notes 1, 2, 5</b> | fIL = 32.768 kHz (typ.)          |  |   | 0.32  |      | μA   |    |
| A/D converter operating current                       | IADC <b>Notes 1, 6</b>    | When conversion at maximum speed | Normal mode, AVREFF = VDD = 5.0 V      |   | 1.3   | 1.7  | mA   |    |
|   |                           |                                  | Low voltage mode, AVREFF = VDD = 3.0 V |   | 0.5   | 0.7  | mA   |    |
| A/D converter internal reference voltage current      | IADREF <b>Note 1</b>      |                                  |  |   | 100   |      | μA   |    |
| Temperature sensor operating current                  | ITMPS <b>Note 1</b>       |                                  |  |   | 110   |      | μA   |    |
| LVD operating current                                 | ILVD0 <b>Notes 1, 7</b>   |                                  |  |   | 0.02  |      | μA   |    |
|   | ILVD1 <b>Notes 1, 7</b>   |                                  |  |   | 0.02  |      | μA   |    |
| Self-programming operating current                    | IFSP <b>Notes 1, 8</b>    |                                  |  |   | 2.5   | 12.2 | mA   |    |
| Data flash rewrite operating current                  | IBGO <b>Notes 1, 9</b>    |                                  |  |   | 2.5   | 12.2 | mA   |    |
| SNOOZE mode sequencer operating current               | ISMS <b>Notes 1, 10</b>   | fIH = 32 MHz                     |  |   | 0.93  |      | mA   |    |
|   |                           | fIL = 32.768 kHz                 |  |   | 0.97  |      | μA   |    |
| SNOOZE operating current                              | ISNOZ <b>Note 1</b>       | fIH=32 MHz                       | ADC to be in use                       | The ADC is shifting from the STOP mode to the SNOOZE mode. <b>Note 11</b> |       | 0.5  | 0.7  | mA |
|   |                           |                                  |  | The ADC is operating in the low-voltage mode. AVREFF = VDD = 3.0 V        |       | 0.9  | 1.4  |    |
|   |                           |                                  |  | Simplified SPI (CSI)/UART to be in use                                    |       | 0.6  | 0.79 | mA |
|   |                           |                                  |  | SMS <b>Note 13</b>  |       | 1.4  |      | mA |
| Low-speed peripheral clock supply current             | ISXP <b>Notes 1, 12</b>   | RTCLPC = 0                       |  |   | 0.22  |      | μA   |    |
| Operating current of the true random number generator | ITRNG <b>Note 1</b>       |                                  |  |   | 1.1   |      | mA   |    |

(Notes and Remarks are listed on the next page.)

- Note 1.** This current flows into VDD.
- Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
- Note 3.** This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IRTC, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.
- Note 4.** This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IIT, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current.
- Note 5.** This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.
- Note 6.** This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter is operating or in the HALT mode.
- Note 7.** This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- Note 8.** This current only flows during self-programming.
- Note 9.** This current only flows while the data flash memory is being rewritten.
- Note 10.** This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and ISMS, when the SNOOZE mode sequencer is operating or in the HALT mode.
- Note 11.** For shift time to the SNOOZE mode, see **20.3.3 SNOOZE mode** in the RL78/G22 User's Manual.
- Note 12.** This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the subsystem clock X (fsx) selected as the CPU clock, while the subsystem clock X (fsx) is oscillating.
- Note 13.** The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to IDD1. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.

**Remark 1.** f<sub>IL</sub>: Low-speed on-chip oscillator clock frequency

**Remark 2.** f<sub>SX</sub>: Subsystem clock X frequency

**Remark 3.** f<sub>CLK</sub>: CPU/peripheral hardware clock frequency

**Remark 4.** The typical value for the ambient operating temperature (T<sub>A</sub>) is +25°C unless otherwise specified.

## 2.4 AC Characteristics

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Symbol          | Conditions  |                                 | Min.                           | Typ.                | Max.    | Unit               |    |
|---|-----------------|---|---------------------------------|--------------------------------|---------------------|---------|--------------------|----|
| Instruction cycle<br>(minimum instruction<br>execution time)        | TCY             | Main system clock<br>(fMAIN) operation                | HS<br>(high-speed main)<br>mode | 1.8 V ≤ VDD ≤ 5.5 V            | 0.03125             | 1       | μs                 |    |
|   |                 |   |                                 | 1.6 V ≤ VDD ≤ 1.8 V            | 0.25                | 1       | μs                 |    |
|   |                 |   | LS<br>(low-speed main)<br>mode  | 1.8 V ≤ VDD ≤ 5.5 V            | 0.04167             | 1       | μs                 |    |
|   |                 |   |                                 | 1.6 V ≤ VDD ≤ 1.8 V            | 0.25                | 1       | μs                 |    |
|   |                 | LP<br>(low-power main)<br>mode                        | 1.6 V ≤ VDD ≤ 5.5 V             | 0.5                            | 1                   | μs      |                    |    |
|   |                 | Subsystem clock (fSUB) operation                      |                                 | 1.6 V ≤ VDD ≤ 5.5 V            | 26.041              | 30.5    | 31.3               | μs |
|   |                 | In the<br>self-programming<br>mode                    | HS<br>(high-speed main)<br>mode | 1.8 V ≤ VDD ≤ 5.5 V            | 0.03125             | 1       | μs                 |    |
|   |                 |   |                                 | LS<br>(low-speed main)<br>mode | 1.8 V ≤ VDD ≤ 5.5 V | 0.04167 | 1                  | μs |
| External system clock<br>frequency                                  | fEX             | 1.8 V ≤ VDD ≤ 5.5 V                                   |                                 | 1.0                            |                     | 20.0    | MHz                |    |
|   |                 | 1.6 V ≤ VDD < 1.8 V                                   |                                 | 1.0                            |                     | 4.0     | MHz                |    |
|   | fEXS            |   |                                 | 32                             |                     | 38.4    | kHz                |    |
| External system clock<br>input high-level width,<br>low-level width | tEXH,<br>tEXL   | 1.8 V ≤ VDD ≤ 5.5 V                                   |                                 | 24                             |                     |         | ns                 |    |
|   |                 | 1.6 V ≤ VDD < 1.8 V                                   |                                 | 120                            |                     |         | ns                 |    |
|   | tEXHS,<br>tEXLS |   |                                 | 13.7                           |                     |         | μs                 |    |
| Ti00 to Ti07 input<br>high-level width, low-level<br>width          | tTIH,<br>tTIL   |   |                                 | 1/fMCK<br>+ 10                 |                     |         | ns <sup>Note</sup> |    |
| TO00 to TO07 output<br>frequency                                    | fTO             | HS (high-speed main) mode<br>LS (low-speed main) mode | 4.0 V ≤ VDD ≤ 5.5 V             |                                |                     | 16      | MHz                |    |
|   |                 |   | 2.7 V ≤ VDD < 4.0 V             |                                |                     | 8       | MHz                |    |
|   |                 |   | 1.8 V ≤ VDD < 2.7 V             |                                |                     | 4       | MHz                |    |
|   |                 |   | 1.6 V ≤ VDD < 1.8 V             |                                |                     | 2       | MHz                |    |
|   |                 | LP (low-power main) mode                              | 1.6 V ≤ VDD ≤ 5.5 V             |                                |                     | 2       | MHz                |    |
| PCLBUZ0, PCLBUZ1<br>output frequency                                | fPCL            | HS (high-speed main) mode<br>LS (low-speed main) mode | 4.0 V ≤ VDD ≤ 5.5 V             |                                |                     | 16      | MHz                |    |
|   |                 |   | 2.7 V ≤ VDD < 4.0 V             |                                |                     | 8       | MHz                |    |
|   |                 |   | 1.8 V ≤ VDD < 2.7 V             |                                |                     | 4       | MHz                |    |
|   |                 |   | 1.6 V ≤ VDD < 1.8 V             |                                |                     | 2       | MHz                |    |
|   |                 | LP (low-power main) mode                              | 1.6 V ≤ VDD < 1.8 V             |                                |                     | 2       | MHz                |    |
| Interrupt input high-level<br>width, low-level width                | tINTH,<br>tINTL | INTP0 to INTP6, INTP8, INTP9                          |                                 | 1.6 V ≤ VDD ≤ 5.5 V            | 1                   |         | μs                 |    |
| Key interrupt input low-<br>level width                             | tKRH,<br>tKRL   | KR0 to KR5  |                                 | 1.8 V ≤ VDD ≤ 5.5 V            | 250                 |         | ns                 |    |
|   |                 |   |                                 | 1.6 V ≤ VDD < 1.8 V            | 1                   |         | μs                 |    |
| RESET low-level width   | tRSL            |   |                                 |                                | 10                  |         | μs                 |    |

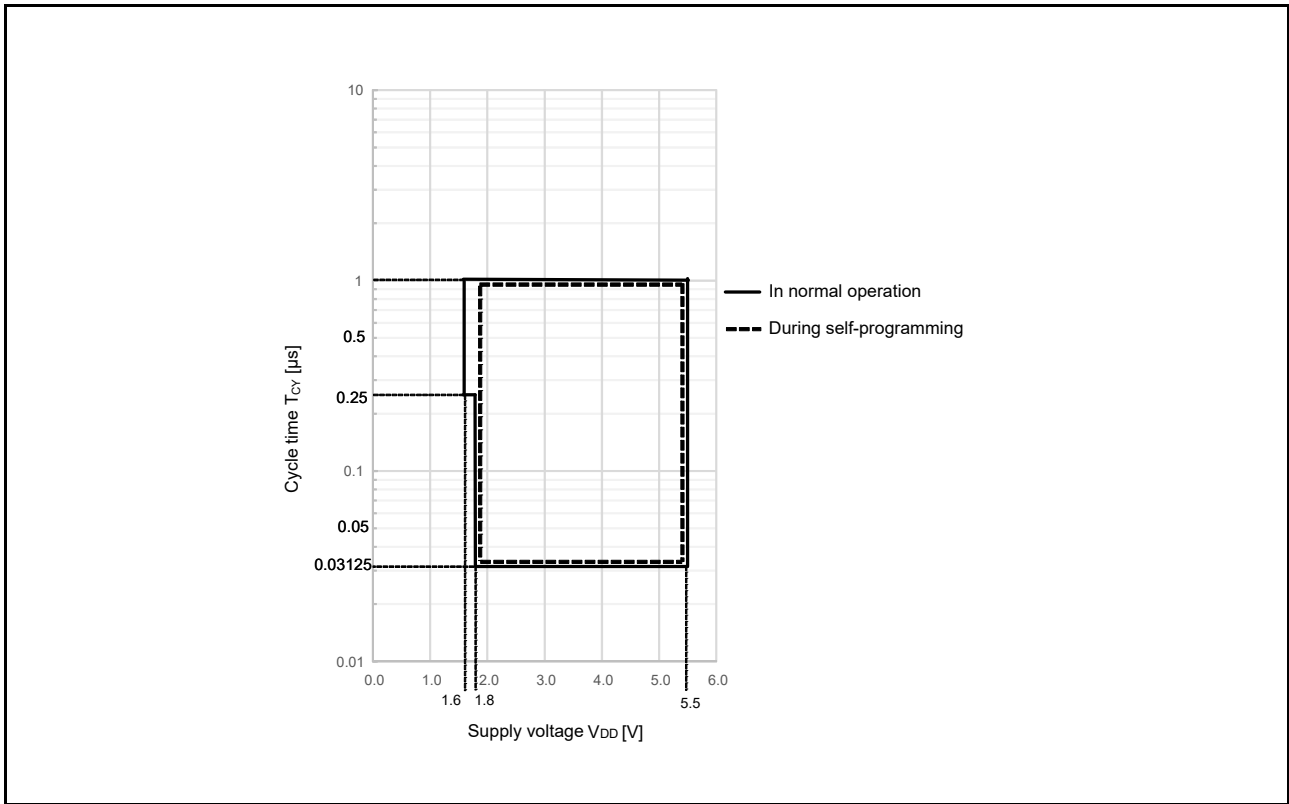
**Remark** fMCK: Timer array unit operating clock frequency

To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn).

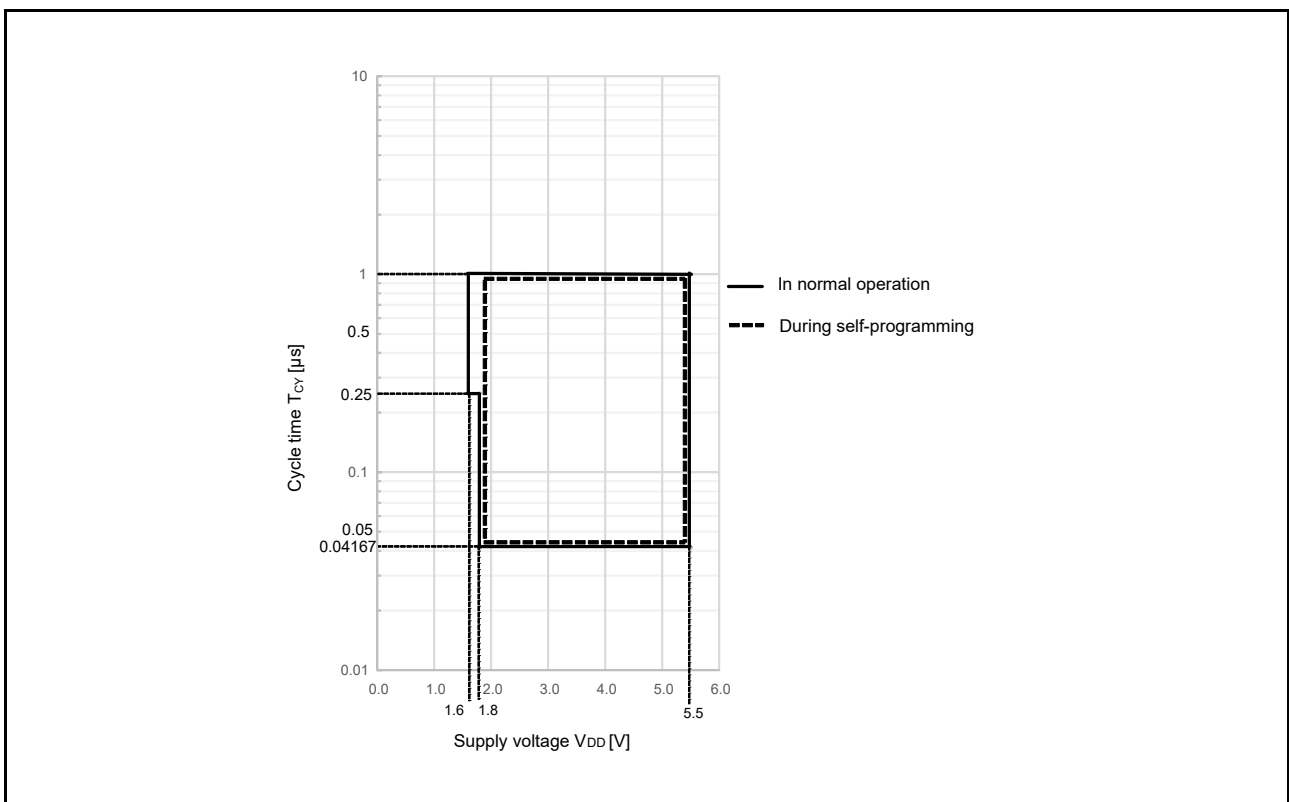
m: Unit number (m = 0), n: Channel number (n = 0 to 3)

- Minimum Instruction Execution Time during Main System Clock Operation

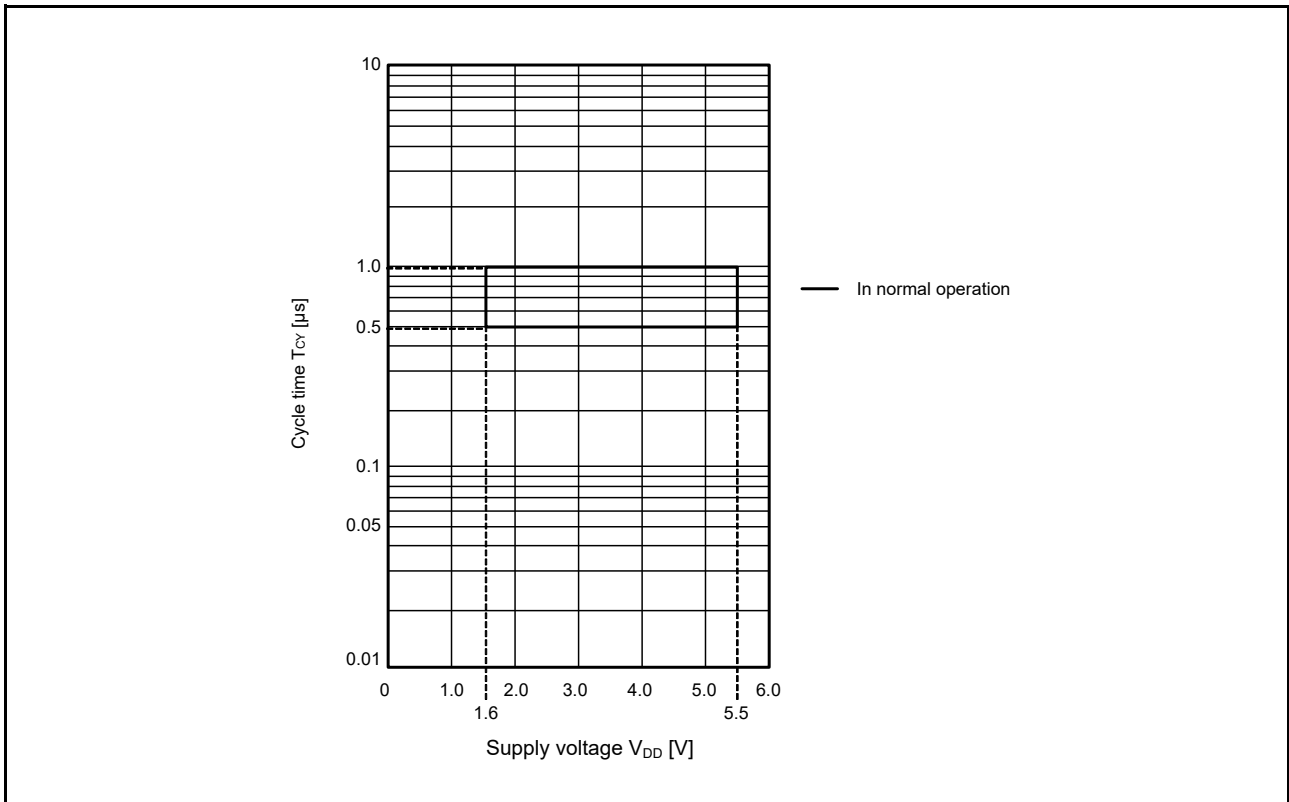
(a)  $T_{CY}$  vs  $V_{DD}$  in HS (high-speed main) mode



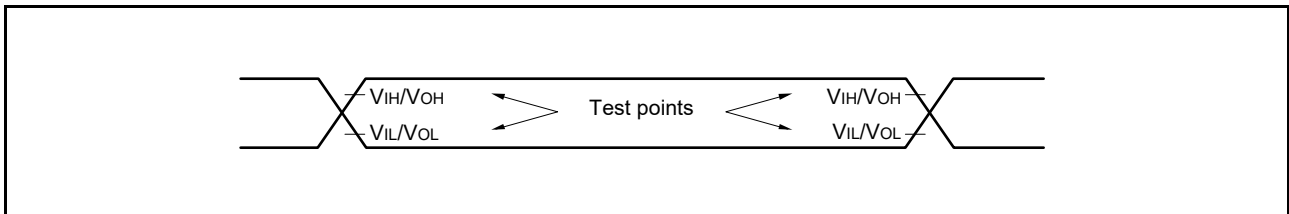
(b)  $T_{CY}$  vs  $V_{DD}$  in LS (low-speed main) mode



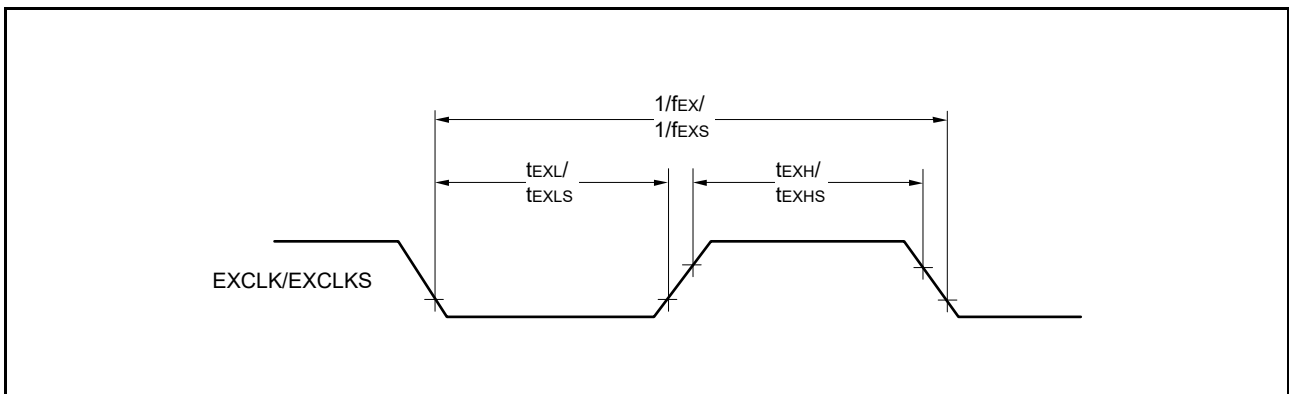
(c)  $T_{CY}$  vs  $V_{DD}$  in LP (low-power main) mode



(d) AC Timing Test Points

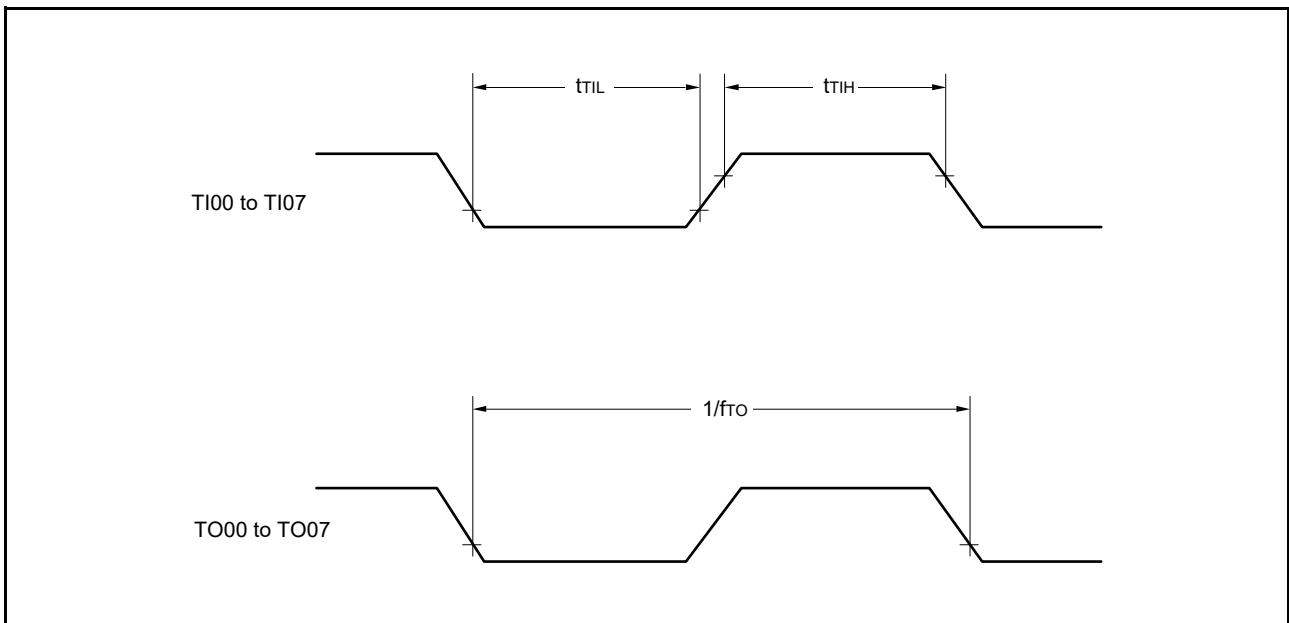


(e) External System Clock Timing

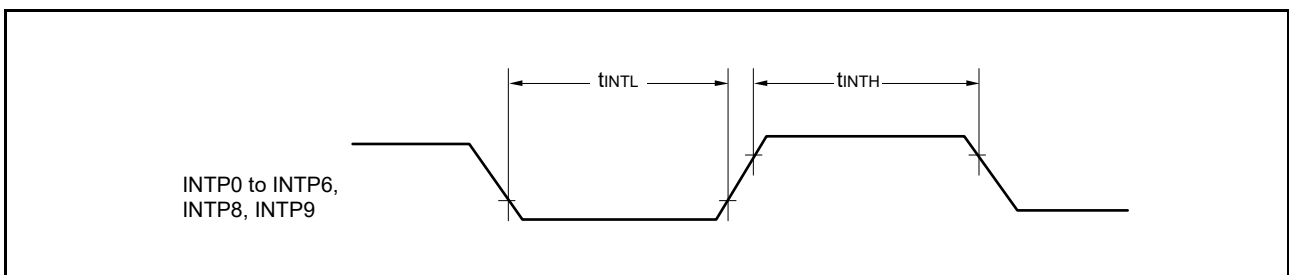




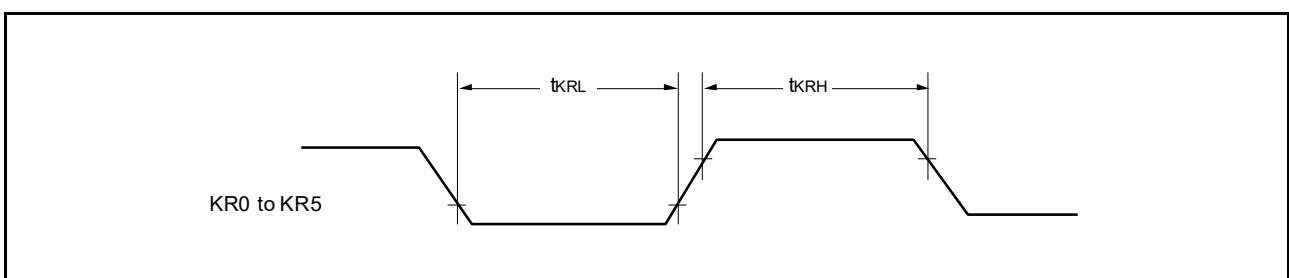
(f) TI/TO Timing



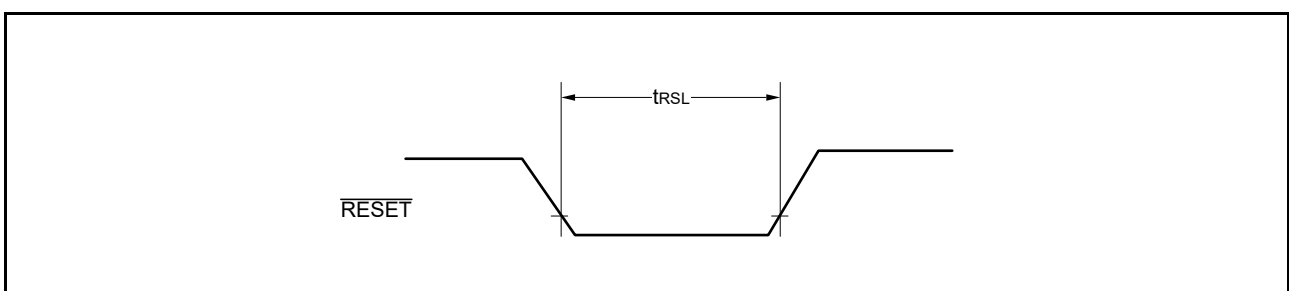
(g) Interrupt Request Input Timing



(h) Key Interrupt Input Timing

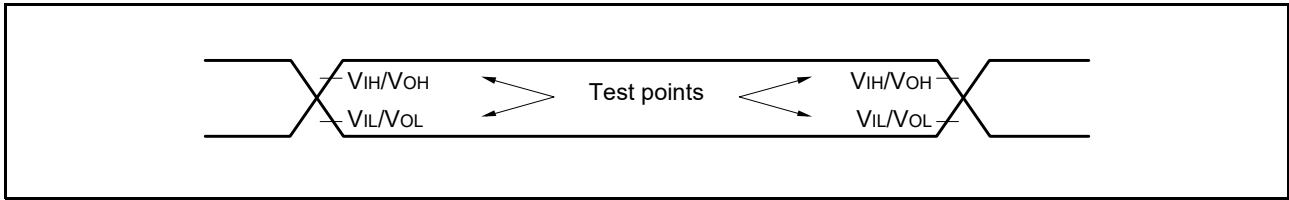


(i)  $\overline{\text{RESET}}$  Input Timing



## 2.5 Characteristics of the Peripheral Functions

### AC Timing Test Points



### 2.5.1 Serial array unit

(1) In UART communications with devices operating at same voltage levels

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                    | Symbol | Conditions   | HS<br>(High-Speed Main)<br>Mode |        | LS<br>(Low-Speed Main)<br>Mode |        | LP<br>(Low-Power Main)<br>Mode |        | Unit |
|-------------------------|--------|--|---------------------------------|--------|--------------------------------|--------|--------------------------------|--------|------|
|                         |        |  | Min.                            | Max.   | Min.                           | Max.   | Min.                           | Max.   |      |
| Transfer rate<br>Note 1 |        | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                         |                                 | fMCK/6 |                                | fMCK/6 |                                | fMCK/6 | bps  |
|                         |        | Theoretical value of the maximum transfer rate<br>fMCK = fCLK>Note 2 |                                 | 5.3    |                                | 4      |                                | 0.33   | Mbps |

**Note 1.** The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are as follows.

HS (high-speed main) mode: 32 MHz ( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

4 MHz ( $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

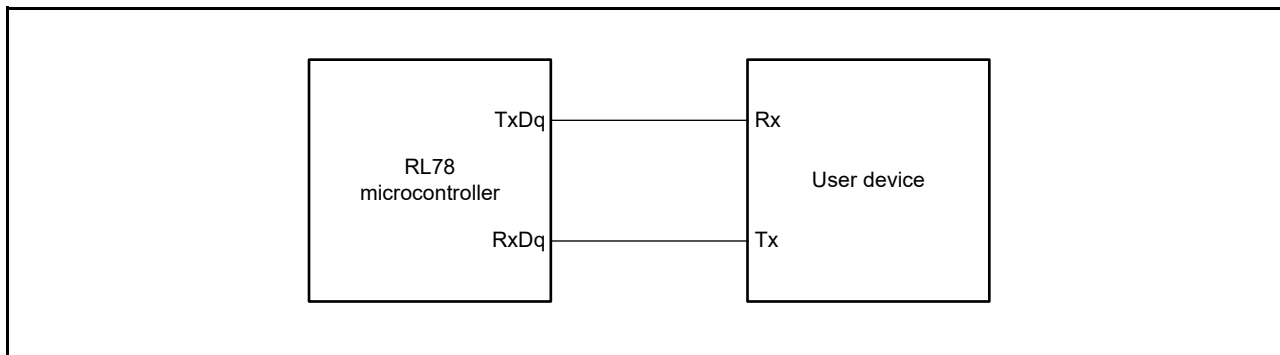
LS (low-speed main) mode: 24 MHz ( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

4 MHz ( $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

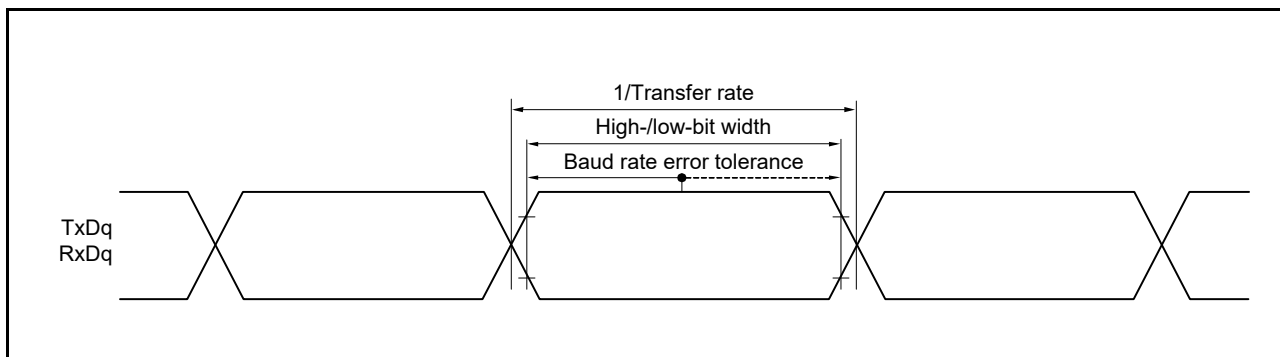
LP (low-power main) mode: 2 MHz ( $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )

**Caution** Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

(a) Connection in the UART communications with devices operating at same voltage levels



(b) Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)



**Remark 1.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**Remark 2.** f<sub>MCK</sub>: Serial array unit operation clock frequency

To set this operating clock, set the CKSMn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

(2) In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +85°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Symbol     | Conditions                  |                     | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|---|------------|-----------------------------|---------------------|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|   |            |                             |                     | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |
| SCKp cycle time                                       | tkCY1      | tkCY1 ≥ 2/fCLK              | 4.0 V ≤ VDD ≤ 5.5 V | 62.5                            |      | 83.3                           |      | 1000                           |      | ns   |
|   |            |                             | 2.7 V ≤ VDD ≤ 5.5 V | 83.3                            |      | 125                            |      | 1000                           |      | ns   |
| SCKp high-/low-level width                            | tkH1, tkL1 | 4.0 V ≤ VDD ≤ 5.5 V         |                     | tkCY1/2 - 7                     |      | tkCY1/2 - 10                   |      | tkCY1/2 - 50                   |      | ns   |
|   |            | 2.7 V ≤ VDD ≤ 5.5 V         |                     | tkCY1/2 - 10                    |      | tkCY1/2 - 15                   |      | tkCY1/2 - 50                   |      | ns   |
| Slp setup time (to SCKp↑) <sup>Note 1</sup>           | tsIK1      | 4.0 V ≤ VDD ≤ 5.5 V         |                     | 23                              |      | 33                             |      | 110                            |      | ns   |
|   |            | 2.7 V ≤ VDD ≤ 5.5 V         |                     | 33                              |      | 50                             |      | 110                            |      | ns   |
| Slp hold time (from SCKp↑) <sup>Note 1</sup>          | tkSI1      | 2.7 V ≤ VDD ≤ 5.5 V         |                     | 10                              |      | 10                             |      | 10                             |      | ns   |
| Delay time from SCKp↓ to SOp output <sup>Note 2</sup> | tkSO1      | C = 20 pF <sup>Note 3</sup> |                     |                                 | 10   |                                | 10   |                                | 10   | ns   |

**Note 1.** The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SCKp and SOp output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

**Remark 1.** The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**Remark 3.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00)

- (3) In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Symbol        | Conditions   | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |    |
|---|---------------|--|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|----|
|   |               |  | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |    |
| SCKp cycle time   | tkCY1         | tkCY1 ≥ 4/fCLK                                     | 2.7 V ≤ VDD ≤ 5.5 V             | 125  |                                | 166  |                                | 2000 |      | ns |
|   |               |  | 2.4 V ≤ VDD ≤ 5.5 V             | 250  |                                | 250  |                                | 2000 |      | ns |
|   |               |  | 1.8 V ≤ VDD ≤ 5.5 V             | 500  |                                | 500  |                                | 2000 |      | ns |
|   |               |  | 1.6 V ≤ VDD ≤ 5.5 V             | 1000 |                                | 1000 |                                | 2000 |      | ns |
| SCKp high-/low-level width                                  | tkH1,<br>tkL1 | 4.0 V ≤ VDD ≤ 5.5 V                                | tkCY1/2<br>- 12                 |      | tkCY1/2<br>- 21                |      | tkCY1/2<br>- 50                |      | ns   |    |
|   |               | 2.7 V ≤ VDD ≤ 5.5 V                                | tkCY1/2<br>- 18                 |      | tkCY1/2<br>- 25                |      | tkCY1/2<br>- 50                |      | ns   |    |
|   |               | 2.4 V ≤ VDD ≤ 5.5 V                                | tkCY1/2<br>- 38                 |      | tkCY1/2<br>- 38                |      | tkCY1/2<br>- 50                |      | ns   |    |
|   |               | 1.8 V ≤ VDD ≤ 5.5 V                                | tkCY1/2<br>- 50                 |      | tkCY1/2<br>- 50                |      | tkCY1/2<br>- 50                |      | ns   |    |
|   |               | 1.6 V ≤ VDD ≤ 5.5 V                                | tkCY1/2<br>- 100                |      | tkCY1/2<br>- 100               |      | tkCY1/2<br>- 100               |      | ns   |    |
| Slp setup time<br>(to SCKp↑) <sup>Note 1</sup>              | tSIK1         | 4.0 V ≤ VDD ≤ 5.5 V                                | 44                              |      | 54                             |      | 110                            |      | ns   |    |
|   |               | 2.7 V ≤ VDD ≤ 5.5 V                                | 44                              |      | 54                             |      | 110                            |      | ns   |    |
|   |               | 2.4 V ≤ VDD ≤ 5.5 V                                | 75                              |      | 75                             |      | 110                            |      | ns   |    |
|   |               | 1.8 V ≤ VDD ≤ 5.5 V                                | 110                             |      | 110                            |      | 110                            |      | ns   |    |
|   |               | 1.6 V ≤ VDD ≤ 5.5 V                                | 220                             |      | 220                            |      | 220                            |      | ns   |    |
| Slp hold time<br>(from SCKp↑)<br><sup>Note 1</sup>          | tkSI1         | 1.6 V ≤ VDD ≤ 5.5 V                                | 19                              |      | 19                             |      | 19                             |      | ns   |    |
| Delay time from<br>SCKp↓ to SOP<br>output <sup>Note 2</sup> | tkSO1         | 1.6 V ≤ VDD ≤ 5.5 V<br>C = 30 pF <sup>Note 3</sup> |                                 | 25   |                                | 25   |                                | 25   | ns   |    |

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SCKp and SOP output lines.

**Caution** Select the normal input buffer for the Slp pin and the normal output mode for the SOP pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

**Remark 1.** p: CSI number (p = 00, 01, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

**Remark 2.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 11)

(4) In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Item                           | Symbol        | Conditions          |                    | HS<br>(High-Speed Main)<br>Mode |                    | LS<br>(Low-Speed<br>Main)<br>Mode |                    | LP<br>(Low-Power Main)<br>Mode |                   | Unit |    |
|--------------------------------|---------------|---------------------|--------------------|---------------------------------|--------------------|-----------------------------------|--------------------|--------------------------------|-------------------|------|----|
|                                |               |                     |                    | Min.                            | Max.               | Min.                              | Max.               | Min.                           | Max.              |      |    |
| SCKp cycle time<br>Note 4      | tkCY2         | 4.0 V ≤ VDD ≤ 5.5 V | 20 MHz < fMCK      | 8/fMCK                          |                    | 8/fMCK                            |                    | —                              |                   | ns   |    |
|                                |               |                     | fMCK ≤ 20 MHz      | 6/fMCK                          |                    | 6/fMCK                            |                    | 6/fMCK                         |                   | ns   |    |
|                                |               | 2.7 V ≤ VDD ≤ 5.5 V | 16 MHz < fMCK      | 8/fMCK                          |                    | 8/fMCK                            |                    | —                              |                   | ns   |    |
|                                |               |                     | fMCK ≤ 16 MHz      | 6/fMCK                          |                    | 6/fMCK                            |                    | 6/fMCK                         |                   | ns   |    |
|                                |               | 2.4 V ≤ VDD ≤ 5.5 V |                    |                                 | 6/fMCK<br>and 500  |                                   | 6/fMCK<br>and 500  |                                | 6/fMCK<br>and 500 |      | ns |
|                                |               | 1.8 V ≤ VDD ≤ 5.5 V |                    |                                 | 6/fMCK<br>and 750  |                                   | 6/fMCK<br>and 750  |                                | 6/fMCK<br>and 750 |      | ns |
| 1.6 V ≤ VDD ≤ 5.5 V            |               |                     | 6/fMCK<br>and 1500 |                                 | 6/fMCK<br>and 1500 |                                   | 6/fMCK<br>and 1500 |                                | ns                |      |    |
| SCKp high-/<br>low-level width | tkH2,<br>tkL2 | 4.0 V ≤ VDD ≤ 5.5 V |                    | tkCY2/2 - 7                     |                    | tkCY2/2 - 7                       |                    | tkCY2/2 - 7                    |                   | ns   |    |
|                                |               | 2.7 V ≤ VDD ≤ 5.5 V |                    | tkCY2/2 - 8                     |                    | tkCY2/2 - 8                       |                    | tkCY2/2 - 8                    |                   | ns   |    |
|                                |               | 1.8 V ≤ VDD ≤ 5.5 V |                    | tkCY2/2<br>- 18                 |                    | tkCY2/2<br>- 18                   |                    | tkCY2/2<br>- 18                |                   | ns   |    |
|                                |               | 1.6 V ≤ VDD ≤ 5.5 V |                    | tkCY2/2<br>- 66                 |                    | tkCY2/2<br>- 66                   |                    | tkCY2/2<br>- 66                |                   | ns   |    |

(Notes, Caution, and Remarks are listed on the next page.)

- (4) In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Item  | Symbol | Conditions                     | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit            |    |
|---|--------|--------------------------------|---------------------------------|------|--------------------------------|------|--------------------------------|------|-----------------|----|
|   |        |                                | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |                 |    |
| Slp setup time<br>(to SCKp↑) <sup>Note 1</sup>              | tsIK2  | 2.7 V ≤ VDD ≤ 5.5 V            | 1/fMCK<br>+ 20                  |      | 1/fMCK<br>+ 30                 |      | 1/fMCK<br>+ 30                 |      | ns              |    |
|   |        | 1.8 V ≤ VDD ≤ 5.5 V            | 1/fMCK<br>+ 30                  |      | 1/fMCK<br>+ 30                 |      | 1/fMCK<br>+ 30                 |      | ns              |    |
|   |        | 1.6 V ≤ VDD ≤ 5.5 V            | 1/fMCK<br>+ 40                  |      | 1/fMCK<br>+ 40                 |      | 1/fMCK<br>+ 40                 |      | ns              |    |
| Slp hold time<br>(from SCKp↑) <sup>Note 1</sup>             | tkSI2  | 1.8 V ≤ VDD ≤ 5.5 V            | 1/fMCK<br>+ 31                  |      | 1/fMCK<br>+ 31                 |      | 1/fMCK<br>+ 31                 |      | ns              |    |
|   |        | 1.6 V ≤ VDD ≤ 5.5 V            | 1/fMCK<br>+ 250                 |      | 1/fMCK<br>+ 250                |      | 1/fMCK<br>+ 250                |      | ns              |    |
| Delay time from<br>SCKp↓ to SOp output<br><sup>Note 2</sup> | tkSO2  | C = 30 pF<br><sup>Note 3</sup> | 2.7 V ≤ VDD ≤ 5.5 V             |      | 2/fMCK<br>+ 44                 |      | 2/fMCK<br>+ 110                |      | 2/fMCK<br>+ 110 | ns |
|   |        |                                | 2.4 V ≤ VDD ≤ 5.5 V             |      | 2/fMCK<br>+ 75                 |      | 2/fMCK<br>+ 110                |      | 2/fMCK<br>+ 110 | ns |
|   |        |                                | 1.8 V ≤ VDD ≤ 5.5 V             |      | 2/fMCK<br>+ 110                |      | 2/fMCK<br>+ 110                |      | 2/fMCK<br>+ 110 | ns |
|   |        |                                | 1.6 V ≤ VDD ≤ 5.5 V             |      | 2/fMCK<br>+ 220                |      | 2/fMCK<br>+ 220                |      | 2/fMCK<br>+ 220 | ns |

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 3.** C is the load capacitance of the SOp output line.

**Note 4.** Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

**Caution** Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

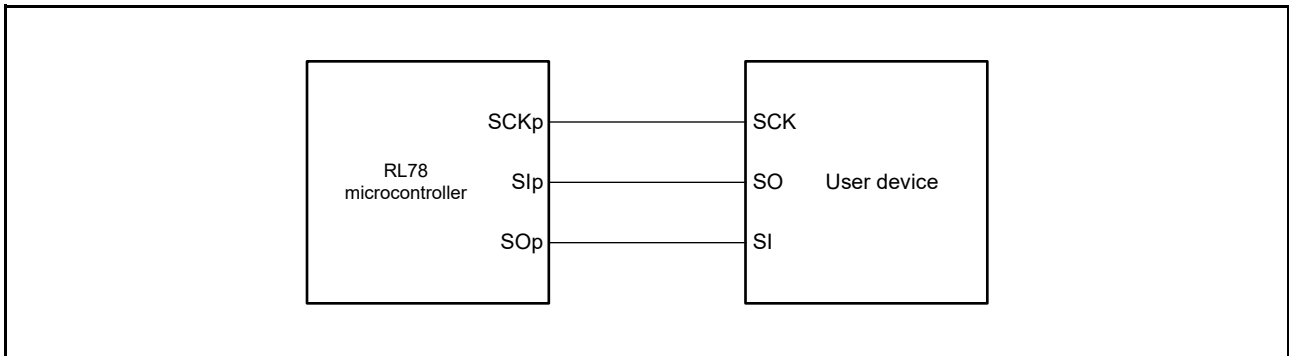
**Remark 1.** p: CSI number (p = 00, 01, 11, 20, 21), m: Unit number (m = 0, 1), n: Channel number (n = 0, 1, 3), g: PIM and POM numbers (g = 0, 1, 5, 7)

**Remark 2.** fMCK: Serial array unit operation clock frequency

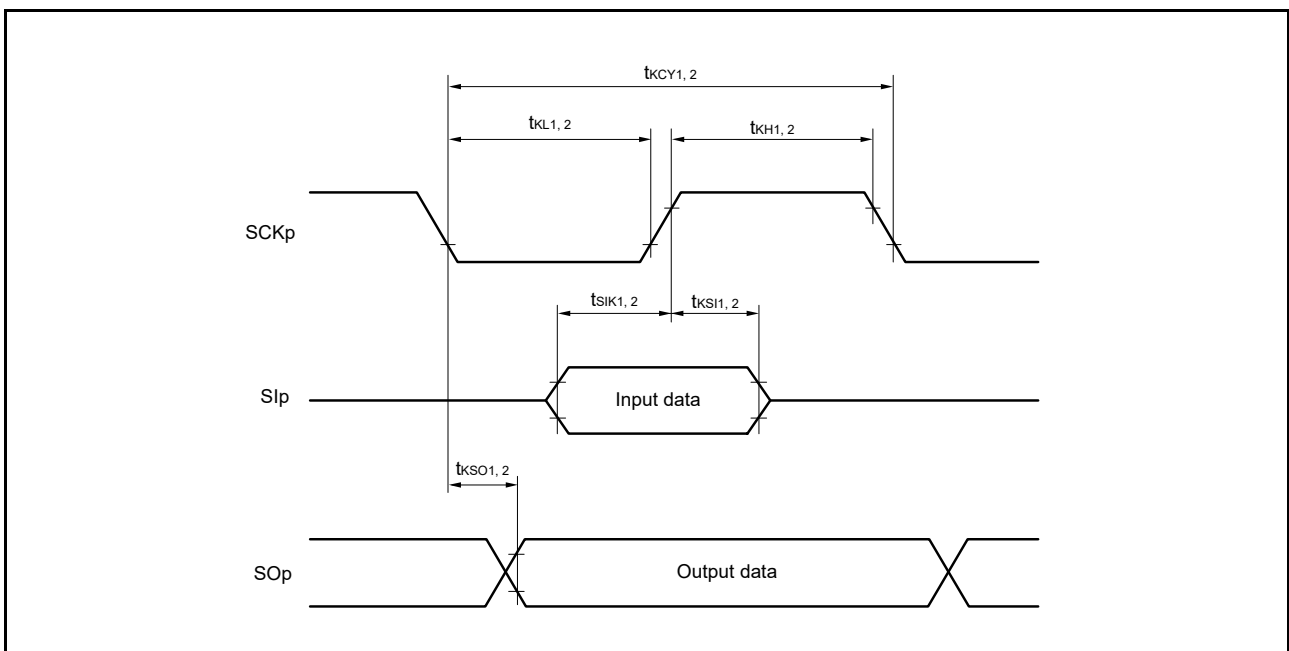
To set this operating clock, use the CKS<sub>mn</sub> bit in the serial mode register mn (SMR<sub>mn</sub>).

m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

(a) Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels

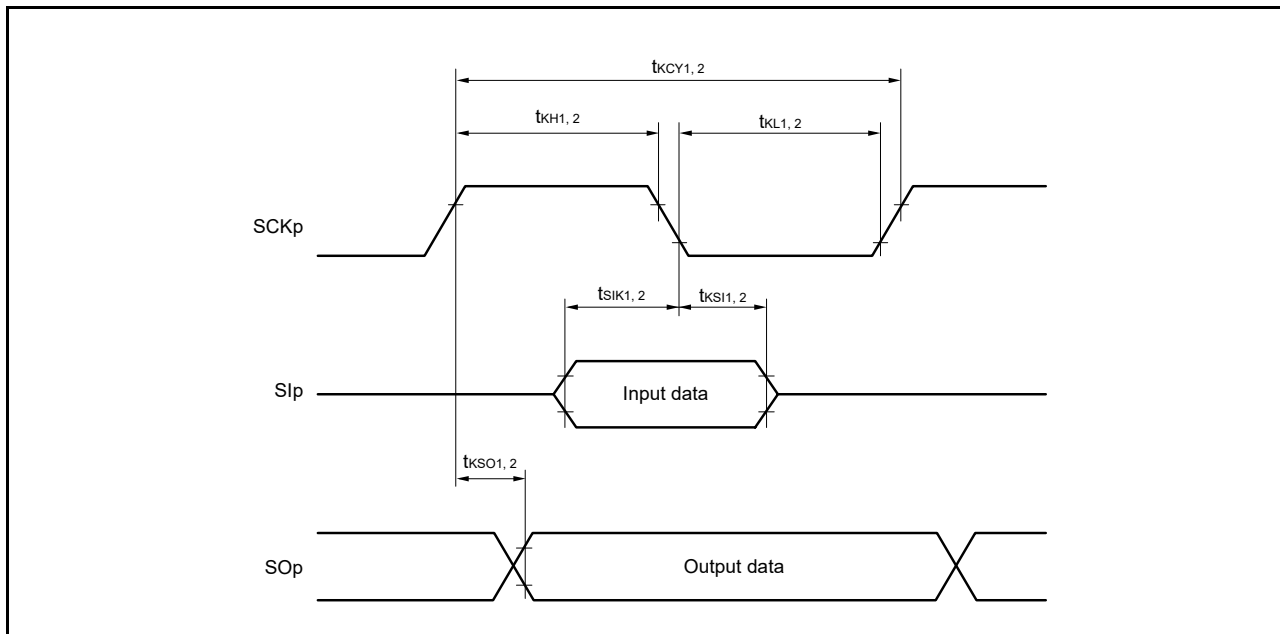


(b) Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1





(c) Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



**Remark 1.** p: CSI number (p = 00, 01, 11, 20, 21)

**Remark 2.** m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

(5) In simplified I<sup>2</sup>C communications with devices operating at same voltage levels(TA = -40 to +105°C, 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(1/2)

| Item                           | Symbol            | Conditions  | HS<br>(High-Speed Main)<br>Mode |                | LS<br>(Low-Speed Main)<br>Mode |                | LP<br>(Low-Power Main)<br>Mode |               | Unit |
|--------------------------------|-------------------|---|---------------------------------|----------------|--------------------------------|----------------|--------------------------------|---------------|------|
|                                |                   |   | Min.                            | Max.           | Min.                           | Max.           | Min.                           | Max.          |      |
| SCLr clock frequency           | f <sub>SCL</sub>  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ |                                 | 1000<br>Note 1 |                                | 1000<br>Note 1 |                                | 400<br>Note 1 | kHz  |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  |                                 | 400<br>Note 1  |                                | 400<br>Note 1  |                                | 400<br>Note 1 | kHz  |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  |                                 | 300<br>Note 1  |                                | 300<br>Note 1  |                                | 300<br>Note 1 | kHz  |
|                                |                   | 1.6 V ≤ V <sub>DD</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  |                                 | 250<br>Note 1  |                                | 250<br>Note 1  |                                | 250<br>Note 1 | kHz  |
| Hold time when SCLr<br>is low  | t <sub>LOW</sub>  | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 475                             |                | 475                            |                | 1150                           |               | ns   |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1150                            |                | 1150                           |                | 1150                           |               | ns   |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1550                            |                | 1550                           |                | 1550                           |               | ns   |
|                                |                   | 1.6 V ≤ V <sub>DD</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1850                            |                | 1850                           |                | 1850                           |               | ns   |
| Hold time when SCLr<br>is high | t <sub>HIGH</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 475                             |                | 475                            |                | 1150                           |               | ns   |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1150                            |                | 1150                           |                | 1150                           |               | ns   |
|                                |                   | 1.8 V ≤ V <sub>DD</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1550                            |                | 1550                           |                | 1550                           |               | ns   |
|                                |                   | 1.6 V ≤ V <sub>DD</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1850                            |                | 1850                           |                | 1850                           |               | ns   |

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)

(5) In simplified I<sup>2</sup>C communications with devices operating at same voltage levels

(T<sub>A</sub> = -40 to +105°C, 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(2/2)

| Item                             | Symbol              | Conditions  | HS<br>(High-Speed Main)<br>Mode              |      | LS<br>(Low-Speed Main)<br>Mode               |      | LP<br>(Low-Power Main)<br>Mode               |      | Unit |
|----------------------------------|---------------------|---|--|------|--|------|--|------|------|
|                                  |                     |   | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| Data setup time<br>(reception)   | t <sub>SU:DAT</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 1/f <sub>MCK</sub><br>+ 85<br><b>Note 2</b>  |      | 1/f <sub>MCK</sub><br>+ 85<br><b>Note 2</b>  |      | 1/f <sub>MCK</sub><br>+ 145<br><b>Note 2</b> |      | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 1/f <sub>MCK</sub><br>+ 145<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 145<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 145<br><b>Note 2</b> |      | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1/f <sub>MCK</sub><br>+ 230<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 230<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 230<br><b>Note 2</b> |      | ns   |
|                                  |                     | 1.6 V ≤ V <sub>DD</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 1/f <sub>MCK</sub><br>+ 290<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 290<br><b>Note 2</b> |      | 1/f <sub>MCK</sub><br>+ 290<br><b>Note 2</b> |      | ns   |
| Data hold time<br>(transmission) | t <sub>HD:DAT</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ | 0  | 305  | 0  | 305  | 0  | 305  | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 3 kΩ  | 0  | 355  | 0  | 355  | 0  | 355  | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> < 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 0  | 405  | 0  | 405  | 0  | 405  | ns   |
|                                  |                     | 1.6 V ≤ V <sub>DD</sub> < 1.8 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5 kΩ  | 0  | 405  | 0  | 405  | 0  | 405  | ns   |

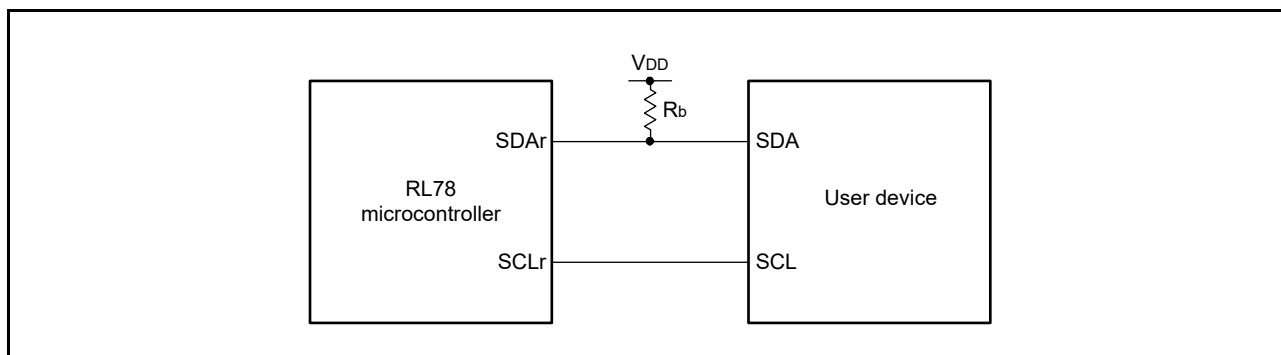
**Note 1.** The listed times must be no greater than f<sub>MCK</sub>/4.

**Note 2.** Set f<sub>MCK</sub> so that it will not exceed the hold time when SCLr is low or high.

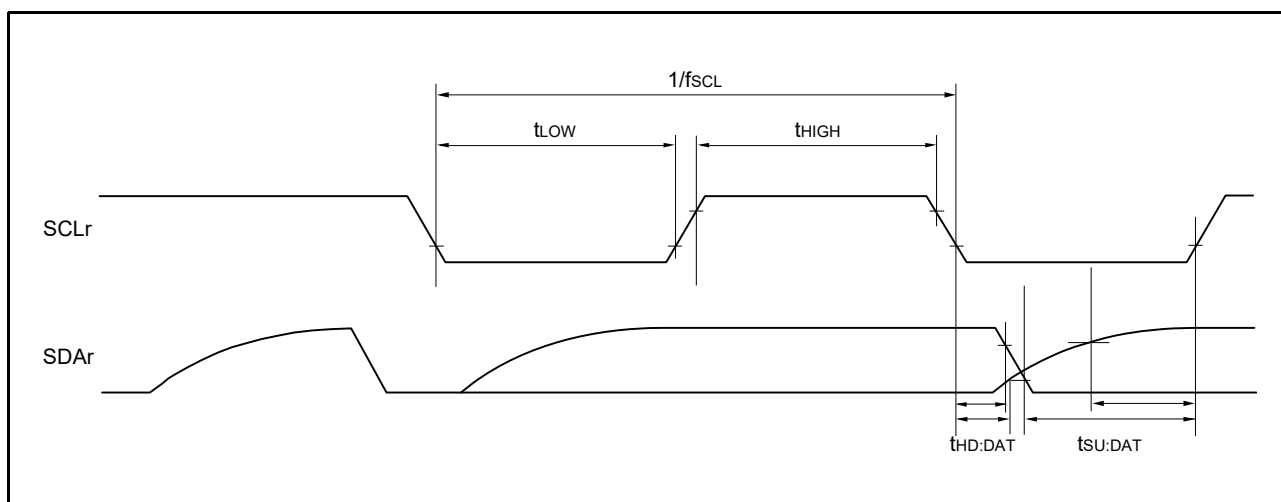
**Caution** Select the normal input buffer and the N-ch open drain output [withstand voltage of V<sub>DD</sub>] mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

(a) Connection in the simplified I<sup>2</sup>C communications with devices operating at same voltage levels



(b) Timing of serial transfer in the simplified I<sup>2</sup>C communications with devices operating at same voltage levels



**Remark 1.** R<sub>b</sub>[Ω]: Communication line (SDAr) pull-up resistance, C<sub>b</sub>[F]: Communication line (SDAr, SCLr) load capacitance

**Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21), g: PIM number (g = 0, 1, 3, 7), h: POM number (g = 1, 5, 7)

**Remark 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

(6) In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Item          | Symbol | Conditions | HS<br>(High-Speed Main)<br>Mode   |   | LS<br>(Low-Speed Main)<br>Mode |                      | LP<br>(Low-Power Main)<br>Mode |                      | Unit             |                      |      |
|---------------|--------|------------|---|---|--------------------------------|----------------------|--------------------------------|----------------------|------------------|----------------------|------|
|               |        |            | Min.  | Max.  | Min.                           | Max.                 | Min.                           | Max.                 |                  |                      |      |
| Transfer rate |        | Reception  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V                                      |   | fMCK/6<br>Note 1               |                      | fMCK/6<br>Note 1               |                      | fMCK/6<br>Note 1 | bps                  |      |
|               |        |            | Theoretical value of the maximum transfer rate<br>fMCK = fCLK <sup>Note 3</sup> |   | 5.3                            |                      | 4                              |                      | 0.33             | Mbps                 |      |
|               |        |            | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V                                      |   | fMCK/6<br>Note 1               |                      | fMCK/6<br>Note 1               |                      | fMCK/6<br>Note 1 | bps                  |      |
|               |        |            |   | Theoretical value of the maximum transfer rate<br>fMCK = fCLK <sup>Note 3</sup> |                                | 5.3                  |                                | 4                    |                  | 0.33                 | Mbps |
|               |        |            |   | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V                                      |                                | fMCK/6<br>Notes 1, 2 |                                | fMCK/6<br>Notes 1, 2 |                  | fMCK/6<br>Notes 1, 2 | bps  |
|               |        |            |   | Theoretical value of the maximum transfer rate<br>fMCK = fCLK <sup>Note 3</sup> |                                | 5.3                  |                                | 4                    |                  | 0.33                 | Mbps |

**Note 1.** Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

**Note 2.** Use this rate with VDD ≥ Vb.

**Note 3.** The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:  
 HS (high-speed main) mode: 32 MHz (1.8 V ≤ VDD ≤ 5.5 V)  
 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)  
 LS (low-speed main) mode: 24 MHz (1.8 V ≤ VDD ≤ 5.5 V)  
 4 MHz (1.6 V ≤ VDD ≤ 5.5 V)  
 LP (low-power main) mode: 2 MHz (1.6 V ≤ VDD ≤ 5.5 V)

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output [withstand voltage of VDD] mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Vb[V]: Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**Remark 3.** fMCK: Serial array unit operation clock frequency  
 To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00, 01)

**Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

(6) In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Item          | Symbol | Conditions   | HS<br>(High-Speed Main)<br>Mode   |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit           |      |
|---------------|--------|--------------|---|------|--------------------------------|------|--------------------------------|------|----------------|------|
|               |        |              | Min.  | Max. | Min.                           | Max. | Min.                           | Max. |                |      |
| Transfer rate |        | Transmission | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V  |      | Note 1                         |      | Note 1                         |      | Note 1         | bps  |
|               |        |              | Theoretical value of the maximum transfer rate<br>Cb = 50 pF,<br>Rb = 1.4 kΩ,<br>Vb = 2.7 V |      | 2.8Note 2                      |      | 2.8Note 2                      |      | 2.8Note 2      | Mbps |
|               |        |              | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V  |      | Note 3                         |      | Note 3                         |      | Note 3         | bps  |
|               |        |              | Theoretical value of the maximum transfer rate<br>Cb = 50 pF,<br>Rb = 2.7 kΩ,<br>Vb = 2.3 V |      | 1.2Note 4                      |      | 1.2Note 4                      |      | 1.2Note 4      | Mbps |
|               |        |              | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V  |      | Notes 5, 6                     |      | Notes 5, 6                     |      | Notes 5, 6     | bps  |
|               |        |              | Theoretical value of the maximum transfer rate<br>Cb = 50 pF,<br>Rb = 5.5 kΩ,<br>Vb = 1.6 V |      | 0.43<br>Note 7                 |      | 0.43<br>Note 7                 |      | 0.43<br>Note 7 | Mbps |

**Note 1.** The smaller maximum transfer rate derived by using fmCK/6 or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when 4.0 V ≤ VDD ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 2.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes 3 to 7 and Caution are listed on the next page.)

**Note 3.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $2.7\text{ V} \leq V_{DD} < 4.0\text{ V}$ ,  $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

**Note 4.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

**Note 5.** Use this rate with  $V_{DD} \geq V_b$ .

**Note 6.** The smaller maximum transfer rate derived by using  $f_{MCK}/6$  or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when  $1.8\text{ V} \leq V_{DD} < 3.3\text{ V}$ ,  $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

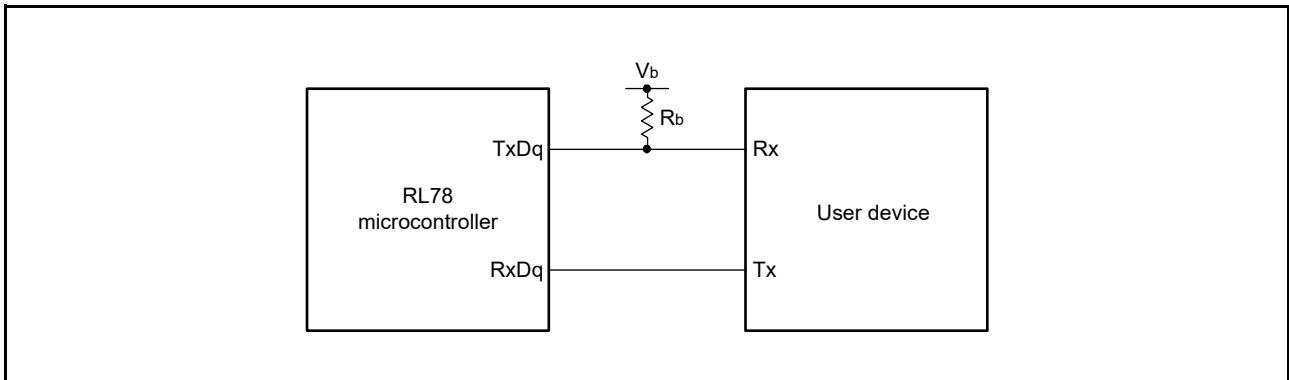
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{\left(\frac{1}{\text{Transfer rate}}\right) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

This value is the theoretical value of the relative difference between the transmission and reception sides.

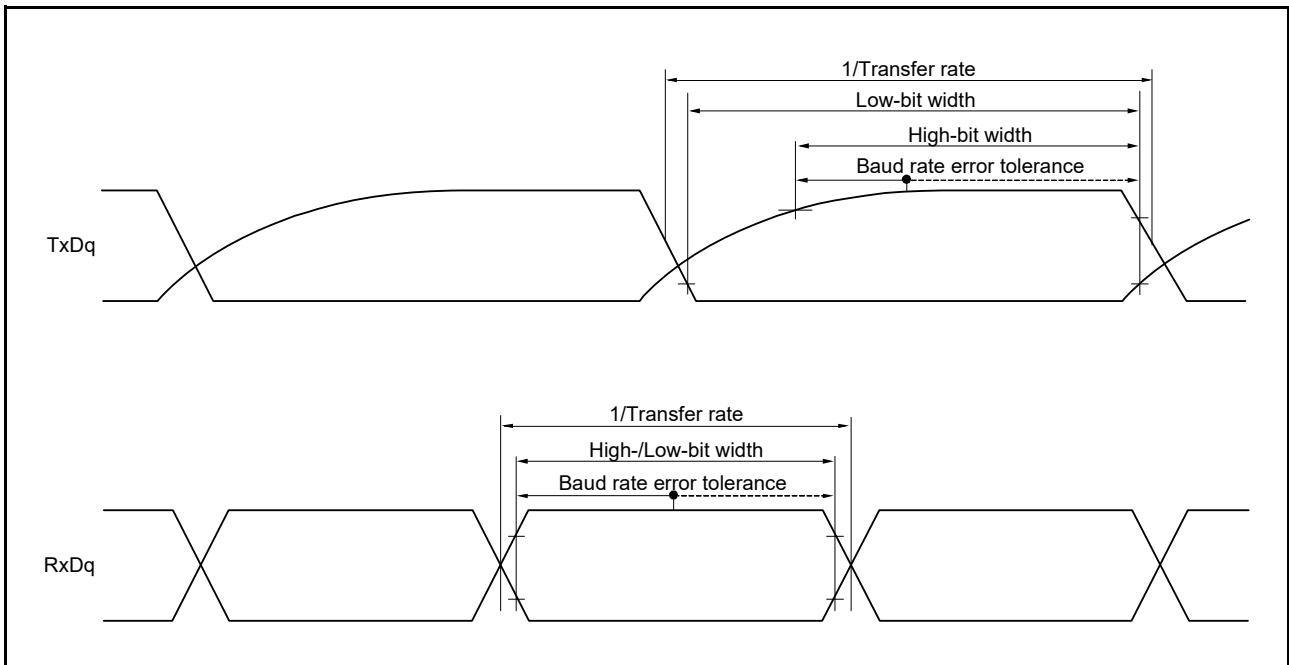
**Note 7.** This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

**Caution** Select the TTL input buffer for the RxDq pin and the N-ch open drain output [withstand voltage of  $V_{DD}$ ] mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For  $V_{IH}$  and  $V_{IL}$ , see the DC characteristics with TTL input buffer selected.

(a) In UART communications with devices operating at different voltage levels



(b) Bit width in the UART communications with devices operating at different voltage levels (reference)



**Remark 1.**  $R_b[\Omega]$ : Communication line (TxDq) pull-up resistance,  $C_b[F]$ : Communication line (TxDq) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** q: UART number (q = 0 to 2), g: PIM and POM number (g = 0, 1)

**Remark 3.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01)

**Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.



(7) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Item  | Symbol | Conditions  | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed<br>Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|---|--------|---|---------------------------------|------|-----------------------------------|------|--------------------------------|------|------|
|   |        |   | Min.                            | Max. | Min.                              | Max. | Min.                           | Max. |      |
| SCKp cycle time                                 | tkCY1  | tkCY1 ≥ 2/fCLK<br>4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF,<br>Rb = 1.4 kΩ | 200                             |      | 200                               |      | 2300                           |      | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF,<br>Rb = 2.7 kΩ                   | 300                             |      | 300                               |      | 2300                           |      | ns   |
| SCKp high-level width                           | tkH1   | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ                      | tkCY1/2<br>- 50                 |      | tkCY1/2<br>- 50                   |      | tkCY1/2<br>- 50                |      | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ                      | tkCY1/2<br>- 120                |      | tkCY1/2<br>- 120                  |      | tkCY1/2<br>- 120               |      | ns   |
| SCKp low-level width                            | tkL1   | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ                      | tkCY1/2<br>- 7                  |      | tkCY1/2<br>- 7                    |      | tkCY1/2<br>- 50                |      | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ                      | tkCY1/2<br>- 10                 |      | tkCY1/2<br>- 10                   |      | tkCY1/2<br>- 50                |      | ns   |
| Slp setup time<br>(to SCKp↑)Note 1              | tsIK1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ                      | 58                              |      | 58                                |      | 479                            |      | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ                      | 121                             |      | 121                               |      | 479                            |      | ns   |
| Slp hold time<br>(from SCKp↑)Note 1             | tkSI1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ                      | 10                              |      | 10                                |      | 10                             |      | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ                      | 10                              |      | 10                                |      | 10                             |      | ns   |
| Delay time from<br>SCKp↓ to SOp<br>outputNote 1 | tkSO1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ                      |                                 | 60   |                                   | 60   |                                | 60   | ns   |
|   |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ                      |                                 | 130  |                                   | 130  |                                | 130  | ns   |

(Notes, Caution, and Remarks are listed on the next page.)

- (7) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

(TA = -40 to +105°C, 2.7 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Item   | Symbol | Conditions   | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|--|--------|--|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|  |        |  | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |
| Slp setup time<br>(to SCKp↓) <sup>Note 2</sup>           | tsIK1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ | 23                              |      | 23                             |      | 110                            |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ | 33                              |      | 33                             |      | 110                            |      | ns   |
| Slp hold time<br>(from SCKp↓) <sup>Note 2</sup>          | tkSI1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ | 10                              |      | 10                             |      | 10                             |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ | 10                              |      | 10                             |      | 10                             |      | ns   |
| Delay time from SCKp↑<br>to SOp output <sup>Note 2</sup> | tkSO1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 20 pF, Rb = 1.4 kΩ |                                 | 10   |                                | 10   |                                | 10   | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 20 pF, Rb = 2.7 kΩ |                                 | 10   |                                | 10   |                                | 10   | ns   |

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output [withstand voltage of VDD] mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

**Remark 1.** Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

**Remark 2.** p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

**Remark 3.** fMCK: Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn= 00)

**Remark 4.** The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

- (8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/3)

| Item                  | Symbol | Conditions  | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|-----------------------|--------|---|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|                       |        |   | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |
| SCKp cycle time       | tkCY1  | tkCY1 ≥ 4/fCLK<br>4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF,<br>Rb = 1.4 kΩ | 300                             |      | 300                            |      | 2300                           |      | ns   |
|                       |        |   | 500                             |      | 500                            |      | 2300                           |      | ns   |
|                       |        |   | 1150                            |      | 1150                           |      | 2300                           |      | ns   |
| SCKp high-level width | tkH1   | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                      | tkCY1/2<br>- 75                 |      | tkCY1/2<br>- 75                |      | tkCY1/2<br>- 75                |      | ns   |
|                       |        |   | tkCY1/2<br>- 170                |      | tkCY1/2<br>- 170               |      | tkCY1/2<br>- 170               |      | ns   |
|                       |        |   | tkCY1/2<br>- 458                |      | tkCY1/2<br>- 458               |      | tkCY1/2<br>- 458               |      | ns   |
| SCKp low-level width  | tkL1   | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                      | tkCY1/2<br>- 12                 |      | tkCY1/2<br>- 12                |      | tkCY1/2<br>- 50                |      | ns   |
|                       |        |   | tkCY1/2<br>- 18                 |      | tkCY1/2<br>- 18                |      | tkCY1/2<br>- 50                |      | ns   |
|                       |        |   | tkCY1/2<br>- 50                 |      | tkCY1/2<br>- 50                |      | tkCY1/2<br>- 50                |      | ns   |

**Note** Use this setting with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the SIp pin and the N-ch open drain output [withstand voltage of VDD] mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed two pages after the next page.)

- (8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/3)

| Item   | Symbol | Conditions  | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|--|--------|---|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|  |        |   | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |
| Slp setup time<br>(to SCKp↑) <sup>Note 1</sup>           | tsIK1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    | 81                              |      | 81                             |      | 479                            |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    | 177                             |      | 177                            |      | 479                            |      | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ | 479                             |      | 479                            |      | 479                            |      | ns   |
| Slp hold time<br>(from SCKp↑) <sup>Note 1</sup>          | tKSI1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    | 19                              |      | 19                             |      | 19                             |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    | 19                              |      | 19                             |      | 19                             |      | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ | 19                              |      | 19                             |      | 19                             |      | ns   |
| Delay time from SCKp↓<br>to SOp output <sup>Note 1</sup> | tKSO1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    |                                 | 100  |                                | 100  |                                | 100  | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    |                                 | 195  |                                | 195  |                                | 195  | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ |                                 | 483  |                                | 483  |                                | 483  | ns   |

**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

**Note 2.** Use this setting with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output [withstand voltage of VDD] mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the page after the next page.)

- (8) In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(3/3)

| Item   | Symbol | Conditions  | HS<br>(High-Speed Main)<br>Mode |      | LS<br>(Low-Speed Main)<br>Mode |      | LP<br>(Low-Power Main)<br>Mode |      | Unit |
|--|--------|---|---------------------------------|------|--------------------------------|------|--------------------------------|------|------|
|  |        |   | Min.                            | Max. | Min.                           | Max. | Min.                           | Max. |      |
| Slp setup time<br>(to SCKp↓) <sup>Note 1</sup>           | tsIK1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    | 44                              |      | 44                             |      | 110                            |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    | 44                              |      | 44                             |      | 110                            |      | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ | 110                             |      | 110                            |      | 110                            |      | ns   |
| Slp hold time<br>(from SCKp↓) <sup>Note 1</sup>          | tkSI1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    | 19                              |      | 19                             |      | 19                             |      | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    | 19                              |      | 19                             |      | 19                             |      | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ | 19                              |      | 19                             |      | 19                             |      | ns   |
| Delay time from SCKp↑<br>to SOp output <sup>Note 1</sup> | tkSO1  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    |                                 | 25   |                                | 25   |                                | 25   | ns   |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    |                                 | 25   |                                | 25   |                                | 25   | ns   |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ |                                 | 25   |                                | 25   |                                | 25   | ns   |

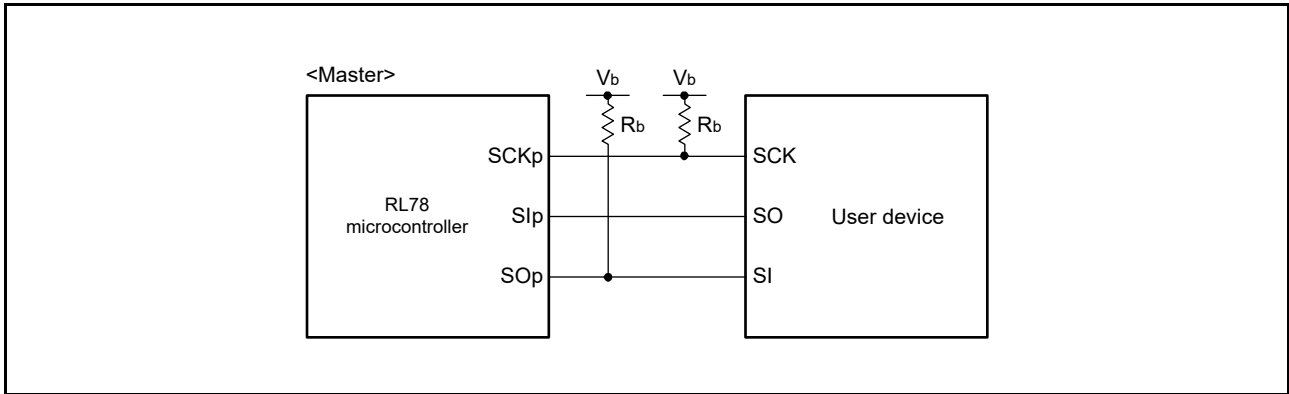
**Note 1.** This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 2.** Use this setting with VDD ≥ Vb.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output [withstand voltage of VDD] mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(a) Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



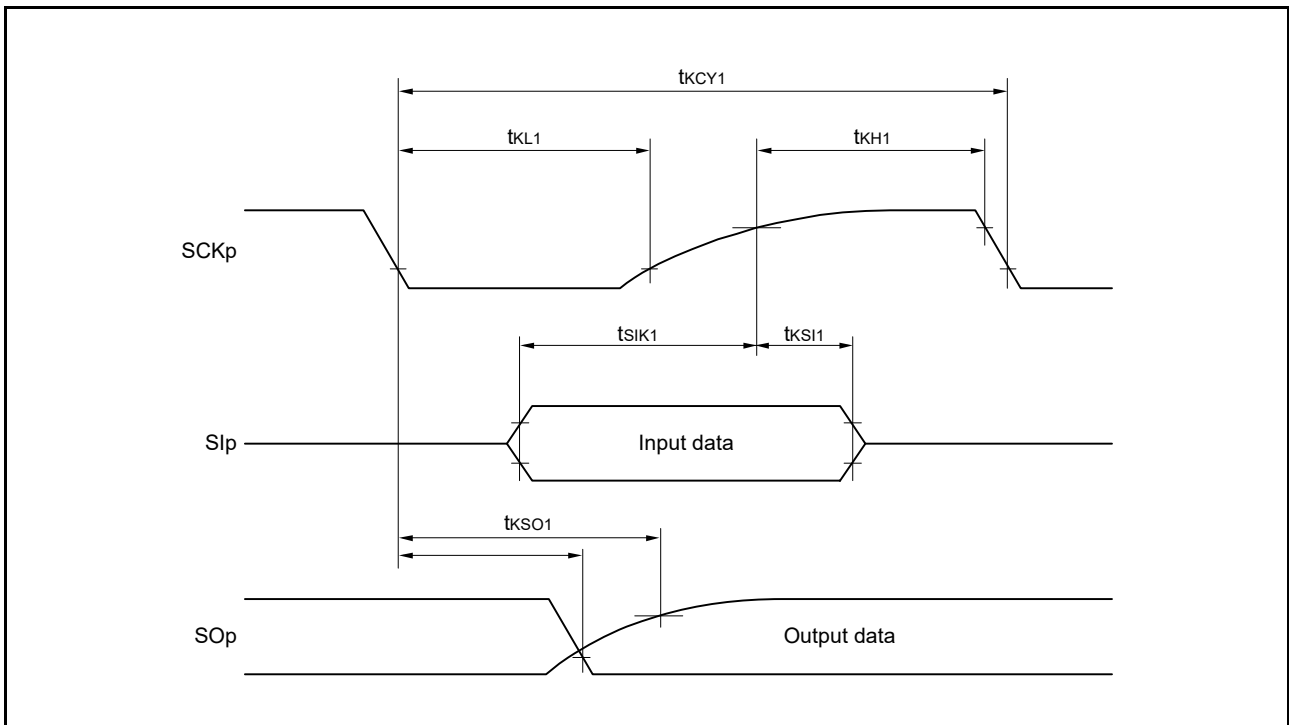
**Remark 1.**  $R_b[\Omega]$ : Communication line (SCKp, SOp) pull-up resistance,  $C_b[F]$ : Communication line (SCKp, SOp) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

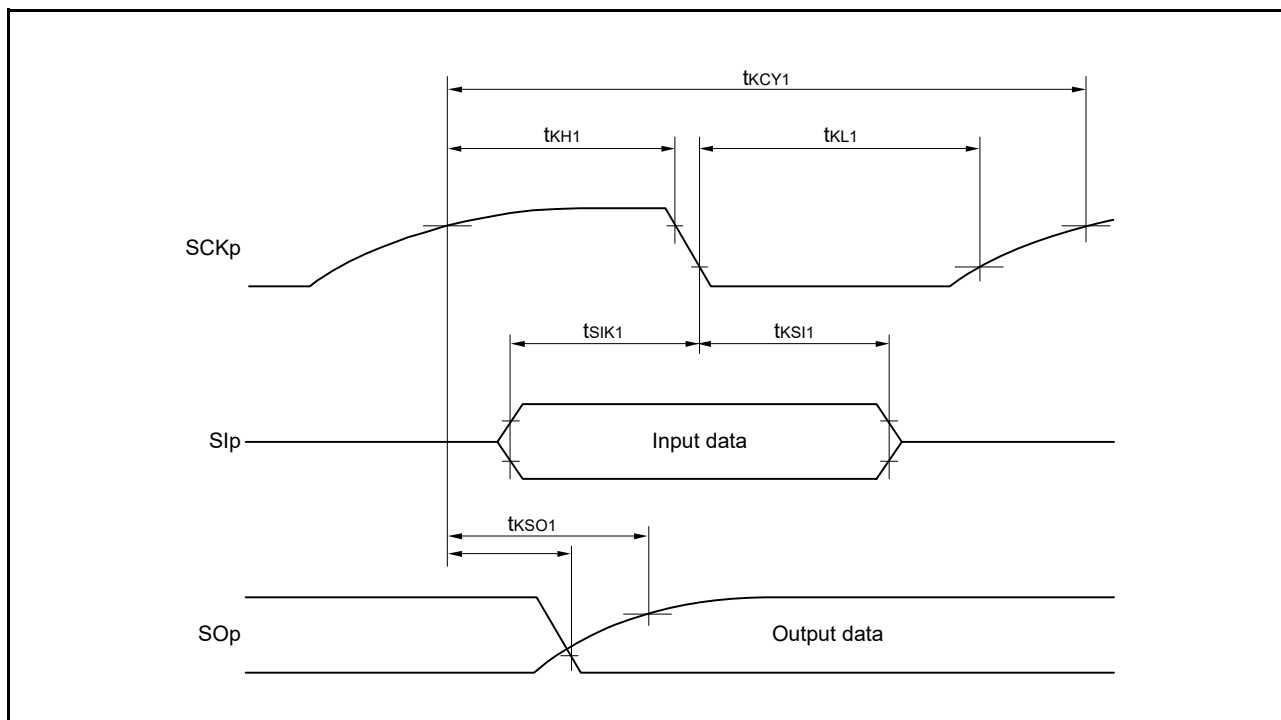
**Remark 3.**  $f_{MCK}$ : Serial array unit operation clock frequency  
 To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00)

**Remark 4.** Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(b) Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when  $DAP_{mn} = 0$  and  $CKP_{mn} = 0$ , or  $DAP_{mn} = 1$  and  $CKP_{mn} = 1$



(c) Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



**Remark 1.** p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

**Remark 2.** Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(9) In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(1/2)

| Item                                   | Symbol | Conditions  |                        | HS<br>(High-Speed Main)<br>Mode |         | LS<br>(Low-Speed Main)<br>Mode |         | LP<br>(Low-Power Main)<br>Mode |         | Unit |    |
|--|--------|---|------------------------|---------------------------------|---------|--------------------------------|---------|--------------------------------|---------|------|----|
|  |        |   |                        | Min.                            | Max.    | Min.                           | Max.    | Min.                           | Max.    |      |    |
| SCKp<br>cycle<br>time<br><b>Note 1</b> | tkCY2  | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V                  | 24 MHz < fMCK          | 14/fMCK                         |         | —                              |         | —                              |         | ns   |    |
|  |        |   | 20 MHz < fMCK ≤ 24 MHz | 12/fMCK                         |         | 12/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 8 MHz < fMCK ≤ 20 MHz  | 10/fMCK                         |         | 10/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 4 MHz < fMCK ≤ 8 MHz   | 8/fMCK                          |         | 8/fMCK                         |         | —                              |         | ns   |    |
|  |        |   | fMCK ≤ 4 MHz           | 6/fMCK                          |         | 6/fMCK                         |         | 10/fMCK                        |         | ns   |    |
|  |        | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,                 | 24 MHz < fMCK          | 20/fMCK                         |         | —                              |         | —                              |         | ns   |    |
|  |        |   | 20 MHz < fMCK ≤ 24 MHz | 16/fMCK                         |         | 16/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 16 MHz < fMCK ≤ 20 MHz | 14/fMCK                         |         | 14/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 8 MHz < fMCK ≤ 16 MHz  | 12/fMCK                         |         | 12/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 4 MHz < fMCK ≤ 8 MHz   | 8/fMCK                          |         | 8/fMCK                         |         | —                              |         | ns   |    |
|  |        | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V<br><b>Note 2</b> | 24 MHz < fMCK          | 48/fMCK                         |         | —                              |         | —                              |         | ns   |    |
|  |        |   | 20 MHz < fMCK ≤ 24 MHz | 36/fMCK                         |         | 36/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 16 MHz < fMCK ≤ 20 MHz | 32/fMCK                         |         | 32/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 8 MHz < fMCK ≤ 16 MHz  | 26/fMCK                         |         | 26/fMCK                        |         | —                              |         | ns   |    |
|  |        |   | 4 MHz < fMCK ≤ 8 MHz   | 16/fMCK                         |         | 16/fMCK                        |         | —                              |         | ns   |    |
|  |        |   |                        | fMCK ≤ 4 MHz                    | 10/fMCK |                                | 10/fMCK |                                | 10/fMCK |      | ns |

(Notes and Caution are listed on the next page, and Remarks are listed on the page after the next page.)



- (9) In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

(2/2)

| Item   | Symbol        | Conditions  | HS<br>(High-Speed Main)<br>Mode |                 | LS<br>(Low-Speed Main)<br>Mode |                 | LP<br>(Low-Power Main)<br>Mode |                 | Unit |
|--|---------------|---|---------------------------------|-----------------|--------------------------------|-----------------|--------------------------------|-----------------|------|
|  |               |   | Min.                            | Max.            | Min.                           | Max.            | Min.                           | Max.            |      |
| SCKp high-/low-level width                               | tkH2,<br>tkL2 | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V  | tkCY2/2<br>- 12                 |                 | tkCY2/2<br>- 12                |                 | tkCY2/2<br>- 50                |                 | ns   |
|  |               | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V  | tkCY2/2<br>- 18                 |                 | tkCY2/2<br>- 18                |                 | tkCY2/2<br>- 50                |                 | ns   |
|  |               | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>                              | tkCY2/2<br>- 50                 |                 | tkCY2/2<br>- 50                |                 | tkCY2/2<br>- 50                |                 | ns   |
| Slp setup time<br>(to SCKp↑) <sup>Note 3</sup>           | tsIK2         | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V  | 1/fMCK<br>+ 20                  |                 | 1/fMCK<br>+ 20                 |                 | 1/fMCK<br>+ 30                 |                 | ns   |
|  |               | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V  | 1/fMCK<br>+ 20                  |                 | 1/fMCK<br>+ 20                 |                 | 1/fMCK<br>+ 30                 |                 | ns   |
|  |               | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup>                              | 1/fMCK<br>+ 30                  |                 | 1/fMCK<br>+ 30                 |                 | 1/fMCK<br>+ 30                 |                 | ns   |
| Slp hold time<br>(from SCKp↑) <sup>Note 3</sup>          | tkSI2         |   | 1/fMCK<br>+ 31                  |                 | 1/fMCK<br>+ 31                 |                 | 1/fMCK<br>+ 31                 |                 | ns   |
| Delay time from SCKp↓<br>to SOp output <sup>Note 4</sup> | tkSO2         | 4.0 V ≤ VDD ≤ 5.5 V,<br>2.7 V ≤ Vb ≤ 4.0 V,<br>Cb = 30 pF, Rb = 1.4 kΩ                    |                                 | 2/fMCK<br>+ 120 |                                | 2/fMCK<br>+ 120 |                                | 2/fMCK<br>+ 573 | ns   |
|  |               | 2.7 V ≤ VDD < 4.0 V,<br>2.3 V ≤ Vb ≤ 2.7 V,<br>Cb = 30 pF, Rb = 2.7 kΩ                    |                                 | 2/fMCK<br>+ 214 |                                | 2/fMCK<br>+ 214 |                                | 2/fMCK<br>+ 573 | ns   |
|  |               | 1.8 V ≤ VDD < 3.3 V,<br>1.6 V ≤ Vb ≤ 2.0 V <sup>Note 2</sup> ,<br>Cb = 30 pF, Rb = 5.5 kΩ |                                 | 2/fMCK<br>+ 573 |                                | 2/fMCK<br>+ 573 |                                | 2/fMCK<br>+ 573 | ns   |

**Note 1.** Transfer rate in the SNOOZE mode: 1 Mbps (max.)

**Note 2.** Use this setting with VDD ≥ Vb.

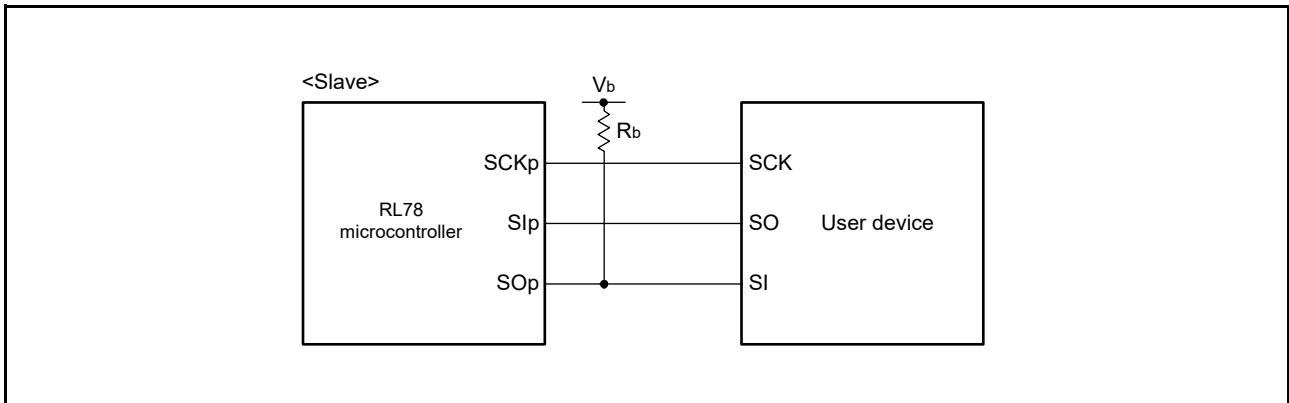
**Note 3.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The Slp setup time becomes “to SCKp↓” and Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Note 4.** This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The delay time to SOp output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

**Caution** Select the TTL input buffer for the Slp pin and the N-ch open drain output [withstand voltage of VDD] mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(a) Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels



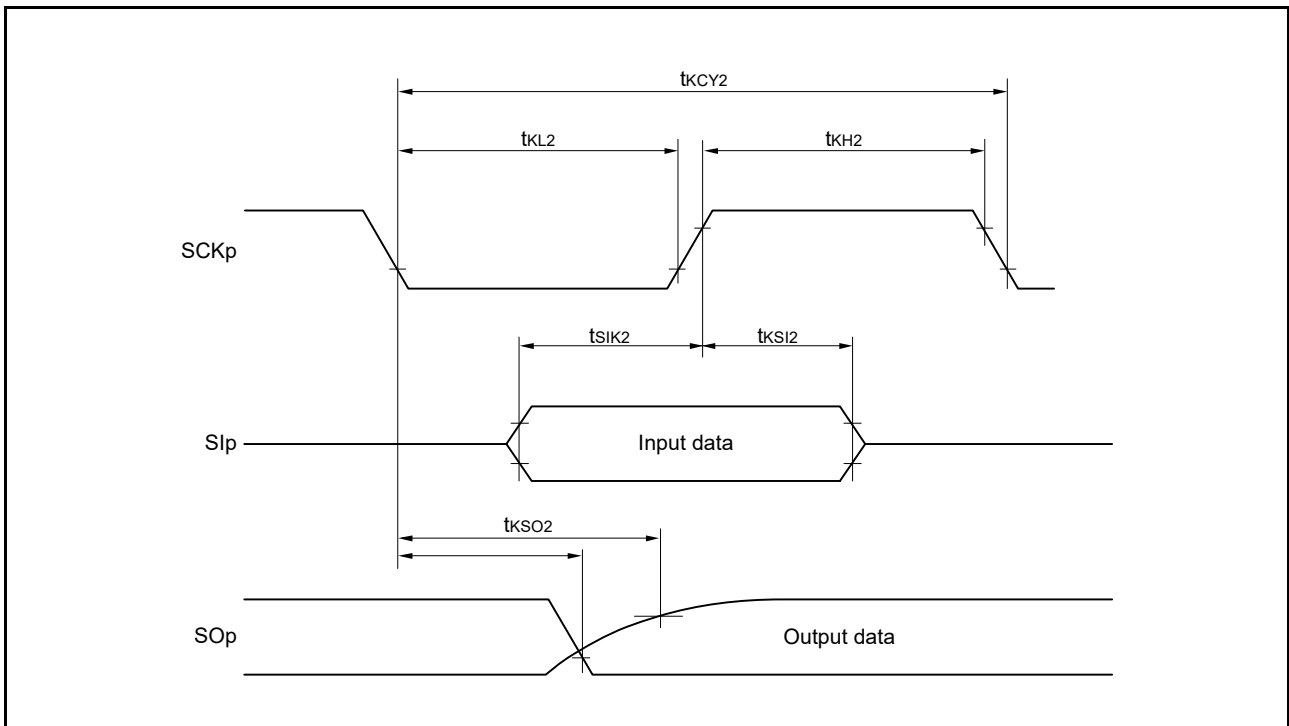
**Remark 1.**  $R_b[\Omega]$ : Communication line (SO<sub>p</sub>) pull-up resistance,  $C_b[F]$ : Communication line (SO<sub>p</sub>) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

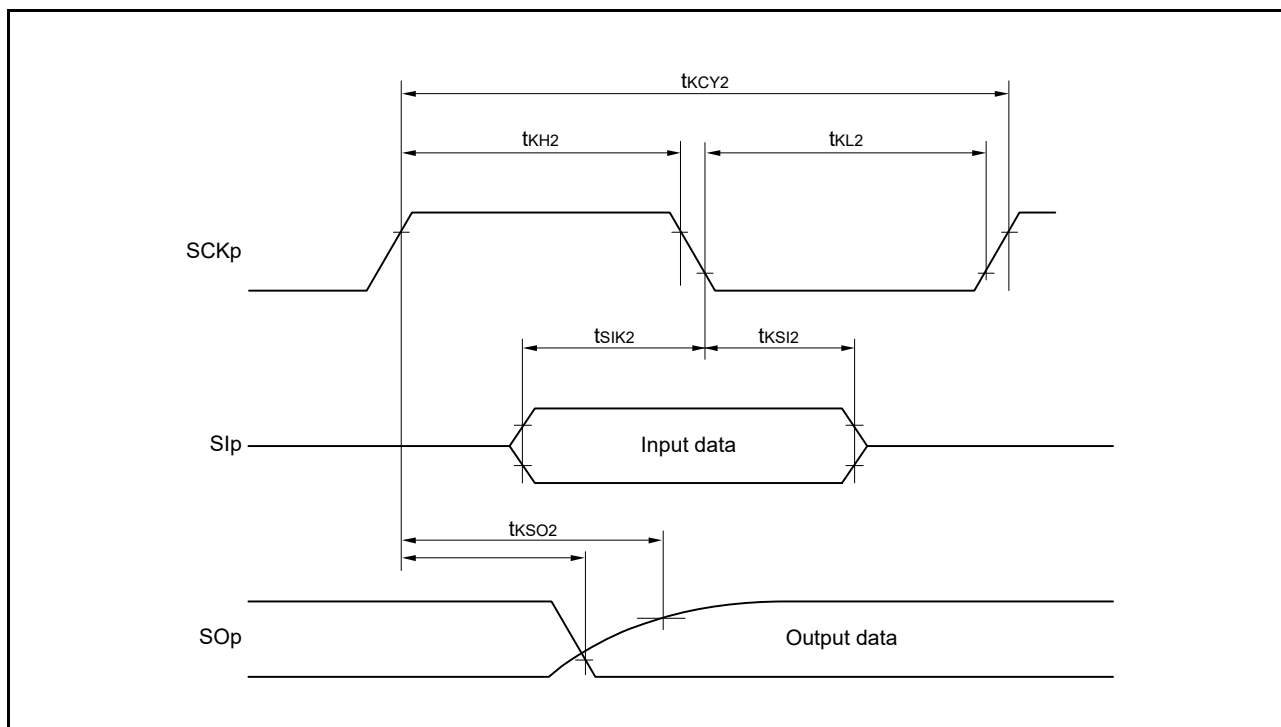
**Remark 3.** f<sub>MCK</sub>: Serial array unit operation clock frequency  
 To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).  
 m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

**Remark 4.** Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(b) Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



(c) Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



**Remark 1.** p: CSI number (p = 00, 01, 20), m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11), g: PIM and POM number (g = 1, 3, 7)

**Remark 2.** Communications by using CSI01 of 48-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

(10) Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)(T<sub>A</sub> = -40 to +105°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(1/2)

| Item                        | Symbol            | Conditions   | HS<br>(High-Speed Main)<br>Mode |                | LS<br>(Low-Speed Main)<br>Mode |                | LP<br>(Low-Power Main)<br>Mode |               | Unit |
|-----------------------------|-------------------|--|---------------------------------|----------------|--------------------------------|----------------|--------------------------------|---------------|------|
|                             |                   |  | Min.                            | Max.           | Min.                           | Max.           | Min.                           | Max.          |      |
| SCLr clock frequency        | f <sub>SCL</sub>  | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     |                                 | 1000<br>Note 1 |                                | 1000<br>Note 1 |                                | 300<br>Note 1 | kHz  |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     |                                 | 1000<br>Note 1 |                                | 1000<br>Note 1 |                                | 300<br>Note 1 | kHz  |
|                             |                   | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ                    |                                 | 400<br>Note 1  |                                | 400<br>Note 1  |                                | 300<br>Note 1 | kHz  |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    |                                 | 400<br>Note 1  |                                | 400<br>Note 1  |                                | 300<br>Note 1 | kHz  |
|                             |                   | 1.8 V ≤ V <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ |                                 | 300<br>Note 1  |                                | 300<br>Note 1  |                                | 300<br>Note 1 | kHz  |
| Hold time when SCLr is low  | t <sub>LOW</sub>  | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 475                             |                | 475                            |                | 1550                           |               | ns   |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 475                             |                | 475                            |                | 1550                           |               | ns   |
|                             |                   | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ                    | 1150                            |                | 1550                           |                | 1550                           |               | ns   |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 1150                            |                | 1550                           |                | 1550                           |               | ns   |
|                             |                   | 1.8 V ≤ V <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 1550                            |                | 1550                           |                | 1550                           |               | ns   |
| Hold time when SCLr is high | t <sub>HIGH</sub> | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 245                             |                | 245                            |                | 610                            |               | ns   |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                     | 200                             |                | 200                            |                | 610                            |               | ns   |
|                             |                   | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ                    | 675                             |                | 675                            |                | 610                            |               | ns   |
|                             |                   | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                    | 600                             |                | 600                            |                | 610                            |               | ns   |
|                             |                   | 1.8 V ≤ V <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <sup>Note 2</sup> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 610                             |                | 610                            |                | 610                            |               | ns   |

(10) Simplified I<sup>2</sup>C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)(T<sub>A</sub> = -40 to +105°C, 1.8 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

(2/2)

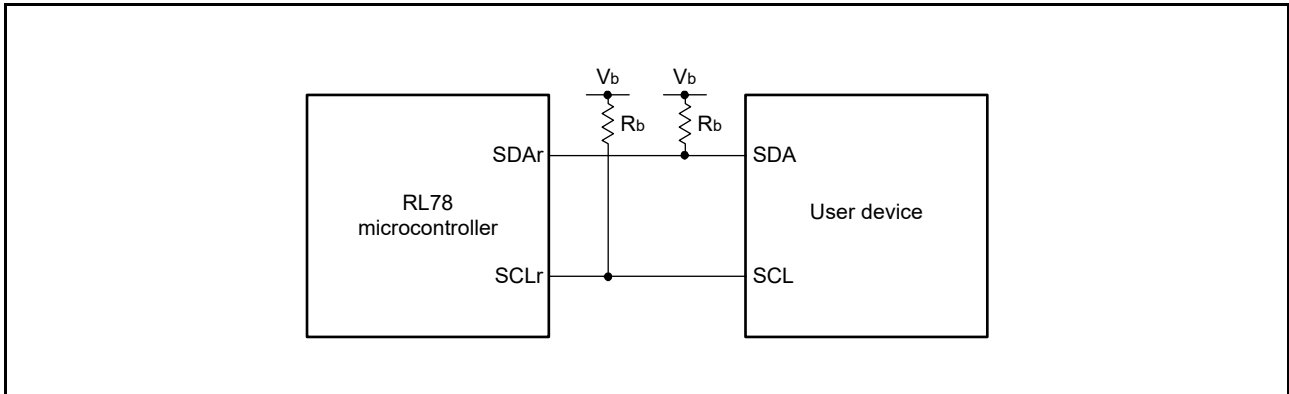
| Item                             | Symbol              | Conditions   | HS<br>(High-Speed Main)<br>Mode              |      | LS<br>(Low-Speed Main)<br>Mode               |      | LP<br>(Low-Power Main)<br>Mode               |      | Unit |
|----------------------------------|---------------------|--|--|------|--|------|--|------|------|
|                                  |                     |  | Min.   | Max. | Min.   | Max. | Min.   | Max. |      |
| Data setup time<br>(reception)   | t <sub>SU:DAT</sub> | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                 | 1/f <sub>MCK</sub><br>+ 135<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 135<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | ns   |
|                                  |                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                 | 1/f <sub>MCK</sub><br>+ 135<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 135<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | ns   |
|                                  |                     | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ                | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | ns   |
|                                  |                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <b>Note 2</b> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | 1/f <sub>MCK</sub><br>+ 190<br><b>Note 3</b> |      | ns   |
| Data hold time<br>(transmission) | t <sub>HD:DAT</sub> | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                 | 0  | 305  | 0  | 305  | 0  | 305  | ns   |
|                                  |                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 50 pF, R <sub>b</sub> = 2.7 kΩ                 | 0  | 305  | 0  | 305  | 0  | 305  | ns   |
|                                  |                     | 4.0 V ≤ V <sub>DD</sub> ≤ 5.5 V,<br>2.7 V ≤ V <sub>b</sub> ≤ 4.0 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.8 kΩ                | 0  | 355  | 0  | 355  | 0  | 355  | ns   |
|                                  |                     | 2.7 V ≤ V <sub>DD</sub> < 4.0 V,<br>2.3 V ≤ V <sub>b</sub> ≤ 2.7 V,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 2.7 kΩ                | 0  | 355  | 0  | 355  | 0  | 355  | ns   |
|                                  |                     | 1.8 V ≤ V <sub>DD</sub> < 3.3 V,<br>1.6 V ≤ V <sub>b</sub> ≤ 2.0 V <b>Note 2</b> ,<br>C <sub>b</sub> = 100 pF, R <sub>b</sub> = 5.5 kΩ | 0  | 405  | 0  | 405  | 0  | 405  | ns   |

**Note 1.** The listed times must be no greater than f<sub>MCK</sub>/4.**Note 2.** Use this setting with V<sub>DD</sub> ≥ V<sub>b</sub>.**Note 3.** Set f<sub>MCK</sub> so that it will not exceed the hold time when SCLr is low or high.

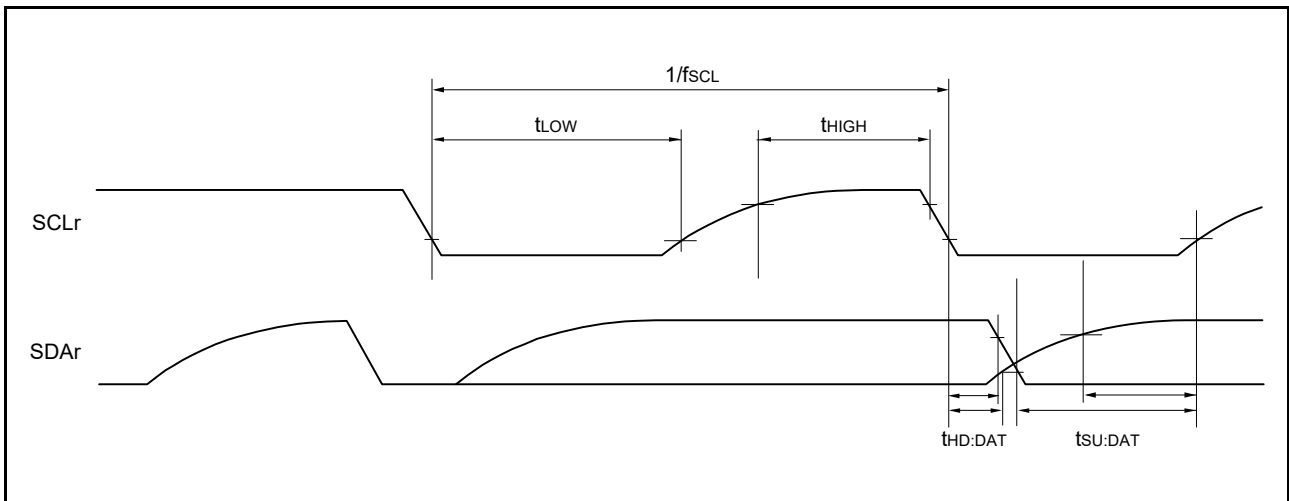
**Caution** Select the TTL input buffer and the N-ch open drain output [withstand voltage of V<sub>DD</sub>] mode for the SDAr pin and the N-ch open drain output [withstand voltage of V<sub>DD</sub>] mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V<sub>IH</sub> and V<sub>IL</sub>, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

(a) Connection in the I<sup>2</sup>C communications with devices operating at different voltage levels



(b) Timing of serial transfer in the simplified I<sup>2</sup>C communications with devices operating at different voltage levels



**Remark 1.**  $R_b[\Omega]$ : Communication line (SDAr, SCLr) pull-up resistance,  $C_b[F]$ : Communication line (SDAr, SCLr) load capacitance,  $V_b[V]$ : Communication line voltage

**Remark 2.** r: IIC number (r = 00, 01, 11, 20, 21), g: PIM and POM number (g = 0, 1, 3, 7), POM number (h = 1, 5, 7)

**Remark 3.**  $f_{MCK}$ : Serial array unit operation clock frequency

To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn).

m: Unit number, n: Channel number (mn = 00, 01, 03, 10, 11)

## 2.5.2 Serial interface UARTA

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item          | Symbol | Conditions | Min. | Typ. | Max.   | Unit |
|---------------|--------|------------|------|------|--------|------|
| Transfer rate |        |            | 200  | 0    | 153600 | bps  |

**Caution** Select the normal input buffer for the RxDAn pin and the normal output mode for the TxDAn pin by using port input mode register g (PIMg) and port output mode register g (POMg).

**Remark** n: Unit number (n = 0), g: PIM or POM number (g = 7)

### 2.5.3 Serial interface IICA

#### (1) I<sup>2</sup>C standard mode

(T<sub>A</sub> = -40 to +105°C, 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Item  | Symbol              | Conditions                              | Min. | Typ. | Max. | Unit |
|---|---------------------|---|------|------|------|------|
| SCLA0 clock frequency                           | f <sub>SCL</sub>    | Standard mode: f <sub>CLK</sub> ≥ 1 MHz | 0    |      | 100  | kHz  |
| Setup time of restart condition                 | t <sub>SU:STA</sub> |   | 4.7  |      |      | μs   |
| Hold time <sup>Note 1</sup>                     | t <sub>HD:STA</sub> |   | 4.0  |      |      | μs   |
| Hold time when SCLA0 is low                     | t <sub>LOW</sub>    |   | 4.7  |      |      | μs   |
| Hold time when SCLA0 is high                    | t <sub>HIGH</sub>   |   | 4.0  |      |      | μs   |
| Data setup time (reception)                     | t <sub>SU:DAT</sub> |   | 250  |      |      | ns   |
| Data hold time (transmission) <sup>Note 2</sup> | t <sub>HD:DAT</sub> |   | 0    |      | 3.45 | μs   |
| Setup time of stop condition                    | t <sub>SU:STO</sub> |   | 4.0  |      |      | μs   |
| Bus-free time                                   | t <sub>BUF</sub>    |   | 4.7  |      |      | μs   |

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of t<sub>HD:DAT</sub> applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

**Caution** The listed frequency and times apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (I<sub>OH1</sub>, I<sub>OL1</sub>, V<sub>OH1</sub>, V<sub>OL1</sub>) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (C<sub>b</sub>) and communication line pull-up resistor (R<sub>b</sub>) are as follows.  
C<sub>b</sub> = 400 pF, R<sub>b</sub> = 2.7 kΩ



(2) I<sup>2</sup>C fast mode

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item  | Symbol  | Conditions                                       | Min. | Typ. | Max. | Unit |
|---|---------|--|------|------|------|------|
| SCLA0 clock frequency                           | fSCL    | Fast mode: fCLK ≥ 3.5 MHz<br>1.8 V ≤ VDD ≤ 5.5 V | 0    |      | 400  | kHz  |
| Setup time of restart condition                 | tSU:STA | 1.8 V ≤ VDD ≤ 5.5 V                              | 0.6  |      |      | μs   |
| Hold time <sup>Note 1</sup>                     | tHD:STA | 1.8 V ≤ VDD ≤ 5.5 V                              | 0.6  |      |      | μs   |
| Hold time when SCLA0 is low                     | tLOW    | 1.8 V ≤ VDD ≤ 5.5 V                              | 1.3  |      |      | μs   |
| Hold time when SCLA0 is high                    | tHIGH   | 1.8 V ≤ VDD ≤ 5.5 V                              | 0.6  |      |      | μs   |
| Data setup time (reception)                     | tSU:DAT | 1.8 V ≤ VDD ≤ 5.5 V                              | 100  |      |      | ns   |
| Data hold time (transmission) <sup>Note 2</sup> | tHD:DAT | 1.8 V ≤ VDD ≤ 5.5 V                              | 0    |      | 0.9  | μs   |
| Setup time of stop condition                    | tSU:STO | 1.8 V ≤ VDD ≤ 5.5 V                              | 0.6  |      |      | μs   |
| Bus-free time                                   | tBUF    | 1.8 V ≤ VDD ≤ 5.5 V                              | 1.3  |      |      | μs   |

**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

**Caution** The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.  
Cb = 320 pF, Rb = 1.1 kΩ

(3) I<sup>2</sup>C fast mode plus

(T<sub>A</sub> = -40 to +105°C, 1.6 V ≤ V<sub>DD</sub> ≤ 5.5 V, V<sub>SS</sub> = 0 V)

| Item  | Symbol              | Conditions   | Min. | Typ. | Max. | Unit |
|---|---------------------|--|------|------|------|------|
| SCLA0 clock frequency                           | f <sub>SCL</sub>    | Fast mode plus: f <sub>CLK</sub> ≥ 10 MHz<br>2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V | 0    |      | 1000 | kHz  |
| Setup time of restart condition                 | t <sub>SU:STA</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.26 |      |      | μs   |
| Hold time <sup>Note 1</sup>                     | t <sub>HD:STA</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.26 |      |      | μs   |
| Hold time when SCLA0 is low                     | t <sub>LOW</sub>    | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.5  |      |      | μs   |
| Hold time when SCLA0 is high                    | t <sub>HIGH</sub>   | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.26 |      |      | μs   |
| Data setup time (reception)                     | t <sub>SU:DAT</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 50   |      |      | ns   |
| Data hold time (transmission) <sup>Note 2</sup> | t <sub>HD:DAT</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0    |      | 0.45 | μs   |
| Setup time of stop condition                    | t <sub>SU:STO</sub> | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.26 |      |      | μs   |
| Bus-free time                                   | t <sub>BUF</sub>    | 2.7 V ≤ V <sub>DD</sub> ≤ 5.5 V  | 0.5  |      |      | μs   |

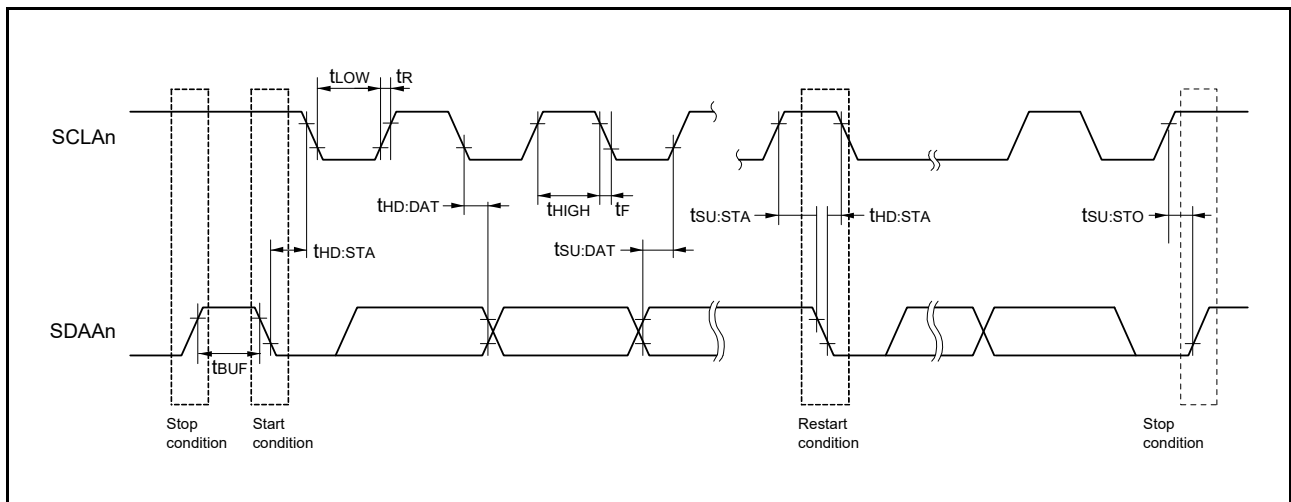
**Note 1.** The first clock pulse is generated after this period when the start or restart condition is detected.

**Note 2.** The maximum value of t<sub>HD:DAT</sub> applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

**Caution** The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

**Remark** The maximum value of communication line capacitance (C<sub>b</sub>) and communication line pull-up resistor (R<sub>b</sub>) are as follows.  
C<sub>b</sub> = 120 pF, R<sub>b</sub> = 1.1 kΩ

I<sup>2</sup>C serial transfer timing



**Remark** n = 0

## 2.6 Characteristics of the Analog Circuits

### 2.6.1 Characteristics of the A/D converter for TA = -40 to +85°C

Reference for the characteristics of the A/D converter

| Reference Voltage<br>Input Channel  | Reference Voltage (+) = AVREFP<br>Reference Voltage (-) = AVREFM | Reference Voltage (+) = VDD<br>Reference Voltage (-) = VSS | Reference Voltage (+) = VBGR<br>Reference Voltage (-) = AVREFM |
|---|--|--|--|
| ANI0 to ANI7  | See 2.6.1 (1)  | See 2.6.1 (3)  | See 2.6.1 (4)  |
| ANI16 to ANI19  | See 2.6.1 (2)  |  |  |
| Internal reference voltage,<br>temperature sensor output<br>voltage, and TSCAP voltage<br>of the CTSU | See 2.6.1 (1)  |  | —  |

- (1) Reference voltage (+) = AVREFP/ANI0 (ADREFP1 = 0, ADREFP0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

(TA = -40 to +85°C, 1.6 V ≤ AVREFP ≤ VDD ≤ 5.5 V, VSS = 0 V, reference voltage (+) = AVREFP,

reference voltage (-) = AVREFM = 0 V) (1/2)

| Item   | Symbol | Conditions   | Min.                                     | Typ.   | Max. | Unit  |      |
|--|--------|--|--|--------|------|-------|------|
| Resolution                                     | RES    |  | 8  |        | 10   | Bit   |      |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution<br>AVREFP = VDD <sup>Note 3</sup>  | 1.8 V ≤ AVREFP ≤ 5.5 V                   |        | 1.2  | ±3.5  | LSB  |
|  |        |  | 1.6 V ≤ AVREFP ≤ 5.5 V <sup>Note 4</sup> |        | 1.2  | ±7.0  | LSB  |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI2 to ANI7  | 3.6 V ≤ VDD ≤ 5.5 V                      | 2.125  |      | 39    | μs   |
|  |        |  | 2.7 V ≤ VDD ≤ 5.5 V                      | 3.1875 |      | 39    | μs   |
|  |        |  | 1.8 V ≤ VDD ≤ 5.5 V                      | 17     |      | 39    | μs   |
|  |        |  | 1.6 V ≤ VDD ≤ 5.5 V                      | 57     |      | 95    | μs   |
|  |        | 10-bit resolution<br>conversion target:<br>Internal reference<br>temperature sensor<br>output voltage, and<br>TSCAP voltage of<br>the CTSU | 3.6 V ≤ VDD ≤ 5.5 V                      | 2.375  |      | 39    | μs   |
|  |        |  | 2.7 V ≤ VDD ≤ 5.5 V                      | 3.5625 |      | 39    | μs   |
| Zero-scale error <sup>Notes 1, 2</sup>         | Ezs    | 10-bit resolution<br>AVREFP = VDD <sup>Note 3</sup>  | 1.8 V ≤ AVREFP ≤ 5.5 V                   |        |      | ±0.25 | %FSR |
|  |        |  | 1.6 V ≤ AVREFP ≤ 5.5 V <sup>Note 4</sup> |        |      | ±0.50 | %FSR |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution<br>AVREFP = VDD <sup>Note 3</sup>  | 1.8 V ≤ AVREFP ≤ 5.5 V                   |        |      | ±0.25 | %FSR |
|  |        |  | 1.6 V ≤ AVREFP ≤ 5.5 V <sup>Note 4</sup> |        |      | ±0.50 | %FSR |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution<br>AVREFP = VDD <sup>Note 3</sup>  | 1.8 V ≤ AVREFP ≤ 5.5 V                   |        |      | ±2.5  | LSB  |
|  |        |  | 1.6 V ≤ AVREFP ≤ 5.5 V <sup>Note 4</sup> |        |      | ±5.0  | LSB  |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution<br>AVREFP = VDD <sup>Note 3</sup>  | 1.8 V ≤ AVREFP ≤ 5.5 V                   |        |      | ±1.5  | LSB  |
|  |        |  | 1.6 V ≤ AVREFP ≤ 5.5 V <sup>Note 4</sup> |        |      | ±2.0  | LSB  |

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , reference voltage (+) =  $AV_{REFP}$ ,  
reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ ) (2/2)

| Item                 | Symbol    | Conditions  | Min.                       | Typ. | Max.        | Unit |
|----------------------|-----------|---|----------------------------|------|-------------|------|
| Analog input voltage | $V_{AIN}$ | ANI2 to ANI7  | 0                          |      | $AV_{REFP}$ | V    |
|                      |           | Internal reference voltage<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )        | $VBGR$ <b>Note 5</b>       |      |             | V    |
|                      |           | Temperature sensor output voltage<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ) | $V_{TMPS25}$ <b>Note 5</b> |      |             | V    |
|                      |           | TSCAP voltage of the CTSU<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )         | $V_{TSCAP}$                |      |             | V    |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When reference voltage (+) =  $V_{DD}$  and reference voltage (-) =  $V_{SS}$ , the maximum values are as follows.

Overall error: Add  $\pm 10$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .

Zero-scale/full-scale error: Add  $\pm 0.05\%$ FSR to the maximum value when  $V_{DD} = AV_{REFP}$ .

Integral linearity error and differential linearity error: Add  $\pm 0.5$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .

**Note 4.** The listed value applies when the settings of the maximum and minimum conversion time values are respectively  $57\ \mu\text{s}$  and  $95\ \mu\text{s}$ .

**Note 5.** See **2.6.3 Characteristics of the temperature sensor and internal reference voltage.**

(2) Reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0$ ,  $ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), conversion target: ANI16 to ANI19

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  
reference voltage (+) =  $AV_{REFP}$ , reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

| Item   | Symbol | Conditions  | Min.   | Typ.   | Max.        | Unit       |               |
|--|--------|---|--|--------|-------------|------------|---------------|
| Resolution                                     | RES    |   | 8  |        | 10          | Bit        |               |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$                      |        | 1.2         | $\pm 5.0$  | LSB           |
|  |        |   | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$<br><sup>Note 4</sup> |        | 1.2         | $\pm 5.0$  |               |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI16 to ANI19   | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                         | 2.125  |             | 39         | $\mu\text{s}$ |
|  |        |   | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                         | 3.1875 |             | 39         | $\mu\text{s}$ |
|  |        |   | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                         | 17     |             | 39         | $\mu\text{s}$ |
|  |        |   | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                         | 57     |             | 95         |               |
| Zero-scale error <sup>Notes 1, 2</sup>         | EZS    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$                      |        |             | $\pm 0.35$ | %FSR          |
|  |        |   | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$<br><sup>Note 4</sup> |        |             | $\pm 0.60$ |               |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$                      |        |             | $\pm 0.35$ | %FSR          |
|  |        |   | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$<br><sup>Note 4</sup> |        |             | $\pm 0.60$ |               |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$                      |        |             | $\pm 3.5$  | LSB           |
|  |        |   | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$<br><sup>Note 4</sup> |        |             | $\pm 6.0$  |               |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $1.8\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$                      |        |             | $\pm 2.0$  | LSB           |
|  |        |   | $1.6\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$<br><sup>Note 4</sup> |        |             | $\pm 2.5$  |               |
| Analog input voltage                           | VAIN   | ANI16 to ANI19  | 0  |        | $AV_{REFP}$ | V          |               |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.

- Overall error: Add  $\pm 4.0$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .
- Zero-scale/full-scale error: Add  $\pm 0.20\%$  FSR to the maximum value when  $V_{DD} = AV_{REFP}$ .
- Integral linearity error/differential linearity error: Add  $\pm 2.0$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .

**Note 4.** The listed value applies when the settings of the maximum and minimum conversion time values are respectively  $57\ \mu\text{s}$  and  $95\ \mu\text{s}$ .

- (3) Reference voltage (+) =  $V_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) =  $V_{SS}$  (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage<sup>Note 5</sup>, temperature sensor output voltage<sup>Note 5</sup>, TSCAP voltage of the CTSU

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , reference voltage (+) =  $V_{DD}$ , reference voltage (-) =  $V_{SS}$ )

| Item   | Symbol | Conditions   |  | Min.                           | Typ. | Max.       | Unit          |
|--|--------|--|--|--------------------------------|------|------------|---------------|
| Resolution                                     | RES    |  |  | 8                              |      | 10         | Bit           |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   |                                | 1.2  | $\pm 7.0$  | LSB           |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 3</sup> |                                | 1.2  | $\pm 10.5$ | LSB           |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI0 to ANI7,<br>ANI16 to ANI19   | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 2.125                          |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 3.1875                         |      | 39         | $\mu\text{s}$ |
|  |        |  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 17                             |      | 39         | $\mu\text{s}$ |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 57                             |      | 95         | $\mu\text{s}$ |
|  |        | 10-bit resolution<br>conversion target:<br>Internal reference<br>voltage,<br>temperature sensor<br>output voltage, and<br>TSCAP voltage of<br>the CTSU | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 2.375                          |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 3.5625                         |      | 39         | $\mu\text{s}$ |
|  |        |  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   | 17                             |      | 39         | $\mu\text{s}$ |
|  |        |  |  |                                |      |            |               |
| Zero-scale error <sup>Notes 1, 2</sup>         | Ezs    | 10-bit resolution  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   |                                |      | $\pm 0.60$ | %FSR          |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 3</sup> |                                |      | $\pm 0.85$ | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   |                                |      | $\pm 0.60$ | %FSR          |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 3</sup> |                                |      | $\pm 0.85$ | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   |                                |      | $\pm 4.0$  | LSB           |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 3</sup> |                                |      | $\pm 6.0$  | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution  | $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$                   |                                |      | $\pm 2.0$  | LSB           |
|  |        |  | $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ <sup>Note 3</sup> |                                |      | $\pm 2.5$  | LSB           |
| Analog input voltage                           | VAIN   | ANI0 to ANI7, ANI16 to ANI19   |  | 0                              |      | $V_{DD}$   | V             |
|  |        | Internal reference voltage<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )   |  | $V_{BGR}$ <sup>Note 4</sup>    |      |            | V             |
|  |        | Temperature sensor output voltage<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )  |  | $V_{TMPS25}$ <sup>Note 4</sup> |      |            | V             |
|  |        | TSCAP voltage of the CTSU<br>( $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ )  |  | $V_{TSCAP}$                    |      |            | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** The listed value applies when the settings of the maximum and minimum conversion time values are respectively 57  $\mu\text{s}$  and 95  $\mu\text{s}$ .

**Note 4.** See **2.6.3 Characteristics of the temperature sensor and internal reference voltage.**

**Note 5.** If the internal reference voltage or temperature sensor output voltage is to be A/D converted,  $V_{DD}$  must be at least 1.8 V.

- (4) Reference voltage (+) =  $V_{DD}$  (ADREFP1 = 1, ADREFP0 = 0), reference voltage (-) =  $AV_{REFM}/ANI1$  (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

( $T_A = -40$  to  $+85^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , reference voltage (+) =  $V_{BGR}$ <sup>Note 3</sup>, reference voltage (-) =  $AV_{REFM}$ <sup>Note 4</sup> = 0 V)

| Item   | Symbol | Conditions | Min. | Typ. | Max.                        | Unit          |
|--|--------|------------|------|------|-----------------------------|---------------|
| Resolution                                     | RES    |            | 8    |      |                             | Bit           |
| Conversion time                                | tCONV  |            | 17   |      | 39                          | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | Ezs    |            |      |      | $\pm 0.60$                  | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    |            |      |      | $\pm 2.0$                   | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    |            |      |      | $\pm 1.0$                   | LSB           |
| Analog input voltage                           | VAIN   |            | 0    |      | $V_{BGR}$ <sup>Note 3</sup> | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** See **2.6.3 Characteristics of the temperature sensor and internal reference voltage.**

**Note 4.** When reference voltage (-) =  $V_{SS}$ , the maximum values are as follows.

- Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value when reference voltage (-) =  $AV_{REFM}$ .
- Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value when reference voltage (-) =  $AV_{REFM}$ .
- Differential linearity error: Add  $\pm 0.2$  LSB to the maximum value when reference voltage (-) =  $AV_{REFM}$ .

## 2.6.2 Characteristics of the A/D converter for $T_A = -40$ to $+105^\circ\text{C}$

Reference for the characteristics of the A/D converter

| Reference Voltage<br>Input Channel  | Reference Voltage (+) = AVREFF<br>Reference Voltage (-) = AVREFM | Reference Voltage (+) = VDD<br>Reference Voltage (-) = VSS | Reference Voltage (+) = VBGR<br>Reference Voltage (-) = AVREFM |
|---|--|--|--|
| ANI0 to ANI7  | See 2.6.2 (1)  | See 2.6.2 (3)  | See 2.6.2 (4)  |
| ANI16 to ANI19  | See 2.6.2 (2)  |  |  |
| Internal reference voltage,<br>temperature sensor output<br>voltage, and TSCAP voltage<br>of the CTSU | See 2.6.2 (1)  |  | —  |

- (1) Reference voltage (+) = AVREFF/ANI0 (ADREFF1 = 0, ADREFF0 = 1), reference voltage (-) = AVREFM/ANI1 (ADREFM = 1), conversion target: ANI2 to ANI7, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq \text{AVREFF} \leq \text{VDD} \leq 5.5\text{ V}$ ,  $\text{VSS} = 0\text{ V}$ , reference voltage (+) = AVREFF, reference voltage (-) = AVREFM = 0 V)

| Item   | Symbol | Conditions   | Min.   | Typ.   | Max.                     | Unit          |
|--|--------|--|--|--------|--------------------------|---------------|
| Resolution                                     | RES    |  | 8  |        | 10                       | Bit           |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution<br>AVREFF = VDD <sup>Note 3</sup><br>$2.4\text{ V} \leq \text{AVREFF} \leq 5.5\text{ V}$   |  | 1.2    | $\pm 3.5$                | LSB           |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI2 to ANI7  | $3.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 2.125  | 39                       | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 3.1875 | 39                       | $\mu\text{s}$ |
|  |        |  | $2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 17     | 39                       | $\mu\text{s}$ |
|  |        | 10-bit resolution<br>conversion target:<br>Internal reference<br>voltage,<br>temperature sensor<br>output voltage, and<br>TSCAP voltage of<br>the CTSU | $3.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 2.375  | 39                       | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 3.5625 | 39                       | $\mu\text{s}$ |
|  |        |  | $2.4\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$ | 17     | 39                       | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | EZS    | 10-bit resolution<br>AVREFF = VDD <sup>Note 3</sup><br>$2.4\text{ V} \leq \text{AVREFF} \leq 5.5\text{ V}$   |  |        | $\pm 0.25$               | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution<br>AVREFF = VDD <sup>Note 3</sup><br>$2.4\text{ V} \leq \text{AVREFF} \leq 5.5\text{ V}$   |  |        | $\pm 0.25$               | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution<br>AVREFF = VDD <sup>Note 3</sup><br>$2.4\text{ V} \leq \text{AVREFF} \leq 5.5\text{ V}$   |  |        | $\pm 2.5$                | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution<br>AVREFF = VDD <sup>Note 3</sup><br>$2.4\text{ V} \leq \text{AVREFF} \leq 5.5\text{ V}$   |  |        | $\pm 1.5$                | LSB           |
| Analog input voltage                           | VAIN   | ANI2 to ANI7   | 0  |        | AVREFF                   | V             |
|  |        | Internal reference voltage   |  |        | VBGR <sup>Note 4</sup>   | V             |
|  |        | Temperature sensor output voltage  |  |        | VTMP25 <sup>Note 4</sup> | V             |
|  |        | TSCAP voltage of the CTSU  |  |        | VTSCAP                   | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When reference voltage (+) = VDD and reference voltage (-) = VSS, the maximum values are as follows.

Overall error: Add  $\pm 10$  LSB to the maximum value when  $\text{VDD} = \text{AVREFF}$ .

Zero-scale/full-scale error: Add  $\pm 0.05\%$ FSR to the maximum value when  $\text{VDD} = \text{AVREFF}$ .

Integral linearity error and differential linearity error: Add  $\pm 0.5$  LSB to the maximum value when  $\text{VDD} = \text{AVREFF}$ .

**Note 4.** See 2.6.3 Characteristics of the temperature sensor and internal reference voltage.



(2) Reference voltage (+) =  $AV_{REFP}/ANI0$  ( $ADREFP1 = 0, ADREFP0 = 1$ ), reference voltage (-) =  $AV_{REFM}/ANI1$  ( $ADREFM = 1$ ), conversion target: ANI16 to ANI19

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ ,  
reference voltage (+) =  $AV_{REFP}$ , reference voltage (-) =  $AV_{REFM} = 0\text{ V}$ )

| Item   | Symbol | Conditions  |   | Min.   | Typ. | Max.        | Unit          |
|--|--------|---|---|--------|------|-------------|---------------|
| Resolution                                     | RES    |   |   | 8      |      | 10          | Bit           |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |        | 1.2  | $\pm 5.0$   | LSB           |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI16 to ANI19   | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 2.125  |      | 39          | $\mu\text{s}$ |
|  |        |   | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 3.1875 |      | 39          | $\mu\text{s}$ |
|  |        |   | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 17     |      | 39          | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | EZS    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |        |      | $\pm 0.35$  | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |        |      | $\pm 0.35$  | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |        |      | $\pm 3.5$   | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution<br>$AV_{REFP} = V_{DD}$ <sup>Note 3</sup> | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |        |      | $\pm 2.0$   | LSB           |
| Analog input voltage                           | VAIN   | ANI16 to ANI19  |   | 0      |      | $AV_{REFP}$ | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** When  $AV_{REFP} < V_{DD}$ , the maximum values are as follows.

- Overall error: Add  $\pm 4.0$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .
- Zero-scale/full-scale error: Add  $\pm 0.20\%$  FSR to the maximum value when  $V_{DD} = AV_{REFP}$ .
- Integral linearity error/differential linearity error: Add  $\pm 2.0$  LSB to the maximum value when  $V_{DD} = AV_{REFP}$ .

- (3) Reference voltage (+) =  $V_{DD}$  (ADREFP1 = 0, ADREFP0 = 0), reference voltage (-) =  $V_{SS}$  (ADREFM = 0), conversion target: ANI0 to ANI7, and ANI16 to ANI19, internal reference voltage, temperature sensor output voltage, and TSCAP voltage of the CTSU

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , reference voltage (+) =  $V_{DD}$ , reference voltage (-) =  $V_{SS}$ )

| Item   | Symbol | Conditions   |   | Min.                           | Typ. | Max.       | Unit          |
|--|--------|--|---|--------------------------------|------|------------|---------------|
| Resolution                                     | RES    |  |   | 8                              |      | 10         | Bit           |
| Overall error <sup>Note 1</sup>                | AINL   | 10-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |                                | 1.2  | $\pm 7.0$  | LSB           |
| Conversion time                                | tCONV  | 10-bit resolution<br>conversion target:<br>ANI0 to ANI7,<br>ANI16 to ANI19   | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 2.125                          |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 3.1875                         |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 17                             |      | 39         | $\mu\text{s}$ |
|  |        | 10-bit resolution<br>conversion target:<br>Internal reference<br>voltage,<br>temperature sensor<br>output voltage, and<br>and TSCAP voltage of<br>the CTSU | $3.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 2.375                          |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.7\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 3.5625                         |      | 39         | $\mu\text{s}$ |
|  |        |  | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    | 17                             |      | 39         | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | Ezs    | 10-bit resolution  | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    |                                |      | $\pm 0.60$ | %FSR          |
| Full-scale error <sup>Notes 1, 2</sup>         | EFS    | 10-bit resolution  | $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$    |                                |      | $\pm 0.60$ | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    | 10-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |                                |      | $\pm 4.0$  | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    | 10-bit resolution  | $2.4\text{ V} \leq AV_{REFP} \leq 5.5\text{ V}$ |                                |      | $\pm 2.0$  | LSB           |
| Analog input voltage                           | VAIN   | ANI0 to ANI7, ANI16 to ANI19   |   | 0                              |      | $V_{DD}$   | V             |
|  |        | Internal reference voltage   |   | $V_{BGR}$ <sup>Note 3</sup>    |      |            | V             |
|  |        | Temperature sensor output voltage  |   | $V_{TMPS25}$ <sup>Note 3</sup> |      |            | V             |
|  |        | TSCAP voltage of the CTSU  |   | $V_{TSCAP}$                    |      |            | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** See **2.6.3 Characteristics of the temperature sensor and internal reference voltage.**

- (4) Reference voltage (+) =  $V_{DD}$  (ADREFP1 = 1, ADREFP0 = 0), reference voltage (–) =  $AV_{REFM}/ANI1$  (ADREFM = 1), conversion target: ANI0, ANI2 to ANI7, ANI16 to ANI19

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ , reference voltage (+) =  $V_{BGR}$ <sup>Note 3</sup>, reference voltage (–) =  $AV_{REFM}$ <sup>Note 4</sup> = 0 V)

| Item   | Symbol | Conditions | Min. | Typ. | Max.                        | Unit          |
|--|--------|------------|------|------|-----------------------------|---------------|
| Resolution                                     | RES    |            | 8    |      |                             | Bit           |
| Conversion time                                | tCONV  |            | 17   |      | 39                          | $\mu\text{s}$ |
| Zero-scale error <sup>Notes 1, 2</sup>         | Ezs    |            |      |      | $\pm 0.60$                  | %FSR          |
| Integral linearity error <sup>Note 1</sup>     | ILE    |            |      |      | $\pm 2.0$                   | LSB           |
| Differential linearity error <sup>Note 1</sup> | DLE    |            |      |      | $\pm 1.0$                   | LSB           |
| Analog input voltage                           | VAIN   |            | 0    |      | $V_{BGR}$ <sup>Note 3</sup> | V             |

**Note 1.** This value does not include the quantization error ( $\pm 1/2$  LSB).

**Note 2.** This value is indicated as a ratio (%FSR) to the full-scale value.

**Note 3.** See **2.6.3 Characteristics of the temperature sensor and internal reference voltage.**

**Note 4.** When reference voltage (–) =  $V_{SS}$ , the maximum values are as follows.

- Zero-scale error: Add  $\pm 0.35\%$ FSR to the maximum value when reference voltage (–) =  $AV_{REFM}$ .
- Integral linearity error: Add  $\pm 0.5$  LSB to the maximum value when reference voltage (–) =  $AV_{REFM}$ .
- Differential linearity error: Add  $\pm 0.2$  LSB to the maximum value when reference voltage (–) =  $AV_{REFM}$ .

### 2.6.3 Characteristics of the temperature sensor and internal reference voltage

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ ,  $V_{SS} = 0\text{ V}$ )

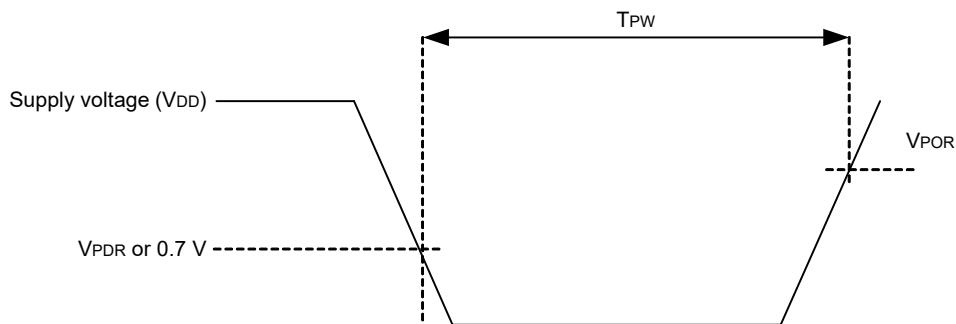
| Item                              | Symbol  | Conditions   | Min. | Typ. | Max. | Unit                 |
|-----------------------------------|---------|--|------|------|------|----------------------|
| Temperature sensor output voltage | VTMPS25 | Setting ADS register = 80H, $T_A = +25^\circ\text{C}$    |      | 1.05 |      | V                    |
| Internal reference voltage        | VBGR    | Setting ADS register = 81H                               | 1.42 | 1.48 | 1.54 | V                    |
| Temperature coefficient           | FVTMPS  | Temperature dependency of the temperature sensor voltage |      | -3.3 |      | mV/ $^\circ\text{C}$ |
| Operation stabilization wait time | tAMP    |  | 5    |      |      | $\mu\text{s}$        |

### 2.6.4 Characteristics of the POR circuit

( $T_A = -40$  to  $+105^\circ\text{C}$ ,  $V_{SS} = 0\text{ V}$ )

| Item                                | Symbol     | Conditions | Min. | Typ. | Max. | Unit          |
|-------------------------------------|------------|------------|------|------|------|---------------|
| Detection voltage                   | VPOR, VPDR |            | 1.43 | 1.50 | 1.57 | V             |
| Minimum pulse width <sup>Note</sup> | TPW        |            | 300  |      |      | $\mu\text{s}$ |

**Note** This width is the minimum time required for a POR reset when  $V_{DD}$  falls below  $VPDR$ . This width is also the minimum time required for a POR reset from when  $V_{DD}$  falls below  $0.7\text{ V}$  to when  $V_{DD}$  exceeds  $VPOR$  in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



## 2.6.5 Characteristics of the LVD circuit

### (1) LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item              | Symbol               | Conditions                           | Min. | Typ. | Max. | Unit |    |
|-------------------|----------------------|--------------------------------------|------|------|------|------|----|
| Detection voltage | VLVD00               | The power supply voltage is rising.  | 3.84 | 3.96 | 4.08 | V    |    |
|                   |                      | The power supply voltage is falling. | 3.76 | 3.88 | 4.00 | V    |    |
|                   | VLVD01               | The power supply voltage is rising.  | 2.88 | 2.97 | 3.06 | V    |    |
|                   |                      | The power supply voltage is falling. | 2.82 | 2.91 | 3.00 | V    |    |
|                   | VLVD02               | The power supply voltage is rising.  | 2.59 | 2.67 | 2.75 | V    |    |
|                   |                      | The power supply voltage is falling. | 2.54 | 2.62 | 2.70 | V    |    |
|                   | VLVD03               | The power supply voltage is rising.  | 2.31 | 2.38 | 2.45 | V    |    |
|                   |                      | The power supply voltage is falling. | 2.26 | 2.33 | 2.40 | V    |    |
|                   | VLVD04               | The power supply voltage is rising.  | 1.84 | 1.90 | 1.95 | V    |    |
|                   |                      | The power supply voltage is falling. | 1.80 | 1.86 | 1.91 | V    |    |
|                   | VLVD05               | The power supply voltage is rising.  | 1.64 | 1.69 | 1.74 | V    |    |
|                   |                      | The power supply voltage is falling. | 1.60 | 1.65 | 1.70 | V    |    |
|                   | Minimum pulse width  | tLW                                  |      | 500  |      |      | μs |
|                   | Detection delay time |                                      |      |      |      | 500  | μs |

## (2) LVD1 Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item                 |                                      | Symbol          | Conditions                           | Min. | Typ. | Max. | Unit |
|----------------------|--------------------------------------|-----------------|--------------------------------------|------|------|------|------|
| Detection voltage    | Supply voltage level                 | VLVD10          | The power supply voltage is rising.  | 4.08 | 4.16 | 4.24 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 4.00 | 4.08 | 4.16 | V    |
|                      |                                      | VLVD11          | The power supply voltage is rising.  | 3.88 | 3.96 | 4.04 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 3.80 | 3.88 | 3.96 | V    |
|                      |                                      | VLVD12          | The power supply voltage is rising.  | 3.68 | 3.75 | 3.82 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 3.60 | 3.67 | 3.74 | V    |
|                      |                                      | VLVD13          | The power supply voltage is rising.  | 3.48 | 3.55 | 3.62 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 3.40 | 3.47 | 3.54 | V    |
|                      |                                      | VLVD14          | The power supply voltage is rising.  | 3.28 | 3.35 | 3.42 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 3.20 | 3.27 | 3.34 | V    |
|                      |                                      | VLVD15          | The power supply voltage is rising.  | 3.07 | 3.13 | 3.19 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 3.00 | 3.06 | 3.12 | V    |
|                      |                                      | VLVD16          | The power supply voltage is rising.  | 2.91 | 2.97 | 3.03 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.85 | 2.91 | 2.97 | V    |
|                      |                                      | VLVD17          | The power supply voltage is rising.  | 2.76 | 2.82 | 2.87 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.70 | 2.76 | 2.81 | V    |
|                      |                                      | VLVD18          | The power supply voltage is rising.  | 2.61 | 2.66 | 2.71 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.55 | 2.60 | 2.65 | V    |
|                      |                                      | VLVD19          | The power supply voltage is rising.  | 2.45 | 2.50 | 2.55 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.40 | 2.45 | 2.50 | V    |
|                      |                                      | VLVD110         | The power supply voltage is rising.  | 2.35 | 2.40 | 2.45 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.30 | 2.35 | 2.40 | V    |
|                      |                                      | VLVD111         | The power supply voltage is rising.  | 2.25 | 2.30 | 2.34 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.20 | 2.25 | 2.29 | V    |
|                      |                                      | VLVD112         | The power supply voltage is rising.  | 2.15 | 2.20 | 2.24 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.10 | 2.15 | 2.19 | V    |
|                      |                                      | VLVD113         | The power supply voltage is rising.  | 2.05 | 2.09 | 2.13 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 2.00 | 2.04 | 2.08 | V    |
|                      |                                      | VLVD114         | The power supply voltage is rising.  | 1.94 | 1.98 | 2.02 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 1.90 | 1.94 | 1.98 | V    |
|                      |                                      | VLVD115<br>Note | The power supply voltage is rising.  | 1.84 | 1.88 | 1.91 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 1.80 | 1.84 | 1.87 | V    |
|                      |                                      | VLVD116<br>Note | The power supply voltage is rising.  | 1.74 | 1.78 | 1.81 | V    |
|                      |                                      |                 | The power supply voltage is falling. | 1.70 | 1.74 | 1.77 | V    |
| VLVD117<br>Note      | The power supply voltage is rising.  | 1.64            | 1.67                                 | 1.70 | V    |      |      |
|                      | The power supply voltage is falling. | 1.60            | 1.63                                 | 1.66 | V    |      |      |
| Minimum pulse width  |                                      | tLW             |                                      | 500  |      |      | μs   |
| Detection delay time |                                      |                 |                                      |      |      | 500  | μs   |

**Note** This setting can only be used when LVD0 is disabled.

### 2.6.6 Characteristics of the rising slope of the power supply voltage

(TA = -40 to +105°C, VSS = 0 V)

| Item                              | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|-----------------------------------|--------|------------|------|------|------|------|
| Power supply voltage rising slope | SVDD   |            |      |      | 54   | V/ms |

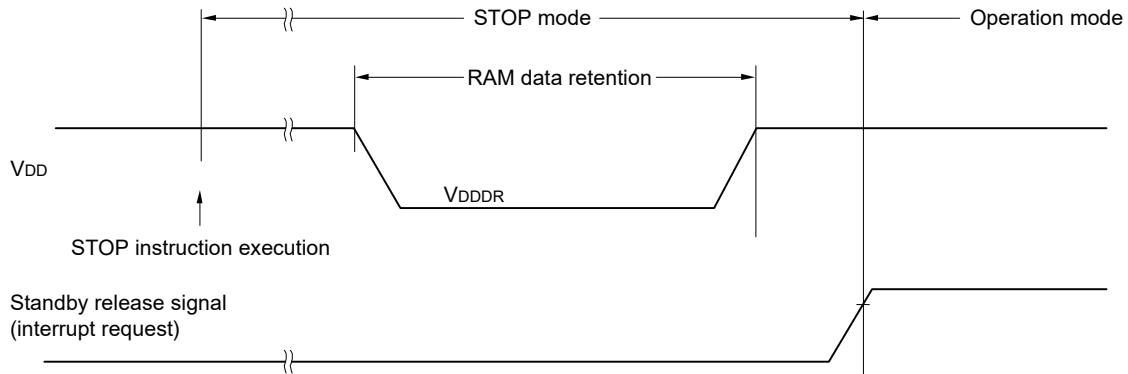
**Caution** Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VDD reaches the operating voltage range shown in AC characteristics.

### 2.7 Characteristics of Retention of RAM Data

(TA = -40 to +105°C, VSS = 0V)

| Item                          | Symbol | Conditions | Min.                 | Typ. | Max. | Unit |
|-------------------------------|--------|------------|----------------------|------|------|------|
| Data retention supply voltage | VDDDR  |            | 1.43 <sup>Note</sup> |      | 5.5  | V    |

**Note** This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



### 2.8 Characteristics of Flash Memory Programming

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item   | Symbol | Conditions                          | Min.    | Typ.      | Max. | Unit  |
|--|--------|-------------------------------------|---------|-----------|------|-------|
| CPU/peripheral hardware clock frequency                | fCLK   |                                     | 1       |           | 32   | MHz   |
| Number of code flash rewrites <sup>Notes 1, 2, 3</sup> | Cerwr  | Retained for 20 years<br>TA = +85°C | 1,000   |           |      | Times |
| Number of data flash rewrites <sup>Notes 1, 2, 3</sup> |        | Retained for 1 year<br>TA = +25°C   |         | 1,000,000 |      |       |
|  |        | Retained for 5 years<br>TA = +85°C  | 100,000 |           |      |       |
|  |        | Retained for 20 years<br>TA = +85°C | 10,000  |           |      |       |

**Note 1.** 1 erase + 1 write after the erase is regarded as 1 rewrite.  
The retaining years are until next rewrite after the rewrite.

**Note 2.** The listed numbers of times apply when using flash memory programmer and Renesas Electronics self-programming library.

**Note 3.** These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.



## (1) Code flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item   |          | Symbol  | fCLK = 1 MHz |      |        | fCLK = 2 MHz, 3 MHz |      |        | 4 MHz ≤ fCLK < 8 MHz |      |       | 8 MHz ≤ fCLK < 32 MHz |      |       | fCLK = 32 MHz |      |       | Unit |
|--|----------|---------|--------------|------|--------|---------------------|------|--------|----------------------|------|-------|-----------------------|------|-------|---------------|------|-------|------|
|  |          |         | Min.         | Typ. | Max.   | Min.                | Typ. | Max.   | Min.                 | Typ. | Max.  | Min.                  | Typ. | Max.  | Min.          | Typ. | Max.  |      |
| Programming time   | 4 bytes  | tp4     | —            | 74.7 | 656.5  | —                   | 51.0 | 464.6  | —                    | 41.7 | 384.8 | —                     | 37.1 | 346.2 | —             | 34.2 | 321.9 | μs   |
| Erasure time   | 2 Kbytes | te2K    | —            | 10.4 | 312.2  | —                   | 7.7  | 258.5  | —                    | 6.4  | 231.8 | —                     | 5.8  | 218.4 | —             | 5.6  | 214.4 | ms   |
| Blank checking time  | 4 bytes  | tbc4    | —            | —    | 38.4   | —                   | —    | 19.2   | —                    | —    | 13.1  | —                     | —    | 10.2  | —             | —    | 8.3   | μs   |
|  | 2 Kbytes | tbc2K   | —            | —    | 2618.9 | —                   | —    | 1309.5 | —                    | —    | 658.3 | —                     | —    | 332.8 | —             | —    | 234.1 | μs   |
| Time taken to forcibly stop the erasure                                      |          | tSED    | —            | —    | 18.0   | —                   | —    | 14.0   | —                    | —    | 12.0  | —                     | —    | 11.0  | —             | —    | 10.3  | μs   |
| Security setting time  |          | tAWSSAS | —            | 18.2 | 526.2  | —                   | 14.4 | 469.2  | —                    | 12.5 | 441.1 | —                     | 11.6 | 427.1 | —             | 11.3 | 422.6 | ms   |
| Time until programming starts following cancellation of the STOP instruction |          | —       | 20           | —    | —      | 20                  | —    | —      | 20                   | —    | —     | 20                    | —    | —     | 20            | —    | —     | μs   |

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

## (2) Data flash memory

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item   |           | Symbol | fCLK = 1 MHz |      |        | fCLK = 2 MHz, 3 MHz |      |       | 4 MHz ≤ fCLK < 8 MHz |      |       | 8 MHz ≤ fCLK < 32 MHz |      |       | fCLK = 32 MHz |      |       | Unit |
|--|-----------|--------|--------------|------|--------|---------------------|------|-------|----------------------|------|-------|-----------------------|------|-------|---------------|------|-------|------|
|  |           |        | Min.         | Typ. | Max.   | Min.                | Typ. | Max.  | Min.                 | Typ. | Max.  | Min.                  | Typ. | Max.  | Min.          | Typ. | Max.  |      |
| Programming time   | 1 byte    | tp4    | —            | 74.7 | 656.5  | —                   | 51.0 | 464.6 | —                    | 41.7 | 384.8 | —                     | 37.1 | 346.2 | —             | 34.2 | 321.9 | μs   |
| Erasure time   | 256 bytes | te2K   | —            | 7.8  | 259.2  | —                   | 6.4  | 232.0 | —                    | 5.8  | 218.5 | —                     | 5.5  | 211.8 | —             | 5.4  | 209.7 | ms   |
| Blank checking time  | 1 byte    | tbc4   | —            | —    | 38.4   | —                   | —    | 19.2  | —                    | —    | 13.1  | —                     | —    | 10.2  | —             | —    | 8.3   | μs   |
|  | 256 bytes | tbc2K  | —            | —    | 1326.1 | —                   | —    | 663.1 | —                    | —    | 335.1 | —                     | —    | 171.2 | —             | —    | 121.0 | μs   |
| Time taken to forcibly stop the erasure                                      |           | tSED   | —            | —    | 18.0   | —                   | —    | 14.0  | —                    | —    | 12.0  | —                     | —    | 11.0  | —             | —    | 10.3  | μs   |
| Time until programming starts following cancellation of the STOP instruction |           | —      | 20           | —    | —      | 20                  | —    | —     | 20                   | —    | —     | 20                    | —    | —     | 20            | —    | —     | μs   |
| Time until reading starts following setting DFLEN to 1                       |           | —      | 0.25         | —    | —      | 0.25                | —    | —     | 0.25                 | —    | —     | 0.25                  | —    | —     | 0.25          | —    | —     | μs   |

**Caution** The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

### 2.9 Dedicated Flash Memory Programmer Communication (UART)

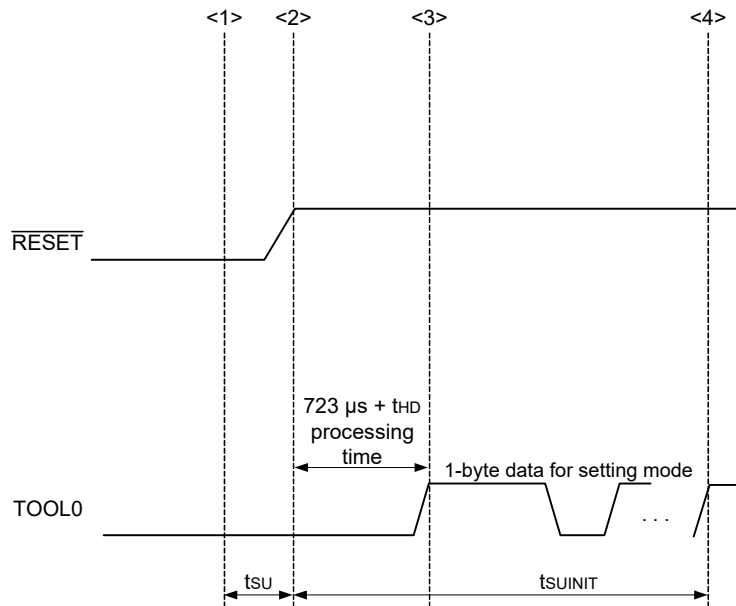
(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item          | Symbol | Conditions                | Min.    | Typ. | Max.      | Unit |
|---------------|--------|---------------------------|---------|------|-----------|------|
| Transfer rate |        | During serial programming | 115,200 |      | 1,000,000 | bps  |

### 2.10 Timing of Entry to Flash Memory Programming Modes

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

| Item   | Symbol  | Conditions  | Min. | Typ. | Max. | Unit |
|--|---------|---|------|------|------|------|
| Time to complete the communication for the initial setting after the external reset is released  | tsuINIT | POR and LVD reset must be released before the external reset is released. |      |      | 100  | ms   |
| Time to release the external reset after the TOOL0 pin is set to the low level   | tsu     | POR and LVD reset must be released before the external reset is released. | 10   |      |      | μs   |
| Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included) | tHD     | POR and LVD reset must be released before the external reset is released. | 1    |      |      | ms   |



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

**Remark** tsuINIT: The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

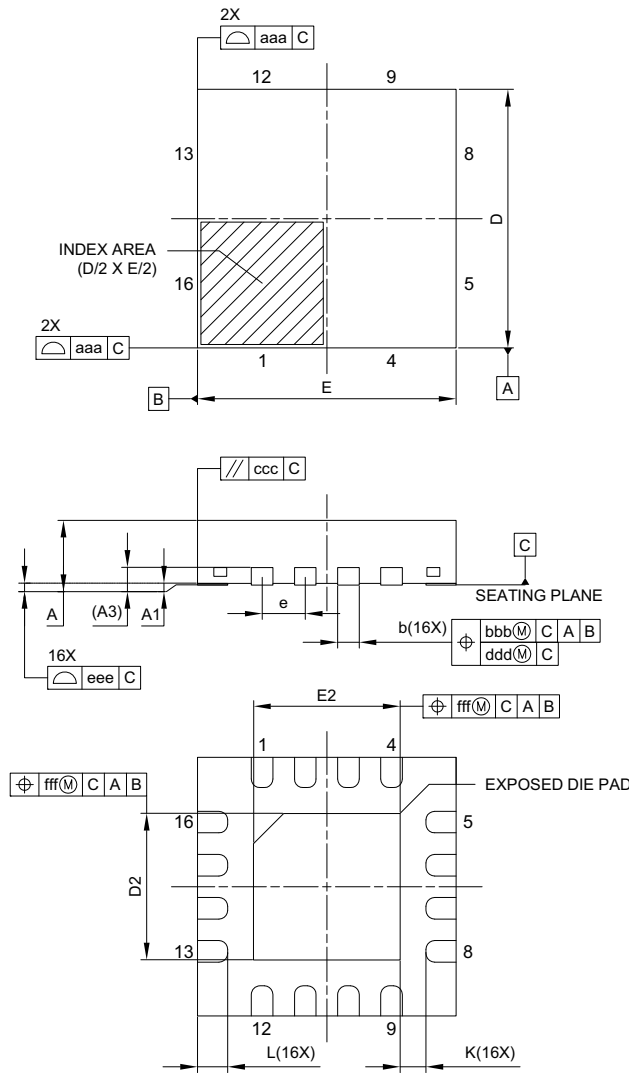
tsu: Time to release the external reset after the TOOL0 pin is set to the low level

tHD: Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

### 3. Package Drawings

#### 3.1 16-pin Products

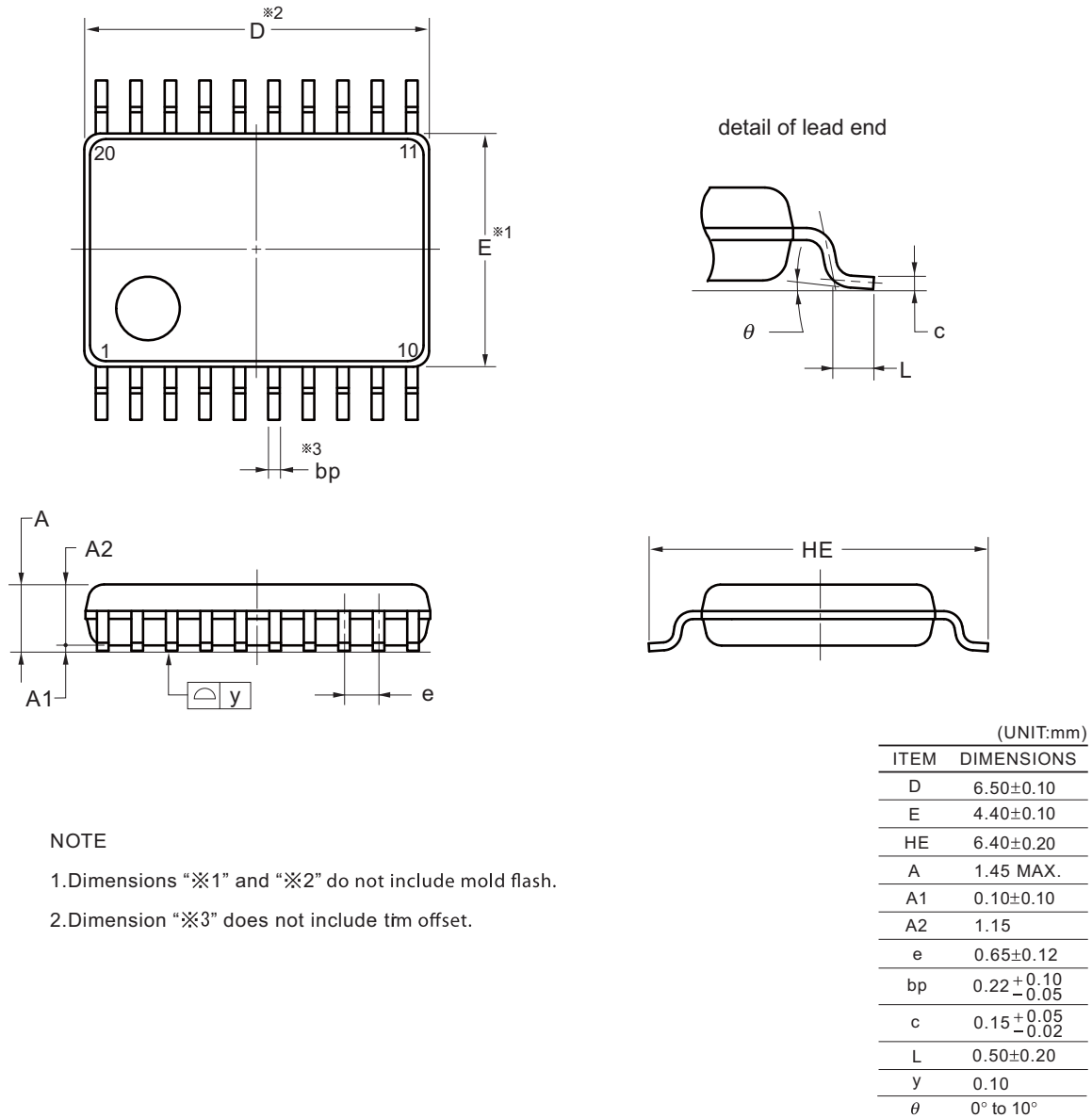
|                     |              |               |
|---------------------|--------------|---------------|
| JEITA Package code  | RENESAS code | MASS(TYP.)[g] |
| P-HWQFN016-3x3-0.50 | PWQN0016KD-A | 0.02          |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 0.80 |
| A1               | 0.00                     | 0.02 | 0.05 |
| A3               | 0.203 REF.               |      |      |
| b                | 0.20                     | 0.25 | 0.30 |
| D                | 3.00 BSC                 |      |      |
| E                | 3.00 BSC                 |      |      |
| e                | 0.50 BSC                 |      |      |
| L                | 0.30                     | 0.35 | 0.40 |
| K                | 0.20                     | —    | —    |
| D2               | 1.65                     | 1.70 | 1.75 |
| E2               | 1.65                     | 1.70 | 1.75 |
| aaa              | 0.15                     |      |      |
| bbb              | 0.10                     |      |      |
| ccc              | 0.10                     |      |      |
| ddd              | 0.05                     |      |      |
| eee              | 0.08                     |      |      |
| fff              | 0.10                     |      |      |

3.2 20-pin Products

|                        |              |                |                 |
|------------------------|--------------|----------------|-----------------|
| JEITA Package Code     | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LSSOP20-4.4x6.5-0.65 | PLSP0020JB-A | P20MA-65-NAA-1 | 0.1             |



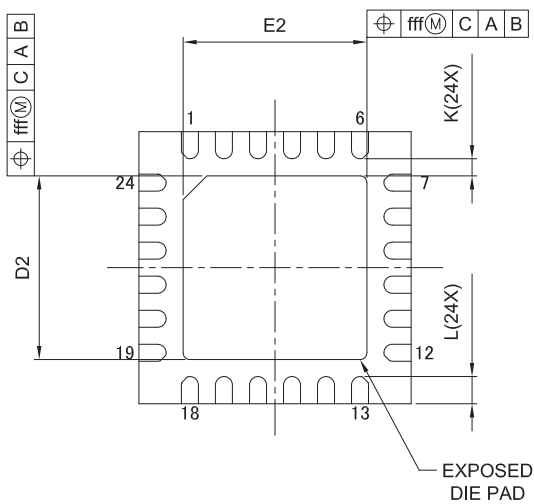
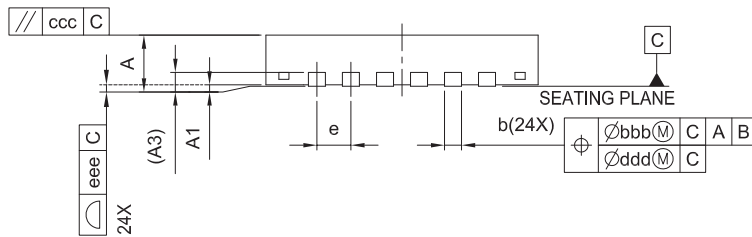
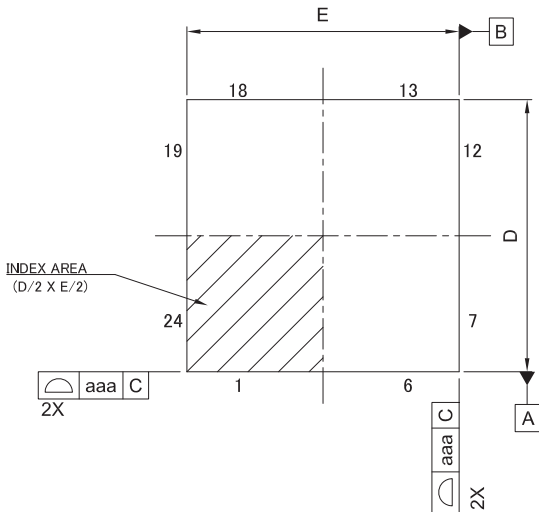
NOTE

1. Dimensions "※1" and "※2" do not include mold flash.
2. Dimension "※3" does not include tim offset.

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### 3.3 24-pin Products

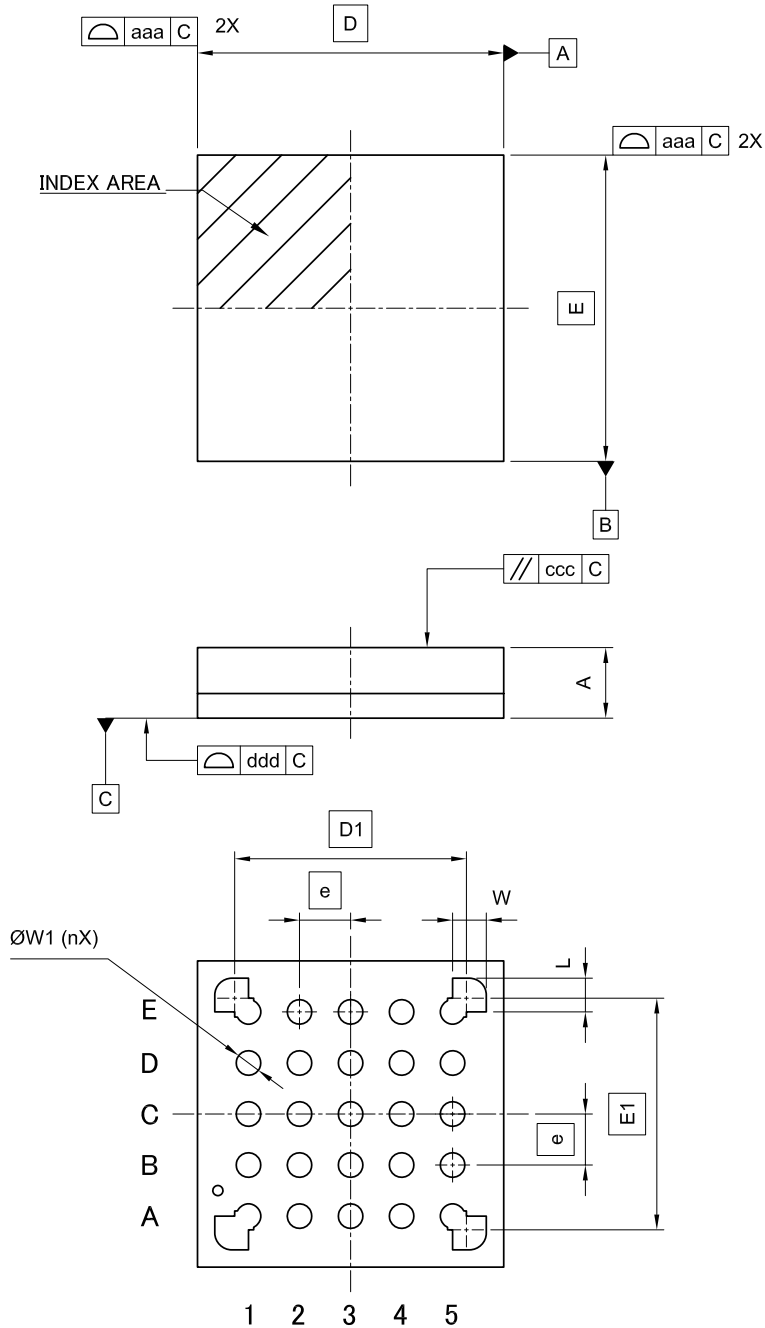
|                    |              |                 |
|--------------------|--------------|-----------------|
| JEITA Package Code | RENESAS Code | MASS (TYP.) [g] |
| P-HWQFN24-4x4-0.50 | PWQN0024KG-A | 0.04            |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 0.80 |
| A <sub>1</sub>   | 0.00                     | 0.02 | 0.05 |
| A <sub>3</sub>   | 0.203 REF.               |      |      |
| b                | 0.18                     | 0.25 | 0.30 |
| D                | 4.00 BSC                 |      |      |
| E                | 4.00 BSC                 |      |      |
| e                | 0.50 BSC                 |      |      |
| L                | 0.35                     | 0.40 | 0.45 |
| K                | 0.20                     | —    | —    |
| D <sub>2</sub>   | 2.65                     | 2.70 | 2.75 |
| E <sub>2</sub>   | 2.65                     | 2.70 | 2.75 |
| aaa              | 0.15                     |      |      |
| bbb              | 0.10                     |      |      |
| ccc              | 0.10                     |      |      |
| ddd              | 0.05                     |      |      |
| eee              | 0.08                     |      |      |
| fff              | 0.10                     |      |      |

3.4 25-pin Products

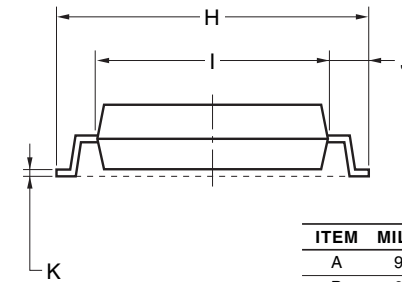
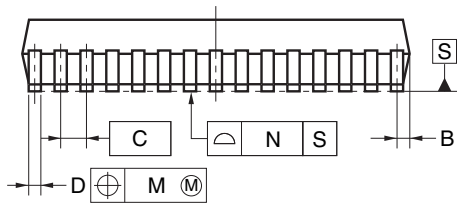
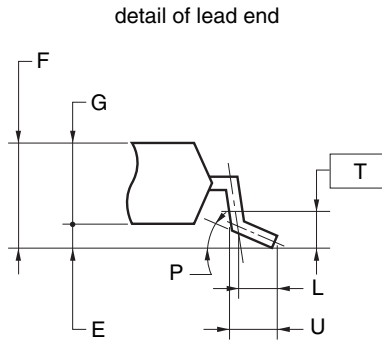
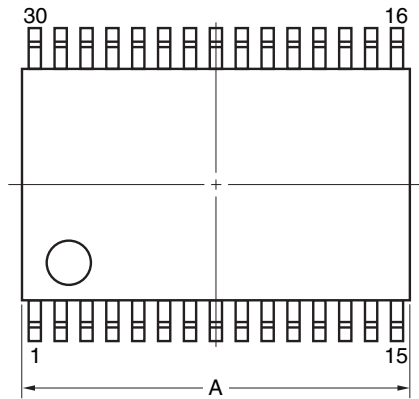
|                    |              |               |
|--------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-WLGA25-3x3-0.50  | PWLG0025KB-A | 0.01          |



| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min.                     | Nom.  | Max. |
| $D$              | —                        | 3.00  | —    |
| $E$              | —                        | 3.00  | —    |
| $D1$             | 2.27                     |       |      |
| $E1$             | 2.27                     |       |      |
| A                | —                        | —     | 0.76 |
| W1               | 0.19                     | 0.24  | 0.29 |
| W                | —                        | 0.330 | —    |
| L                | —                        | 0.330 | —    |
| $e$              | 0.50                     |       |      |
| aaa              | —                        | —     | 0.10 |
| ccc              | —                        | —     | 0.20 |
| ddd              | —                        | —     | 0.08 |
| n                | —                        | 25    | —    |

3.5 30-pin Products

|                     |              |                |                 |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code  | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LSSOP30-0300-0.65 | PLSP0030JB-B | S30MC-65-5A4-3 | 0.18            |



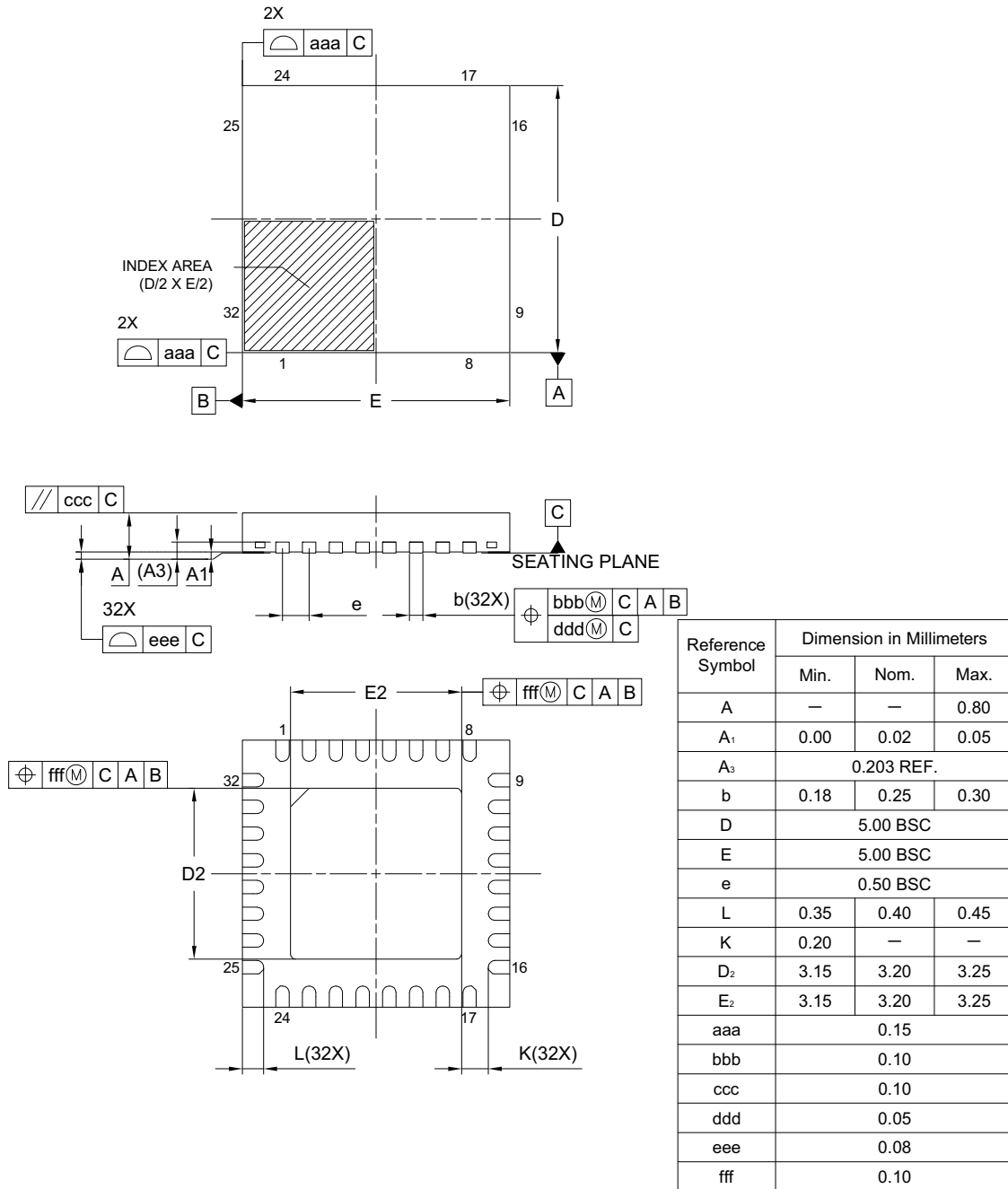
**NOTE**  
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS                            |
|------|--|
| A    | 9.85±0.15                              |
| B    | 0.45 MAX.                              |
| C    | 0.65 (T.P.)                            |
| D    | 0.24 <sup>+0.08</sup> <sub>-0.07</sub> |
| E    | 0.1±0.05                               |
| F    | 1.3±0.1                                |
| G    | 1.2                                    |
| H    | 8.1±0.2                                |
| I    | 6.1±0.2                                |
| J    | 1.0±0.2                                |
| K    | 0.17±0.03                              |
| L    | 0.5                                    |
| M    | 0.13                                   |
| N    | 0.10                                   |
| P    | 3° <sup>+5°</sup> <sub>-3°</sub>       |
| T    | 0.25                                   |
| U    | 0.6±0.15                               |

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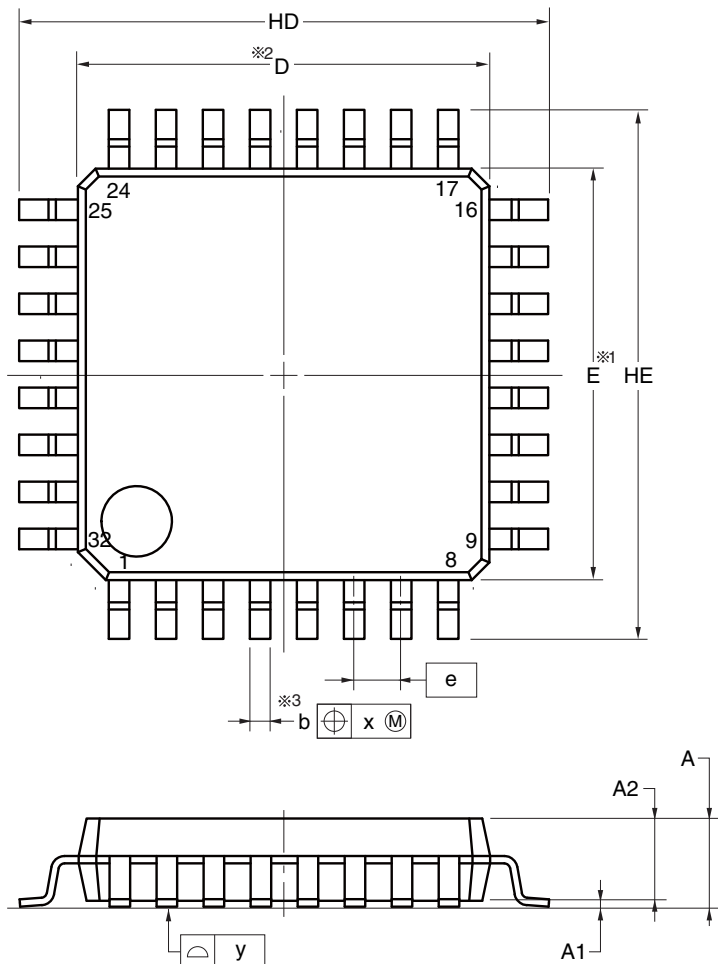
3.6 32-pin Products

|                     |              |                 |
|---------------------|--------------|-----------------|
| JEITA Package code  | RENESAS code | MASS (TYP.) [g] |
| P-HWQFN032-5x5-0.50 | PWQN0032KE-A | 0.06            |

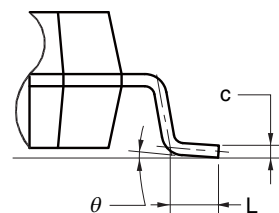




|                    |              |                |                 |
|--------------------|--------------|----------------|-----------------|
| JEITA Package Code | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LQFP32-7x7-0.80  | PLQP0032GB-A | P32GA-80-GBT-1 | 0.2             |



detail of lead end



(UNIT:mm)

| ITEM | DIMENSIONS  |
|------|-------------|
| D    | 7.00±0.10   |
| E    | 7.00±0.10   |
| HD   | 9.00±0.20   |
| HE   | 9.00±0.20   |
| A    | 1.70 MAX.   |
| A1   | 0.10±0.10   |
| A2   | 1.40        |
| b    | 0.37±0.05   |
| c    | 0.145±0.055 |
| L    | 0.50±0.20   |
| θ    | 0° to 8°    |
| e    | 0.80        |
| x    | 0.20        |
| y    | 0.10        |

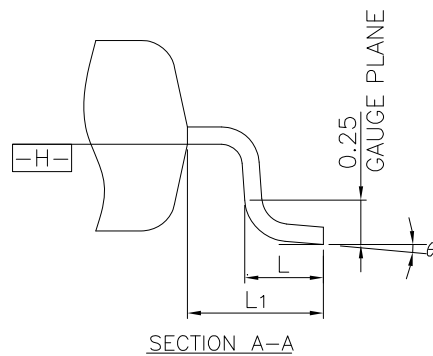
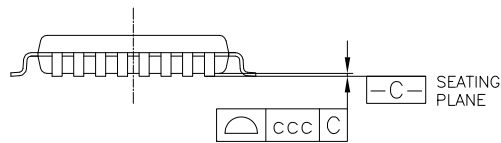
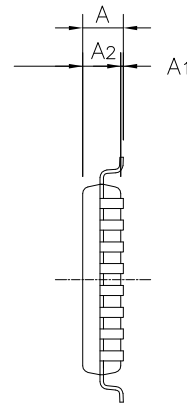
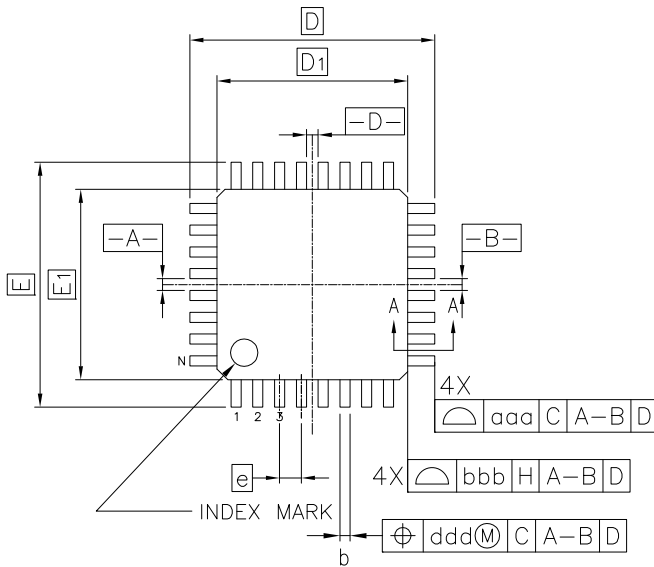
**NOTE**

1. Dimensions “\*1” and “\*2” do not include mold flash.
2. Dimension “\*3” does not include trim offset.

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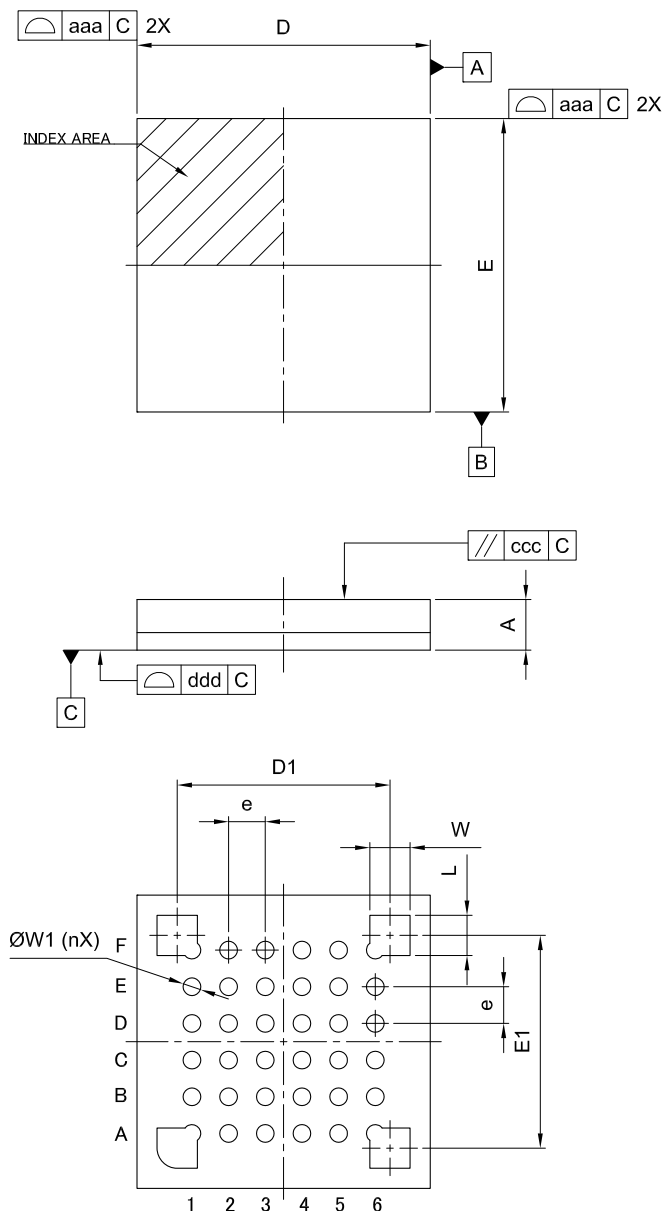
|                    |              |               |
|--------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-LQFP32-7x7-0.80  | PLQP0032GE-A | 0.18          |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 1.60 |
| A <sub>1</sub>   | 0.05                     | —    | 0.15 |
| A <sub>2</sub>   | 1.35                     | 1.40 | 1.45 |
| D                | —                        | 9.00 | —    |
| D <sub>1</sub>   | —                        | 7.00 | —    |
| E                | —                        | 9.00 | —    |
| E <sub>1</sub>   | —                        | 7.00 | —    |
| N                | —                        | 32   | —    |
| e                | —                        | 0.80 | —    |
| b                | 0.30                     | 0.37 | 0.45 |
| c                | 0.09                     | —    | 0.20 |
| θ                | 0°                       | 3.5° | 7°   |
| L                | 0.45                     | 0.60 | 0.75 |
| L <sub>1</sub>   | —                        | 1.00 | —    |
| aaa              | —                        | —    | 0.20 |
| bbb              | —                        | —    | 0.20 |
| ccc              | —                        | —    | 0.10 |
| ddd              | —                        | —    | 0.20 |

3.7 36-pin Products

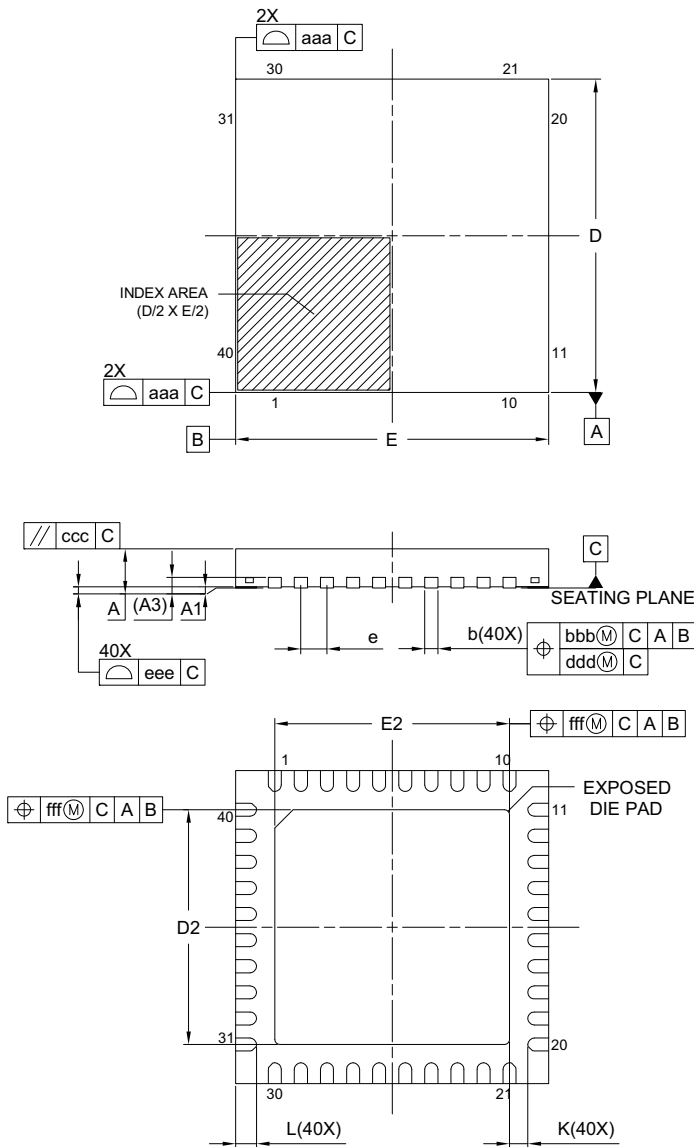
|                      |              |                 |
|----------------------|--------------|-----------------|
| JEITA Package Code   | RENESAS Code | MASS (Typ.) [g] |
| P-WFLGA36-4 × 4-0.50 | PWLG0036KB-A | 0.02            |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| D                | —                        | 4.00 | —    |
| E                | —                        | 4.00 | —    |
| D1               | 2.90 BSC                 |      |      |
| E1               | 2.90 BSC                 |      |      |
| A                | —                        | —    | 0.76 |
| W1               | 0.19                     | 0.24 | 0.29 |
| W                | —                        | 0.55 | —    |
| L                | —                        | 0.55 | —    |
| e                | 0.50 BSC                 |      |      |
| aaa              | 0.10                     |      |      |
| ccc              | 0.20                     |      |      |
| ddd              | 0.08                     |      |      |
| n                | —                        | 36   | —    |

3.8 40-pin Products

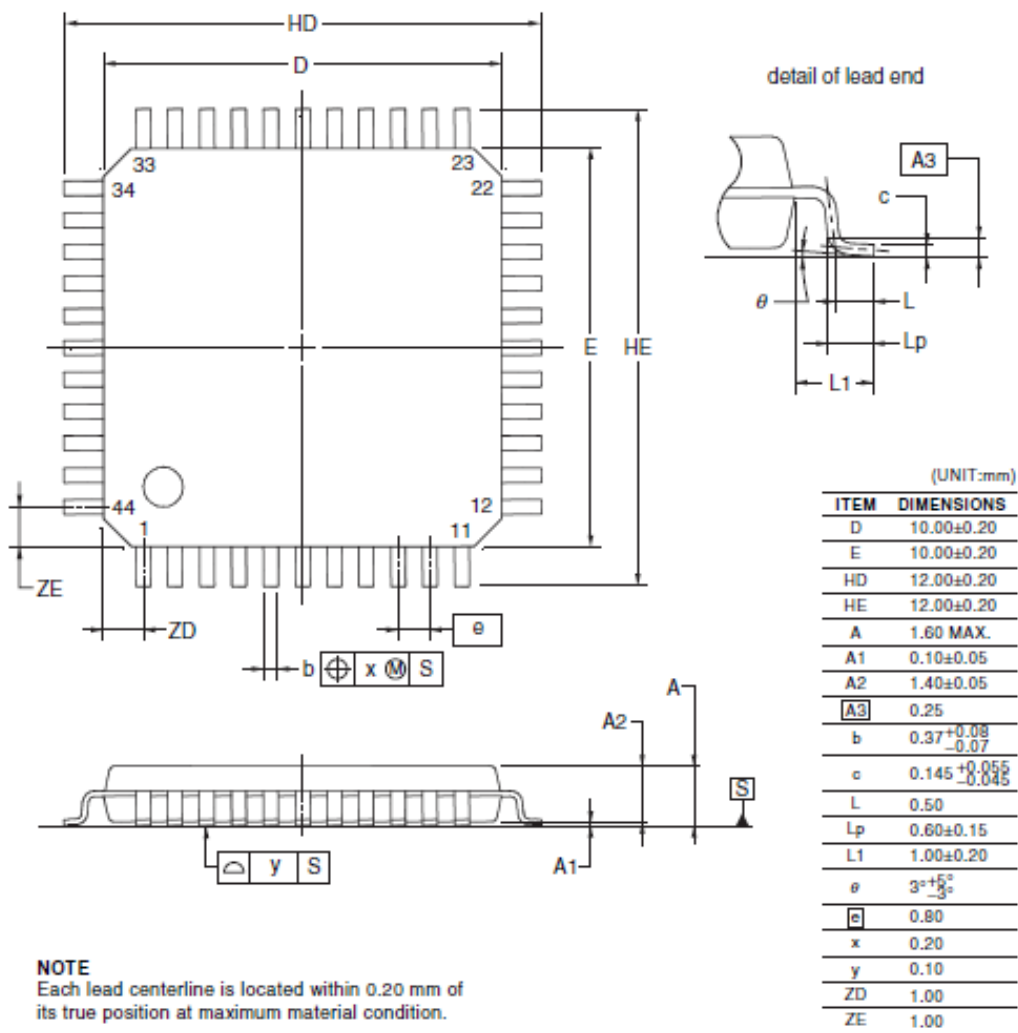
|                     |              |                 |
|---------------------|--------------|-----------------|
| JEITA Package code  | RENESAS code | MASS (TYP.) [g] |
| P-HWQFN040-6x6-0.50 | PWQN0040KD-A | 0.08            |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 0.80 |
| A <sub>1</sub>   | 0.00                     | 0.02 | 0.05 |
| A <sub>3</sub>   | 0.203 REF.               |      |      |
| b                | 0.18                     | 0.25 | 0.30 |
| D                | 6.00 BSC                 |      |      |
| E                | 6.00 BSC                 |      |      |
| e                | 0.50 BSC                 |      |      |
| L                | 0.30                     | 0.40 | 0.50 |
| K                | 0.20                     | —    | —    |
| D <sub>2</sub>   | 4.45                     | 4.50 | 4.55 |
| E <sub>2</sub>   | 4.45                     | 4.50 | 4.55 |
| aaa              | 0.15                     |      |      |
| bbb              | 0.10                     |      |      |
| ccc              | 0.10                     |      |      |
| ddd              | 0.05                     |      |      |
| eee              | 0.08                     |      |      |
| fff              | 0.10                     |      |      |

3.9 44-pin Products

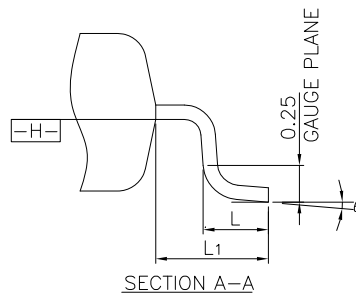
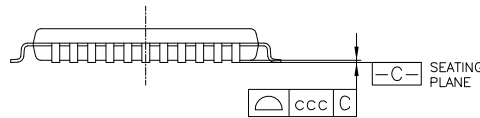
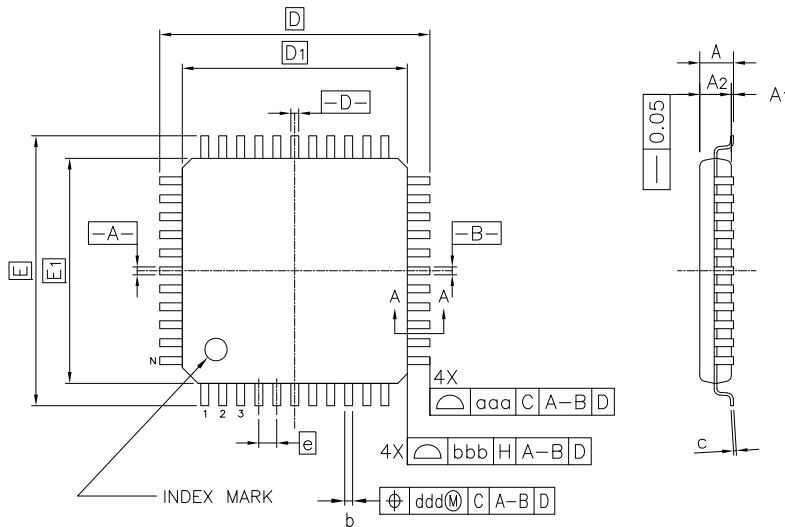
|                     |              |                |                 |
|---------------------|--------------|----------------|-----------------|
| JEITA Package Code  | RENESAS Code | Previous Code  | MASS (TYP.) [g] |
| P-LQFP44-10x10-0.80 | PLQP0044GC-A | P44GB-80-UES-2 | 0.36            |



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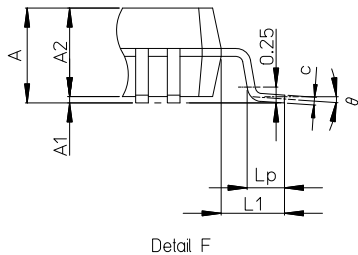
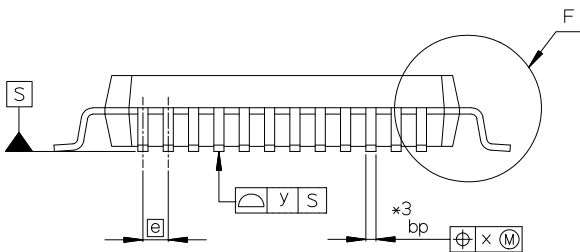
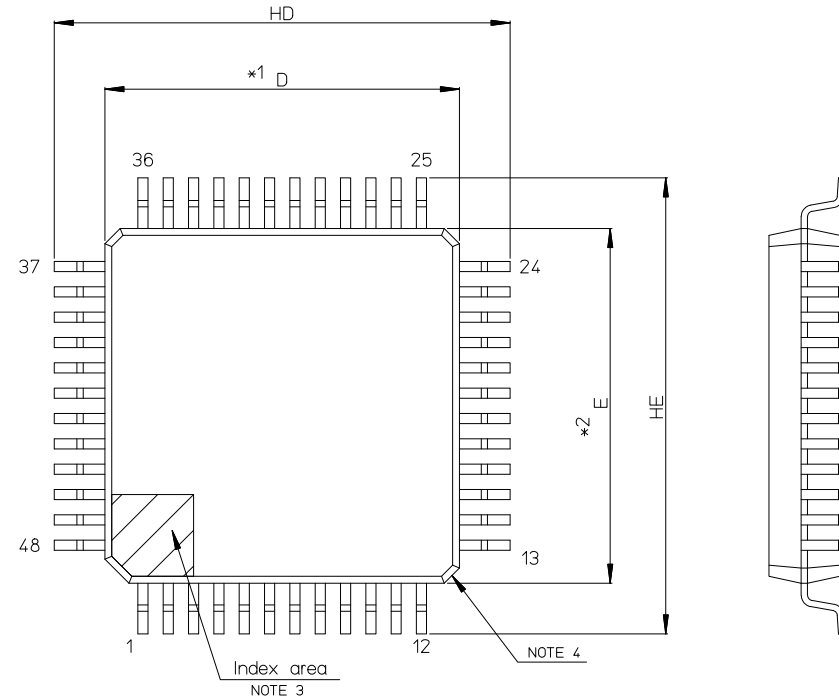
|                      |              |               |
|----------------------|--------------|---------------|
| JEITA Package code   | RENESAS code | MASS(TYP.)[g] |
| P-LQFP044-10x10-0.80 | PLQP0044GE-A | 0.34          |



| Reference Symbol | Dimension in Millimeters |       |      |
|------------------|--------------------------|-------|------|
|                  | Min.                     | Nom.  | Max. |
| A                | —                        | —     | 1.60 |
| A <sub>1</sub>   | 0.05                     | —     | 0.15 |
| A <sub>2</sub>   | 1.35                     | 1.40  | 1.45 |
| D                | —                        | 12.00 | —    |
| D <sub>1</sub>   | —                        | 10.00 | —    |
| E                | —                        | 12.00 | —    |
| E <sub>1</sub>   | —                        | 10.00 | —    |
| N                | —                        | 44    | —    |
| e                | —                        | 0.80  | —    |
| b                | 0.30                     | 0.37  | 0.45 |
| c                | 0.09                     | —     | 0.20 |
| θ                | 0°                       | 3.5°  | 7°   |
| L                | 0.45                     | 0.60  | 0.75 |
| L <sub>1</sub>   | —                        | 1.00  | —    |
| aaa              | —                        | —     | 0.20 |
| bbb              | —                        | —     | 0.20 |
| ccc              | —                        | —     | 0.10 |
| ddd              | —                        | —     | 0.20 |

3.10 48-pin Products

|                    |               |               |            |
|--------------------|---------------|---------------|------------|
| JEITA Package Code | RENESAS Code  | Previous Code | MASS[Typ.] |
| P-LFQFP48-7x7-0.50 | PLQFP0048KB-B | —             | 0.2g       |

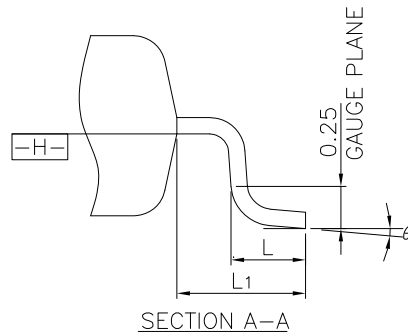
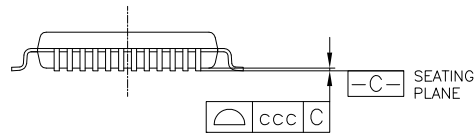
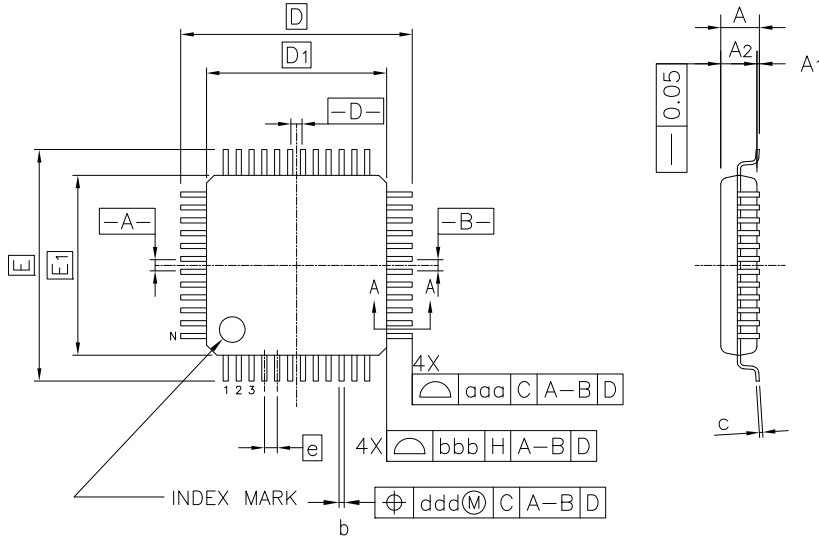


- NOTE)
1. DIMENSIONS \*1\* AND \*2\* DO NOT INCLUDE MOLD FLASH.
  2. DIMENSION \*3\* DOES NOT INCLUDE TRIM OFFSET.
  3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
  4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min                      | Nom  | Max  |
| D                | 6.9                      | 7.0  | 7.1  |
| E                | 6.9                      | 7.0  | 7.1  |
| A2               | —                        | 1.4  | —    |
| HD               | 8.8                      | 9.0  | 9.2  |
| HE               | 8.8                      | 9.0  | 9.2  |
| A                | —                        | —    | 1.7  |
| A1               | 0.05                     | —    | 0.15 |
| bp               | 0.17                     | 0.20 | 0.27 |
| c                | 0.09                     | —    | 0.20 |
| θ                | 0°                       | 3.5° | 8°   |
| e                | —                        | 0.5  | —    |
| x                | —                        | —    | 0.08 |
| y                | —                        | —    | 0.08 |
| Lp               | 0.45                     | 0.6  | 0.75 |
| L1               | —                        | 1.0  | —    |

<R>

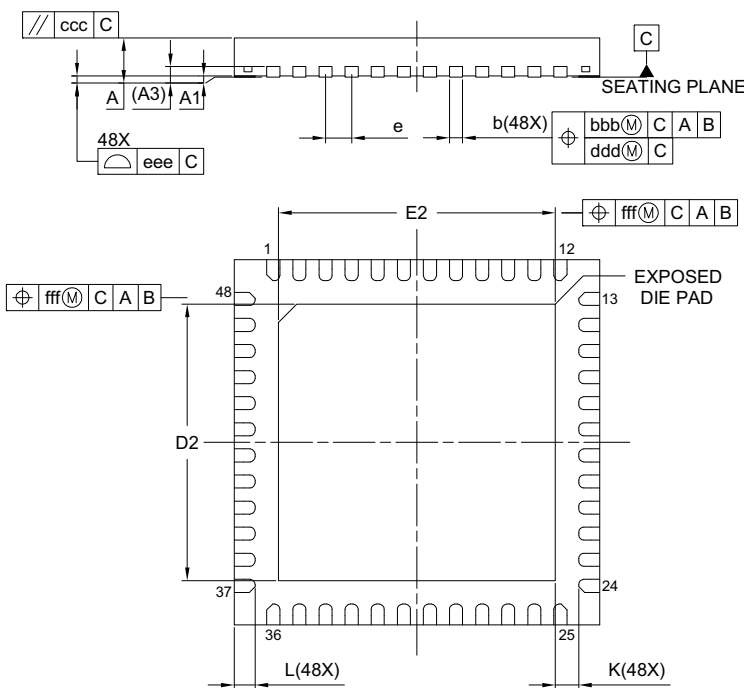
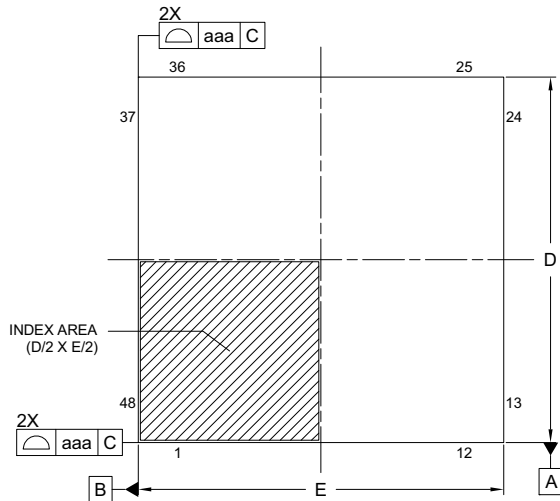
|                    |              |               |
|--------------------|--------------|---------------|
| JEITA Package code | RENESAS code | MASS(TYP.)[g] |
| P-LFQFP48-7x7-0.50 | PLQP0048KL-A | 0.18          |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 1.60 |
| A <sub>1</sub>   | 0.05                     | —    | 0.15 |
| A <sub>2</sub>   | 1.35                     | 1.40 | 1.45 |
| D                | —                        | 9.00 | —    |
| D <sub>1</sub>   | —                        | 7.00 | —    |
| E                | —                        | 9.00 | —    |
| E <sub>1</sub>   | —                        | 7.00 | —    |
| N                | —                        | 48   | —    |
| e                | —                        | 0.50 | —    |
| b                | 0.17                     | 0.22 | 0.27 |
| c                | 0.09                     | —    | 0.20 |
| θ                | 0°                       | 3.5° | 7°   |
| L                | 0.45                     | 0.60 | 0.75 |
| L <sub>1</sub>   | —                        | 1.00 | —    |
| aaa              | —                        | —    | 0.20 |
| bbb              | —                        | —    | 0.20 |
| ccc              | —                        | —    | 0.08 |
| ddd              | —                        | —    | 0.08 |



|                     |              |                 |
|---------------------|--------------|-----------------|
| JEITA Package code  | RENESAS code | MASS (TYP.) [g] |
| P-HWQFN048-7x7-0.50 | PWQN0048KC-A | 0.13 g          |



| Reference Symbol | Dimension in Millimeters |      |      |
|------------------|--------------------------|------|------|
|                  | Min.                     | Nom. | Max. |
| A                | —                        | —    | 0.80 |
| A <sub>1</sub>   | 0.00                     | 0.02 | 0.05 |
| A <sub>3</sub>   | 0.203 REF.               |      |      |
| b                | 0.20                     | 0.25 | 0.30 |
| D                | 7.00 BSC                 |      |      |
| E                | 7.00 BSC                 |      |      |
| e                | 0.50 BSC                 |      |      |
| L                | 0.30                     | 0.40 | 0.50 |
| K                | 0.20                     | —    | —    |
| D <sub>2</sub>   | 5.25                     | 5.30 | 5.35 |
| E <sub>2</sub>   | 5.25                     | 5.30 | 5.35 |
| aaa              | 0.15                     |      |      |
| bbb              | 0.10                     |      |      |
| ccc              | 0.10                     |      |      |
| ddd              | 0.05                     |      |      |
| eee              | 0.08                     |      |      |
| fff              | 0.10                     |      |      |

|                  |                    |
|------------------|--------------------|
| Revision History | RL78/G22 Datasheet |
|------------------|--------------------|

| Rev. | Date         | Description |  |
|------|--------------|-------------|--|
|      |              | Page        | Summary  |
| 1.00 | Dec 28, 2022 | —           | First edition issued   |
| 1.10 | Jun 12, 2024 | p.4         | Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G22 was modified. |
|      |              | p.5         | Table 1 - 1 List of Ordering Part Numbers was modified.                      |
|      |              | p.54        | 2.4 AC Characteristics was modified.   |
|      |              | p.114       | 3.6 32-pin Products: The figure was added.                                   |
|      |              | p.118       | 3.9 44-pin Products: The figure was added.                                   |
|      |              | p.120       | 3.10 48-pin Products: The figure was added.                                  |

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## General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

### 1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity.

Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

### 2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

### 3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

### 4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

### 5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

### 6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).

### 7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

### 8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems.

The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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