

True low-power platform, 41- μ A/MHz operating current, 210-nA data retention current for 4 KB of RAM, up to 768-KB code flash memory and 48-KB RAM, capacitive sensing unit, from 30 to 128 pins, 1.6-5.5 V

1. Outline

1.1 Features

Ultra-low power consumption technology

- VDD = single power supply voltage of 1.6 to 5.5 V
- HALT mode
- STOP mode

High-speed wakeup from the STOP mode is possible.

- SNOOZE mode

RL78 CPU core

- CISC architecture with 3-stage pipeline
- Minimum instruction execution time:
Can be changed from high speed (0.03125 μ s @ 32 MHz operation with the high-speed on-chip oscillator clock) to ultra-low speed (30.5 μ s @ 32.768 kHz operation with the subsystem clock)
- Multiply/divide/multiply & accumulate instructions are supported.
- Address space: 1 MB
- General-purpose registers:
(8-bit register \times 8) \times 4 banks
- On-chip RAM: 12 to 48 KB

Code flash memory

- Code flash memory: 96 to 768 KB
- Block size: 2 KB
- Prohibition of block erase and rewriting (security function)
- On-chip debugging
- Self-programming (with boot swapping and flash shield window)

Data flash memory

- Data flash memory: 8 KB
- Background operation (BGO):
Instructions can be executed from the program memory while rewriting the data flash memory.
- Number of rewrites: 1,000,000 times (typ.)

High-speed on-chip oscillator

- Select from 32 MHz, 24 MHz, 16 MHz, 12 MHz, 8 MHz, 6 MHz, 4 MHz, 3 MHz, 2 MHz, or 1 MHz
- High accuracy: $\pm 1.0\%$
(VDD = 1.8 to 5.5 V, TA = -20 to +85°C)

Middle-speed on-chip oscillator

- Select from 4 MHz, 2 MHz, or 1 MHz (with adjustability)

Low-speed on-chip oscillator

- 32.768 kHz (typ.) (with adjustability)

Operating ambient temperature

- TA = -40 to +85°C (2D: Consumer applications)
- TA = -40 to +105°C (3C: Industrial applications)

Power management and reset function

- On-chip power-on-reset (POR) circuit
- On-chip voltage detectors (LVD0 and LVD1)

Data transfer controller (DTC)

- Transfer modes:
Normal transfer mode, repeat transfer mode, block transfer mode
- Activation sources: Activated by interrupt sources.
- Chain transfer function

SNOOZE mode sequencer (SMS)

- Calculations and comparison of values by the commands for use in processing by the sequencer can realize intermittent operations where the RL78/G23 does not have to return to normal operation.
- Sequentially handling a total of 32 processes with the use of desired commands from among 21 different ones
- The SNOOZE mode sequencer offers operation with low power consumption without using the CPU, flash memory, and RAM.

Logic and event link controller (ELCL)

- Event signals can be set up between specified peripheral functions.
- The signals can be generated by the input of multiple event signals to the logic circuit.
- Flip-flop circuits are incorporated to handle setting and resetting functions.

Serial interface

- Simplified SPI (CSI^{Note 1}): 3 to 8 channels
- UART/UART (LIN-bus supported)/UARTA: 3 to 6 channels
- I²C/Simplified I²C: 4 to 10 channels

Remote control signal receiver

- 1 channel
- Matching of 4 waveform patterns (header, data 0, data 1, and special data)

Timers

- 16-bit timer: 8 to 16 channels
- 32-bit interval timer:
 - 1 channel in 32-bit counter mode
 - 2 channels in 16-bit counter mode
 - 4 channels in 8-bit counter mode
- Realtime clock: 1 channel (counting of one second to 99 years, alarm interrupt, and clock correction)
- Watchdog timer: 1 channel (operates with the dedicated low-speed on-chip oscillator clock)

A/D converter

- 8-/10-/12-bit resolution A/D converter
- Analog input: 8 to 26 channels
- Internal reference voltage (1.48 V) and temperature sensor

D/A converter

- 8-bit resolution D/A converter
- Analog output: 2 channels
- Output voltage: 0 V to V_{DD}
- Realtime output function

Comparator

- 2 channels
- Operating modes:
 - Comparator high-speed mode and comparator low-speed mode
- The external reference voltage and the internal reference voltage or D/A converter output are selectable as the reference voltage.

Capacitive sensing unit

- CTSU2L operating voltage condition: V_{DD} = 1.8 to 5.5 V
- Self-capacitance method:
 - A single pin configures a single key, supporting up to 32 keys
- Mutual capacitance method:
 - Matrix configuration with 8 × 8 pins, supporting up to 64 keys

Input/output port pins

- Number of port pins: 26 to 120
 - (N-ch open drain I/O [withstand voltage of 6 V]: 2 to 4, N-ch open drain I/O [V_{DD} withstand voltage ^{Note 2}/EV_{DD} withstand voltage^{Note 3}]: 10 to 33, output current control pins: 6 to 8)
- Can be set to N-ch open drain or TTL input buffer, and use of an on-chip pull-up resistor can be specified.
- Connectable to a device with different voltage (1.8, 2.5, or 3 V)

Others

- Key interrupt input
- Clock output/buzzer output controller
- BCD (binary-coded decimal) correction circuit

Note 1. Although the CSI function is generally called SPI, it is also called CSI in this product, so it is referred to as such in this manual.

Note 2. This applies to the 30- to 52-pin products.

Note 3. This applies to the 64- to 128-pin products.

Remark The functions mounted depend on the product. See **1.6 Outline of Functions**.

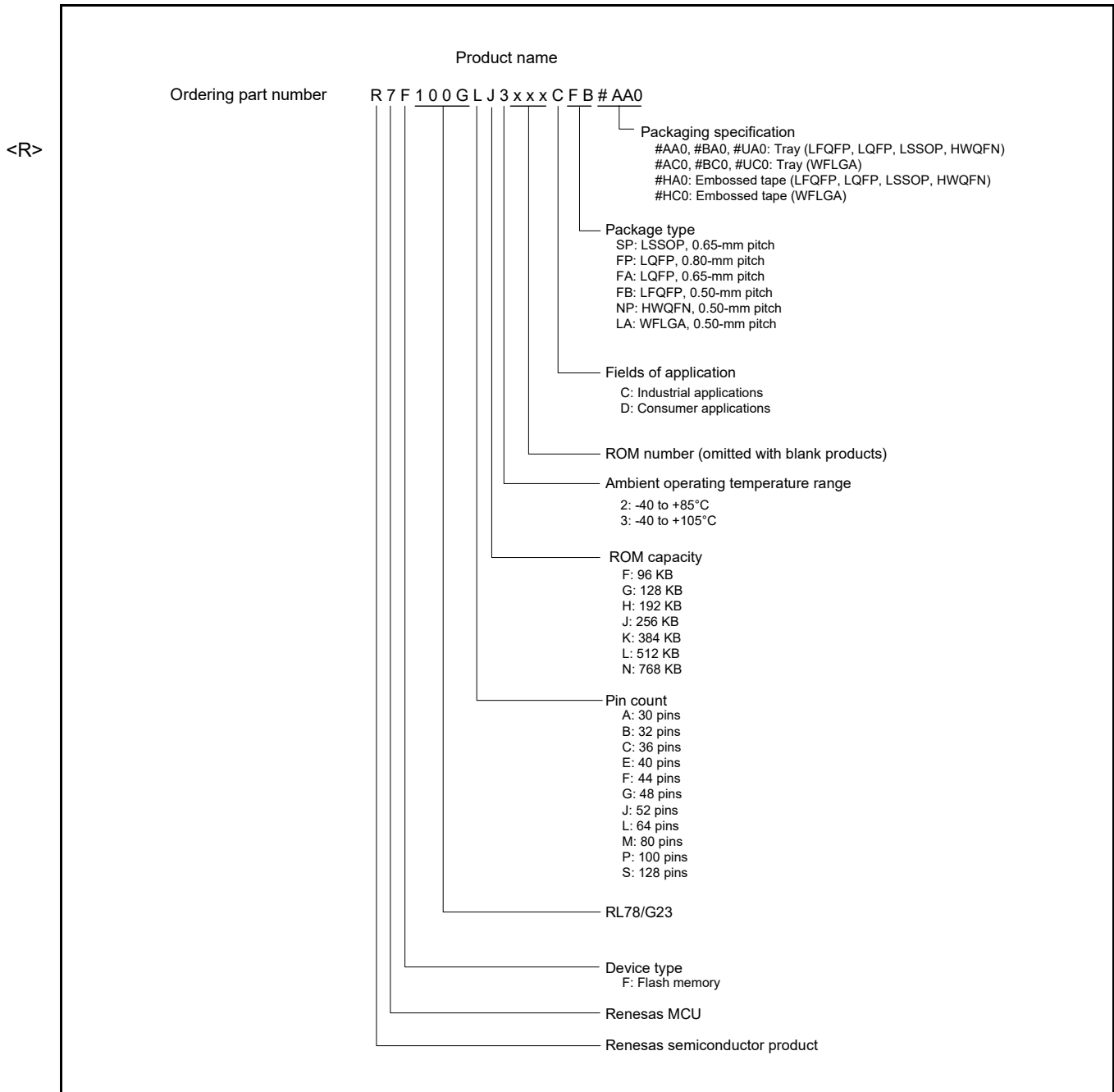
O ROM, RAM capacities

Flash ROM	Data flash	RAM	RL78/G23					
			30 pins	32 pins	36 pins	40 pins	44 pins	48 pins
768 KB	8 KB	48 KB	—	—	—	—	R7F100GFN	R7F100GGN
512 KB	8 KB	48 KB	—	—	—	—	R7F100GFL	R7F100GGL
384 KB	8 KB	32 KB	—	—	—	—	R7F100GFK	R7F100GGK
256 KB	8 KB	24 KB	R7F100GAJ	R7F100GBJ	R7F100GCJ	R7F100GEJ	R7F100GFJ	R7F100GGJ
192 KB	8 KB	20 KB	R7F100GAH	R7F100GBH	R7F100GCH	R7F100GEH	R7F100GFH	R7F100GGH
128 KB	8 KB	16 KB	R7F100GAG	R7F100GBG	R7F100GCG	R7F100GEG	R7F100GFG	R7F100GGG
96 KB	8 KB	12 KB	R7F100GAF	R7F100GBF	R7F100GCF	R7F100GEF	R7F100GFF	R7F100GGF

Flash ROM	Data flash	RAM	RL78/G23				
			52 pins	64 pins	80 pins	100 pins	128 pins
768 KB	8 KB	48 KB	R7F100GJN	R7F100GLN	R7F100GMN	R7F100GPN	R7F100GSN
512 KB	8 KB	48 KB	R7F100GJL	R7F100GLL	R7F100GML	R7F100GPL	R7F100GSL
384 KB	8 KB	32 KB	R7F100GJK	R7F100GLK	R7F100GMK	R7F100GPK	R7F100GSK
256 KB	8 KB	24 KB	R7F100GJJ	R7F100GLJ	R7F100GMJ	R7F100GPJ	R7F100GSJ
192 KB	8 KB	20 KB	R7F100GJH	R7F100GLH	R7F100GMH	R7F100GPH	—
128 KB	8 KB	16 KB	R7F100GJG	R7F100GLG	R7F100GMG	R7F100GPG	—
96 KB	8 KB	12 KB	R7F100GJF	R7F100GLF	—	—	—

1.2 List of Part Numbers

Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23



<R> Table 1 - 1 List of Ordering Part Numbers (1/3)

Pin count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
30	30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)	C	R7F100GAF3CSP, R7F100GAG3CSP, R7F100GAH3CSP, R7F100GAJ3CSP	#AA0, #BA0, #UA0, #HA0	PLSP0030JB-B
		D	R7F100GAF2DSP, R7F100GAG2DSP, R7F100GAH2DSP, R7F100GAJ2DSP		
32	32-pin plastic HWQFN (5 × 5 mm, 0.5-mm pitch)	C	R7F100GBF3CNP, R7F100GBG3CNP, R7F100GBH3CNP, R7F100GBJ3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0032KE-A
		D	R7F100GBF2DNP, R7F100GBG2DNP, R7F100GBH2DNP, R7F100GBJ2DNP		
	32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)	C	R7F100GBF3CFP, R7F100GBG3CFP, R7F100GBH3CFP, R7F100GBJ3CFP	#AA0, #BA0, #UA0, #HA0	PLQP0032GB-A, PLQP0032GE-A
		D	R7F100GBF2DFP, R7F100GBG2DFP, R7F100GBH2DFP, R7F100GBJ2DFP		
36	36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)	C	R7F100GCF3CLA, R7F100GCG3CLA, R7F100GCH3CLA, R7F100GCJ3CLA	#AC0, #BC0, #UC0, #HC0	PWL0036KB-A
		D	R7F100GCF2DLA, R7F100GCG2DLA, R7F100GCH2DLA, R7F100GCJ2DLA		
40	40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)	C	R7F100GEF3CNP, R7F100GEG3CNP, R7F100GEH3CNP, R7F100GEJ3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0040KD-A
		D	R7F100GEF2DNP, R7F100GEG2DNP, R7F100GEH2DNP, R7F100GEJ2DNP		
44	44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)	C	R7F100GFF3CFP, R7F100GFG3CFP, R7F100GFH3CFP, R7F100GFJ3CFP, R7F100GFK3CFP, R7F100GFL3CFP, R7F100GFN3CFP	#AA0, #BA0, #UA0, #HA0	PLQP0044GC-A, PLQP0044GE-A
		D	R7F100GFF2DFP, R7F100GFG2DFP, R7F100GFH2DFP, R7F100GFJ2DFP, R7F100GFK2DFP, R7F100GFL2DFP, R7F100GFN2DFP		
48	48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)	C	R7F100GGF3CFB, R7F100GGG3CFB, R7F100GGH3CFB, R7F100GGJ3CFB, R7F100GGK3CFB, R7F100GGL3CFB, R7F100GGN3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0048KB-B, PLQP0048KL-A
		D	R7F100GGF2DFB, R7F100GGG2DFB, R7F100GGH2DFB, R7F100GGJ2DFB, R7F100GGK2DFB, R7F100GGL2DFB, R7F100GGN2DFB		
	48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)	C	R7F100GGF3CNP, R7F100GGG3CNP, R7F100GGH3CNP, R7F100GGJ3CNP, R7F100GGK3CNP, R7F100GGL3CNP, R7F100GGN3CNP	#AA0, #BA0, #UA0, #HA0	PWQN0048KC-A
		D	R7F100GGF2DNP, R7F100GGG2DNP, R7F100GGH2DNP, R7F100GGJ2DNP, R7F100GGK2DNP, R7F100GGL2DNP, R7F100GGN2DNP		

<R> Table 1 - 1 List of Ordering Part Numbers (2/3)

Pin count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
52	52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)	C	R7F100GJF3CFA, R7F100GJG3CFA, R7F100GJH3CFA, R7F100GJJ3CFA, R7F100GJK3CFA, R7F100GJL3CFA, R7F100GJN3CFA	#AA0, #BA0, #UA0, #HA0	PLQP0052JA-A
		D	R7F100GJF2DFA, R7F100GJG2DFA, R7F100GJH2DFA, R7F100GJJ2DFA, R7F100GJK2DFA, R7F100GJL2DFA, R7F100GJN2DFA		
64	64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)	C	R7F100GLF3CFA, R7F100GLG3CFA, R7F100GLH3CFA, R7F100GLJ3CFA, R7F100GLK3CFA, R7F100GLL3CFA, R7F100GLN3CFA	#AA0, #BA0, #UA0, #HA0	PLQP0064JA-A
		D	R7F100GLF2DFA, R7F100GLG2DFA, R7F100GLH2DFA, R7F100GLJ2DFA, R7F100GLK2DFA, R7F100GLL2DFA, R7F100GLN2DFA		
	64-pin plastic LQFP (10 × 10 mm, 0.50-mm pitch)	C	R7F100GLF3CFB, R7F100GLG3CFB, R7F100GLH3CFB, R7F100GLJ3CFB, R7F100GLK3CFB, R7F100GLL3CFB, R7F100GLN3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0064KB-C, PLQP0064KL-A
		D	R7F100GLF2DFB, R7F100GLG2DFB, R7F100GLH2DFB, R7F100GLJ2DFB, R7F100GLK2DFB, R7F100GLL2DFB, R7F100GLN2DFB		
	64-pin plastic WFLGA (5 × 5 mm, 0.50-mm pitch)	C	R7F100GLF3CLA, R7F100GLG3CLA, R7F100GLH3CLA, R7F100GLJ3CLA, R7F100GLK3CLA, R7F100GLL3CLA, R7F100GLN3CLA	#AC0, #BC0, #UC0, #HC0	PWLG0064KB-A
		D	R7F100GLF2DLA, R7F100GLG2DLA, R7F100GLH2DLA, R7F100GLJ2DLA, R7F100GLK2DLA, R7F100GLL2DLA, R7F100GLN2DLA		
80	80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)	C	R7F100GMG3CFA, R7F100GMH3CFA, R7F100GMJ3CFA, R7F100GMK3CFA, R7F100GML3CFA, R7F100GMN3CFA	#AA0, #BA0, #UA0, #HA0	PLQP0080JA-B
		D	R7F100GMG2DFA, R7F100GMH2DFA, R7F100GMJ2DFA, R7F100GMK2DFA, R7F100GML2DFA, R7F100GMN2DFA		
	80-pin plastic LQFP (12 × 12 mm, 0.50-mm pitch)	C	R7F100GMG3CFB, R7F100GMH3CFB, R7F100GMJ3CFB, R7F100GMK3CFB, R7F100GML3CFB, R7F100GMN3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0080KB-B
		D	R7F100GMG2DFB, R7F100GMH2DFB, R7F100GMJ2DFB, R7F100GMK2DFB, R7F100GML2DFB, R7F100GMN2DFB		

<R> Table 1 - 1 List of Ordering Part Numbers (3/3)

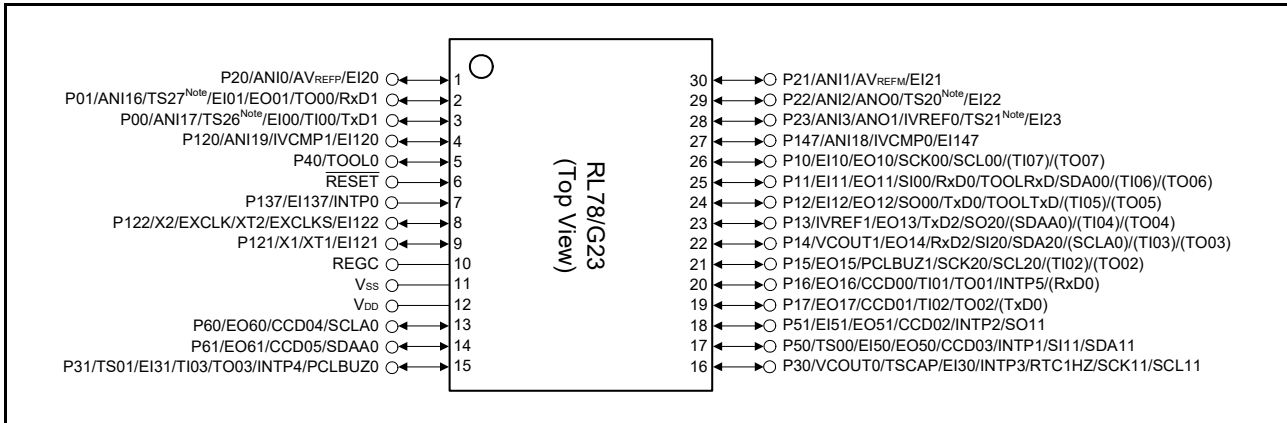
Pin count	Package	Fields of Application Note	Ordering Part Number		Renesas Code
			Product Name	Packaging Specification	
100	100-pin plastic LQFP (14 × 14 mm, 0.50-mm pitch)	C	R7F100GPG3CFB, R7F100GPH3CFB, R7F100GPJ3CFB, R7F100GPK3CFB, R7F100GPL3CFB, R7F100GPN3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0100KB-B
		D	R7F100GPG2DFB, R7F100GPH2DFB, R7F100GPJ2DFB, R7F100GPK2DFB, R7F100GPL2DFB, R7F100GPN2DFB		
	100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)	C	R7F100GPG3CFA, R7F100GPH3CFA, R7F100GPJ3CFA, R7F100GPK3CFA, R7F100GPL3CFA, R7F100GPN3CFA	#AA0, #BA0, #UA0, #HA0	PLQP0100JC-A
		D	R7F100GPG2DFA, R7F100GPH2DFA, R7F100GPJ2DFA, R7F100GPK2DFA, R7F100GPL2DFA, R7F100GPN2DFA		
128	128-pin plastic LQFP (14 × 20 mm, 0.50-mm pitch)	C	R7F100GSJ3CFB, R7F100GSK3CFB, R7F100GSL3CFB, R7F100GSN3CFB	#AA0, #BA0, #UA0, #HA0	PLQP0128KD-A
		D	R7F100GSJ2DFB, R7F100GSK2DFB, R7F100GSL2DFB, R7F100GSN2DFB		

Note For the fields of application, see **Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23**.

1.3 Pin Configuration (Top View)

1.3.1 30-pin products

- 30-pin plastic LSSOP (7.62 mm (300), 0.65-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 2 Multiplexed Pin Functions of the 30-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	30LSSOP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
2	P01	—	EI01/ EO01	—	ANI16	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
3	P00	—	EI00	—	ANI17	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
4	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
5	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
6	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
7	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
8	P122	—	EI122	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
9	P121	—	EI121	X1/XT1	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
13	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
14	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
15	P31	—	EI31	PCLBUZ0	—	—	—	INTP4	—	TS01	TI03/ TO03	—	—	—	—	—
16	P30	—	EI30	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—	—	—
17	P50	CCD03	EI50/ EO50	—	—	—	INTP1	—	TS00	—	—	—	SI11/ SDA11	—	—	—
18	P51	CCD02	EI51/ EO51	—	—	—	INTP2	—	—	—	—	—	SO11	—	—	—
19	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/ TO02	—	(TxD0)	—	—	—
20	P16	CCD00	EO16	—	—	—	INTP5	—	—	—	TI01/ TO01	—	(RxD0)	—	—	—
21	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
22	P14	—	EO14	—	—	VCOUT1	—	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
23	P13	—	EO13	—	—	IVREF1	—	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
24	P12	—	EI12/ EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
25	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
26	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
27	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—

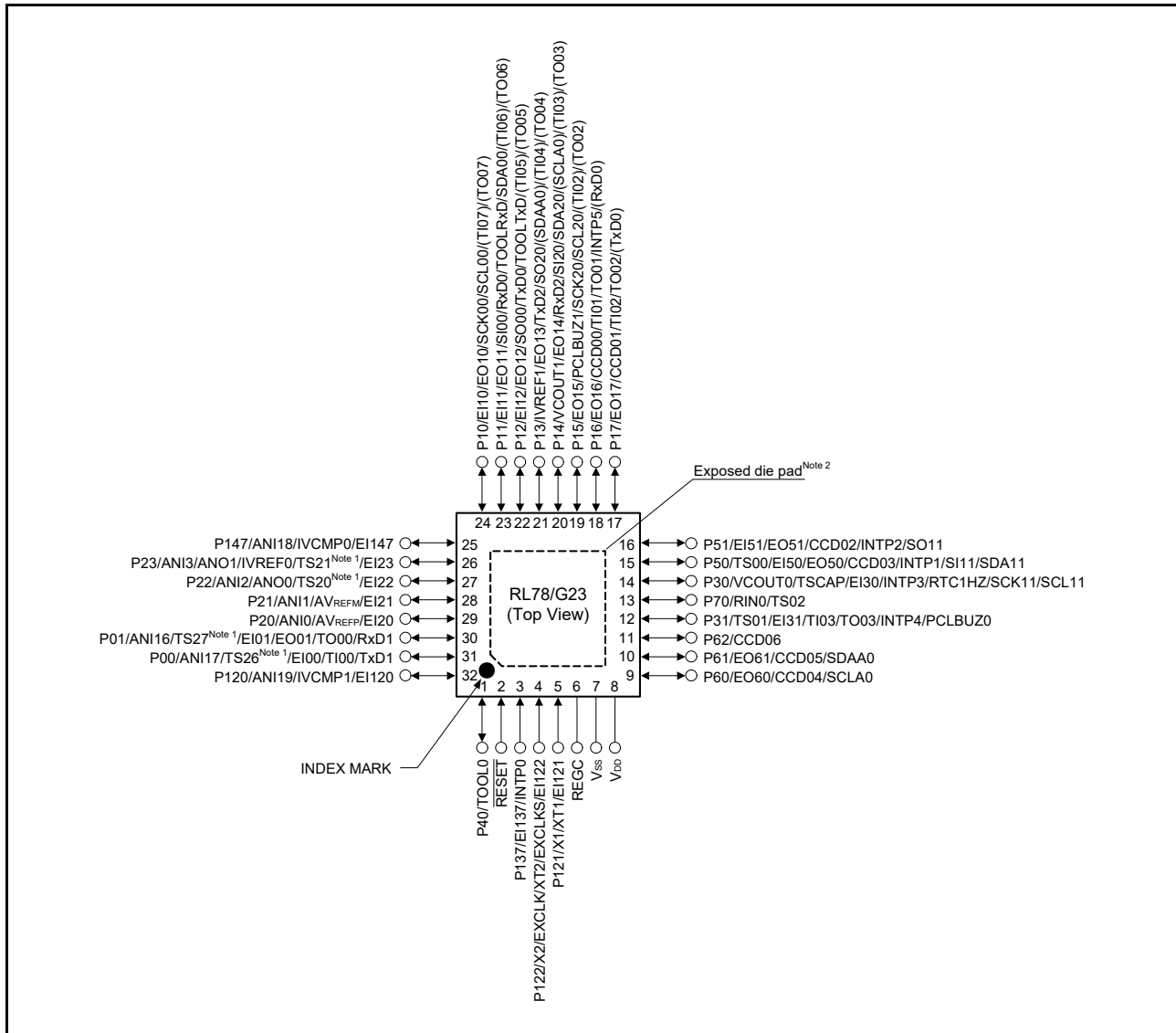
Table 1 - 2 Multiplexed Pin Functions of the 30-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	30LSSOP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
28	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
29	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
30	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.2 32-pin products

- 32-pin plastic HWQFN (5 × 5 mm, 0.50-mm pitch)
- 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch)



Note 1. Not present in products with 128 or fewer Kbytes of code flash memory.

Note 2. The 32-pin plastic LQFP (7 × 7 mm, 0.80-mm pitch) products do not have an exposed die pad.

Caution Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to Vss.

Table 1 - 3 Multiplexed Pin Functions of the 32-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	32HWQFN, 32LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
2	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
3	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
4	P122	—	EI122	X2/XT2/ EXCLK/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
5	P121	—	EI121	X1/XT1	—	—	—	—	—	—	—	—	—	—	—	—
6	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
7	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
8	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
9	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
10	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
11	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	P31	—	EI31	PCLBUZ0	—	—	—	INTP4	—	TS01	TI03/ TO03	—	—	—	—	—
13	P70	—	—	—	—	—	—	—	—	TS02	—	—	—	—	—	RINO
14	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—	—
15	P50	CCD03	EI50/ EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—	—
16	P51	CCD02	EI51/ EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
17	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/ TO02	—	(TxD0)	—	—	—
18	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/ TO01	—	(RxD0)	—	—	—
19	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
20	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
21	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
22	P12	—	EI12/ EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
23	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
24	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
25	P147	—	—	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
26	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
27	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—

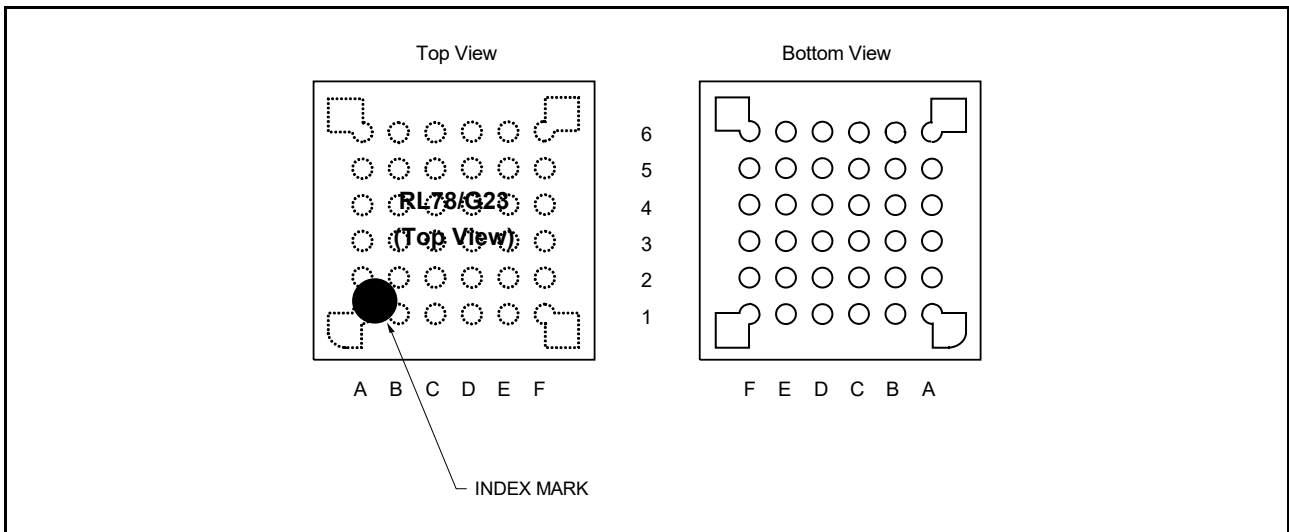
Table 1 - 3 Multiplexed Pin Functions of the 32-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	Digital port	Output current control port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)	Remote control signal receiver (REMIC)
32HWQFN, 32LQFP																
28	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
29	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
30	P01	—	EI01/ EO01	—	ANI16	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
31	P00	—	EI00	—	ANI17	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
32	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.3 36-pin products

- 36-pin plastic WFLGA (4 × 4 mm, 0.50-mm pitch)



	A	B	C	D	E	F
6	P60/EO60/CCD04/ SCLA0	V _{DD}	P121/X1/XT1/EI121	P122/X2/EXCLK/XT2/ EXCLKS/EI122	P137/EI137/INTP0	P40/TOOL0
5	P62/CCD06	P61/EO61/CCD05/ SDAA0	V _{SS}	REGC	$\overline{\text{RESET}}$	P120/ANI19/IVCMP1/ EI120
4	P72/TS04/SO21/ TxDA0	P71/TS03/SI21/ SDA21/RxDA0	P14/VCOUT1/EO14/ RxD2/SI20/SDA20/ (SCLA0)/(TI03)/ (TO03)	P31/TS01/EI31/TI03/ TO03/INTP4/ PCLBUZ0	P00/TS26 ^{Note} /EI00/ TI00/TxD1	P01/TS27 ^{Note} /EI01/ EO01/TO00/RxD1
3	P50/TS00/EI50/EO50/ CCD03/INTP1/SI11/ SDA11	P70/TS02/RIN0/ SCK21/SCL21	P15/EO15/PCLBUZ1/ SCK20/SCL20/ (TI02)/(TO02)	P22/ANI2/ANO0/ TS20 ^{Note} /EI22	P20/ANI0/AVREFP/ EI20	P21/ANI1/AVREFM/ EI21
2	P30/VCOUT0/TSCAP/ EI30/INTP3/RTC1HZ/ SCK11/SCL11	P16/EO16/CCD00/ TI01/TO01/INTP5/ (RxD0)	P12/EI12/EO12/SO00/ TxD0/TOOLTxD/ (TI05)/(TO05)	P11/EI11/EO11/SI00/ RxD0/TOOLRxD/ SDA00/(TI06)/(TO06)	P24/ANI4/TS22 ^{Note}	P23/ANI3/ANO1/ IVREF0/TS21 ^{Note} / EI23
1	P51/EI51/EO51/ CCD02/INTP2/ SO11	P17/EO17/CCD01/ TI02/TO02(TxD0)	P13/IVREF1/EO13/ TxD2/SO20/(SDAA0)/ (TI04)/(TO04)	P10/EI10/EO10/ SCK00/SCL00/ (TI07)/(TO07)	P147/ANI18/IVCMP0/ EI147	P25/ANI5/TS23 ^{Note}

Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 4 Multiplexed Pin Functions of the 36-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	36WFLGA	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTS2UL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
A1	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
A2	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
A3	P50	CCD03	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
A4	P72	—	—	—	—	—	—	—	—	TS04	—	—	SO21	—	TxDA0	—
A5	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	—	—	—
A6	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
B1	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(TxD0)	—	—	—
B2	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(RxD0)	—	—	—
B3	P70	—	—	—	—	—	—	—	—	TS02	—	—	SCK21/SCL21	—	—	RIN0
B4	P71	—	—	—	—	—	—	—	—	TS03	—	—	SI21/SDA21	—	RxDA0	—
B5	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
B6	—	—	—	V _{DD}	—	—	—	—	—	—	—	—	—	—	—	—
C1	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/TO04	—	SO20/TxD2	(SDAA0)	—	—
C2	P12	—	EI12/EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/TO05	—	SO00/TxD0	—	—	—
C3	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/TO02	—	SCK20/SCL20	—	—	—
C4	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/TO03	—	SI20/RxD2/SDA20	(SCLA0)	—	—
C5	—	—	—	V _{SS}	—	—	—	—	—	—	—	—	—	—	—	—
C6	P121	—	EI121	X1/XT1	—	—	—	—	—	—	—	—	—	—	—	—
D1	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/TO07	—	SCK00/SCL00	—	—	—
D2	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/TO06	—	SI00/RxD0/SDA00	—	—	—
D3	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
D4	P31	—	EI31	PCLBUZ0	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
D5	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
D6	P122	—	EI122	X2/XT2/EXCLK/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
E1	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
E2	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—

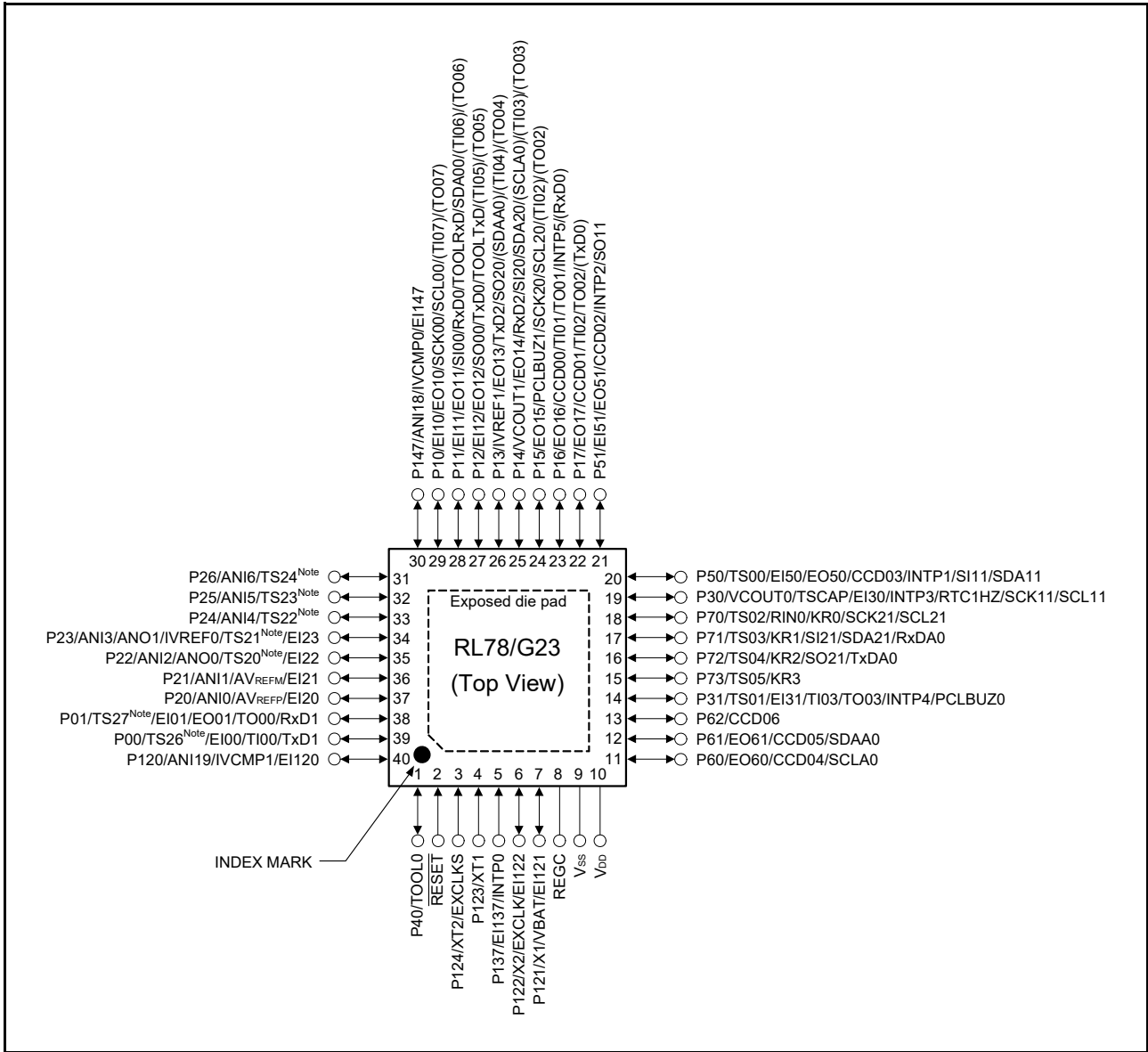
Table 1 - 4 Multiplexed Pin Functions of the 36-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	36WFLGA	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
E3	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
E4	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
E5	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
E6	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
F1	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
F2	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
F3	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
F4	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
F5	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
F6	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.4 40-pin products

- 40-pin plastic HWQFN (6 × 6 mm, 0.50-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Remark 3. It is recommended to connect an exposed die pad to V_{ss}.

Table 1 - 5 Multiplexed Pin Functions of the 40-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	40HWQFN	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
2	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
3	P124	—	—	XT2/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
4	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
5	P137	—	EH137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
6	P122	—	EH122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
7	P121	—	EH121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
8	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
9	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
11	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
12	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
13	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	P31	—	EI31	PCLBUZ0	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
15	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
16	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxD A0	—
17	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxD A0	—
18	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
19	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
20	P50	CCD03	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
21	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
22	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(Tx D0)	—	—	—
23	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(Rx D0)	—	—	—
24	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/TO02	—	SCK20/SCL20	—	—	—
25	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/TO03	—	SI20/xD2/SDA20	(SCLA0)	—	—
26	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/TO04	—	SO20/TxD2	(SDAA0)	—	—
27	P12	—	EH12/EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/TO05	—	SO00/TxD0	—	—	—
28	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/TO06	—	SI00/RxD0/SDA00	—	—	—

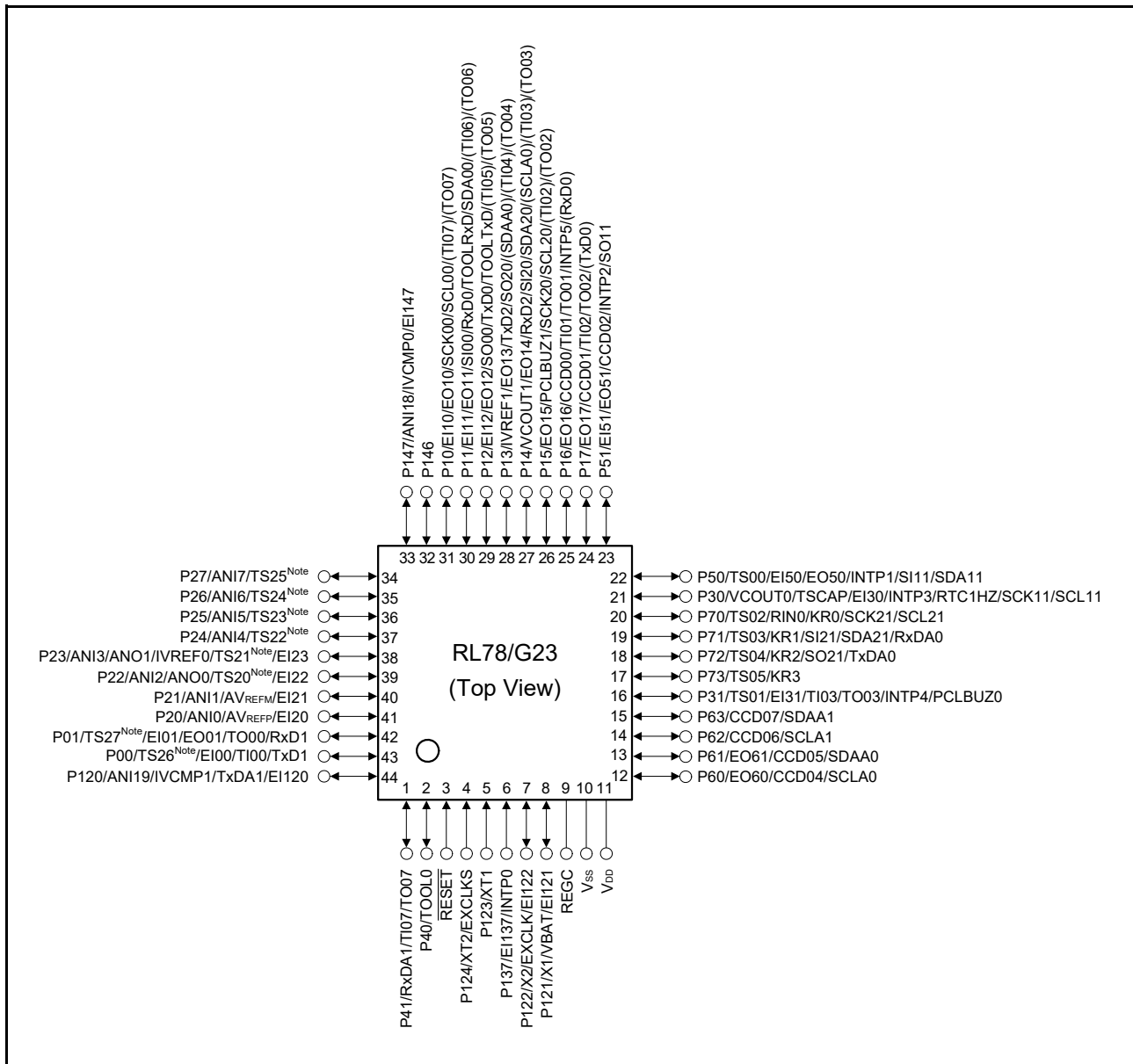
Table 1 - 5 Multiplexed Pin Functions of the 40-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	40HWQFN	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
29	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/(TO07)	—	SCK00/SCL00	—	—	—
30	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
31	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—
32	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
33	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—
34	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
35	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
36	P21	—	EI21	—	ANI1/AVREFM	—	—	—	—	—	—	—	—	—	—	—
37	P20	—	EI20	—	ANI0/AVREFP	—	—	—	—	—	—	—	—	—	—	—
38	P01	—	EI01/EO01	—	—	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
39	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
40	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.5 44-pin products

- 44-pin plastic LQFP (10 × 10 mm, 0.80-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 6 Multiplexed Pin Functions of the 44-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	44LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P41	—	—	—	—	—	—	—	—	—	TI07/TO07	—	—	—	RxDA1	—
2	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
3	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
4	P124	—	—	XT2/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
5	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
6	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
7	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
8	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
9	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
12	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
13	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
14	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
15	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
16	P31	—	EI31	PCLBUZ0	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
17	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
18	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
19	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxDA0	—
20	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
21	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
22	P50	—	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
23	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
24	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(TxD0)	—	—	—
25	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(RxD0)	—	—	—
26	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/(TO02)	—	SCK20/SCL20	—	—	—
27	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/(TO03)	—	SI20/RxD2/SDA20	(SCLA0)	—	—
28	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/(TO04)	—	SO20/TxD2	(SDAA0)	—	—
29	P12	—	EI12/EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/(TO05)	—	SO00/TxD0	—	—	—

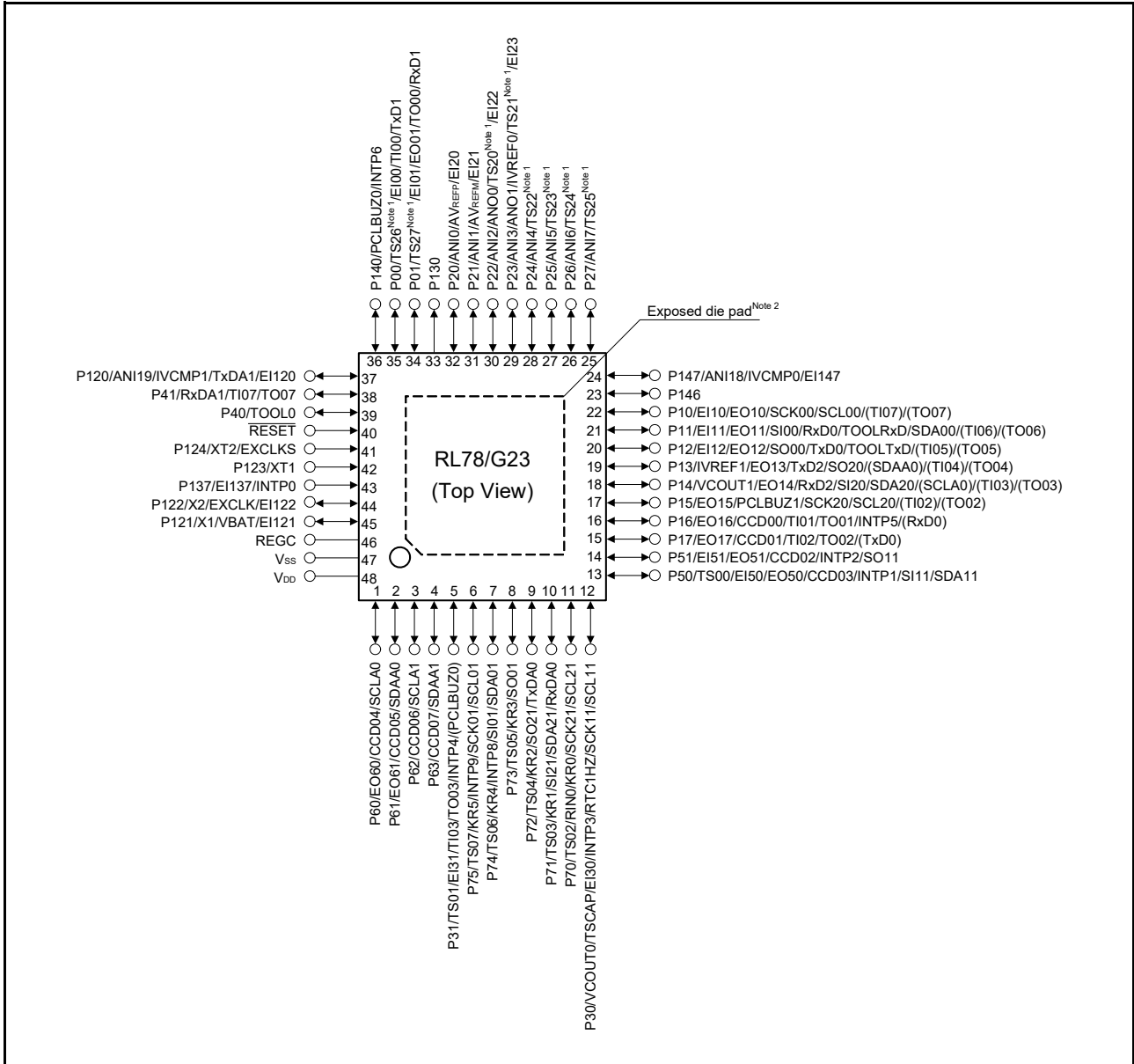
Table 1 - 6 Multiplexed Pin Functions of the 44-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	44LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
30	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
31	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
32	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
33	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
34	P27	—	—	—	ANI7	—	—	—	—	TS25 Note	—	—	—	—	—	—
35	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—
36	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
37	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—
38	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
39	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
40	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
41	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
42	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
43	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
44	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	TxDA1	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.6 48-pin products

- 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch)
- 48-pin plastic HWQFN (7 × 7 mm, 0.50-mm pitch)



- Note 1.** Not present in products with 128 or fewer Kbytes of code flash memory.
- Note 2.** The 48-pin plastic LFQFP (7 × 7 mm, 0.50-mm pitch) products do not have an exposed die pad.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G23 User's Manual.
- Remark 3.** It is recommended to connect an exposed die pad to V_{SS}.

Table 1 - 7 Multiplexed Pin Functions of the 48-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	48LFQFP, 48HWQFN	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
2	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
3	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
4	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
5	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/ TO03	—	—	—	—	—
6	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	SCK01/ SCL01	—	—	—
7	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	SI01/ SDA01	—	—	—
8	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	SO01	—	—	—
9	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
10	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/ SDA21	—	RxDA0	—
11	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/ SCL21	—	—	RIN0
12	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—	—
13	P50	CCD03	EI50/ EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—	—
14	P51	CCD02	EI51/ EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
15	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/ TO02	—	(TxD0)	—	—	—
16	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/ TO01	—	(RxD0)	—	—	—
17	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
18	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
19	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
20	P12	—	EI12/ EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
21	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
22	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
23	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
24	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
25	P27	—	—	—	ANI7	—	—	—	—	TS25 Note	—	—	—	—	—	—
26	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—

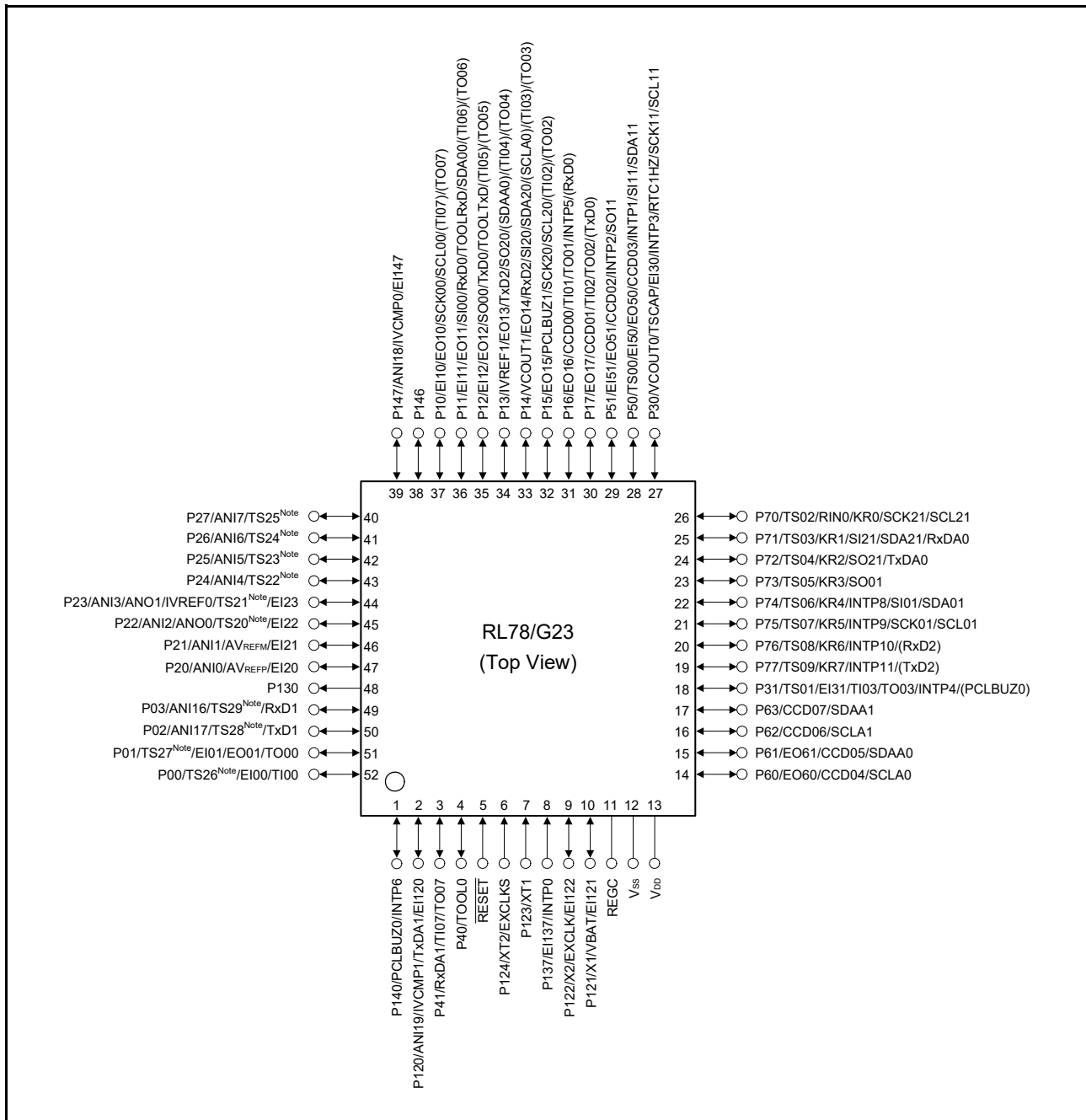
Table 1 - 7 Multiplexed Pin Functions of the 48-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	Digital port	Output current control port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)	Remote control signal receiver (REMIC)
27	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
28	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—
29	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
30	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
31	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
32	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
33	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
34	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	RxD1	—	—	—
35	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	TxD1	—	—	—
36	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
37	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	TxDA1	—
38	P41	—	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	RxDA1	—
39	P40	—	—	TO0L0	—	—	—	—	—	—	—	—	—	—	—	—
40	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
41	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
42	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
43	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
44	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
45	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
46	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
47	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
48	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.7 52-pin products

- 52-pin plastic LQFP (10 × 10 mm, 0.65-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

Caution Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

Remark 1. For pin identification, see 1.4 Pin Identification.

Remark 2. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 8 Multiplexed Pin Functions of the 52-pin Products (1/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	52LFQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
2	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	TxDA1	—
3	P41	—	—	—	—	—	—	—	—	—	TI07/TO07	—	—	—	RxDA1	—
4	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
5	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
6	P124	—	—	XT2/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
7	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
8	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
9	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
10	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
11	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
14	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
15	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
16	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
17	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
18	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
19	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
20	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
21	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	SCK01/SCL01	—	—	—
22	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	SI01/SDA01	—	—	—
23	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	SO01	—	—	—
24	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
25	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxDA0	—
26	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
27	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
28	P50	CCD03	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
29	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
30	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(TxD0)	—	—	—
31	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(RxD0)	—	—	—

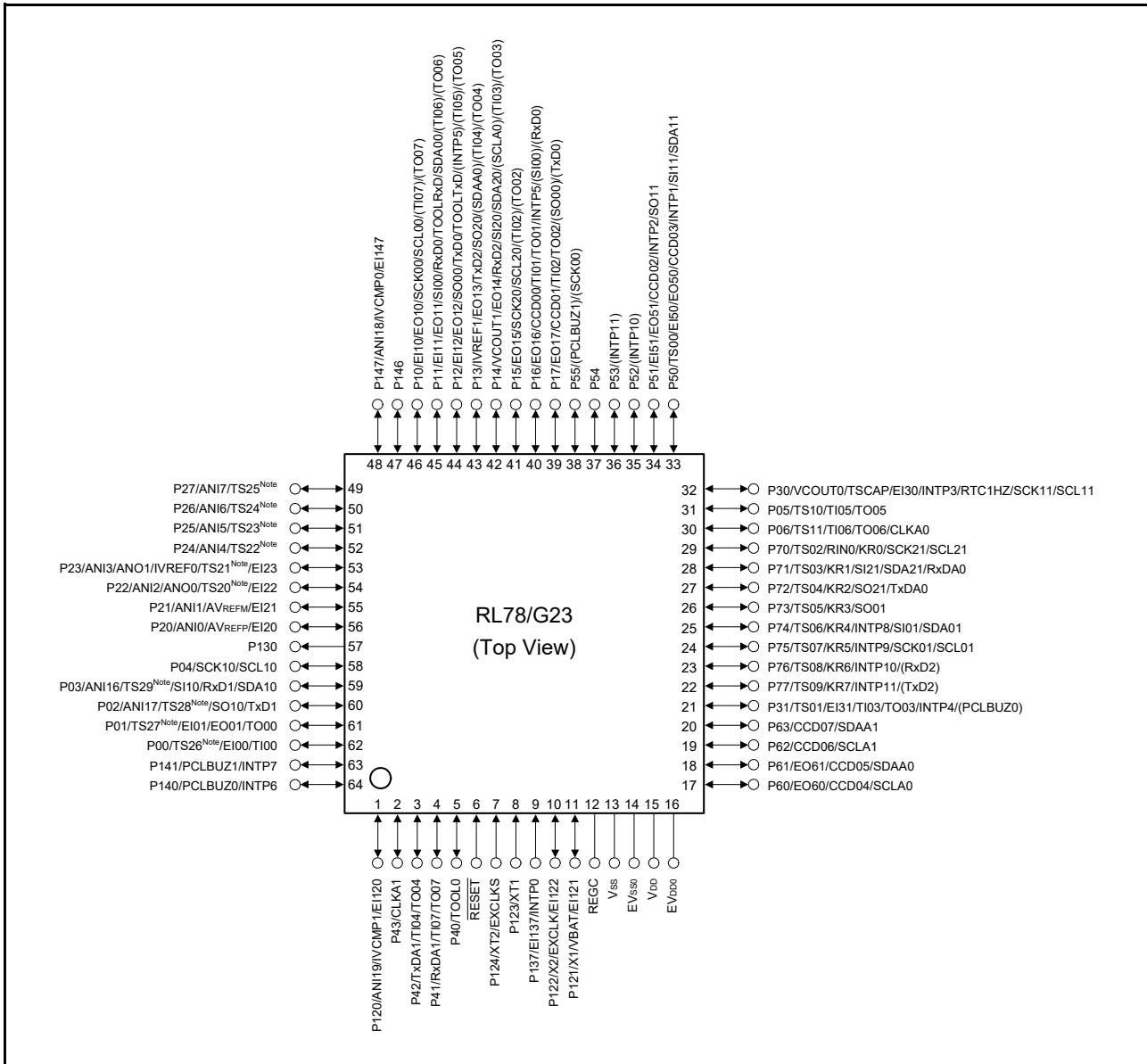
Table 1 - 8 Multiplexed Pin Functions of the 52-pin Products (2/2)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	52LFGFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
32	P15	—	EO15	PCLBUZ1	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
33	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
34	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
35	P12	—	EH12/ EO12	TOOLTxD	—	—	—	—	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
36	P11	—	EH11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
37	P10	—	EH10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
38	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
39	P147	—	EH147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
40	P27	—	—	—	ANI7	—	—	—	—	TS25 Note	—	—	—	—	—	—
41	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—
42	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
43	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—
44	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
45	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
46	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
47	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
48	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
49	P03	—	—	—	ANI16	—	—	—	—	TS29 Note	—	—	RxD1	—	—	—
50	P02	—	—	—	ANI17	—	—	—	—	TS28 Note	—	—	TxD1	—	—	—
51	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	—	—	—	—
52	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.8 64-pin products

- 64-pin plastic LQFP (12 × 12 mm, 0.65-mm pitch)
- 64-pin plastic LFQFP (10 × 10 mm, 0.50-mm pitch)



Note Not present in products with 128 or fewer Kbytes of code flash memory.

- Caution 1.** Connect the EVSS0 pin to the same ground as the VSS pin.
- Caution 2.** Make sure that the voltage on the VDD pin is no less than that on the EVDD0 pin.
- Caution 3.** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 9 Multiplexed Pin Functions of the 64-pin Products (1/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	64LQFP, 64LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
2	P43	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKA1	—
3	P42	—	—	—	—	—	—	—	—	—	TI04/TO04	—	—	—	TxDA1	—
4	P41	—	—	—	—	—	—	—	—	—	TI07/TO07	—	—	—	RxDA1	—
5	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
6	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
7	P124	—	—	XT2/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
8	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
9	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
10	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
11	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
12	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
14	—	—	—	EVss0	—	—	—	—	—	—	—	—	—	—	—	—
15	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
16	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—
17	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
18	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
19	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
20	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
21	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
22	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
23	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
24	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	SCK01/SCL01	—	—	—
25	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	SI01/SDA01	—	—	—
26	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	SO01	—	—	—
27	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
28	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxDA0	—
29	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
30	P06	—	—	—	—	—	—	—	—	TS11	TI06/TO06	—	—	—	CLKA0	—
31	P05	—	—	—	—	—	—	—	—	TS10	TI05/TO05	—	—	—	—	—

Table 1 - 9 Multiplexed Pin Functions of the 64-pin Products (2/3)

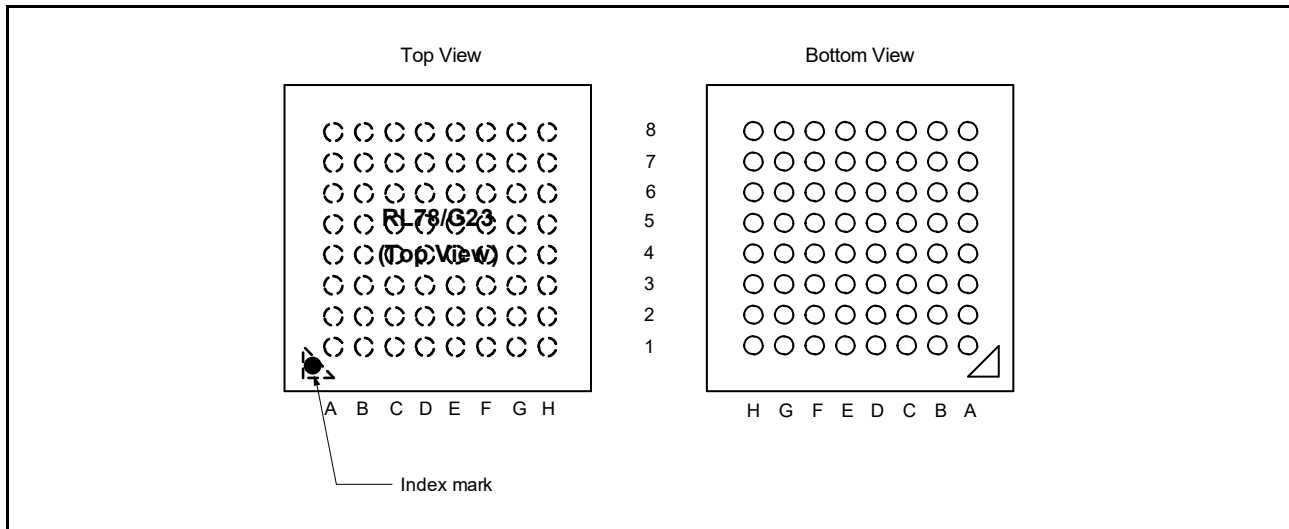
Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	64LQFP, 64LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
32	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—	—
33	P50	CCD03	EI50/ EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/ SDA11	—	—	—
34	P51	CCD02	EI51/ EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
35	P52	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
36	P53	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
37	P54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
38	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
39	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/ TO02	—	(SO00)/ TxD0	—	—	—
40	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/ TO01	—	(SI00)/ RxD0	—	—	—
41	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
42	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
43	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
44	P12	—	EI12/ EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
45	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
46	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
47	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
49	P27	—	—	—	ANI7	—	—	—	—	TS25 Note	—	—	—	—	—	—
50	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—
51	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—
52	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—
53	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
54	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—
55	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
56	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
57	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 9 Multiplexed Pin Functions of the 64-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	Digital port	Output current control port	ELCL input/output port		A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)	Remote control signal receiver (REMIC)
58	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—
59	P03	—	—	—	ANI16	—	—	—	—	TS29 Note	—	—	SI10/ RxD1/ SDA10	—	—	—
60	P02	—	—	—	ANI17	—	—	—	—	TS28 Note	—	—	SO10/ TxD1	—	—	—
61	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	—	—	—	—
62	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	—	—	—	—
63	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
64	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

- 64-pin plastic WFLGA (5 × 5 mm, 0.50-mm pitch)



	A	B	C	D	E	F	G	H
8	EVDD0	EVSS0	P121/X1/EI121/ VBAT	P122/X2/EXCLK/ EI122	P137/INTP0/ EI137	P123/XT1	P124/XT2/ EXCLKS	P120/ANI19/ IVCMP1/EI120
7	P60/CCD04/ SCLA0/EO60	VDD	VSS	REGC	RESET	P01/TS27Note/ EI01/EO01/ TO00	P00/TS26Note/ EI00/TI00	P140/PCLBUZ0/ INTP6
6	P61/CCD05/ SDAA0/EO61	P62/CCD06/ SCLA1	P63/CCD07/ SDAA1	P40/TOOL0	P41/TI07/TO07/ RxDA1	P43/CLKA1	P02/ANI17/ TS28Note/ SO10/TxD1	P141/PCLBUZ1/ INTP7
5	P77/KR7/TS09/ INTP11/(TxD2)	P31/TI03/TO03/ INTP4/TS01/ EI31/(PCLBUZ0)	P53/(INTP11)	P42/TI04/TO04/ TxDA1	P03/ANI16/ TS29Note/ SI10/RxD1/ SDA10	P04/SCK10/ SCL10	P130	P20/ANI0/ AVREFP/EI20
4	P75/KR5/TS07/ INTP9/SCK01/ SCL01	P76/KR6/TS08/ INTP10/(RxD2)	P52/(INTP10)	P54	P16/CCD00/ TI01/TO01/ INTP5/EO16/ (SI00)/(RxD0)	P21/ANI1/ AVREFM/EI21	P22/ANI2/ANO0/ EI22/TS20Note	P23/ANI3/ANO1/ IVREF0/EI23/ TS21Note
3	P70/KR0/TS02/ RIN0/SCK21/ SCL21	P73/KR3/TS05/ SO01	P74/KR4/TS06/ INTP8/SI01/ SDA01	P17/CCD01/ TI02/TO02/ EO17/(SO00)/ (TxD0)	P15/SCK20/ SCL20/EO15/ (TI02)/(TO02)	P12/SO00/TxD0/ TOOLTxD/EI12/ EO12/(INTP5)/ (TI05)/(TO05)	P24/ANI4/ TS22Note	P26/ANI6/ TS24Note
2	P30/INTP3/ TSCAP/ RTC1HZ/EI30/ VCOUT0/ SCK11/SCL11	P72/KR2/TS04/ SO21/TxDA0	P71/KR1/TS03/ SI21/SDA21/ RxDA0	P06/TS11/TI06/ TO06/CLKA0	P14/RxD2/ SI20/SDA20/ VCOUT1/EO14/ (SCLA0)/(TI03)/ (TO03)	P11/SI00/RxD0/ TOOLRxD/ SDA00/EI11/ EO11/(TI06)/ (TO06)	P25/ANI5/ TS23Note	P27/ANI7/ TS25Note
1	P05/TS10/TI05/ TO05	P50/CCD03/ TS00/EI50/ EO50/INTP1/ SI11/SDA11	P51/CCD02/ EI51/EO51/ INTP2/SO11	P55/(PCLBUZ1)/ (SCK00)	P13/TxD2/SO20/ IVREF1/EO13/ (SDAA0)/(TI04)/ (TO04)	P10/SCK00/ SCL00/EI10/ EO10/(TI07)/ (TO07)	P146	P147/ANI18/ EI147/IVCMP0

Note Not present in products with 128 or fewer Kbytes of code flash memory.

(Cautions and Remarks are listed on the next page.)

Caution 1. Connect the EVSS0 pin to the same ground as the VSS pin.

Caution 2. Make sure that the voltage on the VDD pin is no less than that on the EVDD0 pin.

Caution 3. Connect the REGC pin to VSS via a capacitor (0.47 to 1 μ F).

Remark 1. For pin identification, see **1.4 Pin Identification**.

Remark 2. When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD and EVDD0 pins and connect the VSS and EVSS0 pins to separate ground lines.

Remark 3. Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 10 Multiplexed Pin Functions 2 of the 64-pin Products (1/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	64WFLGA	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
A1	P05	—	—	—	—	—	—	—	—	TS10	TI05/TO05	—	—	—	—	—
A2	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
A3	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
A4	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	SCK01/SCL01	—	—	—
A5	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
A6	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
A7	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
A8	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—
B1	P50	CCD03	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
B2	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
B3	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	SO01	—	—	—
B4	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
B5	P31	—	EI31 (PCLBUZ0)	—	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
B6	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
B7	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
B8	—	—	—	EVSS0	—	—	—	—	—	—	—	—	—	—	—	—
C1	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
C2	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxDA0	—
C3	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	SI01/SDA01	—	—	—
C4	P52	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
C5	P53	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
C6	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
C7	—	—	—	VSS	—	—	—	—	—	—	—	—	—	—	—	—
C8	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
D1	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
D2	P06	—	—	—	—	—	—	—	—	TS11	TI06/TO06	—	—	—	CLKA0	—
D3	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(SO00)/(TxD0)	—	—	—
D4	P54	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
D5	P42	—	—	—	—	—	—	—	—	—	TI04/TO04	—	—	—	TxDA1	—
D6	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
D7	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 10 Multiplexed Pin Functions 2 of the 64-pin Products (2/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces				
	64WFLGA	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)	Remote control signal receiver (REMIC)
D8	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—	—
E1	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—	—
E2	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—	—
E3	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—	—
E4	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/ TO01	—	(SI00)/ (RxD0)	—	—	—	—
E5	P03	—	—	—	ANI16	—	—	—	—	TS29 Note	—	—	SI10/ RxD1/ SDA10	—	—	—	—
E6	P41	—	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	RxDA1	—	—
E7	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—	—
E8	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—	—
F1	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—	—
F2	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—	—
F3	P12	—	EI12/ EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—	—
F4	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—	—
F5	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—	—
F6	P43	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKA1	—	—
F7	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27 Note	TO00	—	—	—	—	—	—
F8	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—	—
G1	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
G2	P25	—	—	—	ANI5	—	—	—	—	TS23 Note	—	—	—	—	—	—	—
G3	P24	—	—	—	ANI4	—	—	—	—	TS22 Note	—	—	—	—	—	—	—
G4	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20 Note	—	—	—	—	—	—	—
G5	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
G6	P02	—	—	—	ANI17	—	—	—	—	TS28 Note	—	—	SO10/ TxD1	—	—	—	—
G7	P00	—	EI00	—	—	—	—	—	—	TS26 Note	TI00	—	—	—	—	—	—
G8	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—	—
H1	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—	—

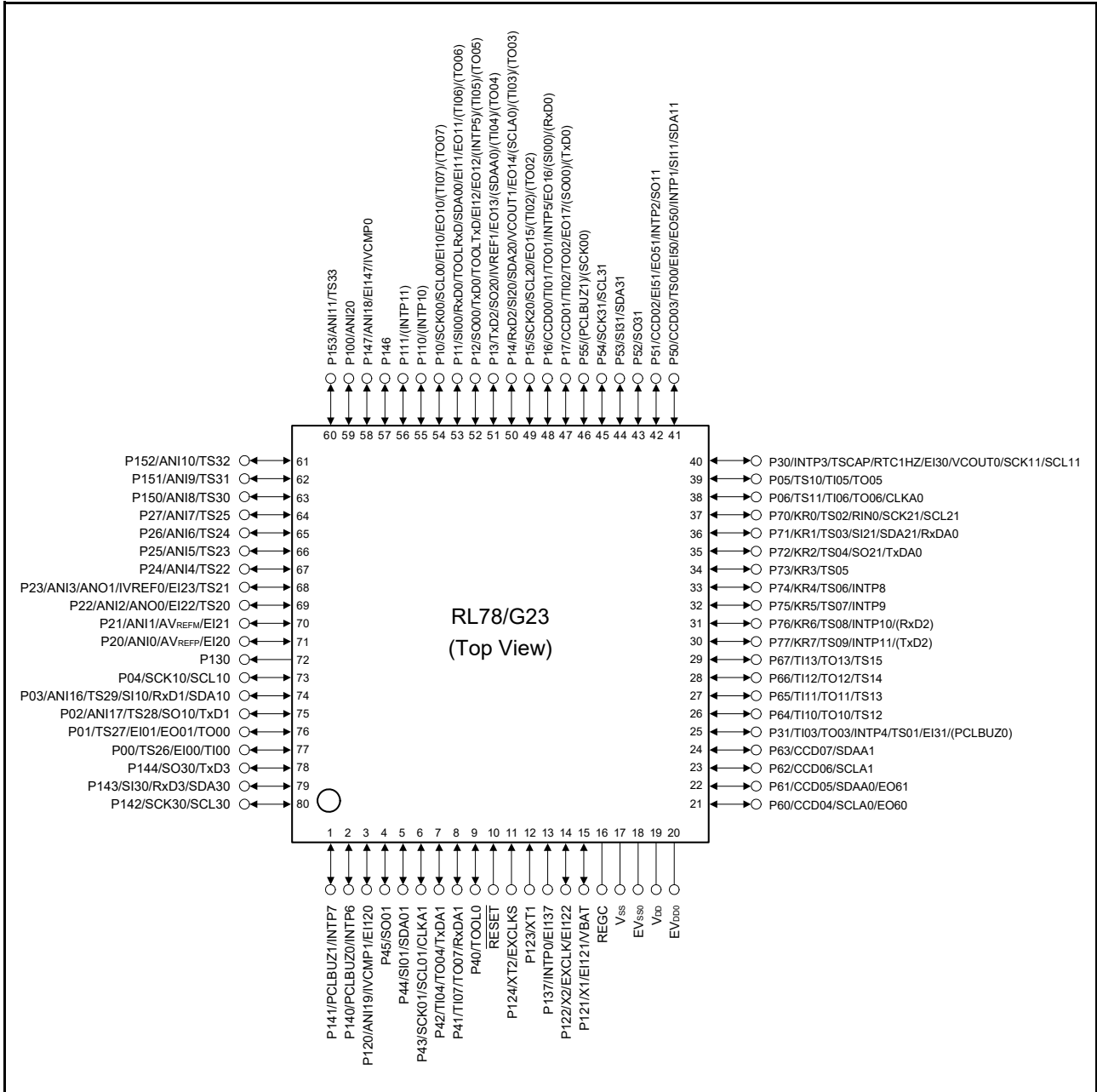
Table 1 - 10 Multiplexed Pin Functions 2 of the 64-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	64WFLGA	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
H2	P27	—	—	—	ANI7	—	—	—	—	TS25 Note	—	—	—	—	—	—
H3	P26	—	—	—	ANI6	—	—	—	—	TS24 Note	—	—	—	—	—	—
H4	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21 Note	—	—	—	—	—	—
H5	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
H6	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
H7	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
H8	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—

Note Not present in products with 128 or fewer Kbytes of code flash memory.

1.3.9 80-pin products

- 80-pin plastic LQFP (14 × 14 mm, 0.65-mm pitch)
- 80-pin plastic LFQFP (12 × 12 mm, 0.50-mm pitch)



- Caution 1.** Connect the EV_{VSS0} pin to the same ground as the V_{SS} pin.
- Caution 2.** Make sure that the voltage on the V_{DD} pin is no less than that on the EV_{VDD0} pin.
- Caution 3.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD} and EV_{VDD0} pins and connect the V_{SS} and EV_{VSS0} pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to **Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR)** in the RL78/G23 User's Manual.

Table 1 - 11 Multiplexed Pin Functions of the 80-pin Products (1/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	80LFQFP, 80LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
2	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
3	P120	—	EH120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
4	P45	—	—	—	—	—	—	—	—	—	—	—	SO01	—	—	—
5	P44	—	—	—	—	—	—	—	—	—	—	—	SI01/ SDA01	—	—	—
6	P43	—	—	—	—	—	—	—	—	—	—	—	SCK01/ SCL01	—	CLKA1	—
7	P42	—	—	—	—	—	—	—	—	—	TI04/ TO04	—	—	—	TxDA1	—
8	P41	—	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	RxDA1	—
9	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
10	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
11	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
12	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
13	P137	—	EH137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
14	P122	—	EH122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
15	P121	—	EH121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
16	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
17	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
18	—	—	—	EVss0	—	—	—	—	—	—	—	—	—	—	—	—
19	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
20	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—
21	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
22	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
23	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
24	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
25	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/ TO03	—	—	—	—	—
26	P64	—	—	—	—	—	—	—	—	TS12	TI10/ TO10	—	—	—	—	—
27	P65	—	—	—	—	—	—	—	—	TS13	TI11/ TO11	—	—	—	—	—
28	P66	—	—	—	—	—	—	—	—	TS14	TI12/ TO12	—	—	—	—	—
29	P67	—	—	—	—	—	—	—	—	TS15	TI13/ TO13	—	—	—	—	—
30	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
31	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
32	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	—	—	—	—

Table 1 - 11 Multiplexed Pin Functions of the 80-pin Products (2/3)

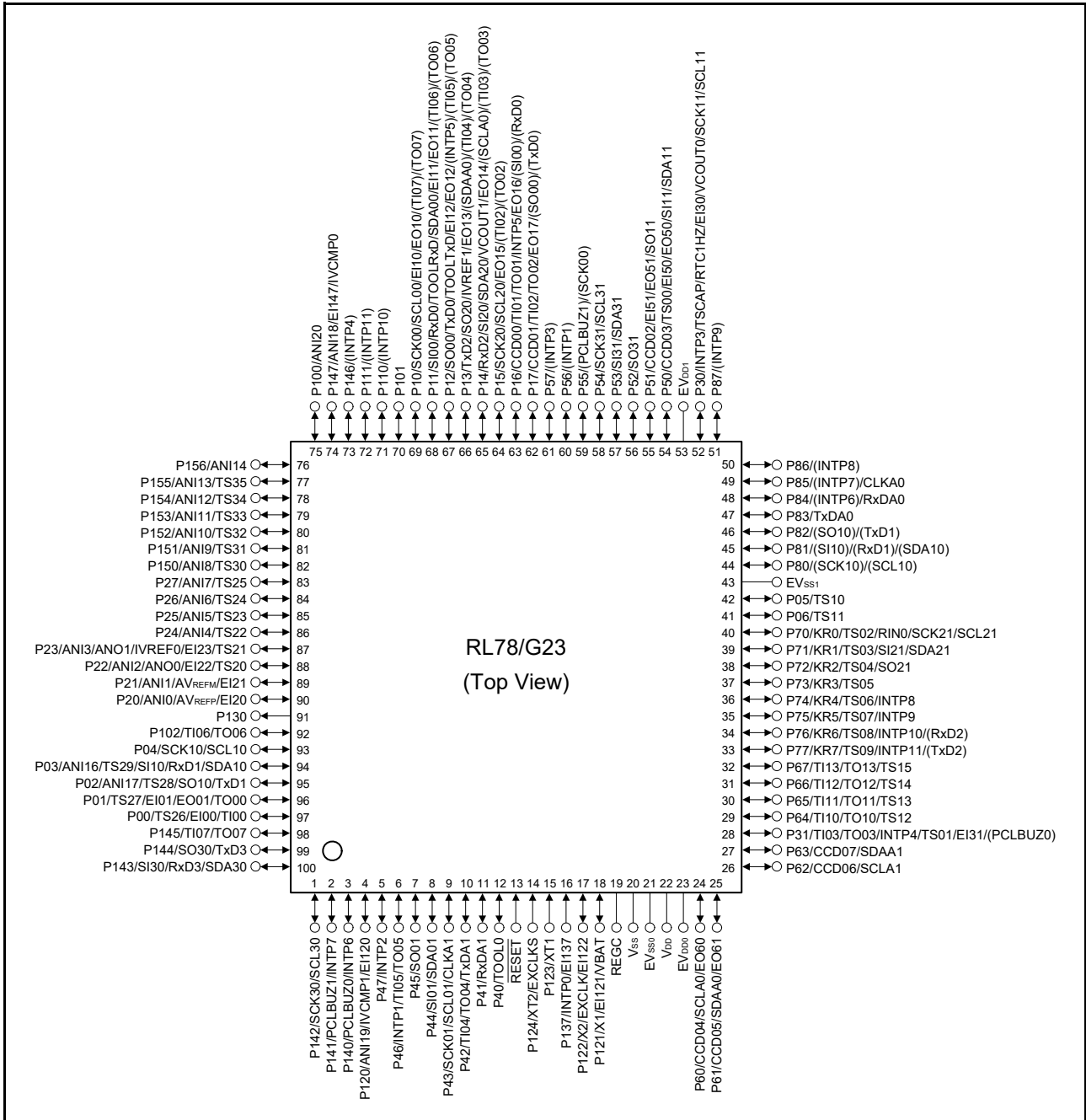
Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	80LQFP, 80LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
33	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	—	—	—	—
34	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
35	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	TxDA0	—
36	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	RxDA0	—
37	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RINO
38	P06	—	—	—	—	—	—	—	—	TS11	TI06/TO06	—	—	—	CLKA0	—
39	P05	—	—	—	—	—	—	—	—	TS10	TI05/TO05	—	—	—	—	—
40	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
41	P50	CCD03	EI50/EO50	—	—	—	—	INTP1	—	TS00	—	—	SI11/SDA11	—	—	—
42	P51	CCD02	EI51/EO51	—	—	—	—	INTP2	—	—	—	—	SO11	—	—	—
43	P52	—	—	—	—	—	—	—	—	—	—	—	SO31	—	—	—
44	P53	—	—	—	—	—	—	—	—	—	—	—	SI31/SDA31	—	—	—
45	P54	—	—	—	—	—	—	—	—	—	—	—	SCK31/SCL31	—	—	—
46	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
47	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(SO00)/TxD0	—	—	—
48	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(SI00)/RxD0	—	—	—
49	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/TO02	—	SCK20/SCL20	—	—	—
50	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/TO03	—	SI20/RxD2/SDA20	(SCLA0)	—	—
51	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/TO04	—	SO20/TxD2	(SDAA0)	—	—
52	P12	—	EI12/EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/TO05	—	SO00/TxD0	—	—	—
53	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/TO06	—	SI00/RxD0/SDA00	—	—	—
54	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/TO07	—	SCK00/SCL00	—	—	—
55	P110	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
56	P111	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
57	P146	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
59	P100	—	—	—	ANI20	—	—	—	—	—	—	—	—	—	—	—
60	P153	—	—	—	ANI11	—	—	—	—	TS33	—	—	—	—	—	—

Table 1 - 11 Multiplexed Pin Functions of the 80-pin Products (3/3)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	80LFGFP, 80LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
61	P152	—	—	—	ANI10	—	—	—	—	TS32	—	—	—	—	—	—
62	P151	—	—	—	ANI9	—	—	—	—	TS31	—	—	—	—	—	—
63	P150	—	—	—	ANI8	—	—	—	—	TS30	—	—	—	—	—	—
64	P27	—	—	—	ANI7	—	—	—	—	TS25	—	—	—	—	—	—
65	P26	—	—	—	ANI6	—	—	—	—	TS24	—	—	—	—	—	—
66	P25	—	—	—	ANI5	—	—	—	—	TS23	—	—	—	—	—	—
67	P24	—	—	—	ANI4	—	—	—	—	TS22	—	—	—	—	—	—
68	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21	—	—	—	—	—	—
69	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20	—	—	—	—	—	—
70	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
71	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
72	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
73	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—
74	P03	—	—	—	ANI16	—	—	—	—	TS29	—	—	SI10/ RxD1/ SDA10	—	—	—
75	P02	—	—	—	ANI17	—	—	—	—	TS28	—	—	SO10/ TxD1	—	—	—
76	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27	TO00	—	—	—	—	—
77	P00	—	EI00	—	—	—	—	—	—	TS26	TI00	—	—	—	—	—
78	P144	—	—	—	—	—	—	—	—	—	—	—	SO30/ TxD3	—	—	—
79	P143	—	—	—	—	—	—	—	—	—	—	—	SI30/ RxD3/ SDA30	—	—	—
80	P142	—	—	—	—	—	—	—	—	—	—	—	SCK30/ SCL30	—	—	—

1.3.10 100-pin products

- 100-pin plastic LFQFP (14 × 14 mm, 0.50-mm pitch)



- Caution 1.** Connect the EVSS0 and EVSS1 pins to the same ground as the VSS pin.
- Caution 2.** Make sure that the voltage on the VDD pin is no less than that on the EVDD0 and EVDD1 pins. Also make sure that the voltage on the EVDD0 is the same as that on the EVDD1 pin.
- Caution 3.** Connect the REGC pin to VSS via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the VDD, EVDD0, and EVDD1 pins and connect the VSS, EVSS0, and EVSS1 pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G23 User's Manual.

Table 1 - 12 Multiplexed Pin Functions of the 100-pin Products (1/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	100LFGFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTS2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P142	—	—	—	—	—	—	—	—	—	—	—	SCK30/ SCL30	—	—	—
2	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
3	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
4	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
5	P47	—	—	—	—	—	—	INTP2	—	—	—	—	—	—	—	—
6	P46	—	—	—	—	—	—	INTP1	—	—	TI05/ TO05	—	—	—	—	—
7	P45	—	—	—	—	—	—	—	—	—	—	—	SO01	—	—	—
8	P44	—	—	—	—	—	—	—	—	—	—	—	SI01/ SDA01	—	—	—
9	P43	—	—	—	—	—	—	—	—	—	—	—	SCK01/ SCL01	—	CLKA1	—
10	P42	—	—	—	—	—	—	—	—	—	TI04/ TO04	—	—	—	TxDA1	—
11	P41	—	—	—	—	—	—	—	—	—	—	—	—	—	RxDA1	—
12	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
13	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
14	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
15	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
16	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
17	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
18	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
19	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
20	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
21	—	—	—	EVss0	—	—	—	—	—	—	—	—	—	—	—	—
22	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
23	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—
24	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
25	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
26	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
27	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
28	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/ TO03	—	—	—	—	—
29	P64	—	—	—	—	—	—	—	—	TS12	TI10/ TO10	—	—	—	—	—
30	P65	—	—	—	—	—	—	—	—	TS13	TI11/ TO11	—	—	—	—	—
31	P66	—	—	—	—	—	—	—	—	TS14	TI12/ TO12	—	—	—	—	—

Table 1 - 12 Multiplexed Pin Functions of the 100-pin Products (2/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	100LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
32	P67	—	—	—	—	—	—	—	—	TS15	TI13/TO13	—	—	—	—	—
33	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
34	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
35	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	—	—	—	—
36	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	—	—	—	—
37	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
38	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	—	—
39	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	—	—
40	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
41	P06	—	—	—	—	—	—	—	—	TS11	—	—	—	—	—	—
42	P05	—	—	—	—	—	—	—	—	TS10	—	—	—	—	—	—
43	—	—	—	EVss1	—	—	—	—	—	—	—	—	—	—	—	—
44	P80	—	—	—	—	—	—	—	—	—	—	—	(SCK10)/ (SCL10)	—	—	—
45	P81	—	—	—	—	—	—	—	—	—	—	—	(SI10)/ (RxD1)/ (SDA10)	—	—	—
46	P82	—	—	—	—	—	—	—	—	—	—	—	(SO10)/ (TxD1)	—	—	—
47	P83	—	—	—	—	—	—	—	—	—	—	—	—	—	TxDA0	—
48	P84	—	—	—	—	—	—	(INTP6)	—	—	—	—	—	—	RxDA0	—
49	P85	—	—	—	—	—	—	(INTP7)	—	—	—	—	—	—	CLKA0	—
50	P86	—	—	—	—	—	—	(INTP8)	—	—	—	—	—	—	—	—
51	P87	—	—	—	—	—	—	(INTP9)	—	—	—	—	—	—	—	—
52	P30	—	EI30	—	—	—	VCOU0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/ SCL11	—	—	—
53	—	—	—	EVDD1	—	—	—	—	—	—	—	—	—	—	—	—
54	P50	CCD03	EI50/ EO50	—	—	—	—	—	—	TS00	—	—	SI11/ SDA11	—	—	—
55	P51	CCD02	EI51/ EO51	—	—	—	—	—	—	—	—	—	SO11	—	—	—
56	P52	—	—	—	—	—	—	—	—	—	—	—	SO31	—	—	—
57	P53	—	—	—	—	—	—	—	—	—	—	—	SI31/ SDA31	—	—	—
58	P54	—	—	—	—	—	—	—	—	—	—	—	SCK31/ SCL31	—	—	—
59	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
60	P56	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—
61	P57	—	—	—	—	—	—	(INTP3)	—	—	—	—	—	—	—	—
62	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/ TO02	—	(SO00)/ (TxD0)	—	—	—

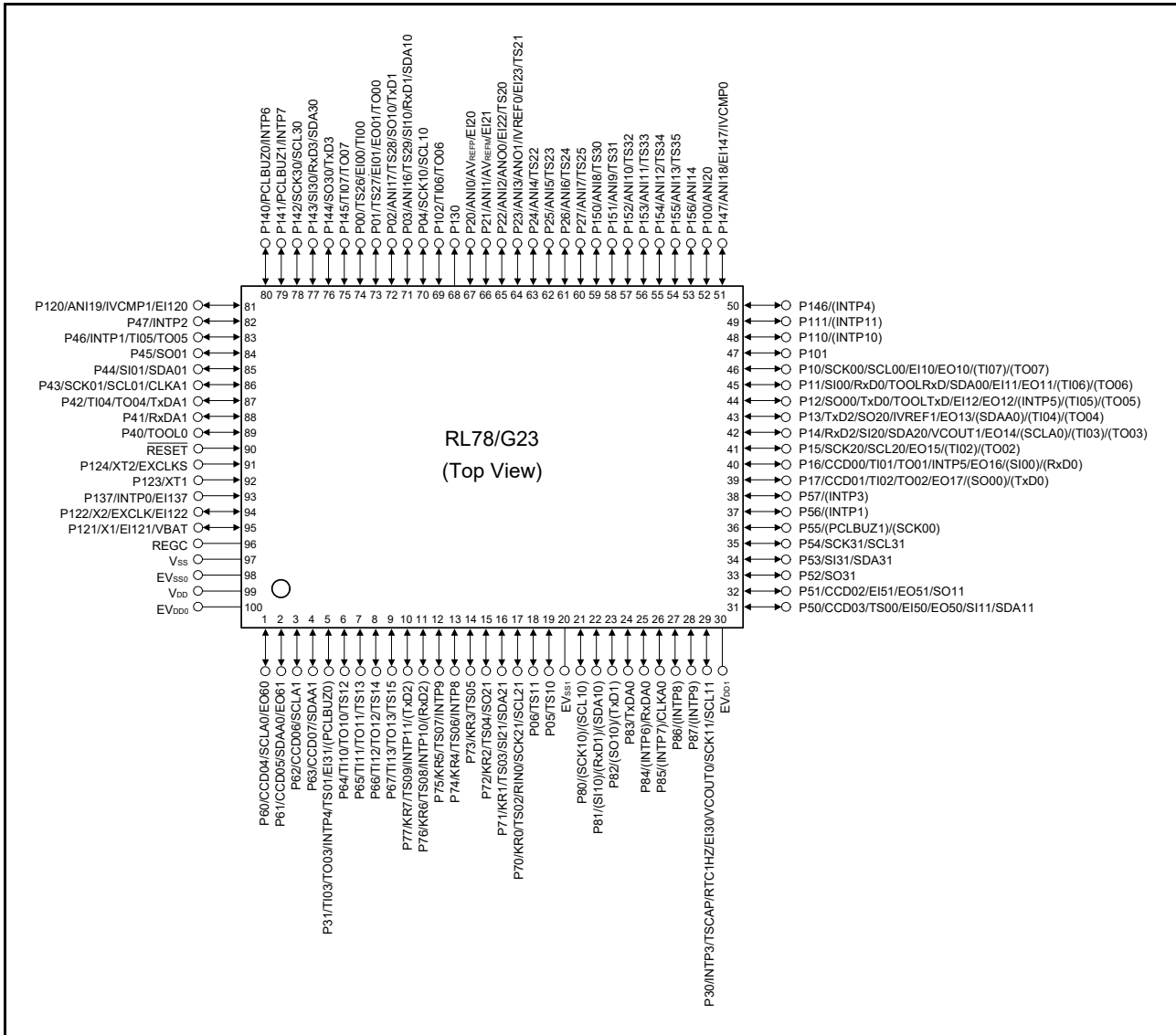
Table 1 - 12 Multiplexed Pin Functions of the 100-pin Products (3/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	100LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
63	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(SI00)/ (RxD0)	—	—	—
64	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/ (TO02)	—	SCK20/ SCL20	—	—	—
65	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/ (TO03)	—	SI20/ RxD2/ SDA20	(SCLA0)	—	—
66	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/ (TO04)	—	SO20/ TxD2	(SDAA0)	—	—
67	P12	—	EI12/ EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/ (TO05)	—	SO00/ TxD0	—	—	—
68	P11	—	EI11/ EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/ (TO06)	—	SI00/ RxD0/ SDA00	—	—	—
69	P10	—	EI10/ EO10	—	—	—	—	—	—	—	(TI07)/ (TO07)	—	SCK00/ SCL00	—	—	—
70	P101	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
71	P110	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
72	P111	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
73	P146	—	—	—	—	—	—	(INTP4)	—	—	—	—	—	—	—	—
74	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
75	P100	—	—	—	ANI20	—	—	—	—	—	—	—	—	—	—	—
76	P156	—	—	—	ANI14	—	—	—	—	—	—	—	—	—	—	—
77	P155	—	—	—	ANI13	—	—	—	—	TS35	—	—	—	—	—	—
78	P154	—	—	—	ANI12	—	—	—	—	TS34	—	—	—	—	—	—
79	P153	—	—	—	ANI11	—	—	—	—	TS33	—	—	—	—	—	—
80	P152	—	—	—	ANI10	—	—	—	—	TS32	—	—	—	—	—	—
81	P151	—	—	—	ANI9	—	—	—	—	TS31	—	—	—	—	—	—
82	P150	—	—	—	ANI8	—	—	—	—	TS30	—	—	—	—	—	—
83	P27	—	—	—	ANI7	—	—	—	—	TS25	—	—	—	—	—	—
84	P26	—	—	—	ANI6	—	—	—	—	TS24	—	—	—	—	—	—
85	P25	—	—	—	ANI5	—	—	—	—	TS23	—	—	—	—	—	—
86	P24	—	—	—	ANI4	—	—	—	—	TS22	—	—	—	—	—	—
87	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21	—	—	—	—	—	—
88	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20	—	—	—	—	—	—
89	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
90	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
91	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
92	P102	—	—	—	—	—	—	—	—	—	TI06/ TO06	—	—	—	—	—
93	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—

Table 1 - 12 Multiplexed Pin Functions of the 100-pin Products (4/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	100LFQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
94	P03	—	—	—	ANI16	—	—	—	—	TS29	—	—	SI10/ RxD1/ SDA10	—	—	—
95	P02	—	—	—	ANI17	—	—	—	—	TS28	—	—	SO10/ TxD1	—	—	—
96	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27	TO00	—	—	—	—	—
97	P00	—	EI00	—	—	—	—	—	—	TS26	TI00	—	—	—	—	—
98	P145	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	—	—	—
99	P144	—	—	—	—	—	—	—	—	—	—	—	SO30/ TxD3	—	—	—
100	P143	—	—	—	—	—	—	—	—	—	—	—	SI30/ RxD3/ SDA30	—	—	—

- 100-pin plastic LQFP (14 × 20 mm, 0.65-mm pitch)



- Caution 1.** Connect the EV_{SS0} and EV_{SS1} pins to the same ground as the V_{SS} pin.
- Caution 2.** Make sure that the voltage on the V_{DD} pin is no less than that on the EV_{DD0} and EV_{DD1} pins. Also make sure that the voltage on the EV_{DD0} is the same as that on the EV_{DD1} pin.
- Caution 3.** Connect the REGC pin to V_{SS} via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0}, and EV_{DD1} pins and connect the V_{SS}, EV_{SS0}, and EV_{SS1} pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G23 User's Manual.

Table 1 - 13 Multiplexed Pin Functions 2 of the 100-pin Products (1/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI's			Timers		Communications Interfaces			
	100LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
2	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
3	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
4	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
5	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
6	P64	—	—	—	—	—	—	—	—	TS12	TI10/TO10	—	—	—	—	—
7	P65	—	—	—	—	—	—	—	—	TS13	TI11/TO11	—	—	—	—	—
8	P66	—	—	—	—	—	—	—	—	TS14	TI12/TO12	—	—	—	—	—
9	P67	—	—	—	—	—	—	—	—	TS15	TI13/TO13	—	—	—	—	—
10	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
11	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
12	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	—	—	—	—
13	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	—	—	—	—
14	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
15	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	—	—
16	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	—	—
17	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
18	P06	—	—	—	—	—	—	—	—	TS11	—	—	—	—	—	—
19	P05	—	—	—	—	—	—	—	—	TS10	—	—	—	—	—	—
20	—	—	—	EVss1	—	—	—	—	—	—	—	—	—	—	—	—
21	P80	—	—	—	—	—	—	—	—	—	—	—	(SCK10)/SCL10	—	—	—
22	P81	—	—	—	—	—	—	—	—	—	—	—	(SI10)/(RxD1)/SDA10	—	—	—
23	P82	—	—	—	—	—	—	—	—	—	—	—	(SO10)/(TxD1)	—	—	—
24	P83	—	—	—	—	—	—	—	—	—	—	—	—	—	TxDA0	—
25	P84	—	—	—	—	—	—	(INTP6)	—	—	—	—	—	—	RxDA0	—
26	P85	—	—	—	—	—	—	(INTP7)	—	—	—	—	—	—	CLKA0	—
27	P86	—	—	—	—	—	—	(INTP8)	—	—	—	—	—	—	—	—
28	P87	—	—	—	—	—	—	(INTP9)	—	—	—	—	—	—	—	—
29	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	SCK11/SCL11	—	—	—
30	—	—	—	EVDD1	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 13 Multiplexed Pin Functions 2 of the 100-pin Products (2/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI's			Timers		Communications Interfaces			
	100LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUZL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
31	P50	CCD03	EI50/EO50	—	—	—	—	—	—	TS00	—	—	SI11/SDA11	—	—	—
32	P51	CCD02	EI51/EO51	—	—	—	—	—	—	—	—	—	SO11	—	—	—
33	P52	—	—	—	—	—	—	—	—	—	—	—	SO31	—	—	—
34	P53	—	—	—	—	—	—	—	—	—	—	—	SI31/SDA31	—	—	—
35	P54	—	—	—	—	—	—	—	—	—	—	—	SCK31/SCL31	—	—	—
36	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
37	P56	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—
38	P57	—	—	—	—	—	—	(INTP3)	—	—	—	—	—	—	—	—
39	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(SO00)/TxD0	—	—	—
40	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(SI00)/RxD0	—	—	—
41	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/TO02	—	SCK20/SCL20	—	—	—
42	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/TO03	—	SI20/RxD2/SDA20	(SCLA0)	—	—
43	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/TO04	—	SO20/TxD2	(SDAA0)	—	—
44	P12	—	EI12/EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/TO05	—	SO00/TxD0	—	—	—
45	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/TO06	—	SI00/RxD0/SDA00	—	—	—
46	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/TO07	—	SCK00/SCL00	—	—	—
47	P101	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48	P110	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
49	P111	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
50	P146	—	—	—	—	—	—	(INTP4)	—	—	—	—	—	—	—	—
51	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
52	P100	—	—	—	ANI20	—	—	—	—	—	—	—	—	—	—	—
53	P156	—	—	—	ANI14	—	—	—	—	—	—	—	—	—	—	—
54	P155	—	—	—	ANI13	—	—	—	—	TS35	—	—	—	—	—	—
55	P154	—	—	—	ANI12	—	—	—	—	TS34	—	—	—	—	—	—
56	P153	—	—	—	ANI11	—	—	—	—	TS33	—	—	—	—	—	—
57	P152	—	—	—	ANI10	—	—	—	—	TS32	—	—	—	—	—	—
58	P151	—	—	—	ANI9	—	—	—	—	TS31	—	—	—	—	—	—
59	P150	—	—	—	ANI8	—	—	—	—	TS30	—	—	—	—	—	—
60	P27	—	—	—	ANI7	—	—	—	—	TS25	—	—	—	—	—	—

Table 1 - 13 Multiplexed Pin Functions 2 of the 100-pin Products (3/4)

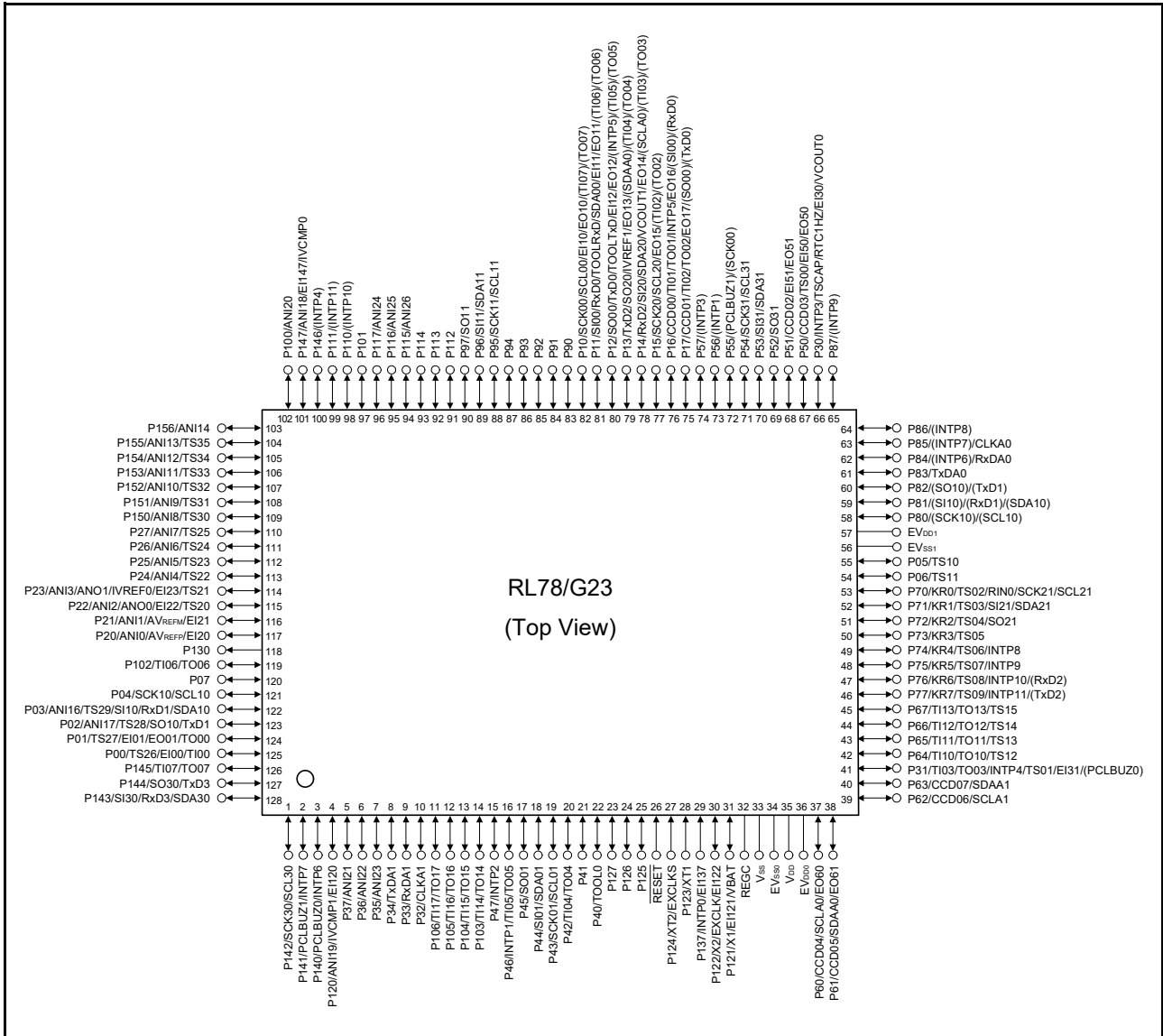
Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	100LOFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
61	P26	—	—	—	ANI6	—	—	—	—	TS24	—	—	—	—	—	—
62	P25	—	—	—	ANI5	—	—	—	—	TS23	—	—	—	—	—	—
63	P24	—	—	—	ANI4	—	—	—	—	TS22	—	—	—	—	—	—
64	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21	—	—	—	—	—	—
65	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20	—	—	—	—	—	—
66	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
67	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
68	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
69	P102	—	—	—	—	—	—	—	—	—	TI06/ TO06	—	—	—	—	—
70	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—
71	P03	—	—	—	ANI16	—	—	—	—	TS29	—	—	SI10/ RxD1/ SDA10	—	—	—
72	P02	—	—	—	ANI17	—	—	—	—	TS28	—	—	SO10/ TxD1	—	—	—
73	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27	TO00	—	—	—	—	—
74	P00	—	EI00	—	—	—	—	—	—	TS26	TI00	—	—	—	—	—
75	P145	—	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	—	—
76	P144	—	—	—	—	—	—	—	—	—	—	—	SO30/ TxD3	—	—	—
77	P143	—	—	—	—	—	—	—	—	—	—	—	SI30/ RxD3/ SDA30	—	—	—
78	P142	—	—	—	—	—	—	—	—	—	—	—	SCK30/ SCL30	—	—	—
79	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
80	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
81	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
82	P47	—	—	—	—	—	—	INTP2	—	—	—	—	—	—	—	—
83	P46	—	—	—	—	—	—	INTP1	—	—	TI05/ TO05	—	—	—	—	—
84	P45	—	—	—	—	—	—	—	—	—	—	—	SO01	—	—	—
85	P44	—	—	—	—	—	—	—	—	—	—	—	SI01/ SDA01	—	—	—
86	P43	—	—	—	—	—	—	—	—	—	—	—	SCK01/ SCL01	—	CLKA1	—
87	P42	—	—	—	—	—	—	—	—	—	TI04/ TO04	—	—	—	TxDA1	—
88	P41	—	—	—	—	—	—	—	—	—	—	—	—	—	RxDA1	—
89	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 13 Multiplexed Pin Functions 2 of the 100-pin Products (4/4)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	100LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
90	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
91	P124	—	—	XT2/EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
92	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
93	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
94	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
95	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
96	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—
97	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
98	—	—	—	EVSS0	—	—	—	—	—	—	—	—	—	—	—	—
99	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
100	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—

1.3.11 128-pin products

- 128-pin plastic LFQFP (14 × 20 mm, 0.50-mm pitch)



- Caution 1.** Connect the EV_{ss0} and EV_{ss1} pins to the same ground as the V_{ss} pin.
- Caution 2.** Make sure that the voltage on the V_{DD} pin is no less than that on the EV_{DD0} and EV_{DD1} pins. Also make sure that the voltage on the EV_{DD0} is the same as that on the EV_{DD1} pin.
- Caution 3.** Connect the REGC pin to V_{ss} via a capacitor (0.47 to 1 μF).

- Remark 1.** For pin identification, see 1.4 Pin Identification.
- Remark 2.** When using the microcontroller for an application where the noise generated inside the microcontroller must be reduced, it is recommended to supply separate powers to the V_{DD}, EV_{DD0}, and EV_{DD1} pins and connect the V_{ss}, EV_{ss0}, and EV_{ss1} pins to separate ground lines.
- Remark 3.** Functions in parentheses in the above figure can be assigned via settings in the peripheral I/O redirection register (PIOR). Refer to Figure 4 - 10 Format of Peripheral I/O Redirection Register (PIOR) in the RL78/G23 User's Manual.

Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products (1/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	128LFGFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTS2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
1	P142	—	—	—	—	—	—	—	—	—	—	—	SCK30/ SCL30	—	—	—
2	P141	—	—	PCLBUZ1	—	—	—	INTP7	—	—	—	—	—	—	—	—
3	P140	—	—	PCLBUZ0	—	—	—	INTP6	—	—	—	—	—	—	—	—
4	P120	—	EI120	—	ANI19	—	IVCMP1	—	—	—	—	—	—	—	—	—
5	P37	—	—	—	ANI21	—	—	—	—	—	—	—	—	—	—	—
6	P36	—	—	—	ANI22	—	—	—	—	—	—	—	—	—	—	—
7	P35	—	—	—	ANI23	—	—	—	—	—	—	—	—	—	—	—
8	P34	—	—	—	—	—	—	—	—	—	—	—	—	—	TxDA1	—
9	P33	—	—	—	—	—	—	—	—	—	—	—	—	—	RxDA1	—
10	P32	—	—	—	—	—	—	—	—	—	—	—	—	—	CLKA1	—
11	P106	—	—	—	—	—	—	—	—	—	TI17/ TO17	—	—	—	—	—
12	P105	—	—	—	—	—	—	—	—	—	TI16/ TO16	—	—	—	—	—
13	P104	—	—	—	—	—	—	—	—	—	TI15/ TO15	—	—	—	—	—
14	P103	—	—	—	—	—	—	—	—	—	TI14/ TO14	—	—	—	—	—
15	P47	—	—	—	—	—	—	INTP2	—	—	—	—	—	—	—	—
16	P46	—	—	—	—	—	—	INTP1	—	—	TI05/ TO05	—	—	—	—	—
17	P45	—	—	—	—	—	—	—	—	—	—	—	SO01	—	—	—
18	P44	—	—	—	—	—	—	—	—	—	—	—	SI01/ SDA01	—	—	—
19	P43	—	—	—	—	—	—	—	—	—	—	—	SCK01/ SCL01	—	—	—
20	P42	—	—	—	—	—	—	—	—	—	TI04/ TO04	—	—	—	—	—
21	P41	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
22	P40	—	—	TOOL0	—	—	—	—	—	—	—	—	—	—	—	—
23	P127	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
24	P126	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
25	P125	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
26	—	—	—	RESET	—	—	—	—	—	—	—	—	—	—	—	—
27	P124	—	—	XT2/ EXCLKS	—	—	—	—	—	—	—	—	—	—	—	—
28	P123	—	—	XT1	—	—	—	—	—	—	—	—	—	—	—	—
29	P137	—	EI137	—	—	—	—	INTP0	—	—	—	—	—	—	—	—
30	P122	—	EI122	X2/EXCLK	—	—	—	—	—	—	—	—	—	—	—	—
31	P121	—	EI121	X1/VBAT	—	—	—	—	—	—	—	—	—	—	—	—
32	—	—	—	REGC	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products (2/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMI			Timers		Communications Interfaces			
	128LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
33	—	—	—	Vss	—	—	—	—	—	—	—	—	—	—	—	—
34	—	—	—	EVss0	—	—	—	—	—	—	—	—	—	—	—	—
35	—	—	—	VDD	—	—	—	—	—	—	—	—	—	—	—	—
36	—	—	—	EVDD0	—	—	—	—	—	—	—	—	—	—	—	—
37	P60	CCD04	EO60	—	—	—	—	—	—	—	—	—	—	SCLA0	—	—
38	P61	CCD05	EO61	—	—	—	—	—	—	—	—	—	—	SDAA0	—	—
39	P62	CCD06	—	—	—	—	—	—	—	—	—	—	—	SCLA1	—	—
40	P63	CCD07	—	—	—	—	—	—	—	—	—	—	—	SDAA1	—	—
41	P31	—	EI31	(PCLBUZ0)	—	—	—	INTP4	—	TS01	TI03/TO03	—	—	—	—	—
42	P64	—	—	—	—	—	—	—	—	TS12	TI10/TO10	—	—	—	—	—
43	P65	—	—	—	—	—	—	—	—	TS13	TI11/TO11	—	—	—	—	—
44	P66	—	—	—	—	—	—	—	—	TS14	TI12/TO12	—	—	—	—	—
45	P67	—	—	—	—	—	—	—	—	TS15	TI13/TO13	—	—	—	—	—
46	P77	—	—	—	—	—	—	INTP11	KR7	TS09	—	—	(TxD2)	—	—	—
47	P76	—	—	—	—	—	—	INTP10	KR6	TS08	—	—	(RxD2)	—	—	—
48	P75	—	—	—	—	—	—	INTP9	KR5	TS07	—	—	—	—	—	—
49	P74	—	—	—	—	—	—	INTP8	KR4	TS06	—	—	—	—	—	—
50	P73	—	—	—	—	—	—	—	KR3	TS05	—	—	—	—	—	—
51	P72	—	—	—	—	—	—	—	KR2	TS04	—	—	SO21	—	—	—
52	P71	—	—	—	—	—	—	—	KR1	TS03	—	—	SI21/SDA21	—	—	—
53	P70	—	—	—	—	—	—	—	KR0	TS02	—	—	SCK21/SCL21	—	—	RIN0
54	P06	—	—	—	—	—	—	—	—	TS11	—	—	—	—	—	—
55	P05	—	—	—	—	—	—	—	—	TS10	—	—	—	—	—	—
56	—	—	—	EVss1	—	—	—	—	—	—	—	—	—	—	—	—
57	—	—	—	EVDD1	—	—	—	—	—	—	—	—	—	—	—	—
58	P80	—	—	—	—	—	—	—	—	—	—	—	(SCK10)/(SCL10)	—	—	—
59	P81	—	—	—	—	—	—	—	—	—	—	—	(SI10)/(RxD1)/(SDA10)	—	—	—
60	P82	—	—	—	—	—	—	—	—	—	—	—	(SO10)/(TxD1)	—	—	—
61	P83	—	—	—	—	—	—	—	—	—	—	—	—	—	TxDA0	—
62	P84	—	—	—	—	—	—	(INTP6)	—	—	—	—	—	—	RxDA0	—
63	P85	—	—	—	—	—	—	(INTP7)	—	—	—	—	—	—	CLKA0	—
64	P86	—	—	—	—	—	—	(INTP8)	—	—	—	—	—	—	—	—

Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products (3/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	128LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSUL)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
65	P87	—	—	—	—	—	—	(INTP9)	—	—	—	—	—	—	—	—
66	P30	—	EI30	—	—	—	VCOUT0	INTP3	—	TSCAP	—	RTC1HZ	—	—	—	—
67	P50	CCD03	EI50/EO50	—	—	—	—	—	—	TS00	—	—	—	—	—	—
68	P51	CCD02	EI51/EO51	—	—	—	—	—	—	—	—	—	—	—	—	—
69	P52	—	—	—	—	—	—	—	—	—	—	—	SO31	—	—	—
70	P53	—	—	—	—	—	—	—	—	—	—	—	SI31/SDA31	—	—	—
71	P54	—	—	—	—	—	—	—	—	—	—	—	SCK31/SCL31	—	—	—
72	P55	—	—	(PCLBUZ1)	—	—	—	—	—	—	—	—	(SCK00)	—	—	—
73	P56	—	—	—	—	—	—	(INTP1)	—	—	—	—	—	—	—	—
74	P57	—	—	—	—	—	—	(INTP3)	—	—	—	—	—	—	—	—
75	P17	CCD01	EO17	—	—	—	—	—	—	—	TI02/TO02	—	(SO00)/TxD0	—	—	—
76	P16	CCD00	EO16	—	—	—	—	INTP5	—	—	TI01/TO01	—	(SI00)/RxD0	—	—	—
77	P15	—	EO15	—	—	—	—	—	—	—	(TI02)/TO02	—	SCK20/SCL20	—	—	—
78	P14	—	EO14	—	—	—	VCOUT1	—	—	—	(TI03)/TO03	—	SI20/RxD2/SDA20	(SCLA0)	—	—
79	P13	—	EO13	—	—	—	IVREF1	—	—	—	(TI04)/TO04	—	SO20/TxD2	(SDAA0)	—	—
80	P12	—	EI12/EO12	TOOLTxD	—	—	—	(INTP5)	—	—	(TI05)/TO05	—	SO00/TxD0	—	—	—
81	P11	—	EI11/EO11	TOOLRxD	—	—	—	—	—	—	(TI06)/TO06	—	SI00/RxD0/SDA00	—	—	—
82	P10	—	EI10/EO10	—	—	—	—	—	—	—	(TI07)/TO07	—	SCK00/SCL00	—	—	—
83	P90	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
84	P91	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
85	P92	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
86	P93	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
87	P94	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
88	P95	—	—	—	—	—	—	—	—	—	—	—	SCK11/SCL11	—	—	—
89	P96	—	—	—	—	—	—	—	—	—	—	—	SI11/SDA11	—	—	—
90	P97	—	—	—	—	—	—	—	—	—	—	—	SO11	—	—	—
91	P112	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
92	P113	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
93	P114	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products (4/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMs			Timers		Communications Interfaces			
	128LQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
94	P115	—	—	—	ANI26	—	—	—	—	—	—	—	—	—	—	—
95	P116	—	—	—	ANI25	—	—	—	—	—	—	—	—	—	—	—
96	P117	—	—	—	ANI24	—	—	—	—	—	—	—	—	—	—	—
97	P101	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
98	P110	—	—	—	—	—	—	(INTP10)	—	—	—	—	—	—	—	—
99	P111	—	—	—	—	—	—	(INTP11)	—	—	—	—	—	—	—	—
100	P146	—	—	—	—	—	—	(INTP4)	—	—	—	—	—	—	—	—
101	P147	—	EI147	—	ANI18	—	IVCMP0	—	—	—	—	—	—	—	—	—
102	P100	—	—	—	ANI20	—	—	—	—	—	—	—	—	—	—	—
103	P156	—	—	—	ANI14	—	—	—	—	—	—	—	—	—	—	—
104	P155	—	—	—	ANI13	—	—	—	—	TS35	—	—	—	—	—	—
105	P154	—	—	—	ANI12	—	—	—	—	TS34	—	—	—	—	—	—
106	P153	—	—	—	ANI11	—	—	—	—	TS33	—	—	—	—	—	—
107	P152	—	—	—	ANI10	—	—	—	—	TS32	—	—	—	—	—	—
108	P151	—	—	—	ANI9	—	—	—	—	TS31	—	—	—	—	—	—
109	P150	—	—	—	ANI8	—	—	—	—	TS30	—	—	—	—	—	—
110	P27	—	—	—	ANI7	—	—	—	—	TS25	—	—	—	—	—	—
111	P26	—	—	—	ANI6	—	—	—	—	TS24	—	—	—	—	—	—
112	P25	—	—	—	ANI5	—	—	—	—	TS23	—	—	—	—	—	—
113	P24	—	—	—	ANI4	—	—	—	—	TS22	—	—	—	—	—	—
114	P23	—	EI23	—	ANI3	ANO1	IVREF0	—	—	TS21	—	—	—	—	—	—
115	P22	—	EI22	—	ANI2	ANO0	—	—	—	TS20	—	—	—	—	—	—
116	P21	—	EI21	—	ANI1/ AVREFM	—	—	—	—	—	—	—	—	—	—	—
117	P20	—	EI20	—	ANI0/ AVREFP	—	—	—	—	—	—	—	—	—	—	—
118	P130	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
119	P102	—	—	—	—	—	—	—	—	TI06/ TO06	—	—	—	—	—	—
120	P07	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
121	P04	—	—	—	—	—	—	—	—	—	—	—	SCK10/ SCL10	—	—	—
122	P03	—	—	—	ANI16	—	—	—	—	TS29	—	—	SI10/ RxD1/ SDA10	—	—	—
123	P02	—	—	—	ANI17	—	—	—	—	TS28	—	—	SO10/ TxD1	—	—	—
124	P01	—	EI01/ EO01	—	—	—	—	—	—	TS27	TO00	—	—	—	—	—
125	P00	—	EI00	—	—	—	—	—	—	TS26	TI00	—	—	—	—	—
126	P145	—	—	—	—	—	—	—	—	—	TI07/ TO07	—	—	—	—	—

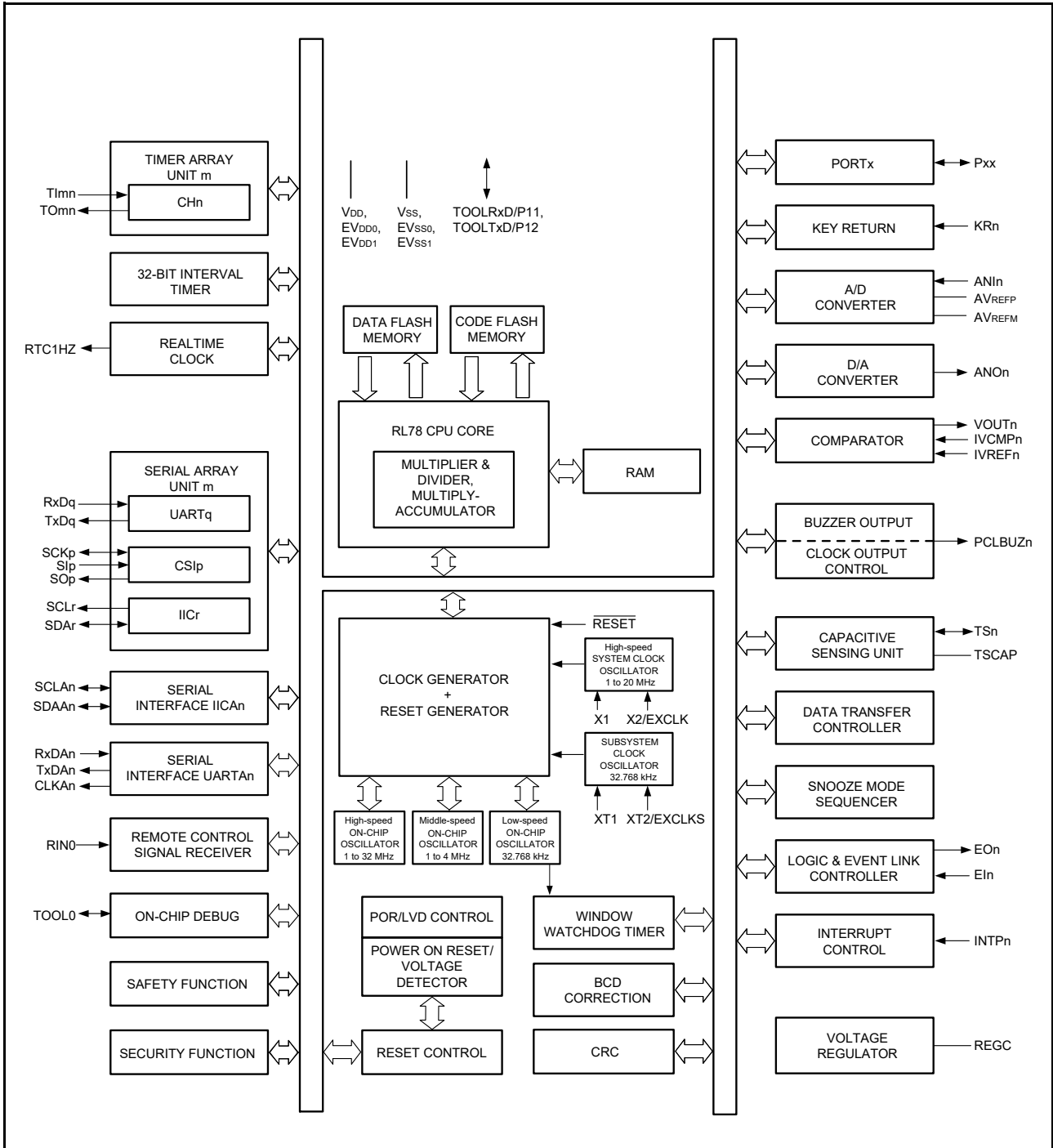
Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products (5/5)

Pin Number	I/O			Power supply, system clock, and debugging	Analog Circuits			HMIs			Timers		Communications Interfaces			
	128LFQFP	Digital port	Output current control port		ELCL input/output port	A/D converter (ADC)	D/A converter (DAC)	Comparator (CMP)	Interrupt (INTP)	Key interrupt (KR)	Capacitive sensing unit (CTSU2L)	Timer array unit (TAU)	Realtime Clock (RTC)	Serial array unit (SAU)	Serial interface IICA (IICA)	Serial interface UARTA (UARTA)
127	P144	—	—	—	—	—	—	—	—	—	—	—	SO30/TxD3	—	—	—
128	P143	—	—	—	—	—	—	—	—	—	—	—	SI30/RxD3/SDA30	—	—	—

1.4 Pin Identification

ANI0 to ANI14,		PCLBUZ0, PCLBUZ1:	Programmable clock output/buzzer output
ANI16 to ANI26:	Analog input		
ANO0, ANO1:	Analog output	REGC:	Regulator capacitance
AVREFM:	Analog reference voltage minus	RESET:	Reset
AVREFP:	Analog reference voltage plus	RIN0:	IR remote controller input
CCD00 to CCD07:	Controlled current drive output	RTC1HZ:	Realtime clock correction clock (1 Hz) output
CLKA0, CLKA1:	Asynchronous serial clock output		
EI00, EI01, EI10 to EI12,		RxD0 to RxD3,	
EI20 to EI23, EI30, EI31,		RxDA0, RxDA1:	Receive data
EI50, EI51,		SCLA0, SCLA1,	
EI120 to EI122,		SCK00, SCK01, SCK10,	
EI137, EI147:	Logic & event link controller input	SCK11, SCK20, SCK21,	
EO01, EO10 to EO17,		SCK30, SCK31:	Serial clock input/output
EO50, EO51,		SCL00, SCL01, SCL10,	
EO60, EO61:	Logic & event link controller output	SCL11, SCL20, SCL21,	
EVDD0, EVDD1:	Power supply for port	SCL30, SCL31:	Serial clock output
EVSS0, EVSS1:	Ground for port	SDAA0, SDAA1, SDA00,	
EXCLK:	External clock input (main system clock)	SDA01, SDA10, SDA11,	
EXCLKS:	External clock input (subsystem clock)	SDA20, SDA21, SDA30,	
INTP0 to INTP11:	Interrupt request from peripheral modules	SDA31:	Serial data input/output
IVCMP0, IVCMP1:	Comparator input	SI00, SI01, SI10, SI11,	
IVREF0, IVREF1:	Comparator reference input	SI20, SI21, SI30, SI31:	Serial data input
KR0 to KR7:	Key return	SO00, SO01, SO10,	
P00 to P07:	Port 0	SO11, SO20, SO21,	
P10 to P17:	Port 1	SO30, SO31:	Serial data output
P20 to P27:	Port 2	TSCAP:	Touch sensor capacitance
P30 to P37:	Port 3	TI00 to TI07, TI10 to TI17:	Timer input
P40 to P47:	Port 4	TO00 to TO07,	
P50 to P57:	Port 5	TO10 to TO17:	Timer output
P60 to P67:	Port 6	TOOL0:	Data input/output for tool
P70 to P77:	Port 7	TOOLRxD, TOOLTxD:	Data input/output for external device
P80 to P87:	Port 8	TS00 to TS15, TS20 to TS35:	Capacitive sensor
P90 to P97:	Port 9	TxD0 to TxD3,	
P100 to P106:	Port 10	TxDA0, TxDA1:	Transmit data
P110 to P117:	Port 11	VBAT:	Battery backup power supply
P120 to P127:	Port 12	VCOU0, VCOU1:	Comparator output
P130, P137:	Port 13	VDD:	Power supply
P140 to P147:	Port 14	VSS:	Ground
P150 to P156:	Port 15	X1, X2:	Crystal oscillator (main system clock)
		XT1, XT2:	Crystal oscillator (subsystem clock)

1.5 Block Diagram



- Caution 1.** 32- to 128-pin products incorporate the remote control signal receiver.
- Caution 2.** 36- to 128-pin products incorporate the serial interface UARTA.
- Caution 3.** 40- to 128-pin products incorporate the key return function.

Remark m: Unit number, n: Channel number, p: CSI number, q: UART number, r: Simplified I²C number, xx: Port number

1.6 Outline of Functions

[30-, 32-, 36-, 40-, 44-, and 48-pin products]

Caution This outline describes the functions at the time when peripheral I/O redirection register (PIOR) is set to 00H.

(1/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Code flash memory		96 to 256 KB	96 to 256 KB	96 to 256 KB	96 to 256 KB	96 to 768 KB	96 to 768 KB
Data flash memory		8 KB	8 KB	8 KB	8 KB	8 KB	8 KB
RAM		12 to 24 KB	12 to 24 KB	12 to 24 KB	12 to 24 KB	12 to 48 KB	12 to 48 KB
Address space		1 MB					
CPU/ peripheral hardware clock frequency (fCLK)	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (V _{DD} = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz ^{Note 1} (V _{DD} = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (V _{DD} = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz ^{Note 1} (V _{DD} = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz ^{Note 2} (V _{DD} = 1.6 to 5.5 V)					
	Subsystem clock	SUB mode: 32.768 kHz (V _{DD} = 1.6 to 5.5 V)					
Main system clock	High-speed system clock (fmx)	1 to 20 MHz					
	High-speed on-chip oscillator clock (fIH)	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz					
	Middle-speed on-chip oscillator clock (fIM)	1 MHz, 2 MHz, 4 MHz					
Subsystem clock	Subsystem clock X (fsx)	32.768 kHz (V _{DD} = 2.4 to 5.5 V)			32.768 kHz (V _{DD} = 1.6 to 5.5 V)		
	Low-speed on-chip oscillator clock (fIL)	32.768 kHz (typ.)					
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)					
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (fIH))					
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc. 					
I/O port	Total number of pins	26	28	32	36	40	44
	CMOS I/O	23 (N-ch open drain I/O [V _{DD} withstand voltage]: 10)	24 (N-ch open drain I/O [V _{DD} withstand voltage]: 10)	28 (N-ch open drain I/O [V _{DD} withstand voltage]: 12)	30 (N-ch open drain I/O [V _{DD} withstand voltage]: 12)	33 (N-ch open drain I/O [V _{DD} withstand voltage]: 12)	36 (N-ch open drain I/O [V _{DD} withstand voltage]: 13)
	CMOS input	1	1	1	3	3	3
	CMOS output	—	—	—	—	—	1
	N-ch open drain I/O (withstand voltage: 6 V)	2	3	3	3	4	4
	Output current control port	6	7	7	7	7	8

(2/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Timers	16-bit timer	8 channels					
	Watchdog timer	1 channel					
	Realtime clock (RTC)	1 channel					
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode					
	Timer output	4 channels (PWM outputs: 3 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4}			5 channels (PWM outputs: 4 ^{Note 3}), 8 channels (PWM outputs: 7 ^{Note 3}) ^{Note 4}		
	RTC output	1 channel					
Clock output/buzzer output		2 channels • 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fsXP))					
8-/10-/12-bit resolution A/D converter		8 channels			9 channels	10 channels	
D/A converter		2 channels					
Comparator		2 channels					
Serial interface		<p>[30- and 32-pin products]</p> <ul style="list-style-type: none"> Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART (UART supporting LIN-bus): 1 channel <p>[36-, 40-, and 44-pin products]</p> <ul style="list-style-type: none"> Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel <p>[48-pin products]</p> <ul style="list-style-type: none"> Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel 					
	UARTA	—			1 channel		2 channels
	I ² C bus	1 channel			2 channels		
Remote control signal receiver		—		1 channel			
Data transfer controller (DTC)		30 sources	30 sources	32 sources	33 sources	35 sources	36 sources
Logic and event link controller (ELCL)		1					
SNOOZE mode sequencer (SMS)		1					
Capacitive sensing unit	ROM size: 96 to 128 KB	2	3	5	6	6	8
	ROM size: 192 to 768 KB	6	7	11	13	14	16
Vectored interrupt sources	Internal	31	32	35	35	39	39
	External	6	6	6	7	7	10
Key interrupt		—			4		6

(3/3)

Item		30-pin	32-pin	36-pin	40-pin	44-pin	48-pin
		R7F100GAx	R7F100GBx	R7F100GCx	R7F100GEx	R7F100GFx	R7F100GGx
Reset		<ul style="list-style-type: none"> • Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution^{Note 5} • Internal reset by RAM parity error • Internal reset by illegal-memory access 					
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)					
Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)					
	LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)					
On-chip debugging		Available (tracing supported)					
Power supply voltage		VDD = 1.6 to 5.5 V					
Operating ambient temperature		TA = -40 to +85°C (2D: Consumer applications), TA = -40 to +105°C (3C: Industrial applications)					

Note 1. Overwrite the flash memory during operation at 2 MHz or a lower frequency.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves). For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G23 User's Manual.

Note 4. This applies when the setting of the PIOR0 bit is 1.

Note 5. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

[52-, 64-, 80-, 100-, and 128-pin products]

Caution This outline describes the functions at the time when peripheral I/O redirection register (PIOR) is set to 00H.

(1/3)

Item		52-pin	64-pin	80-pin	100-pin	128-pin
		R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
Code flash memory		96 to 768 KB	96 to 768 KB	128 to 768 KB	128 to 768 KB	256 to 768 KB
Data flash memory		8 KB	8 KB	8 KB	8 KB	8 KB
RAM		12 to 48 KB	12 to 48 KB	16 to 48 KB	16 to 48 KB	24 to 48 KB
Address space		1 MB				
CPU/ peripheral hardware clock frequency (fCLK)	Main system clock	HS (high-speed main) mode: 1 to 32 MHz (VDD = 1.8 to 5.5 V) HS (high-speed main) mode: 1 to 4 MHz ^{Note 1} (VDD = 1.6 to 5.5 V) LS (low-speed main) mode: 1 to 24 MHz (VDD = 1.8 to 5.5 V) LS (low-speed main) mode: 1 to 4 MHz ^{Note 1} (VDD = 1.6 to 5.5 V) LP (low-power main) mode: 1 to 2 MHz ^{Note 2} (VDD = 1.6 to 5.5 V)				
	Subsystem clock	SUB mode: 32.768 kHz (VDD = 1.6 to 5.5 V)				
Main system clock	High-speed system clock (fMX)	1 to 20 MHz				
	High-speed on-chip oscillator clock (fIH)	1 MHz, 2 MHz, 3 MHz, 4 MHz, 6 MHz, 8 MHz, 12 MHz, 16 MHz, 24 MHz, 32 MHz				
	Middle-speed on-chip oscillator clock (fIM)	1 MHz, 2 MHz, 4 MHz				
Subsystem clock	Subsystem clock X (fSX)	32.768 kHz (VDD = 1.6 to 5.5 V)				
	Low-speed on-chip oscillator clock (fIL)	32.768 kHz (typ.)				
General-purpose registers		8 bits × 32 registers (8 bits × 8 registers × 4 banks)				
Minimum instruction execution time		0.03125 μs (at the 32-MHz operation with the high-speed on-chip oscillator clock (fIH))				
Instruction set		<ul style="list-style-type: none"> • Data transfer (8/16 bits) • Adder and subtractor/logical operation (8/16 bits) • Multiplication (8 bits × 8 bits, 16 bits × 16 bits), division (16 bits ÷ 16 bits, 32 bits ÷ 32 bits) • Multiplication and accumulation (16 bits × 16 bits + 32 bits) • Rotate, barrel shift, and bit manipulation (set, reset, test, and Boolean operation), etc. 				
I/O port	Total number of pins	48	58	74	92	120
	CMOS I/O	40 (N-ch open drain I/O [VDD withstand voltage]: 15)	50 (N-ch open drain I/O [EVDD withstand voltage]: 22 ^{Note 3} / 18 ^{Note 4})	66 (N-ch open drain I/O [EVDD withstand voltage]: 27)	84 (N-ch open drain I/O [EVDD withstand voltage]: 31)	112 (N-ch open drain I/O [EVDD withstand voltage]: 33)
	CMOS input	3	3	3	3	3
	CMOS output	1	1	1	1	1
	N-ch open drain I/O (withstand voltage: 6 V)	4	4	4	4	4
	Output current control port	8	8	8	8	8

(2/3)

Item		52-pin	64-pin	80-pin	100-pin	128-pin
		R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
Timers	16-bit timer	8 channels		12 channels		16 channels
	Watchdog timer	1 channel				
	Realtime clock (RTC)	1 channel				
	32-bit interval timer (TML32)	1 channel in 32-bit counter mode, 2 channels in 16-bit counter mode, 4 channels in 8-bit counter mode				
	Timer output	5 channels (PWM outputs: 4 ^{Note 5}), 8 channels (PWM outputs: 7 ^{Note 5}) ^{Note 6}	8 channels (PWM outputs: 7 ^{Note 5})	12 channels (PWM outputs: 10 ^{Note 5})		16 channels (PWM outputs: 14 ^{Note 5})
	RTC output	1 channel				
Clock output/buzzer output		2 channels				
		<ul style="list-style-type: none"> • 3.91 kHz, 7.81 kHz, 15.63 kHz, 2 MHz, 4 MHz, 8 MHz, 16 MHz (at the 32-MHz operation with the main system clock (fMAIN)) • 256 Hz, 512 Hz, 1.024 kHz, 2.048 kHz, 4.096 kHz, 8.192 kHz, 16.384 kHz, 32.768 kHz (at the 32.768-kHz operation with the low-speed peripheral clock (fsXP)) 				
8-/10-/12-bit resolution A/D converter		12 channels	12 channels	17 channels	20 channels	26 channels
D/A converter		2 channels				
Comparator		2 channels				
Serial interfaces		<p>[52-pin products]</p> <ul style="list-style-type: none"> • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 1 channel/simplified I²C: 1 channel/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel <p>[64-pin products]</p> <ul style="list-style-type: none"> • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel <p>[80-, 100-, and 128-pin products]</p> <ul style="list-style-type: none"> • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART (UART supporting LIN-bus): 1 channel • Simplified SPI (CSI): 2 channels/simplified I²C: 2 channels/UART: 1 channel 				
	UARTA	2 channels				
	I ² C bus	2 channels				
Remote control signal receiver		1 channel				
Data transfer controller (DTC)		36 sources	37 sources	39 sources		
Logic and event link controller (ELCL)		1				
SNOOZE mode sequencer (SMS)		1				
Capacitive sensing unit	ROM size: 96 to 128 KB	10	12	30	32	32
	ROM size: 192 to 768 KB	20	22	30	32	32
Vectored interrupt sources	Internal	39	39	44	44	48
	External	12	13	13	13	13
Key interrupt		8				

(3/3)

Item		52-pin	64-pin	80-pin	100-pin	128-pin
		R7F100GJx	R7F100GLx	R7F100GMx	R7F100GPx	R7F100GSx
Reset		<ul style="list-style-type: none"> • Reset by RESET pin • Internal reset by watchdog timer • Internal reset by power-on-reset • Internal reset by voltage detectors (LVD0 and LVD1) • Internal reset by illegal instruction execution^{Note 7} • Internal reset by RAM parity error • Internal reset by illegal-memory access 				
Power-on-reset circuit		Detection voltage • 1.50 V (typ.)				
Voltage detector	LVD0	Detection voltage • Rising edge: 1.69 V to 3.96 V (6 stages) • Falling edge: 1.65 V to 3.88 V (6 stages)				
	LVD1	Detection voltage • Rising edge: 1.67 V to 4.16 V (18 stages) • Falling edge: 1.63 V to 4.08 V (18 stages)				
On-chip debugging		Available (tracing supported)				
Power supply voltage		VDD = 1.6 to 5.5 V				
Operating ambient temperature		TA = -40 to +85°C (2D: Consumer applications), TA = -40 to +105°C (3C: Industrial applications)				

Note 1. Overwrite the flash memory during operation at 2 MHz or a lower frequency.

Note 2. When the flash memory is to be overwritten, switch to high-speed main (HS) mode or low-speed main (LS) mode.

Note 3. This only applies to the products with 96- and 128-Kbyte flash memory.

Note 4. This only applies to the products with 192- to 768-Kbyte flash memory.

Note 5. The number of PWM outputs varies depending on the setting of channels in use (the number of masters and slaves).
For details, see **7.9.3 Operation for the multiple PWM output function** in the RL78/G23 User's Manual.

Note 6. This applies when the setting of the PIOR0 bit is 1.

Note 7. In normal operation, executing the instruction code FFH triggers an internal reset, but this is not the case during emulation by the on-chip debugging emulator.

2. Electrical Characteristics

This section describes the electrical characteristics of the following products.

- 2D: Consumer applications, $T_A = -40$ to $+85^\circ\text{C}$
R7F100Gxx2Dxx
- 3C: Industrial applications, $T_A = -40$ to $+105^\circ\text{C}$
R7F100Gxx3Cxx

- Caution 1.** RL78 microcontrollers have on-chip debugging functionality for use in the development and evaluation of user systems. Do not use on-chip debugging with products designated as part of mass production, because using this function may cause the guaranteed number of times the flash memory is rewritten to be exceeded, and product reliability therefore cannot be guaranteed. Renesas Electronics is not liable for problems occurring when on-chip debugging is used with products designated as part of mass production.
- Caution 2.** For the consumer application products, the ambient operating temperature of $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ applies.
- Caution 3.** For products that do not have an EVDD0, EVDD1, EVSS0, or EVSS1 pin, read EVDD0 and EVDD1 as VDD, and EVSS0 and EVSS1 as Vss.
- Caution 4.** The present pins differ depending on the products. For details, see section 2.1 Functions of Port Pins through section 2.2.1 Functions for each product in the RL78/G23 User's Manual.

2.1 Absolute Maximum Ratings

(1/2)

Item	Symbols	Conditions	Ratings	Unit
Supply voltage	VDD		-0.5 to +6.5	V
	EVDD0, EVDD1	EVDD0 = EVDD1	-0.5 to +6.5	V
	EVSS0, EVSS1	EVSS0 = EVSS1	-0.5 to +0.3	V
REGC pin input voltage	VIREGC	REGC	-0.3 to +2.1 and -0.3 to VDD + 0.3 ^{Note 1}	V
Input voltage	Vi1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 ^{Note 2}	V
	Vi2	P60 to P63 (N-ch open-drain)	-0.3 to +6.5	V
	Vi3	P20 to P27, P121 to P124, P137, P150 to P156, EXCLK, EXCLKS, $\overline{\text{RESET}}$	-0.3 to VDD + 0.3 ^{Note 2}	V
Output voltage	VO1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-0.3 to EVDD0 + 0.3 and -0.3 to VDD + 0.3 ^{Note 2}	V
	VO2	P20 to P27, P121, P122, P150 to P156	-0.3 to VDD + 0.3 ^{Note 2}	V
Analog input voltage	VAI1	ANI16 to ANI26	-0.3 to EVDD0 + 0.3 and -0.3 to AVREFP + 0.3 Notes 2, 3	V
	VAI2	ANI0 to ANI14	-0.3 to VDD + 0.3 and -0.3 to AVREFP + 0.3 Notes 2, 3	V

Note 1. Connect the REGC pin to Vss via a capacitor (0.47 to 1 μF). The listed value is the absolute maximum rating of the REGC pin. Only use the capacitor connection. Do not apply a specific voltage to this pin.

Note 2. This voltage must be no higher than 6.5 V.

Note 3. The voltage on a pin in use for A/D conversion must not exceed AVREFP + 0.3.

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark 1. The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

Remark 2. AVREFP refers to the positive reference voltage of the A/D converter.

Remark 3. The reference voltage is Vss.

(2/2)

Item	Symbols	Conditions		Ratings	Unit
High-level output current	IOH1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	-40	mA
		Total of all pins -170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	-70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	-100	mA
	IOH2	Per pin	P20 to P27, P121, P122, P150 to P156	-5	mA
		Total of all pins		-20	mA
Low-level output current	IOL1	Per pin	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	40 ^{Note}	mA
		Total of all pins 170 mA	P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145	70	mA
			P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147	100	mA
	IOL2	Per pin	P20 to P27, P121, P122, P150 to P156	10	mA
		Total of all pins		20	mA
Ambient operating temperature	TA	In normal operation mode	3C: Industrial applications	-40 to +105	°C
			2D: Consumer applications		
		In flash memory programming mode	3C: Industrial applications	-40 to +105	
			2D: Consumer applications		
Storage temperature	T _{stg}			-65 to +150	°C

Note The rating for the following port pins is 80 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P110 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

Caution Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.2 Characteristics of the Oscillators

2.2.1 Characteristics of the X1 oscillator

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
X1 clock oscillation allowable input cycle time ^{Note}	Ceramic resonator/ crystal resonator		0.05		1	μs

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

Caution Since the CPU is started by the high-speed on-chip oscillator clock after release from the reset state, the user should use the oscillation stabilization time counter status register (OSTC) to check the X1 clock oscillation stabilization time. Specify the values for the oscillation stabilization time in the OSTC register and the oscillation stabilization time select register (OSTS) after having sufficiently evaluated the oscillation stabilization time with the resonator to be used.

2.2.2 Characteristics of the XT1 oscillator

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ for the 30- to 36-pin products, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$ for the 40- to 128-pin products, $V_{SS} = 0\text{ V}$)

Item	Resonator	Conditions	Min.	Typ.	Max.	Unit
XT1 clock oscillation frequency (f_{XT}) ^{Note}	Crystal resonator			32.768		kHz

Note The listed time and frequency indicate permissible ranges of the oscillator. For actual applications, request evaluation by the manufacturer of the oscillator circuit mounted on a board so you can use appropriate values. Refer to AC Characteristics for instruction execution time.

2.2.3 Characteristics of the On-chip Oscillators

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator clock frequency	f _H			1		32	MHz
High-speed on-chip oscillator clock frequency accuracy ^{Note 1}		HIPREC = 1	+85 to +105°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-2.0	+2.0	%
				1.6 V ≤ V _{DD} ≤ 5.5 V	-6.0	+6.0	%
			-20 to +85°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.0	+1.0	%
				1.6 V ≤ V _{DD} ≤ 5.5 V	-5.0	+5.0	%
			-40 to -20°C	1.8 V ≤ V _{DD} ≤ 5.5 V	-1.5	+1.5	%
				1.6 V ≤ V _{DD} ≤ 5.5 V	-5.5	+5.5	%
HIPREC = 0 ^{Note 2}			-15		0	%	
High-speed on-chip oscillator clock correction resolution					0.05		%
Middle-speed on-chip oscillator clock frequency ^{Note 3}	f _M			1		4	MHz
Middle-speed on-chip oscillator clock frequency accuracy ^{Note 1}				-12		+12	%
Middle-speed on-chip oscillator clock correction resolution					0.15		%
Middle-speed on-chip oscillator frequency temperature coefficient						±0.17 ^{Note 4}	%/°C
Low-speed on-chip oscillator clock frequency ^{Note 3}	f _L				32.768		kHz
Low-speed on-chip oscillator clock frequency accuracy ^{Note 1}				-15		+15	%
Low-speed on-chip oscillator clock correction resolution					0.3		%
Low-speed on-chip oscillator frequency temperature coefficient						±0.21 ^{Note 4}	%/°C

Note 1. The accuracy values were obtained in testing of this product.

Note 2. The listed condition applies when the setting of the FRQSEL3 bit is 1.

Note 3. The listed values only indicate the characteristics of the oscillators. Refer to AC Characteristics for instruction execution time.

Note 4. Guaranteed by characterization results.

2.3 DC Characteristics

2.3.1 Pin characteristics

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(1/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Allowable high-level output current ^{Note 1}	IOH1	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			-10.0 Note 2	mA
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			-55.0 Note 4	mA
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			-10.0	mA
			$1.8\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			-5.0	mA
			$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$			-2.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			-80.0 Note 5	mA
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$			-19.0	mA
			$1.8\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$			-10.0	mA
			$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$			-5.0	mA
		Total of all pins (when duty $\leq 70\%$ ^{Note 3})	$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			-135.0 Note 6	mA
	IOH2	Per pin for P20 to P27, P121, P122, P150 to P156	$4.0\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$			-3.0 Note 2	mA
			$2.7\text{ V} \leq \text{VDD} < 4.0\text{ V}$			-1.0 Note 2	mA
			$1.8\text{ V} \leq \text{VDD} < 2.7\text{ V}$			-1.0 Note 2	mA
			$1.6\text{ V} \leq \text{VDD} < 1.8\text{ V}$			-0.5 Note 2	mA
		Total of all pins (when duty $\leq 70\%$ ^{Note 3})	$4.0\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$			-20.0	mA
			$2.7\text{ V} \leq \text{VDD} < 4.0\text{ V}$			-10.0	mA
			$1.8\text{ V} \leq \text{VDD} < 2.7\text{ V}$			-5.0	mA
			$1.6\text{ V} \leq \text{VDD} < 1.8\text{ V}$			-5.0	mA

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from the EVDD0, EVDD1, or VDD pin to an output pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = $(\text{IOH} \times 0.7)/(n \times 0.01)$

Example when $n = 80\%$ and $\text{IOH} = -10.0\text{ mA}$

Total output current from the listed pins = $(-10.0 \times 0.7)/(80 \times 0.01) \approx -8.7\text{ mA}$

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

(Notes, Caution, and Remark continue on the next page.)

- Note 4.** The maximum value is -30 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.
- Note 5.** The maximum value is -50 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.
- Note 6.** The maximum values are respectively -100 mA and -60 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of -40°C to +85°C and of +85°C to +105°C.
- Caution** **The following pins are not capable of the output of high-level signals in the N-ch open-drain mode.**
P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144
- Remark** The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Allowable low-level output current ^{Note 1}	IOL1	Per pin for P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147			20.0 Notes 2, 3	mA	
		Per pin for P60 to P63			15.0 Note 2	mA	
		Total of P00 to P04, P07, P32 to P37, P40 to P47, P102 to P106, P120, P125 to P127, P130, P140 to P145 (when duty ≤ 70% ^{Note 4})	4.0 V ≤ EVDD0 ≤ 5.5 V			70.0 Note 5	mA
			2.7 V ≤ EVDD0 < 4.0 V			15.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			9.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			4.5	mA
		Total of P05, P06, P10 to P17, P30, P31, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100, P101, P110 to P117, P146, P147 (when duty ≤ 70% ^{Note 4})	4.0 V ≤ EVDD0 ≤ 5.5 V			80.0 Note 5	mA
			2.7 V ≤ EVDD0 < 4.0 V			35.0	mA
			1.8 V ≤ EVDD0 < 2.7 V			20.0	mA
			1.6 V ≤ EVDD0 < 1.8 V			10.0	mA
	Total of all pins (when duty ≤ 70% ^{Note 4})				150.0 Note 6	mA	
	IOL2	Per pin for P20 to P27, P121, P122, P150 to P156	4.0 V ≤ VDD ≤ 5.5 V			8.5 Note 2	mA
			2.7 V ≤ VDD < 4.0 V			1.5 Note 2	mA
			1.8 V ≤ VDD < 2.7 V			0.6 Note 2	mA
			1.6 V ≤ VDD < 1.8 V			0.4 Note 2	mA
		Total of all pins (when duty ≤ 70% ^{Note 4})	4.0 V ≤ VDD ≤ 5.5 V			20	mA
			2.7 V ≤ VDD < 4.0 V			20	mA
1.8 V ≤ VDD < 2.7 V					15	mA	
1.6 V ≤ VDD < 1.8 V					10	mA	

Note 1. Device operation is guaranteed at the listed currents even if current is flowing from an output pin to the EVSS0, EVSS1, or VSS pin.

Note 2. The combination of these and other pins must also not exceed the value for maximum total current.

Note 3. The maximum rating for the following port pins is 40 mA when IOL1 = 40.0 mA is specified by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin package products

Note 4. The listed currents apply when the duty cycle is no greater than 70%. Use the following formula to calculate the output current when the duty cycle is greater than 70%, where n is the duty cycle.

- Total output current from the listed pins = (IOL × 0.7)/(n × 0.01)

Example when n = 80% and IOL = 10.0 mA

Total output current from the listed pins = (10.0 × 0.7)/(80 × 0.01) ≈ 8.7 mA

Note that the duty cycle has no effect on the current that is allowed to flow into a single pin. A current higher than the absolute maximum rating must not flow into a single pin.

(Notes and Remark continue on the next page.)

Note 5. The maximum value is 40 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.

Note 6. The maximum value is 80 mA in the products for industrial applications (R7F100Gxx3Cxx) with an ambient operating temperature range of +85°C to +105°C.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(3/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input voltage, high	VIH1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0.8 EVDD0		EVDD0	V
	VIH2	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	2.2		EVDD0	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	2.0		EVDD0	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	1.5		EVDD0	V
	VIH3	P20 to P27, P150 to P156		0.7 VDD		VDD	V
	VIH4	P60 to P63		0.7 EVDD0		6.0	V
VIH5	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0.8 VDD		VDD	V	
Input voltage, low	UIL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	Normal input buffer	0		0.2 EVDD0	V
	UIL2	P01, P03, P04, P10, P11, P13 to P17, P43, P44, P53 to P55, P80, P81, P142, P143	TTL input buffer 4.0 V ≤ EVDD0 ≤ 5.5 V	0		0.8	V
			TTL input buffer 3.3 V ≤ EVDD0 < 4.0 V	0		0.5	V
			TTL input buffer 1.6 V ≤ EVDD0 < 3.3 V	0		0.32	V
	UIL3	P20 to P27, P150 to P156		0		0.3 VDD	V
	UIL4	P60 to P63		0		0.3 EVDD0	V
UIL5	P121 to P124, P137, EXCLK, EXCLKS, $\overline{\text{RESET}}$		0		0.2 VDD	V	

Caution The maximum value of VIH of pins P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144 is EVDD0, even in the N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(4/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output voltage, high	VOH1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -10.0 mA	EVDD0 - 1.5		V
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -3.0 mA	EVDD0 - 0.7		V
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -2.0 mA	EVDD0 - 0.6		V
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOH1 = -1.5 mA	EVDD0 - 0.5		V
			1.6 V ≤ EVDD0 < 5.5 V, IOH1 = -1.0 mA	EVDD0 - 0.5		V
	VOH2	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ VDD ≤ 5.5 V, IOH2 = -3.0 mA	VDD - 0.7		V
			2.7 V ≤ VDD < 4.0 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.8 V ≤ VDD < 2.7 V, IOH2 = -1.0 mA	VDD - 0.5		V
			1.6 V ≤ VDD < 1.8 V, IOH2 = -0.5 mA	VDD - 0.5		V

Caution P00, P02 to P04, P10 to P15, P17, P34, P42 to P45, P50, P52 to P55, P71, P72, P74, P80 to P83, P96, P120, and P142 to P144 do not output high-level signals in the N-ch open-drain mode.

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(5/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit		
Output voltage, low	VOL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P130, P140 to P147	4.0 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 20.0 mA		1.3	V	
				IOL1 = 40.0 mA ^{Note}		1.3	V	
				4.0 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 8.5 mA		0.7	V
					IOL1 = 17.0 mA ^{Note}		0.7	V
				2.7 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 3.0 mA		0.6	V
					IOL1 = 6.0 mA ^{Note}		0.6	V
				2.7 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 1.5 mA		0.4	V
					IOL1 = 3.0 mA ^{Note}		0.4	V
				1.8 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 0.6 mA		0.4	V
					IOL1 = 1.2 mA ^{Note}		0.4	V
				1.6 V ≤ EVDD0 ≤ 5.5 V	IOL1 = 0.3 mA		0.4	V
					IOL1 = 0.6 mA ^{Note}		0.4	V
	VOL2	P20 to P27, P121, P122, P150 to P156	4.0 V ≤ VDD ≤ 5.5 V, IOL2 = 8.5 mA			0.7	V	
			2.7 V ≤ VDD < 4.0 V, IOL2 = 1.5 mA			0.5	V	
			1.8 V ≤ VDD < 2.7 V, IOL2 = 0.6 mA			0.4	V	
			1.6 V ≤ VDD < 1.8 V, IOL2 = 0.4 mA			0.4	V	
	VOL3	P60 to P63	4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 15.0 mA			2.0	V	
			4.0 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 5.0 mA			0.4	V	
			2.7 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 3.0 mA			0.4	V	
			1.8 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 2.0 mA			0.4	V	
1.6 V ≤ EVDD0 ≤ 5.5 V, IOL3 = 1.0 mA					0.4	V		

Note The listed value applies when IOL1 = 40.0 mA is specified for the following port pins by the 40-mA port output control register (PTDC).

- Pins P04, P10, and P120 of the 64- to 100-pin package products with 384- to 768-Kbyte flash ROM
- Pin P101 of the 100-pin package products with 384- to 768-Kbyte flash ROM
- Pins P17 and P51 of the 30- to 52-pin package products
- Pin P70 of the 32- to 52-pin products

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(6/7)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Output current ^{Note}	CCDIOL	P16, P17, P50, P51, P60 to P63	CCSm = 01H	4.0 V ≤ EVDD0 ≤ 5.5 V	1.0	1.8	2.6	mA
				2.7 V ≤ EVDD0 < 4.0 V	0.8	1.5	2.3	mA
			CCSm = 02H	4.0 V ≤ EVDD0 ≤ 5.5 V	3.0	4.9	6.5	mA
				3.0 V ≤ EVDD0 < 4.0 V	2.7	4.3	5.9	mA
			CCSm = 03H	4.0 V ≤ EVDD0 ≤ 5.5 V	6.6	10.0	13.2	mA
				3.3 V ≤ EVDD0 < 4.0 V	6.0	9.1	12.1	mA
		P60 to P63	CCSm = 04H	4.0 V ≤ EVDD0 ≤ 5.5 V	10.2	15.0	19.8	mA
				3.3 V ≤ EVDD0 < 4.0 V	9.4	13.8	18.2	mA

Note The listed currents apply when the output current control function is enabled.

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(7/7)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input leakage current, high	ILI1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	VI = EVDD0			0.5	μA
	ILI2	P20 to P27, P137, P150 to P156, RESET	VI = VDD			0.5	μA
	ILI3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VDD			0.5	μA
Input leakage current, low	ILIL1	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P60 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120, P125 to P127, P140 to P147	VI = EVSS0			-0.5	μA
	ILIL2	P20 to P27, P137, P150 to P156, RESET	VI = VSS			-0.5	μA
	ILIL3	P121 to P124 (X1, X2, XT1, XT2, EXCLK, EXCLKS)	VI = VSS			-0.5	μA
On-chip pll-up resistance	RU	P00 to P07, P10 to P17, P30 to P37, P40 to P47, P50 to P57, P64 to P67, P70 to P77, P80 to P87, P90 to P97, P100 to P106, P110 to P117, P120 to P122, P125 to P127, P140 to P147	VI = EVSS0, In input port	10	20	100	kΩ

Remark The characteristics of functions multiplexed on a given pin are the same as those for the port pin unless otherwise specified.

2.3.2 Supply current characteristics

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit				
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	V _{DD} = 5.0 V	1.3	—	mA				
						V _{DD} = 1.8 V	1.3	—					
					Normal operation	V _{DD} = 5.0 V	3.0	5.0	mA				
						V _{DD} = 1.8 V	3.0	5.0					
						LS (low-speed main) mode	f _{IH} = 24 MHz ^{Note 2}	Normal operation		V _{DD} = 5.0 V	2.3	3.8	mA
										V _{DD} = 1.8 V	2.3	3.8	
			Normal operation	f _{IH} = 16 MHz ^{Note 2}	V _{DD} = 5.0 V	1.7	2.7	mA					
					V _{DD} = 1.8 V	1.7	2.7						
			Normal operation	f _{IM} = 4 MHz ^{Note 3}	V _{DD} = 5.0 V	0.4	0.7	mA					
					V _{DD} = 1.6 V	0.4	0.7						
			LP (low-power main) mode	f _{IM} = 2 MHz ^{Note 3}	Normal operation	V _{DD} = 5.0 V	200	325	μA				
						V _{DD} = 1.6 V	200	325					
				Normal operation	f _{IM} = 1 MHz ^{Note 3}	V _{DD} = 5.0 V	112	178	μA				
						V _{DD} = 1.6 V	111	176					
			HS (high-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	V _{DD} = 5.0 V	1.9	3.2	mA				
						V _{DD} = 1.8 V	1.9	3.2					
			LS (low-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	V _{DD} = 5.0 V	1.8	3.0	mA				
						V _{DD} = 1.8 V	1.7	3.0					
				Normal operation	f _{MX} = 20 MHz ^{Note 4} , Resonator connection	V _{DD} = 5.0 V	1.9	3.2	mA				
						V _{DD} = 1.8 V	1.9	3.2					
				Normal operation	f _{MX} = 10 MHz ^{Note 4} , Square wave input	V _{DD} = 5.0 V	0.9	1.6	mA				
						V _{DD} = 1.8 V	0.9	1.6					
				Normal operation	f _{MX} = 10 MHz ^{Note 4} , Resonator connection	V _{DD} = 5.0 V	1.0	1.7	mA				
						V _{DD} = 1.8 V	1.0	1.7					
Normal operation	f _{MX} = 8 MHz ^{Note 4} , Square wave input	V _{DD} = 5.0 V	0.8	1.3	mA								
		V _{DD} = 1.8 V	0.7	1.3									
Normal operation	f _{MX} = 8 MHz ^{Note 4} , Resonator connection	V _{DD} = 5.0 V	0.9	1.4	mA								
		V _{DD} = 1.8 V	0.8	1.4									

Note 1. The listed currents are the total currents flowing into V_{DD} and EV_{DD0}, including the input leakage currents flowing when the level of the input pin is fixed to V_{DD}, EV_{DD0} or V_{SS}, EV_{SS0}. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 3. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(Note and Remarks are listed on the next page.)

<R>

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_H: High-speed on-chip oscillator clock frequency

Remark 2. f_M: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fsUB = 32.768 kHz ^{Note 2} , Low-speed on-chip oscillator operation	Normal operation	TA = -40°C		3.2	5.5	μA
						TA = +25°C		3.5	5.8	
						TA = +50°C		3.8	8.5	
						TA = +70°C		4.4	13.8	
						TA = +85°C		5.3	22.1	
				TA = +105°C		7.7	40.9			
				fsUB = 32.768 kHz ^{Note 3} , Square wave input	Normal operation	TA = -40°C		3.2	5.6	μA
						TA = +25°C		3.4	5.7	
						TA = +50°C		3.7	8.5	
						TA = +70°C		4.3	13.7	
						TA = +85°C		5.2	21.4	
				TA = +105°C		7.6	39.0			
				fsUB = 32.768 kHz ^{Note 3} , Resonator connection	Normal operation	TA = -40°C		3.2	5.2	μA
						TA = +25°C		3.4	5.4	
						TA = +50°C		3.7	7.7	
TA = +70°C		4.3	13.4							
TA = +85°C		5.2	20.9							
TA = +105°C		7.7	38.5							

<R> **Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.

<R> **Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

<R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. fIL: Low-speed on-chip oscillator clock frequency

Remark 2. fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz Note 3	VDD = 5.0 V		0.54	1.93	mA
					VDD = 1.8 V		0.53	1.92	
			LS (low-speed main) mode	f _{IH} = 24 MHz Note 3	VDD = 5.0 V		0.45	1.50	mA
					VDD = 1.8 V		0.44	1.49	
				f _{IH} = 16 MHz Note 3	VDD = 5.0 V		0.45	1.19	mA
					VDD = 1.8 V		0.44	1.18	
				f _{IM} = 4 MHz Note 4	VDD = 5.0 V		0.08	0.26	mA
					VDD = 1.6 V		0.08	0.26	
			LP (low-power main) mode	f _{IM} = 2 MHz Note 4	VDD = 5.0 V		33	120	μA
					VDD = 1.6 V		33	120	
				f _{IM} = 1 MHz Note 4	VDD = 5.0 V		29	76	μA
					VDD = 1.6 V		28	74	
			HS (high-speed main) mode	f _{MX} = 20 MHz Note 5 , Square wave input	VDD = 5.0 V		0.22	1.07	mA
					VDD = 1.8 V		0.19	1.03	
			LS (low-speed main) mode	f _{MX} = 20 MHz Note 5 , Square wave input	VDD = 5.0 V		0.22	1.07	mA
					VDD = 1.8 V		0.19	1.03	
				f _{MX} = 20 MHz Note 5 , Resonator connection	VDD = 5.0 V		0.40	1.28	mA
					VDD = 1.8 V		0.39	1.27	
				f _{MX} = 10 MHz Note 5 , Square wave input	VDD = 5.0 V		0.14	0.57	mA
					VDD = 1.8 V		0.12	0.54	
				f _{MX} = 10 MHz Note 5 , Resonator connection	VDD = 5.0 V		0.24	0.69	mA
					VDD = 1.8 V		0.23	0.68	
				f _{MX} = 8 MHz Note 5 , Square wave input	VDD = 5.0 V		0.12	0.47	mA
					VDD = 1.8 V		0.10	0.44	
f _{MX} = 8 MHz Note 5 , Resonator connection	VDD = 5.0 V		0.21	0.58	mA				
	VDD = 1.8 V		0.20	0.57					

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the "Typ." column do not include the operating currents of the peripheral modules.
- The currents in the "Max." column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_H: High-speed on-chip oscillator clock frequency

Remark 2. f_M: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/4)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fsUB = 32.768 kHz>Note 3, Low-speed on-chip oscillator operation	TA = -40°C		0.53	2.31	μA
					TA = +25°C		0.65	2.38	
					TA = +50°C		0.80	4.95	
					TA = +70°C		1.17	9.97	
					TA = +85°C		1.78	17.96	
					TA = +105°C		4.41	37.71	
				fsUB = 32.768 kHz, Square wave input Note 4	TA = -40°C		0.20	1.97	μA
					TA = +25°C		0.29	2.00	
					TA = +50°C		0.54	5.33	
					TA = +70°C		0.99	10.94	
					TA = +85°C		1.70	19.62	
					TA = +105°C		4.10	41.82	
				fsUB = 32.768 kHz, Resonator connection Note 5	TA = -40°C		0.21	2.04	μA
					TA = +25°C		0.33	2.28	
					TA = +50°C		0.49	4.98	
	TA = +70°C		1.05		11.36				
	TA = +85°C		1.76		20.04				
	TA = +105°C		4.20		42.52				
	IDD3	STOP mode	RAMSDS = 0>Note 6	TA = -40°C		0.15	1.45	μA	
				TA = +25°C		0.23	1.45		
				TA = +50°C		0.45	4		
TA = +70°C					0.9	9			
TA = +85°C					1.6	17			
TA = +105°C					4	35			
RAMSDS = 1>Note 7				TA = -40°C		0.14	1.45	μA	
				TA = +25°C		0.21	1.45		
				TA = +50°C		0.4	3.5		
				TA = +70°C		0.8	8.5		
				TA = +85°C		1.4	15		
				TA = +105°C		3.2	30		
RAMSDS = 1, 128-Hz realtime clock operation>Note 8				TA = -40°C		0.22	1.53	μA	
				TA = +25°C		0.32	1.56		
				TA = +50°C		0.53	3.62		
	TA = +70°C		0.94	8.64					
	TA = +85°C		1.55	15.15					
	TA = +105°C		3.40	30.20					

(Notes and Remarks are listed on the next page.)

- <R> **Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode or the STOP mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- <R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
- <R> **Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.
- <R> **Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).
- <R> **Note 6.** The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.
- <R> **Note 7.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.
- <R> **Note 8.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.
- Remark 1.** fIL: Low-speed on-chip oscillator clock frequency
- Remark 2.** fSUB: Subsystem clock frequency (XT1 clock oscillation frequency)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V		1.4	—	mA
						VDD = 1.8 V		1.4	—	
				Normal operation	VDD = 5.0 V		3.0	5.0	mA	
					VDD = 1.8 V		3.0	5.0		
			LS (low-speed main) mode	f _{IH} = 24 MHz ^{Note 2}	Normal operation	VDD = 5.0 V		2.3	3.8	mA
						VDD = 1.8 V		2.3	3.8	
				f _{IH} = 16 MHz ^{Note 2}	Normal operation	VDD = 5.0 V		1.7	2.8	mA
				VDD = 1.8 V		1.7	2.7			
			f _{IM} = 4 MHz ^{Note 3}	Normal operation	VDD = 5.0 V		0.4	0.7	mA	
					VDD = 1.6 V		0.4	0.7		
		LP (low-power main) mode	f _{IM} = 2 MHz ^{Note 3}	Normal operation	VDD = 5.0 V		203	329	μA	
					VDD = 1.6 V		202	328		
			f _{IM} = 1 MHz ^{Note 3}	Normal operation	VDD = 5.0 V		115	181	μA	
					VDD = 1.6 V		114	180		
		HS (high-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V		1.9	3.2	mA	
					VDD = 1.8 V		1.9	3.2		
		LS (low-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V		1.8	3.0	mA	
					VDD = 1.8 V		1.7	3.0		
			f _{MX} = 20 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V		1.9	3.2	mA	
					VDD = 1.8 V		1.9	3.2		
f _{MX} = 10 MHz ^{Note 4} , Square wave input	Normal operation		VDD = 5.0 V		0.9	1.6	mA			
			VDD = 1.8 V		0.9	1.6				
f _{MX} = 10 MHz ^{Note 4} , Resonator connection	Normal operation		VDD = 5.0 V		1.0	1.7	mA			
			VDD = 1.8 V		1.0	1.7				
f _{MX} = 8 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V		0.8	1.3	mA				
		VDD = 1.8 V		0.7	1.3					
f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V		0.9	1.4	mA				
		VDD = 1.8 V		0.8	1.4					

- <R>
- Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.
- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
 - The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- Note 2.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

(Note and Remarks are listed on the next page.)

Note 4. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Remark 1. f_H: High-speed on-chip oscillator clock frequency

Remark 2. f_M: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(2/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fsUB = 32.768 kHzNote 2, Low-speed on-chip oscillator operation	Normal operation	TA = -40°C		3.3	6.1	μA
						TA = +25°C		3.6	6.3	
						TA = +50°C		3.9	9.6	
						TA = +70°C		4.5	15.9	
						TA = +85°C		5.4	25.3	
				TA = +105°C		7.8	56.3			
				fsUB = 32.768 kHzNote 3, Square wave input	Normal operation	TA = -40°C		3.3	6.1	μA
						TA = +25°C		3.5	6.4	
						TA = +50°C		3.8	9.6	
						TA = +70°C		4.4	16.1	
		TA = +85°C				5.3	26.4			
		fsUB = 32.768 kHzNote 3, Resonator connection	Normal operation	TA = -40°C		3.3	6.0	μA		
				TA = +25°C		3.5	6.0			
				TA = +50°C		3.8	8.9			
				TA = +70°C		4.4	15.3			
TA = +85°C				5.3	25.6					
TA = +105°C		7.9	55.3							

<R> **Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.

<R> **Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

<R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. fIL: Low-speed on-chip oscillator clock frequency

Remark 2. fsUB: Subsystem clock frequency (XT1 clock oscillation frequency)

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current ^{Note 1}	IDD2 ^{Note 2}	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 3}	VDD = 5.0 V		0.57	1.97	mA
					VDD = 1.8 V		0.56	1.96	
			LS (low-speed main) mode	f _{IH} = 24 MHz ^{Note 3}	VDD = 5.0 V		0.47	1.53	mA
					VDD = 1.8 V		0.47	1.52	
				f _{IH} = 16 MHz ^{Note 3}	VDD = 5.0 V		0.48	1.22	mA
					VDD = 1.8 V		0.47	1.21	
				f _{IM} = 4 MHz ^{Note 4}	VDD = 5.0 V		0.08	0.27	mA
					VDD = 1.6 V		0.08	0.26	
			LP (low-power main) mode	f _{IM} = 2 MHz ^{Note 4}	VDD = 5.0 V		38	126	μA
					VDD = 1.6 V		37	125	
				f _{IM} = 1 MHz ^{Note 4}	VDD = 5.0 V		32	79	μA
					VDD = 1.6 V		32	79	
			HS (high-speed main) mode	f _{MX} = 20 MHz ^{Note 5} , Square wave input	VDD = 5.0 V		0.23	1.07	mA
					VDD = 1.8 V		0.19	1.03	
			LS (low-speed main) mode	f _{MX} = 20 MHz ^{Note 5} , Square wave input	VDD = 5.0 V		0.23	1.07	mA
					VDD = 1.8 V		0.19	1.03	
				f _{MX} = 20 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.41	1.30	mA
					VDD = 1.8 V		0.40	1.28	
				f _{MX} = 10 MHz ^{Note 5} , Square wave input	VDD = 5.0 V		0.14	0.57	mA
					VDD = 1.8 V		0.12	0.54	
				f _{MX} = 10 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.24	0.69	mA
					VDD = 1.8 V		0.23	0.68	
				f _{MX} = 8 MHz ^{Note 5} , Square wave input	VDD = 5.0 V		0.12	0.47	mA
					VDD = 1.8 V		0.10	0.44	
f _{MX} = 8 MHz ^{Note 5} , Resonator connection	VDD = 5.0 V		0.21	0.58	mA				
	VDD = 1.8 V		0.20	0.57					

<R>

Note 1. The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.

- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
- The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.

Note 2. The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.

Note 3. The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 4. The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.

Note 5. The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

Remark 1. f_H: High-speed on-chip oscillator clock frequency

Remark 2. f_M: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = 0 V)

(4/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fSUB = 32.768 kHz>Note 3, Low-speed on-chip oscillator operation	TA = -40°C		0.62	2.94	μA
					TA = +25°C		0.74	3.00	
					TA = +50°C		0.88	6.00	
					TA = +70°C		1.22	12.01	
					TA = +85°C		2.69	22.92	
					TA = +105°C		5.08	54.47	
				fSUB = 32.768 kHz, Square wave input>Note 4	TA = -40°C		0.25	2.54	μA
					TA = +25°C		0.37	2.73	
					TA = +50°C		0.74	7.35	
					TA = +70°C		1.33	15.13	
					TA = +85°C		2.35	27.33	
					TA = +105°C		4.81	62.95	
				fSUB = 32.768 kHz, Resonator connection>Note 5	TA = -40°C		0.27	2.68	μA
					TA = +25°C		0.39	2.87	
					TA = +50°C		0.78	7.63	
					TA = +70°C		1.34	15.20	
					TA = +85°C		2.35	27.33	
					TA = +105°C		4.67	61.97	
	IDD3	STOP mode	RAMSDS = 0>Note 6	TA = -40°C		0.19	2.00	μA	
				TA = +25°C		0.30	2.00		
				TA = +50°C		0.65	5.00		
TA = +70°C					1.20	11.00			
TA = +85°C					2.20	20.00			
TA = +105°C					4.50	50.00			
RAMSDS = 1>Note 7				TA = -40°C		0.18	2.00	μA	
				TA = +25°C		0.29	2.00		
				TA = +50°C		0.60	4.50		
				TA = +70°C		1.10	10.00		
RAMSDS = 1, 128-Hz realtime clock operation>Note 8				TA = -40°C		0.23	2.05	μA	
				TA = +25°C		0.40	2.11		
			TA = +50°C		0.72	4.62			
			TA = +70°C		1.23	10.13			
			TA = +85°C		2.14	19.14			
	TA = +105°C		4.16	45.16					

(Notes and Remarks are listed on the next page.)

- <R> **Note 1.** The listed currents are the total currents flowing into VDD and EVDD0, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0 or VSS, EVSS0. In the subsystem clock operation mode or the STOP mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- <R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
- <R> **Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.
- <R> **Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).
- <R> **Note 6.** The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.
- <R> **Note 7.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.
- <R> **Note 8.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.
- Remark 1.** f_{IL}: Low-speed on-chip oscillator clock frequency
- Remark 2.** f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (1/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD1	Operating mode	HS (high-speed main) mode	f _{IH} = 32 MHz ^{Note 2}	Basic operation	VDD = 5.0 V	1.6	—	mA
						VDD = 1.8 V	1.5	—	
					Normal operation	VDD = 5.0 V	3.5	5.6	mA
						VDD = 1.8 V	3.5	5.6	
			LS (low-speed main) mode	f _{IH} = 24 MHz ^{Note 2}	Normal operation	VDD = 5.0 V	2.6	4.2	mA
						VDD = 1.8 V	2.6	4.2	
				f _{IH} = 16 MHz ^{Note 2}	Normal operation	VDD = 5.0 V	2.0	3.1	mA
						VDD = 1.8 V	1.9	3.1	
				f _{IM} = 4 MHz ^{Note 3}	Normal operation	VDD = 5.0 V	0.5	0.9	mA
						VDD = 1.6 V	0.5	0.8	
		LP (low-power main) mode	f _{IM} = 2 MHz ^{Note 3}	Normal operation	VDD = 5.0 V	229	361	μA	
					VDD = 1.6 V	227	358		
			f _{IM} = 1 MHz ^{Note 3}	Normal operation	VDD = 5.0 V	128	197	μA	
					VDD = 1.6 V	125	193		
		HS (high-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V	2.2	3.5	mA	
					VDD = 1.8 V	2.2	3.5		
		LS (low-speed main) mode	f _{MX} = 20 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V	2.1	3.4	mA	
					VDD = 1.8 V	2.0	3.3		
			f _{MX} = 20 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	2.2	3.6	mA	
					VDD = 1.8 V	2.2	3.5		
f _{MX} = 10 MHz ^{Note 4} , Square wave input	Normal operation		VDD = 5.0 V	1.1	1.8	mA			
			VDD = 1.8 V	1.1	1.8				
f _{MX} = 10 MHz ^{Note 4} , Resonator connection	Normal operation		VDD = 5.0 V	1.2	1.9	mA			
			VDD = 1.8 V	1.2	1.9				
f _{MX} = 8 MHz ^{Note 4} , Square wave input	Normal operation	VDD = 5.0 V	0.9	1.5	mA				
		VDD = 1.8 V	0.9	1.5					
f _{MX} = 8 MHz ^{Note 4} , Resonator connection	Normal operation	VDD = 5.0 V	1.0	1.6	mA				
		VDD = 1.8 V	1.0	1.6					

- <R> **Note 1.** The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.
- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
 - The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- Note 2.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- (Remarks are listed on the next page.)

Remark 1. f_H: High-speed on-chip oscillator clock frequency

Remark 2. f_M: Middle-speed on-chip oscillator clock frequency

Remark 3. f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (2/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD1	Operating mode	Subsystem clock operation mode	fs _{SUB} = 32.768 kHz ^{Note 2} , Low-speed on-chip oscillator operation	Normal operation	TA = -40°C		3.8	7.7	μA
						TA = +25°C		4.1	8.0	
						TA = +50°C		4.6	13.5	
						TA = +70°C		5.6	24.0	
						TA = +85°C		7.1	40.8	
				TA = +105°C		11.1	88.8			
				fs _{SUB} = 32.768 kHz ^{Note 3} , Square wave input	Normal operation	TA = -40°C		3.8	7.7	μA
						TA = +25°C		4.0	8.0	
						TA = +50°C		4.5	13.6	
						TA = +70°C		5.3	24.1	
						TA = +85°C		6.7	40.3	
				TA = +105°C		10.7	88.1			
				fs _{SUB} = 32.768 kHz ^{Note 3} , Resonator connection	Normal operation	TA = -40°C		3.8	7.4	μA
						TA = +25°C		4.1	7.8	
						TA = +50°C		4.5	12.6	
TA = +70°C		5.4	24.2							
TA = +85°C		6.8	39.8							
TA = +105°C		10.8	87.4							

<R> **Note 1.** The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. In the subsystem clock operation mode, the currents in both the "Typ." and "Max." columns do not include the operating currents of the peripheral modules.

<R> **Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.

<R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, middle-speed on-chip oscillator, and low-speed on-chip oscillator are stopped, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).

Remark 1. fil: Low-speed on-chip oscillator clock frequency

Remark 2. fs_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (3/4)

Item	Symbol	Conditions				Min.	Typ.	Max.	Unit
Supply current Note 1	IDD2 Note 2	HALT mode	HS (high-speed main) mode	f _{IH} = 32 MHz Note 3	VDD = 5.0 V		0.60	2.00	mA
					VDD = 1.8 V		0.59	1.99	
			LS (low-speed main) mode	f _{IH} = 24 MHz Note 3	VDD = 5.0 V		0.49	1.56	mA
					VDD = 1.8 V		0.48	1.55	
				f _{IH} = 16 MHz Note 3	VDD = 5.0 V		0.49	1.24	mA
					VDD = 1.8 V		0.48	1.23	
				f _{IM} = 4 MHz Note 4	VDD = 5.0 V		0.09	0.28	mA
					VDD = 1.6 V		0.09	0.27	
			LP (low-power main) mode	f _{IM} = 2 MHz Note 4	VDD = 5.0 V		40	129	μA
					VDD = 1.6 V		37	125	
				f _{IM} = 1 MHz Note 4	VDD = 5.0 V		33	80	μA
					VDD = 1.6 V		32	79	
			HS (high-speed main) mode	f _{MX} = 20 MHz Note 5, Square wave input	VDD = 5.0 V		0.25	1.10	mA
					VDD = 1.8 V		0.21	1.05	
			LS (low-speed main) mode	f _{MX} = 20 MHz Note 5, Square wave input	VDD = 5.0 V		0.25	1.10	mA
					VDD = 1.8 V		0.21	1.05	
				f _{MX} = 20 MHz Note 5, Resonator connection	VDD = 5.0 V		0.41	1.30	mA
					VDD = 1.8 V		0.40	1.28	
				f _{MX} = 10 MHz Note 5, Square wave input	VDD = 5.0 V		0.15	0.59	mA
					VDD = 1.8 V		0.13	0.55	
				f _{MX} = 10 MHz Note 5, Resonator connection	VDD = 5.0 V		0.25	0.70	mA
					VDD = 1.8 V		0.24	0.69	
				f _{MX} = 8 MHz Note 5, Square wave input	VDD = 5.0 V		0.13	0.48	mA
					VDD = 1.8 V		0.11	0.45	
f _{MX} = 8 MHz Note 5, Resonator connection	VDD = 5.0 V		0.22	0.59	mA				
	VDD = 1.8 V		0.21	0.58					

- <R> **Note 1.** The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. The following points apply in the HS (high-speed main), LS (low-speed main), and LP (low-power main) modes.
- The currents in the “Typ.” column do not include the operating currents of the peripheral modules.
 - The currents in the “Max.” column include the operating currents of the peripheral modules, except for those flowing into the A/D converter, LVD circuit, I/O port, and on-chip pull-up/pull-down resistors, and those flowing while the data flash memory is being rewritten.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- Note 3.** The listed currents apply when the high-speed system clock, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 4.** The listed currents apply when the high-speed on-chip oscillator, high-speed system clock, low-speed on-chip oscillator, and subsystem clock are stopped.
- Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, low-speed on-chip oscillator, and subsystem clock are stopped.

(Remarks are listed on the next page.)

- Remark 1.** f_H: High-speed on-chip oscillator clock frequency
- Remark 2.** f_M: Middle-speed on-chip oscillator clock frequency
- Remark 3.** f_{MX}: High-speed system clock frequency (X1 clock oscillation frequency or external main system clock frequency)
- Remark 4.** The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products

<R> (TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V) (4/4)

Item	Symbol	Conditions			Min.	Typ.	Max.	Unit	
Supply current Note 1	IDD2 Note 2	HALT mode	Subsystem clock operation mode	fsUB = 32.768 kHz>Note 3, Low-speed on-chip oscillator operation	TA = -40°C		0.62	3.95	μA
					TA = +25°C		0.78	4.00	
					TA = +50°C		1.03	9.16	
					TA = +70°C		1.62	19.34	
					TA = +85°C		3.50	37.35	
					TA = +105°C		6.77	85.36	
				fsUB = 32.768 kHz, Square wave input>Note 4	TA = -40°C		0.25	3.55	μA
					TA = +25°C		0.41	3.73	
					TA = +50°C		0.90	10.93	
					TA = +70°C		1.76	23.42	
					TA = +85°C		2.92	41.07	
					TA = +105°C		6.27	94.30	
				fsUB = 32.768 kHz, Resonator connection>Note 5	TA = -40°C		0.27	3.62	μA
					TA = +25°C		0.43	3.87	
					TA = +50°C		0.92	11.07	
					TA = +70°C		1.79	23.63	
					TA = +85°C		2.94	41.21	
					TA = +105°C		6.28	94.37	
	IDD3	STOP mode	RAMSDS = 0>Note 6	TA = -40°C		0.21	3.00	μA	
				TA = +25°C		0.35	3.00		
				TA = +50°C		0.75	8.00		
TA = +70°C					1.60	18.00			
TA = +85°C					2.80	34.00			
TA = +105°C					6.00	80.00			
RAMSDS = 1>Note 7				TA = -40°C		0.19	3.00	μA	
				TA = +25°C		0.32	3.00		
				TA = +50°C		0.65	7.00		
				TA = +70°C		1.25	17.00		
				TA = +85°C		2.10	30.00		
				TA = +105°C		4.50	70.00		
RAMSDS = 1, 128-Hz realtime clock operation>Note 8			TA = -40°C		0.27	3.08	μA		
			TA = +25°C		0.42	3.10			
			TA = +50°C		0.76	7.11			
	TA = +70°C		1.38	17.13					
	TA = +85°C		2.23	30.13					
	TA = +105°C		4.64	70.14					

(Notes and Remarks are listed on the next page.)

- <R> **Note 1.** The listed currents are the total currents flowing into VDD, EVDD0 and EVDD1, including the input leakage currents flowing when the level of the input pin is fixed to VDD, EVDD0, EVDD1 or VSS, EVSS0, EVSS1. In the subsystem clock operation mode or the STOP mode, the currents in both the “Typ.” and “Max.” columns do not include the operating currents of the peripheral modules.
- Note 2.** The listed currents apply when the HALT instruction has been fetched from the flash memory for execution.
- <R> **Note 3.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and subsystem clock are stopped.
- <R> **Note 4.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped.
- <R> **Note 5.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, high-speed system clock, and low-speed on-chip oscillator are stopped, and the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1).
- <R> **Note 6.** The listed currents with this setting allow retention of the contents of the entire RAM area. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped. For the current for operation of the subsystem clock in the STOP mode, refer to that in the HALT mode.
- <R> **Note 7.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator and subsystem clock oscillation are stopped.
- <R> **Note 8.** The listed currents with this setting allow retention of the contents of a specified 4-Kbyte area of the RAM. The listed currents apply when the low-speed on-chip oscillator is stopped, the setting of RTCLPC is 1, and the low power consumption oscillation 3 is specified (AMPHS1, AMPHS0 = 1, 1). The current flowing into the RTC is included.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{SUB}: Subsystem clock frequency (XT1 clock oscillation frequency)

4. Peripheral Functions (Common to all products)

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-speed on-chip oscillator operating current	IFIH Note 1				380		μA
Middle-speed on-chip oscillator operating current	IFIM Note 1				20		μA
Low-speed on-chip oscillator operating current	IFIL Note 1				0.3		μA
RTC operating current	IRTC Notes 1, 2, 3	fRTCCLK = 32.768 kHz			0.005		μA
		fRTCCLK = 128 Hz			0.002		μA
32-bit interval timer operating current	IIT Notes 1, 2, 4				0.04		μA
Watchdog timer operating current	IWDTC Notes 1, 2, 5	fIL = 32.768 kHz (typ.)			0.32		μA
A/D converter operating current	IADC Notes 1, 6	When conversion at maximum speed	Normal mode, AVREFP = VDD = 5.0 V		0.95	1.6	mA
			Low voltage mode, AVREFP = VDD = 3.0 V		0.5	0.75	mA
AVREFP current	IADREF Note 7	AVREFP = 5.0 V			52		μA
A/D converter internal reference voltage current	IADREF Note 1				114		μA
Temperature sensor operating current	ITMPS Note 1				110		μA
D/A converter operating current	IDAC Notes 1, 8	Per channel			150		μA
Comparator operating current	ICMP Notes 1, 9				6		μA
LVD operating current	ILVD0 Notes 1, 10				0.02		μA
	ILVD1 Notes 1, 10				0.02		μA
Self-programming operating current	IFSP Notes 1, 11				2.5	12.2	mA
Data flash rewrite operating current	IBGO Notes 1, 12				2.5	12.2	mA

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit		
SNOOZE mode sequencer operating current	ISMS Notes 1, 13	f _{IH} = 32 MHz	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.1		mA		
			30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.1				
			44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.4				
		f _{IL} = 32.768 kHz	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.2		μA		
			30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.2				
			44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products		1.6				
SNOOZE operating current	ISNOZ Note 1	f _{IH} =32 MHz	ADC to be in use	The ADC is shifting from the STOP mode to the SNOOZE mode. Note 14		0.6	0.81	mA	
				The ADC is operating in the low-voltage mode. AVREFP = VDD = 3.0 V		1.2	1.56		
				Simplified SPI (CSI)/UART to be in use			0.7	0.92	mA
		SMS Note 15	30- to 64-pin package products with 96- to 128-Kbyte flash ROM		1.6		mA		
				30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM		1.7			
				44- to 80-pin package products with 384- to 768-Kbyte flash ROM, and 100- to 128-pin package products		2.0			
Remote control signal receiver operating current	I _{REM} Notes 1, 16				0.03		μA		
Low-speed peripheral clock supply current	I _{SXP} Notes 1, 17	RTCLPC = 0			0.22		μA		
Output current control operating current	IC _{CCA} Notes 1, 18	The setting of the CCDE register is not 00H.			100		μA		
		IC _{CDP} Notes 19, 20	Per single output current control port	Setting of the low-level output current: Hi-Z		30		μA	
				Setting of the low-level output current: 2 to 15 mA		200		μA	
Operating current of the true random number generator	I _{TRNG} Note 1				1.1		mA		

(Notes and Remarks continue on the next page.)

- Note 1.** This current flows into VDD.
- Note 2.** The listed currents apply when the high-speed on-chip oscillator, middle-speed on-chip oscillator, and high-speed system clock are stopped.
- Note 3.** This current flows into the realtime clock (RTC). It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IRTC, when the realtime clock is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current. IDD2 in the subsystem clock operation mode includes the operating current of the realtime clock.
- Note 4.** This current only flows to the 32-bit interval timer. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IIT, when the 32-bit interval timer is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current.
- Note 5.** This current only flows to the watchdog timer. It includes the operating current of the low-speed on-chip oscillator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and IWDT when the watchdog timer is operating.
- Note 6.** This current only flows to the A/D converter. The supply current of the RL78 microcontrollers is the sum of IDD1 or IDD2 and IADC when the A/D converter is operating or in the HALT mode.
- Note 7.** This current flows into AVREFF.
- Note 8.** This current only flows to the D/A converter. The supply current of the RL78 microcontrollers is the sum of the values of either IDD1 or IDD2, and IDAC, when the D/A converter is operating or in the HALT mode.
- Note 9.** This current only flows to the comparator. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ICMP when the comparator is in operation.
- Note 10.** This current only flows to the LVD circuit. The supply current of the RL78 microcontrollers is the sum of IDD1, IDD2 or IDD3 and ILVD when the LVD circuit is in operation.
- Note 11.** This current only flows during self programming.
- Note 12.** This current only flows while the data flash memory is being rewritten.
- Note 13.** This current only flows into the SNOOZE mode sequencer. Note that the operating current of the low-speed on-chip oscillator and the XT1 oscillator are not included. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and ISMS, when the SNOOZE mode sequencer is operating or in the HALT mode.
- Note 14.** For shift time to the SNOOZE mode, see **23.3.3 SNOOZE mode** in the RL78/G23 User's Manual.
- Note 15.** The listed values apply when the SNOOZE mode sequencer is in normal operation equivalent to IDD1. They do not include the current flowing into the peripheral functions other than the SNOOZE mode sequencer.
- Note 16.** This current flows into the remote control signal receiver. It does not include the operating current of the low-speed on-chip oscillator or the XT1 oscillator. The supply current of the RL78 microcontrollers is the sum of either IDD1 or IDD2, and IIT, when the remote control signal receiver is operating or in the HALT mode. When the low-speed on-chip oscillator is selected, IFIL should be included in the supply current.
- Note 17.** This current is added to the supply current in the HALT mode when the setting of RTCLPC is 0 in the STOP mode, or when the setting of RTCLPC is 0 with the subsystem clock X (fsx) selected as the CPU clock, while the subsystem clock X (fsx) is oscillating.
- Note 18.** This current is added to the supply current when the output voltage control port is set.
- Note 19.** This current does not include the current flowing into the I/O port pins.
- Note 20.** This current only flows to EVDD0 and EVDD1.

Remark 1. f_{IL}: Low-speed on-chip oscillator clock frequency

Remark 2. f_{sx}: Subsystem clock X frequency

Remark 3. f_{CLK}: CPU/peripheral hardware clock frequency

Remark 4. The typical value for the ambient operating temperature (T_A) is +25°C unless otherwise specified.

2.4 AC Characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit	
Instruction cycle (minimum instruction execution time)	TCY	Main system clock (fMAIN) operation	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
			LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.04167		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.25		1	μs
		LP (low-power main) mode	1.6 V ≤ VDD ≤ 5.5 V	0.5		1	μs	
		Subsystem clock (fSUB) operation		1.6 V ≤ VDD ≤ 5.5 V	26.041	30.5	31.3	μs
		In the self programming mode	HS (high-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V	0.03125		1	μs
				1.6 V ≤ VDD ≤ 1.8 V	0.5		1	μs
LS (low-speed main) mode	1.8 V ≤ VDD ≤ 5.5 V		0.04167		1	μs		
	1.6 V ≤ VDD ≤ 1.8 V		0.5		1	μs		
External system clock frequency	fEX	1.8 V ≤ VDD ≤ 5.5 V		1.0		20.0	MHz	
		1.6 V ≤ VDD < 1.8 V		1.0		4.0	MHz	
	fEXS			32		38.4	kHz	
<R> External system clock input high-level width, low-level width	tEXH, tEXL	1.8 V ≤ VDD ≤ 5.5 V		24			ns	
		1.6 V ≤ VDD < 1.8 V		120			ns	
	tEXHS, tEXLS			13.7			μs	
TI00 to TI07, TI10 to TI17 input high-level width, low-level width	tTIH, tTIL			1/fMCK + 10			ns ^{Note}	
TO00 to TO07, TO10 to TO17 output frequency	fTO	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz	
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz	
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz	
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz	
		LP (low-power main) mode	1.6 V ≤ EVDD0 ≤ 5.5 V			2	MHz	
PCLBUZ0, PCLBUZ1 output frequency	fPCL	HS (high-speed main) mode LS (low-speed main) mode	4.0 V ≤ EVDD0 ≤ 5.5 V			16	MHz	
			2.7 V ≤ EVDD0 < 4.0 V			8	MHz	
			1.8 V ≤ EVDD0 < 2.7 V			4	MHz	
			1.6 V ≤ EVDD0 < 1.8 V			2	MHz	
		LP (low-power main) mode	1.6 V ≤ EVDD0 < 1.8 V			2	MHz	
Interrupt input high-level width, low-level width	fINTH, fINTL	INTP0		1.6 V ≤ VDD ≤ 5.5 V	1		μs	
		INTP1 to INTP11		1.6 V ≤ EVDD0 ≤ 5.5 V	1		μs	
Key interrupt input low- level width	fKRH, fKRL	KR0 to KR7		1.8 V ≤ EVDD0 ≤ 5.5 V	250		ns	
				1.6 V ≤ EVDD0 < 1.8 V	1		μs	
RESET low-level width	trSL			10			μs	

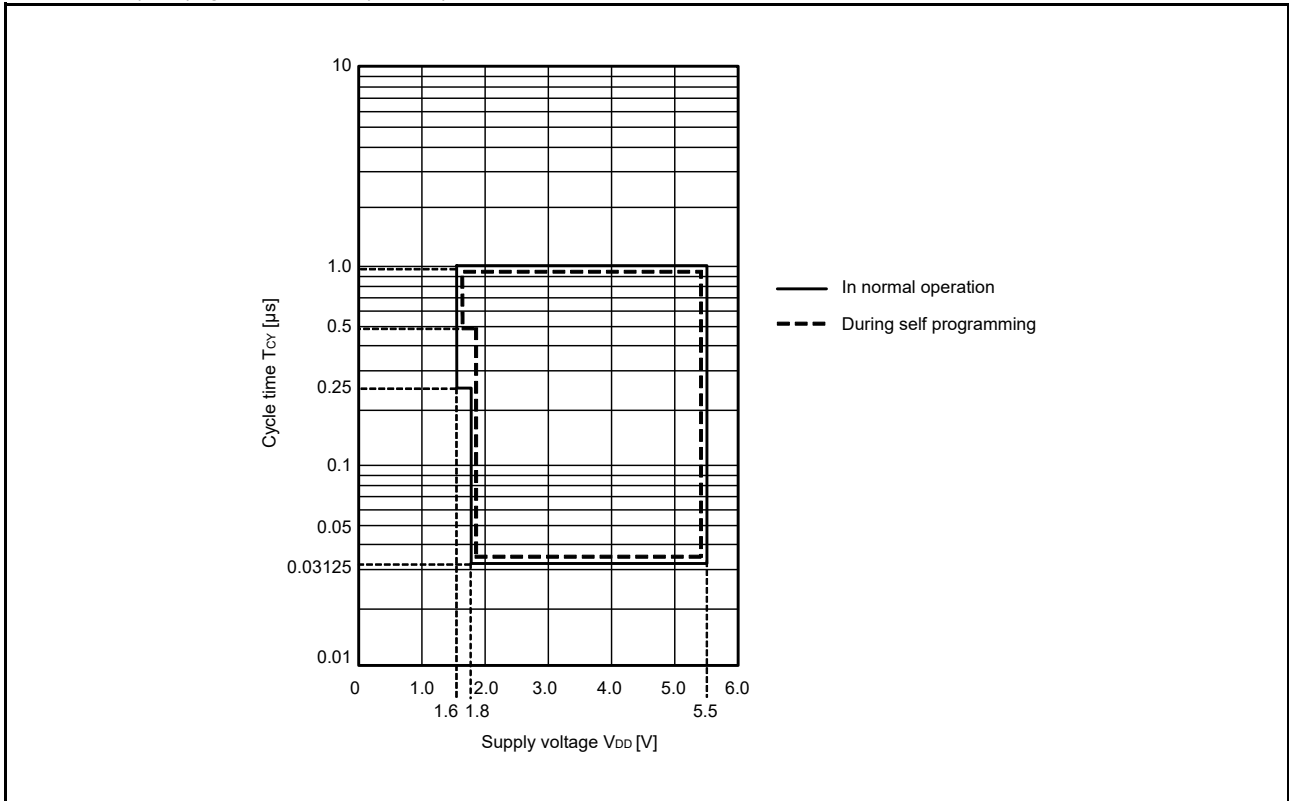
(Note and Remark are listed on the next page.)

Note The following conditions are required for low voltage interface when $EVDD0 < VDD$.
1.8 V \leq EVDD0 < 2.7 V: 125 ns min.
1.6 V \leq EVDD0 < 1.8 V: 250 ns min.

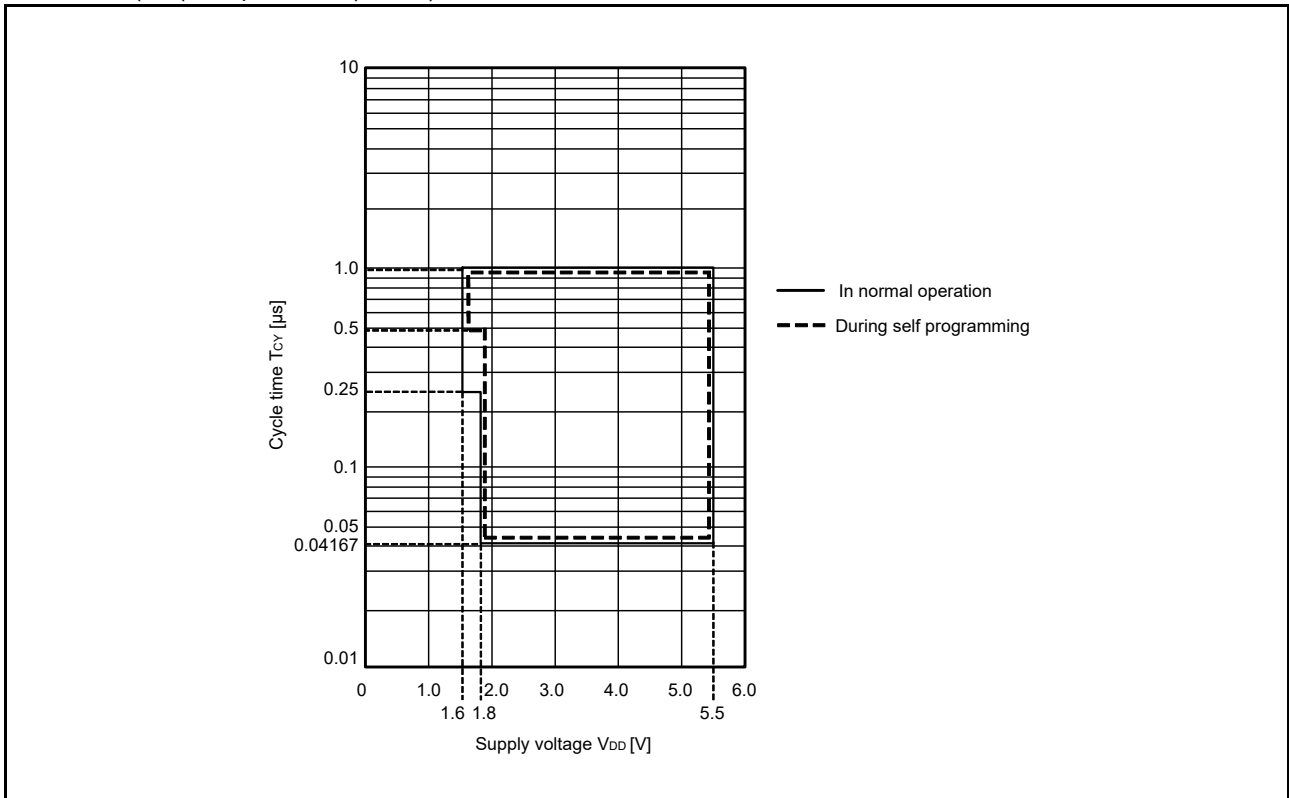
Remark fmck: Timer array unit operating clock frequency
(To set this operating clock, use the CKSmn0 and CKSmn1 bits of the timer mode register mn (TMRmn) (m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7).))

Minimum Instruction Execution Time during Main System Clock Operation

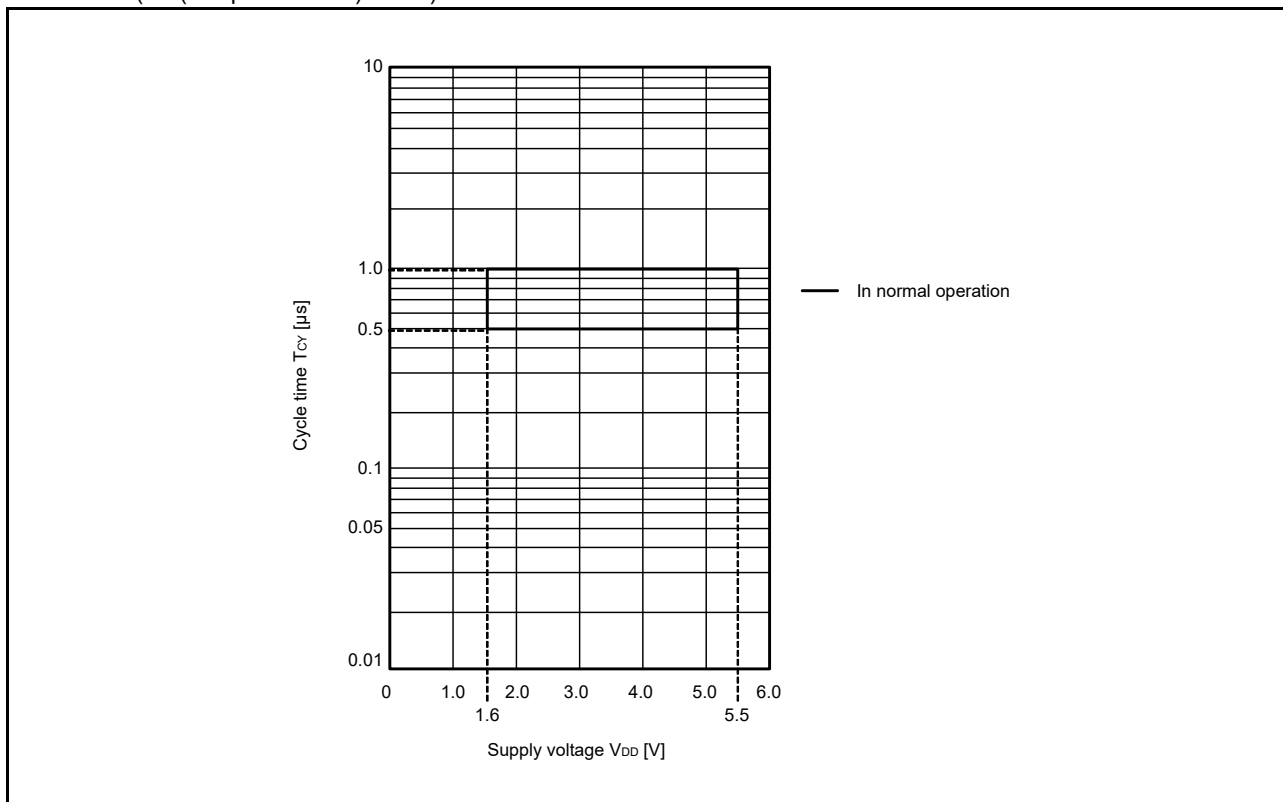
TCY vs VDD (HS (high-speed main) mode)



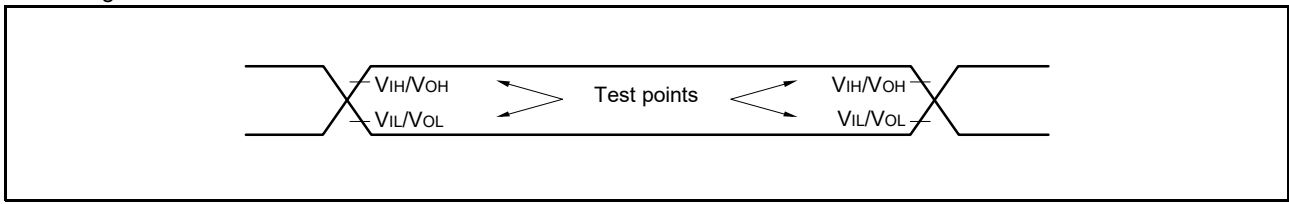
TCY vs VDD (LS (low-speed main) mode)



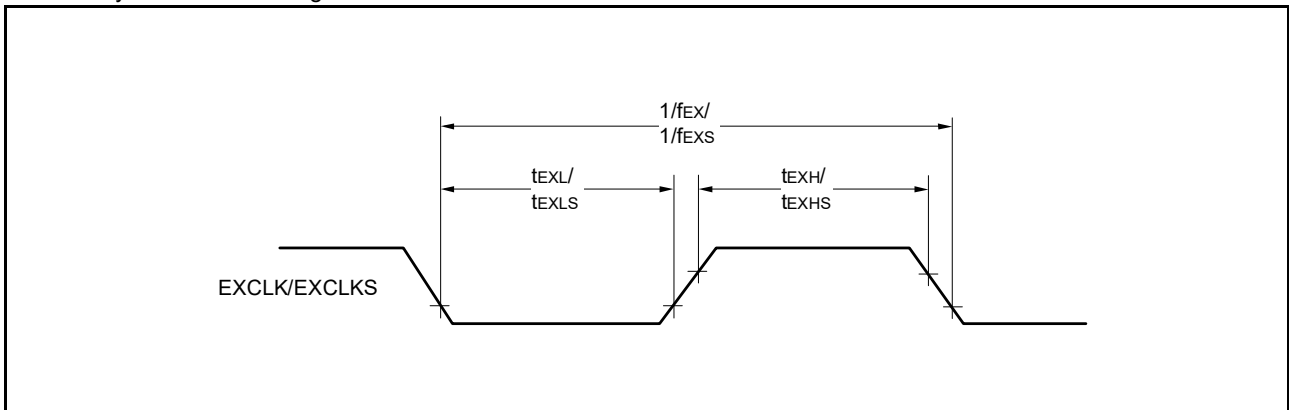
TCY vs VDD (LP (low-power main) mode)



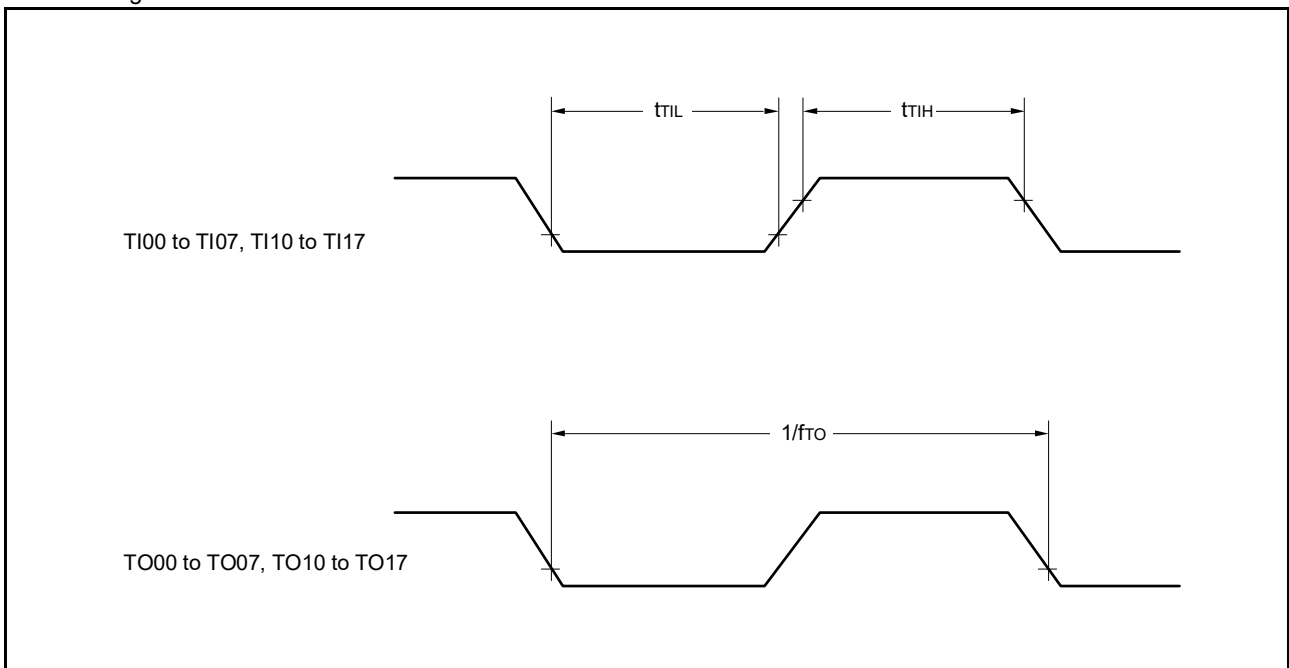
AC Timing Test Points



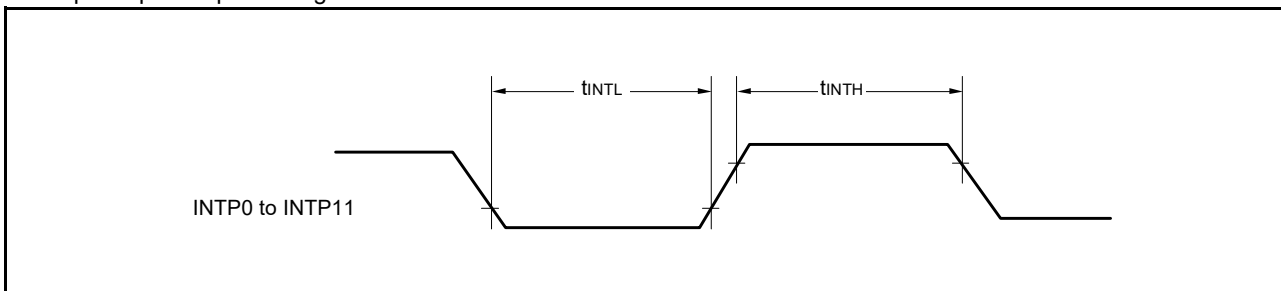
External System Clock Timing



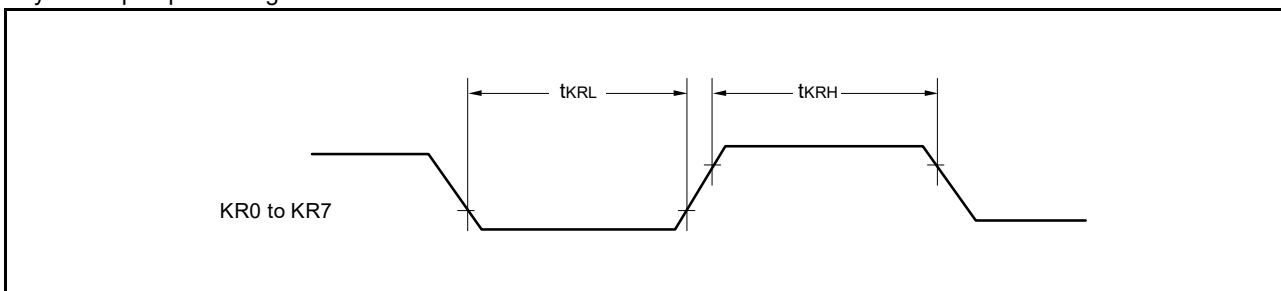
TI/TO Timing



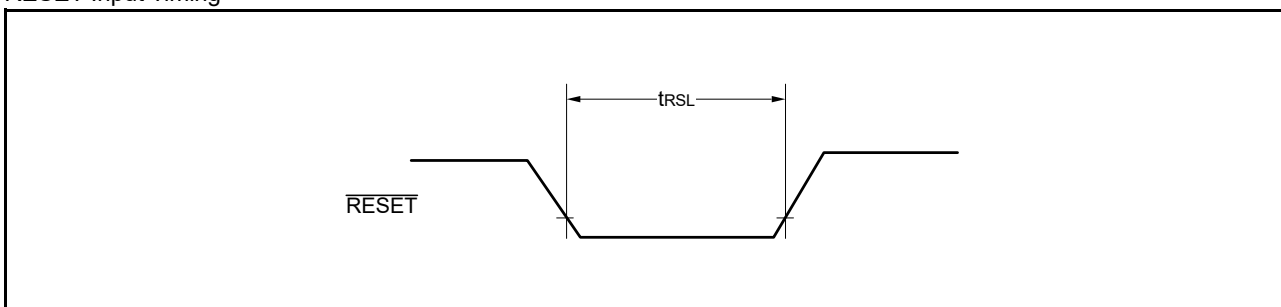
Interrupt Request Input Timing



Key Interrupt Input Timing

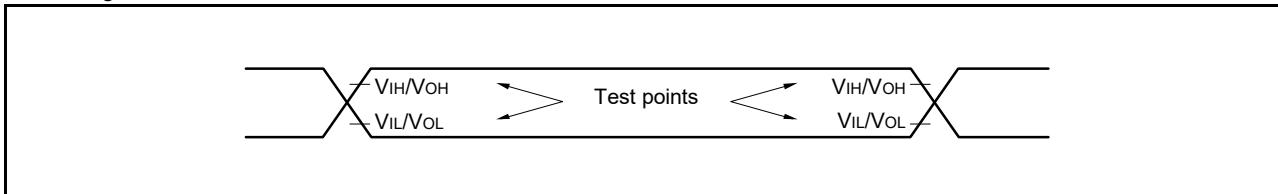


$\overline{\text{RESET}}$ Input Timing



2.5 Characteristics of the Peripheral Functions

AC Timing Test Points



2.5.1 Serial array unit

1. In UART communications with devices operating at same voltage levels

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Transfer rate Note 1		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		fMCK/6 Note 2		fMCK/6 Note 2		fMCK/6	bps
		Theoretical value of the maximum transfer rate fMCK = fCLK Note 3		5.3		4		0.33	Mbps

Note 1. The transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$.

$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: 2.6 Mbps max.

$1.8\text{ V} \leq \text{EVDD0} < 2.4\text{ V}$: 1.3 Mbps max.

$1.6\text{ V} \leq \text{EVDD0} < 1.8\text{ V}$: 0.6 Mbps max.

Note 3. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are as follows.

HS (high-speed main) mode : 32 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

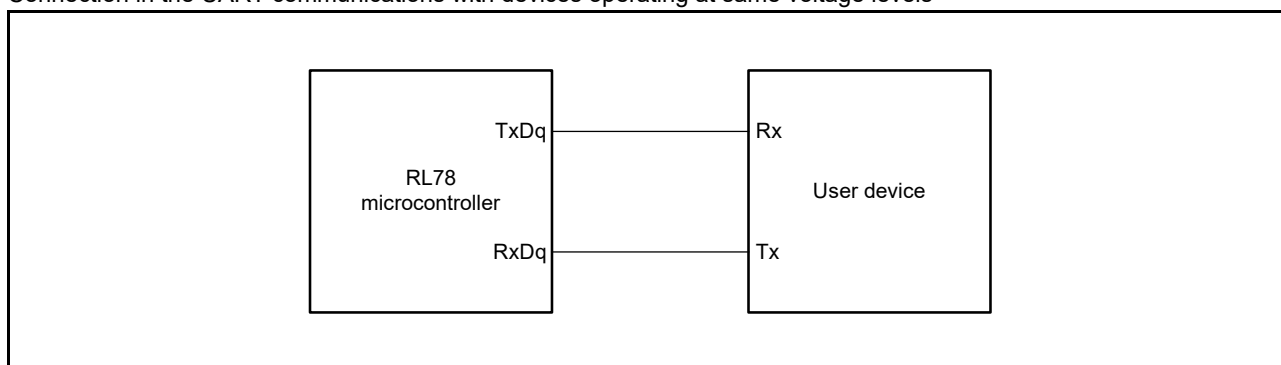
LS (low-speed main) mode : 24 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

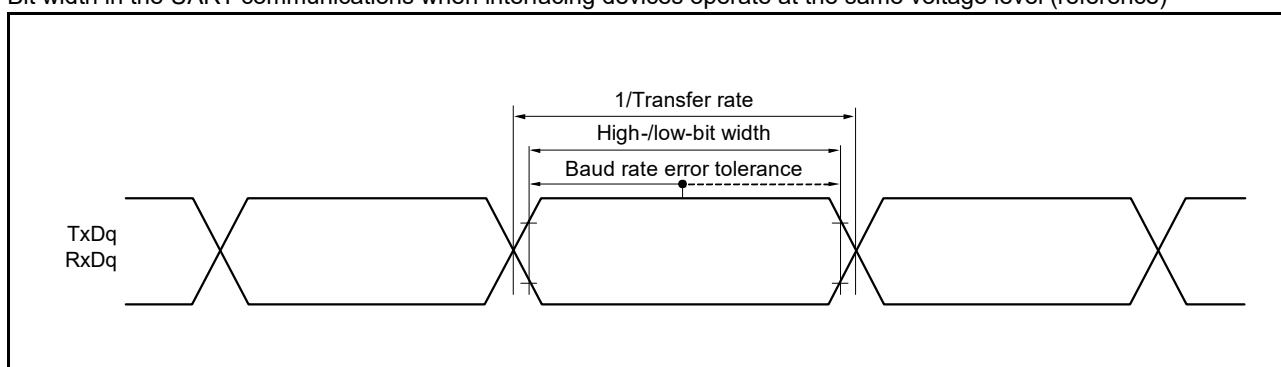
LP (low-power main) mode : 2 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Connection in the UART communications with devices operating at same voltage levels



Bit width in the UART communications when interfacing devices operate at the same voltage level (reference)



- Remark 1.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- Remark 2.** fMCK: Serial array unit operation clock frequency
 (To set this operating clock, set the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13).)

2. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+85^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 \geq 2/fCLK 4.0 V \leq EVDD0 \leq 5.5 V	62.5		83.3		1000		ns
			83.3		125		1000		ns
SCKp high-/ low-level width	tkH1, tkL1	4.0 V \leq EVDD0 \leq 5.5 V	tkCY1/2 - 7		tkCY1/2 - 10		tkCY1/2 - 50		ns
		2.7 V \leq EVDD0 \leq 5.5 V	tkCY1/2 - 10		tkCY1/2 - 15		tkCY1/2 - 50		ns
Slp setup time (to SCKp \uparrow) Note 1	tsIK1	4.0 V \leq EVDD0 \leq 5.5 V	23		33		110		ns
		2.7 V \leq EVDD0 \leq 5.5 V	33		50		110		ns
Slp hold time (from SCKp \uparrow) Note 1	tkS1	2.7 V \leq EVDD0 \leq 5.5 V	10		10		10		ns
Delay time from SCKp \downarrow to SOp output Note 2	tkSO1	C = 20 pF Note 3		10		10		10	ns

Note 1. The setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp \downarrow ” and that for the Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOp output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOp output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOp pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number (mn = 00).)

3. In simplified SPI (CSI) communications in the master mode with devices operating at same voltage levels with the internal SCKp clock

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK	2.7 V ≤ EVDD0 ≤ 5.5 V	125		166		2000		ns
			2.4 V ≤ EVDD0 ≤ 5.5 V	250		250		2000		ns
			1.8 V ≤ EVDD0 ≤ 5.5 V	500		500		2000		ns
			1.6 V ≤ EVDD0 ≤ 5.5 V	1000		1000		2000		ns
SCKp high-/low-level width	tkH1, tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 12		tkCY1/2 - 21		tkCY1/2 - 50		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 18		tkCY1/2 - 25		tkCY1/2 - 50		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 38		tkCY1/2 - 38		tkCY1/2 - 50		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	tkCY1/2 - 100		tkCY1/2 - 100		tkCY1/2 - 100		ns	
Slp setup time (to SCKp↑) ^{Note 1}	tsIK1	4.0 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns	
		2.7 V ≤ EVDD0 ≤ 5.5 V	44		54		110		ns	
		2.4 V ≤ EVDD0 ≤ 5.5 V	75		75		110		ns	
		1.8 V ≤ EVDD0 ≤ 5.5 V	110		110		110		ns	
		1.6 V ≤ EVDD0 ≤ 5.5 V	220		220		220		ns	
Slp hold time (from SCKp↑) ^{Note 1}	tkSI1	1.6 V ≤ EVDD0 ≤ 5.5 V	19		19		19		ns	
Delay time from SCKp↓ to SOP output ^{Note 2}	tkSO1	1.6 V ≤ EVDD0 ≤ 5.5 V C = 30 pF ^{Note 3}		25		25		25	ns	

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp↓” and that for the Slp hold time becomes “from SCKp↓” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOP output becomes “from SCKp↑” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. C is the load capacitance of the SCKp and SOP output lines.

Caution Select the normal input buffer for the Slp pin and the normal output mode for the SOP pin and SCKp pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

Remark 2. fMCK: Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time Note 1	tkCY2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$20\text{ MHz} < f_{\text{MCK}}$	8/fMCK		8/fMCK		—		ns	
			$f_{\text{MCK}} \leq 20\text{ MHz}$	6/fMCK		6/fMCK		6/fMCK		ns	
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$	$16\text{ MHz} < f_{\text{MCK}}$	8/fMCK		8/fMCK		—		ns	
			$f_{\text{MCK}} \leq 16\text{ MHz}$	6/fMCK		6/fMCK		6/fMCK		ns	
		$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			6/fMCK and 500		6/fMCK and 500		6/fMCK and 500		ns
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			6/fMCK and 750		6/fMCK and 750		6/fMCK and 750		ns
$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			6/fMCK and 1500		6/fMCK and 1500		6/fMCK and 1500		ns		
SCKp high-/ low-level width	tkH2, tkL2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 7		tkCY2/2 - 7		tkCY2/2 - 7		ns	
		$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 8		tkCY2/2 - 8		tkCY2/2 - 8		ns	
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 18		ns	
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		tkCY2/2 - 66		tkCY2/2 - 66		tkCY2/2 - 66		ns	

(Notes, Caution, and Remarks are listed on the next page.)

4. In simplified SPI (CSI) communications in the slave mode with devices operating at same voltage levels with the SCKp external clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Slp setup time (to SCKp \uparrow) Note 2	tsik2	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 20		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30	ns	
		$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30		$1/\text{fMCK}$ + 30	ns	
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 40		$1/\text{fMCK}$ + 40		$1/\text{fMCK}$ + 40	ns	
Slp hold time (from SCKp \uparrow) Note 2	tski2	$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 31		$1/\text{fMCK}$ + 31		$1/\text{fMCK}$ + 31	ns	
		$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$		$1/\text{fMCK}$ + 250		$1/\text{fMCK}$ + 250		$1/\text{fMCK}$ + 250	ns	
Delay time from SCKp \downarrow to SOP output Note 3	tkso2	C = 30 pF Note 4	$2.7\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			$2/\text{fMCK}$ + 44		$2/\text{fMCK}$ + 110	$2/\text{fMCK}$ + 110	ns
			$2.4\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			$2/\text{fMCK}$ + 75		$2/\text{fMCK}$ + 110	$2/\text{fMCK}$ + 110	ns
			$1.8\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			$2/\text{fMCK}$ + 110		$2/\text{fMCK}$ + 110	$2/\text{fMCK}$ + 110	ns
			$1.6\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$			$2/\text{fMCK}$ + 220		$2/\text{fMCK}$ + 220	$2/\text{fMCK}$ + 220	ns

Note 1. Transfer rate in the SNOOZE mode is 1 Mbps at the maximum.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the Slp setup time becomes “to SCKp \downarrow ” and that for the Slp hold time becomes “from SCKp \downarrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 3. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1. The setting for the delay time to SOP output becomes “from SCKp \uparrow ” when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 4. C is the load capacitance of the SOP output line.

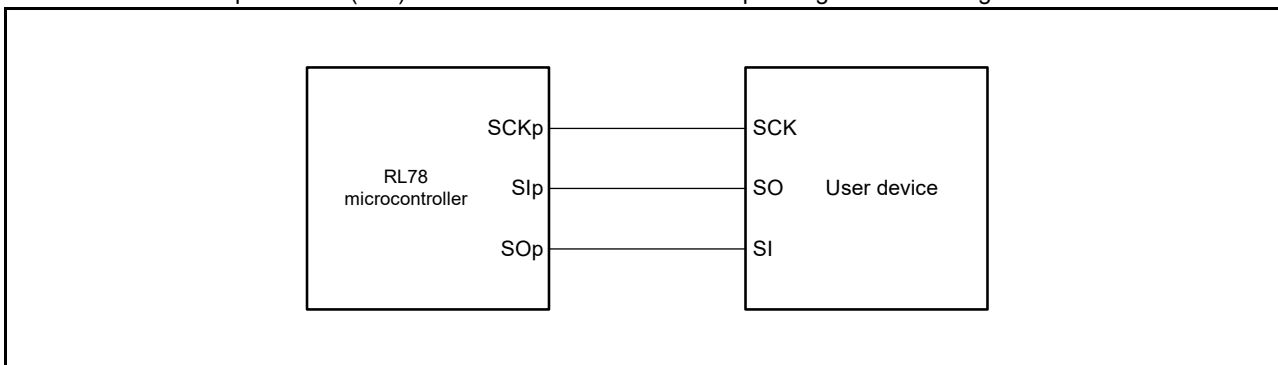
Caution Select the normal input buffer for the Slp pin and SCKp pin and the normal output mode for the SOP pin by using the port input mode register g (PIMg) and the port output mode register g (POMg).

Remark 1. p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31), m: Unit number (m = 0, 1), n: Channel number (n = 0 to 3), g: PIM and POM numbers (g = 0, 1, 4, 5, 8, 14)

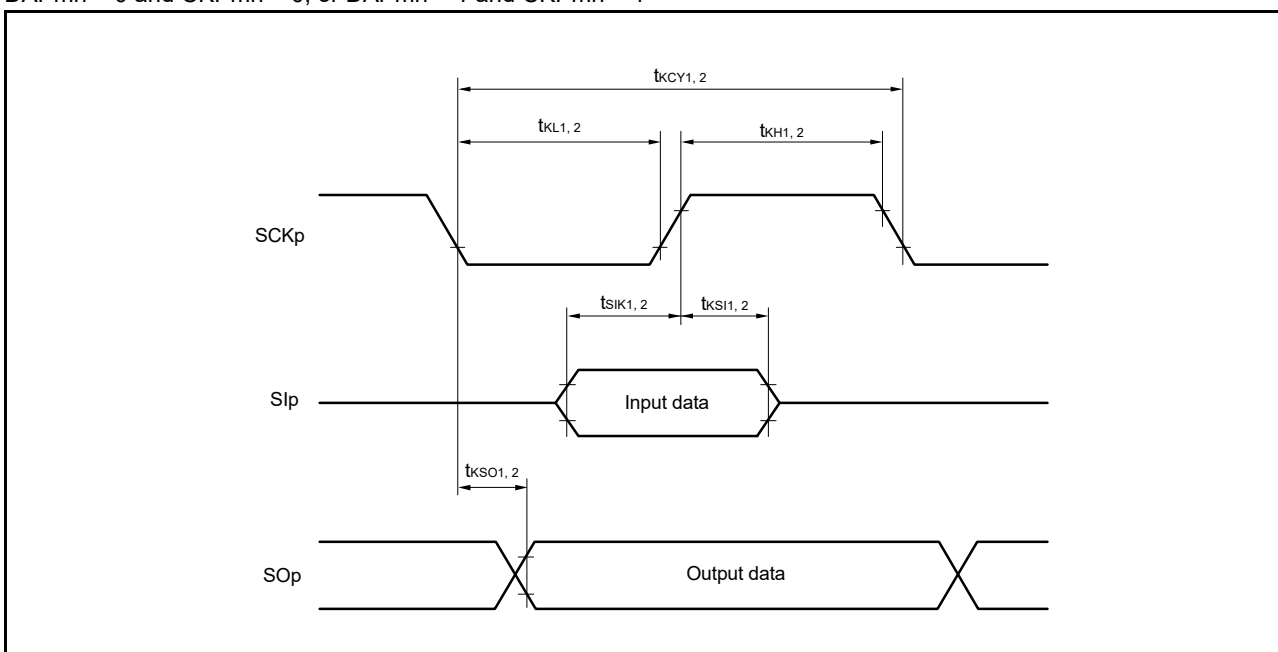
Remark 2. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

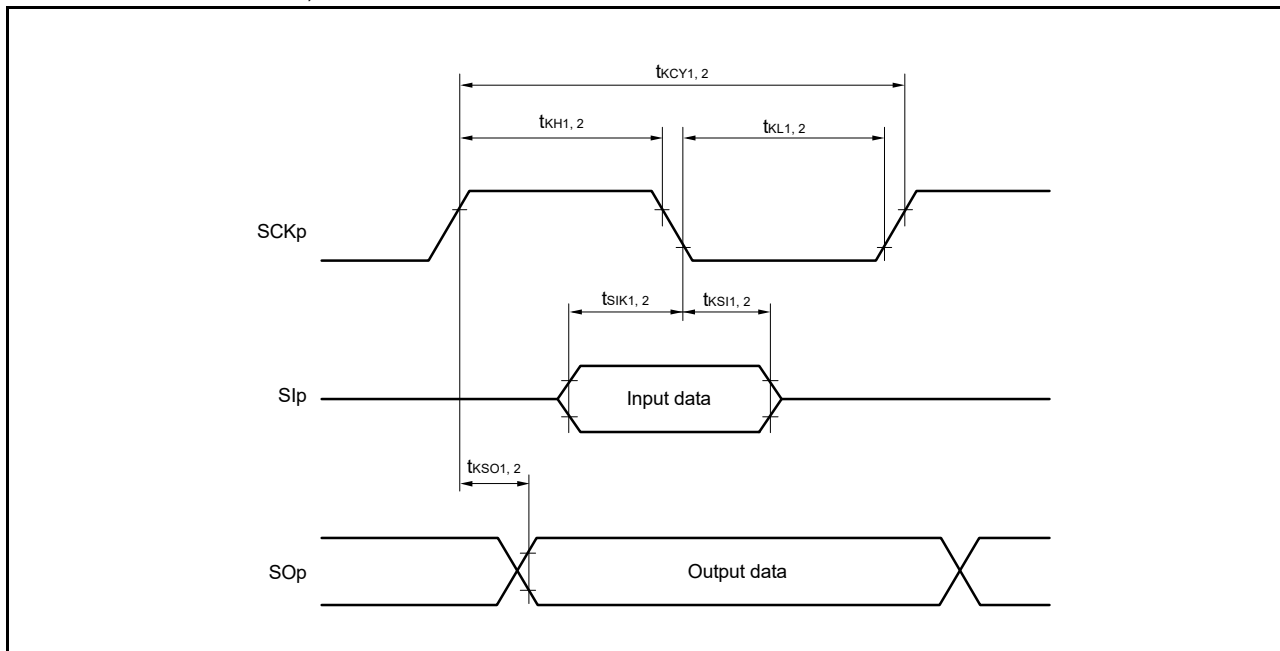
Connection in the simplified SPI (CSI) communications with devices operating at same voltage levels



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications with devices operating at same voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



- Remark 1.** p: CSI number (p = 00, 01, 10, 11, 20, 21, 30, 31)
- Remark 2.** m: Unit number, n: Channel number (mn = 00 to 03, 10 to 13)

5. In simplified I²C communications with devices operating at same voltage levels

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	fSCL	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ		1000 Note 1		1000 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ		400 Note 1		400 Note 1		400 Note 1	kHz
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ		250 Note 1		250 Note 1		250 Note 1	kHz
Hold time when SCLr is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns
Hold time when SCLr is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V, Cb = 50 pF, Rb = 2.7 kΩ	475		475		1150		ns
		1.8 V ≤ EVDD0 ≤ 5.5 V, Cb = 100 pF, Rb = 3 kΩ	1150		1150		1150		ns
		1.8 V ≤ EVDD0 < 2.7 V, Cb = 100 pF, Rb = 5 kΩ	1550		1550		1550		ns
		1.6 V ≤ EVDD0 < 1.8 V, Cb = 100 pF, Rb = 5 kΩ	1850		1850		1850		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 120.)

5. In simplified I²C communications with devices operating at same voltage levels(T_A = -40 to +105°C, 1.6 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(2/2)

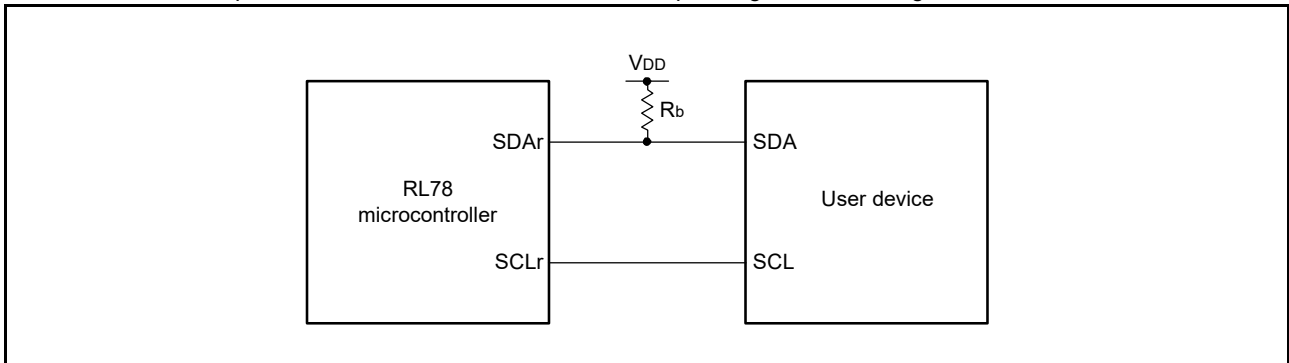
Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	tsu:DAT	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 85 Note 2		1/f _{MCK} + 85 Note 2		1/f _{MCK} + 145 Note 2		ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	1/f _{MCK} + 145 Note 2		1/f _{MCK} + 145 Note 2		1/f _{MCK} + 145 Note 2		ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 230 Note 2		1/f _{MCK} + 230 Note 2		1/f _{MCK} + 230 Note 2		ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	1/f _{MCK} + 290 Note 2		1/f _{MCK} + 290 Note 2		1/f _{MCK} + 290 Note 2		ns
Data hold time (transmission)	t _{HD} :DAT	2.7 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		1.8 V ≤ EV _{DD0} ≤ 5.5 V, C _b = 100 pF, R _b = 3 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 2.7 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns
		1.6 V ≤ EV _{DD0} < 1.8 V, C _b = 100 pF, R _b = 5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.**Note 2.** Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

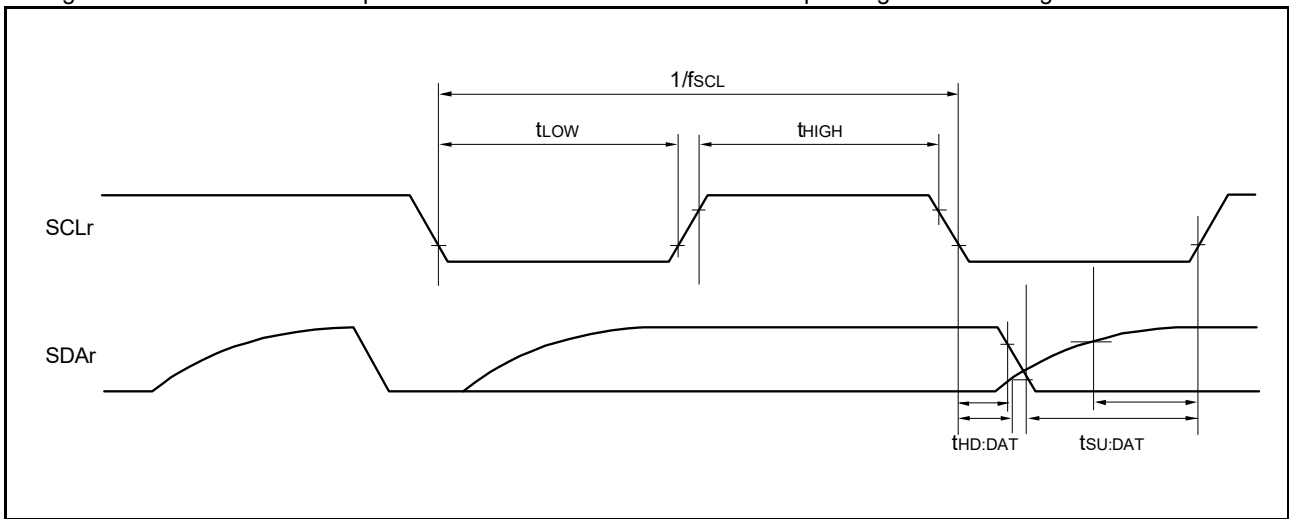
Caution Select the normal input buffer and the N-ch open drain output (withstand voltage of V_{DD} (when 30- to 52-pin products)/withstand voltage of EV_{DD} (when 64- to 128-pin products)) mode for the SDAr pin and the normal output mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register h (POMh).

(Remarks are listed on the next page.)

Connection in the simplified I²C communications with devices operating at same voltage levels



Timing of serial transfer in the simplified I²C communications with devices operating at same voltage levels



- Remark 1.** R_b[Ω]: Communication line (SDAr) pull-up resistance, C_b[F]: Communication line (SDAr, SCLr) load capacitance
- Remark 2.** r: IIC number (r = 00, 01, 10, 11, 20, 21, 30, 31), g: PIM number (g = 0, 1, 4, 5, 8, 14), h: POM number (g = 0, 1, 4, 5, 7 to 9, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$) (1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate		Reception	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$		$\text{fMCK}/6$ Note 1		$\text{fMCK}/6$ Note 1		$\text{fMCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $\text{fMCK} = \text{fCLK}$ Note 2		5.3		4		0.33	Mbps
			$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$		$\text{fMCK}/6$ Note 1		$\text{fMCK}/6$ Note 1		$\text{fMCK}/6$ Note 1	bps
			Theoretical value of the maximum transfer rate $\text{fMCK} = \text{fCLK}$ Note 2		5.3		4		0.33	Mbps
			$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$		$\text{fMCK}/6$ Notes 1, 3, 4		$\text{fMCK}/6$ Notes 1, 3		$\text{fMCK}/6$ Notes 1, 3	bps
			Theoretical value of the maximum transfer rate $\text{fMCK} = \text{fCLK}$ Note 2		5.3		4		0.33	Mbps

Note 1. Transfer rate in the SNOOZE mode is within the range from 4800 to 9600 bps.

Note 2. The maximum operating frequencies of the CPU/peripheral hardware clock (fCLK) are:

HS (high-speed main) mode : 32 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

LS (low-speed main) mode : 24 MHz ($1.8\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

4 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

LP (low-power main) mode : 2 MHz ($1.6\text{ V} \leq \text{VDD} \leq 5.5\text{ V}$)

Note 3. Use this rate with $\text{EVDD0} \geq \text{V}_b$.

Note 4. The following conditions are required for low voltage interface when $\text{EVDD0} < \text{VDD}$.

$2.4\text{ V} \leq \text{EVDD0} < 2.7\text{ V}$: 2.6 Mbps (max.)

$1.8\text{ V} \leq \text{EVDD0} < 2.4\text{ V}$: 1.3 Mbps (max.)

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of VDD (when 30- to 52-pin products)/withstand voltage of EVDD (when 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

Remark 1. $\text{V}_b[\text{V}]$: Communication line voltage

Remark 2. q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)

Remark 3. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)

Remark 4. Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

6. In UART communications with devices operating at different voltage levels (1.8 V, 2.5 V, 3 V)

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
Transfer rate		Transmission	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V		Note 1		Note 1		Note 1	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 1.4 kΩ, Vb = 2.7 V		2.8Note 2		2.8Note 2		2.8Note 2	Mbps
			2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V		Note 3		Note 3		Note 3	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 2.7 kΩ, Vb = 2.3 V		1.2Note 4		1.2Note 4		1.2Note 4	Mbps
			1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V		Notes 5, 6		Notes 5, 6		Notes 5, 6	bps
			Theoretical value of the maximum transfer rate Cb = 50 pF, Rb = 5.5 kΩ, Vb = 1.6 V		0.43 Note 7		0.43 Note 7		0.43 Note 7	Mbps

Note 1. The smaller maximum transfer rate derived by using fmck/6 or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.2}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides

Note 2. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 1** above to calculate the maximum transfer rate under conditions of the customer.

(Notes and Caution continue in the next page.)

Note 3. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $2.7\text{ V} \leq EV_{DD0} < 4.0\text{ V}$, $2.3\text{ V} \leq V_b \leq 2.7\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\} \times 3} \text{ [bps]}$$

$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{2.0}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

Note 4. This rate is calculated as an example when the conditions described in the “Conditions” column are met. See **Note 3** above to calculate the maximum transfer rate under conditions of the customer.

Note 5. Use this rate with $EV_{DD0} \geq V_b$.

Note 6. The smaller maximum transfer rate derived by using $f_{MCK}/6$ or the following expression is the valid maximum transfer rate. Expression for calculating the transfer rate when $1.8\text{ V} \leq EV_{DD0} < 3.3\text{ V}$, $1.6\text{ V} \leq V_b \leq 2.0\text{ V}$

$$\text{Maximum transfer rate} = \frac{1}{\{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\} \times 3} \text{ [bps]}$$

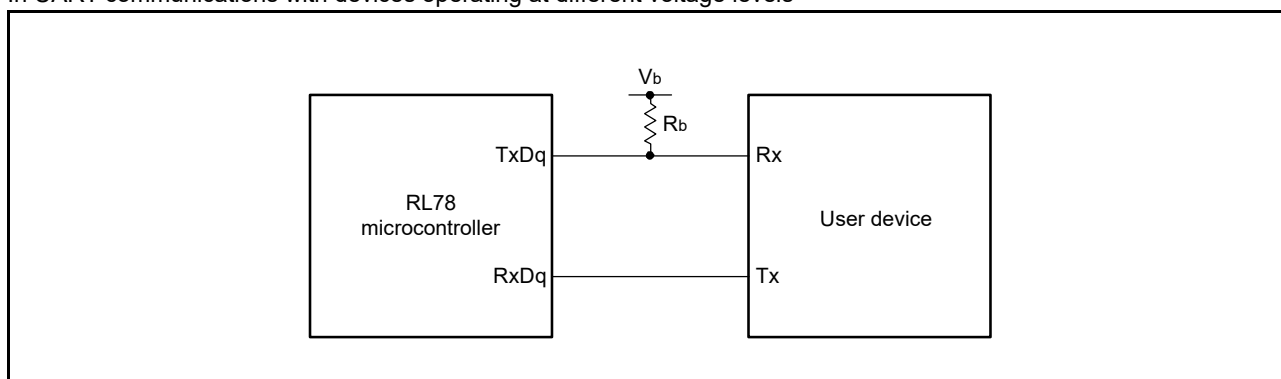
$$\text{Baud rate error (theoretical value)} = \frac{\frac{1}{\text{Transfer rate} \times 2} - \{-C_b \times R_b \times \ln(1 - \frac{1.5}{V_b})\}}{(\frac{1}{\text{Transfer rate}}) \times \text{Number of transferred bits}} \times 100 \text{ [%]}$$

* This value is the theoretical value of the relative difference between the transmission and reception sides.

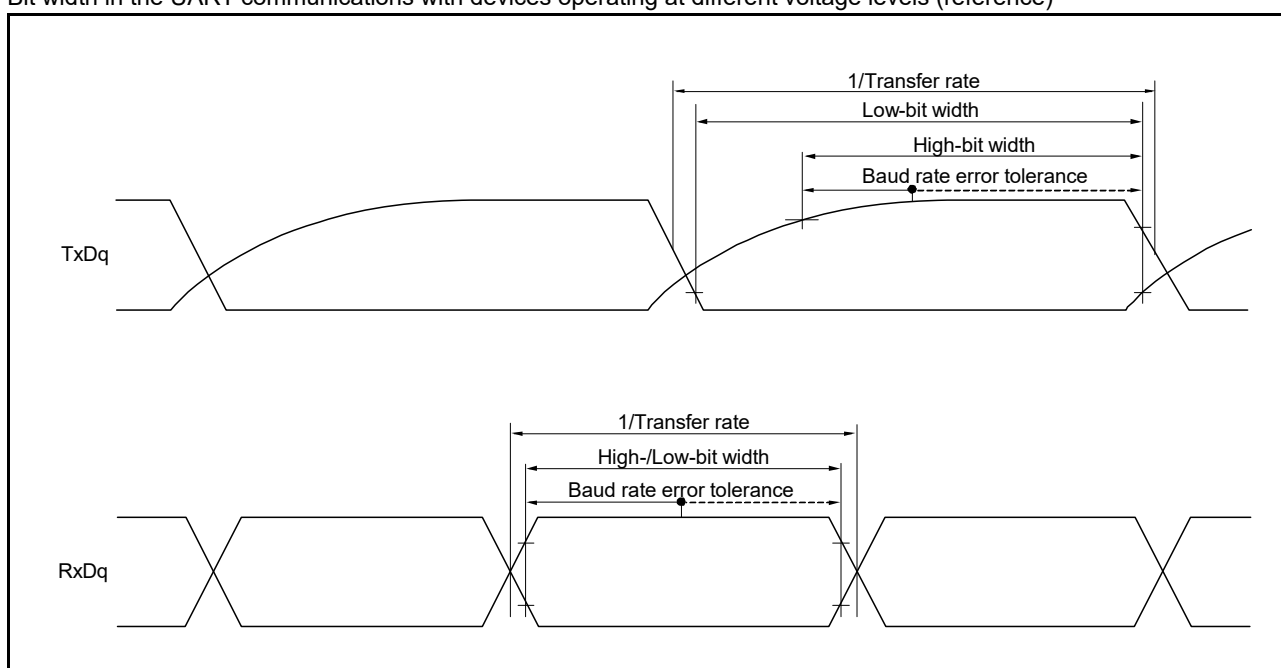
Note 7. This rate is calculated as an example when the conditions described in the “Conditions” column are met. Refer to **Note 6** above to calculate the maximum transfer rate under conditions of the customer.

Caution Select the TTL input buffer for the RxDq pin and the N-ch open drain output (withstand voltage of V_{DD} (when 30- to 52-pin products)/withstand voltage of EV_{DD} (when 64- to 128-pin products)) mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL} , see the DC characteristics with TTL input buffer selected.

In UART communications with devices operating at different voltage levels



Bit width in the UART communications with devices operating at different voltage levels (reference)



- Remark 1.** $R_b[\Omega]$: Communication line (TxDq) pull-up resistance, $C_b[F]$: Communication line (TxDq) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** q: UART number (q = 0 to 3), g: PIM and POM number (g = 0, 1, 8, 14)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00 to 03, 10 to 13).)
- Remark 4.** Communications by using UART2 with devices operating at different voltage levels are not possible when the setting of bit 1 (PIOR1) of the peripheral I/O redirection register (PIOR) is 1.

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 \geq 2/fCLK 4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	200		200		2300		ns
			300		300		2300		ns
SCKp high-level width	tkH1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns
		2.7 V \leq EVDD0 $<$ 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω	tkCY1/2 - 120		tkCY1/2 - 120		tkCY1/2 - 120		ns
SCKp low-level width	tkL1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	tkCY1/2 - 7		tkCY1/2 - 7		tkCY1/2 - 50		ns
		2.7 V \leq EVDD0 $<$ 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω	tkCY1/2 - 10		tkCY1/2 - 10		tkCY1/2 - 50		ns
Slp setup time (to SCKp \uparrow) ^{Note 1}	tsIK1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	58		58		479		ns
		2.7 V \leq EVDD0 $<$ 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω	121		121		479		ns
Slp hold time (from SCKp \uparrow) ^{Note 1}	tkSI1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω	10		10		10		ns
		2.7 V \leq EVDD0 $<$ 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω	10		10		10		ns
Delay time from SCKp \downarrow to SOp output ^{Note 1}	tkSO1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 20 pF, Rb = 1.4 k Ω		60		60		60	ns
		2.7 V \leq EVDD0 $<$ 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 20 pF, Rb = 2.7 k Ω		130		130		130	ns

(Notes, Caution, and Remarks are listed on the next page.)

7. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (2.5 V or 3 V) with the internal SCKp clock (the ratings below are only applicable to CSI00)

($T_A = -40$ to $+105^\circ\text{C}$, $2.7\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) ^{Note 2}	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	23		23		110		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	33		33		110		ns
Slp hold time (from SCKp↓) ^{Note 2}	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$	10		10		10		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$	10		10		10		ns
Delay time from SCKp↑ to SOp output ^{Note 2}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 1.4\text{ k}\Omega$		10		10		10	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$, $\text{C}_b = 20\text{ pF}$, $\text{R}_b = 2.7\text{ k}\Omega$		10		10		10	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (when 30- to 52-pin products)/withstand voltage of EVDD (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

Remark 1. Rb[Ω]: Communication line (SCKp, SOp) pull-up resistance, Cb[F]: Communication line (SCKp, SOp) load capacitance, Vb[V]: Communication line voltage

Remark 2. p: CSI number (p = 00), m: Unit number (m = 0), n: Channel number (n = 0), g: PIM and POM numbers (g = 1)

Remark 3. fMCK: Serial array unit operation clock frequency

(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).)

Remark 4. The listed times are only valid when the peripheral I/O redirect function of CSI00 is not in use.

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

(TA = -40 to +105°C, 1.8 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

(1/3)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp cycle time	tkCY1	tkCY1 ≥ 4/fCLK 4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	300		300		2300		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	500		500		2300		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ	1150		1150		2300		ns
SCKp high-level width	tkH1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 75		tkCY1/2 - 75		tkCY1/2 - 75		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 170		tkCY1/2 - 170		tkCY1/2 - 170		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 458		tkCY1/2 - 458		tkCY1/2 - 458		ns
SCKp low-level width	tkL1	4.0 V ≤ EVDD0 ≤ 5.5 V, 2.7 V ≤ Vb ≤ 4.0 V, Cb = 30 pF, Rb = 1.4 kΩ	tkCY1/2 - 12		tkCY1/2 - 12		tkCY1/2 - 50		ns
		2.7 V ≤ EVDD0 < 4.0 V, 2.3 V ≤ Vb ≤ 2.7 V, Cb = 30 pF, Rb = 2.7 kΩ	tkCY1/2 - 18		tkCY1/2 - 18		tkCY1/2 - 50		ns
		1.8 V ≤ EVDD0 < 3.3 V, 1.6 V ≤ Vb ≤ 2.0 V ^{Note} , Cb = 30 pF, Rb = 5.5 kΩ	tkCY1/2 - 50		tkCY1/2 - 50		tkCY1/2 - 50		ns

Note Use this setting with EVDD0 ≥ Vb.

Caution Select the TTL input buffer for the SIp pin and the N-ch open drain output (withstand voltage of VDD (when 30- to 52-pin products)/withstand voltage of EVDD (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on page 130.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/3)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp \uparrow) ^{Note 1}	tsIK1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 30 pF, Rb = 1.4 k Ω	81		81		479		ns
		2.7 V \leq EVDD0 < 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 30 pF, Rb = 2.7 k Ω	177		177		479		ns
		1.8 V \leq EVDD0 < 3.3 V, 1.6 V \leq Vb \leq 2.0 V ^{Note 2} , Cb = 30 pF, Rb = 5.5 k Ω	479		479		479		ns
Slp hold time (from SCKp \uparrow) ^{Note 1}	tkSI1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 30 pF, Rb = 1.4 k Ω	19		19		19		ns
		2.7 V \leq EVDD0 < 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 30 pF, Rb = 2.7 k Ω	19		19		19		ns
		1.8 V \leq EVDD0 < 3.3 V, 1.6 V \leq Vb \leq 2.0 V ^{Note 2} , Cb = 30 pF, Rb = 5.5 k Ω	19		19		19		ns
Delay time from SCKp \downarrow to SOp output ^{Note 1}	tkSO1	4.0 V \leq EVDD0 \leq 5.5 V, 2.7 V \leq Vb \leq 4.0 V, Cb = 30 pF, Rb = 1.4 k Ω		100		100		100	ns
		2.7 V \leq EVDD0 < 4.0 V, 2.3 V \leq Vb \leq 2.7 V, Cb = 30 pF, Rb = 2.7 k Ω		195		195		195	ns
		1.8 V \leq EVDD0 < 3.3 V, 1.6 V \leq Vb \leq 2.0 V ^{Note 2} , Cb = 30 pF, Rb = 5.5 k Ω		483		483		483	ns

Note 1. This setting applies when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1.

Note 2. Use this setting with EVDD0 \geq Vb.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (when 30- to 52-pin products)/withstand voltage of EVDD (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on page 130.)

8. In simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the internal SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(3/3)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Slp setup time (to SCKp↓) ^{Note 1}	tsIK1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	44		44		110		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	44		44		110		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	110		110		110		ns
Slp hold time (from SCKp↓) ^{Note 1}	tkSI1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$	19		19		19		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$	19		19		19		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$	19		19		19		ns
Delay time from SCKp↑ to SOp output ^{Note 1}	tkSO1	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 1.4\text{ k}\Omega$		25		25		25	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 2.7\text{ k}\Omega$		25		25		25	ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ ^{Note 2} , $\text{Cb} = 30\text{ pF}$, $\text{Rb} = 5.5\text{ k}\Omega$		25		25		25	ns

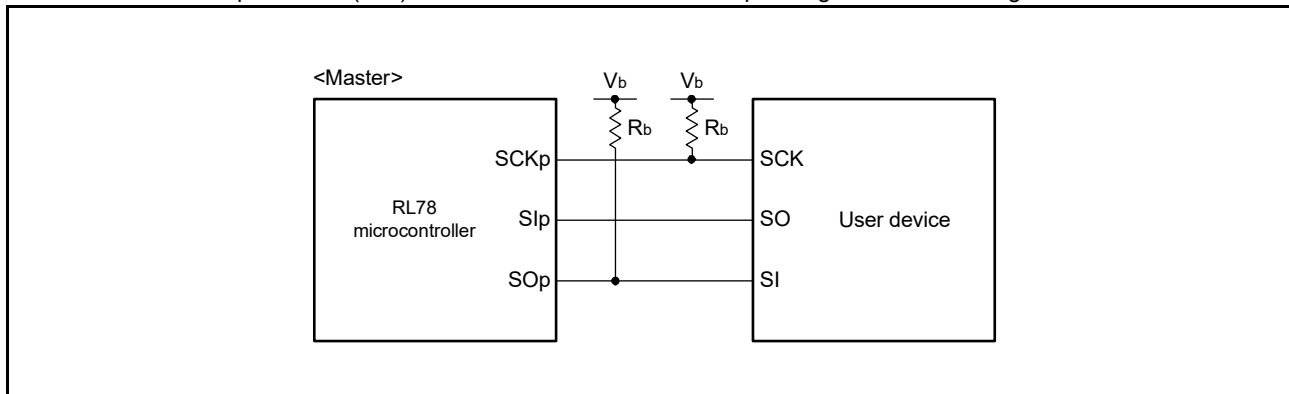
Note 1. This setting applies when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0.

Note 2. Use this setting with $\text{EVDD0} \geq \text{Vb}$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (when 30- to 52-pin products)/withstand voltage of EVDD (when 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

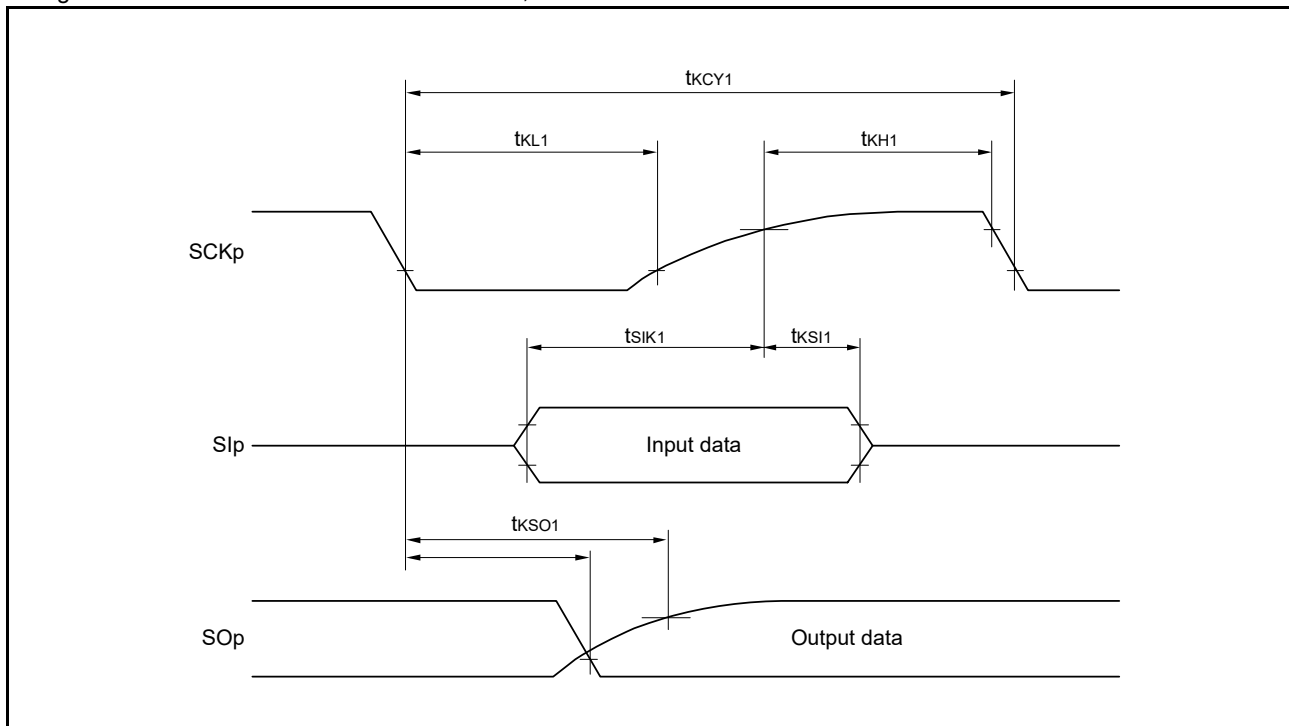
(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels

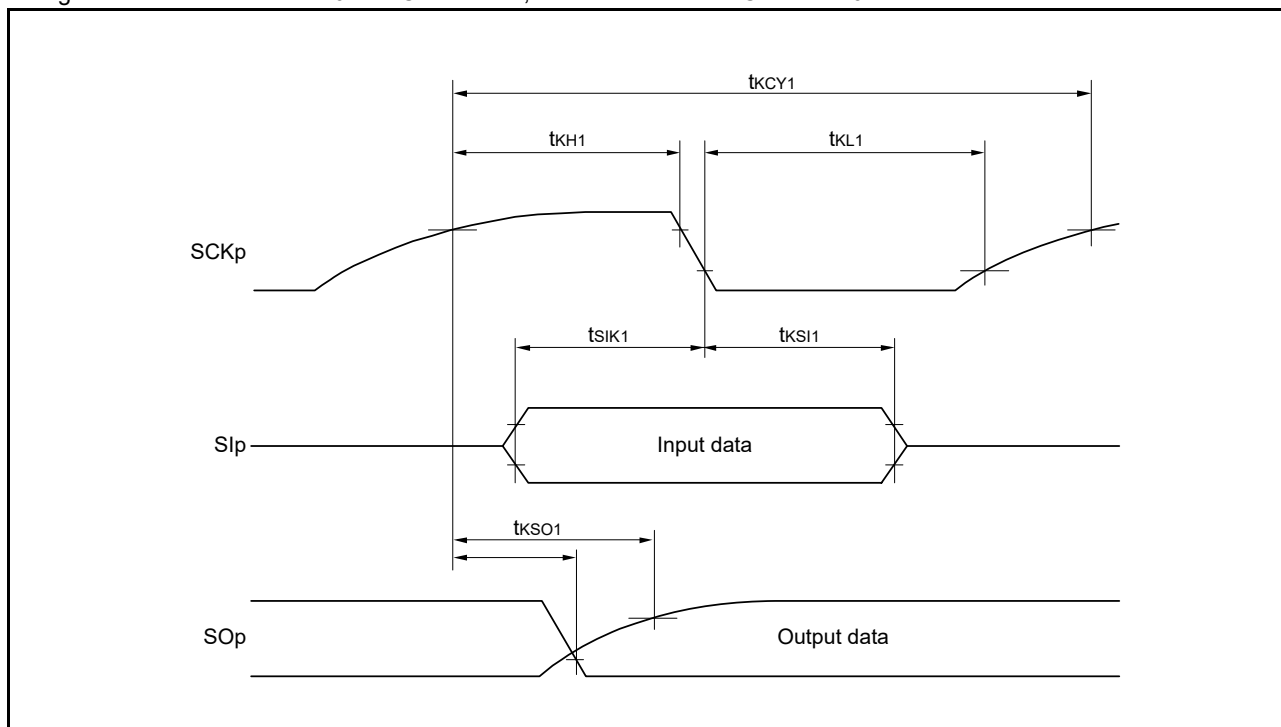


- Remark 1.** $R_b[\Omega]$: Communication line (SCKp, SOp) pull-up resistance, $C_b[F]$: Communication line (SCKp, SOp) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- Remark 3.** fMCK: Serial array unit operation clock frequency
(To set this operating clock, use the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00).)
- Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 0, or DAPmn = 1 and CKPmn = 1



Timing of serial transfer in the simplified SPI (CSI) communications in the master mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 2. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(1/2)

Item	Symbol	Conditions		HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit	
				Min.	Max.	Min.	Max.	Min.	Max.		
SCKp cycle time Note 1	tkCY2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{V}_b \leq 4.0\text{ V}$	$24\text{ MHz} < \text{fMCK}$	14/fMCK		—		—		ns	
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	12/fMCK		12/fMCK		—		ns	
			$8\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	10/fMCK		10/fMCK		—		ns	
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	8/fMCK		8/fMCK		—		ns	
			$\text{fMCK} \leq 4\text{ MHz}$	6/fMCK		6/fMCK		10/fMCK		ns	
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{V}_b \leq 2.7\text{ V}$,	$24\text{ MHz} < \text{fMCK}$	20/fMCK		—		—		ns	
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	16/fMCK		16/fMCK		—		ns	
			$16\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	14/fMCK		14/fMCK		—		ns	
			$8\text{ MHz} < \text{fMCK} \leq 16\text{ MHz}$	12/fMCK		12/fMCK		—		ns	
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	8/fMCK		8/fMCK		—		ns	
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{V}_b \leq 2.0\text{ V}$ Note 2	$24\text{ MHz} < \text{fMCK}$	48/fMCK		—		—		ns	
			$20\text{ MHz} < \text{fMCK} \leq 24\text{ MHz}$	36/fMCK		36/fMCK		—		ns	
			$16\text{ MHz} < \text{fMCK} \leq 20\text{ MHz}$	32/fMCK		32/fMCK		—		ns	
			$8\text{ MHz} < \text{fMCK} \leq 16\text{ MHz}$	26/fMCK		26/fMCK		—		ns	
			$4\text{ MHz} < \text{fMCK} \leq 8\text{ MHz}$	16/fMCK		16/fMCK		—		ns	
				$\text{fMCK} \leq 4\text{ MHz}$	10/fMCK		10/fMCK		10/fMCK		ns

(Notes and Caution are listed on the next page, and Remarks are listed on page 134.)

9. In simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V) with the external SCKp clock

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

(2/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCKp high-/low-level width	tkH2, tkL2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	tkCY2/2 - 12		tkCY2/2 - 12		tkCY2/2 - 50		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	tkCY2/2 - 18		tkCY2/2 - 18		tkCY2/2 - 50		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2	tkCY2/2 - 50		tkCY2/2 - 50		tkCY2/2 - 50		ns
Slp setup time (to SCKp \uparrow) Note 3	tsIK2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$	1/fMCK + 20		1/fMCK + 20		1/fMCK + 30		ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2	1/fMCK + 30		1/fMCK + 30		1/fMCK + 30		ns
Slp hold time (from SCKp \uparrow) Note 3	tkSI2		1/fMCK + 31		1/fMCK + 31		1/fMCK + 31		ns
Delay time from SCKp \downarrow to SOp output Note 4	tkSO2	$4.0\text{ V} \leq \text{EVDD0} \leq 5.5\text{ V}$, $2.7\text{ V} \leq \text{Vb} \leq 4.0\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 1.4\text{ k}\Omega$		2/fMCK + 120		2/fMCK + 120		2/fMCK + 573	ns
		$2.7\text{ V} \leq \text{EVDD0} < 4.0\text{ V}$, $2.3\text{ V} \leq \text{Vb} \leq 2.7\text{ V}$, $C_b = 30\text{ pF}$, $R_b = 2.7\text{ k}\Omega$		2/fMCK + 214		2/fMCK + 214		2/fMCK + 573	ns
		$1.8\text{ V} \leq \text{EVDD0} < 3.3\text{ V}$, $1.6\text{ V} \leq \text{Vb} \leq 2.0\text{ V}$ Note 2 , $C_b = 30\text{ pF}$, $R_b = 5.5\text{ k}\Omega$		2/fMCK + 573		2/fMCK + 573		2/fMCK + 573	ns

Note 1. Transfer rate in the SNOOZE mode: 1 Mbps (max.)

Note 2. Use this setting with $\text{EVDD0} \geq \text{Vb}$.

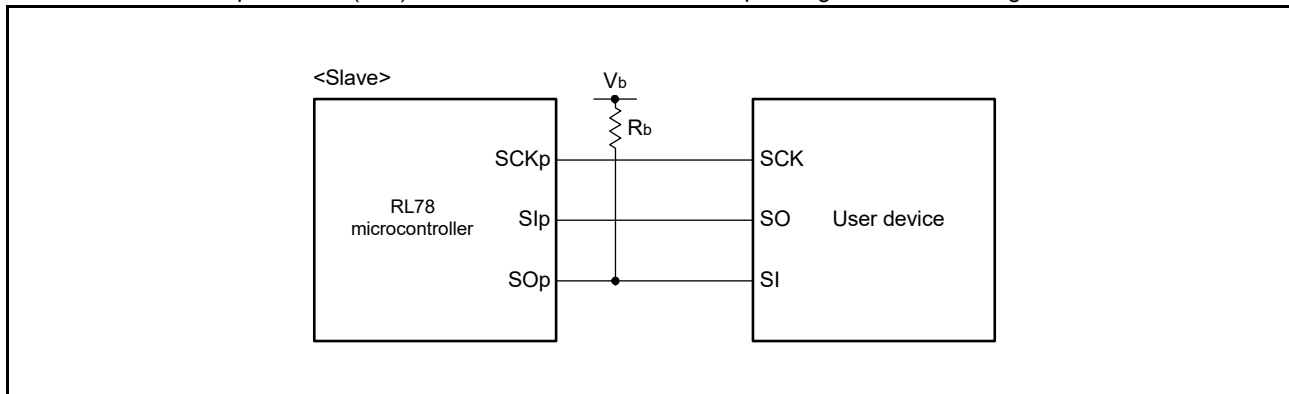
Note 3. This setting applies when $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The Slp setup time becomes “to SCKp \downarrow ” and Slp hold time becomes “from SCKp \downarrow ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

Note 4. This setting applies when $\text{DAPmn} = 0$ and $\text{CKPmn} = 0$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 1$. The delay time to SOp output becomes “from SCKp \uparrow ” when $\text{DAPmn} = 0$ and $\text{CKPmn} = 1$, or $\text{DAPmn} = 1$ and $\text{CKPmn} = 0$.

Caution Select the TTL input buffer for the Slp pin and the N-ch open drain output (withstand voltage of VDD (for the 30- to 52-pin products)/withstand voltage of EVDD (for the 64- to 128-pin products)) mode for the SOp pin and SCKp pin by using port input mode register g (PIMg) and port output mode register g (POMg). For VIH and VIL, see the DC characteristics with TTL input buffer selected.

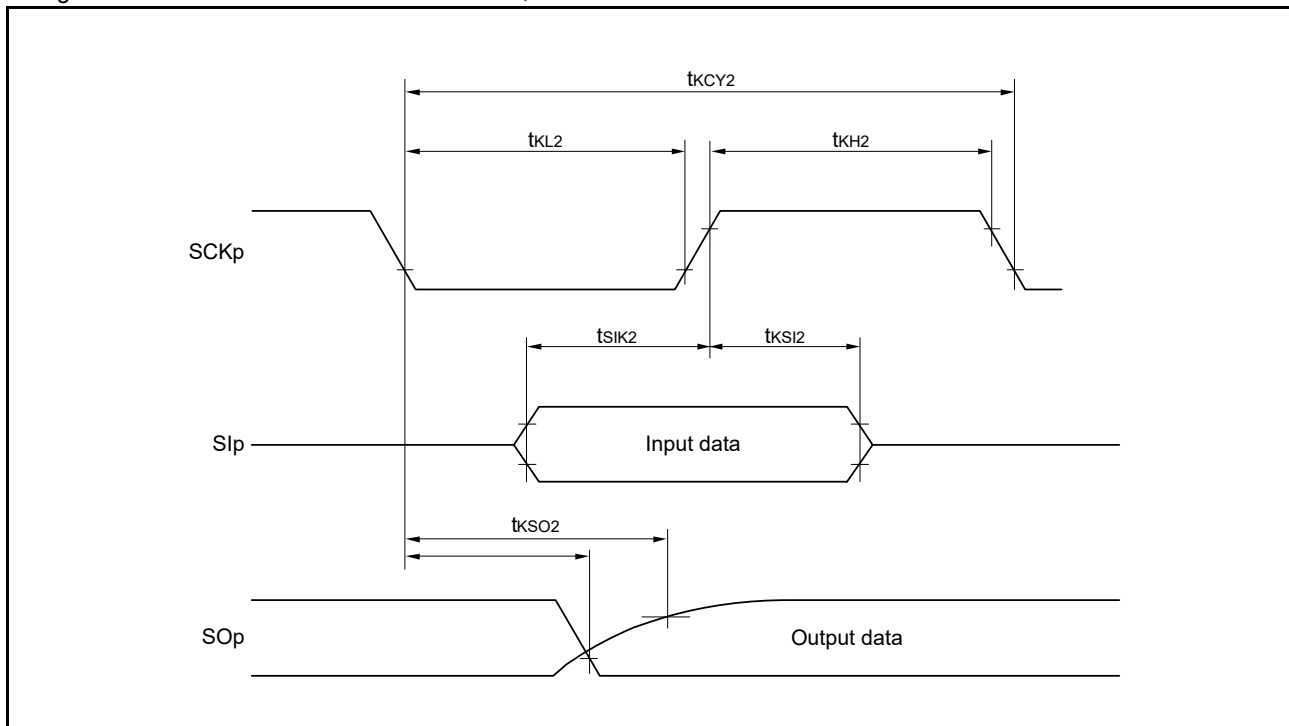
(Remarks are listed on the next page.)

Connection in the simplified SPI (CSI) communications with devices operating at different voltage levels

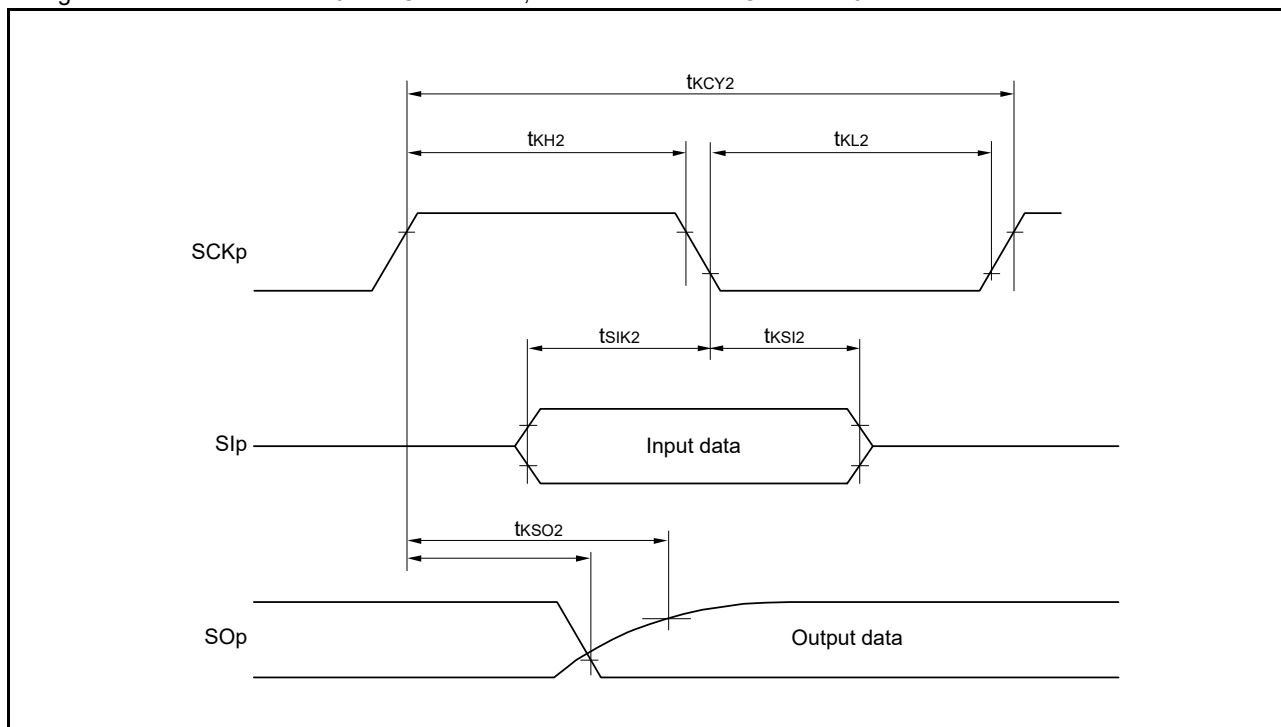


- Remark 1.** $R_b[\Omega]$: Communication line (SO_p) pull-up resistance, $C_b[F]$: Communication line (SO_p) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- Remark 3.** f_{MCK}: Serial array unit operation clock frequency
(To set this operating clock, use the CKSMn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 01, 02, 10, 12 and 13).)
- Remark 4.** Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAP_{mn} = 0 and CKP_{mn} = 0, or DAP_{mn} = 1 and CKP_{mn} = 1



Timing of serial transfer in the simplified SPI (CSI) communications in the slave mode with devices operating at different voltage levels when DAPmn = 0 and CKPmn = 1, or DAPmn = 1 and CKPmn = 0



Remark 1. p: CSI number (p = 00, 01, 10, 20, 30, 31), m: Unit number, n: Channel number (mn = 00, 01, 02, 10, 12, 13), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)

Remark 2. Communications by using CSI01 of 48-, 52-, and 64-pin products, and CSI11 and CSI21 with devices operating at different voltage levels are not possible. Use other CSI channels to handle such communications.

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, or 3 V)(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(1/2)

Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
SCLr clock frequency	f _{SCL}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ		1000 Note 1		1000 Note 1		300 Note 1	kHz
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ		400 Note 1		400 Note 1		300 Note 1	kHz
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ		300 Note 1		300 Note 1		300 Note 1	kHz
Hold time when SCLr is low	t _{LOW}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	475		475		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	475		475		1550		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1150		1550		1550		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1150		1550		1550		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1550		1550		1550		ns
Hold time when SCLr is high	t _{HIGH}	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	245		245		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	200		200		610		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	675		675		610		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	600		600		610		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	610		610		610		ns

10. Simplified I²C communications with devices operating at different voltage levels (1.8 V, 2.5 V, and 3 V)(T_A = -40 to +105°C, 1.8 V ≤ EV_{DD0} = EV_{DD1} ≤ V_{DD} ≤ 5.5 V, V_{SS} = EV_{SS0} = EV_{SS1} = 0 V)

(2/2)

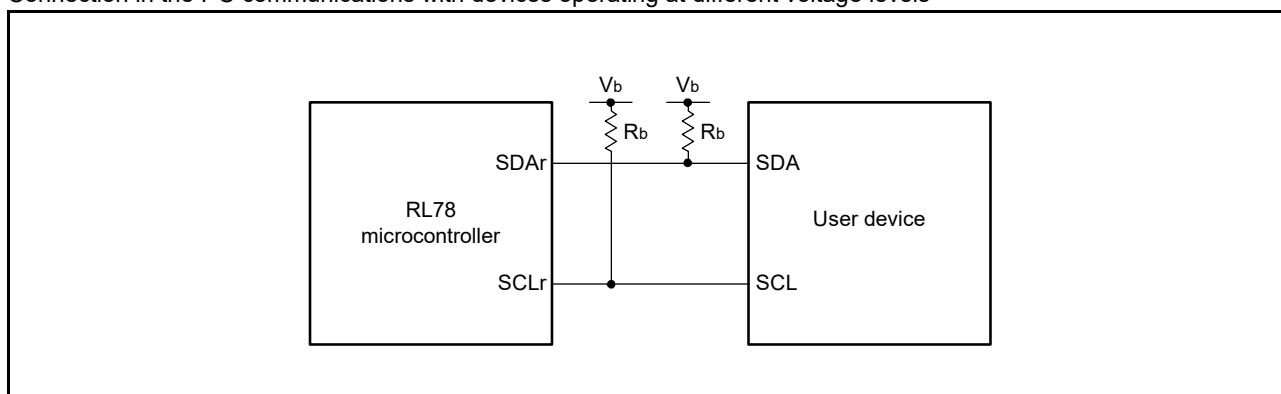
Item	Symbol	Conditions	HS (High-Speed Main) Mode		LS (Low-Speed Main) Mode		LP (Low-Power Main) Mode		Unit
			Min.	Max.	Min.	Max.	Min.	Max.	
Data setup time (reception)	tsu:DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	1/f _{MCK} + 135 Note 3		1/f _{MCK} + 135 Note 3		1/f _{MCK} + 190 Note 3		ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		1/f _{MCK} + 190 Note 3		ns
Data hold time (transmission)	tHD:DAT	4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 50 pF, R _b = 2.7 kΩ	0	305	0	305	0	305	ns
		4.0 V ≤ EV _{DD0} ≤ 5.5 V, 2.7 V ≤ V _b ≤ 4.0 V, C _b = 100 pF, R _b = 2.8 kΩ	0	355	0	355	0	355	ns
		2.7 V ≤ EV _{DD0} < 4.0 V, 2.3 V ≤ V _b ≤ 2.7 V, C _b = 100 pF, R _b = 2.7 kΩ	0	355	0	355	0	355	ns
		1.8 V ≤ EV _{DD0} < 3.3 V, 1.6 V ≤ V _b ≤ 2.0 V ^{Note 2} , C _b = 100 pF, R _b = 5.5 kΩ	0	405	0	405	0	405	ns

Note 1. The listed times must be no greater than f_{MCK}/4.**Note 2.** Use this setting with EV_{DD0} ≥ V_b.**Note 3.** Set f_{MCK} so that it will not exceed the hold time when SCLr is low or high.

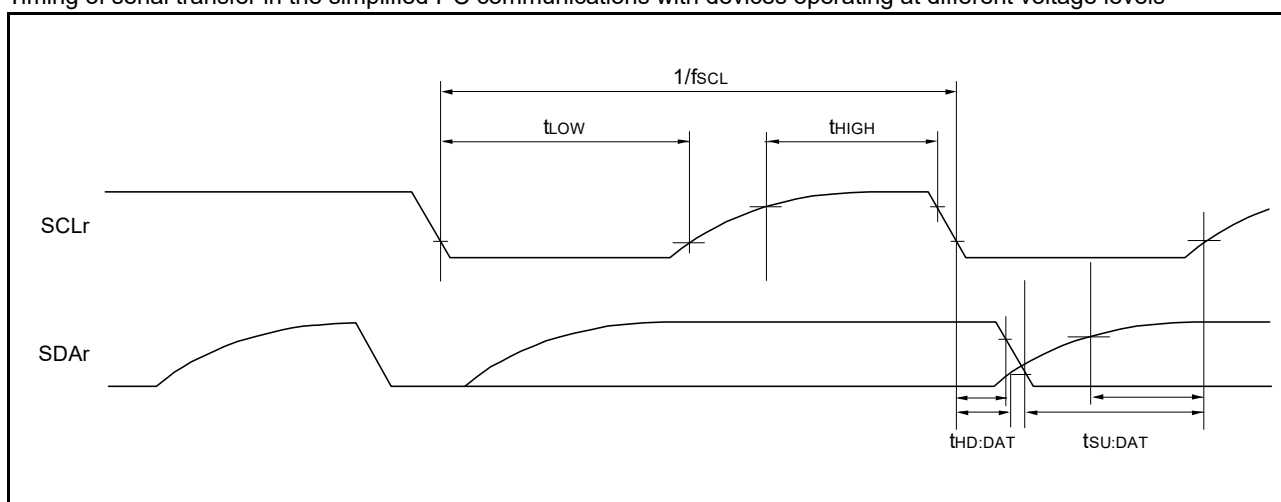
Caution Select the TTL input buffer and the N-ch open drain output (withstand voltage of V_{DD} (for the 30- to 52-pin products)/withstand voltage of EV_{DD} (for the 64- to 128-pin products)) mode for the SDAr pin and the N-ch open drain output (withstand voltage of V_{DD} (for the 30- to 52-pin products)/withstand voltage of EV_{DD} (for the 64- to 128-pin products)) mode for the SCLr pin by using port input mode register g (PIMg) and port output mode register g (POMg). For V_{IH} and V_{IL}, see the DC characteristics with TTL input buffer selected.

(Remarks are listed on the next page.)

Connection in the I²C communications with devices operating at different voltage levels



Timing of serial transfer in the simplified I²C communications with devices operating at different voltage levels



- Remark 1.** $R_b[\Omega]$: Communication line (SDAr, SCLr) pull-up resistance, $C_b[F]$: Communication line (SDAr, SCLr) load capacitance, $V_b[V]$: Communication line voltage
- Remark 2.** r: IIC number (r = 00, 01, 10, 20, 30, 31), g: PIM and POM number (g = 0, 1, 4, 5, 8, 14)
- Remark 3.** f_{MCK} : Serial array unit operation clock frequency
(To set this operating clock, use the CKSmn bit in the serial mode register mn (SMRmn) (m: Unit number, n: Channel number = 00, 01, 02, 10, 12 and 13).)

2.5.2 Serial interface UARTA

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate			200	0	153600	bps

Caution Select the normal input buffer for the RxDq pin and the normal output mode for the TxDq pin by using port input mode register g (PIMg) and port output mode register g (POMg).

Remark g: PIM number (g = 3, 4, 7, 8), h: POM number (h = 3, 4, 7, 8, 12)

2.5.3 Serial interface IICA

1. I²C standard mode

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Standard mode: fCLK ≥ 1 MHz	0		100	kHz
Setup time of restart condition	tSU:STA		4.7			μs
Hold time ^{Note 1}	tHD:STA		4.0			μs
Hold time when SCLA0 is low	tLOW		4.7			μs
Hold time when SCLA0 is high	tHIGH		4.0			μs
Data setup time (reception)	tSU:DAT		250			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT		0		3.45	μs
Setup time of stop condition	tSU:STO		4.0			μs
Bus-free time	tBUF		4.7			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The listed frequency and times apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 400 pF, Rb = 2.7 kΩ

2. I²C fast mode

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode: fCLK ≥ 3.5 MHz 1.8 V ≤ EVDD0 ≤ 5.5 V	0		400	kHz
Setup time of restart condition	tSU:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time ^{Note 1}	tHD:STA	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Hold time when SCLA0 is low	tLOW	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs
Hold time when SCLA0 is high	tHIGH	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Data setup time (reception)	tSU:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	100			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT	1.8 V ≤ EVDD0 ≤ 5.5 V	0		0.9	μs
Setup time of stop condition	tSU:STO	1.8 V ≤ EVDD0 ≤ 5.5 V	0.6			μs
Bus-free time	tBUF	1.8 V ≤ EVDD0 ≤ 5.5 V	1.3			μs

Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (Cb) and communication line pull-up resistor (Rb) are as follows.
Cb = 320 pF, Rb = 1.1 kΩ

3. I²C fast mode plus

(T_A = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
SCLA0 clock frequency	fSCL	Fast mode plus: fCLK ≥ 10 MHz 2.7 V ≤ EVDD0 ≤ 5.5 V	0		1000	kHz
Setup time of restart condition	tSU:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time ^{Note 1}	tHD:STA	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Hold time when SCLA0 is low	tLOW	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs
Hold time when SCLA0 is high	tHIGH	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Data setup time (reception)	tSU:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	50			ns
Data hold time (transmission) ^{Note 2}	tHD:DAT	2.7 V ≤ EVDD0 ≤ 5.5 V	0		0.45	μs
Setup time of stop condition	tSU:STO	2.7 V ≤ EVDD0 ≤ 5.5 V	0.26			μs
Bus-free time	tBUF	2.7 V ≤ EVDD0 ≤ 5.5 V	0.5			μs

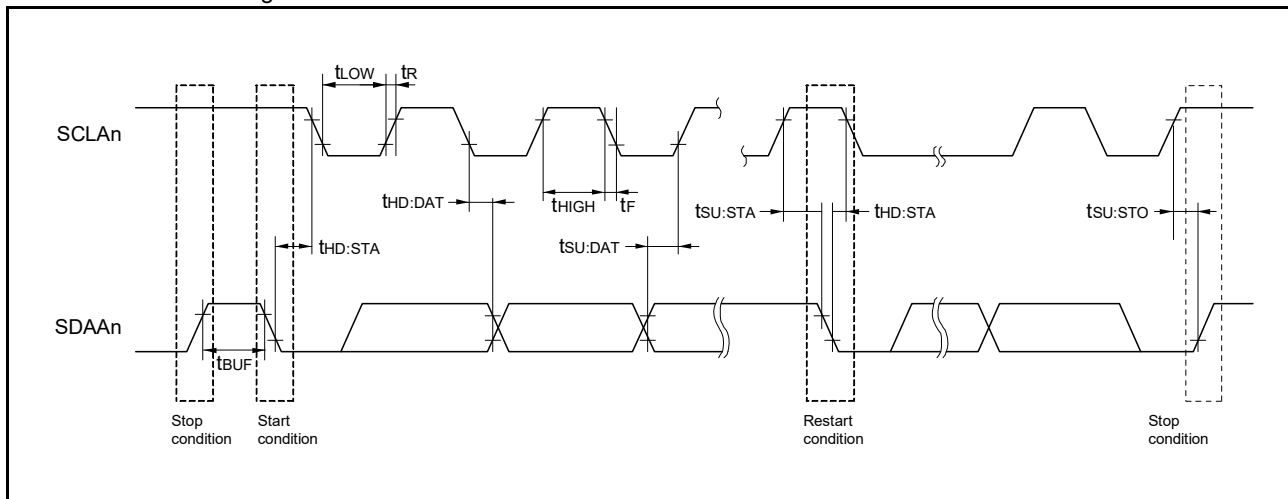
Note 1. The first clock pulse is generated after this period when the start or restart condition is detected.

Note 2. The maximum value of tHD:DAT applies to normal transfer. The clock stretching will be inserted on reception of an acknowledgment (ACK) signal.

Caution The values in the above table apply even when bit 2 (PIOR2) in the peripheral I/O redirection register (PIOR) is 1. In such cases, the pin characteristics (IOH1, IOL1, VOH1, VOL1) must satisfy the values in the redirect destination.

Remark The maximum value of communication line capacitance (C_b) and communication line pull-up resistor (R_b) are as follows.
C_b = 120 pF, R_b = 1.1 kΩ

IICA serial transfer timing



Remark n = 0, 1

2.6 Analog Characteristics

2.6.1 A/D converter characteristics

1. Normal modes 1 and 2

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$,
reference voltage (+) = AV_{REFP} ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = AV_{REFM} ($ADREFM = 1$),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES				12	bit
Conversion clock	f _{AD}		1		32	MHz
Overall error ^{Notes 1, 2, 3, 4, 5}	AINL	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±2.4	±4.5	LSB
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±2.9	±5.7	LSB
		$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±3.0	±5.8	LSB
Conversion time ^{Notes 5, 6}	t _{CONV}	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	2.0			μs
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	2.0			μs
		$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	2.0			μs
Zero-scale error ^{Notes 1, 2, 3, 4, 5, 7}	E _{ZS}	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.01	±0.08	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.01	±0.09	%FSR
		$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.03	±0.13	%FSR
Full-scale error ^{Notes 1, 2, 3, 4, 5, 7}	E _{FS}	$4.5\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.03	±0.09	%FSR
		$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.05	±0.13	%FSR
		$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±0.05	±0.13	%FSR
Analog input voltage	V _{AIN}		0		AV_{REFP}	V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. The values in the column Max. only apply in the case of a normal distribution with $\pm 3\sigma$ variation from the mean.

Note 3. We do not inspect the characteristics of the A/D converter before shipment. The listed values are only results of evaluation.

Note 4. When $AV_{REFP} < V_{DD}$, the maximum values are as follows.

Overall error/zero-scale error/full-scale error: Add (± 0.75 LSB \times (V_{DD} voltage (V) - AV_{REFP} voltage (V))) to the maximum value.

Integral linearity error: Add (± 0.2 LSB \times (V_{DD} voltage (V) - AV_{REFP} voltage (V))) to the maximum value.

Note 5. The listed values apply when the conversion resolution is set to 12 bits.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μs. Accordingly, use standard mode 2 with the longer sampling time.

Note 7. This value is indicated as a ratio (%FSR) to the full-scale value.

($T_A = -40$ to $+105^\circ\text{C}$, $2.4\text{ V} \leq \text{AVREFP} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = 0\text{ V}$,
reference voltage (+) = AVREFP ($\text{ADREFP1} = 0$, $\text{ADREFP0} = 1$), reference voltage (-) = AVREFM ($\text{ADREFM} = 1$),
target pins: ANI2 to ANI14, internal reference voltage, and temperature sensor output voltage)

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	fAD			1		32	MHz
Overall error ^{Notes 1, 2, 3, 4}	AINL	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 7.5	LSB
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 9.0	LSB
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 9.0	LSB
Conversion time ^{Note 5}	tCONV	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	2.0			μs
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	2.0			μs
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$	2.0			μs
Zero-scale error ^{Notes 1, 2, 3, 4, 6}	Ezs	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.17	%FSR
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.21	%FSR
Full-scale error ^{Notes 1, 2, 3, 4, 6}	Efs	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.17	%FSR
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.21	%FSR
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 0.21	%FSR
Integral linearity error ^{Notes 1, 3, 4}	ILE	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 3.0	LSB
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 3.0	LSB
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$			± 3.0	LSB
Differential linearity error ^{Note 1}	DLE	12-bit resolution	$4.5\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		± 1.0		LSB
			$2.7\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		± 1.0		LSB
			$2.4\text{ V} \leq \text{AVREFP} = \text{VDD} \leq 5.5\text{ V}$		± 1.0		LSB
Analog input voltage	VAIN			0		AVREFP	V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ± 3 LSB to the maximum value.

Zero-scale/full-scale error: Add $\pm 0.04\%$ FSR to the maximum value.

Note 3. When reference voltage (+) = VDD and reference voltage (-) = VSS , the maximum values are as follows.

Overall error: Add ± 10 LSB to the maximum value.

Zero-scale/full-scale error: Add $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add ± 4 LSB to the maximum value.

Note 4. When $\text{AVREFP} < \text{VDD}$, the maximum values are as follows.

Overall error/zero-scale error/full-scale error: Add $(\pm 0.75\text{ LSB} \times (\text{VDD voltage (V)} - \text{AVREFP voltage (V)}))$ to the maximum value.

Integral linearity error: Add $(\pm 0.2\text{ LSB} \times (\text{VDD voltage (V)} - \text{AVREFP voltage (V)}))$ to the maximum value.

Note 5. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least $5\ \mu\text{s}$. Accordingly, use standard mode 2 with the longer sampling time.

Note 6. This value is indicated as a ratio (%FSR) to the full-scale value.

2. Low-voltage modes 1 and 2

($T_A = -40$ to $+105^\circ\text{C}$, $1.6\text{ V} \leq AV_{REFP} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$,
reference voltage (+) = AV_{REFP} ($ADREFP1 = 0$, $ADREFP0 = 1$), reference voltage (-) = AV_{REFM} ($ADREFM = 1$),
target pins ANI2 to ANI14, internal reference voltage^{Note 1}, and temperature sensor output voltage^{Note 1})

Item	Symbol	Conditions		Min.	Typ.	Max.	Unit
Resolution	RES			8		12	Bit
Conversion clock	f _{AD}			1		24	MHz
Overall error ^{Notes 2, 3, 4, 5}	AINL	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±9	LSB
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±9	LSB
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±11.5	LSB
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±12.0	LSB
Conversion time ^{Note 6}	t _{CONV}	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	3.33			μs
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	5.0			μs
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	10.0			μs
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$	20.0			μs
Zero-scale error ^{Notes 2, 3, 4, 5, 7}	E _{ZS}	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.27	%FSR
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.28	%FSR
Full-scale error ^{Notes 2, 3, 4, 5, 7}	E _{FS}	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.21	%FSR
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.27	%FSR
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±0.28	%FSR
Integral linearity error ^{Notes 2, 4, 5}	ILE	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±4.0	LSB
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±4.0	LSB
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±4.5	LSB
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$			±4.5	LSB
Differential linearity error ^{Note 2}	DLE	12-bit resolution	$2.7\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.5		LSB
			$2.4\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±1.5		LSB
			$1.8\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±2.0		LSB
			$1.6\text{ V} \leq AV_{REFP} = V_{DD} \leq 5.5\text{ V}$		±2.0		LSB
Analog input voltage	V _{AIN}			0		AV_{REFP}	V

Note 1. If the internal reference voltage or temperature sensor output voltage is to be A/D converted, V_{DD} must be at least 1.8 V.

Note 2. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 3. When pins ANI16 to ANI31 are selected as the target pins for conversion, the maximum values are as follows.

Overall error: Add ± 3 LSB to the maximum value.

Zero-scale/full-scale error: Add $\pm 0.04\%$ FSR to the maximum value.

Note 4. When reference voltage (+) = V_{DD} and reference voltage (-) = V_{SS} , the maximum values are as follows.

Overall error: Add ± 10 LSB to the maximum value.

Zero-scale/full-scale error: Add $\pm 0.25\%$ FSR to the maximum value.

Integral linearity error: Add ± 4 LSB to the maximum value.

Note 5. When $AV_{REFP} < V_{DD}$, the maximum values are as follows.

Overall error/zero-scale error/full-scale error: Add (± 0.75 LSB \times (V_{DD} voltage (V) - AV_{REFP} voltage (V))) to the maximum value.

Integral linearity error: Add (± 0.2 LSB \times (V_{DD} voltage (V) - AV_{REFP} voltage (V))) to the maximum value.

Note 6. When the internal reference voltage or the temperature sensor output voltage is selected as the target for conversion, the sampling time must be at least 5 μ s. Accordingly, use standard mode 2 with the longer sampling time, and use the conversion clock (fAD) of no more than 16 MHz.

Note 7. This value is indicated as a ratio (%FSR) to the full-scale value.

3. When the internal reference voltage is selected as reference voltage (+)

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq V_{DD} \leq 5.5\text{ V}$, $V_{SS} = 0\text{ V}$, low-voltage modes 1 and 2,
reference voltage (+) = internal reference voltage (ADREFP1 = 1, ADREFP0 = 0),
reference voltage (-) = AVREFM (ADREFM = 1))

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES		8			Bit
Conversion clock	fAD	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$	1		2	MHz
Zero-scale error ^{Notes 1, 2, 3}	EZS	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 0.6	%FSR
Integral linearity error ^{Notes 1, 3}	ILE	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$			± 2.0	LSB
Differential linearity error ^{Note 1}	DLE	$1.6\text{ V} \leq V_{DD} \leq 5.5\text{ V}$		± 1.0		LSB
Analog input voltage	VAIN		0		VBGR Note 4	V

Note 1. This value does not include the quantization error ($\pm 1/2$ LSB).

Note 2. This value is indicated as a ratio (%FSR) to the full-scale value.

Note 3. When reference voltage (-) is selected as V_{SS} , the maximum values are as follows.

Zero-scale error: Add $\pm 0.35\%$ FSR to the maximum value.

Integral linearity error: Add ± 0.5 LSB to the maximum value.

Note 4. Refer to **2.6.2 Temperature sensor/internal reference voltage characteristics**.

2.6.2 Temperature sensor/internal reference voltage characteristics

(TA = -40 to +105°C, 1.8 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Temperature sensor output voltage	VTMPS25	Setting ADS register = 80H, TA = +25°C		1.05		V
Internal reference voltage	VBGR	Setting ADS register = 81H	1.42	1.48	1.54	V
Temperature coefficient	FVTMPS	Temperature dependency of the temperature sensor voltage		-3.3		mV/°C
Operation stabilization wait time	tAMP		5			μs

2.6.3 D/A converter characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution	RES				8	Bit
Overall error	AINL	Rload = 8 MΩ, 1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
		Rload = 4 MΩ, 1.8 V ≤ VDD ≤ 5.5 V			±2.5	LSB
Settling time	tSET	Cload = 20 pF	2.7 V ≤ VDD ≤ 5.5 V		3	μs
			1.6 V ≤ VDD ≤ 5.5 V		6	μs

2.6.4 Comparator characteristics

(TA = -40 to +105°C, 1.6 V ≤ EVDD0 = EVDD1 ≤ VDD ≤ 5.5 V, VSS = EVSS0 = EVSS1 = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input voltage range	IVREF	Input to the IVREF0 and IVREF1 pins C0LVL = 0, C1LVL = 0	0		VDD - 1.4 and EVDD0	V
		Input to the IVREF0 and IVREF1 pins C0LVL = 1, C1LVL = 1	1.4		EVDD0	V
	IVCMP	Input to the IVCMP0 and IVCMP1 pins	-0.3		EVDD0 + 0.3	V
Output delay	td	VDD = 3.0 V, Input slew rate > 1 V/μs	High-speed mode		1.5	μs
			Low-speed mode		3.0	μs
Offset voltage	—	High-speed mode			50	mV
		Low-speed mode			40	mV
Operation stabilization wait time	tCMP		30			μs
Internal reference voltage ^{Note}	VBGR2		1.4		1.6	V

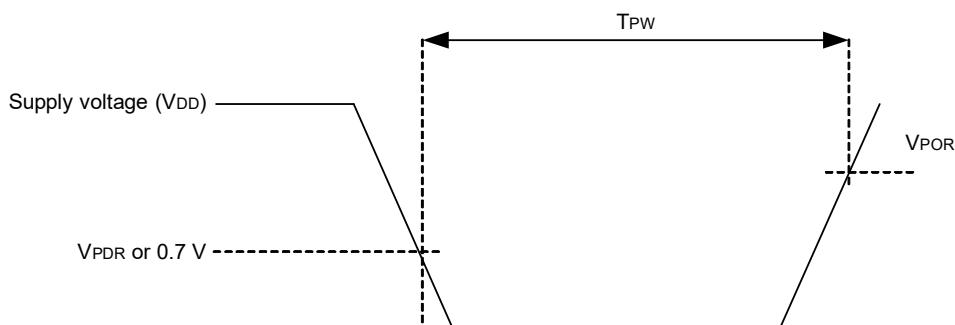
<R> **Note** The internal reference voltage can be selected as comparator reference voltage only when 1.8 V ≤ VDD ≤ 5.5 V.

2.6.5 POR circuit characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Detection voltage	V _{POR} , V _{PDR}		1.43	1.50	1.57	V
Minimum pulse width ^{Note}	T _{PW}		300			μs

Note This width is the minimum time required for a POR reset when V_{DD} falls below V_{PDR}. This width is also the minimum time required for a POR reset from when V_{DD} falls below 0.7 V to when V_{DD} exceeds V_{POR} in the STOP mode or while the main system clock is stopped through setting bit 0 (HIOSTOP) and bit 7 (MSTOP) in the clock operation status control register (CSC).



2.6.6 LVD circuit characteristics

1. LVD0 Detection Voltage in the Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	Conditions	Min.	Typ.	Max.	Unit		
Detection voltage	Supply voltage level	VLVD00	The power supply voltage is rising.	3.84	3.96	4.08	V		
			The power supply voltage is falling.	3.76	3.88	4.00	V		
		VLVD01	The power supply voltage is rising.	2.88	2.97	3.06	V		
			The power supply voltage is falling.	2.82	2.91	3.00	V		
		VLVD02	The power supply voltage is rising.	2.59	2.67	2.75	V		
			The power supply voltage is falling.	2.54	2.62	2.70	V		
		VLVD03	The power supply voltage is rising.	2.31	2.38	2.45	V		
			The power supply voltage is falling.	2.26	2.33	2.40	V		
		VLVD04	The power supply voltage is rising.	1.84	1.90	1.95	V		
			The power supply voltage is falling.	1.80	1.86	1.91	V		
		VLVD05	The power supply voltage is rising.	1.64	1.69	1.74	V		
			The power supply voltage is falling.	1.60	1.65	1.70	V		
		Minimum pulse width		tLW		500			μs
		Detection delay time						500	μs

2. LVD1 Detection Voltage of Reset Mode and Interrupt Mode

(TA = -40 to +105°C, VPDR ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Detection voltage	Supply voltage level	VLVD10	The power supply voltage is rising.	4.08	4.16	4.24	V
			The power supply voltage is falling.	4.00	4.08	4.16	V
		VLVD11	The power supply voltage is rising.	3.88	3.96	4.04	V
			The power supply voltage is falling.	3.80	3.88	3.96	V
		VLVD12	The power supply voltage is rising.	3.68	3.75	3.82	V
			The power supply voltage is falling.	3.60	3.67	3.74	V
		VLVD13	The power supply voltage is rising.	3.48	3.55	3.62	V
			The power supply voltage is falling.	3.40	3.47	3.54	V
		VLVD14	The power supply voltage is rising.	3.28	3.35	3.42	V
			The power supply voltage is falling.	3.20	3.27	3.34	V
		VLVD15	The power supply voltage is rising.	3.07	3.13	3.19	V
			The power supply voltage is falling.	3.00	3.06	3.12	V
		VLVD16	The power supply voltage is rising.	2.91	2.97	3.03	V
			The power supply voltage is falling.	2.85	2.91	2.97	V
		VLVD17	The power supply voltage is rising.	2.76	2.82	2.87	V
			The power supply voltage is falling.	2.70	2.76	2.81	V
		VLVD18	The power supply voltage is rising.	2.61	2.66	2.71	V
			The power supply voltage is falling.	2.55	2.60	2.65	V
		VLVD19	The power supply voltage is rising.	2.45	2.50	2.55	V
			The power supply voltage is falling.	2.40	2.45	2.50	V
		VLVD110	The power supply voltage is rising.	2.35	2.40	2.45	V
			The power supply voltage is falling.	2.30	2.35	2.40	V
		VLVD111	The power supply voltage is rising.	2.25	2.30	2.34	V
			The power supply voltage is falling.	2.20	2.25	2.29	V
		VLVD112	The power supply voltage is rising.	2.15	2.20	2.24	V
			The power supply voltage is falling.	2.10	2.15	2.19	V
		VLVD113	The power supply voltage is rising.	2.05	2.09	2.13	V
			The power supply voltage is falling.	2.00	2.04	2.08	V
		VLVD114	The power supply voltage is rising.	1.94	1.98	2.02	V
			The power supply voltage is falling.	1.90	1.94	1.98	V
		VLVD115 Note	The power supply voltage is rising.	1.84	1.88	1.91	V
			The power supply voltage is falling.	1.80	1.84	1.87	V
		VLVD116 Note	The power supply voltage is rising.	1.74	1.78	1.81	V
			The power supply voltage is falling.	1.70	1.74	1.77	V
VLVD117 Note	The power supply voltage is rising.	1.64	1.67	1.70	V		
	The power supply voltage is falling.	1.60	1.63	1.66	V		
Minimum pulse width	tLW		500			μs	
Detection delay time					500	μs	

Note This setting can only be used when LVD0 is disabled.

2.6.7 Power supply voltage rising slope characteristics

(TA = -40 to +105°C, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power supply voltage rising slope	SVDD				54	V/ms

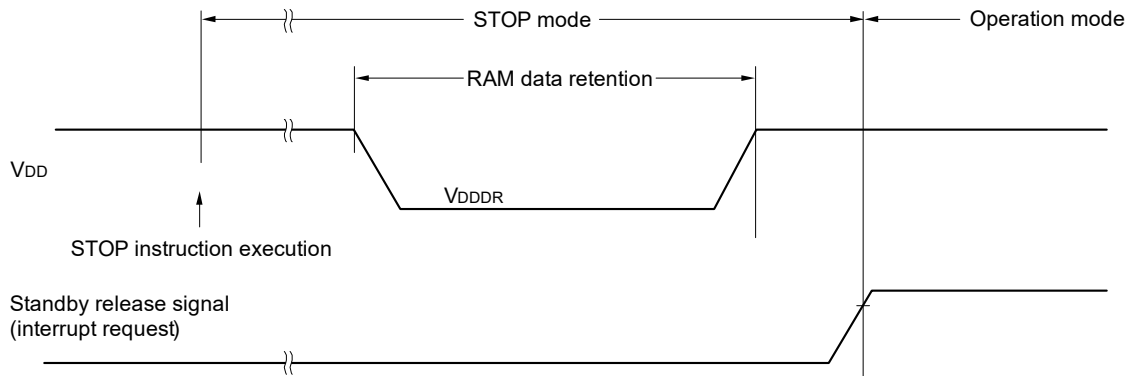
Caution Make sure to keep the internal reset state by the LVD0 circuit or an external reset until VDD reaches the operating voltage range shown in AC characteristics.

2.7 RAM Data Retention Characteristics

(TA = -40 to +105°C, VSS = 0V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Data retention supply voltage	VDDDR		1.43 ^{Note}		5.5	V

Note This voltage depends on the POR detection voltage. When the voltage drops, the data in RAM are retained until a POR is applied, but are not retained following a POR.



2.8 Flash Memory Programming Characteristics

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU/peripheral hardware clock frequency	fCLK		1		32	MHz
Number of code flash rewrites ^{Notes 1, 2, 3}	C _{erwr}	Retained for 20 years TA = +85°C	1,000			Times
Number of data flash rewrites ^{Notes 1, 2, 3}		Retained for 1 year TA = +25°C		1,000,000		
		Retained for 5 years TA = +85°C	100,000			
		Retained for 20 years TA = +85°C	10,000			

Note 1. 1 erase + 1 write after the erase is regarded as 1 rewrite. The retaining years are until next rewrite after the rewrite.

Note 2. The listed numbers of times apply when using flash memory programmer and Renesas Electronics self programming library.

Note 3. These are the characteristics of the flash memory and the results obtained from reliability testing by Renesas Electronics Corporation.

1. Code flash memory

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	4 bytes	tP4	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs
Erase time	2 Kbytes	tE2K	—	10.4	312.2	—	7.7	258.5	—	6.4	231.8	—	5.8	218.4	—	5.6	214.4	ms
Blank checking time	4 bytes	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	2 Kbytes	tBC2K	—	—	2618.9	—	—	1309.5	—	—	658.3	—	—	332.8	—	—	234.1	μs
Time taken to forcibly stop the erasure		tSED	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Security setting time		tAWSSAS	—	18.2	526.2	—	14.4	469.2	—	12.5	441.1	—	11.6	427.1	—	11.3	422.6	ms
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2. Data flash memory

(TA = -40 to +105°C, 1.6 V ≤ VDD ≤ 5.5 V, VSS = 0 V)

Item		Symbol	fCLK = 1 MHz			fCLK = 2 MHz, 3 MHz			4 MHz ≤ fCLK < 8 MHz			8 MHz ≤ fCLK < 32 MHz			fCLK = 32 MHz			Unit
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Programming time	1 byte	tP4	—	74.7	656.5	—	51.0	464.6	—	41.7	384.8	—	37.1	346.2	—	34.2	321.9	μs
Erase time	256 bytes	tE2K	—	7.8	259.2	—	6.4	232.0	—	5.8	218.5	—	5.5	211.8	—	5.4	209.7	ms
Blank checking time	1 byte	tBC4	—	—	38.4	—	—	19.2	—	—	13.1	—	—	10.2	—	—	8.3	μs
	256 bytes	tBC2K	—	—	1326.1	—	—	663.1	—	—	335.1	—	—	171.2	—	—	121.0	μs
Time taken to forcibly stop the erasure		tSED	—	—	18.0	—	—	14.0	—	—	12.0	—	—	11.0	—	—	10.3	μs
Time until programming starts following cancellation of the STOP instruction		—	20	—	—	20	—	—	20	—	—	20	—	—	20	—	—	μs
Time until reading starts following setting DFLEN to 1		—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	0.25	—	—	μs

Caution The listed values do not include the time until the operations of the flash memory start following execution of an instruction by software.

2.9 Dedicated Flash Memory Programmer Communication (UART)

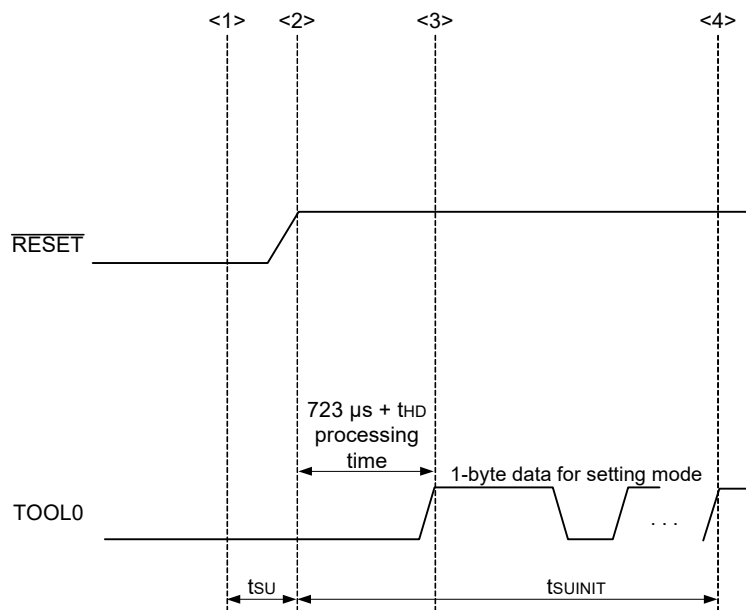
($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transfer rate		During serial programming	115,200		1,000,000	bps

2.10 Timing of Entry to Flash Memory Programming Modes

($T_A = -40$ to $+105^\circ\text{C}$, $1.8\text{ V} \leq \text{EVDD0} = \text{EVDD1} \leq \text{VDD} \leq 5.5\text{ V}$, $\text{VSS} = \text{EVSS0} = \text{EVSS1} = 0\text{ V}$)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Time to complete the communication for the initial setting after the external reset is released	tsuINIT	POR and LVD reset must be released before the external reset is released.			100	ms
Time to release the external reset after the TOOL0 pin is set to the low level	tsu	POR and LVD reset must be released before the external reset is released.	10			μs
Time to hold the TOOL0 pin at the low level after the external reset is released (the processing time of the firmware to control the flash memory is not included)	tHD	POR and LVD reset must be released before the external reset is released.	1			ms



- <1> The low level is input to the TOOL0 pin.
- <2> The external reset is released. Note that the POR and LVD reset must be released before the external reset is released.
- <3> The TOOL0 pin is set to the high level.
- <4> Setting of the flash memory programming mode by UART reception and complete the baud rate setting.

Remark tsuINIT : The time during which the communications for the initial setting must be completed within 100 ms after the external reset is released.

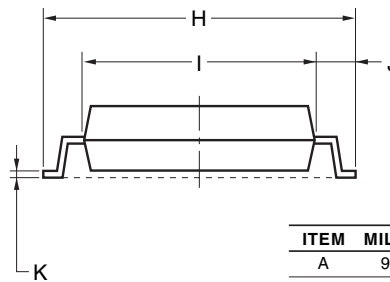
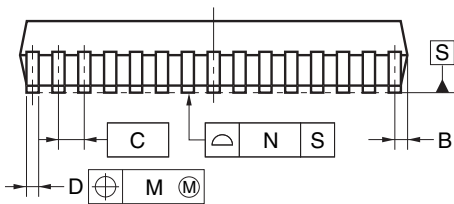
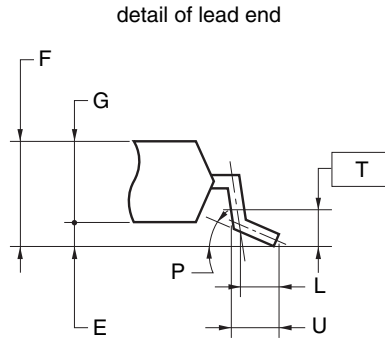
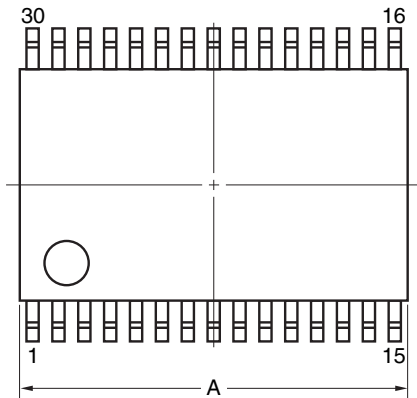
tsu : Time to release the external reset after the TOOL0 pin is set to the low level

tHD : Time to hold the TOOL0 pin at the low level after the external reset is released. It does not include the processing time of the firmware to control the flash memory.

3. Package Drawings

3.1 30-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LSSOP30-0300-0.65	PLSP0030JB-B	S30MC-65-5A4-3	0.18



NOTE

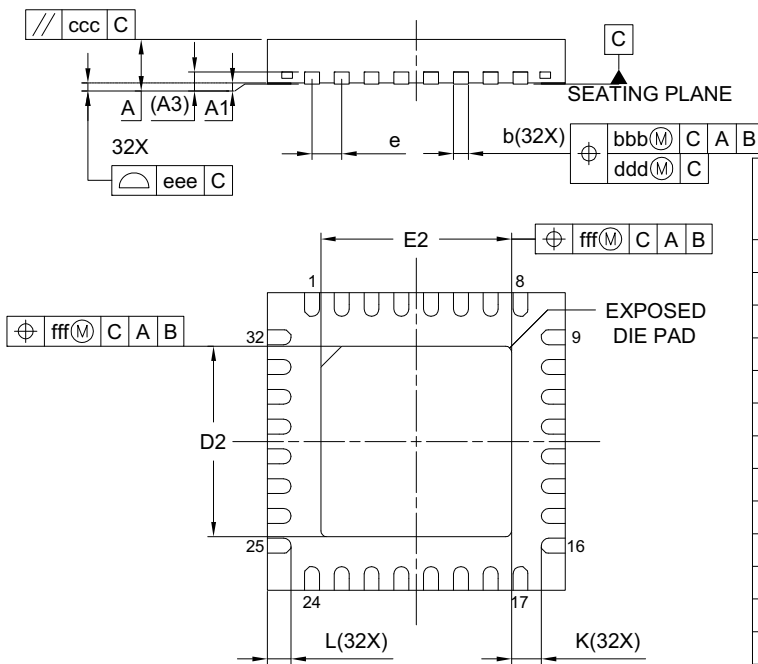
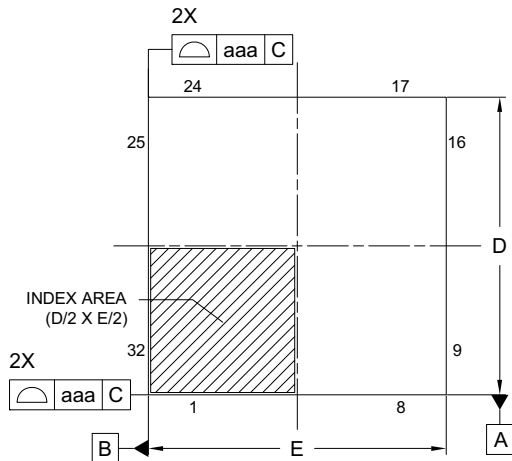
Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	9.85±0.15
B	0.45 MAX.
C	0.65 (T.P.)
D	0.24 ^{+0.08} _{-0.07}
E	0.1±0.05
F	1.3±0.1
G	1.2
H	8.1±0.2
I	6.1±0.2
J	1.0±0.2
K	0.17±0.03
L	0.5
M	0.13
N	0.10
P	3° ^{+5°} _{-3°}
T	0.25
U	0.6±0.15

©2012 Renesas Electronics Corporation. All rights reserved.

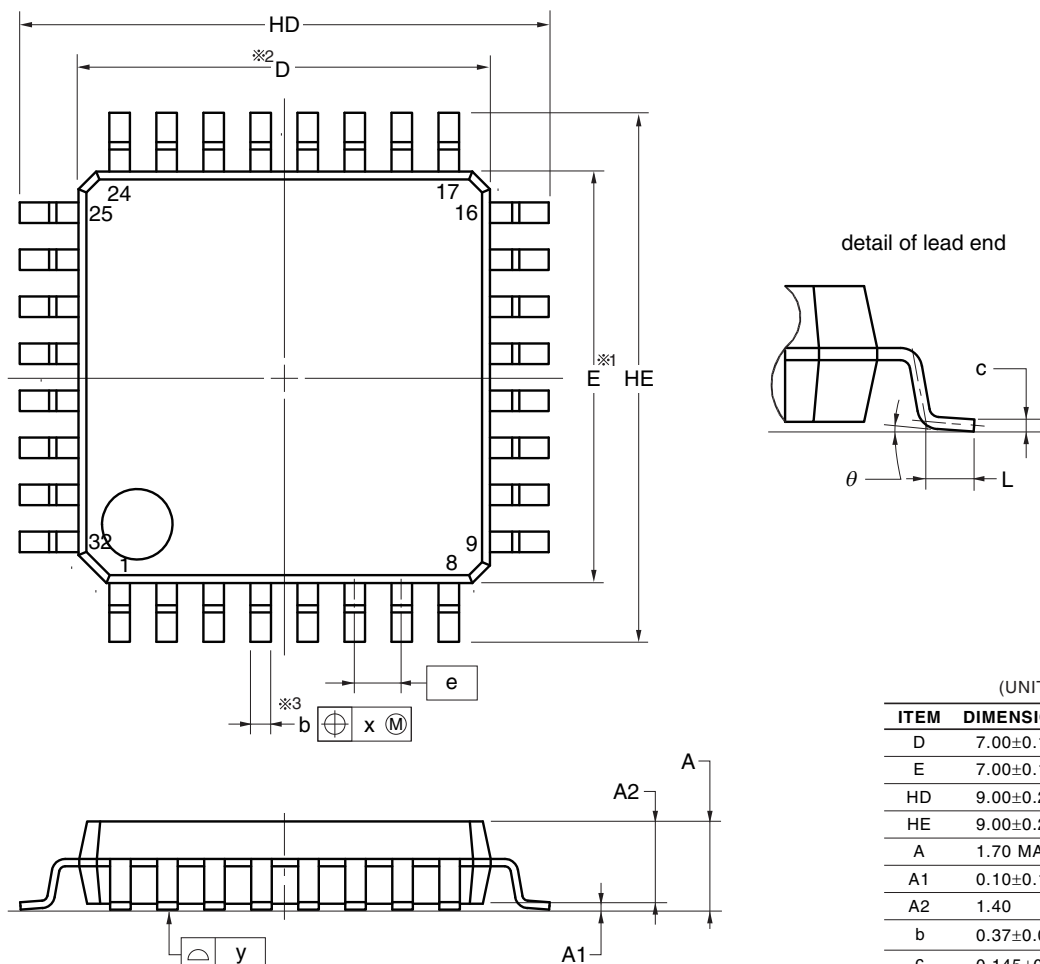
3.2 32-pin Products

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN032-5x5-0.50	PWQN0032KE-A	0.06



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A ₁	0.00	0.02	0.05
A ₃	0.203 REF.		
b	0.18	0.25	0.30
D	5.00 BSC		
E	5.00 BSC		
e	0.50 BSC		
L	0.35	0.40	0.45
K	0.20	—	—
D ₂	3.15	3.20	3.25
E ₂	3.15	3.20	3.25
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP32-7x7-0.80	PLQP0032GB-A	P32GA-80-GBT-1	0.2



(UNIT:mm)

ITEM	DIMENSIONS
D	7.00±0.10
E	7.00±0.10
HD	9.00±0.20
HE	9.00±0.20
A	1.70 MAX.
A1	0.10±0.10
A2	1.40
b	0.37±0.05
c	0.145±0.055
L	0.50±0.20
θ	0° to 8°
e	0.80
x	0.20
y	0.10

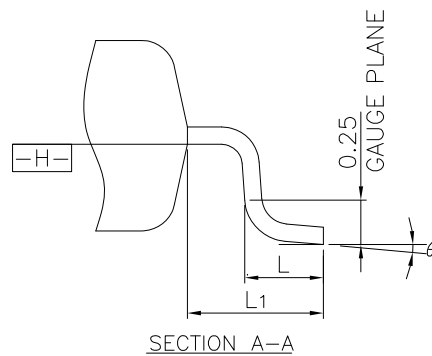
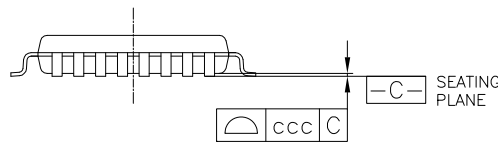
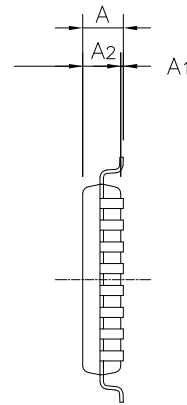
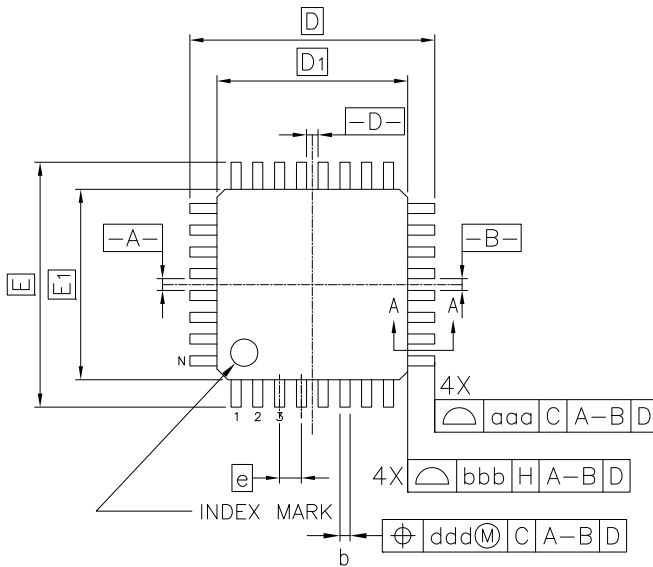
NOTE

1. Dimensions “※1” and “※2” do not include mold flash.
2. Dimension “※3” does not include trim offset.

© 2012 Renesas Electronics Corporation. All rights reserved.

<R>

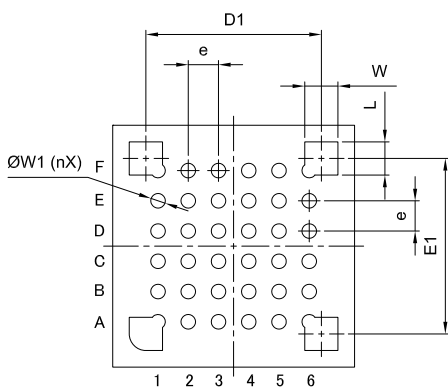
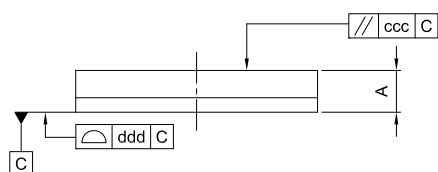
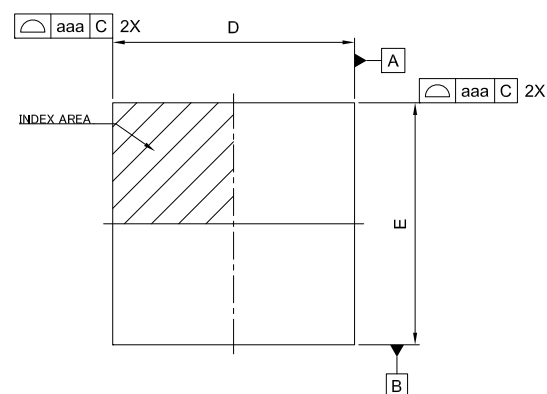
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP32-7x7-0.80	PLQP0032GE-A	0.18



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.60
A ₁	0.05	—	0.15
A ₂	1.35	1.40	1.45
D	—	9.00	—
D ₁	—	7.00	—
E	—	9.00	—
E ₁	—	7.00	—
N	—	32	—
e	—	0.80	—
b	0.30	0.37	0.45
c	0.09	—	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L ₁	—	1.00	—
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.10
ddd	—	—	0.20

3.3 36-pin Products

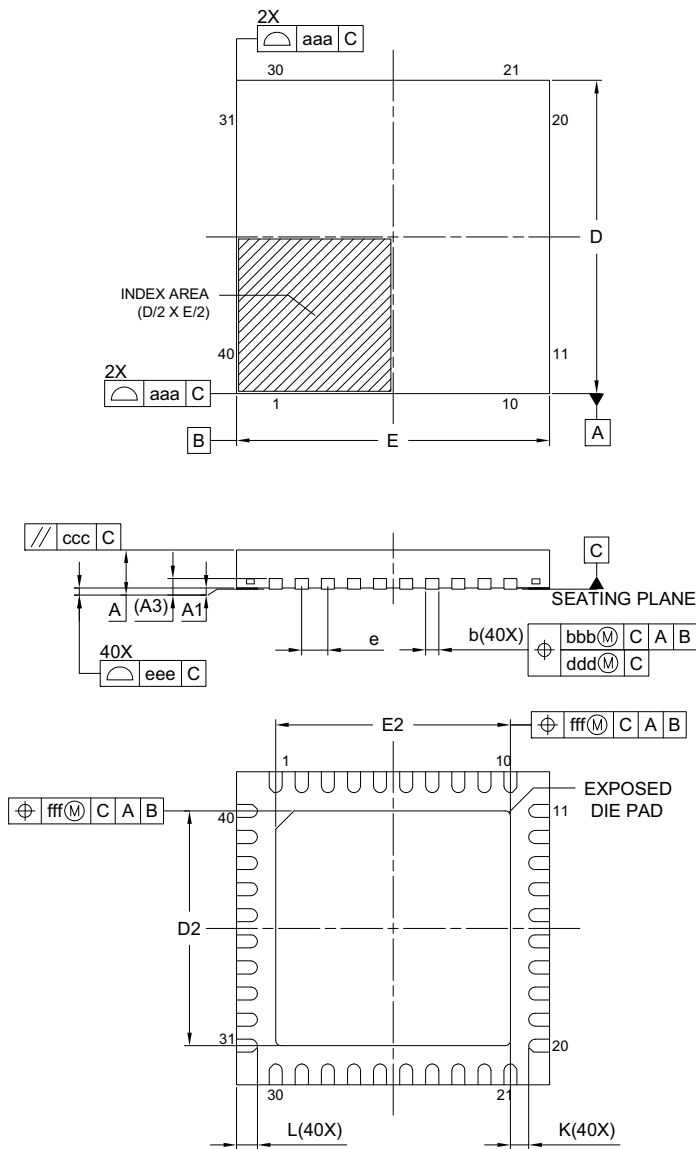
JEITA Package Code	RENESAS Code	MASS (Typ.) [g]
P-WFLGA36-4 × 4-0.50	PWL0036KB-A	0.02



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	4.00	—
E	—	4.00	—
D1	2.90 BSC		
E1	2.90 BSC		
A	—	—	0.76
W1	0.19	0.24	0.29
W	—	0.55	—
L	—	0.55	—
e	0.50 BSC		
aaa	0.10		
ccc	0.20		
ddd	0.08		
n	—	36	—

3.4 40-pin Products

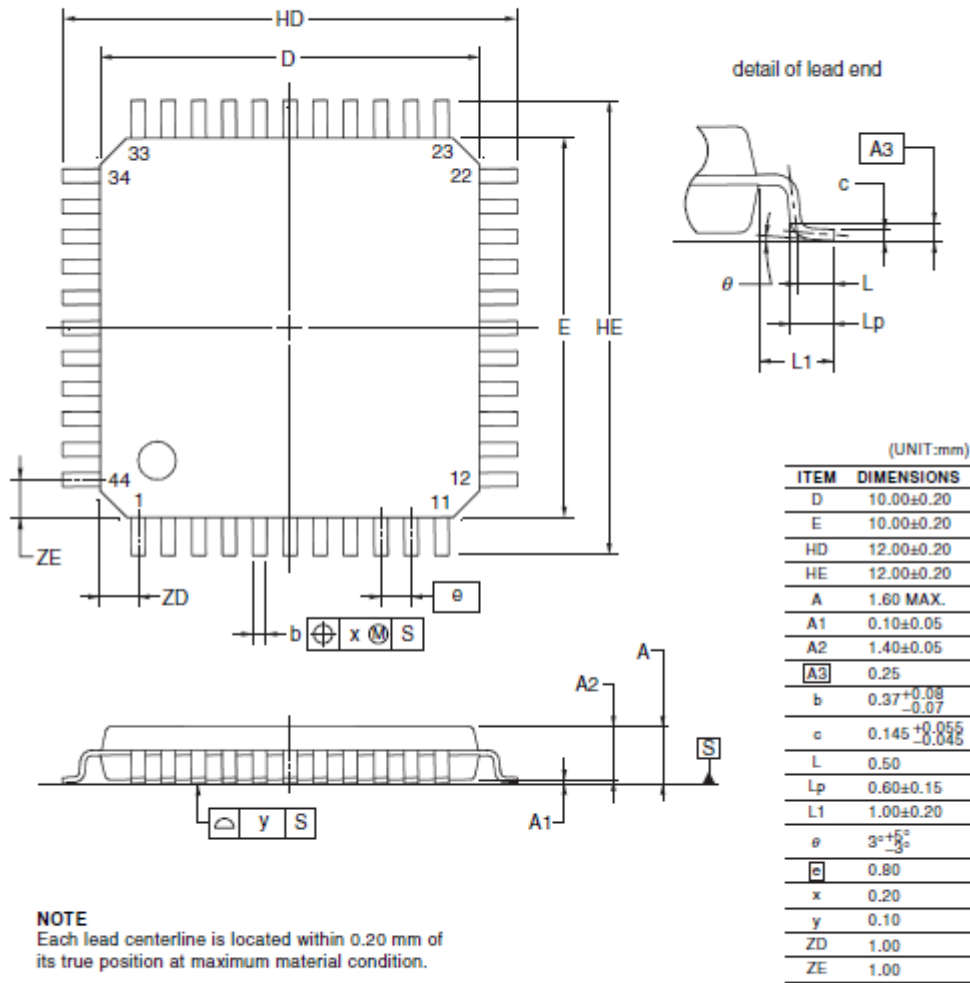
JEITA Package code	RENESAS code	MASS (TYP.)[g]
P-HWQFN040-6x6-0.50	PWQN0040KD-A	0.08



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A ₁	0.00	0.02	0.05
A ₃	0.203 REF.		
b	0.18	0.25	0.30
D	6.00 BSC		
E	6.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D ₂	4.45	4.50	4.55
E ₂	4.45	4.50	4.55
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

3.5 44-pin Products

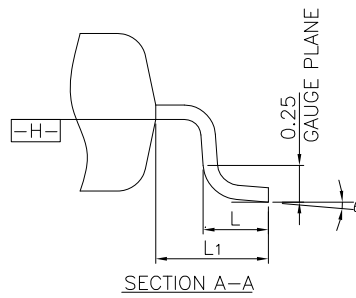
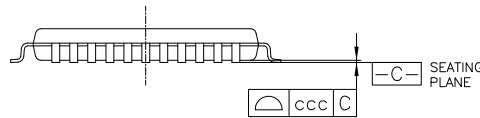
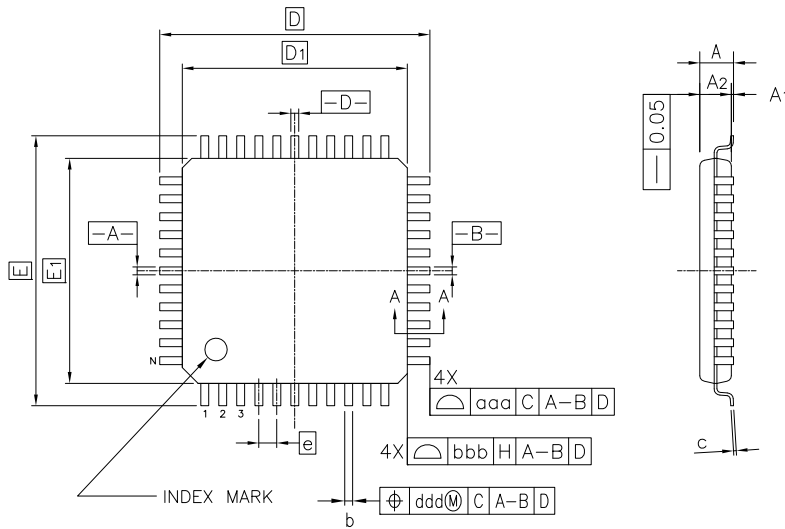
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP44-10x10-0.80	PLQP0044GC-A	P44GB-80-UES-2	0.36



© 2012 Renesas Electronics Corporation. All rights reserved.

<R>

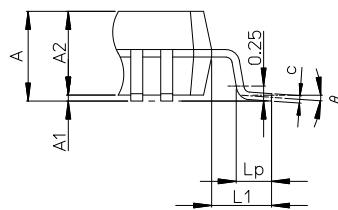
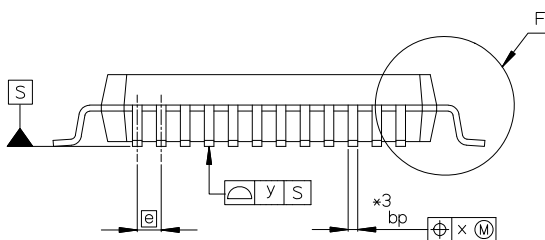
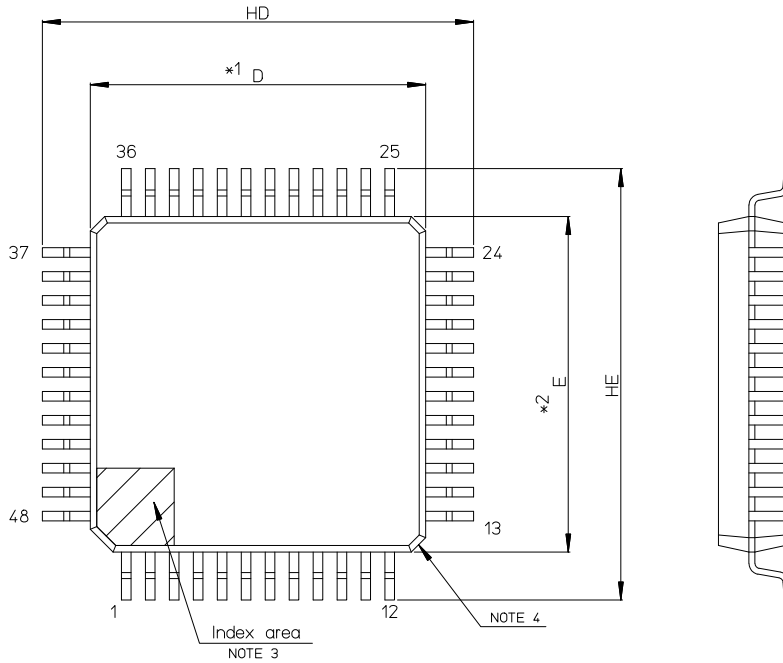
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LQFP044-10x10-0.80	PLQP0044GE-A	0.34



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.60
A ₁	0.05	—	0.15
A ₂	1.35	1.40	1.45
D	—	12.00	—
D ₁	—	10.00	—
E	—	12.00	—
E ₁	—	10.00	—
N	—	44	—
e	—	0.80	—
b	0.30	0.37	0.45
c	0.09	—	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L ₁	—	1.00	—
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.10
ddd	—	—	0.20

3.6 48-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-LFQFP48-7x7-0.50	PLQP0048KB-B	—	0.2g



Detail F

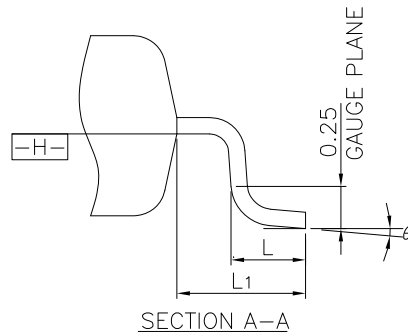
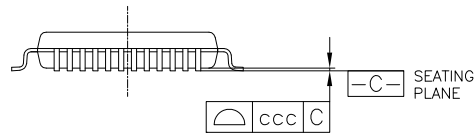
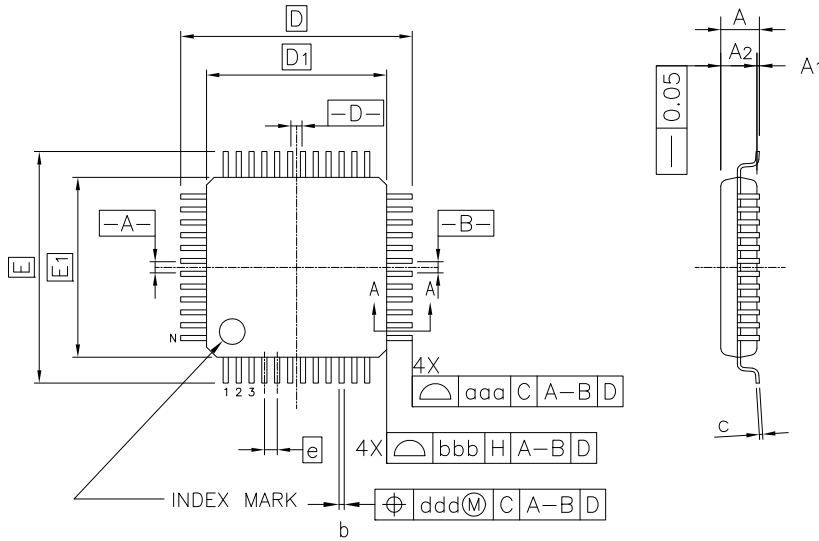
NOTE1)

1. DIMENSIONS *1' AND *2' DO NOT INCLUDE MOLD FLASH.
2. DIMENSION *3' DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	6.9	7.0	7.1
E	6.9	7.0	7.1
A2	—	1.4	—
HD	8.8	9.0	9.2
HE	8.8	9.0	9.2
A	—	—	1.7
A1	0.05	—	0.15
bp	0.17	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Lp	0.45	0.6	0.75
L1	—	1.0	—

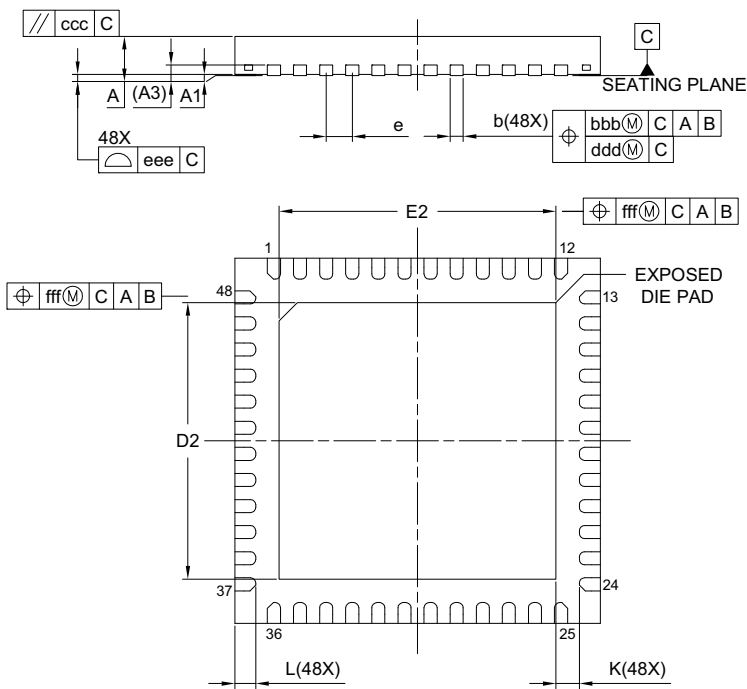
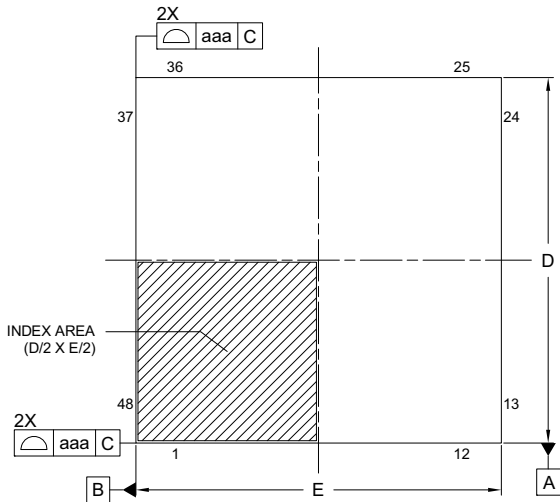
<R>

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP48-7x7-0.50	PLQP0048KL-A	0.18



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.60
A ₁	0.05	—	0.15
A ₂	1.35	1.40	1.45
D	—	9.00	—
D ₁	—	7.00	—
E	—	9.00	—
E ₁	—	7.00	—
N	—	48	—
e	—	0.50	—
b	0.17	0.22	0.27
c	0.09	—	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L ₁	—	1.00	—
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

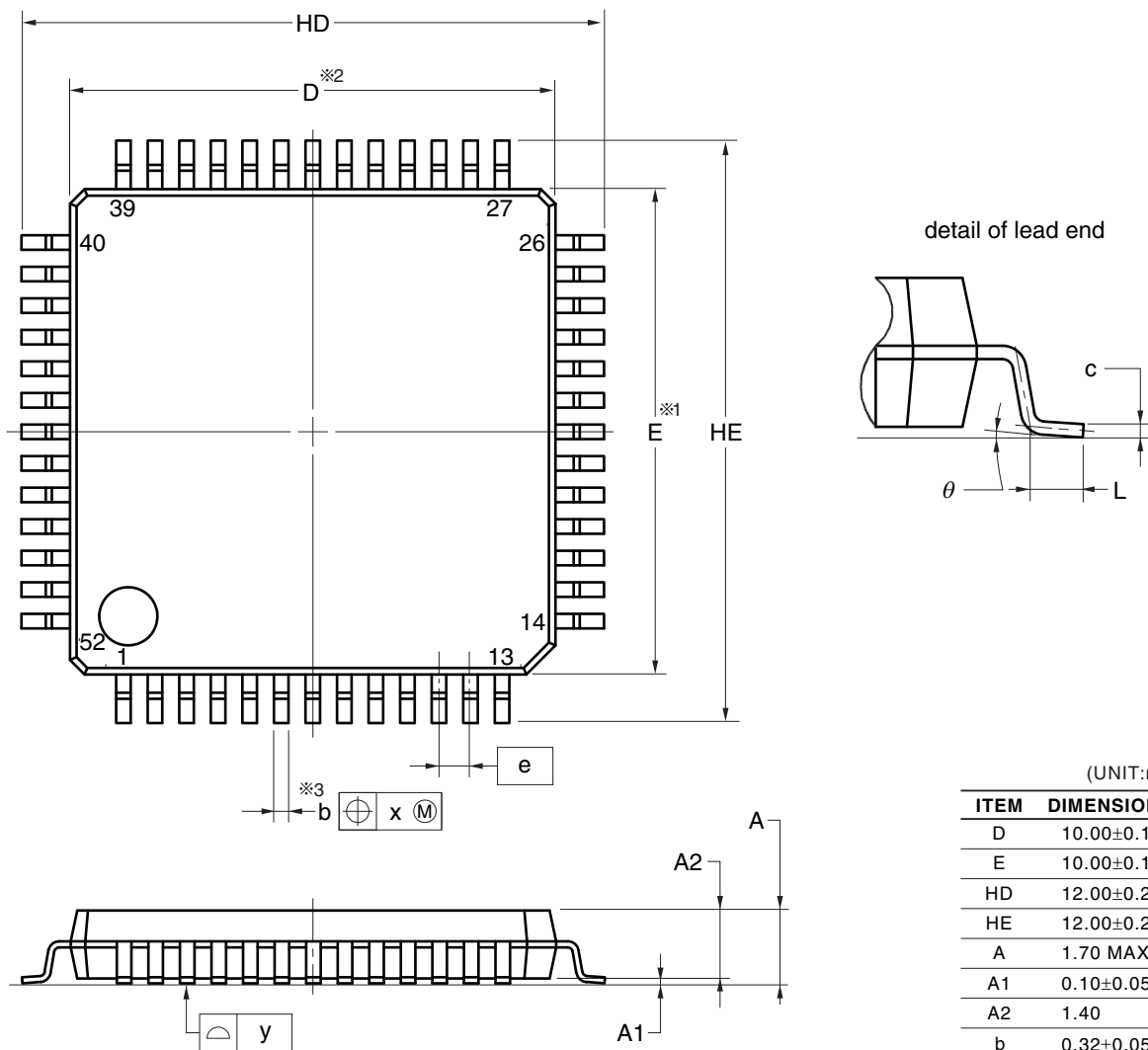
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-HWQFN048-7x7-0.50	PWQN0048KC-A	0.13 g



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	0.80
A ₁	0.00	0.02	0.05
A ₃	0.203 REF.		
b	0.20	0.25	0.30
D	7.00 BSC		
E	7.00 BSC		
e	0.50 BSC		
L	0.30	0.40	0.50
K	0.20	—	—
D ₂	5.25	5.30	5.35
E ₂	5.25	5.30	5.35
aaa	0.15		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		

3.7 52-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP52-10x10-0.65	PLQP0052JA-A	P52GB-65-GBS-1	0.3



(UNIT:mm)

ITEM	DIMENSIONS
D	10.00±0.10
E	10.00±0.10
HD	12.00±0.20
HE	12.00±0.20
A	1.70 MAX.
A1	0.10±0.05
A2	1.40
b	0.32±0.05
c	0.145±0.055
L	0.50±0.15
θ	0° to 8°
e	0.65
x	0.13
y	0.10

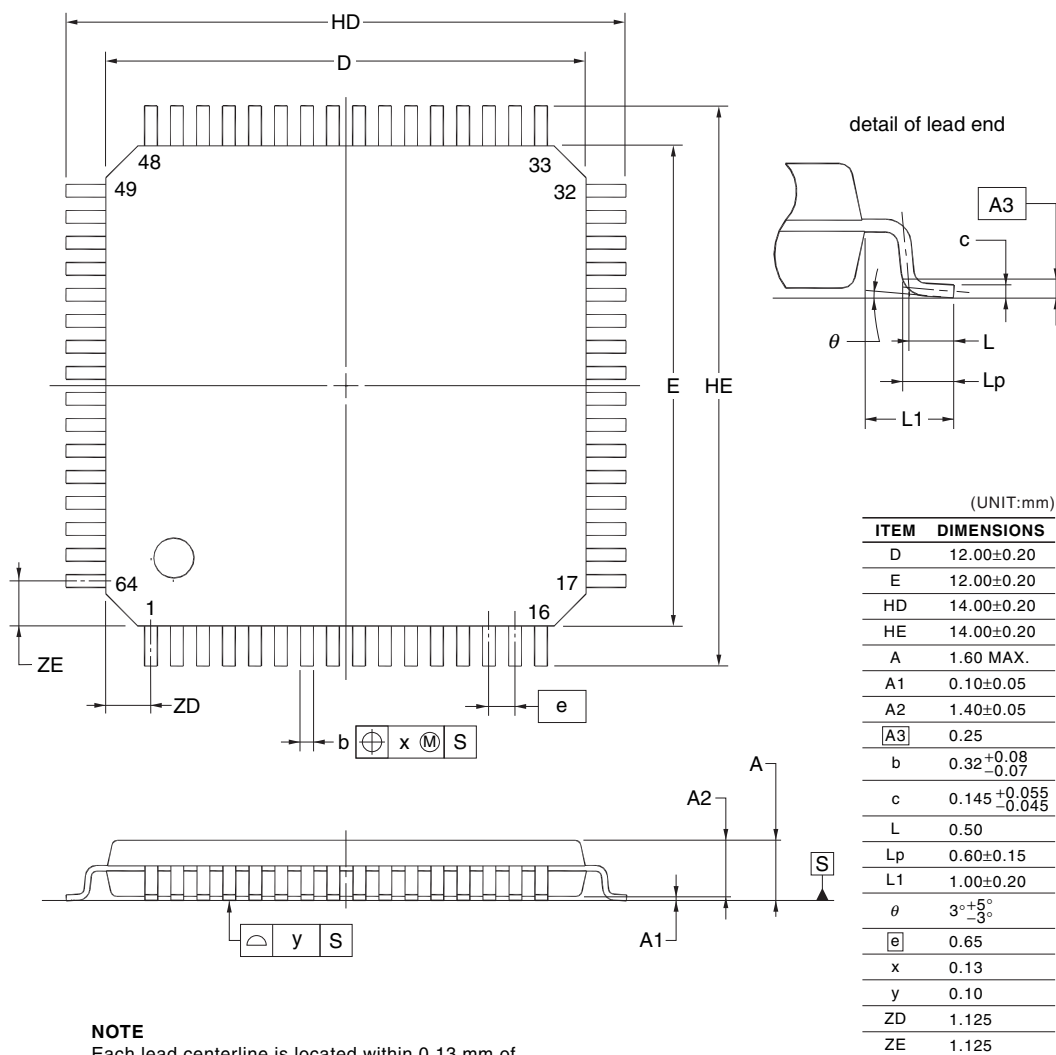
NOTE

1. Dimensions “※1” and “※2” do not include mold flash.
2. Dimension “※3” does not include trim offset.

© 2012 Renesas Electronics Corporation. All rights reserved.

3.8 64-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP64-12x12-0.65	PLQP0064JA-A	P64GK-65-UET-2	0.51

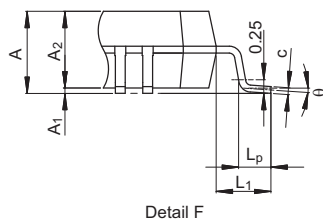
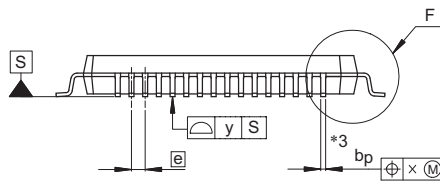
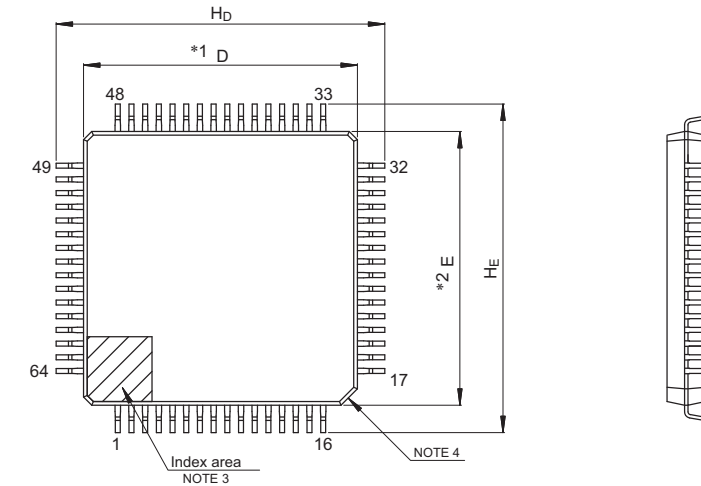


NOTE
Each lead centerline is located within 0.13 mm of its true position at maximum material condition.

©2012 Renesas Electronics Corporation. All rights reserved.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP64-10x10-0.50	PLQP0064KB-C	—	0.3

Unit: mm



NOTE)

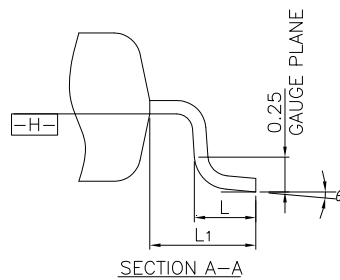
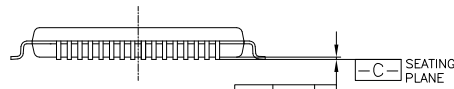
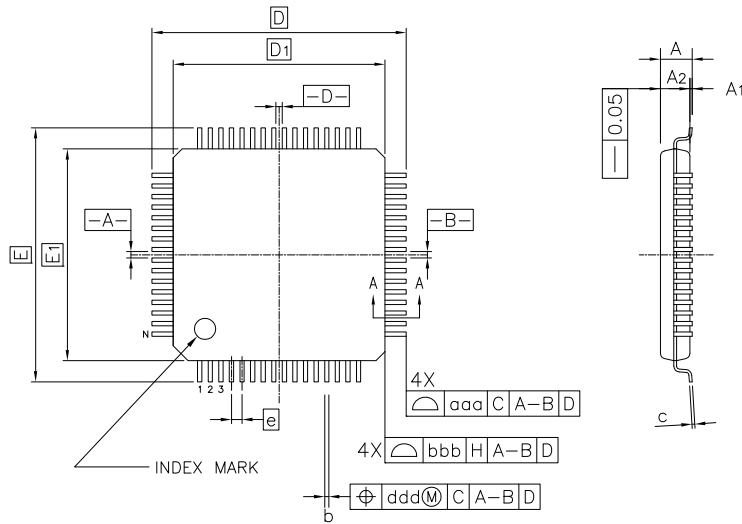
1. DIMENSIONS "**1" AND "**2" DO NOT INCLUDE MOLD FLASH.
2. DIMENSION "**3" DOES NOT INCLUDE TRIM OFFSET.
3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	9.9	10.0	10.1
E	9.9	10.0	10.1
A ₂	—	1.4	—
H _D	11.8	12.0	12.2
H _E	11.8	12.0	12.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

© 2015 Renesas Electronics Corporation. All rights reserved.

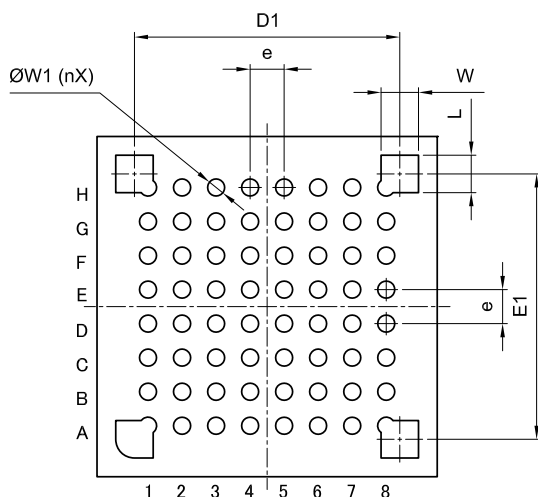
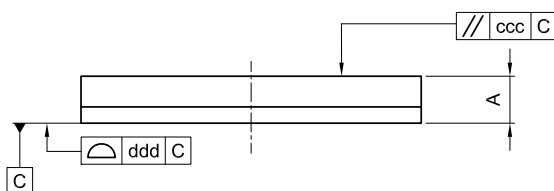
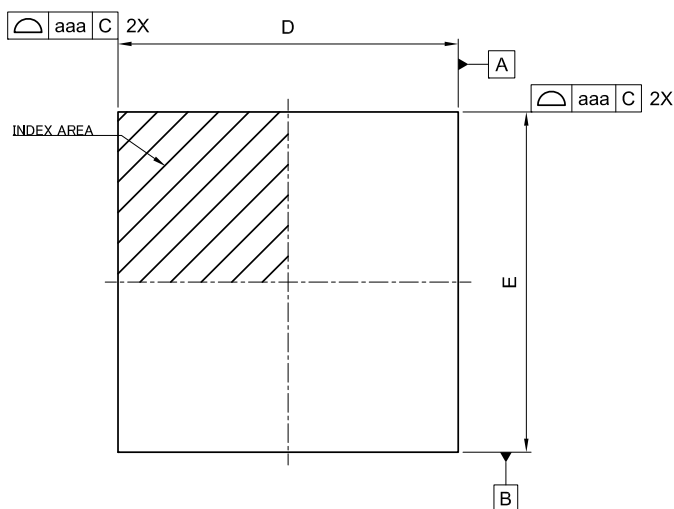
<R>

JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-LFQFP064-10x10-0.50	PLQP0064KL-A	0.36



Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
A	—	—	1.60
A ₁	0.05	—	0.15
A ₂	1.35	1.40	1.45
D	—	12.00	—
D ₁	—	10.00	—
E	—	12.00	—
E ₁	—	10.00	—
N	—	64	—
e	—	0.50	—
b	0.17	0.22	0.27
c	0.09	—	0.20
θ	0°	3.5°	7°
L	0.45	0.60	0.75
L ₁	—	1.00	—
aaa	—	—	0.20
bbb	—	—	0.20
ccc	—	—	0.08
ddd	—	—	0.08

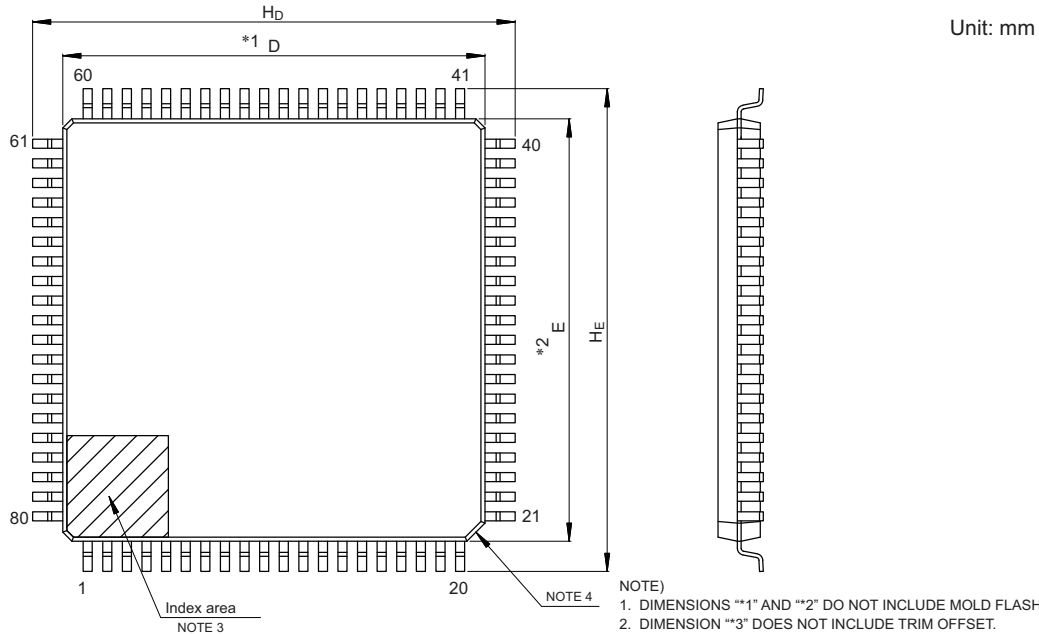
JEITA Package code	RENESAS code	MASS(TYP.)[g]
P-WFLGA64-5x5-0.50	PWLG0064KB-A	0.035



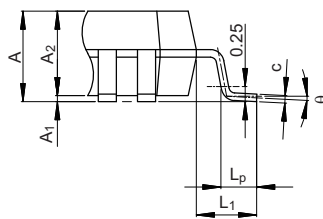
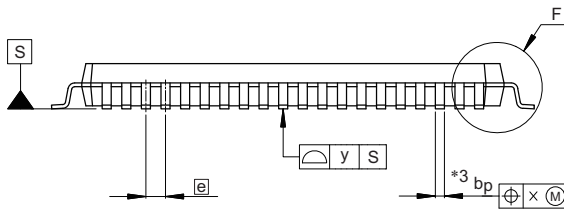
Reference Symbol	Dimension in Millimeters		
	Min.	Nom.	Max.
D	—	5.00	—
E	—	5.00	—
D1	3.90 BSC		
E1	3.90 BSC		
A	—	—	0.76
W1	0.21	0.25	0.29
W	—	0.55	—
L	—	0.55	—
e	0.50 BSC		
aaa	—	—	0.10
ccc	—	—	0.20
ddd	—	—	0.08
n	—	64	—

3.9 80-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LQFP80-14x14-0.65	PLQP0080JA-B	—	0.6



- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.

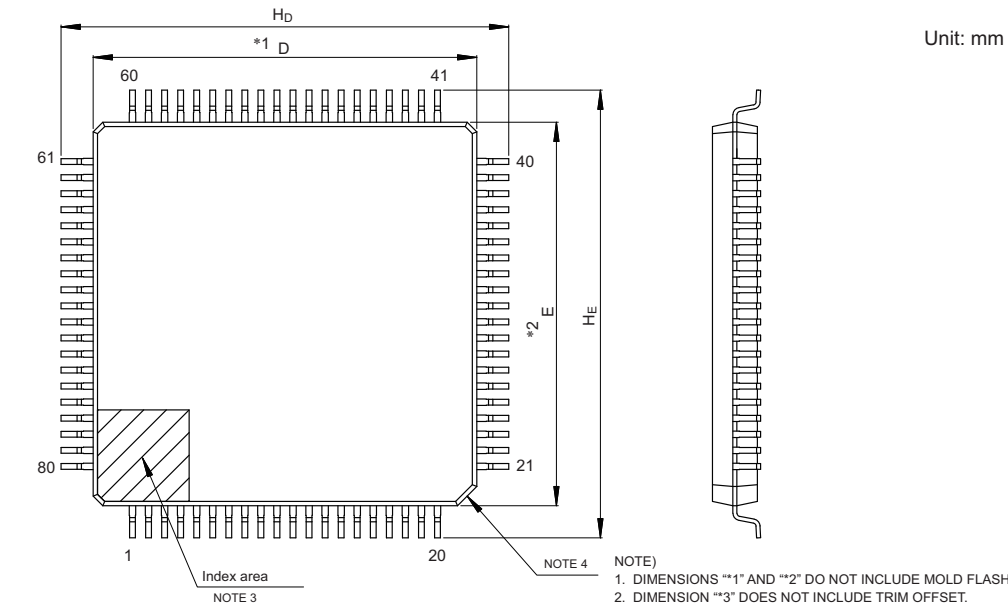


Detail F

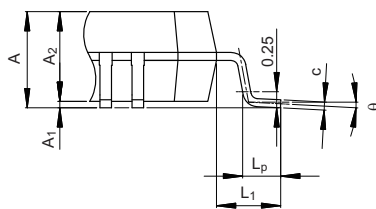
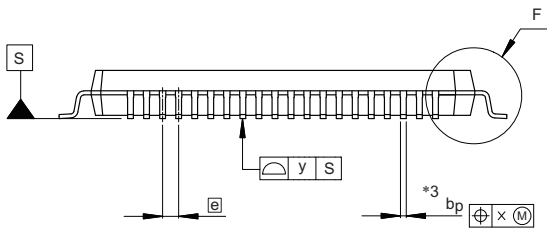
Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.22	0.30	0.38
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.65	—
x	—	—	0.13
y	—	—	0.10
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

© 2016 Renesas Electronics Corporation. All rights reserved.

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP80-12x12-0.50	PLQP0080KB-B	—	0.5



- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



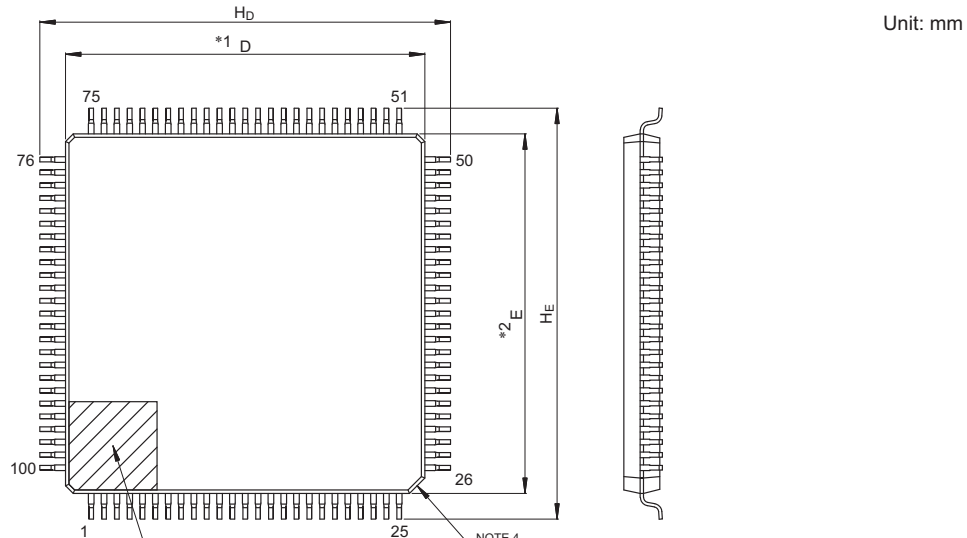
Detail F

Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	11.9	12.0	12.1
E	11.9	12.0	12.1
A ₂	—	1.4	—
H _D	13.8	14.0	14.2
H _E	13.8	14.0	14.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
[e]	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

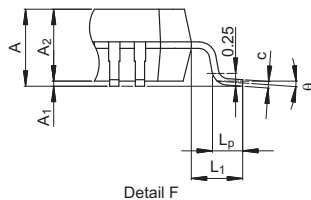
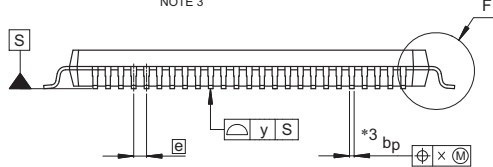
© 2017 Renesas Electronics Corporation. All rights reserved.

3.10 100-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (Typ) [g]
P-LFQFP100-14x14-0.50	PLQP0100KB-B	—	0.6



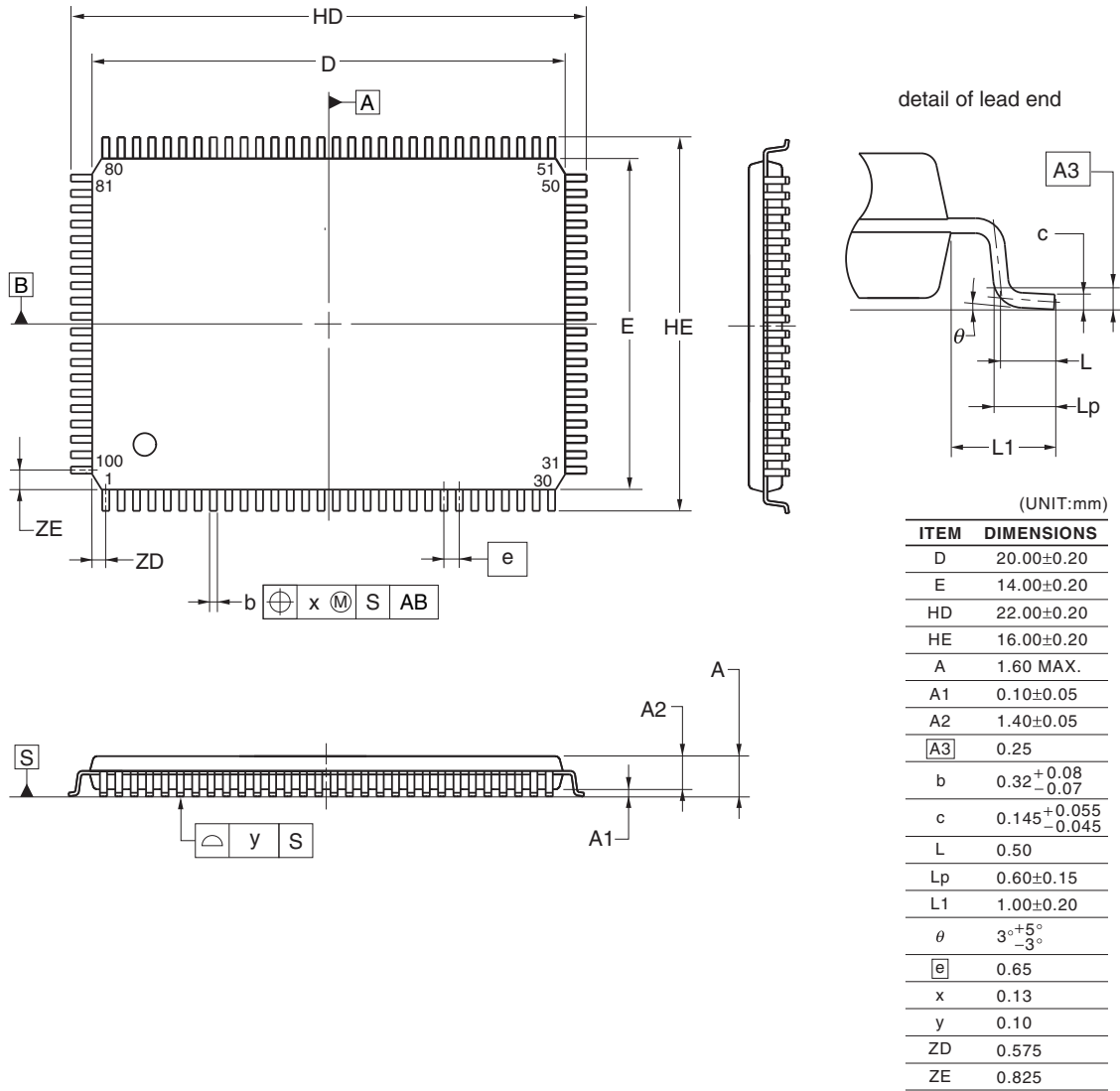
- NOTE)
1. DIMENSIONS **1" AND **2" DO NOT INCLUDE MOLD FLASH.
 2. DIMENSION **3" DOES NOT INCLUDE TRIM OFFSET.
 3. PIN 1 VISUAL INDEX FEATURE MAY VARY, BUT MUST BE LOCATED WITHIN THE HATCHED AREA.
 4. CHAMFERS AT CORNERS ARE OPTIONAL, SIZE MAY VARY.



Reference Symbol	Dimensions in millimeters		
	Min	Nom	Max
D	13.9	14.0	14.1
E	13.9	14.0	14.1
A ₂	—	1.4	—
H _D	15.8	16.0	16.2
H _E	15.8	16.0	16.2
A	—	—	1.7
A ₁	0.05	—	0.15
b _p	0.15	0.20	0.27
c	0.09	—	0.20
θ	0°	3.5°	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
L _p	0.45	0.6	0.75
L ₁	—	1.0	—

© 2015 Renesas Electronics Corporation. All rights reserved.

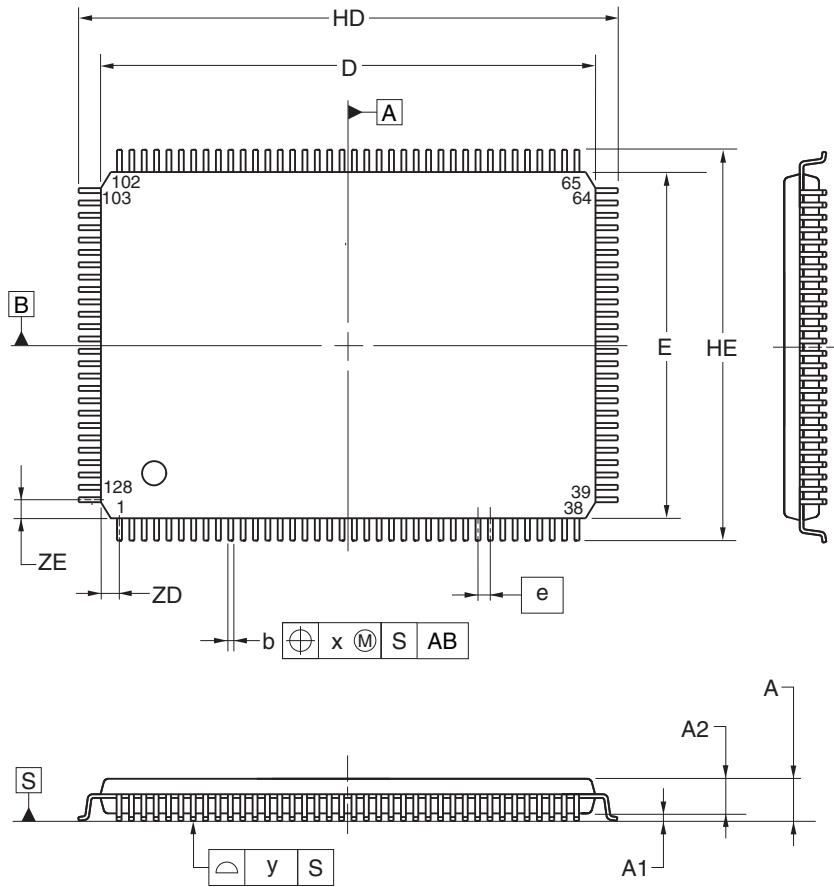
JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LQFP100-14x20-0.65	PLQP0100JC-A	P100GF-65-GBN-1	0.92



©2012 Renesas Electronics Corporation. All rights reserved.

3.11 128-pin Products

JEITA Package Code	RENESAS Code	Previous Code	MASS (TYP.) [g]
P-LFQFP128-14x20-0.50	PLQP0128KD-A	P128GF-50-GBP-1	0.92



detail of lead end

(UNIT:mm)

ITEM	DIMENSIONS
D	20.00±0.20
E	14.00±0.20
HD	22.00±0.20
HE	16.00±0.20
A	1.60 MAX.
A1	0.10±0.05
A2	1.40±0.05
A3	0.25
b	0.22±0.05
c	0.145 ^{+0.055} _{-0.045}
L	0.50
Lp	0.60±0.15
L1	1.00±0.20
θ	3° ^{+5°} _{-3°}
e	0.50
x	0.08
y	0.08
ZD	0.75
ZE	0.75

©2012 Renesas Electronics Corporation. All rights reserved.

REVISION HISTORY

RL78/G23 Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Apr 13, 2021	—	First edition issued
1.10	Nov 18, 2021	All	The module name for 3-wire SPI was changed to simplified SPI.
		All	The module name for SPI was changed to simplified SPI.
		p.1	The operating current in the title was modified.
		p.1	1.1 Features: The descriptions of Middle-speed on-chip oscillator were modified.
		p.2	1.1 Features: The descriptions of Timers were modified.
		p.4	Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23 was modified.
		p.11	1.3.4 40-pin products: Figure was modified.
		p.12	1.3.5 44-pin products: Figure was modified.
		p.13	1.3.6 48-pin products: Note 2 was modified.
		p.13	1.3.6 48-pin products: Remark 3 was added.
		p.23	1.5 Block Diagram was modified.
		p.24 to p.26	1.6 Outline of Functions [30-, 32-, 36-, 40-, 44-, and 48-pin products]: The descriptions were modified.
		p.27 to p.29	1.6 Outline of Functions [52-, 64-, 80-, 100-, and 128-pin products]: The descriptions were modified.
		p.31	2.1 Absolute Maximum Ratings: Note was modified.
		p.32	2.2.1 Characteristics of the X1 and XT1 oscillators: Condition was modified.
		p.35	2.3.1 Pin characteristics: Notes 4 to 6 were modified.
		p.36, p.37	2.3.1 Pin characteristics: Notes 3, 5, and 6 were modified.
		p.43 to p.49	2.3.2 Supply current characteristics, (1) 30- to 64-pin package products with 96- to 128-Kbyte flash ROM: The descriptions in the tables were modified.
		p.50 to p.56	2.3.2 Supply current characteristics, (2) 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM was added.
		p.57 to p.63	2.3.2 Supply current characteristics, (3) 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products was added.
		p.64 to p.66	2.3.2 Supply current characteristics, (4) Peripheral Functions (Common to all products): The descriptions in the tables were added. Notes 13, 14, and 16 were modified. Note 19 was modified.
		p.102	2.5.2 Serial interface UARTA: The table was modified.
		p.106	2.6.1 A/D converter characteristics, (1) Normal modes 1 and 2: The descriptions in the table were modified.
		p.108	2.6.1 A/D converter characteristics, (2) Low-voltage modes 1 and 2: The descriptions in the table were modified.
		P.110	2.6.1 A/D converter characteristics, (3) When the internal reference voltage is selected as reference voltage (+): The descriptions in the table were modified.
		p.111	2.6.4 Comparator characteristics: The descriptions in the table were modified.
p.114	2.6.6 LVD circuit characteristics, (2) LVD1 Detection Voltage of Reset Mode and Interrupt Mode: The table was modified.		
p.117	2.8 Flash Memory Programming Characteristics, (2) Data flash memory: The descriptions in the table were modified.		
p.123	3.4 40-Pin Products: The figure was added.		
p.126	3.6 48-Pin Products: The figure was added.		

Rev.	Date	Description	
		Page	Summary
1.20	Oct 12, 2022	p.5, p.6	Table 1 - 1 List of Ordering Part Numbers was modified.
		p.9, p.10	Table 1 - 2 Multiplexed Pin Functions of the 30-pin Products was added.
		p.12, p.13	Table 1 - 3 Multiplexed Pin Functions of the 32-pin Products was added.
		p.15, p.16	Table 1 - 4 Multiplexed Pin Functions of the 36-pin Products was added.
		p.18, p.19	Table 1 - 5 Multiplexed Pin Functions of the 40-pin Products was added.
		p.21, p.22	Table 1 - 6 Multiplexed Pin Functions of the 44-pin Products was added.
		p.24, p.25	Table 1 - 7 Multiplexed Pin Functions of the 48-pin Products was added.
		p.27, p.28	Table 1 - 8 Multiplexed Pin Functions of the 52-pin Products was added.
		p.30 to p.32	Table 1 - 9 Multiplexed Pin Functions of the 64-pin Products was added.
		p.35 to p.37	Table 1 - 10 Multiplexed Pin Functions 2 of the 64-pin Products was added.
		p.39 to p.41	Table 1 - 11 Multiplexed Pin Functions of the 80-pin Products was added.
		p.43 to p.46	Table 1 - 12 Multiplexed Pin Functions of the 100-pin Products was added.
		p.48 to p.51	Table 1 - 13 Multiplexed Pin Functions 2 of the 100-pin Products was added.
		p.53 to p.57	Table 1 - 14 Multiplexed Pin Functions of the 128-pin Products was added.
		P.62	1.6 Outline of Functions [30-, 32-, 36-, 40-, 44-, and 48-pin products] was modified.
		P.65	1.6 Outline of Functions [52-, 64-, 80-, 100-, and 128-pin products] was modified.
		P.66	2 The section title was modified, and the description and Cautions 1 to 4 were added to the beginning of the section.
		p.67, p.68	2.1 Absolute Maximum Ratings was modified.
		p.69	2.2.1 Characteristics of the X1 oscillator was modified.
		p.69	2.2.2 Characteristics of the XT1 oscillator was added.
		p.72, p.75 to p.77, p.79	2.3.1 Pin characteristics, Note, and Cautions were modified.
		p.85	2.3.2 Supply current characteristics: 1. Notes 3 to 5 were modified.
		p.91	2.3.2 Supply current characteristics: 2. Notes 3 to 5 were modified.
p.97	2.3.2 Supply current characteristics: 3. Notes 3 to 5 were modified.		
p.98 to p.100	2.3.2 Supply current characteristics: 4. Peripheral Functions (Common to all products) was modified, and Note 20 was added.		
p.101	2.4 AC Characteristics was modified.		
p.142, p.143	2.6.1 A/D converter characteristics: 2. Low-voltage modes 1 and 2 was modified, and Note 7 was added.		
p.156	3.3 36-pin Products was modified.		
p.164	3.8 64-pin Products was modified.		
1.21	Nov 15, 2022	p.5	Table 1 - 1 List of Ordering Part Numbers was modified.
1.30	Jan 31, 2024	p.4	Figure 1 - 1 Part Number, Memory Size, and Package of RL78/G23 was modified.
		p.5 to p.7	Table 1 - 1 List of Ordering Part Numbers was modified.
		p.80	2.3.2 Supply current characteristics, 1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM (1/4): Note 1 was modified.
		p.82	2.3.2 Supply current characteristics, 1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM (2/4): Notes 1 to 3 were modified.
		p.83	2.3.2 Supply current characteristics, 1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM (3/4): Note 1 was modified.
p.86	2.3.2 Supply current characteristics, 1. 30- to 64-pin package products with 96- to 128-Kbyte flash ROM (4/4): Notes 1 and 3 to 8 were modified.		

Rev.	Date	Description	
		Page	Summary
1.30	Jan 31, 2024	p.87	2.3.2 Supply current characteristics, 2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM (1/4): Note 1 was modified.
		p.89	2.3.2 Supply current characteristics, 2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM (2/4): Notes 1 to 3 were modified.
		p.90	2.3.2 Supply current characteristics, 2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM (3/4): Note 1 was modified.
		p.93	2.3.2 Supply current characteristics, 2. 30- to 64-pin package products with 192- to 256-Kbyte flash ROM and 80-pin package product with 128- to 256-Kbyte flash ROM (4/4): Notes 1 and 3 to 8 were modified.
		p.94	2.3.2 Supply current characteristics, 3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products (1/4) and Note 1 was modified.
		p.96	2.3.2 Supply current characteristics, 3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products (2/4) and Notes 1 to 3 were modified.
		p.97	2.3.2 Supply current characteristics, 3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products (3/4) and Note 1 was modified.
		p.99, p.100	2.3.2 Supply current characteristics, 3. 44- to 80-pin package products with 384- to 768-Kbyte flash ROM and 100- to 128-pin package products (4/4), Notes 1, and 3 to 8 were modified.
		p.104	2.4 AC Characteristics was modified.
		p.148	2.6.4 Comparator characteristics: Note was added.
		p.159	3.2 32-pin Products: The figure was added.
		p.163	3.5 44-pin Products: The figure was added.
		p.165	3.6 48-pin Products: The figure was added.
p.170	3.8 64-pin Products: The figure was added.		

SuperFlash is a registered trademark of Silicon Storage Technology, Inc. in several countries including the United States and Japan.

Caution: This product uses SuperFlash® technology licensed from Silicon Storage Technology, Inc.

All trademarks and registered trademarks are the property of their respective owners.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.

2. Processing at power-on

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.

3. Input of signal during power-off state

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.

4. Handling of unused pins

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.

5. Clock signals

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.

6. Voltage application waveform at input pin

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).

7. Prohibition of access to reserved addresses

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.

8. Differences between products

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall be responsible for determining what licenses are required from any third parties, and obtaining such licenses for the lawful import, export, manufacture, sales, utilization, distribution or other disposal of any products incorporating Renesas Electronics products, if required.
5. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
6. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.

"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.

Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.

7. No semiconductor product is absolutely secure. Notwithstanding any security measures or features that may be implemented in Renesas Electronics hardware or software products, Renesas Electronics shall have absolutely no liability arising out of any vulnerability or security breach, including but not limited to any unauthorized access to or use of a Renesas Electronics product or a system that uses a Renesas Electronics product. RENESAS ELECTRONICS DOES NOT WARRANT OR GUARANTEE THAT RENESAS ELECTRONICS PRODUCTS, OR ANY SYSTEMS CREATED USING RENESAS ELECTRONICS PRODUCTS WILL BE INVULNERABLE OR FREE FROM CORRUPTION, ATTACK, VIRUSES, INTERFERENCE, HACKING, DATA LOSS OR THEFT, OR OTHER SECURITY INTRUSION ("Vulnerability Issues"). RENESAS ELECTRONICS DISCLAIMS ANY AND ALL RESPONSIBILITY OR LIABILITY ARISING FROM OR RELATED TO ANY VULNERABILITY ISSUES. FURTHERMORE, TO THE EXTENT PERMITTED BY APPLICABLE LAW, RENESAS ELECTRONICS DISCLAIMS ANY AND ALL WARRANTIES, EXPRESS OR IMPLIED, WITH RESPECT TO THIS DOCUMENT AND ANY RELATED OR ACCOMPANYING SOFTWARE OR HARDWARE, INCLUDING BUT NOT LIMITED TO THE IMPLIED WARRANTIES OF MERCHANTABILITY, OR FITNESS FOR A PARTICULAR PURPOSE.
8. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
9. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
10. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
11. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
12. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
13. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
14. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.

(Note2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.5.0-1 October 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/