RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group

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Features

This LSI has following features.

■ CPU (Arm® Cortex®-A9)

- Operating frequency: 400 MHz
- Single-precision/double-precision FPU
- Arm® NEON™

■ On-chip memory

- 3 MB (RZ/A1LU, RZ/A1L)
- 2 MB (RZ/A1LC)

■ Main graphics and camera input functions

- LCD controller (VDC5): 1 channel
  - LCD output: Max. WXGA
  - Screen superimposition: 3 layers
  - Video input: Max. XGA
- CMOS camera input (CEU): 1 channel
- JPEG coding engine: 1 channel (RZ/A1LU only)

■ Main memory interface functions

- NOR flash, SDRAM
- QSPI serial flash: 1 channel (ability to run stored programs directly)
- SD host interface: 2 channels
- MMC host interface: 1 channel

■ Main communication functions

- USB 2.0 High Speed: 2 channels (Host/Function switchable)
- 10M/100M EtherMAC: 1channel
- SCIF: 5 channels
- I2C: 4 channels
- SSI: 4 channels
- RSPI: 3 channels
- CAN: 2 channels
- Ethernet AVB: 1 channel (RZ/A1LU only)

1. Overview

1.1 Outline of Specification

Table 1.1 Features of RZ/A1L, RZ/A1LU, and RZ/A1LC

Items	Specification
CPU	• Arm Cortex-A9 processor • Maximum operating frequency: 400 MHz • Instruction cache size: 32 Kbytes • Data cache size: 32 Kbytes (write-back algorithm) • TLB entries: 128 entries • Jazelle® architecture extension: Full implementation • Media processing engine with NEON™ technology
L2 cache memory	• Arm CoreLink™ Level 2 Cache Controller L2C-310 • Operating frequency: 133 MHz • Cache size: 128 Kbytes
Interrupt controller	• Arm PrimeCell® Generic Interrupt Controller (PL390) • External interrupt pins (NMI, IRQ7 to IRQ0, and TINT121 to TINT0) • On-chip peripheral interrupts: Priority level set for each module • 32 priority levels available
Bus state controller	• Address space divided into six areas (0 to 5), each a maximum of 64 Mbytes • The following features settable for each area independently —Bus size (8, 16, or 32 bits): Available sizes depend on the area. —Number of access wait cycles (different wait cycles can be specified for read and write access cycles in some areas) —Idle wait cycle insertion (between the same area access cycles or different area access cycles) —Specifying the memory to be connected to each area enables direct connection to SRAM, SRAM with byte selection, SDRAM, and burst ROM (clocked synchronous or asynchronous). The address/data multiplexed I/O (MPX) interface is also available. • Outputs a chip select signal ($\overline{CS0}$ to $\overline{CS5}$) according to the target area ($\overline{CS}$ assert or negate timing can be selected by software) • SDRAM refresh Auto refresh or self refresh mode selectable • SDRAM burst access
Direct memory access controller	• Sixteen channels; external requests are available for one of them. • Can be activated by on-chip peripheral modules. • A specific DMA transfer interval can be specified to adjust the bus occupancy. • Link mode (DMA transfer under descriptor control) supported • Transfer information can be automatically reloaded.
Clock pulse generator	• Clock mode: Input clock can be selected from external input (EXTAL or USB_X1) or crystal resonator. • Input clock can be multiplied by 32 (max.) by the internal PLL circuit. • Peak values of EMI noise can be reduced by the on-chip SSCG circuit. • Five types of clocks generated: —CPU clock (Iφ): Maximum 400.00 MHz —Internal bus clock (Bφ): Maximum 133.33 MHz —Peripheral clock 1 (P1φ): Maximum 66.67 MHz —Peripheral clock 0 (P0φ): Maximum 33.33 MHz
Watchdog timer	• On-chip one-channel watchdog timer • A counter overflow can reset the LSI.
Power-down modes	• Four power-down modes provided to reduce the power consumption in this LSI —Sleep mode —Software standby mode —Deep standby mode —Module standby mode

Items	Specification
Multi-function timer pulse unit 2	• Maximum 16 lines of pulse inputs/outputs based on five channels of 16-bit timers • 18 output compare and input capture registers • Input capture function • Pulse output modes Toggle, PWM, complementary PWM, and reset-synchronized PWM modes • Synchronization of multiple counters • Complementary PWM output mode —Non-overlapping waveforms output for 3-phase inverter control —Automatic dead time setting —0% to 100% PWM duty value specifiable —A/D converter start request delaying function —Interrupt skipping at crest or trough • Reset-synchronized PWM mode Three-phase PWM waveforms in positive and negative phases can be output with a required duty value. • Phase counting mode Two-phase encoder pulse counting available
OS timer	• Two-channel 32-bit counters • Two operating modes: —Interval timer mode —Free-running comparison mode • DMA transfer request or interrupt request can be issued when a compare match occurs.
Realtime clock	• Internal clock, calendar function, alarm function • Interrupts can be generated at intervals of 1/64 s by the 32.768-kHz on-chip crystal oscillator.
Serial communication interface with FIFO	• Five channels • Clock synchronous mode or asynchronous mode selectable • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • Separate 16-byte FIFO registers for transmission and reception • Modem control function (channels 0 to 2 in asynchronous mode)
Serial communication interface	• Two channels • Clock synchronous mode, asynchronous mode, or smart card interface mode is selectable. • Simultaneous transmission and reception (full-duplex communication) supported • Dedicated baud rate generator • LSB first/MSB first selectable • Modem control function • Encoding and decoding of IrDA communications waveforms in accord with version 1.0 of the IrDA standard (on channel 0)
Renesas serial peripheral interface	• Three channels • SPI operation • Master mode and slave mode selectable • Programmable bit length, clock polarity, and clock phase can be selected. • Consecutive transfers • MSB first/LSB first selectable • Maximum transfer rate: 33.33 Mbps
SPI multi I/O bus controller	• One channel • Up to two serial flash memories with multiple I/O bus sizes (single/dual/quad) can be connected. • External address space read mode (built-in read cache) • SPI operating mode • Clock polarity and clock phase can be selected. • MSB first/LSB first selectable • Maximum transfer rate: 533.33Mbps (SDR transfer, with two serial flash memories connected) 1066.66Mbps (DDR transfer, with two serial flash memories connected) (RZ/A1LU only)
I^2C bus interface	• Four channels • Master mode and slave mode supported • Support for 7-bit and 10-bit slave address formats • Support for multi-master operation • Timeout detection

Items	Specification
Serial sound interface	• Four-channel bidirectional serial transfer • Duplex communication (channels 0, 1, and 3) • Support of various serial audio formats • Support of master and slave functions • Generation of programmable word clock and bit clock • Multi-channel formats • Support of 8, 16, 18, 20, 22, 24, and 32-bit data formats • Support of eight-stage FIFO for transmission and reception • Support of TDM mode • Support of WS continue mode in which the SSIWS signal is not stopped. • Support of direct transfer to the SCUX module • A change of the sampling frequency can be detected.
Media local bus (RZ/A1L only)	• Conforms with version 2.0 of the MediaLB standard. Data transfer at up to 50 Mbps is possible.
SCUX	• Sampling rate conversion —Asynchronous or synchronous sampling rate conversion is possible. —Sampling rate (synchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input [kHz]: 8, 11.025, 12, 16, 22.05, 24, 32, 44.1, 48, 64, 88.2, or 96 is selectable. Output [kHz]: 8, 16, 24, 44.1, 48, or 96 is selectable. —Sampling rate (asynchronous mode) Note: The selectable sampling rates depend on the number of used channels and rate ratio. Input/output [kHz]: 1 to 96 —Data format: 16 or 24 bits • Digital volume and mute functions —The digital volume can be set within the range from a multiple of 0 to 8 (−120 to 18 dB) —Volume ramping supports soft mute, fade-in, and fade-out. —The zero crossing mute function can apply muting at zero-crossing points. • Mixer —Data of two to four source systems can be mixed (added together) into one system. —The ratio to add the sources can be set. • Direct transfer to the serial sound interface module is supported.
CAN interface	• Two channels • ISO11898-1 compliant • Message buffer: —Up to 64 2-channel receive message buffers: shared among all channels. —16 transmit message buffers per channel
IEBus™ controller (RZ/A1L only)	• Conforms with the IEBus protocol (communication modes 1 and 2). • Transfer rates: approximately 18 kbps (in communication mode 1), approximately 27 kbps (in communication mode 2) • Maximum numbers of bytes for transfer: 32 bytes/frame (in communication mode 1), 128 bytes/frame (in communication mode 2) • Operating clock: 8 MHz Note: Input of peripheral clock 0 (P0φ) running at 32 MHz is required.
Renesas SPDIF interface	• Support of IEC60958 standard (stereo and consumer use modes only) • Sampling frequencies of 32 kHz, 44.1 kHz, and 48 kHz • Audio word sizes of 16 to 24 bits per sample • Biphase mark encoding • Double buffered data • Parity encoded serial data • Simultaneous transmit and receive • Receiver autodetects IEC 61937 compressed mode data.

Items	Specification
CD-ROM decoder (RZ/A1L only)	• Support of five formats: Mode 0, mode 1, mode 2, mode 2 form 1, and mode 2 form 2 • Sync codes detection and protection (Protection: When a sync code is not detected, it is automatically inserted.) • Descrambling • ECC correction —P, Q, PQ, and QP correction —PQ or QP correction can be repeated up to three times. • EDC check Performed before and after ECC • Mode and form are automatically detected. • Link sectors are automatically detected. • Buffering data control Buffering CD-ROM data including Sync code is transferred in specified format, after the data is descrambled, corrected by ECC, and checked by EDC.
LIN interface (RZ/A1L only)	• Conforms with revisions 1.3, 2.0, 2.1, and 2.2 of the LIN protocol and SAEJ 2062. • Master mode selectable
Ethernet controller	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 10 and 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • E-DMAC (Direct Memory Access Controller for Ethernet controller) function
EthernetAVB (RZ/A1LU only)	• Conforms with the Ethernet or the IEEE802.3 MAC (Media Access Control) layer standard • MAC function Constructs/deconstructs data frames (frame format conforming to IEEE802.3, 2000 Edition) Supports transfer at 100 Mbps Supports full-duplex mode Flow control conforming to IEEE802.3x Supports an MII (Media Independent Interface) for connection to a PHY interface in conformance with IEEE 802.3 Upward protocol support (checksum) function • AVB-DMAC (DMAC dedicated to EthernetAVB) function AVB-DMAC conforms with the following 3 standards; IEEE802.1AS (Clock Synchronization Protocol), IEEE802.1Qav (Realtime Transfer Protocol) and IEEE802.1Qat (Bandwidth Reservation Protocol)
USB 2.0 host/function module	• Two channels • Conforms to the Universal Serial Bus Specification Revision 2.0 • 480-Mbps, 12-Mbps, and 1.5-Mbps transfer rates provided (host mode) • 480-Mbps and 12-Mbps transfer rates provided (function mode) • On-chip 8-Kbyte RAM as communication buffers
Video display controller 5	• Video input interface BT601, BT656 format (NTSC/PAL) input: Input clock: 27 MHz/54 MHz Digital pin input (channel 0): YCbCr422, YCbCr444, RGB888, RGB666, RGB565 Digital pin input size: Maximum input video image size to be set*: 1440 pixels × 1024 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the connected device. Examples of input video image size : XGA (1024 × 768), SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320) • Input video control Horizontal noise reduction (NR) and brightness and gain adjustment using matrix operation

Items	Specification
Video display controller 5	• Scaling control Vertical and horizontal scaling up or down of input video possible at a desired ratio (scaling up of graphics also possible) Scaling up ratio: 1 to 8; scaling down ratio: 1/8 to 1 Interpolation: Hold or linear selectable 2D IP conversion: 2D IP conversion through separately setting the initial phases for the top and bottom fields • Video recording Output pixel format: YCbCr444, YCbCr422, RGB888, RGB565 Output field rate: 1/1, 1/2, 1/4, 1/8 Rotation: Horizontal mirroring and 90/180/270 degree rotation for YCbCr422 and RGB565 Maximum video image size to be stored: ×1 size of input video image • Output video control Black stretch: Black area stretched according to Y signal state Enhancer capability: LTI (transient improvement) and sharpness (contour emphasis) for Y signal • Three graphics layers (one of them also for input video) Available input pixel formats 1 bit/pixel: CLUT1 4 bits/pixel: CLUT4 8 bits/pixel: CLUT8 16 bits/pixel: YCbCr422 (graphics layers 0 and 1), RGB565, ARGB1555, RGBA5551, ARGB4444 32 bits/pixel: ARGB8888, RGBA8888, RGB888, YCbCr444 (graphics layer 0) • Superimposition Alpha blending in a rectangular area: Input video, layer 1, and layer 2 blended according to the transparency percentage α (fade-in and fade-out function available) Chroma key function: Mixing based on transparency percentage α using the specified RGB and CLUT value Pixel-base alpha blending: Alpha blending for each pixel based on transparency percentage α • Panel output control Panel output correction: Brightness adjustment and contrast adjustment, gamma correction, panel dithering TCON: Various timing output for LCD panel driving provided by a total of seven vertical and horizontal panel driver signals Panel output pixel format: RGB888, RGB666, RGB565, serial RGB Output video image size: Maximum output video image size to be set*: 1999 pixels × 2035 lines (horizontal × vertical) Note:*Depends on the AC characteristics of the display panel. Examples of output video image size: XGA (1024 × 768), SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320)
JPEG codec unit (RZ/A1LU only)	• Compression and decompression method conforming to the JPEG baseline standard within the range described in this document. • Operational precision: Conforming to JPEG Part 2, ISO-IEC10918-2 • Pixel format: Compression: YCbCr422 Decompression: YCbCr444, YCbCr422, YCbCr411, YCbCr420 Output pixel format to the buffer: YCbCr422, ARGB8888, RGB565 • Four quantization tables provided • Four Huffman tables provided (two tables for AC coefficients and two tables for DC coefficients) • Markers supported: SOI, SOF0, SOS, DQT, DHT, DRI, RSTm, and EOI • Image data rate: Max. 133.33 Mbytes/s (at 66.67-MHz operation)

Items	Specification
Capture engine unit	• Examples of input video image size : 5 megapixels (2,560 × 1,920), 3 megapixels (2,048 × 1,536), 2 megapixels (1,632 × 1,224), UXGA (1,600 × 1,200), SXGA (1) (1,280 × 1,024), SXGA (2) (1,280 × 960), WXGA (1,280 × 768), XGA (1,024 × 768), SVGA (800 × 600), WVGA (800 × 480), VGA (640 × 480), WQVGA (480 × 240), QVGA (320 × 240, 240 × 320) Note: Depends on the AC characteristics of the connected device, frame rate of the connected device, and transfer speed to the destination RAM. • Input format: 8-bit YCbCr422 binary data • Memory output format: YCbCr422, YCbCr420 Note: The captured data cannot be displayed via the video display controller 5 because the Y data and CbCr data are split when written to memory.
SD host interface	• Two channels • SD memory I/O card interface (1-/4-bit SD bus) • Error check function: CRC7 (command), CRC16 (data) • Interrupt requests —Card access interrupt —SDIO access interrupt —Card detect interrupt • DMA transfer requests —SD_BUF write —SD_BUF read • Card detection function, write protect supported
MMC host interface	• Interface to multi-media card (MMC) • Data bus: 1-/4-/8-bit MMC mode • Interrupt requests: card detection, error/time-out, and normal operation • DMA transfer requests: CE_DATA write and CE_DATA read • Card detection function
General I/O ports	• 176-pin QFP or BGA: 78 I/Os, 8 inputs with open-drain outputs, and 14 inputs (input only) • 208-pin, 233-pin: 100 I/O pins, 8 input pins with open-drain outputs, and 14 inputs (input only) • Input or output can be selected for each bit.
A/D converter	• 12-bit resolution • Eight input channels • Minimum conversion time: 5.0 µs • A/D conversion request by the external trigger or timer trigger
Debugging interface	• Arm CoreSight™ architecture • JTAG-standard pin assignment
On-chip RAM	• 3-Mbyte (RZ/A1L and RZ/A1LU) or 2-Mbyte (RZ/A1LC) large capacity memory for video display/ recording and work (128 Kbytes are used for data retention) • 128-Kbyte memory for data retention (16 Kbytes × 2, 32 Kbytes × 1, 64 Kbytes × 1)
Boot modes	• Four boot modes Boot mode 0: Booting from memory (bus width: 16 bits) connected to CS0 area Boot mode 1: Booting from a serial flash memory Boot mode 2: Booting from a NAND flash memory with SD controller Boot mode 3: Booting from a NAND flash memory with MMC controller
Power supply voltage	• Vcc: 1.10 to 1.26 V • PVcc: 3.0 to 3.6 V

Items	Specification
Package	• PLBG0176KA-A 176-pin BGA, 8-mm square, 0.5-mm pitch JEITA package code: P-LFBGA176-8×8-0.50 RENESAS code: PLBG0176KA-A • PLQP0176KB-A 176-pin QFP, 24-mm square, 0.5-mm pitch JEITA package code: P-LFQFP176-24×24-0.50 RENESAS code: PLQP0176KB-A • PLQP0208KB-A 208-pin QFP, 28-mm square, 0.5-mm pitch JEITA package code: P-LFQFP208-28×28-0.50 RENESAS Code : PLQP0208KB-A • PRBG0233GA-A 233-pin BGA, 15-mm square, 0.8-mm pitch JEITA package code: P-FBGA233-15x15-0.80 RENESAS Code : PRBG0233GA-A

1.2 Block Diagram

This LSI has two main buses: the north main bus where peripheral modules are connected and the south main bus where on-chip RAM and external ROM and RAM are connected. Figure 1.1 is a schematic diagram of the internal buses.

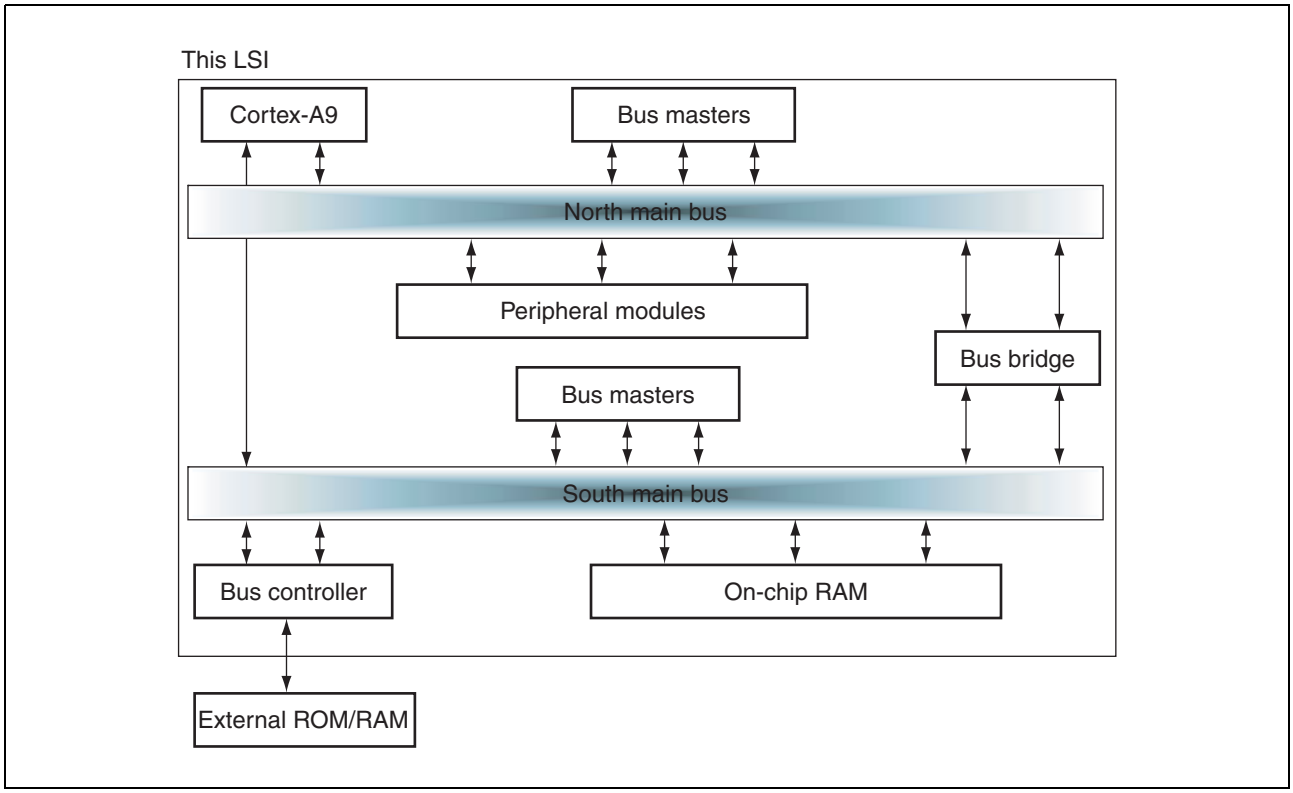


Figure 1.1 Schematic Diagram of LSI Internal Bus

Figure 1.2 shows the schematic diagram of North Main Bus, Figure 1.3 shows the schematic diagram of South Main Bus.

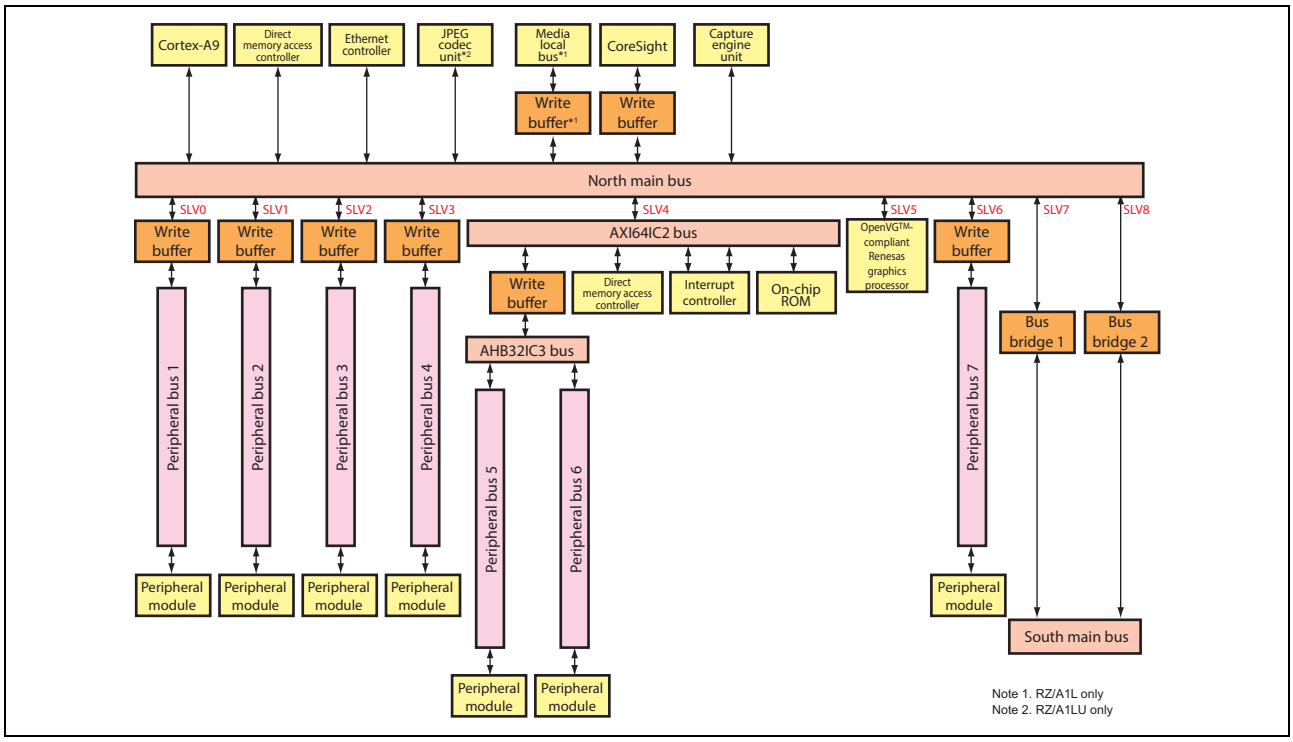


Figure 1.2 North Main Bus Configuration

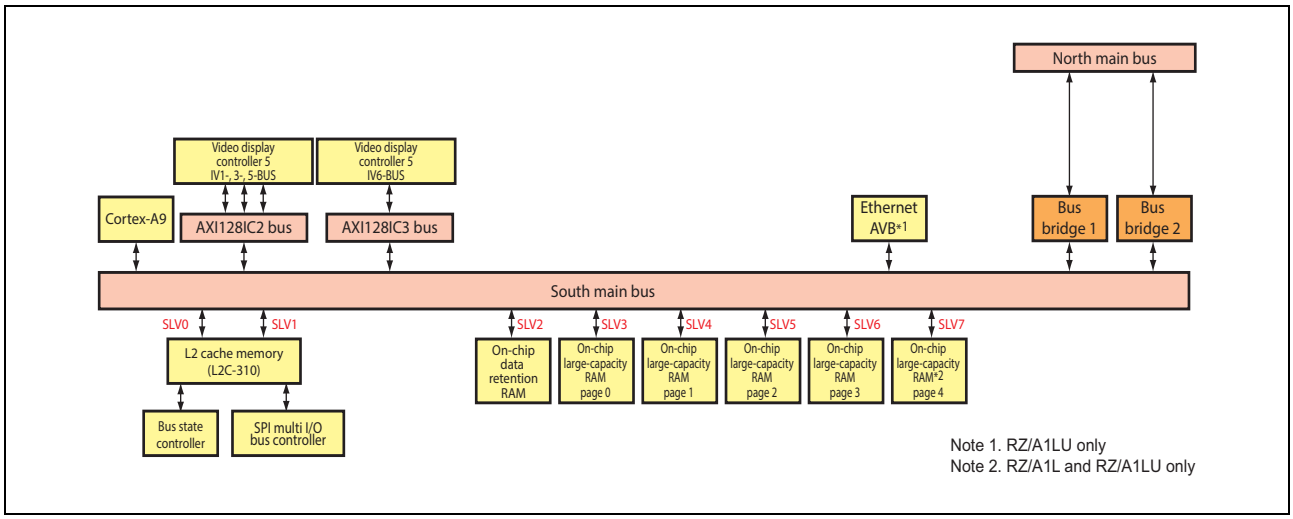


Figure 1.3 South Main Bus Configuration

1.3 Product Lineup

Table 1.2 Product Lineup

Group	Part Number	Temperature Range	Quality Level	Package
RZ/A1L	R7S721020VCBG	-40 to +85°C	Industry usage etc.	PLBG0176KA-A
	R7S721020VCFP		Industry usage etc.	PLQP0176KB-A
	R7S721020VLFP		Car Accessories	
	R7S721021VCFP		Industry usage etc.	PLQP0208KB-A
	R7S721021VLFP		Car Accessories	PLQP0208KB-A
RZ/A1LU	R7S721030VCBG	-40 to +85°C	Industry usage etc.	PLBG0176KA-A
	R7S721030VCFP		Industry usage etc.	PLQP0176KB-A
	R7S721030VLFP		Car Accessories	
	R7S721031VCFP		Industry usage etc.	PLQP0208KB-A
	R7S721031VLFP		Car Accessories	
	R7S721031VCBG		Industry usage etc.	PRBG0233GA-A
	R7S721031VLBG		Car Accessories	
RZ/A1LC	R7S721034VCBG	-40 to +85°C	Industry usage etc.	PLBG0176KA-A

2. Pin

2.1 Pin Functions

2.1.1 Pin Function of Functional Blocks

Table 2.1 List of Pin Functions

Classification	Symbol	I/O	Name	Function
Power supply	Vcc	I	Power supply	Power supply pins. All the Vcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	Vss	I	Ground	Ground pins. All the Vss pins must be connected to the system power supply (0 V). This LSI does not operate correctly if there is a pin left open.
	PVcc	I	Power supply for I/O circuits	Power supply for I/O pins. All the PVcc pins must be connected to the system power supply. This LSI does not operate correctly if there is a pin left open.
	PLLVcc	I	Power supply for PLL	Power supply for the on-chip PLL oscillator.
Clock	EXTAL	I	External clock	Connected to a crystal resonator. An external clock signal may also be input to the EXTAL pin.
	XTAL	O	Crystal	Connected to a crystal resonator.
	CKIO	O	System clock output	Supplies the system clock to external devices.
	AUDIO_CLK	I	External clock for audio	Input pin of external clock for audio. A clock input to the divider is selected from an oscillation clock input on this pin or pins AUDIO_X1 and AUDIO_X2.
	AUDIO_X1	I	Crystal resonator/ external clock for audio	Pins connected to a crystal resonator for audio. An external clock can be input on pin AUDIO_X1. A clock input to the divider is selected from an oscillation clock input on these pins or the AUDIO_CLK pin.
	AUDIO_X2	O		
	AUDIO_XOUT	O	AUDIO_X1 clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal.
	AUDIO_XOUT2	O	AUDIO_X1 divided-by-two clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by two.
	AUDIO_XOUT3	O	AUDIO_X1 divided-by-three clock output	Output for the on-chip crystal oscillator on AUDIO_X1 or the external clock signal after frequency division of the selected signal by three.

Classification	Symbol	I/O	Name	Function
Operating mode control	MD_BOOT1, MD_BOOT0	I	Mode set	Sets the operating mode. Do not change the signal levels on these pins while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLK	I	Clock mode set	Sets the clock operating mode. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	MD_CLKS	I	SSCG clock mode set	Switches the SSCG circuit on or off. Do not change the signal levels on this pin while the $\overline{\text{RES}}$ pin is asserted or until the mode is fixed, after the negation.
	BSCANP	I	Boundary scan set	Boundary scan setting pin. This pin is set to the high level for a boundary scan and to the low level for normal operation.
System control	$\overline{\text{RES}}$	I	Power-on reset	This LSI enters the power-on reset state when this signal goes low.
	$\overline{\text{WDTOVF}}$	O	Watchdog timer overflow	Outputs an overflow signal from the watchdog timer.
Interrupts	NMI	I	Non-maskable interrupt	Non-maskable interrupt request pin. It is handled as an FIQ exception. Fix it high when not in use.
	IRQ7 to IRQ0	I	Interrupt requests 7 to 0	Maskable interrupt request pins. Level-input or edge-input detection can be selected. When the edge-input detection is selected, the rising edge, falling edge, or both edges can also be selected.
	TINT121 to TINT0	I	Interrupt requests 121 to 0	Maskable interrupt request pins. High-level-input or rising edge-input detection can be selected.
Address bus	A25 to A0	O	Address bus	Outputs addresses.
Data bus	D31 to D0	I/O	Data bus	Bidirectional data bus.

Classification	Symbol	I/O	Name	Function
Bus control	$\overline{CS5}$ to $\overline{CS0}$	O	Chip select 5 to 0	Chip-select signals for external memory or devices.
	$\overline{RD}$	O	Read	Indicates that data is read from an external device.
	RD/$\overline{WR}$	O	Read/write	Read/write signal.
	$\overline{BS}$	O	Bus start	Bus-cycle start signal.
	$\overline{AH}$	O	Address hold	Address hold timing signal for the device that uses the address/data-multiplexed bus.
	$\overline{WAIT}$	I	Wait	Inserts a wait cycle into the bus cycles during access to the external space.
	$\overline{WE0}$	O	Byte select	Indicates a write access to bits 7 to 0 of data of external memory or device.
	$\overline{WE1}$	O	Byte select	Indicates a write access to bits 15 to 8 of data of external memory or device.
	$\overline{WE2}$	O	Byte select	Indicates a write access to bits 23 to 16 of data of external memory or device.
	$\overline{WE3}$	O	Byte select	Indicates a write access to bits 31 to 24 of data of external memory or device.
	DQMLL	O	Byte select	Selects bits D7 to D0 when SDRAM is connected.
	DQMLU	O	Byte select	Selects bits D15 to D8 when SDRAM is connected.
	DQMUL	O	Byte select	Selects bits D23 to D16 when SDRAM is connected.
	DQMUU	O	Byte select	Selects bits D31 to D24 when SDRAM is connected.
	$\overline{RAS}$	O	RAS	Connected to the $\overline{RAS}$ pin when SDRAM is connected.
	$\overline{CAS}$	O	CAS	Connected to the $\overline{CAS}$ pin when SDRAM is connected.
	CKE	O	CK enable	Connected to the CKE pin when SDRAM is connected.
Direct memory access controller	DREQ0	I	DMA-transfer request	Input pin to receive external requests for DMA transfer.
	DACK0	O	DMA-transfer request accept	Output pin for signals indicating acceptance of external requests from external devices.
	TEND0	O	DMA-transfer end output	Output pin for DMA transfer end.

Classification	Symbol	I/O	Name	Function
Multi-function timer pulse unit 2	TCLKA, TCLKB, TCLKC, TCLKD	I	Timer clock input	External clock input pins for the timer.
	TIOC0A, TIOC0B, TIOC0C, TIOC0D Note: TIOC0B pin is not present on products in the 176-pin package.	I/O	Input capture/ output compare (channel 0)	The TGRA_0 to TGRD_0 input capture input/output compare output/PWM output pins.
	TIOC1A, TIOC1B	I/O	Input capture/ output compare (channel 1)	The TGRA_1 and TGRB_1 input capture input/output compare output/PWM output pins.
	TIOC2A, TIOC2B	I/O	Input capture/ output compare (channel 2)	The TGRA_2 and TGRB_2 input capture input/output compare output/PWM output pins.
	TIOC3A, TIOC3B, TIOC3C, TIOC3D	I/O	Input capture/ output compare (channel 3)	The TGRA_3 to TGRD_3 input capture input/output compare output/PWM output pins.
	TIOC4A, TIOC4B, TIOC4C, TIOC4D	I/O	Input capture/ output compare (channel 4)	The TGRA_4 to TGRD_4 input capture input/output compare output/PWM output pins.
Realtime clock	RTC_X1	I	Crystal resonator for realtime clock/ external clock	Connected to 32.768-kHz crystal resonator. The RTC_X1 pin can also be used to input an external clock.
	RTC_X2	O		
Serial communication interface with FIFO	TxD4 to TxD0	O	Transmit data	Data output pins.
	RxD4 to RxD0	I	Receive data	Data input pins.
	SCK4 to SCK0	I/O	Serial clock	Clock input/output pins.
	$\overline{\text{RTS2}}$ to $\overline{\text{RTS0}}$	I/O	Transmit request	Modem control pins.
	$\overline{\text{CTS2}}$ to $\overline{\text{CTS0}}$	I/O	Transmit enable	Modem control pins.
Serial communication interface	SCI_SCK1, SCI_SCK0	I/O	Serial clock	Clock input/output pins.
	SCI_TXD1, SCI_TXD0	O	Transmit data	Data output pins.
	SCI_RXD1, SCI_RXD0	I	Receive data	Data input pins.
	$\overline{\text{SCI\_CTS1}}$/$\overline{\text{RTS1}}$, SCI_CTS0/$\overline{\text{RTS0}}$	I/O	Transmit and receive start control	I/O pins for controlling the start of transmission and reception.
Renesas serial peripheral interface	MOSI2 to MOSI0	I/O	Data	Data I/O pins.
	MISO2 to MISO0	I/O	Data	Data I/O pins.
	RSPCK2 to RSPCK0	I/O	Clock	Clock I/O pins.
	SSL20, SSL10, SSL00	I/O	Slave select	Slave select I/O pins.
SPI multi I/O bus controller	SPBCLK_0	O	Clock	Clock output pins.
	SPBSSL_0	O	Slave select	Slave select output pins.
	SPBMO0_0/SPBIO00_0, SPBMI0_0/SPBIO10_0, SPBIO20_0, SPBIO30_0, SPBMO1_0/SPBIO01_0, SPBMI1_0/SPBIO11_0, SPBIO21_0, SPBIO31_0	I/O	Data	Data I/O pins for channel.

Classification	Symbol	I/O	Name	Function
I²C bus interface	RIIC3SCL to RIIC0SCL	I/O	Serial clock pin	Serial clock I/O pins.
	RIIC3SDA to RIIC0SDA	I/O	Serial data pin	Serial data I/O pins.
Serial sound interface	SSITxD3, SSITxD1, SSITxD0	O	Data output	Serial data output pin.
	SSIRxD3, SSIRxD1, SSIRxD0	I	Data input	Serial data input pin.
	SSIDATA2	I/O	Data I/O	Serial data I/O pins.
	SSISCK3 to SSISCK0	I/O	SSI clock I/O	I/O pins for serial clocks.
	SSIWS3 to SSIWS0	I/O	SSI clock LR I/O	I/O pins for word selection.
Media local bus (RZ/A1L only)	MLB_CLK	I	Clock input	MediaLB clock input pin.
	MLB_SIG	I/O	Signal information I/O	MediaLB signal information I/O pin.
	MLB_DAT	I/O	Data I/O	MediaLB data I/O pin.
CAN interface	CAN_CLK	I	Clock source for CAN communication	Clock source for CAN communication.
	CAN1TX, CAN0TX	O	CAN bus transmit data	Output pins for transmit data on the CAN bus.
	CAN1RX, CAN0RX	I	CAN bus receive data	Input pins for receive data on the CAN bus.
IEBus™ controller (RZ/A1L only)	IETxD	O	IEBus™ controller transmit data	Output pin for transmit data on IEBus™ controller.
	IERxD	I	IEBus™ controller receive data	Input pin for receive data on IEBus™ controller.
Renesas SPDIF interface	SPDIF_OUT	O	Output data	Transmit data output pin.
	SPDIF_IN	I	Input data	Receive data input pin.
LIN interface (RZ/A1L only)	RLIN30TX	O	Output data	Transmit data output pins.
	RLIN30RX	I	Input data	Receive data input pins.
Ethernet controller, EthernetAVB (RZ/A1LU only) Note: Regarding the switching of pin functions between Ethernet controller and EthernetAVB, refer to section 41, Ports, in the RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual.	ET_TXCLK	I	Transmit clock	Clock pin for transmission.
	ET_TXEN	O	Transmit enable	Transmit data enable pin
	ET_TXD3 to ET_TXD0	O	Transmit data	MII transmit data pins.
	ET_COL	I	Collision detection	Collision detection pin.
	ET_TXER	O	Transmit error	Transmit error output pin.
	ET_RXCLK	I	Receive clock	Receive clock pin
	ET_RXDV	I	Receive enable	Receive data enable pin
	ET_RXD3 to ET_RXD0	I	Receive data	MII receive data pins.
	ET_RXER	I	Receive error	Receive error input pin.
	ET_CRS	I	Carrier detection	Carrier detection pin.
	ET_MDC	O	Management data clock	Clock pin for information transfer via MDIO.
	ET_MDIO	I/O	Management data I/O	Bidirectional pin for exchange of management data
EthernetAVB (RZ/A1LU only)	AVB_CAPTURE	I	Timer capture	Capturing input pin for AVTP presentation timer
	AVB_GPTP_EXTERN	I	gPTP timer external clock	External clock pin for gPTP timer

Classification	Symbol	I/O	Name	Function
USB 2.0 host/ function module	DP1, DP0	I/O	USB 2.0 host/function module D+ data	D+ data pins for USB 2.0 host/function module bus.
	DM1, DM0	I/O	USB 2.0 host/function module D– data	D– data pins for USB 2.0 host/function module bus.
	VBUS1, VBUS0	I	VBUS input	Connected to Vbus on USB 2.0 host/ function module bus.
	REFRIN	I	Reference input	Connected to USBAPVss via 5.6-kΩ ± 1% resistance. (QFP package) Connected to Vss via 5.6-kΩ ± 1% resistance. (BGA package)
	USB_X1	I	Crystal resonator/ external clock for USB 2.0 host/function module	Connected to a crystal resonator for USB 2.0 host/function module. An external clock signal may also be input to the USB_X1 pin.
	USB_X2	O		
	USBAPVcc	I	Power supply for transceiver analog pins	Power supply for pins.
	USBAPVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver analog pins	Ground for pins.
	USBDPVcc Note: This pin is not present on products in the BGA package.	I	Power supply for transceiver digital pins	Power supply for pins.
	USBDPVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver digital pins	Ground for pins.
	USBAVcc	I	Power supply for transceiver analog core	Power supply for core.
	USBAVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver analog core	Ground for core.
	USBDVcc Note: This pin is not present on products in the BGA package.	I	Power supply for transceiver digital core	Power supply for core.
	USBDVss Note: This pin is not present on products in the BGA package.	I	Ground for transceiver digital core	Ground for core.
	USBUVcc Note: This pin is not present on products in the BGA package.	I	480-MHz power supply for USB 2.0 host/function module	Power supply for 480-MHz sections
	USBUVss Note: This pin is not present on products in the BGA package.	I	480-MHz ground for USB 2.0 host/function module	Ground for 480-MHz sections
Video display controller 5	LCD0_DATA23 to LCD0_DATA0	O	Output data	Data output pins for panel.
	LCD0_TCON6 to LCD0_TCON0	O	Panel timing adjustment output	Output pins for panel timing adjustment
	LCD0_CLK	O	Panel clock	Panel clock output pins.
	LCD0_EXTCLK	I	Panel clock source	Panel clock source input pins.
	DV0_DATA23 to DV0_DATA0	I	Input data	Data input pins for graphics data.
	DV0_VSYNC	I	VSYNC input	VSYNC input pins.
	DV0_HSYNC	I	HSYNC input	HSYNC input pins.
	DV0_CLK	I	Input clock	Clock input signal pins for graphics data.

Classification	Symbol	I/O	Name	Function
Capture engine unit	VIO_D7 to VIO_D0	I	Input data	Graphics data input pins.
	VIO_CLK	I	Input clock	Graphics data clock input pin.
	VIO_VD	I	VSYNC input	VSYNC input pin.
	VIO_HD	I	HSYNC input	HSYNC input pin.
	VIO_FLD	I	FIELD input	Input pin for field information
SD host interface	SD_CLK_0, SD_CLK_1	O	SD clock	Output pins for SD clock.
	SD_CMD_0, SD_CMD_1	I/O	SD command	SD command output and response input signals.
	SD_D3_0 to SD_D0_0, SD_D3_1 to SD_D0_1	I/O	SD data	SD data bus signals.
	SD_CD_0, SD_CD_1	I	SD card detection	SD card detection.
	SD_WP_0, SD_WP_1	I	SD write protection	SD write protection signals.
MMC host interface	MMC_CLK	O	MMC clock	Output pin for MMC clock.
	MMC_CMD	I/O	MMC command	MMC command output and response input signal.
	MMC_D7 to MMC_D0	I/O	MMC data	MMC data bus signals.
	MMC_CD	I	MMC card detection	MMC card detection.
A/D converter	AN7 to AN0	I	Analog input pins	Analog input pins.
	$\overline{\text{ADTRG}}$	I	A/D conversion trigger input	External trigger input pin for starting A/D conversion.
	AVcc	I	Analog power supply	Power supply pin for A/D converter.
	AVss	I	Analog ground	Ground pin for A/D converter.
	AVref	I	Analog reference voltage	Reference voltage pin for A/D converter.
General I/O ports	P2_0 to P2_9, P3_0 to P3_15, P4_0 to P4_7, P5_0 to P5_15, P6_0 to P6_15, P7_0 to P7_11, P8_0 to P8_15 (208-pin and 233-pin products only), P9_0 to P9_5 (208-pin and 233-pin products only)	I/O	General port	78 general I/O port pins in 176-pin QFP and 176-pin BGA products. 100 general I/O port pins in 208-pin and 233-pin products.
	P1_0 to P1_7	I/O	General port	8 input port pins with open-drain output.
	JP0_0, JP0_1, P0_0 to P0_3, P1_8 to P1_15	I	General port	14 general input port pins.
Debugging interface	TCK/SWDCLK	I	Test clock	Test-clock input pin. Also used as the input clock pin for serial wire debugging
	TMS/SWDIO	I, I/O	Test mode select	Test-mode select signal input pin. Also used as the I/O data pin for serial wire debugging
	TDI	I	Test data input	Serial input pin for instructions and data.
	TDO	O	Test data output	Serial output pin for instructions and data.
	$\overline{\text{TRST}}$	I	Test reset	Initialization-signal input pin. Note: When the chip is in CoreSight debugging mode, do not negate the $\overline{\text{TRST}}$ signal while the $\overline{\text{RES}}$ signal is at the high-level.
	TRACEDATA3 to TRACEDATA0	O	Data output	Trace data output pins.
	TRACECLK	O	Clock output	Trace clock output pin.
	TRACECTL	O	Enable output	Trace enable output pin.

2.1.2 List of Pins

Table 2.2 List of Pins

176 QFP	176 BGA	208 QFP	233 BGA	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram
No.	No.	No.	No.	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Figure 2.1
1	B1	1	B1	P5_3	I(s)/O	—	—	D3	I(s)/O	MMC_D7	I(s)/O	ET_TXD3	O	DV0_DATA19	I(s)	LCD0_TCON3	O	—	—	—	—	—	—	(8)
2	C2	2	C2	P5_4	I(s)/O	—	—	D4	I(s)/O	RSPCK2	I(s)/O	SSISCK1	I(s)/O	DV0_DATA20	I(s)	—	—	—	—	—	—	—	—	(8)
3	D2	3	E4	P5_5	I(s)/O	—	—	D5	I(s)/O	SSL20	I(s)/O	SSIWS1	I(s)/O	DV0_DATA21	I(s)	—	—	—	—	—	—	—	—	(8)
4	C1	4	D3	P5_6	I(s)/O	—	—	D6	I(s)/O	MOSI2	I(s)/O	SSITxD1	O	DV0_DATA22	I(s)	SCK2	I(s)/O	—	—	—	—	—	—	(8)
5	D1	5	C1	P5_7	I(s)/O	—	—	D7	I(s)/O	MISO2	I(s)/O	SSIRxD1	I(s)	DV0_DATA23	I(s)	TxD2	O	—	—	—	—	—	—	(8)
6	D3	6	D2	P5_8	I(s)/O	—	—	D8	I(s)/O	CAN0RX	I(s)	TIOC4A	I(s)/O	IRQ3	I(s)	—	—	—	—	—	—	—	—	(8)
7	—	7	—	Vcc																				
8	E3	8	E3	P5_9	I(s)/O	—	—	D9	I(s)/O	CAN0TX	O	TIOC4B	I(s)/O	IRQ4	I(s)	—	—	—	—	—	—	—	—	(8)
9	—	9	—	Vss																				
10	E1	10	D1	P5_10	I(s)/O	—	—	D10	I(s)/O	IERxD*3	I(s)	TIOC4C	I(s)/O	IRQ5	I(s)	—	—	—	—	—	—	—	—	(8)
11	—	11	—	PVcc																				
12	E2	12	E2	P5_11	I(s)/O	—	—	D11	I(s)/O	IETxD*3	O	TIOC4D	I(s)/O	IRQ6	I(s)	—	—	—	—	—	—	—	—	(8)
13	F2	13	E1	P5_12	I(s)/O	—	—	D12	I(s)/O	SSISCK2	I(s)/O	SCK4	I(s)/O	AUDIO_XOUT2	O	—	—	—	—	—	—	—	—	(8)
14	F4	14	F3	P5_13	I(s)/O	—	—	D13	I(s)/O	SSIWS2	I(s)/O	AUDIO_XOUT	O	AUDIO_XOUT3	O	—	—	—	—	—	—	—	—	(8)
15	F3	15	F2	P5_14	I(s)/O	—	—	D14	I(s)/O	SSI DATA2	I(s)/O	RxD4	I(s)	TIOC2A	I(s)/O	—	—	—	—	—	—	—	—	(8)
16	F1	16	F1	P5_15	I(s)/O	—	—	D15	I(s)/O	SD_WP_1	I(s)	TxD4	O	—	—	—	—	—	—	—	—	—	—	(8)
17	G3	17	G3	P6_0	I(s)/O	—	—	D16	I(s)/O	LCD0_DATA8	O	RSPCK0	I(s)/O	TCLKA	I(s)	$\overline{\text{WDTOVF}}$	O	—	—	—	—	—	—	(8)
18	—	18	—	Vss																				
19	G2	19	G1	P6_1	I(s)/O	—	—	D17	I(s)/O	LCD0_DATA9	O	SSL00	I(s)/O	TCLKB	I(s)	—	—	—	—	—	—	—	—	(8)
20	G1	20	G2	P6_2	I(s)/O	—	—	D18	I(s)/O	LCD0_DATA10	O	MOSI0	I(s)/O	TCLKC	I(s)	—	—	—	—	—	—	—	—	(8)
21	—	21	—	Vcc																				
22	H3	22	H3	P6_3	I(s)/O	—	—	D19	I(s)/O	LCD0_DATA11	O	MISO0	I(s)/O	TCLKD	I(s)	—	—	—	—	—	—	—	—	(8)
23	—	23	—	Vss																				
24	H2	24	H2	P6_4	I(s)/O	—	—	D20	I(s)/O	LCD0_DATA12	O	SSISCK3	I(s)/O	MLB_CLK*1	I(s)	—	—	—	—	—	—	—	—	(8)
														AVB_CAPTURE*2	I(s)									
25	—	25	—	PVcc																				
26	H1	26	H1	P6_5	I(s)/O	—	—	D21	I(s)/O	LCD0_DATA13	O	SSIWS3	I(s)/O	MLB_SIG*1	I(s)/O	—	—	—	—	—	—	—	—	(8)
														AVB_GPTP_EXTERN*2	I(s)									
—	—	27	J3	P8_6	I(s)/O	—	—	LCD0_DATA6	O	ET_TXEN	O	IRQ6	I(s)	$\overline{\text{CTS1}}$	I(s)/O	TIOC0C	I(s)/O	—	—	—	—	—	—	(7)
—	—	28	J2	P8_7	I(s)/O	—	—	LCD0_DATA7	O	ET_RXD0	I(s)	IRQ7	I(s)	$\overline{\text{RTS1}}$	I(s)/O	TIOC0D	I(s)/O	—	—	—	—	—	—	(7)
—	—	29	J1	P8_8	I(s)/O	—	—	LCD0_TCON0	O	ET_RXD1	I(s)	AUDIO_XOUT	O	SCK2	I(s)/O	AUDIO_XOUT3	O	—	—	—	—	—	—	(7)
—	—	30	K1	P8_9	I(s)/O	—	—	LCD0_TCON1	O	ET_RXD2	I(s)	CAN1TX	O	RxD2	I(s)	AUDIO_XOUT2	O	—	—	—	—	—	—	(7)
27	J4	31	K2	P6_6	I(s)/O	—	—	D22	I(s)/O	LCD0_DATA14	O	SSITxD3	O	MLB_DAT*3	I(s)/O	—	—	—	—	—	—	—	—	(8)
28	J1	32	K3	P6_7	I(s)/O	—	—	D23	I(s)/O	LCD0_DATA15	O	SSIRxD3	I(s)	IRQ0	I(s)	TIOC3A	I(s)/O	RLIN30 RX*3	I(s)	—	—	TRACE DATA0*4	O	(8)
29	J3	33	K4	P6_8	I(s)/O	—	—	D24	I(s)/O	LCD0_DATA16	O	SSISCK0	I(s)/O	IRQ1	I(s)	TIOC3B	I(s)/O	RLIN30 TX*3	O	—	—	TRACE DATA1*4	O	(8)
—	—	34	—	Vss																				
—	—	35	L1	P8_10	I(s)/O	—	—	LCD0_TCON2	O	ET_RXD3	I(s)	CAN1RX	I(s)	TxD2	O	—	—	—	—	—	—	—	—	(7)
—	—	36	—	PVcc																				
—	—	37	L2	P8_11	I(s)/O	—	—	LCD0_TCON3	O	—	—	SSISCK2	I(s)/O	SCK4	I(s)/O	—	—	—	—	—	—	—	—	(7)
30	J2	38	L3	P6_9	I(s)/O	—	—	D25	I(s)/O	LCD0_DATA17	O	SSIWS0	I(s)/O	IRQ2	I(s)	TIOC3C	I(s)/O	—	—	—	—	TRACE DATA2*4	O	(8)
31	—	39	—	Vss																				
32	K1	40	M3	P6_10	I(s)/O	—	—	D26	I(s)/O	LCD0_DATA18	O	SSITxD0	O	IRQ3	I(s)	TIOC3D	I(s)/O	CAN1 TX	O	—	—	TRACE DATA3*4	O	(8)
33	K2	41	M2	P6_11	I(s)/O	—	—	D27	I(s)/O	LCD0_DATA19	O	SSIRxD0	I(s)	SSI DATA2	I(s)/O	SCK0	I(s)/O	CAN1 RX	I(s)	—	—	TRACE CTL *4	O	(8)

176 QFP	176 BGA	208 QFP	233 BGA	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram
No.	No.	No.	No.	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Figure 2.1
34	—	42	—	Vcc																				
35	K3	43	N2	P6_12	I(s)/O	—	—	D28	I(s)/O	LCD0_ DATA20	O	RSPCK1	I(s)/O	SSI SCK2	I(s)/O	$\overline{\text{RTS0}}$	I(s)/O	DV0_ DATA0	I(s)	—	—	—	—	(8)
36	—	44	—	Vss																				
37	M1	45	N1	CKIO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(5)
38	L2	46	N3	P6_13	I(s)/O	—	—	D29	I(s)/O	LCD0_ DATA21	O	SSL10	I(s)/O	SSI WS2	I(s)/O	$\overline{\text{CTS0}}$	I(s)/O	DV0_ DATA1	I(s)	—	—	—	—	(8)
39	—	47	—	PVcc																				
40	M2	48	P2	P6_14	I(s)/O	—	—	D30	I(s)/O	LCD0_ DATA22	O	MOSI1	I(s)/O	SSI DATA2	I(s)/O	RxD0	I(s)	DV0_ DATA2	I(s)	—	—	—	—	(8)
41	L3	49	R1	P6_15	I(s)/O	—	—	D31	I(s)/O	LCD0_ DATA23	O	MISO1	I(s)/O	—	—	TxD0	O	DV0_ DATA3	I(s)	—	—	—	—	(8)
42	N2	50	R2	P7_0	I(s)/O	—	—	LCD0_ EXTCLK	I(s)	MMC_ CD	I(s)	SD_ CD_1	I(s)	SPDIF_O UT	O	TIOC2A	I(s)/O	DV0_ DATA4	I(s)	SCI_ SCK0	I(s)/O	TRACE CLK*4	O	(7)
43	M3	51	P3	P7_1	I(s)/O	—	—	$\overline{\text{CS1}}$	O	AUDIO_ XOUT	O	SD_ WP_1	I(s)	TxD2	O	—	—	DV0_ DATA5	I(s)	SCI_ RXD0/ IrRXD	I(s)	—	—	(7)
44	N1	52	T1	P7_2	I(s)/O	—	—	$\overline{\text{CS4}}$	O	MMC_D1	I(s)/O	SD_ D1_1	I(s)/O	IRQ4	I(s)	CAN0RX	I(s)	DV0_ DATA6	I(s)	SCI_ TXD0/ IrTXD	O	—	—	(7)
45	P3	53	P5	P7_3	I(s)/O	—	—	$\overline{\text{CS5}}$	O	MMC_D0	I(s)/O	SD_ D0_1	I(s)/O	IRQ3	I(s)	CAN0TX	O	DV0_ DATA7	I(s)	$\overline{\text{SCI_ CTS0/}}$ RTS0	I(s)/O	—	—	(7)
46	—	54	—	Vss																				
47	R2	55	U2	P7_4	I(s)/O	—	—	$\overline{\text{WAIT}}$	I(s)	MMC_ CLK	O	SD_ CLK_1	O	—	—	IETxD*3	O	LCD0_ CLK	O	SCI_ SCK1	I(s)/O	—	—	(7)
48	N4	56	R4	P7_5	I(s)/O	—	—	$\overline{\text{BS}}$	O	MMC_ CMD	I(s)/O	SD_ CMD_1	I(s)/O	TxD0	O	IERxD*3	I(s)	LCD0_ TCON4	O	SCI_ RXD1	I(s)	—	—	(7)
49	P4	57	T3	P7_6	I(s)/O	—	—	$\overline{\text{WE2/}}$ DQMUL	O	MMC_D3	I(s)/O	SD_ D3_1	I(s)/O	IRQ6	I(s)	$\overline{\text{CTS2}}$	I(s)/O	LCD0_ TCON5	O	SCI_ TXD1	O	—	—	(7)
50	—	58	—	PVcc																				
51	R4	59	R5	P7_7	I(s)/O	—	—	$\overline{\text{WE3/}}$ DQMUU/ AH	O	MMC_D2	I(s)/O	SD_ D2_1	I(s)/O	IRQ5	I(s)	$\overline{\text{RTS2}}$	I(s)/O	LCD0_ TCON6	O	$\overline{\text{SCI_ CTS1/}}$ RTS1	I(s)/O	—	—	(7)
52	N5	60	T4	P7_8	I(s)/O	—	—	$\overline{\text{CS2}}$	O	SSISCK1	I(s)/O	DV0_ CLK	I(s)	IRQ3	I(s)	TxD0	O	—	—	—	—	—	—	(7)
53	R5	61	P6	P7_9	I(s)/O	—	—	A25	O	SSIWS1	I(s)/O	DV0_ VSYNC	I(s)	IRQ5	I(s)	SCK3	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	(7)
54	P5	62	U4	P7_10	I(s)/O	—	—	TEND0	O	SSITxD1	O	DV0_ HSYNC	I(s)	—	—	RxD3	I(s)	—	—	—	—	—	—	(7)
55	N6	63	P7	P7_11	I(s)/O	—	—	DACK0	O	SSIRxD1	I(s)	CAN_ CLK	I(s)	SCK2	I(s)/O	TxD3	O	AUDIO_ XOUT	O	AUDIO_ XOUT3	O	—	—	(7)
—	—	64	T5	P8_12	I(s)/O	—	—	LCD0_ TCON4	O	SPDIF_ IN	I(s)	SSIWS2	I(s)/O	RxD4	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	65	—	Vss																				
—	—	66	R6	P8_13	I(s)/O	—	—	LCD0_ TCON5	O	SPDIF_ OUT	O	SSI DATA2	I(s)/O	TxD4	O	—	—	—	—	—	—	—	—	(7)
—	—	67	—	PVcc																				
56	P6	68	U5	P2_0	I(s)/O	—	—	$\overline{\text{CS3}}$	O	RLIN30 RX*3	I(s)	SPDIF_ IN	I(s)	IRQ7	I(s)	—	—	—	—	—	—	—	—	(7)
57	R6	69	T6	P2_1	I(s)/O	—	—	$\overline{\text{RAS}}$	O	RLIN30 TX*3	O	SPDIF_ OUT	O	IRQ6	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	70	U6	P8_14	I(s)/O	—	—	LCD0_ TCON6	O	ET_COL	I(s)	SD_ CD_0	I(s)	SCK1	I(s)/O	—	—	—	—	—	—	—	—	(7)
—	—	71	R7	P8_15	I(s)/O	—	—	—	—	ET_CRS	I(s)	SD_ WP_0	I(s)	RxD1	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	72	T7	P9_0	I(s)/O	—	—	—	—	ET_MDC	O	SD_ D1_0	I(s)/O	TxD1	O	—	—	—	—	—	—	—	—	(7)
—	—	73	U7	P9_1	I(s)/O	—	—	—	—	ET_ MDIO	I(s)/O	SD_ D0_0	I(s)/O	$\overline{\text{CTS0}}$	I(s)/O	—	—	—	—	—	—	—	—	(7)
58	—	74	—	Vcc																				
59	P7	75	R8	P2_2	I(s)/O	—	—	$\overline{\text{CAS}}$	O	CAN1RX	I(s)	TIOC0C	I(s)/O	IRQ5	I(s)	—	—	—	—	—	—	—	—	(7)
60	R7	76	T8	P2_3	I(s)/O	—	—	CKE	O	CAN1TX	O	TIOC0D	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
61	—	77	—	Vss																				
62	—	78	—	PVcc																				
63	M7	79	R9	P0_0	I(s)	MD_ BOOT0	I(s)	—	—	RxD0	I(s)	IRQ4	I(s)	—	—	—	—	—	—	—	—	—	—	(3)
64	N7	80	U8	P0_1	I(s)	MD_ BOOT1	I(s)	—	—	RxD2	I(s)	SSIRxD3	I(s)	$\overline{\text{ADTRG}}$	I(s)	—	—	—	—	—	—	—	—	(3)
65	M8	81	T10	P0_2	I(s)	MD_ CLK	I(s)	—	—	RxD1	I(s)	IRQ7	I(s)	—	—	—	—	—	—	—	—	—	—	(3)
66	M6	82	R10	P0_3	I(s)	MD_ CLKS	I(s)	—	—	RxD3	I(s)	SPDIF_ IN	I(s)	—	—	—	—	—	—	—	—	—	—	(3)
67	P8	83	T9	RTC_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(11)
68	R8	84	U9	RTC_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
69	M9	85	P10	PLLVcc																				

176 QFP	176 BGA	208 QFP	233 BGA	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram
No.	No.	No.	No.	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Figure 2.1
70	R9	86	U11	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
71	P9	87	T11	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
72	—	88	—	Vss																				
73	—	89	—	Vss																				
74	N9	90	R11	NMI	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
75	—	91	—	Vss																				
76	R10	92	U12	$\overline{\text{RES}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
77	—	93	—	PVcc																				
78	P10	94	T12	P1_8	I(s)	—	—	AN0	I(a)	IRQ0	I(s)	RxD0	I(s)	DV0_ DATA4	I(s)	—	—	—	—	—	—	—	—	(4)
79	N10	95	U13	P1_9	I(s)	—	—	AN1	I(a)	IRQ1	I(s)	RxD1	I(s)	DV0_ DATA5	I(s)	—	—	—	—	—	—	—	—	(4)
80	R11	96	R12	P1_10	I(s)	—	—	AN2	I(a)	IRQ2	I(s)	RxD2	I(s)	DV0_ DATA6	I(s)	—	—	—	—	—	—	—	—	(4)
81	N11	97	T13	P1_11	I(s)	—	—	AN3	I(a)	IRQ3	I(s)	RxD3	I(s)	DV0_ DATA7	I(s)	—	—	—	—	—	—	—	—	(4)
82	P12	98	U14	P1_12	I(s)	—	—	AN4	I(a)	IRQ4	I(s)	ET_ RXD0	I(s)	VIO_D4	I(s)	—	—	—	—	—	—	—	—	(4)
83	P11	99	T14	P1_13	I(s)	—	—	AN5	I(a)	IRQ5	I(s)	ET_ RXD1	I(s)	VIO_D5	I(s)	—	—	—	—	—	—	—	—	(4)
84	N12	100	R13	P1_14	I(s)	—	—	AN6	I(a)	IRQ6	I(s)	ET_ RXD2	I(s)	VIO_D6	I(s)	—	—	—	—	—	—	—	—	(4)
85	R12	101	R14	P1_15	I(s)	—	—	AN7	I(a)	IRQ7	I(s)	ET_ RXD3	I(s)	VIO_D7	I(s)	—	—	—	—	—	—	—	—	(4)
86	P13	102	T15	AVcc																				
87	R13	103	U15	AVss																				
88	R14	104	U16	AVref																				
89	N14	105	N14	BSCANP	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(1)
90	—	106	—	PVcc																				
91	P15	107	T17	AUDIO_ X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
92	N15	108	R17	AUDIO_ X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
93	—	109	—	Vss																				
94	M14	110	P15	P2_4	I(s)/O	—	—	$\overline{\text{WE0}}$/ DQMLL	O	—	—	TIOC4A	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
95	—	111	—	Vcc																				
96	M13	112	R16	P2_5	I(s)/O	—	—	$\overline{\text{WE1}}$/$\overline{\text{WE}}$/ DQMLU	O	—	—	TIOC3A	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
97	L13	113	M14	$\overline{\text{TRST}}$	I(s)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(3)
98	L14	114	N15	JP0_1	I	—	—	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(6)
99	L15	115	P16	JP0_0	I	—	—	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
100	L12	116	M15	TMS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
101	K14	117	N16	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(2)
102	—	118	—	Vss																				
103	K13	119	N17	P3_0	I(s)/O	—	—	A1	O	SD_ D2_0	I(s)/O	LCD0_ DATA0	O	ET_ TXCLK	I(s)	—	—	—	—	—	—	—	—	(7)
104	K12	120	M16	P3_1	I(s)/O	—	—	A2	O	SD_ D3_0	I(s)/O	LCD0_ DATA1	O	ET_ TXER	O	—	—	—	—	—	—	—	—	(7)
105	—	121	—	Vcc																				
106	J13	122	L15	P3_2	I(s)/O	—	—	A3	O	SD_ CMD_0	I(s)/O	LCD0_ DATA2	O	ET_ TXEN	O	—	—	—	—	—	—	—	—	(7)
107	—	123	—	Vss																				
108	J15	124	M17	P3_3	I(s)/O	—	—	A4	O	SD_ CLK_0	O	LCD0_ DATA3	O	ET_ RXCLK	I(s)	—	—	—	—	—	—	—	—	(7)
109	—	125	—	PVcc																				
110	J14	126	L16	P3_4	I(s)/O	—	—	A5	O	SD_ D0_0	I(s)/O	LCD0_ DATA4	O	ET_ RXER	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	127	K17	P9_2	I(s)/O	—	—	RSPCK2	I(s)/O	ET_ RXCLK	I(s)	SD_ CLK_0	O	$\overline{\text{RTS0}}$	I(s)/O	TIOC1A	I(s)/O	—	—	—	—	—	—	(7)
—	—	128	—	Vss																				
—	—	129	K15	P9_3	I(s)/O	—	—	SSL20	I(s)/O	ET_ RXER	I(s)	SD_ CMD_0	I(s)/O	SCK0	I(s)/O	TIOC1B	I(s)/O	—	—	—	—	—	—	(7)
—	—	130	—	PVcc																				
111	H15	131	K16	P3_5	I(s)/O	—	—	A6	O	SD_ D1_0	I(s)/O	LCD0_ DATA5	O	ET_ RXDV	I(s)	—	—	—	—	—	—	—	—	(7)
112	H13	132	J15	P3_6	I(s)/O	—	—	A7	O	SD_ WP_0	I(s)	LCD0_ DATA6	O	ET_ COL	I(s)	—	—	—	—	—	—	—	—	(7)
113	H14	133	J16	P3_7	I(s)/O	—	—	A8	O	SD_ CD_0	I(s)	LCD0_ DATA7	O	ET_ CRS	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	134	—	Vss																				
—	—	135	H17	P9_4	I(s)/O	—	—	MOSI2	I(s)/O	ET_ RXDV	I(s)	SD_ D3_0	I(s)/O	RxD0	I(s)	TIOC2A	I(s)/O	—	—	—	—	—	—	(7)

176 QFP	176 BGA	208 QFP	233 BGA	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram
No.	No.	No.	No.	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Figure 2.1
—	—	136	—	PVcc																				
—	—	137	H16	P9_5	I(s)/O	—	—	MISO2	I(s)/O	—	—	SD_ D2_0	I(s)/O	TxD0	O	TIOC2B	I(s)/O	—	—	—	—	—	—	(7)
114	G12	138	H15	P3_8	I(s)/O	—	—	A9	O	—	—	AUDIO_C LK	I(s)	DV0_ DATA8	I(s)	SCK3	I(s)/O	—	—	—	—	—	—	(7)
115	G13	139	H14	P3_9	I(s)/O	—	—	A10	O	—	—	SPDIF_ OUT	O	DV0_ DATA9	I(s)	TxD3	O	—	—	—	—	—	—	(7)
116	—	140	—	Vss																				
117	G15	141	G14	P3_10	I(s)/O	—	—	A11	O	SPBIO 01_0	I(s)/O	TIOC3B	I(s)/O	DV0_ DATA10	I(s)	RxD3	I(s)	—	—	—	—	—	—	(7)
118	G14	142	G17	P3_11	I(s)/O	—	—	A12	O	SPBIO 11_0	I(s)/O	TIOC3A	I(s)/O	DV0_ DATA11	I(s)	—	—	—	—	—	—	—	—	(7)
119	—	143	—	Vcc																				
120	F15	144	G16	P3_12	I(s)/O	—	—	A13	O	SPBIO 21_0	I(s)/O	TIOC3C	I(s)/O	DV0_ DATA12	I(s)	—	—	—	—	—	—	—	—	(7)
121	—	145	—	Vss																				
122	F14	146	G15	P3_13	I(s)/O	—	—	A14	O	SPBIO31_ 0	I(s)/O	TIOC3D	I(s)/O	DV0_ DATA13	I(s)	—	—	—	—	—	—	—	—	(7)
123	—	147	—	PVcc																				
124	F13	148	F17	P3_14	I(s)/O	—	—	A15	O	VIO_CLK	I(s)	SPDIF_ IN	I(s)	DV0_ DATA14	I(s)	SCK1	I(s)/O	AUDIO_ XOUT2	O	—	—	—	—	(7)
125	E14	149	F16	P1_0	I(s)/O(o)	—	—	RIIC0SCL	I(s)/ O(o)	IRQ4	I(s)	ET_ RXD0	I(s)	DV0_ DATA0	I(s)	—	—	—	—	—	—	—	—	(9)
126	E15	150	F15	P1_1	I(s)/O(o)	—	—	RIIC0SDA	I(s)/ O(o)	IRQ5	I(s)	ET_ RXD1	I(s)	DV0_ DATA1	I(s)	—	—	—	—	—	—	—	—	(9)
127	E13	151	E17	P1_2	I(s)/O(o)	—	—	RIIC1SCL	I(s)/ O(o)	IRQ6	I(s)	ET_ RXD2	I(s)	DV0_ DATA2	I(s)	—	—	—	—	—	—	—	—	(9)
128	D15	152	E16	P1_3	I(s)/O(o)	—	—	RIIC1SDA	I(s)/ O(o)	IRQ7	I(s)	ET_ RXD3	I(s)	DV0_ DATA3	I(s)	—	—	—	—	—	—	—	—	(9)
129	D14	153	E15	P1_4	I(s)/O(o)	—	—	RIIC2SCL	I(s)/ O(o)	IRQ0	I(s)	DREQ0	I(s)	VIO_D0	I(s)	—	—	—	—	—	—	—	—	(9)
130	C15	154	D17	P1_5	I(s)/O(o)	—	—	RIIC2SDA	I(s)/ O(o)	IRQ1	I(s)	—	—	VIO_D1	I(s)	—	—	—	—	—	—	—	—	(9)
131	C14	155	D16	P1_6	I(s)/O(o)	—	—	RIIC3SCL	I(s)/ O(o)	IRQ2	I(s)	SSIRxD0	I(s)	VIO_D2	I(s)	—	—	—	—	—	—	—	—	(9)
132	B15	156	C17	P1_7	I(s)/O(o)	—	—	RIIC3SDA	I(s)/ O(o)	IRQ3	I(s)	RxD2	I(s)	VIO_D3	I(s)	—	—	—	—	—	—	—	—	(9)
133	A14	157	A16	P3_15	I(s)/O	—	—	A16	O	VIO_ FLD	I(s)	—	—	DV0_ DATA15	I(s)	TxD1	O	—	—	—	—	—	—	(7)
134	B13	158	A15	P2_6	I(s)/O	—	—	RD/$\overline{WR}$	O	SSIRxD3	I(s)	TIOC2A	I(s)/O	—	—	—	—	—	—	—	—	—	—	(7)
135	C12	159	B15	P2_7	I(s)/O	—	—	$\overline{CS0}$	O	SSISCK3	I(s)/O	TIOC1A	I(s)/O	IRQ2	I(s)	—	—	—	—	—	—	—	—	(7)
136	A13	160	B14	P2_8	I(s)/O	—	—	$\overline{RD}$	O	SSITxD3	O	TIOC0A	I(s)/O	—	—	CAN0TX	O	—	—	—	—	—	—	(7)
137	B12	161	C14	P2_9	I(s)/O	—	—	A0	O	SSIWS3	I(s)/O	SCK0	I(s)/O	IRQ1	I(s)	CAN0RX	I(s)	—	—	—	—	—	—	(7)
138	—	162	—	Vss																				
139	A12	163	A14	USB_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	(10)
140	B11	164	B13	USB_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
141	—	165	—	USBDP Vcc																				
142	—	166	—	USBDP Vss																				
143	B10	167	B12	DM1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
144	A10	168	A12	DP1	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
145	C10	169	C12	VBUS1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
146	—	170	—	USBD Vcc																				
147	—	171	—	USBD Vss																				
148	—	172	—	USBDP Vcc																				
149	—	173	—	USBDP Vss																				
150	A9	174	A11	DM0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
151	B9	175	B11	DP0	I/O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
152	C9	176	C11	VBUS0	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
153	—	177	—	USBD Vcc																				
154	—	178	—	USBD Vss																				
155	B8	179	B10	REFRIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	
156	—	180	—	USBAP Vss																				
157	D10	181	D12	USBAP Vcc																				
158	C8	182	C10	USBA Vcc																				

176 QFP	176 BGA	208 QFP	233 BGA	Port function/ dedicated function		Mode function		Function 1		Function 2		Function 3		Function 4		Function 5		Function 6		Function 7		Function 8		Simplified Circuit Diagram
No.	No.	No.	No.	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Symbol	I/O	Figure 2.1
159	—	183	—	USBA Vss																				
160	—	184	—	USBU Vcc																				
161	—	185	—	USBU Vss																				
162	—	186	—	Vss																				
163	—	187	—	Vss																				
164	C7	188	A9	P4_0	I(s)/O	—	—	A17	O	VIO_VD	I(s)	TIOC1B	I(s)/O	ET_MDC	O	$\overline{CTS1}$	I(s)/O	—	—	—	—	—	—	(7)
165	B7	189	C9	P4_1	I(s)/O	—	—	A18	O	VIO_HD	I(s)	TIOC2B	I(s)/O	ET_MDIO	I(s)/O	$\overline{RTS1}$	I(s)/O	—	—	—	—	—	—	(7)
166	C6	190	A8	P4_2	I(s)/O	—	—	A19	O	SPBIO 20_0	I(s)/O	TRACE DATA2*3	O	—	—	—	—	—	—	—	—	—	—	(7)
167	A6	191	B8	P4_3	I(s)/O	—	—	A20	O	SPBIO 30_0	I(s)/O	TRACE DATA3*3	O	—	—	—	—	—	—	—	—	—	—	(7)
—	—	192	C8	P8_0	I(s)/O	—	—	LCD0_DATA0	O	ET_TXD0	O	SSISCK1	I(s)/O	SCK3	I(s)/O	—	—	—	—	—	—	—	—	(7)
—	—	193	—	Vss																				
—	—	194	B7	P8_1	I(s)/O	—	—	LCD0_DATA1	O	ET_TXD1	O	SSIWS1	I(s)/O	RxD3	I(s)	—	—	—	—	—	—	—	—	(7)
—	—	195	—	PVcc																				
168	B6	196	C7	P4_4	I(s)/O	—	—	A21	O	SPBCLK_0	O	TRACE CLK*3	O	—	—	—	—	—	—	—	—	—	—	(7)
169	A5	197	A6	P4_5	I(s)/O	—	—	A22	O	SPBSSL_0	O	TRACE CTL*3	O	—	—	—	—	—	—	—	—	—	—	(7)
—	—	198	B6	P8_2	I(s)/O	—	—	LCD0_DATA2	O	ET_TXD2	O	SSITxD1	O	TxD3	O	—	—	—	—	—	—	—	—	(7)
—	—	199	D7	P8_3	I(s)/O	—	—	LCD0_DATA3	O	ET_TXD3	O	SSIRxD1	I(s)	—	—	—	—	—	—	—	—	—	—	(7)
—	—	200	C6	P8_4	I(s)/O	—	—	LCD0_DATA4	O	ET_TXCLK	I(s)	—	—	$\overline{CTS2}$	I(s)/O	TIOC0A	I(s)/O	—	—	—	—	—	—	(7)
—	—	201	B5	P8_5	I(s)/O	—	—	LCD0_DATA5	O	ET_TXER	O	—	—	$\overline{RTS2}$	I(s)/O	TIOC0B	I(s)/O	—	—	—	—	—	—	(7)
170	B5	202	A5	P4_6	I(s)/O	—	—	A23	O	SPBIO 00_0	I(s)/O	TRACE DATA0*3	O	—	—	—	—	—	—	—	—	—	—	(7)
171	—	203	—	Vss																				
172	C5	204	C5	P4_7	I(s)/O	—	—	A24	O	SPBIO 10_0	I(s)/O	TRACE DATA1*3	O	—	—	—	—	—	—	—	—	—	—	(7)
173	A4	205	A4	P5_0	I(s)/O	—	—	D0	I(s)/O	MMC_D4	I(s)/O	ET_TXD0	O	DV0_DATA16	I(s)	LCD0_TCON0	O	—	—	—	—	—	—	(8)
174	—	206	—	PVcc																				
175	B4	207	B4	P5_1	I(s)/O	—	—	D1	I(s)/O	MMC_D5	I(s)/O	ET_TXD1	O	DV0_DATA17	I(s)	LCD0_TCON1	O	—	—	—	—	—	—	(8)
176	A3	208	A3	P5_2	I(s)/O	—	—	D2	I(s)/O	MMC_D6	I(s)/O	ET_TXD2	O	DV0_DATA18	I(s)	LCD0_TCON2	O	—	—	—	—	—	—	(8)

[Legend]

(s): Schmitt

(a): Analog

(o): Open drain

Note: • Pins to which the PVcc, Vcc, and Vss functions can be allocated on 176-pin BGA products are listed below.
PVcc: D4, D11, D13, E4, E12, F12, K4, L4, M5, M10, M11, P1
Vcc: A2, B3, C4, D5, D6, D7, M12, N13, P14, R15
Vss: A1, A7, A8, A11, A15, B2, B14, C3, C11, C13, D8, D9, D12, G4, H4, H12, J12, K15, L1, M4, M15, N3, N8, P2, R1, R3

Note: • Pins to which the PVcc, Vcc, and Vss functions can be allocated on 233-pin BGA products are listed below.
PVcc: B17, C13, C16, D8, D9, D15, E14, F4, F14, G4, L4, M4, N4, P1, P8, P9, P12, P13
Vcc: A2, B3, C4, D5, D6, H4, J4, J14, K14, L14, P14, R15, T16, U17
Vss: A1, A7, A10, A13, A17, B2, B9, B16, C3, C15, D4, D10, D11, D13, D14, G7, G8, G9, G10, G11, H7, H8, H9, H10, H11, J7, J8, J9, J10, J11, J17, K7, K8, K9, K10, K11, L7, L8, L9, L10, L11, L17, M1, P4, P11, P17, R3, T2, U1, U3, U10

Note 1. RZ/A1L only. "-" for the RZ/A1LC.
Note 2. RZ/A1LU only. "-" for the RZ/A1LC.
Note 3. RZ/A1L only. "-" for the RZ/A1LU and RZ/A1LC.
Note 4. RZ/A1LU and RZ/A1LC only. "-" for the RZ/A1L.

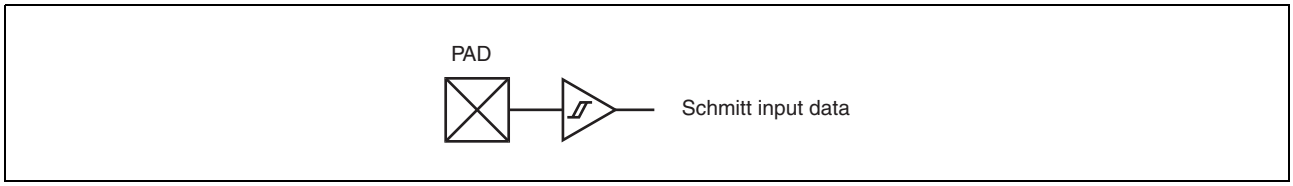


Figure 2.1 (1) Simplified Circuit Diagram (Schmitt Input Buffer)

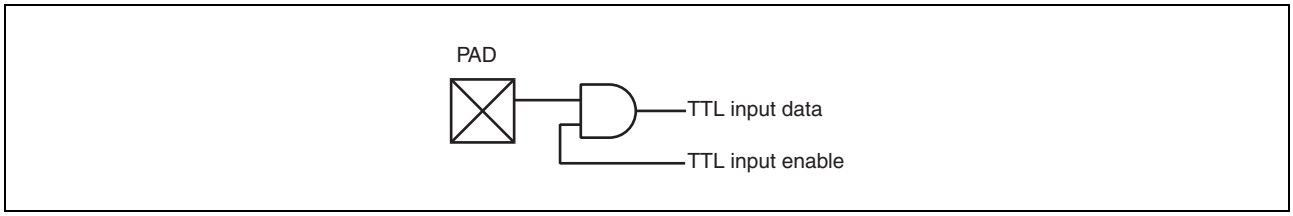


Figure 2.1 (2) Simplified Circuit Diagram (TTL AND Input Buffer)

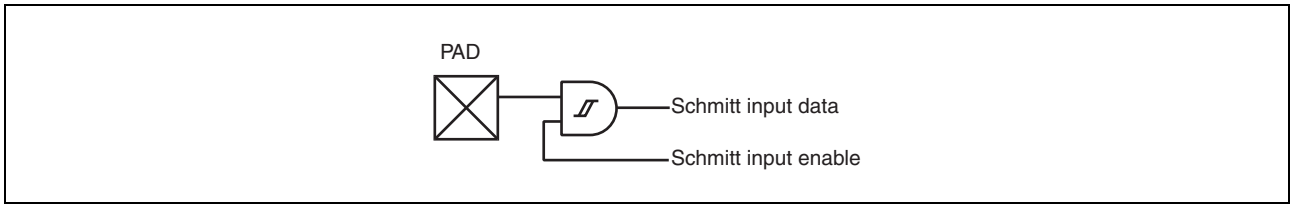


Figure 2.1 (3) Simplified Circuit Diagram (Schmitt AND Input Buffer)

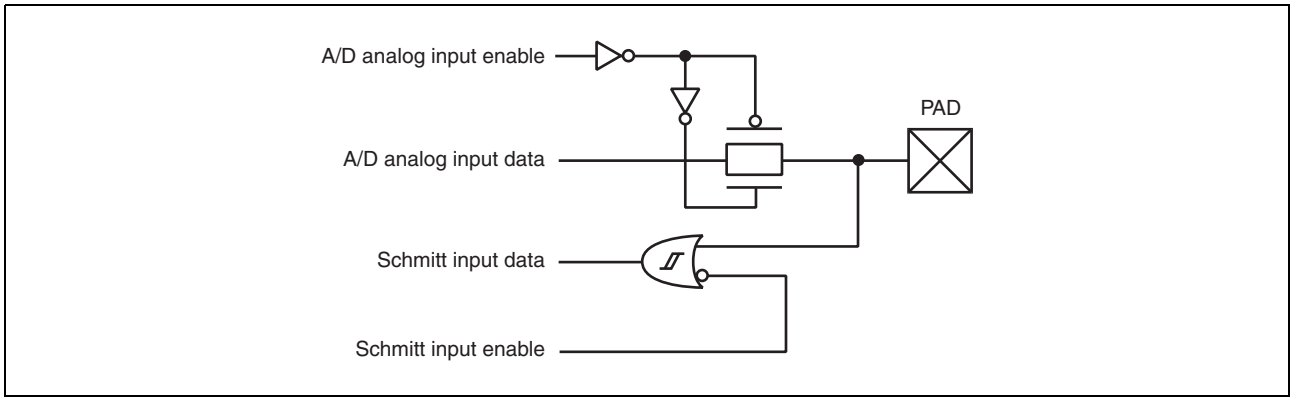


Figure 2.1 (4) Simplified Circuit Diagram (Schmitt OR Input and A/D Input Buffer)

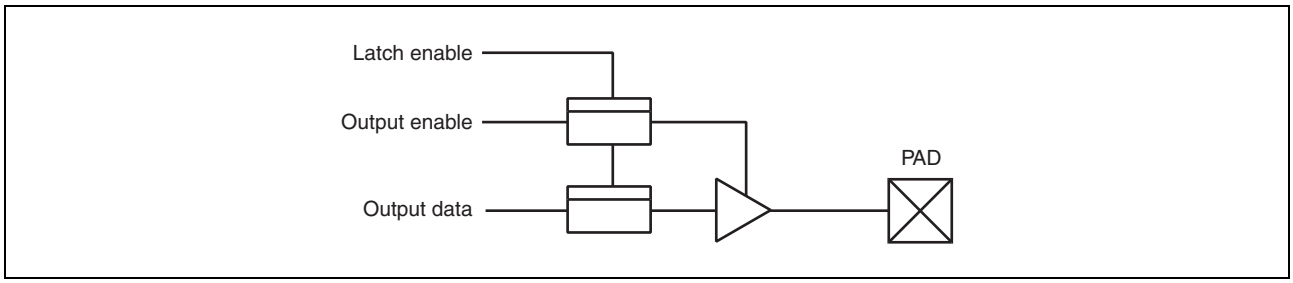


Figure 2.1 (5) Simplified Circuit Diagram (Output Buffer with Enable, with Latch)

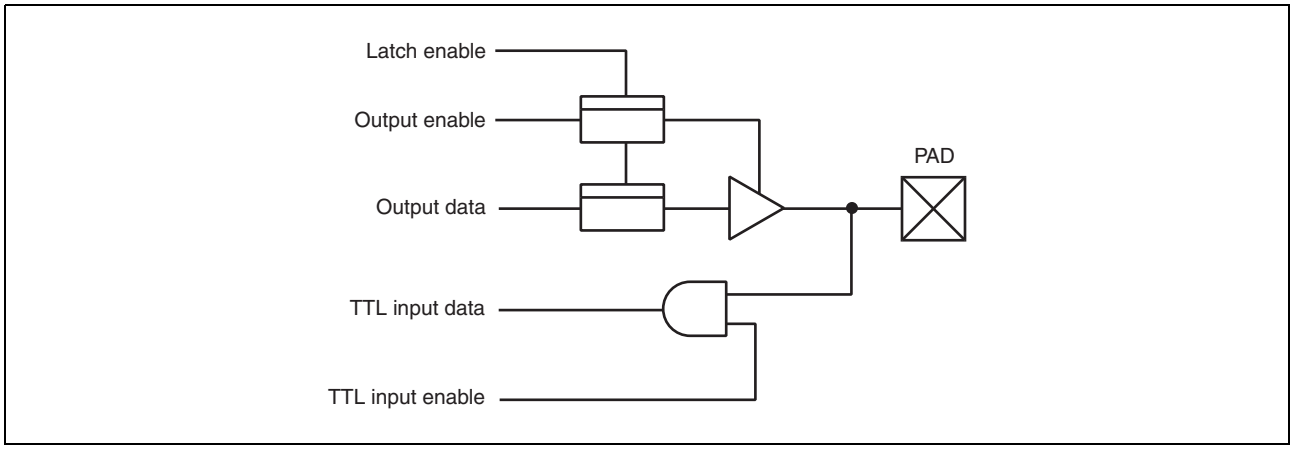


Figure 2.1 (6) Simplified Circuit Diagram (Bidirectional Buffer, TTL AND Input, with Latch)

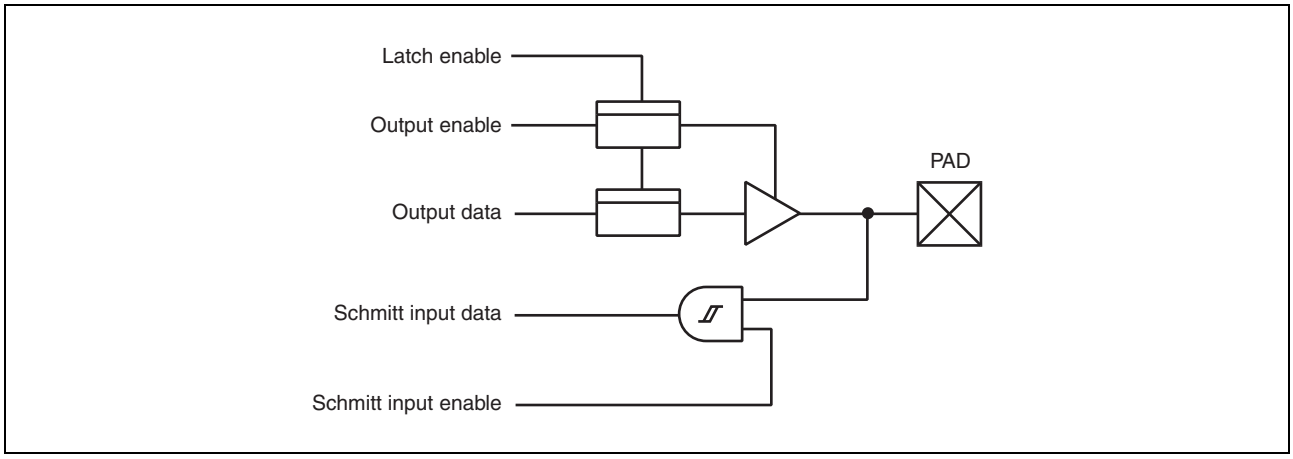


Figure 2.1 (7) Simplified Circuit Diagram (Bidirectional Buffer, Schmitt AND Input, with Latch)

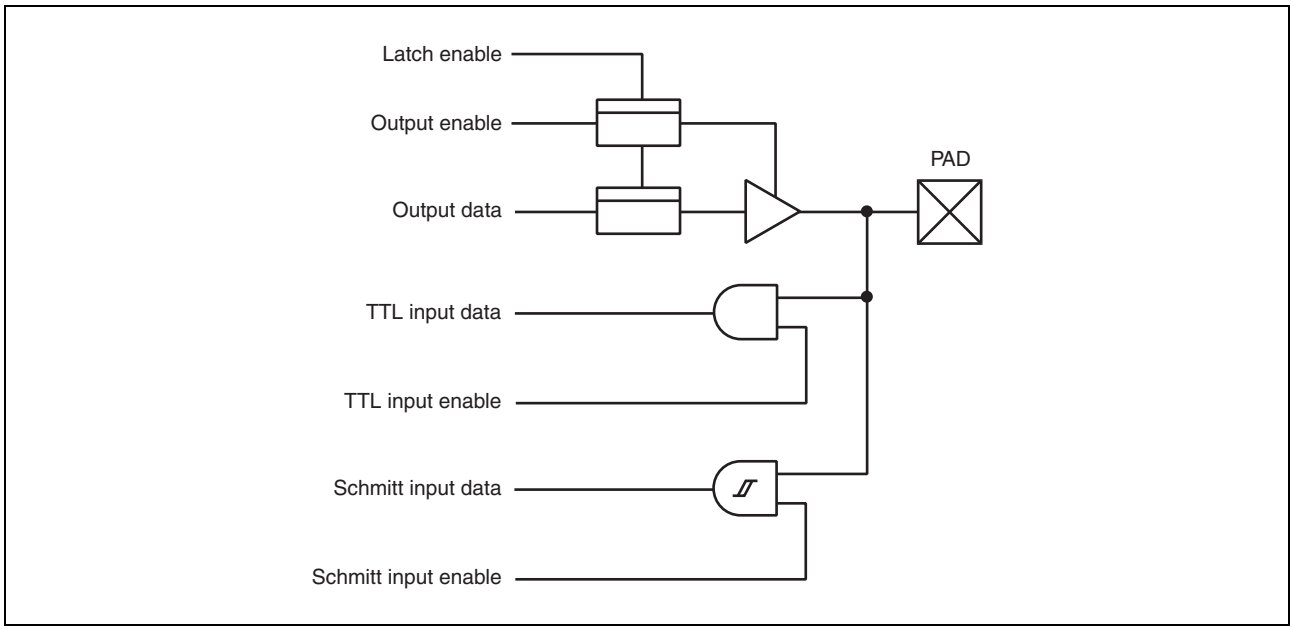


Figure 2.1 (8) Simplified Circuit Diagram (Bidirectional Buffer, TTL AND Input, Schmitt AND Input, with Latch)

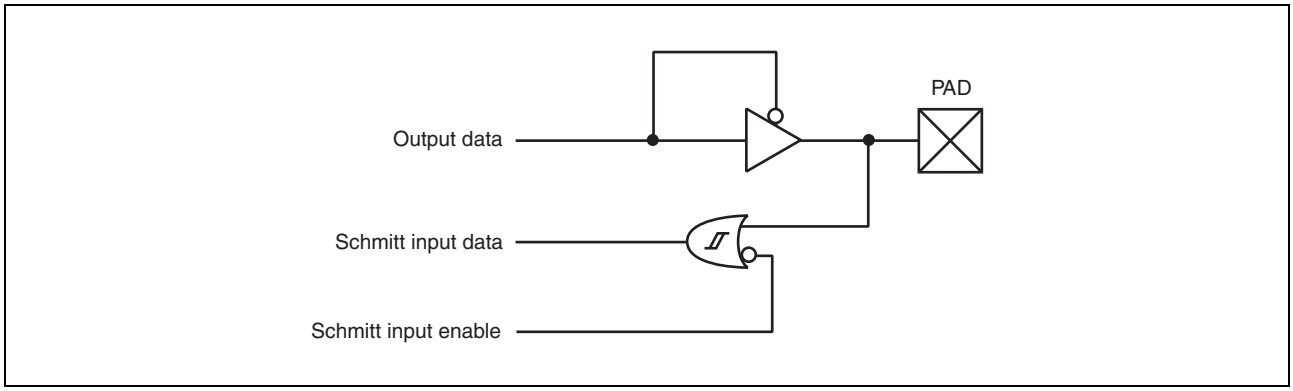


Figure 2.1 (9) Simplified Circuit Diagram (Open Drain Output and Schmitt OR Input Buffer)

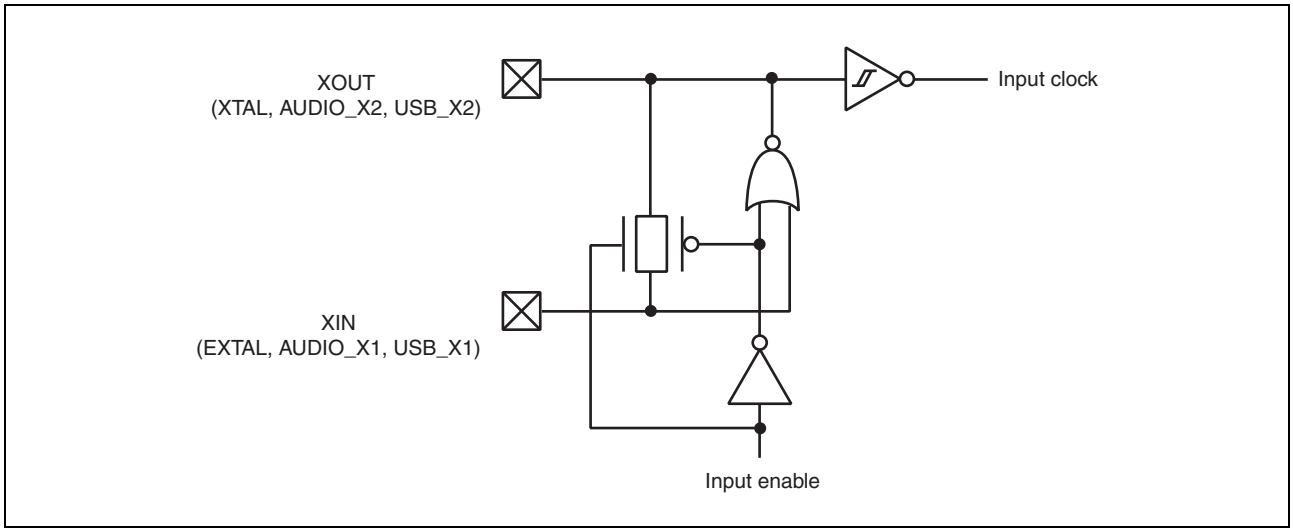


Figure 2.1 (10) Simplified Circuit Diagram (Oscillation Buffer 1)

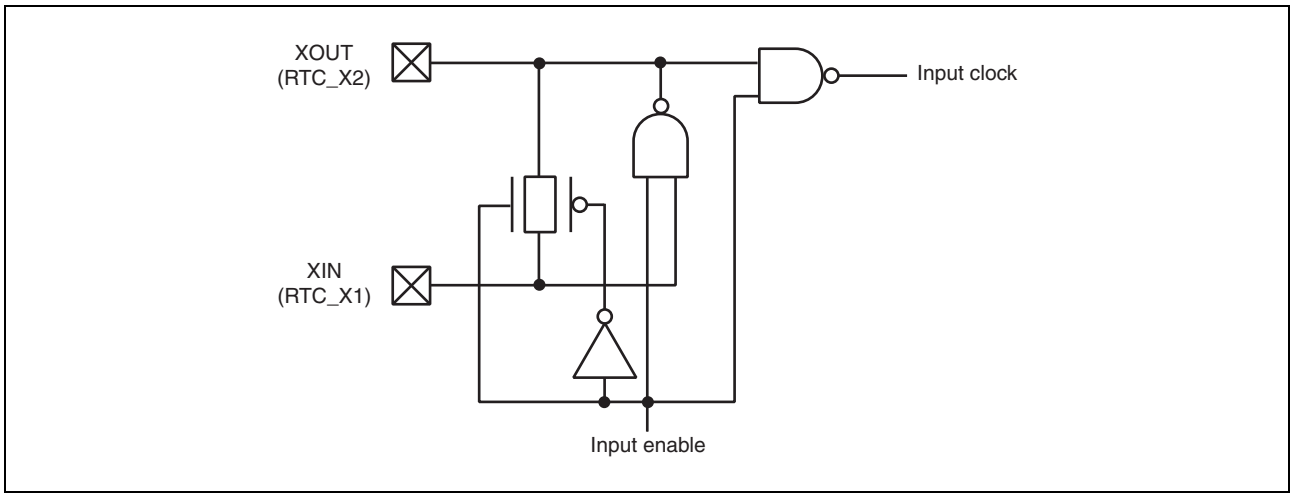


Figure 2.1 (11) Simplified Circuit Diagram (Oscillation Buffer 2)

2.2 Pin Assignment

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
A	Vss	Vcc	P5_2	P5_0	P4_5	P4_3	Vss	Vss	DM0	DP1	Vss	USB_X1	P2_8	P3_15	Vss	A
B	P5_3	Vss	Vcc	P5_1	P4_6	P4_4	P4_1	REFRIN	DP0	DM1	USB_X2	P2_9	P2_6	Vss	P1_7	B
C	P5_6	P5_4	Vss	Vcc	P4_7	P4_2	P4_0	USBAVcc	VBUS0	VBUS1	Vss	P2_7	Vss	P1_6	P1_5	C
D	P5_7	P5_5	P5_8	PVcc	Vcc	Vcc	Vcc	Vss	Vss	USBAPVcc	PVcc	Vss	PVcc	P1_4	P1_3	D
E	P5_10	P5_11	P5_9	PVcc								PVcc	P1_2	P1_0	P1_1	E
F	P5_15	P5_12	P5_14	P5_13								PVcc	P3_14	P3_13	P3_12	F
G	P6_2	P6_1	P6_0	Vss								P3_8	P3_9	P3_11	P3_10	G
H	P6_5	P6_4	P6_3	Vss								Vss	P3_6	P3_7	P3_5	H
J	P6_7	P6_9	P6_8	P6_6								Vss	P3_2	P3_4	P3_3	J
K	P6_10	P6_11	P6_12	PVcc								P3_1	P3_0	TCK	Vss	K
L	Vss	P6_13	P6_15	PVcc								TMS	$\overline{\text{TRST}}$	JP0_1	JP0_0	L
M	CKIO	P6_14	P7_1	Vss	PVcc	P0_3	P0_0	P0_2	PLLVcc	PVcc	PVcc	Vcc	P2_5	P2_4	Vss	M
N	P7_2	P7_0	Vss	P7_5	P7_8	P7_11	P0_1	Vss	NMI	P1_9	P1_11	P1_14	Vcc	BSCANP	AUDIO_X2	N
P	PVcc	Vss	P7_3	P7_6	P7_10	P2_0	P2_2	RTC_X1	XTAL	P1_8	P1_13	P1_12	AVcc	Vcc	AUDIO_X1	P
R	Vss	P7_4	Vss	P7_7	P7_9	P2_1	P2_3	RTC_X2	EXTAL	$\overline{\text{RES}}$	P1_10	P1_15	AVss	AVref	Vcc	R
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Figure 2.2 Pin Assignment of the 176-pin BGA (Upper Perspective View)

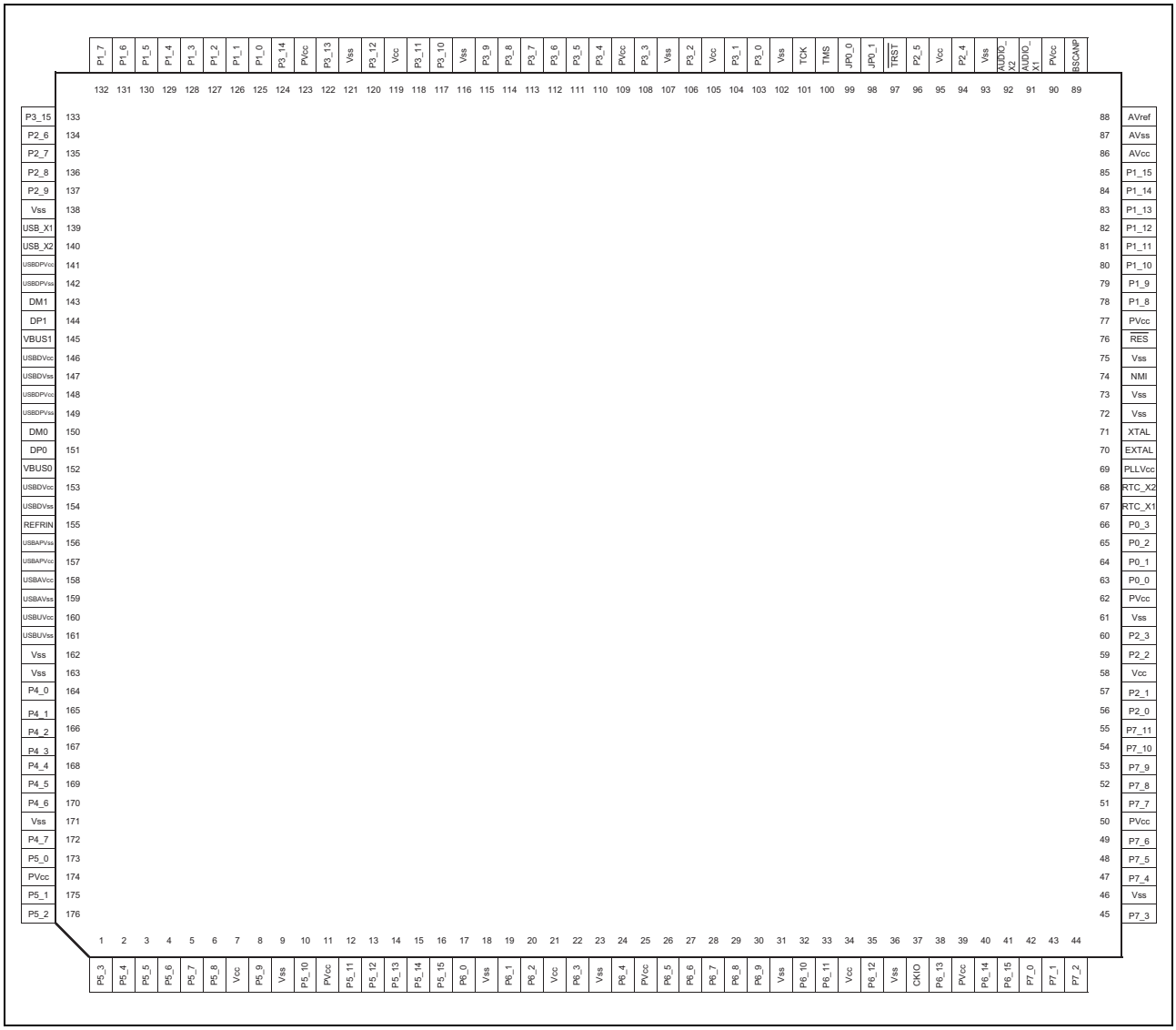


Figure 2.3 Pin Assignment of the 176-pin QFP (Top View)

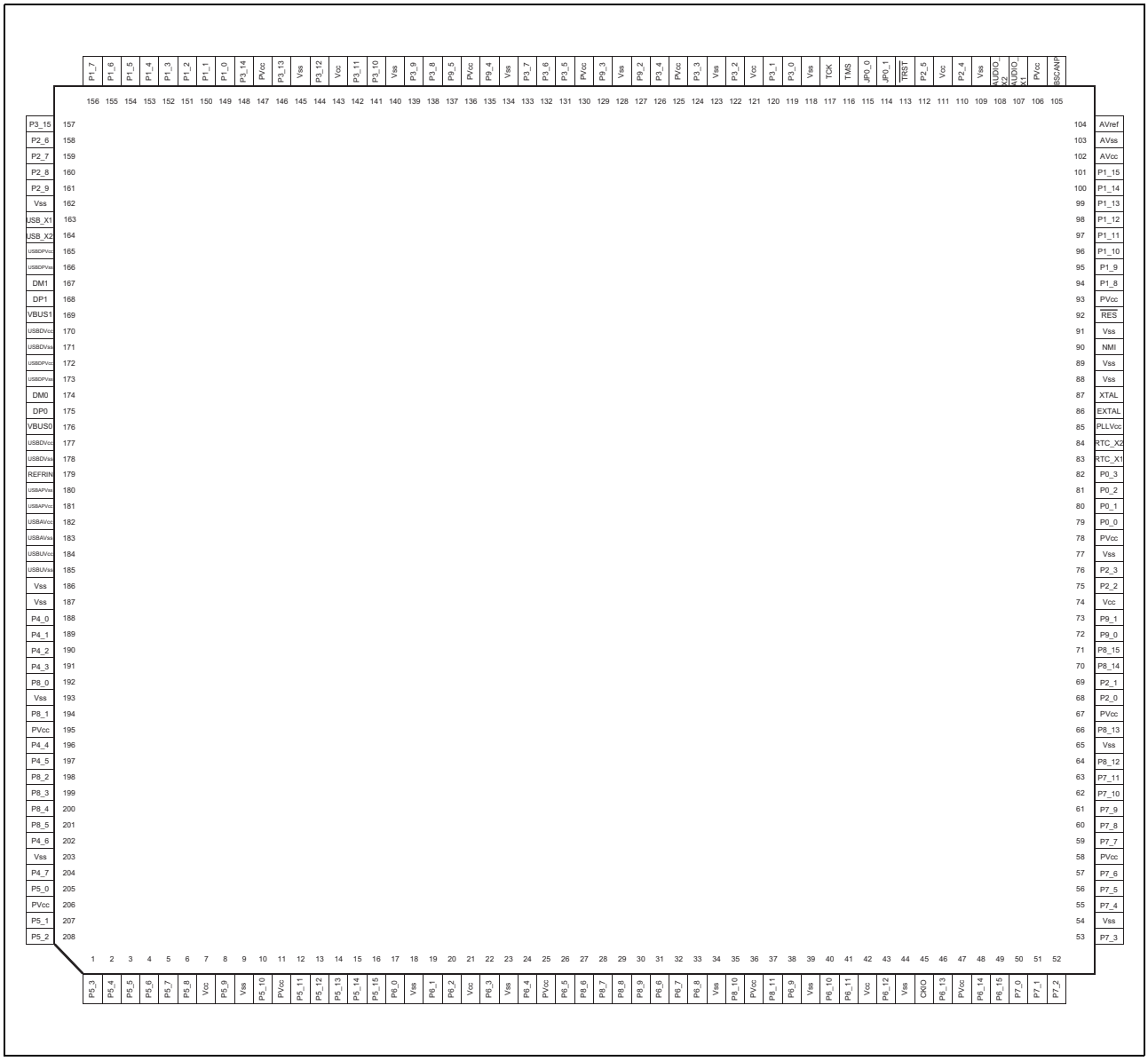


Figure 2.4 Pin Assignment of the 208-pin QFP (Top View)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	Vss	Vcc	P5_2	P5_0	P4_6	P4_5	Vss	P4_2	P4_0	Vss	DM0	DP1	Vss	USB_X1	P2_6	P3_15	Vss	A
B	P5_3	Vss	Vcc	P5_1	P8_5	P8_2	P8_1	P4_3	VSS	REFRIN	DP0	DM1	USB_X2	P2_8	P2_7	Vss	PVcc	B
C	P5_7	P5_4	Vss	Vcc	P4_7	P8_4	P4_4	P8_0	P4_1	USBAVcc	VBUS0	VBUS1	PVcc	P2_9	Vss	PVcc	P1_7	C
D	P5_10	P5_8	P5_6	Vss	Vcc	Vcc	P8_3	PVcc	PVcc	Vss	Vss	USBAPVcc	Vss	Vss	PVcc	P1_6	P1_5	D
E	P5_12	P5_11	P5_9	P5_5										PVcc	P1_4	P1_3	P1_2	E
F	P5_15	P5_14	P5_13	PVcc										PVcc	P1_1	P1_0	P3_14	F
G	P6_1	P6_2	P6_0	PVcc			VSS	VSS	VSS	VSS	VSS			P3_10	P3_13	P3_12	P3_11	G
H	P6_5	P6_4	P6_3	Vcc			VSS	VSS	VSS	VSS	VSS			P3_9	P3_8	P9_5	P9_4	H
J	P8_8	P8_7	P8_6	Vcc			VSS	VSS	VSS	VSS	VSS			Vcc	P3_6	P3_7	Vss	J
K	P8_9	P6_6	P6_7	P6_8			VSS	VSS	VSS	VSS	VSS			Vcc	P9_3	P3_5	P9_2	K
L	P8_10	P8_11	P6_9	PVcc			VSS	VSS	VSS	VSS	VSS			Vcc	P3_2	P3_4	Vss	L
M	Vss	P6_11	P6_10	PVcc										$\overline{\text{TRST}}$	TMS	P3_1	P3_3	M
N	CKIO	P6_12	P6_13	PVcc										BSCANP	JP0_1	TCK	P3_0	N
P	PVcc	P6_14	P7_1	Vss	P7_3	P7_9	P7_11	PVcc	PVcc	PLLVcc	Vss	PVcc	PVcc	Vcc	P2_4	JP0_0	Vss	P
R	P6_15	P7_0	Vss	P7_5	P7_7	P8_13	P8_15	P2_2	P0_0	P0_3	NMI	P1_10	P1_14	P1_15	Vcc	P2_5	AUDIO_X2	R
T	P7_2	Vss	P7_6	P7_8	P8_12	P2_1	P9_0	P2_3	RTC_X1	P0_2	XTAL	P1_8	P1_11	P1_13	AVcc	Vcc	AUDIO_X1	T
U	Vss	P7_4	Vss	P7_10	P2_0	P8_14	P9_1	P0_1	RTC_X2	Vss	EXTAL	$\overline{\text{RES}}$	P1_9	P1_12	AVss	AVref	Vcc	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

Figure 2.5 Pin Assignment of the 233-pin BGA (Upper Perspective View)

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Table 3.1 Absolute Maximum Ratings

Item		Symbol	Value	Unit
Power supply voltage (I/O)		PV_{CC}	–0.3 to 4.2	V
Power supply voltage (Internal)		V_{CC}	–0.3 to 1.6	V
PLL power supply voltage		$PLLV_{CC}$	–0.3 to 1.6	V
Analog power supply voltage		AV_{CC}	–0.3 to 4.2	V
Analog reference voltage		AVref	–0.3 to AV_{CC} +0.3	V
USB transceiver analog power supply voltage (I/O)		$USBAPV_{CC}$	–0.3 to 4.2	V
USB transceiver digital power supply voltage (I/O) Note: Products in BGA packages do not have this pin.		$USBDPV_{CC}$	–0.3 to 4.2	V
USB transceiver analog power supply voltage (internal)		$USBAV_{CC}$	–0.3 to 1.6	V
USB transceiver digital power supply voltage (internal) Note: Products in BGA packages do not have this pin.		$USBDV_{CC}$	–0.3 to 1.6	V
Power supply for USB 480 MHz (internal) Note: Products in BGA packages do not have this pin.		$USBUV_{CC}$	–0.3 to 1.6	V
Input voltage	VBUS	V_{in}	–0.3 to 5.5	V
	Other input pins	V_{in}	–0.3- to 3.3-V power supply (PV_{CC}, AV_{CC}, $USBAPV_{CC}$, $USBDPV_{CC}$) +0.3	V
Operating temperature		T_{opr}	–40 to +85	°C
Storage temperature		T_{stg}	–55 to +125	°C

Caution: Permanent damage to the LSI may result if absolute maximum ratings are exceeded.

3.2 Power-On/Power-Off Sequence

The 1.2-V power supply (V_{CC}, PLLVcc, $USBAV_{CC}$, $USBDV_{CC}$, and $USBUV_{CC}$) and 3.3-V power supply (PV_{CC}, AV_{CC}, $USBAPV_{CC}$, and $USBDPV_{CC}$) can be turned on and off in any order.

When turning on the power, be sure to drive both the $\overline{TRST}$ and $\overline{RES}$ pins low; otherwise, the output pins and input/output pins output undefined levels, resulting in system malfunction.

When turning off the power, drive the $\overline{TRST}$ and $\overline{RES}$ pins low if the undefined output may cause a problem.

3.3 DC Characteristics

- Conditions used to obtain DC characteristics (2) in Table 3.2 other than current consumption
  V_{CC} = USBDV_{CC}= USBUV_{CC} = 1.10 to 1.26 V, PV_{CC} = USBDPV_{CC} = 3.0 to 3.6 V, PLLV_{CC} = 1.10 to 1.26 V,
  AV_{CC} = 3.0 to 3.6 V, USBAPV_{CC} = 3.0 to 3.6 V, USBAV_{CC} = 1.10 to 1.26 V,
  V_{SS} = AV_{SS} = USBDV_{SS} = USBAV_{SS} = USBDPV_{SS} = USBAPV_{SS} = USBUV_{SS} = 0 V,
  Ta = –40 to 85 °C

- Conditions used to obtain DC characteristics (2) in Table 3.2 for current consumption
  V_{CC} = USBDV_{CC} = USBUV_{CC} = 1.18 V, PV_{CC} = USBDPV_{CC} = 3.3 V, PLLV_{CC} = 1.18 V, AV_{CC} = 3.3 V,
  USBAPV_{CC} = 3.3 V, USBAV_{CC} = 1.18 V,
  V_{SS} = AV_{SS} = USBDV_{SS} = USBAV_{SS} = USBDPV_{SS} = USBAPV_{SS} = USBUV_{SS} = 0 V, AVref = 3.3 V, VBUS = 5.0 V,
  Ta = –40 to 85 °C
  Iϕ = 400.00 MHz, Bϕ = 133.33 MHz, P1ϕ = 66.67 MHz, P0ϕ = 33.33 MHz

Note: Products in BGA packages do not have USBDV_{CC}, USBUV_{CC}, USBDPV_{CC}, USBDV_{SS}, USBAV_{SS}, USBDPV_{SS}, USBAPV_{SS}, and USBUV_{SS} pins.

Table 3.2 DC Characteristics (1) [Common Items]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Power supply voltage		PV_{CC}	3.0	3.3	3.6	V	
		V_{CC}	1.10	1.18	1.26	V	
PLL power supply voltage		PLLV_{CC}	1.10	1.18	1.26	V	
Analog power supply voltage		AV_{CC}	3.0	3.3	3.6	V	
USB power supply voltage Note: Products in BGA packages do not have USBDPVcc, USBDVcc, and USBUVcc pins.		USBAPV_{CC} USBDPV_{CC}	3.0	3.3	3.6	V	
		USBAV_{CC} USBDV_{CC} USBUV_{CC}	1.10	1.18	1.26	V	
Input leakage current	All input pins	$\|I_{in}\|$	—	—	1.0	µA	V_{in} = 0.5 to PV_{CC} – 0.5 V
Three-state leakage current	All input/output pins, all output pins (except P1_0 to P1_7) (off state)	$\|I_{STI}\|$	—	—	1.0	µA	V_{in} = 0.5 to PV_{CC} – 0.5 V
	P1_0 to P1_7		—	—	10	µA	
Input capacitance	all input/output pins, all input pins	Cin	—	—	10	pF	

Table 3.2 DC Characteristics (2) [Current Consumption]

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in normal operation		V_{CC}	I_{CC}	—	492	mA	
		$PLLV_{CC}$	$PLLI_{CC}$	—	8	mA	
		PV_{CC}	PI_{CC}	70*1*2	—	mA	
		AV_{CC}	AI_{CC}	—	4	mA	During A/D conversion
		AVref	AIref	—	1	mA	During A/D conversion
		$USBAV_{CC}$	UAI_{CC}	—	6	mA	When the USB host/function is in use.
		$USBDV_{CC}$ + $USBUV_{CC}$	UDI_{CC}*3	—	20	mA	In USB high-speed operation (2ch)
		$USBAPV_{CC}$	$UAPI_{CC}$	—	4	mA	When the USB host/function is in use.
		$USBDPV_{CC}$	$UDPI_{CC}$*4	70*1*2	—	mA	In USB high-speed operation (2ch)
		VBUS	VI_{CC}	—	10	µA	
Current consumption in sleep mode		V_{CC}	Isleep	—	300	mA	
		For the other power supply, the current consumption is the same as in normal operation.					
Current consumption in software standby mode	Ta > 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$	Isstby	32	120	mA	
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$	PIsstby	20	26	µA	
		VBUS	VIsstby	8	10	µA	
	Ta ≤ 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$	Isstby	13	55	mA	
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$	PIsstby	17	20	µA	
		VBUS	VIsstby	8	10	µA	

Table 3.2 DC Characteristics (2) [Current Consumption]

Item		Power Supply	Symbol	Typ.	Max.	Unit	Test Conditions
Current consumption in deep standby mode	Ta > 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$ + $USBUV_{CC}$	Idstby	27	119	µA	RAM 0 Kbytes retained, RTC_X1 selected
				32	137	µA	RAM 16 Kbytes retained, RTC_X1 selected
				37	155	µA	RAM 32 Kbytes retained, RTC_X1 selected
				42	191	µA	RAM 64 Kbytes retained, RTC_X1 selected
				62	263	µA	RAM 128 Kbytes retained, RTC_X1 selected
				When the EXTAL 13 MHz is selected, 5 µA and 7 µA are added to the "Typ." and "Max." values above, respectively.			
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$	PIdstby	13	15	µA	RTC is not operating
				20	25	µA	RTC_X1 selected
				1	—	mA	EXTAL 13 MHz selected, small gain*1
		VBUS	VIdstby	8	10	µA	
	Ta ≤ 50 °C	V_{CC} + $PLLV_{CC}$ + $USBAV_{CC}$ + $USBDV_{CC}$+ $USBUV_{CC}$	Idstby	17	54	µA	RAM 0 Kbytes retained, RTC_X1 selected
				21	71	µA	RAM 16 Kbytes retained, RTC_X1 selected
				25	88	µA	RAM 32 Kbytes retained, RTC_X1 selected
				33	122	µA	RAM 64 Kbytes retained, RTC_X1 selected
				49	190	µA	RAM 128 Kbytes retained, RTC_X1 selected
				When the EXTAL 13 MHz is selected, 5 µA and 7 µA are added to the "Typ." and "Max." values above, respectively.			
		PV_{CC} + AV_{CC} + AVref + $USBAPV_{CC}$ + $USBDPV_{CC}$	PIdstby	12	13	µA	RTC is not operating
				19	23	µA	RTC_X1 selected
				1	—	mA	EXTAL 13 MHz selected, small gain*1
		VBUS	VIdstby	8	10	µA	

Note 1. Reference value. The actual operating current greatly depends on the system (such as slow rising/falling edges caused by IO load and toggle frequency). Be sure to determine the value using the actual system.
Note 2. The sum of PIcc and UDPIcc must be equal to or lower than 150 mA.
Note 3. In the products in BGA packages, UDIcc is added to Icc.
Note 4. In the products in BGA packages, UDPIcc is added to PIcc.

Table 3.2 DC Characteristics (3) [Except I²C Bus Interface, and USB 2.0 Host/Function Module-Related Pins]

Item		Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage*		V_{IH}	2.2	—	PV_{CC} + 0.3	V	
Input low voltage*		V_{IL}	–0.3	—	0.8	V	
Schmitt trigger input characteristics		VT^+	$PV_{CC} \times 0.665$	—	—	V	
		VT^-	—	—	0.8	V	
		$VT^+ – VT^-$	0.2	—	—	V	
Output high voltage		V_{OH}	PV_{CC} – 0.5	—	—	V	I_{OH} = –2.0 mA
Output low voltage		V_{OL}	—	—	0.4	V	I_{OL} = 2.0 mA
RAM standby voltage	Software standby mode (large-capacity on-chip RAM)	V_{RAMS}	0.85	—	—	V	Measured with V_{CC} as parameter
	Deep standby mode (only the on-chip RAM for data retention)	V_{RAMD}	1.10	—	—	V	

Note: * Values for the input of data for boundary scanning through pins TMS, TCK, JP0_0, JP0_1, P5_0 to P5_15, and P6_0 to P6_15.

Table 3.2 DC Characteristics (4) [I²C Bus Interface Related Pins*]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	$PV_{CC} \times 0.7$	—	PV_{CC} + 0.3	V	
Input low voltage	V_{IL}	–0.3	—	$PV_{CC} \times 0.3$	V	
Schmitt trigger input characteristics	$V_{IH} – V_{IL}$	$PV_{CC} \times 0.05$	—	—	V	
Output low voltage	V_{OL}	—	—	0.4	V	I_{OL} = 3.0 mA

Note: * The P1_0 to P1_7 pins are open-drain pins.

Table 3.2 DC Characteristics (5) [USB 2.0 Host/Function Module-Related Pins*]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Reference resistance	R_{REF}	5.6 kΩ ± 1%	5.6 kΩ ± 1%	5.6 kΩ ± 1%		
Input high voltage (VBUS1, VBUS0)	V_{IH}	4.02	—	5.25	V	
Input low voltage (VBUS1, VBUS0)	V_{IL}	–0.3	—	0.5	V	
Input high voltage (USB_X1)	V_{IH}	PV_{CC} – 0.5	—	PV_{CC} + 0.3	V	
Input low voltage (USB_X1)	V_{IL}	–0.3	—	0.5	V	

Note: * REFRIN, VBUS1, VBUS0, USB_X1, and USB_X2 pins

Table 3.2 DC Characteristics (6) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed, Full-Speed, and High-Speed Common Items)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
DP pull-up resistance (when function is selected)	R_{pu}	0.900	—	1.575	kΩ	In idle mode
		1.425	—	3.090	kΩ	In transmit/receive mode
DP and DM pull-down resistance (when host is selected)	R_{pd}	14.25	—	24.80	kΩ	

Note: * DP1, DP0, DM1, and DM pins

Table 3.2 DC Characteristics (7) [USB 2.0 Host/Function Module-Related Pins* (Low-Speed and Full-Speed)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Input high voltage	V_{IH}	2.0	—	—	V	
Input low voltage	V_{IL}	—	—	0.8	V	
Differential input sensitivity	V_{DI}	0.2	—	—	V	| (DP) – (DM) |
Differential common mode range	V_{CM}	0.8	—	2.5	V	
Output high voltage	V_{OH}	2.8	—	3.6	V	I_{OH} = –200 μA
Output low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
Output signal crossover voltage	V_{CRS}	1.3	—	2.0	V	C_L = 50 pF (full-speed) C_L = 200 to 600 pF (low-speed)

Note: * DP1, DP0, DM1, and DM pins

Table 3.2 DC Characteristics (8) [USB 2.0 Host/Function Module-Related Pins* (High-Speed)]

Item	Symbol	Min.	Typ.	Max.	Unit	Test Conditions
Squelch detection threshold voltage (differential voltage)	V_{HSSQ}	100	—	150	mV	
Common mode voltage range	V_{HSCM}	–50	—	500	mV	
Idle state	V_{HSOI}	–10.0	—	10.0	mV	
Output high voltage	V_{HSOH}	360	—	440	mV	
Output low voltage	V_{HSOL}	–10.0	—	10.0	mV	
Chirp J output voltage (difference)	V_{CHIRPJ}	700	—	1100	mV	
Chirp K output voltage (difference)	V_{CHIRPK}	–900	—	–500	mV	

Note: * DP1, DP0, DM1, and DM pins

Table 3.3 Permissible Output Currents

Item		Symbol	Min.	Typ.	Max.	Unit
Permissible output low current (per pin)	P1_0 to P1_7	I_{OL}	—	—	10	mA
	Output pins other than above		—		2	mA
Permissible output high current (per pin)		$-I_{OH}$	—	—	2	mA
Permissible output current (total)		ΣI_O	—	—	150	mA

Caution: To protect the LSI's reliability, do not exceed the output current values in Table 3.3.

3.4 AC Characteristics

Signals input to this LSI are basically handled as signals in synchronization with a clock. The setup and hold times for input pins must be followed.

Conditions for AC characteristics: V_{CC} = $USBDV_{CC}$ = $USBUV_{CC}$ = 1.10 to 1.26 V, PV_{CC} = $USBDPV_{CC}$ = 3.0 to 3.6 V, $PLLV_{CC}$ = 1.10 to 1.26 V, AV_{CC} = 3.0 to 3.6 V, $USBAPV_{CC}$ = 3.0 to 3.6 V, $USBAV_{CC}$ = 1.10 to 1.26 V, V_{SS} = AV_{SS} = $USBDV_{SS}$ = $USBAV_{SS}$ = $USBDPV_{SS}$ = $USBAPV_{SS}$ = $USBUV_{SS}$ = 0 V, Ta = –40 to 85 °C

Note: Products in BGA packages do not have $USBDV_{CC}$, $USBUV_{CC}$, $USBDPV_{CC}$, $USBDV_{SS}$, $USBAV_{SS}$, $USBDPV_{SS}$, $USBAPV_{SS}$, and $USBUV_{SS}$ pins.

Table 3.4 Operating Frequency

Item		Symbol	Min.	Max.	Unit	Remarks
Operating frequency	CPU clock (Iϕ)	f	100.00	400.00	MHz	
	Internal bus clock (Bϕ)		100.00	133.33	MHz	
	Peripheral clock 1 (P1ϕ)		50.00	66.67	MHz	
	Peripheral clock 0 (P0ϕ)		25.00	33.33	MHz	

3.4.1 Clock Timing

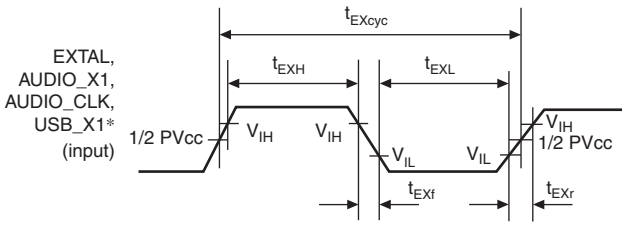
Table 3.5 Clock Timing

Item	Symbol	Min.	Max.	Unit	Figure
EXTAL clock input frequency (when the clock is supplied to USB 2.0 host/function module)	f_{EX}	12MHz ± 100ppm			Figure 3.1
EXTAL clock input frequency (when the clock isn't supplied to USB 2.0 host/function module)		10.00	13.33	MHz	
EXTAL clock input cycle time (when the clock isn't supplied to USB 2.0 host/function module)	t_{EXcyc}	75.00	100.00	ns	
AUDIO_X1 clock input frequency (crystal resonator connected)	f_{EX}	10.00	50.00	MHz	
AUDIO_X1 clock input cycle time (crystal resonator connected)	t_{EXcyc}	20.00	100.00	ns	
AUDIO_X1, AUDIO_CLK clock input frequency (external clock input)	f_{EX}	1.00	50.00	MHz	
AUDIO_X1, AUDIO_CLK clock input cycle time (external clock input)	t_{EXcyc}	20.00	1000.00	ns	
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module and high-speed transfer function is used)	f_{EX}	48 MHz ±100 ppm			
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module, high-speed transfer function is not used, and host controller function is used)		48 MHz ±500 ppm			
USB_X1 clock input frequency (when the 48-MHz clock is supplied to USB 2.0 host/function module, high-speed transfer function is not used, and host controller function is not used)		48 MHz ±2500 ppm			
EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input low pulse width	t_{EXL}	0.4	0.6	t_{EXcyc}	
EXTAL, AUDIO_X1, AUDIO_CLK, USB_X1 clock input high pulse width	t_{EXH}	0.4	0.6	t_{EXcyc}	

Table 3.5 Clock Timing

Item	Symbol	Min.	Max.	Unit	Figure
EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input rise time	t_{EXr}	—	4	ns	Figure 3.1
EXTAL, AUDIO_X1, AUDIO_CLK, USB_ X1 clock input fall time	t_{EXf}	—	4	ns	
CKIO clock output frequency	f_{OP}	50.00	66.67	MHz	
CKIO clock output cycle time	t_{cyc}	15.00	20.00	ns	Figure 3.2 (1) and Figure 3.2 (2)
CKIO clock output low pulse width 1	t_{CKOL1}	$t_{cyc}/2 - t_{CKOr1}$	—	ns	Figure 3.2 (1)
CKIO clock output high pulse width 1	t_{CKOH1}	$t_{cyc}/2 - t_{CKOr1}$	—	ns	
CKIO clock output rise time 1	t_{CKOr1}	—	3	ns	
CKIO clock output fall time 1	t_{CKOf1}	—	3	ns	
CKIO clock output low pulse width 2	t_{CKOL2}	$t_{cyc}/2 - t_{CKOr2}$	—	ns	Figure 3.2 (2)
CKIO clock output high pulse width 2	t_{CKOH2}	$t_{cyc}/2 - t_{CKOr2}$	—	ns	
CKIO clock output rise time 2	t_{CKOr2}	—	2	ns	
CKIO clock output fall time 2	t_{CKOf2}	—	2	ns	
On-chip PLL circuit oscillation settling time	t_{POSC}	1	—	ms	Figure 3.3 and Figure 3.5 (1)
On-chip oscillation circuit oscillation settling time (RTC_X1)	t_{ROSC}	—	3*	s	Figure 3.6
On-chip oscillation circuit oscillation settling time (other than above)		—	4*	ms	Figure 3.3, Figure 3.5 (1), and Figure 3.6
Mode hold time	t_{MDH}	200	—	ns	Figure 3.3 and Figure 3.5 (1)
SSCG stabilizing time	t_{SSCG}	1	—	us	Figure 3.4

Note: * Settings for values smaller than the above specifications may be possible, as long as the values are confirmed through evaluation by the manufacturer of the oscillator.



Note: * When the clock is input on the EXTAL, AUDIO_X1, AUDIO_CLK, or USB_X1

Figure 3.1 EXTAL, AUDIO_X1, AUDIO_CLK, and USB_X1 Clock Input Timing

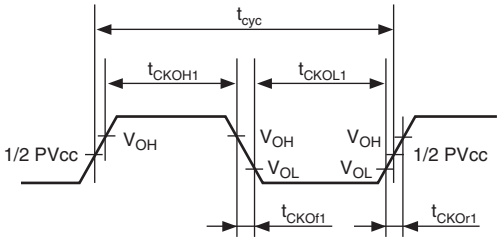


Figure 3.2 (1) CKIO Clock Output Timing 1

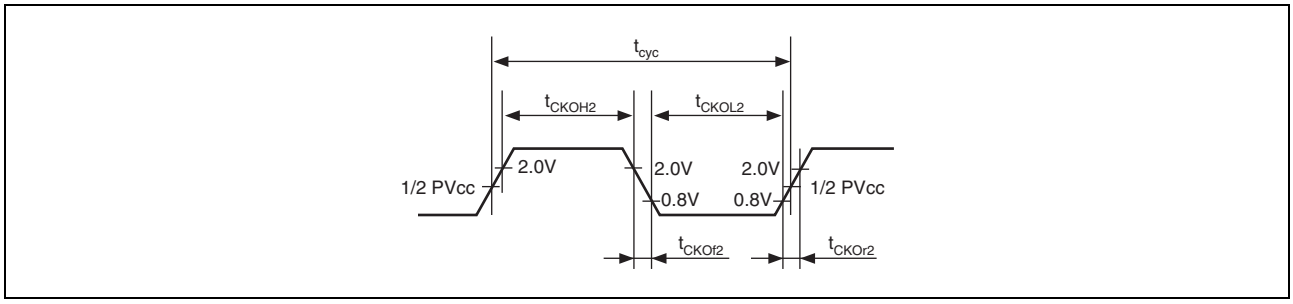


Figure 3.2 (2) CKIO Clock Output Timing 2

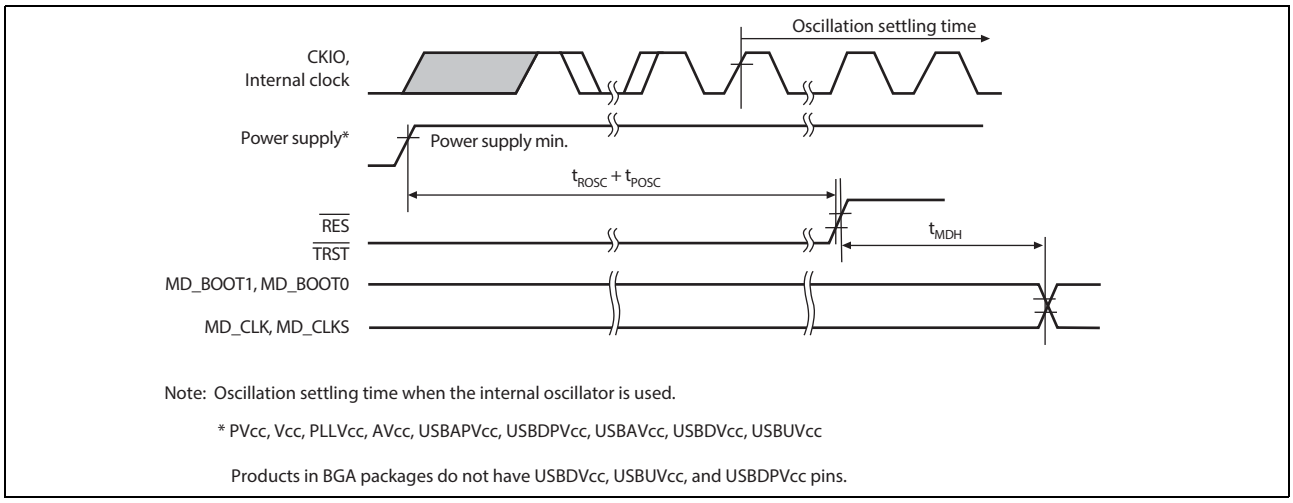


Figure 3.3 Power-On Oscillation Settling Time

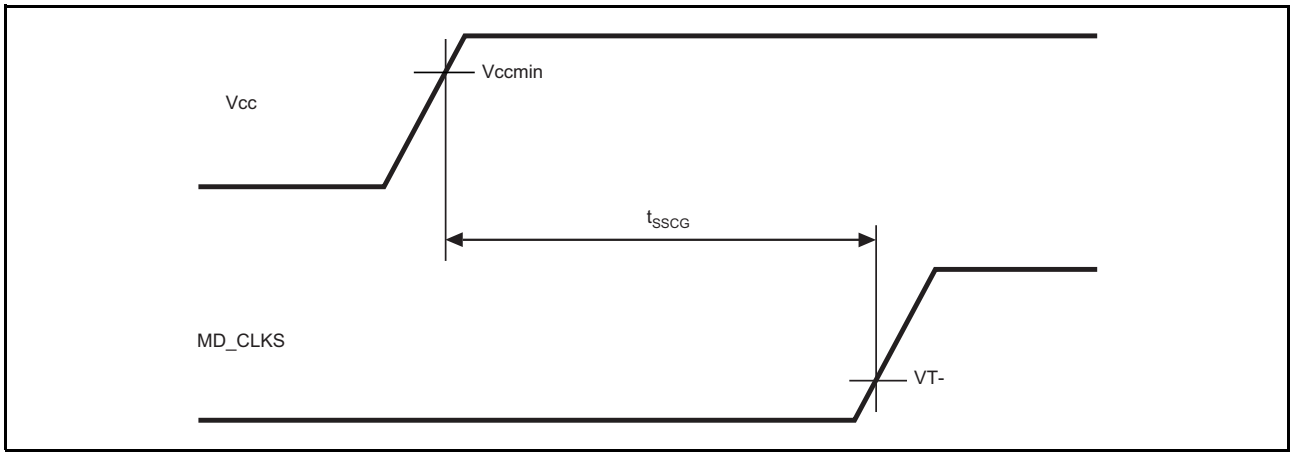


Figure 3.4 SSCG Stabilizing Time

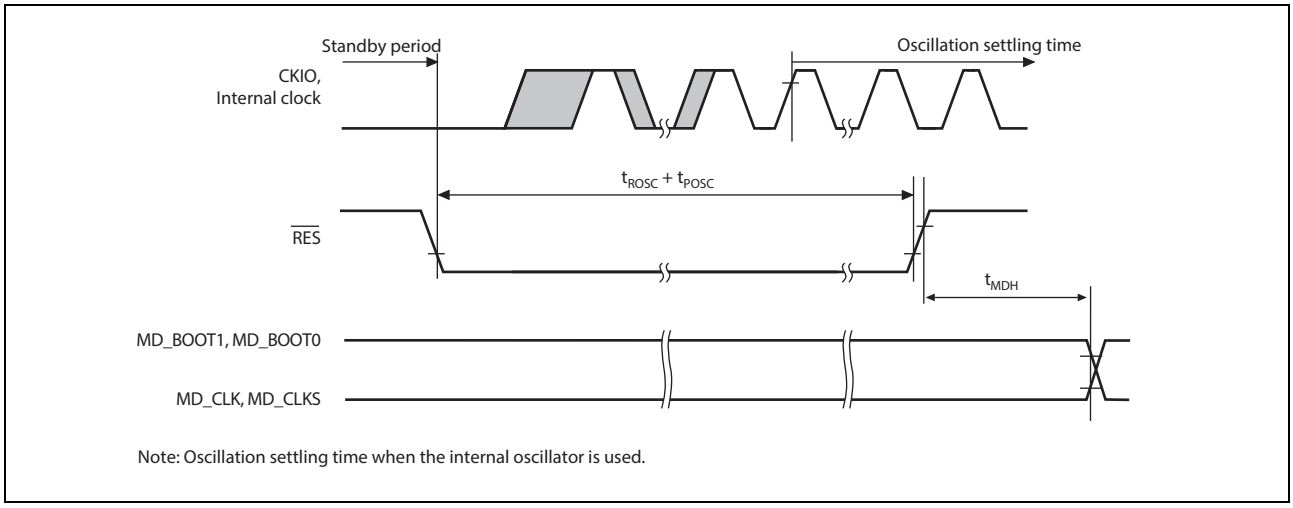


Figure 3.5 (1) Oscillation Stabilizing Time on Return from Standby (Return by Reset)

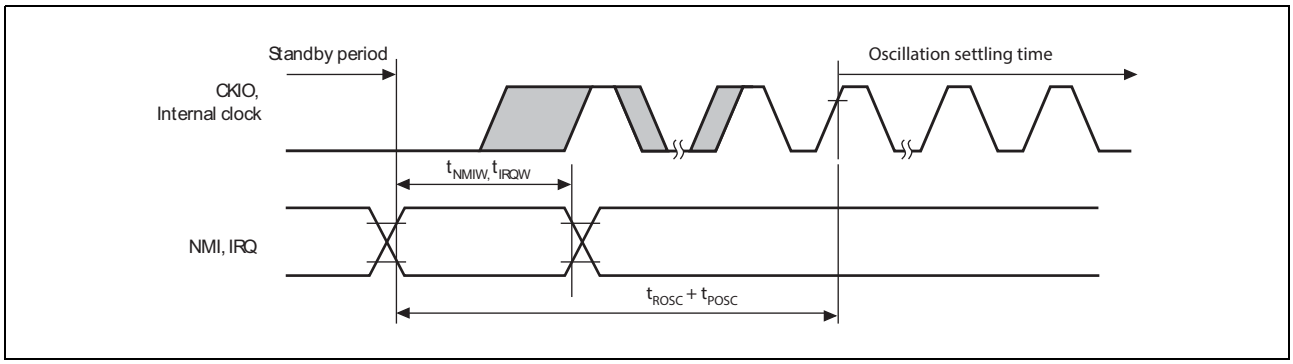


Figure 3.5 (2) Oscillation Stabilizing Time on Return from Standby (Return by NMI or IRQ)

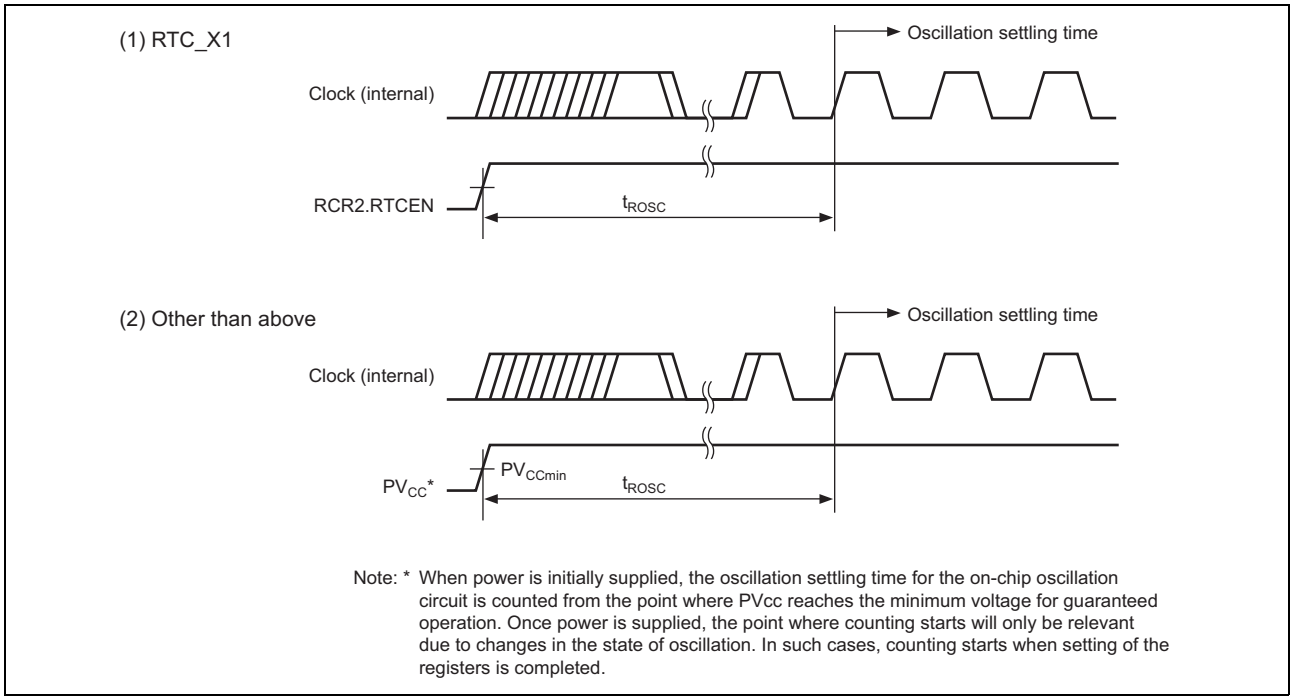


Figure 3.6 On-chip Oscillation Circuit Oscillation Stabilizing Time

3.4.2 Control Signal Timing

Table 3.6 Control Signal Timing

Item		Symbol	Min.	Max.	Unit	Figure
$\overline{\text{RES}}$ pulse width	Exit from standby mode	t_{RESW}	t_{ROSC} + t_{POSC}		ms	Figure 3.7 (1) and Figure 3.5 (1)
	Other than above		20	—	t_{cyc}	
$\overline{\text{TRST}}$ pulse width		t_{TRSW}	20	—	t_{cyc}	
NMI pulse width		t_{NMIW}	20	—	t_{cyc}	Figure 3.7 (2) and Figure 3.5 (2)
IRQ pulse width		t_{IRQW}	20	—	t_{cyc}	
TINT pulse width		t_{TINTW}	20	—	t_{cyc}	
$\overline{\text{RES}}$ input rise time*1		t_{RSr}	—	500	µs	Figure 3.7 (3)
$\overline{\text{RES}}$ negating hold time*2		t_{RSNH}	0	—	ns	Figure 3.7 (4)

Note 1. Make sure that this specification is satisfied when the same signal is controlling the $\overline{\text{TRST}}$ and $\overline{\text{RES}}$ pins.
Note 2. Make sure that this specification is satisfied when different signals are controlling the $\overline{\text{TRST}}$ and $\overline{\text{RES}}$ pins.

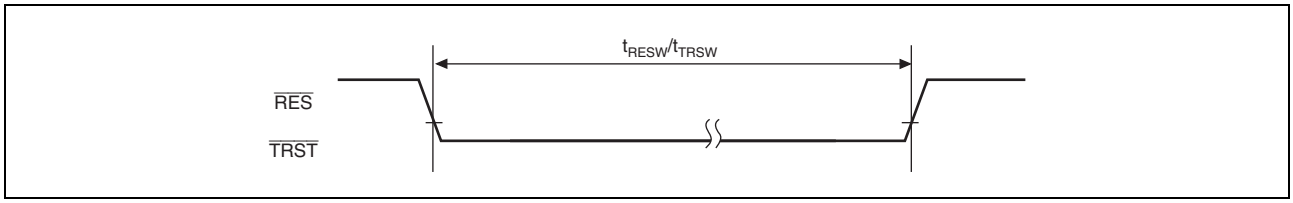


Figure 3.7 (1) Reset Input Timing 1

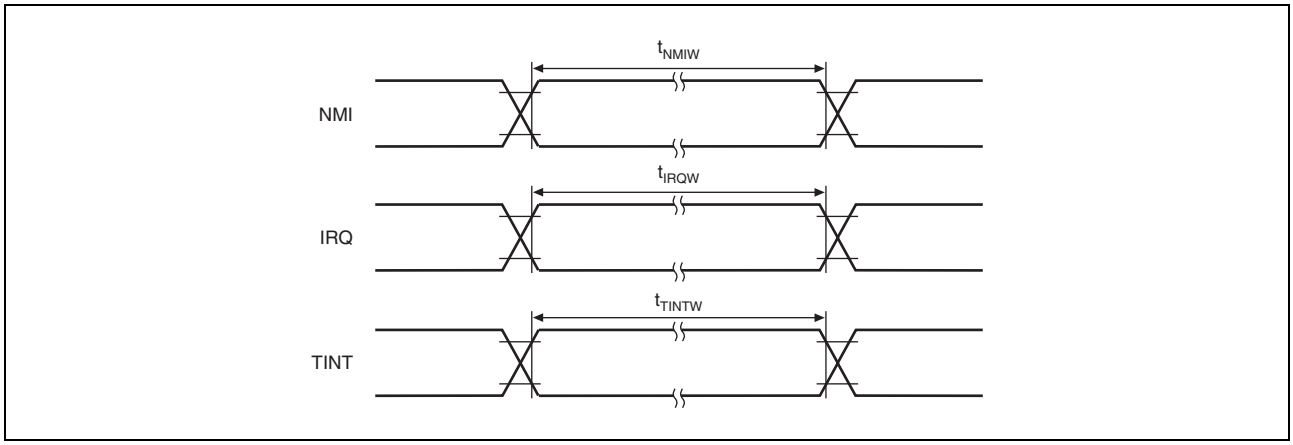


Figure 3.7 (2) Interrupt Signal Input Timing

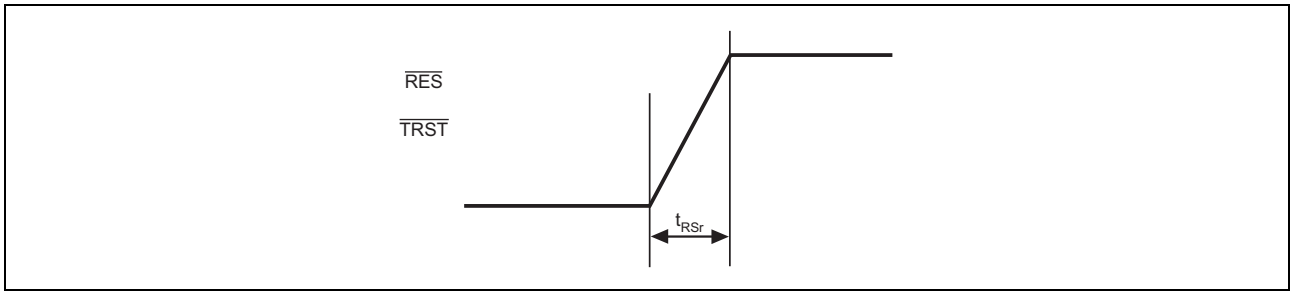


Figure 3.7 (3) Reset Input Timing 2

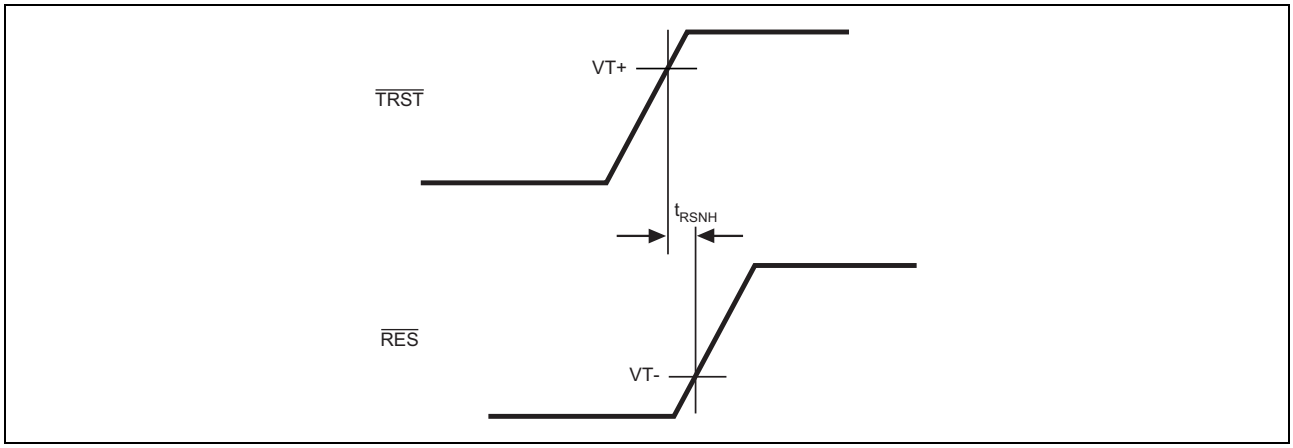


Figure 3.7 (4) Reset Input Timing 3

3.4.3 Bus Timing

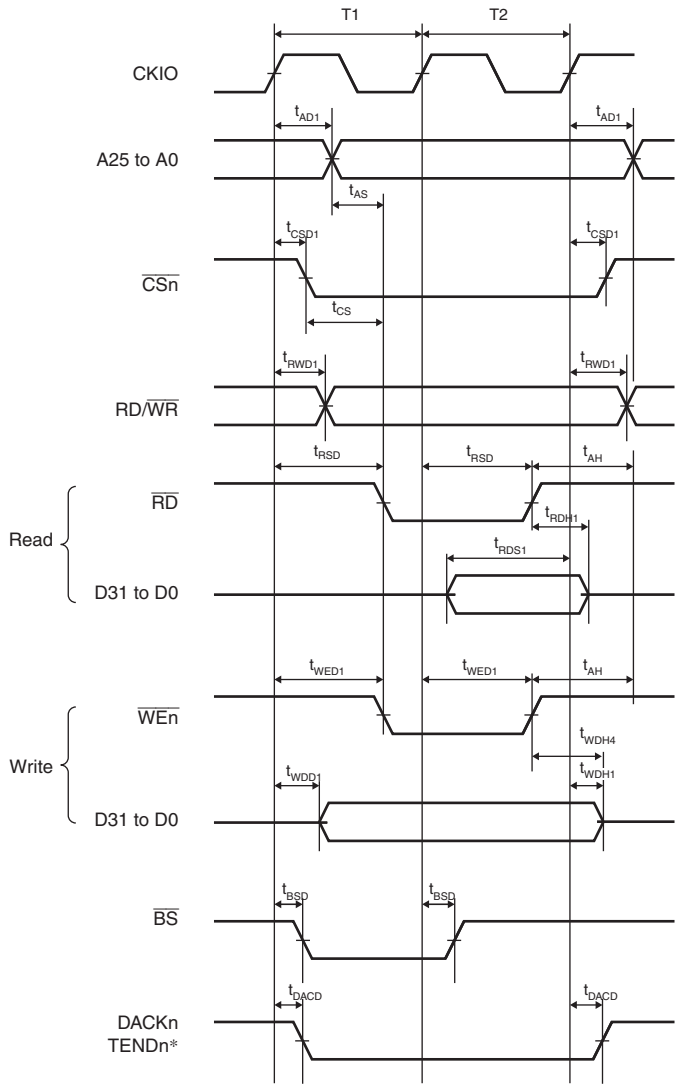
Table 3.7 Bus Timing

		CKIO = 66.67 MHz*1			
Item	**Symbol**	**Min.**	**Max.**	**Unit**	**Figure**
Address delay time 1	t_{AD1}	0/2*3	12	ns	Figure 3.8 to Figure 3.32
Address delay time 2	t_{AD2}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 12	ns	Figure 3.15
Address setup time	t_{AS}	0	—	ns	Figure 3.8 to Figure 3.11, Figure 3.15
Chip enable setup time	t_{CS}	0	—	ns	Figure 3.8 to Figure 3.11, Figure 3.15
Address hold time	t_{AH}	0	—	ns	Figure 3.8 to Figure 3.11
$\overline{BS}$ delay time	t_{BSD}	—	12	ns	Figure 3.8 to Figure 3.29
$\overline{CS}$ delay time 1	t_{CSD1}	0/2*3	12	ns	Figure 3.8 to Figure 3.32
Read write delay time 1	t_{RWD1}	0/2*3	12	ns	Figure 3.8 to Figure 3.32
Read strobe delay time	t_{RSD}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 12	ns	Figure 3.8 to Figure 3.15
Read data setup time 1	t_{RDS1}	$1/2t_{cyc}$+ 5	—	ns	Figure 3.8 to Figure 3.14
Read data setup time 2	t_{RDS2}	7	—	ns	Figure 3.16 to Figure 3.19, Figure 3.24 to Figure 3.26
Read data setup time 3	t_{RDS3}	$1/2t_{cyc}$ + 5	—	ns	Figure 3.15
Read data hold time 1	t_{RDH1}	0	—	ns	Figure 3.8 to Figure 3.14
Read data hold time 2	t_{RDH2}	2	—	ns	Figure 3.16 to Figure 3.19, Figure 3.24 to Figure 3.26
Read data hold time 3	t_{RDH3}	0	—	ns	Figure 3.15
Write enable delay time 1	t_{WED1}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 12	ns	Figure 3.8 to Figure 3.13
Write enable delay time 2	t_{WED2}	—	12	ns	Figure 3.14
Write data delay time 1	t_{WDD1}	—	12	ns	Figure 3.8 to Figure 3.14
Write data delay time 2	t_{WDD2}	—	12	ns	Figure 3.20 to Figure 3.23, Figure 3.27 to Figure 3.29
Write data hold time 1	t_{WDH1}	1	—	ns	Figure 3.8 to Figure 3.14
Write data hold time 2	t_{WDH2}	2	—	ns	Figure 3.20 to Figure 3.23, Figure 3.27 to Figure 3.29
Write data hold time 4	t_{WDH4}	0	—	ns	Figure 3.8 to Figure 3.12
$\overline{WAIT}$ setup time	t_{WTS}	$1/2t_{cyc}$ + 4.5	—	ns	Figure 3.9 to Figure 3.15
$\overline{WAIT}$ hold time	t_{WTH}	$1/2t_{cyc}$ + 3.5	—	ns	Figure 3.9 to Figure 3.15
$\overline{RAS}$ delay time 1	t_{RASD1}	2	12	ns	Figure 3.16 to Figure 3.32
$\overline{CAS}$ delay time 1	t_{CASD1}	2	12	ns	Figure 3.16 to Figure 3.32
DQM delay time 1	t_{DQMD1}	2	12	ns	Figure 3.16 to Figure 3.29
CKE delay time 1	t_{CKED1}	2	12	ns	Figure 3.31
$\overline{AH}$ delay time	t_{AHD}	$1/2t_{cyc}$	$1/2t_{cyc}$ + 12	ns	Figure 3.12
Multiplexed address delay time	t_{MAD}	—	12	ns	Figure 3.12
Multiplexed address hold time	t_{MAH}	1	—	ns	Figure 3.12
Address setup time for $\overline{AH}$	t_{AVVH}	$1/2t_{cyc}$ – 2	—	ns	Figure 3.12
DACK, TEND delay time	t_{DACD}	Refer to the direct memory access controller timing		ns	Figure 3.8 to Figure 3.29

Note 1. The maximum value (fmax) of CKIO (external bus clock) depends on the number of wait cycles and the system configuration of your board.

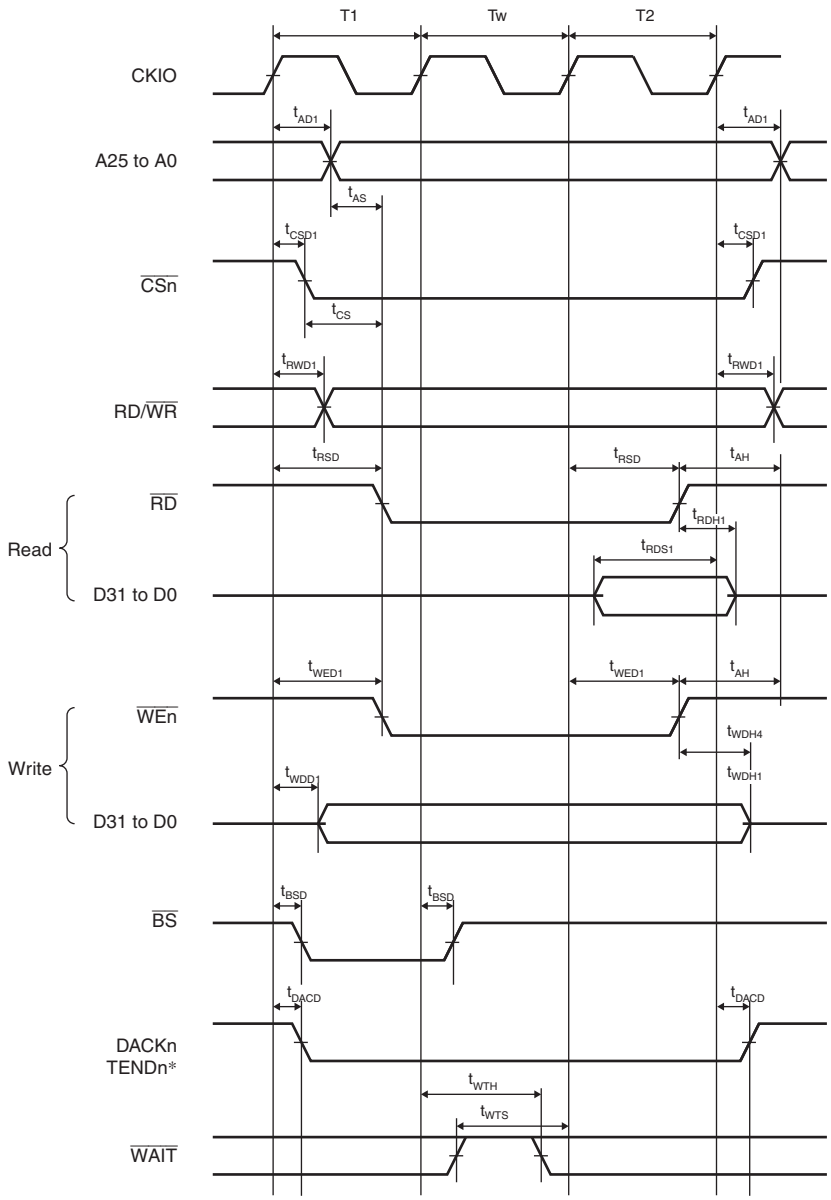
Note 2. 1/2 t_{cyc} indicated in minimum and maximum values for the item of delay, setup, and hold times represents a half cycle from the rising edge with a clock. That is, 1/2 t_{cyc} describes a reference of the falling edge with a clock.

Note 3. Values when SDRAM is used.



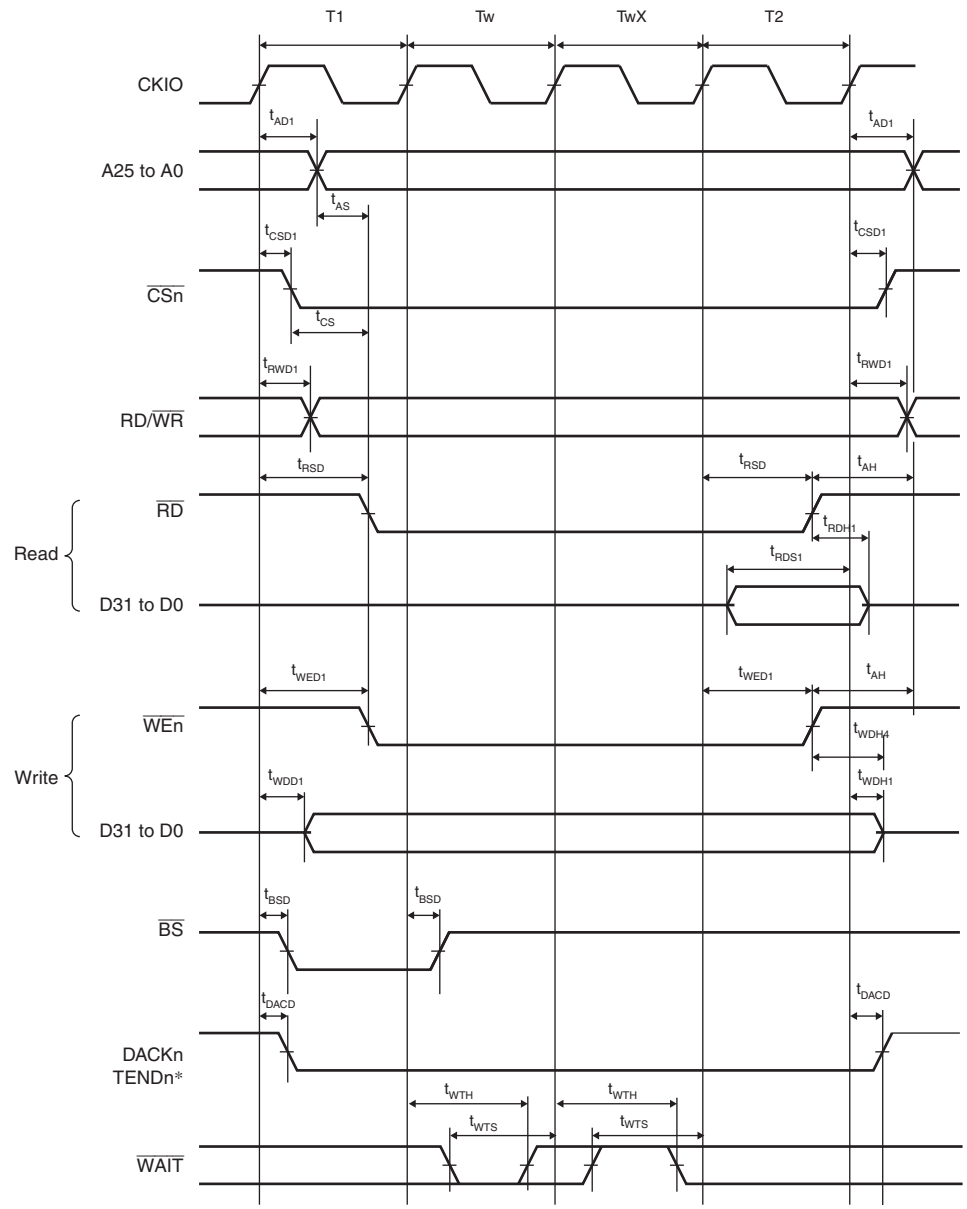
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.8 Basic Bus Timing for Normal Space (No Wait)



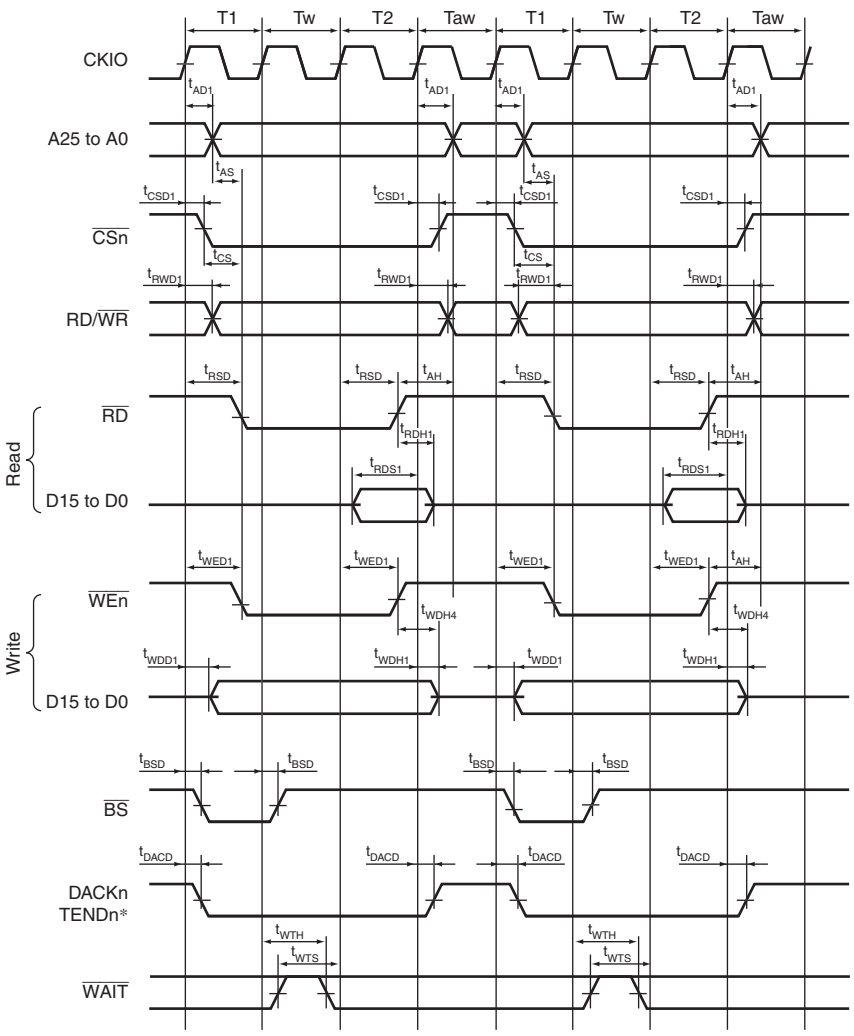
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.9 Basic Bus Timing for Normal Space (One Software Wait Cycle)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.10 Basic Bus Timing for Normal Space (One Software Wait Cycle, One External Wait Cycle)



Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.11 Basic Bus Timing for Normal Space (One Software Wait Cycle, External Wait Cycle Valid (WM Bit = 0), No Idle Cycle)

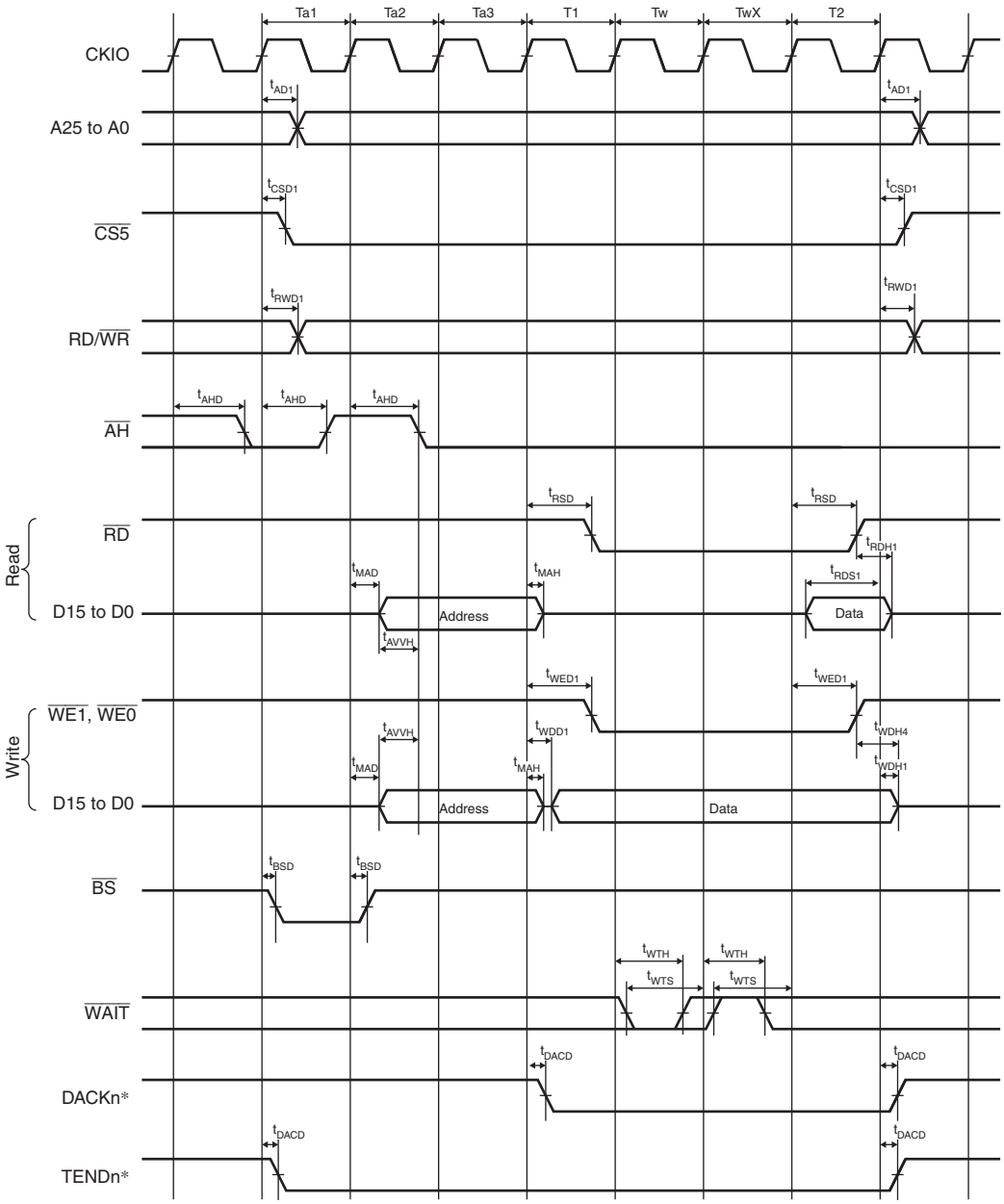


Figure 3.12 MPX-I/O Interface Bus Cycle (Three Address Cycles, One Software Wait Cycle, One External Wait Cycle)

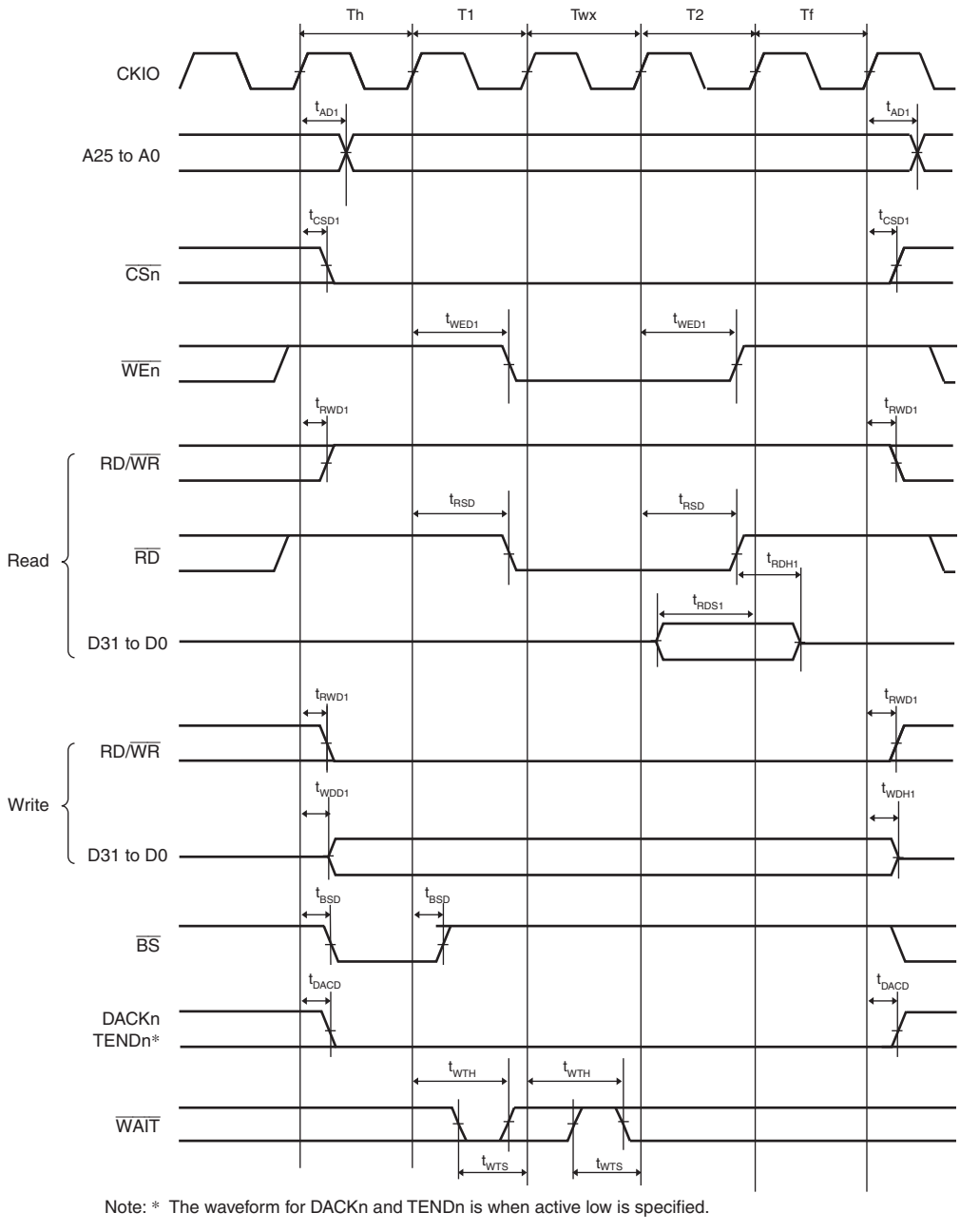


Figure 3.13 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 0 (Write Cycle $\overline{UB}$/$\overline{LB}$ Control))

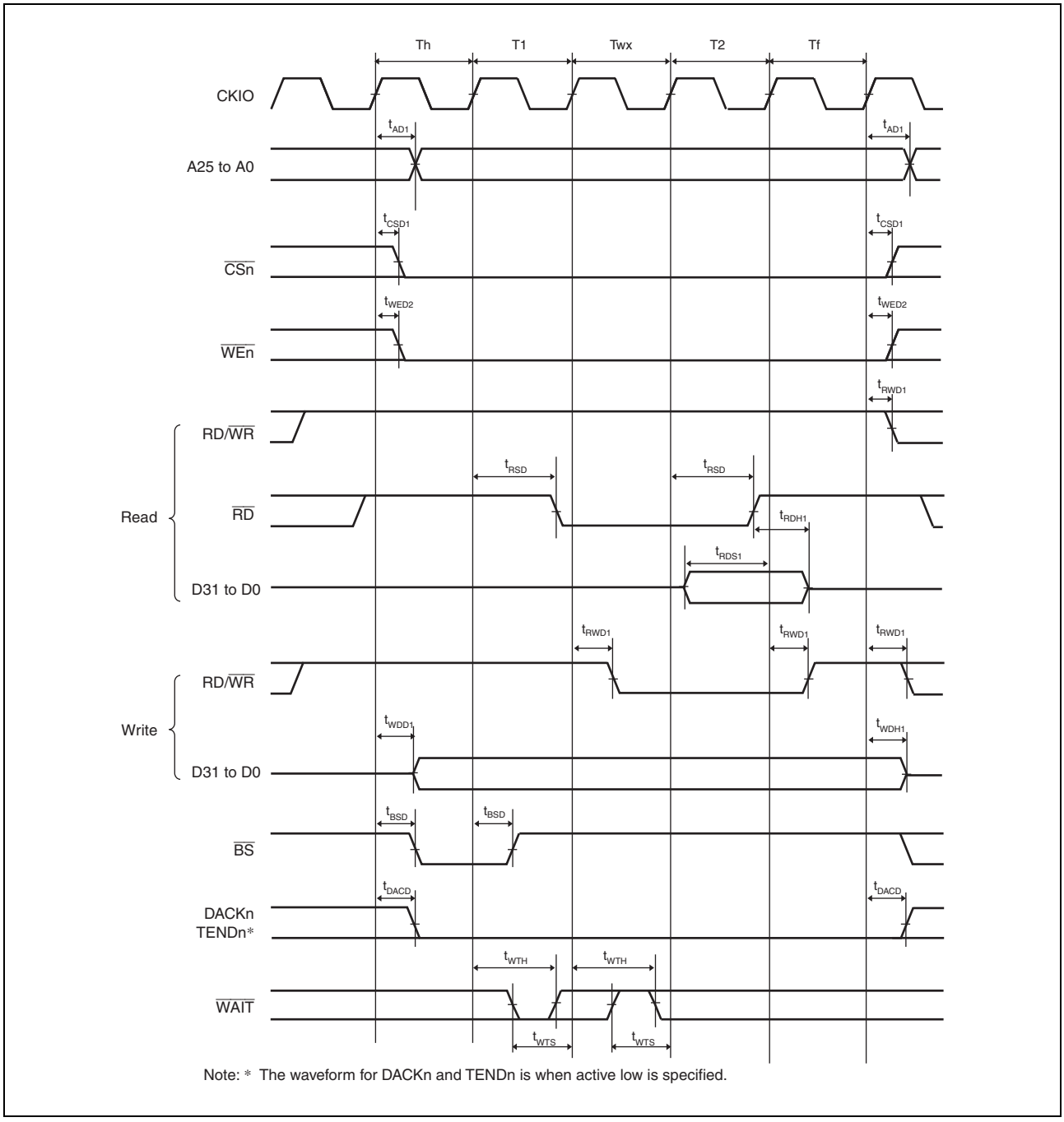
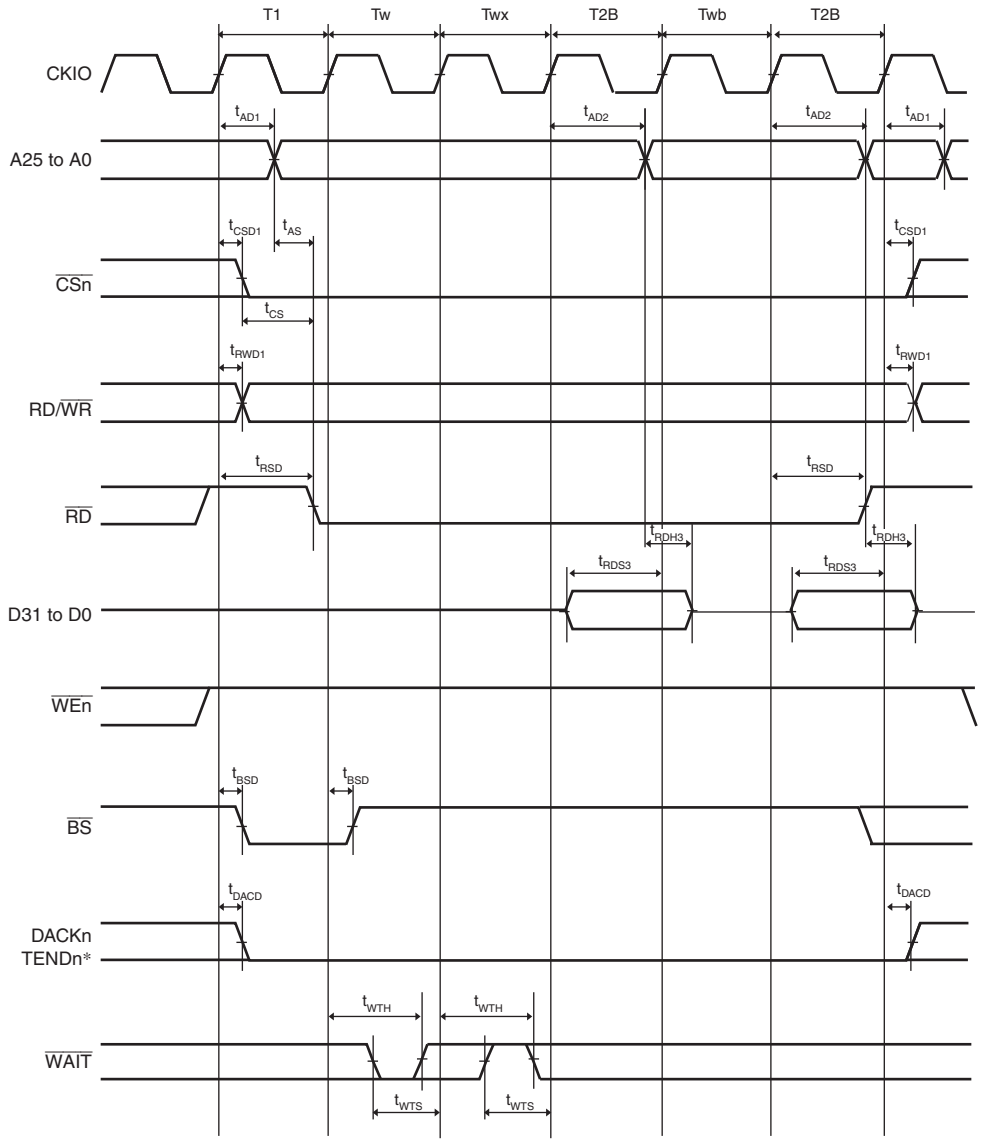
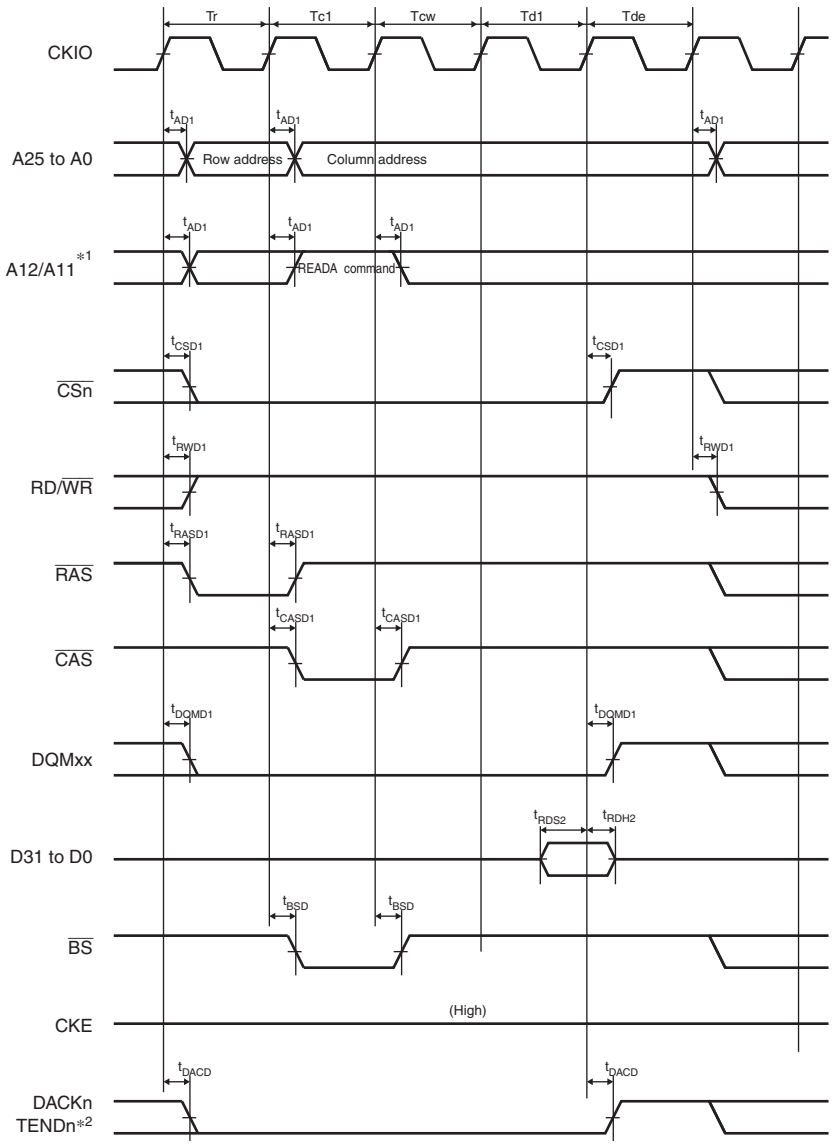


Figure 3.14 Bus Cycle of SRAM with Byte Selection (SW = 1 Cycle, HW = 1 Cycle, One Asynchronous External Wait Cycle, BAS = 1 (Write Cycle $\overline{WE}$ Control))



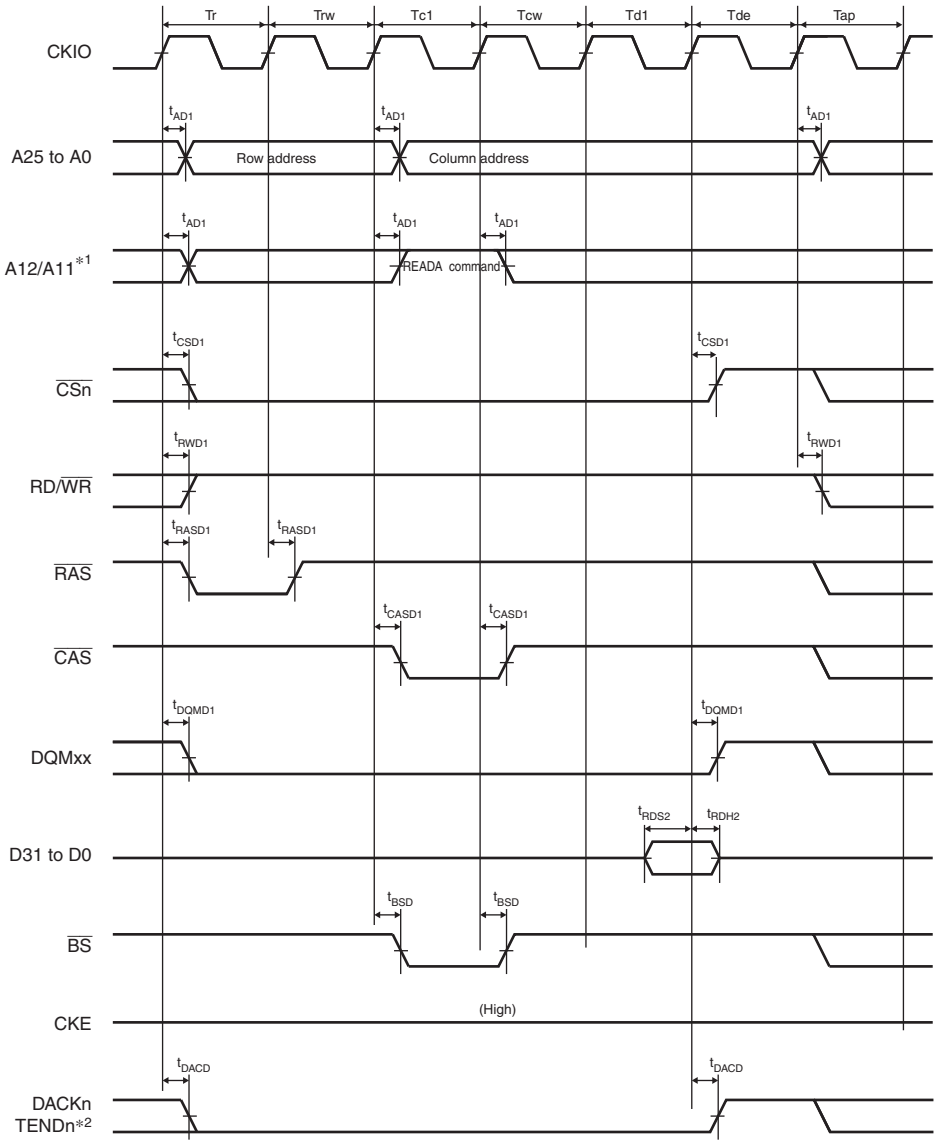
Note: * The waveform for DACKn and TENDn is when active low is specified.

Figure 3.15 Burst ROM Read Cycle (One Software Wait Cycle, One Asynchronous External Burst Wait Cycle, Two Burst)



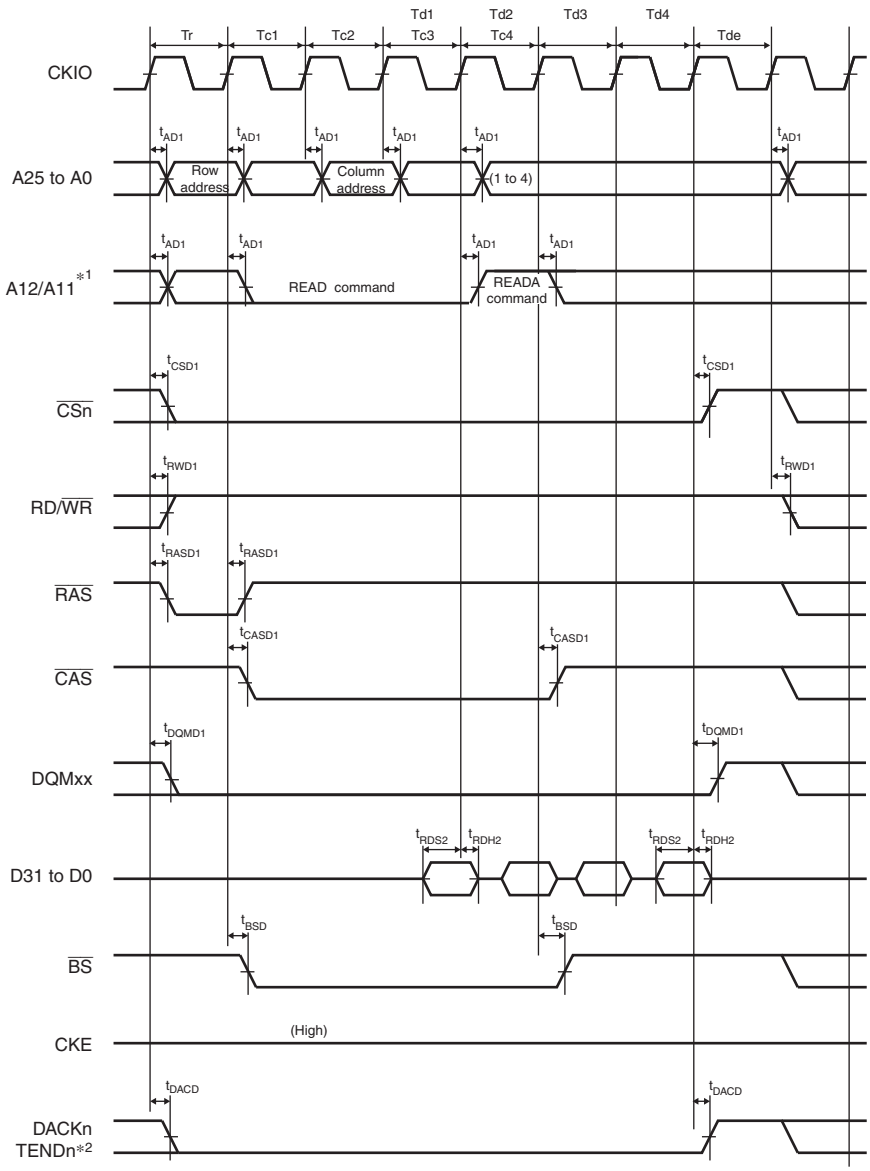
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.16 Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 0 Cycle)



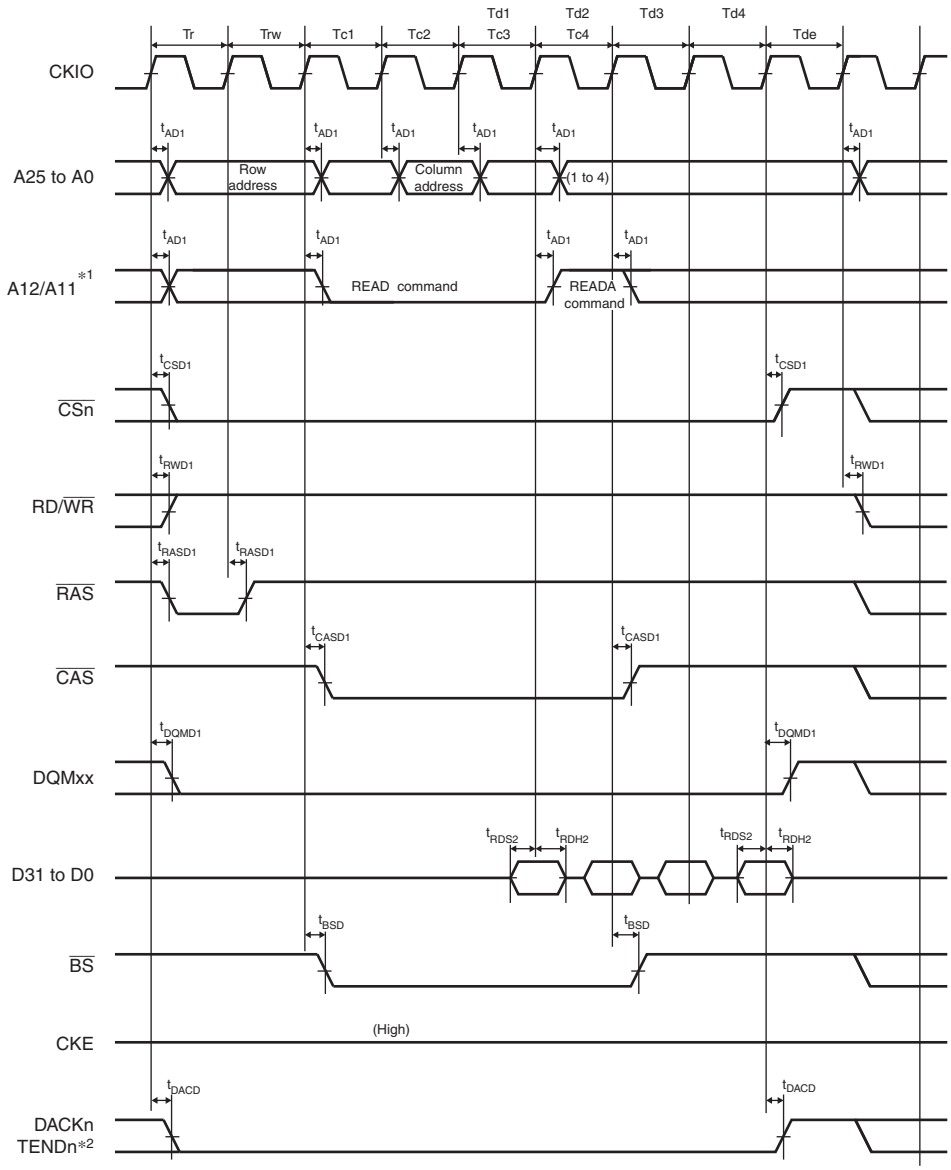
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.17 Synchronous DRAM Single Read Bus Cycle (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 1 Cycle)



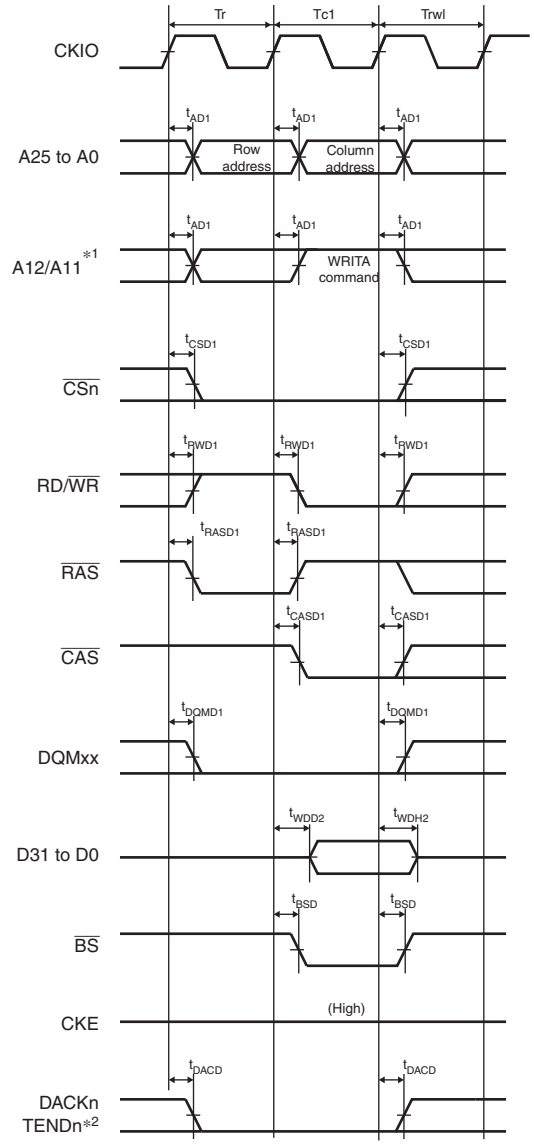
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.18 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 0 Cycle, WTRP = 1 Cycle)



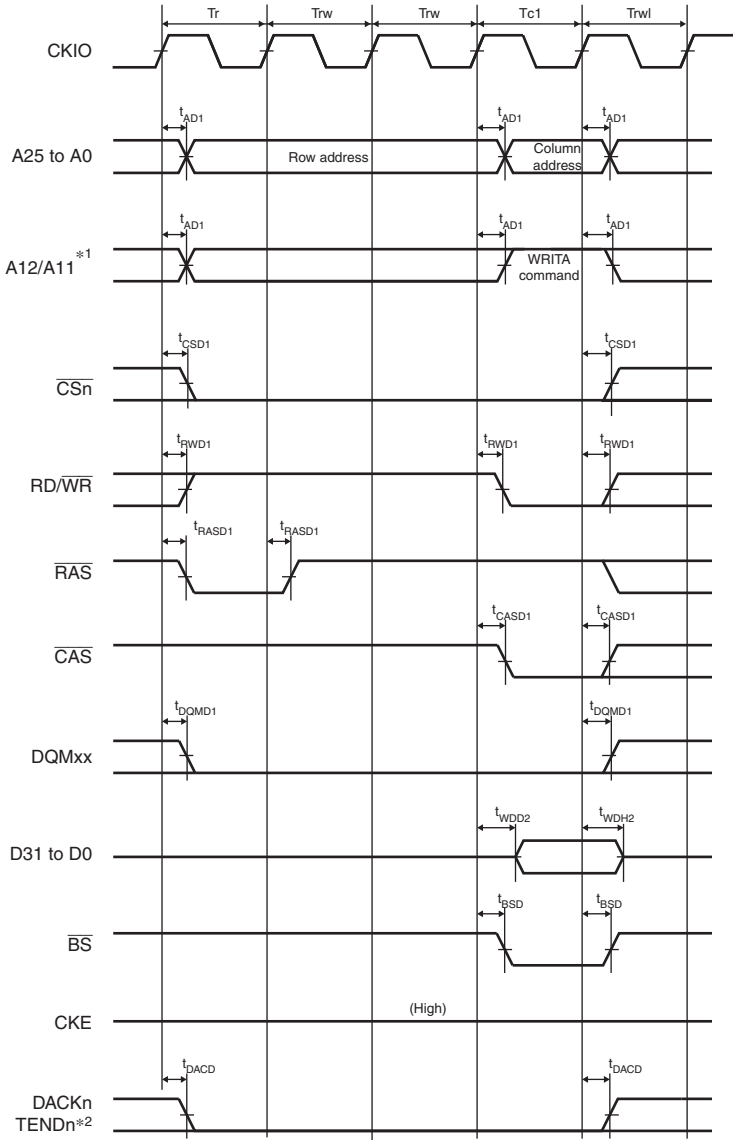
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.19 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Auto Precharge, CAS Latency 2, WTRCD = 1 Cycle, WTRP = 0 Cycle)



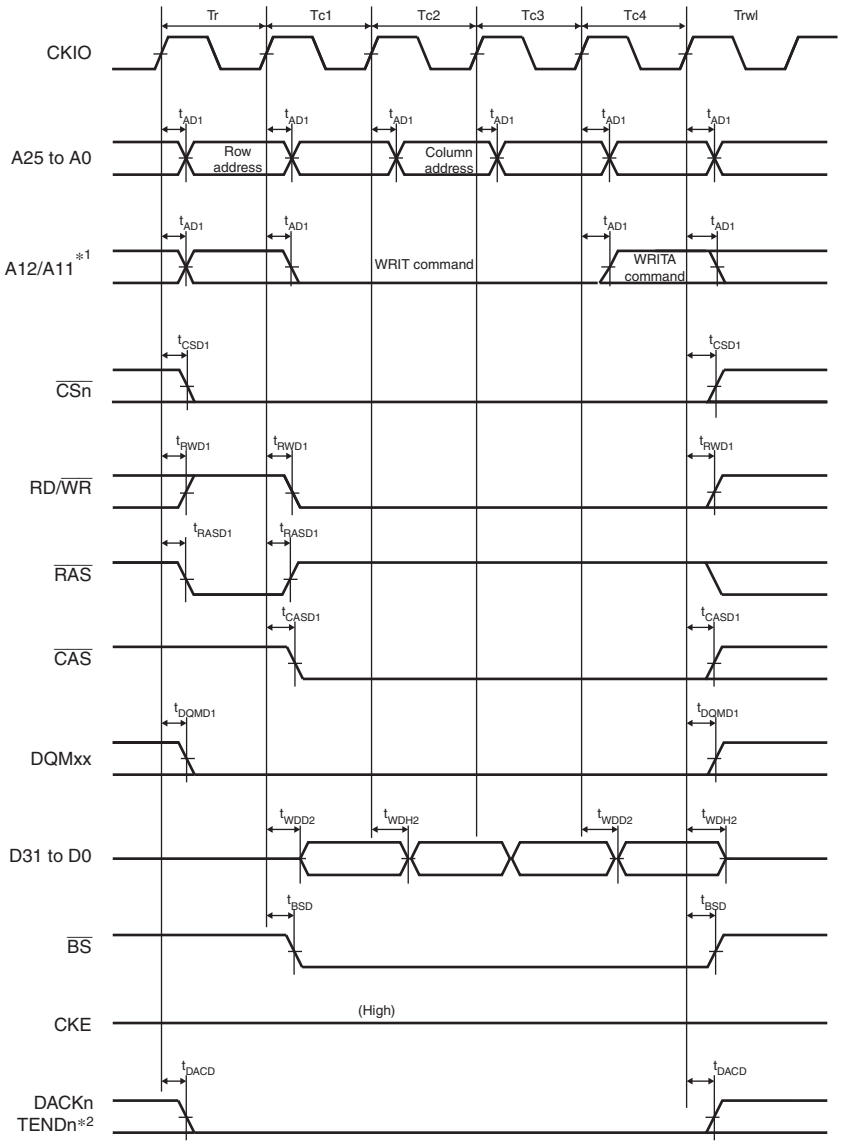
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.20 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, TRWL = 1 Cycle)



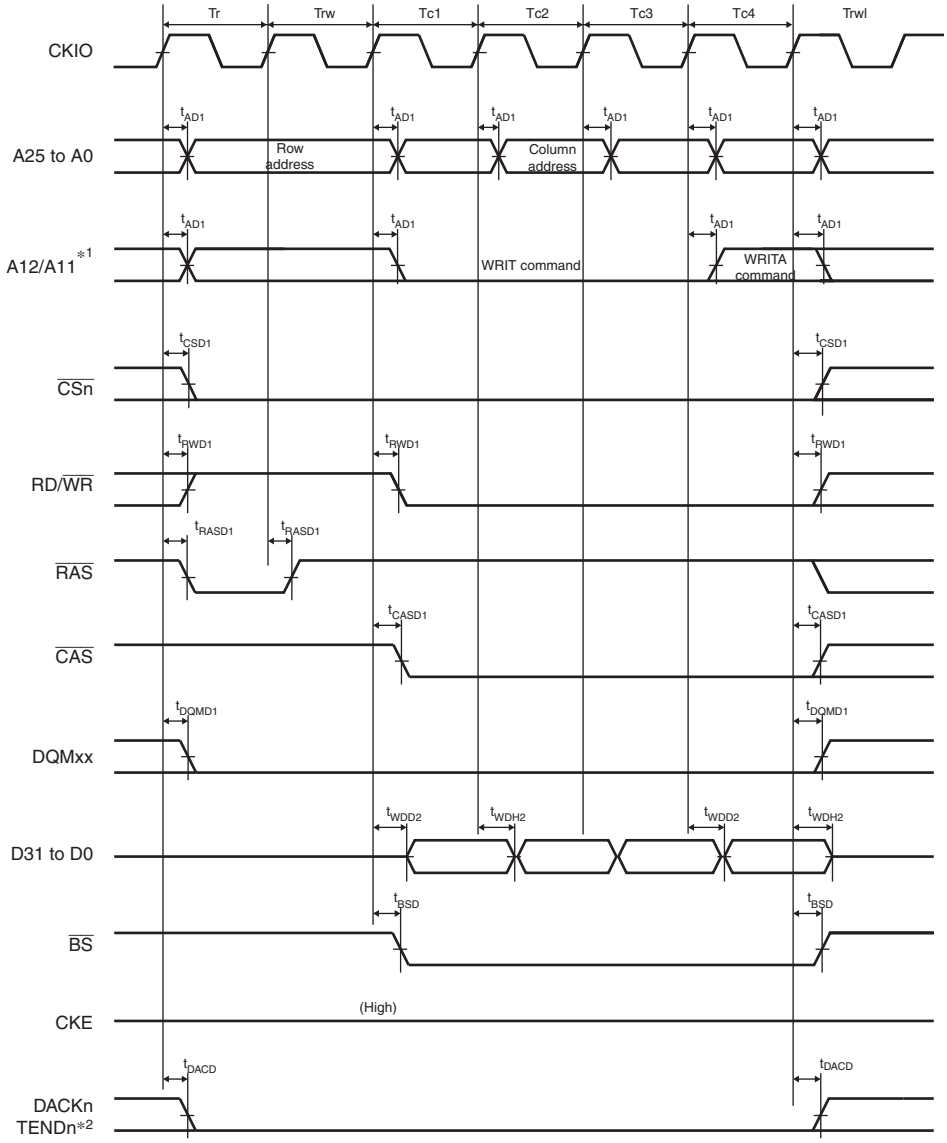
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.21 Synchronous DRAM Single Write Bus Cycle (Auto Precharge, WTRCD = 2 Cycles, TRWL = 1 Cycle)



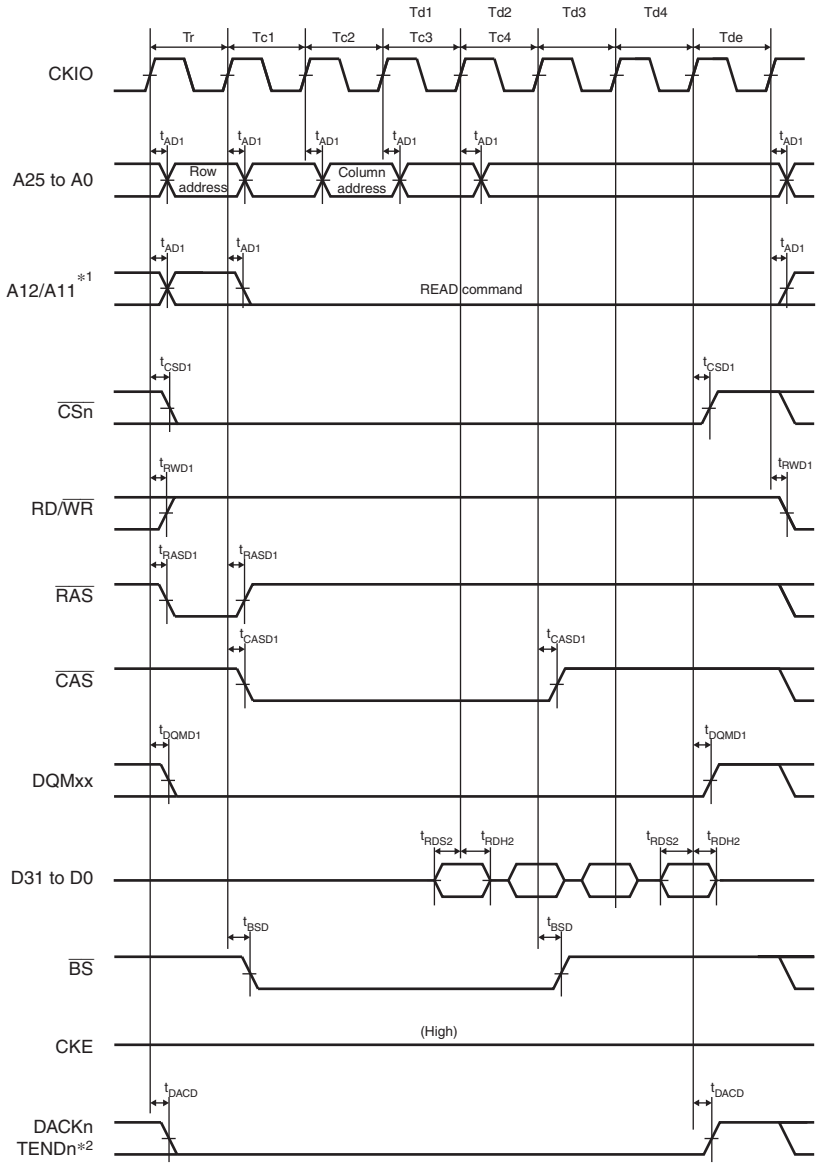
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.22 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 0 Cycle, TRWL = 1 Cycle)



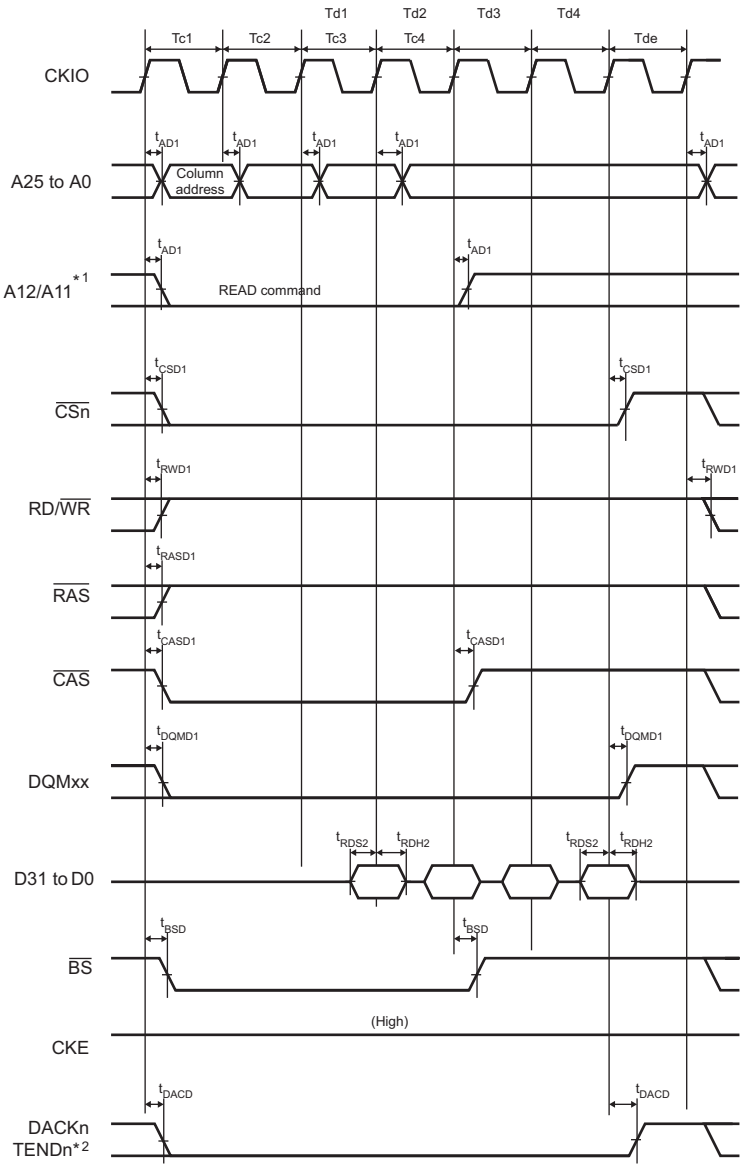
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.23 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Auto Precharge, WTRCD = 1 Cycle, TRWL = 1 Cycle)



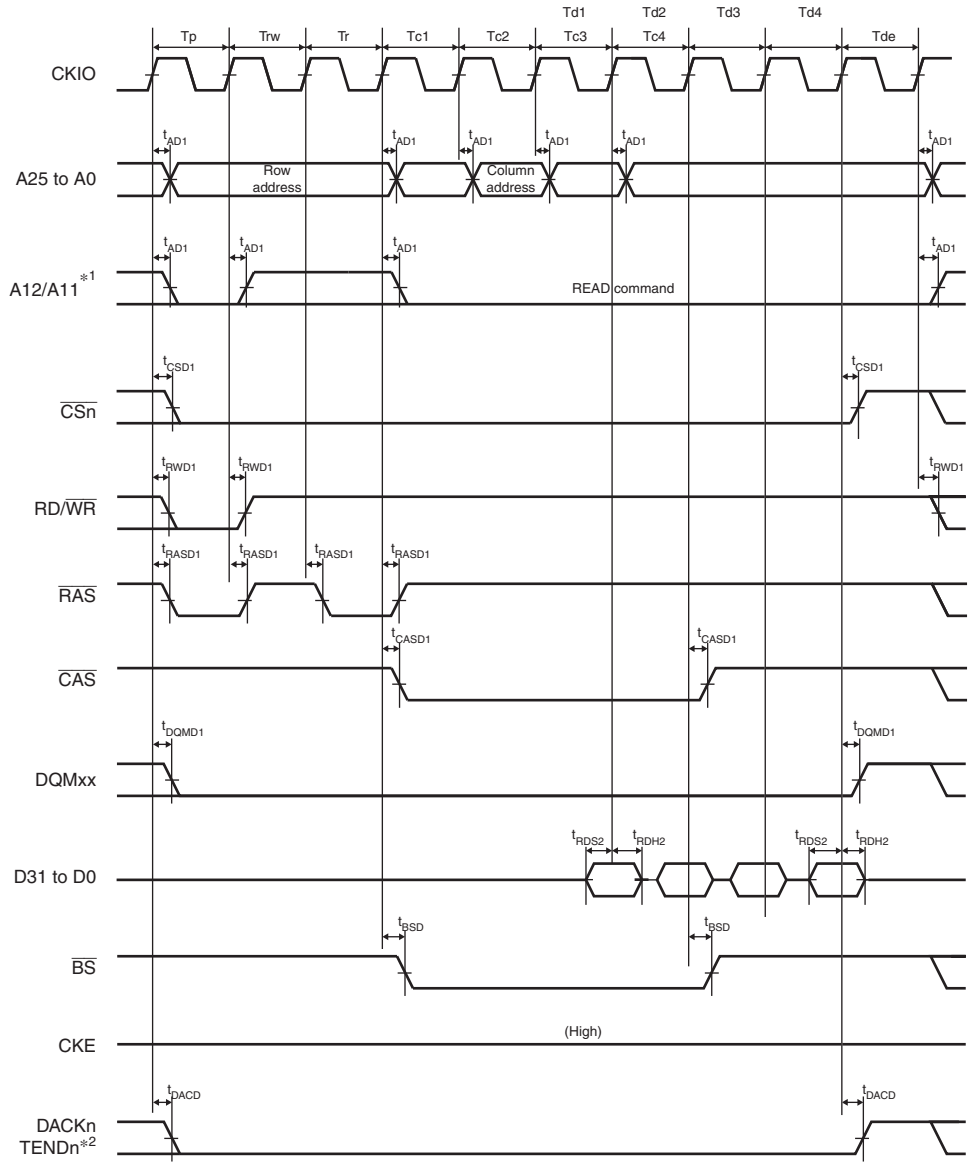
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.24 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: ACT + READ Commands, CAS Latency 2, WTRCD = 0 Cycle)



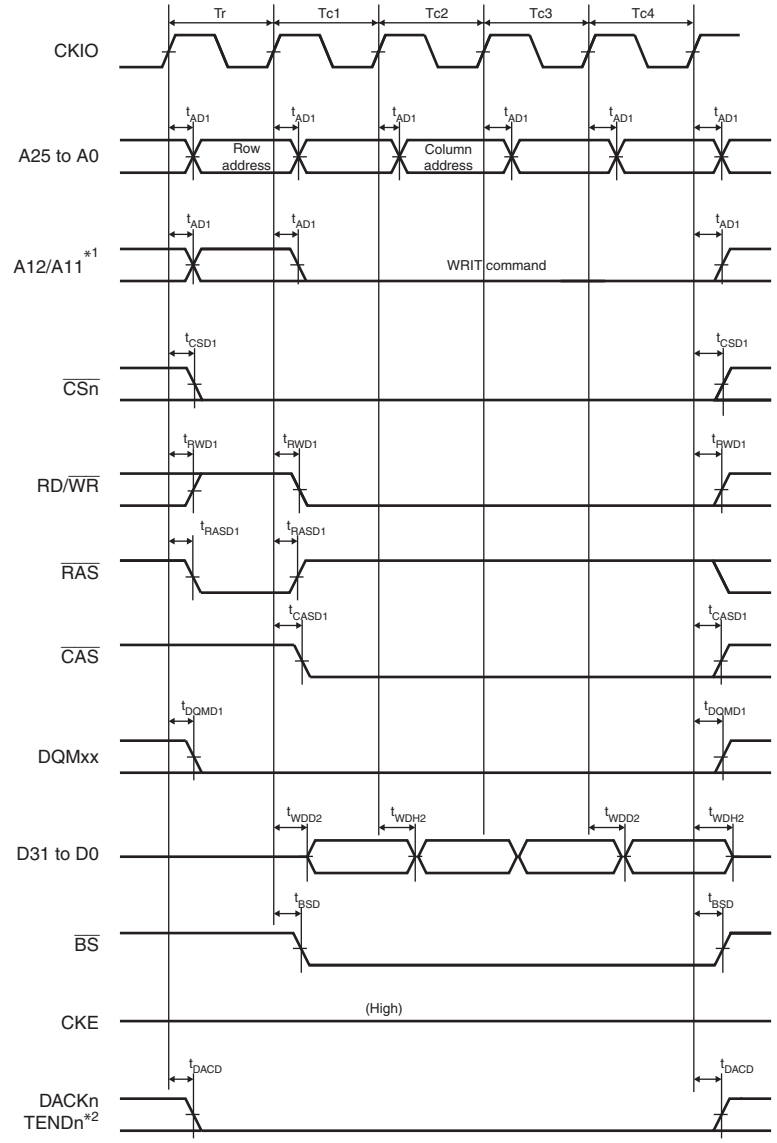
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.25 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: READ Command, Same Row Address, CAS Latency 2, WTRCD = 0 Cycle)



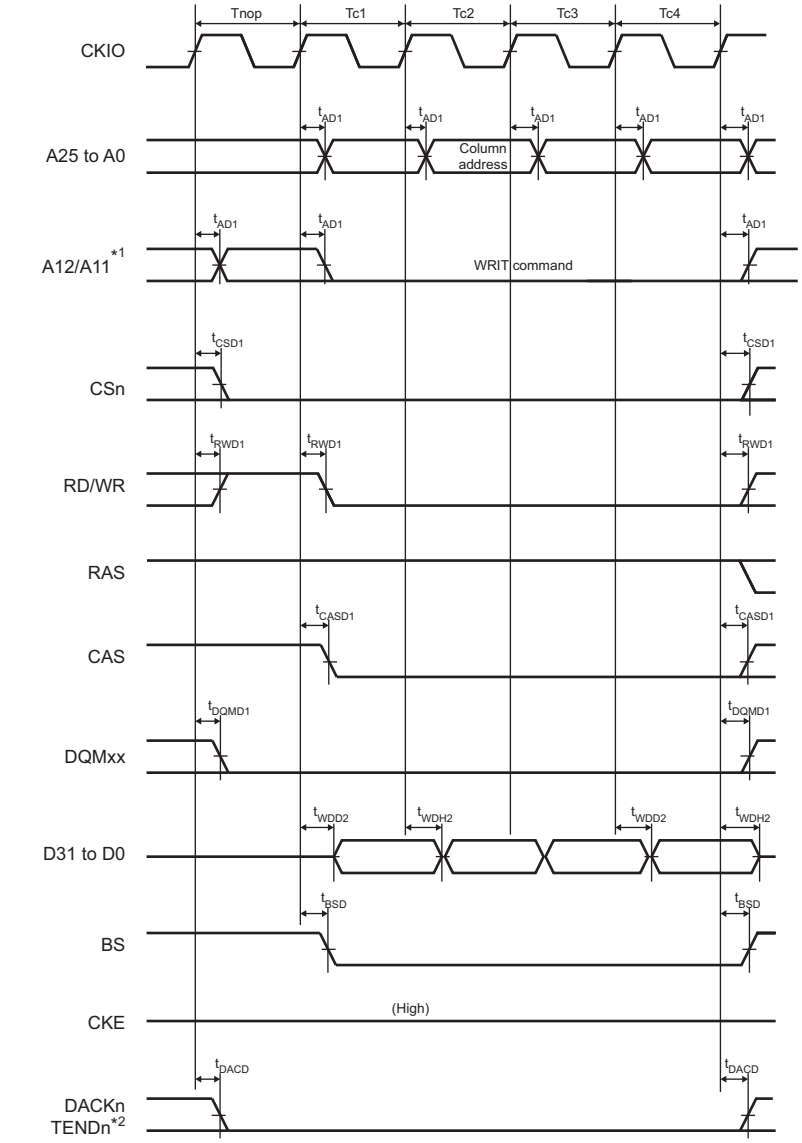
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.26 Synchronous DRAM Burst Read Bus Cycle (Four Read Cycles) (Bank Active Mode: PRE + ACT + READ Commands, Different Row Addresses, CAS Latency 2, WTRCD = 0 Cycle)



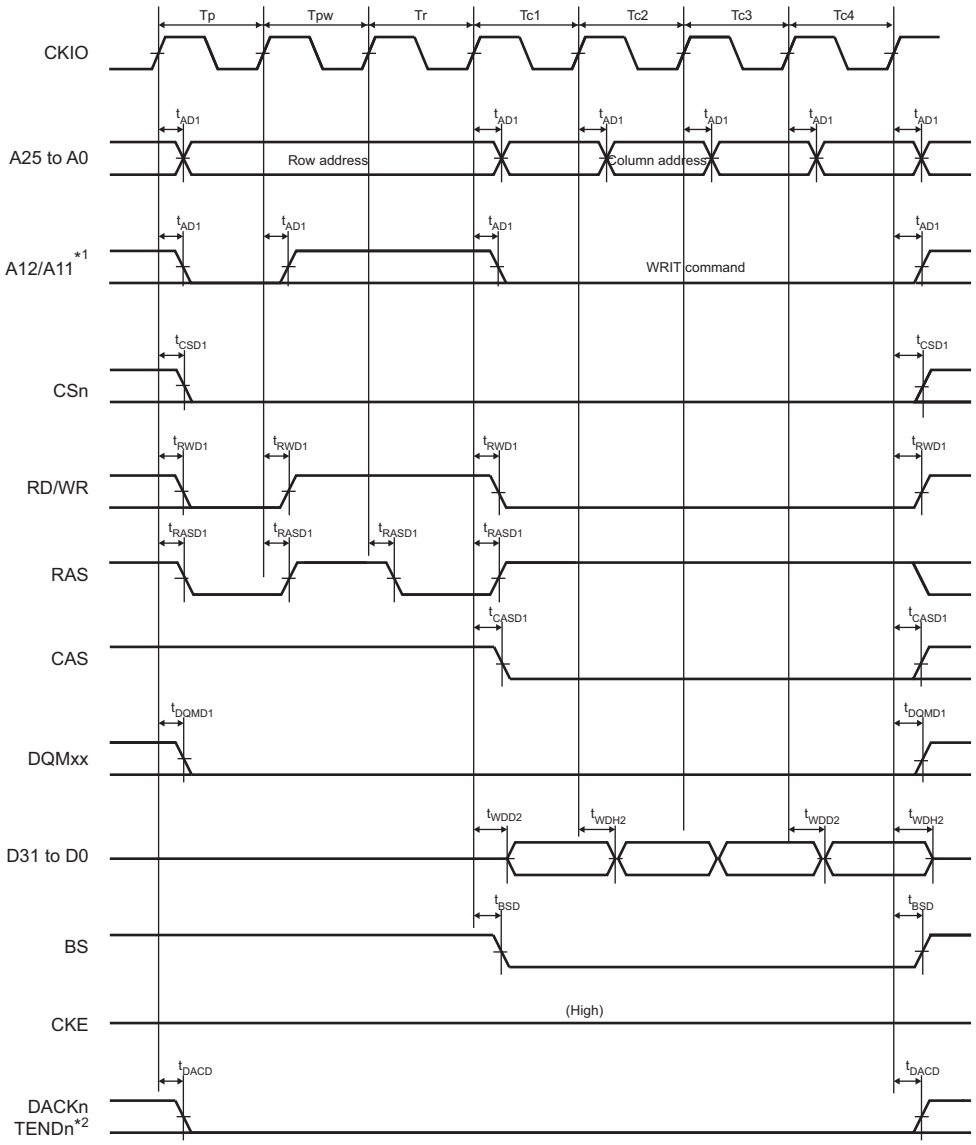
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.27 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: ACT + WRITE Commands, WTRCD = 0 Cycle, TRWL = 0 Cycle)



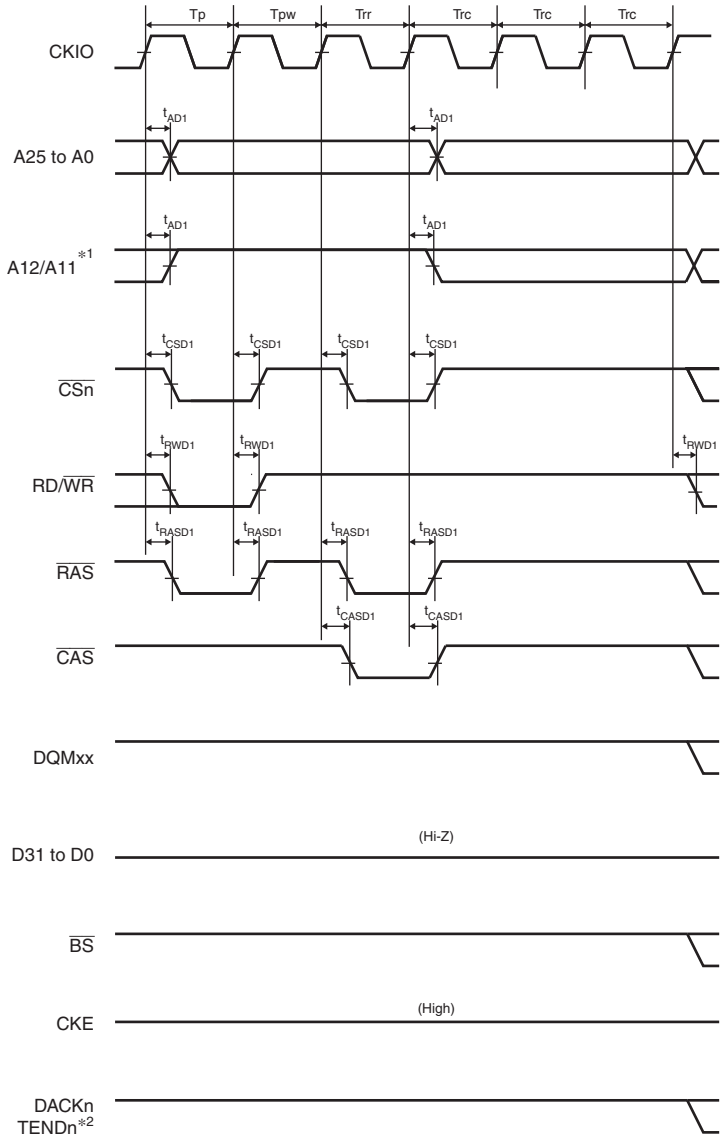
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.28 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: WRITE Command, Same Row Address, WTRCD = 0 Cycle, TRWL = 0 Cycle)



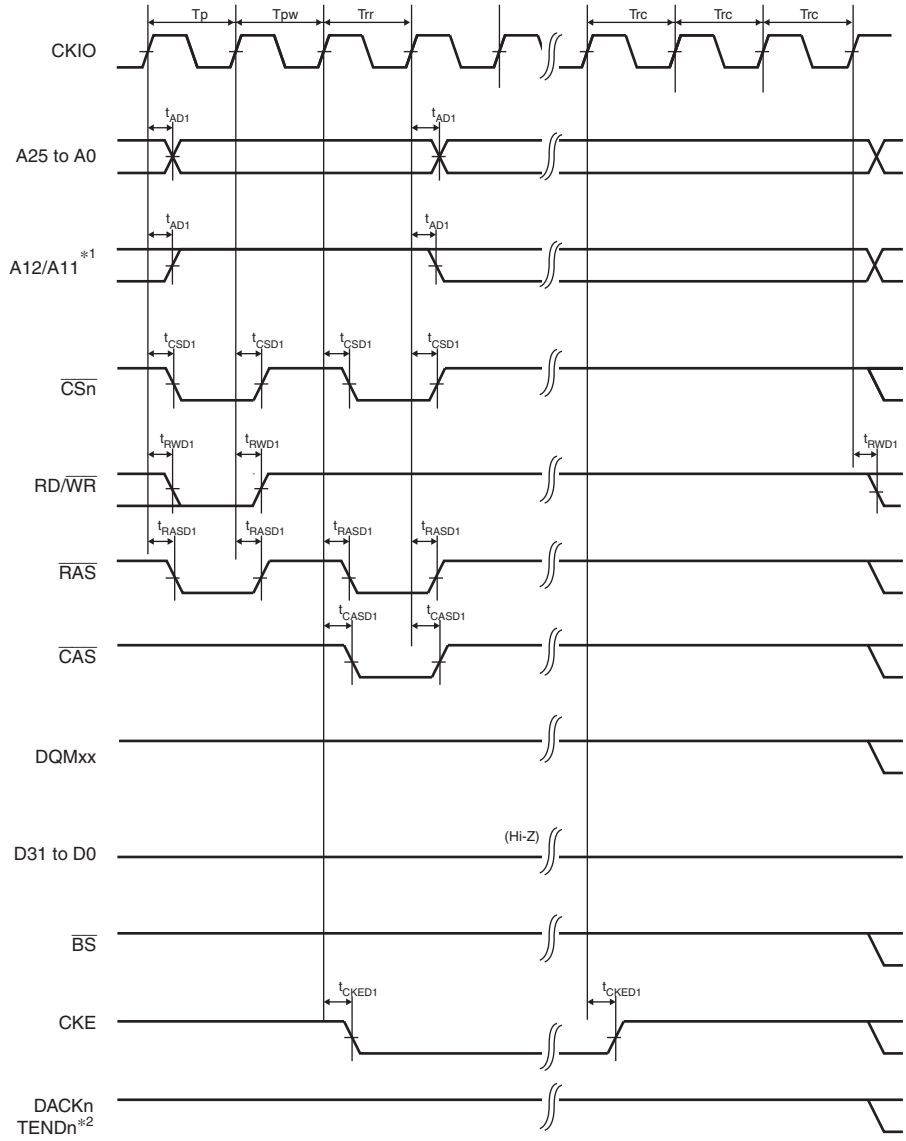
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.29 Synchronous DRAM Burst Write Bus Cycle (Four Write Cycles) (Bank Active Mode: PRE + ACT + WRITE Commands, Different Row Addresses, WTRCD = 0 Cycle, TRWL = 0 Cycle)



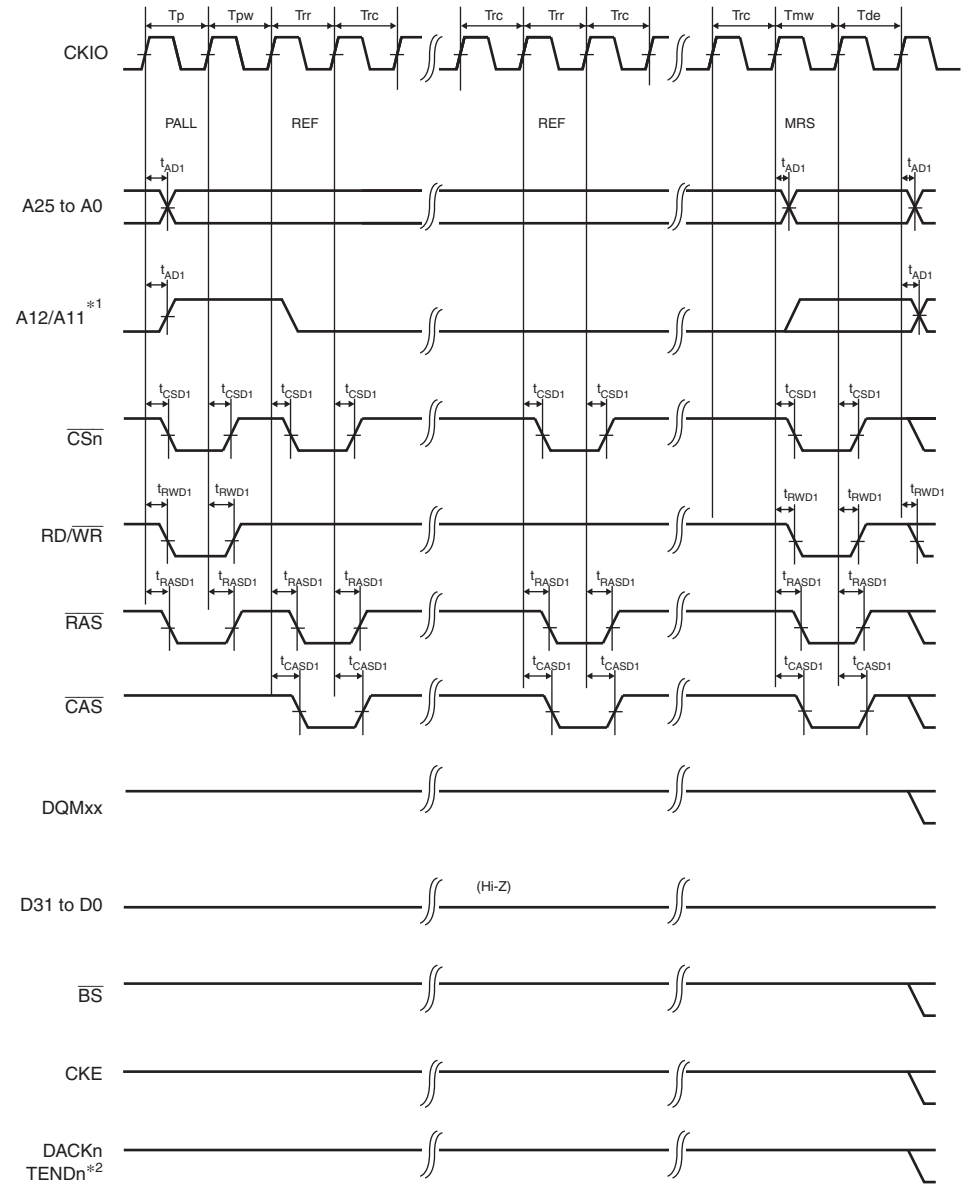
Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.30 Synchronous DRAM Auto-Refreshing Timing (WTRP = 1 Cycle, WTRC = 3 Cycles)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.31 Synchronous DRAM Self-Refreshing Timing (WTRP = 1 Cycle)



Notes: 1. An address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn and TENDn is when active low is specified.

Figure 3.32 Synchronous DRAM Mode Register Write Timing (WTRP = 1 Cycle)

3.4.4 Direct Memory Access Controller Timing

Table 3.8 Direct Memory Access Controller Timing

Item	Symbol	Min.	Max.	Unit	Figure
DREQ setup time	t_{DRQS}	5.5	—	ns	Figure 3.33
DREQ hold time	t_{DRQH}	2.5	—		
DACK, TEND delay time	t_{DACD}	0	12		Figure 3.34

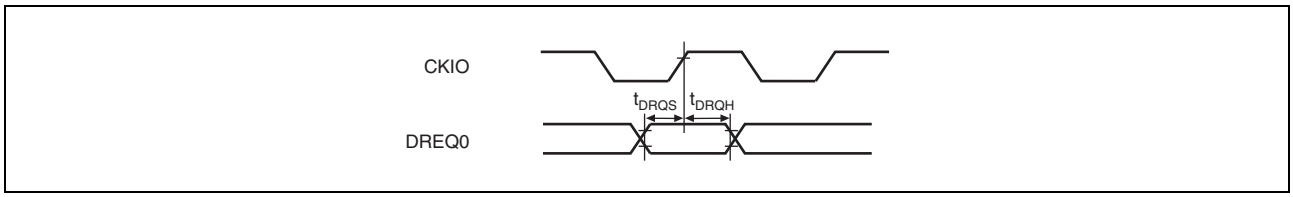


Figure 3.33 DREQ Input Timing

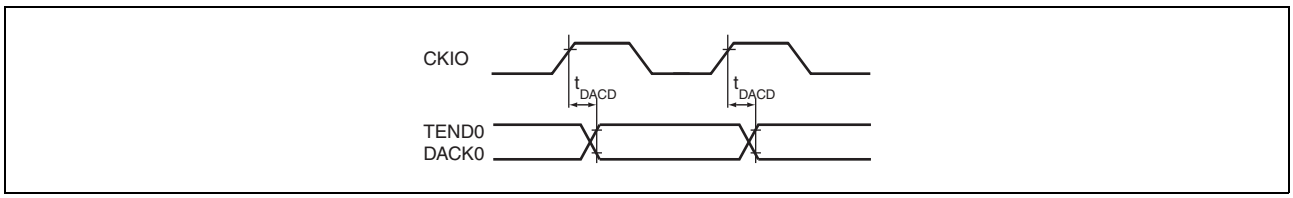


Figure 3.34 DACK, TEND Output Timing

3.4.5 Multi-Function Timer Pulse Unit 2 Timing

Table 3.9 Multi-Function Timer Pulse Unit 2 Timing

Item	Symbol	Min.	Max.	Unit	Figure
Timer clock pulse width (single edge)	$t_{TCKWH/L}$	1.5	—	t_{p0cyc}	Figure 3.35
Timer clock pulse width (both edges)	$t_{TCKWH/L}$	2.5	—	t_{p0cyc}	
Timer clock pulse width (phase counting mode)	$t_{TCKWH/L}$	2.5	—	t_{p0cyc}	

Note: t_{p0cyc} indicates peripheral clock (P0ϕ) cycle.

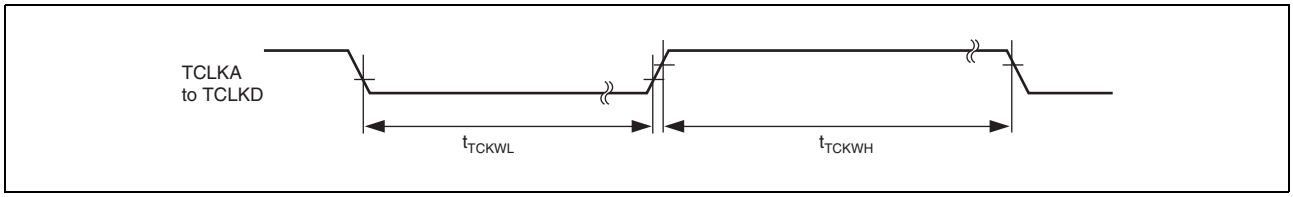


Figure 3.35 Clock Input Timing

3.4.6 Watchdog Timer Timing

Table 3.10 Watchdog Timer Timing

Item	Symbol	Min.	Max.	Unit	Figure
$\overline{\text{WDTOVF}}$ delay time	t_{WOVD}	—	100	ns	Figure 3.36

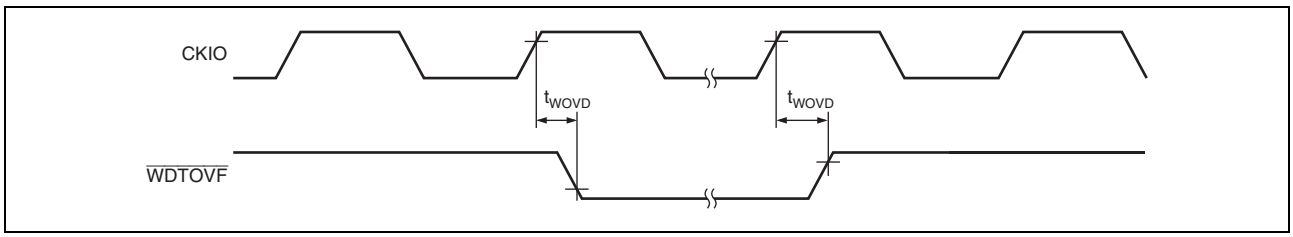


Figure 3.36 $\overline{\text{WDTOVF}}$ Output Timing

3.4.7 Serial Communication Interface with FIFO Timing

Table 3.11 Serial Communication Interface with FIFO Timing

Item		Symbol	Min.	Max.	Unit	Figure
Input clock cycle	(clocked synchronous)	t_{Scyc}	12	—	t_{p1cyc}	Figure 3.37
	(asynchronous)		4	—	t_{p1cyc}	
Input clock rise time		t_{SCKr}	—	1.5	t_{p1cyc}	
Input clock fall time		t_{SCKf}	—	1.5	t_{p1cyc}	
Input clock width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Transmit data delay time (clocked synchronous)		t_{TXD}	—	3 t_{p1cyc} + 15	ns	Figure 3.38
Receive data setup time (clocked synchronous)		t_{RXS}	4 t_{p1cyc} + 15	—	ns	
Receive data hold time (clocked synchronous)		t_{RXH}	1 t_{p1cyc} + 15	—	ns	

Note: t_{p1cyc} indicates the peripheral clock 1 (P1ϕ) cycle.

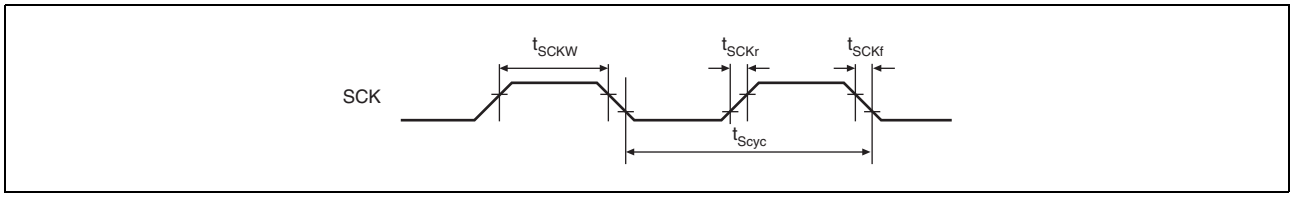


Figure 3.37 SCK Input Clock Timing

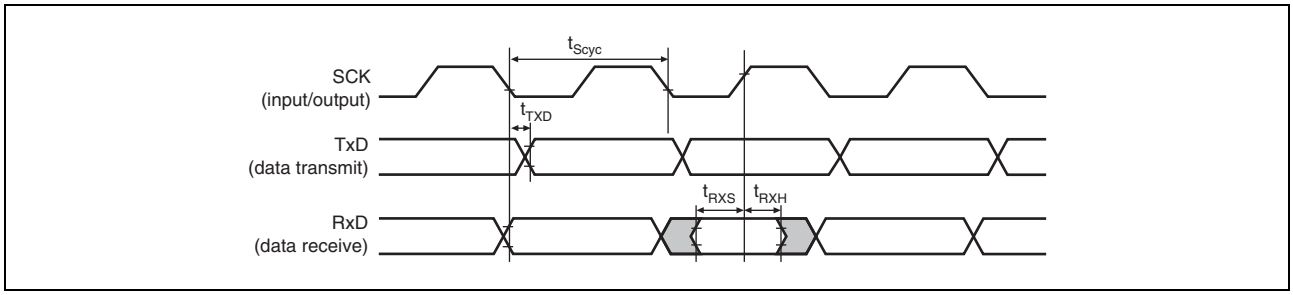


Figure 3.38 Transmit/Receive Data Input/Output Timing in Clocked Synchronous Mode

3.4.8 Serial Communication Interface Timing

Table 3.12 Serial Communication Interface Timing

Item		Symbol	Min.	Max.	Unit	Figure
Input clock cycle	(asynchronous)	t_{Scyc}	4	—	t_{p1cyc}	Figure 3.39
	(clocked synchronous)		6	—		
Input clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Input clock rise time		t_{SCKr}	—	20	ns	
Input clock fall time		t_{SCKf}	—	20	ns	
Output clock cycle	(asynchronous)	t_{Scyc}	16	—	t_{p1cyc}	
	(clocked synchronous)		4	—		
Output clock pulse width		t_{SCKW}	0.4	0.6	t_{Scyc}	
Output clock rise time		t_{SCKr}	—	20	ns	
Output clock fall time		t_{SCKf}	—	20	ns	
Transmit data delay time	(clocked synchronous)	t_{TXD}	—	40	ns	Figure 3.40
Receive data setup time	(clocked synchronous)	t_{RXS}	40	—	ns	
Receive data hold time	(clocked synchronous)	t_{RXH}	40	—	ns	

Note: t_{p1cyc} indicates the peripheral clock 1 (P1ϕ) cycle.

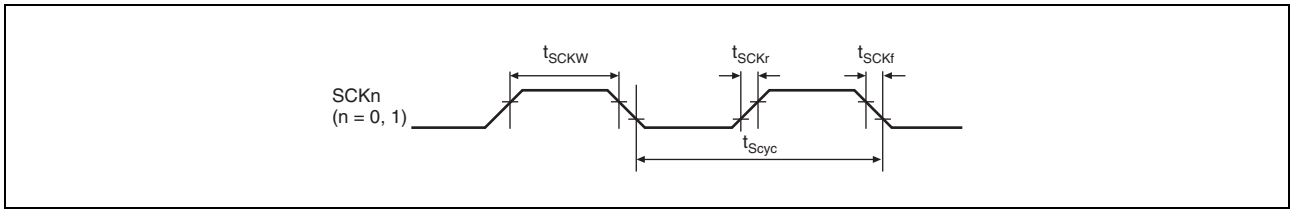


Figure 3.39 SCK Input Clock Timing

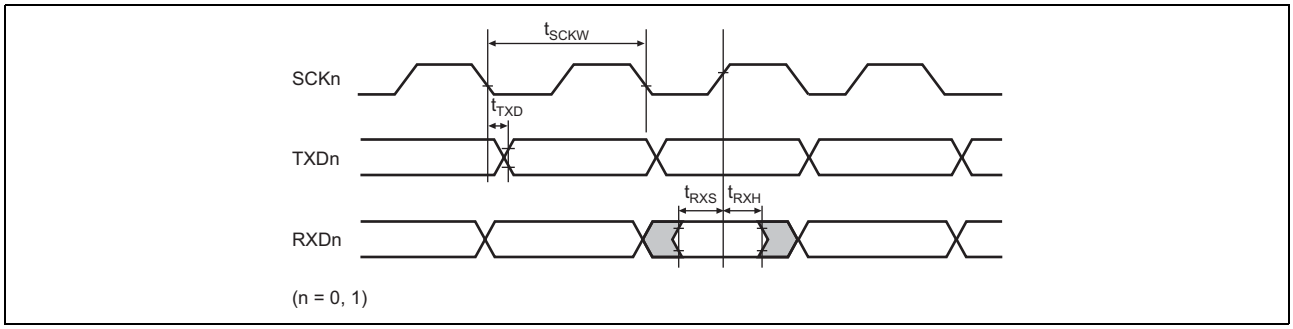


Figure 3.40 Transmit/Receive Data Input/Output Timing in Clocked Synchronous Mode

3.4.9 Renesas Serial Peripheral Interface Timing

Table 3.13 Renesas Serial Peripheral Interface Timing

Item		Symbol	Min.	Max.	Unit	Figure
RSPCK clock cycle	Master	t_{SPcyc}	2	4096	t_{cyc}	Figure 3.41
	Slave		8	4096		
RSPCK clock high pulse width	Master	t_{SPCKWH}	0.4	—	t_{SPcyc}	
	Slave		0.4	—		
RSPCK clock low pulse width	Master	t_{SPCKWL}	0.4	—	t_{SPcyc}	
	Slave		0.4	—		
Data input setup time	Master	t_{SU}	15	—	ns	Figure 3.42 to Figure 3.45
	Slave		0	—	t_{cyc}	
Data input hold time	Master	t_H	0	—	ns	
	Slave		4	—	t_{cyc}	
SSL setup time	Master	t_{LEAD}	$1 \times t_{SPcyc} - 20$	$8 \times t_{SPcyc}$	ns	
	Slave		4	—	t_{cyc}	
SSL hold time	Master	t_{LAG}	$1 \times t_{SPcyc}$	$8 \times t_{SPcyc} + 20$	ns	
	Slave		4	—	t_{cyc}	
Data output delay time	Master	t_{OD}	—	21	ns	
	Slave		—	4	t_{cyc}	
Data output hold time	Master	t_{OH}	5	—	ns	
	Slave		3	—	t_{cyc}	
Continuous transmission delay time	Master	t_{TD}	$1 \times t_{SPcyc} + 2\ t_{cyc}$	$8 \times t_{SPcyc} + 2 \times t_{cyc}$	ns	
	Slave		$4 \times t_{cyc}$	—		
Slave access time		t_{SA}	—	4	t_{cyc}	Figure 3.44 and Figure 3.45
Slave out release time		t_{REL}	—	3	t_{cyc}	

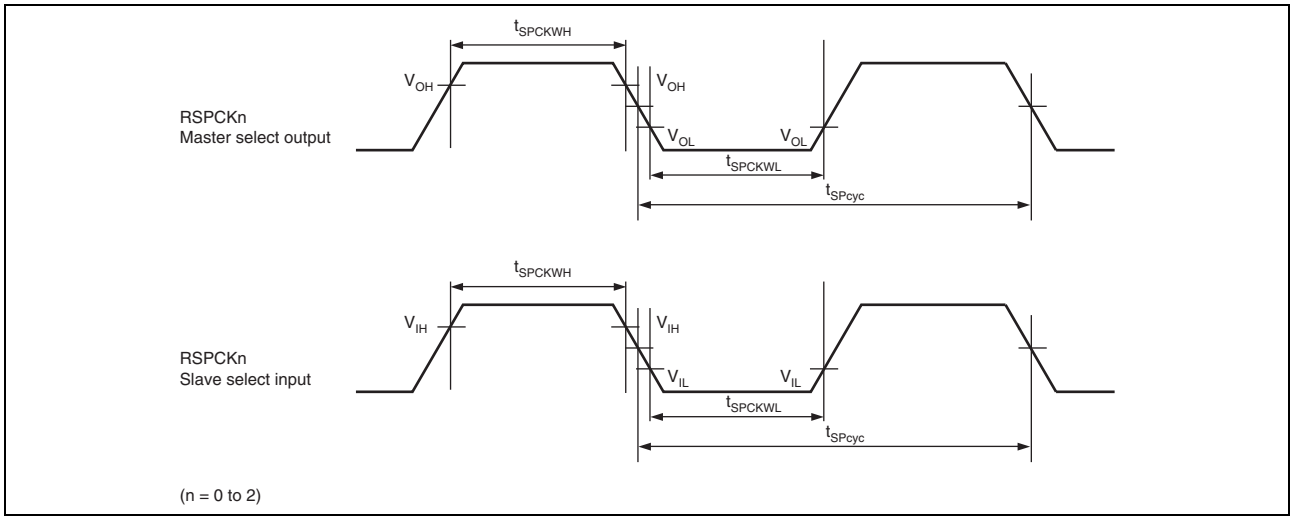


Figure 3.41 Clock Timing

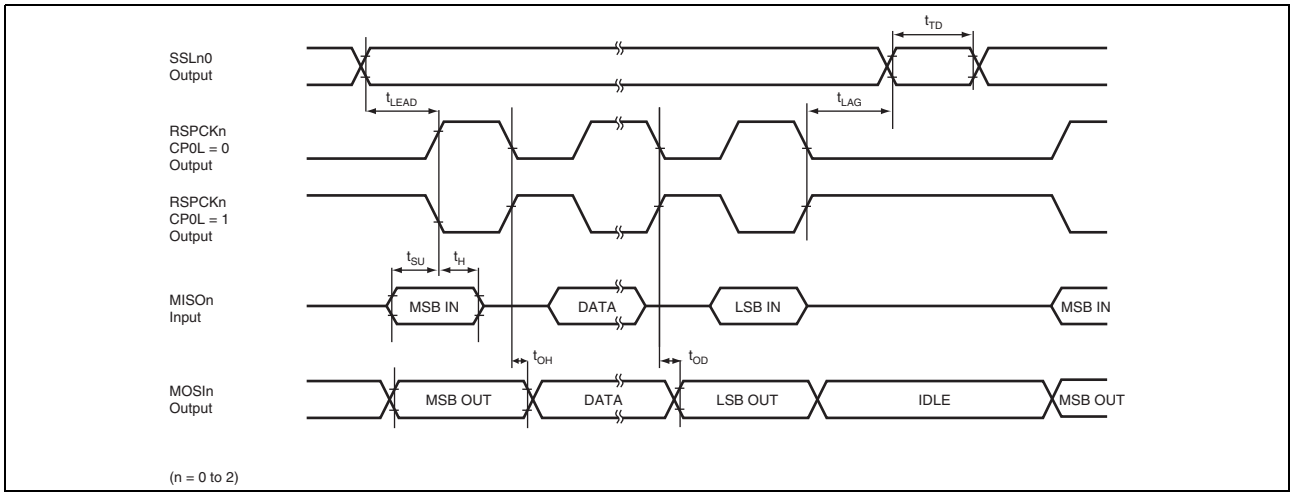


Figure 3.42 Transmission and Reception Timing (Master, CPHA = 0)

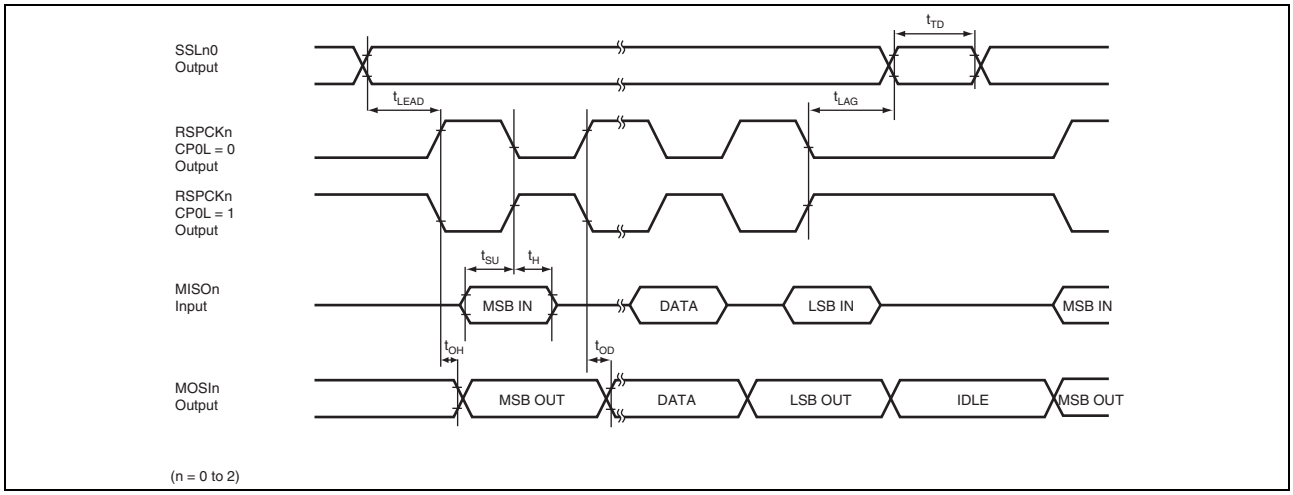


Figure 3.43 Transmission and Reception Timing (Master, CPHA = 1)

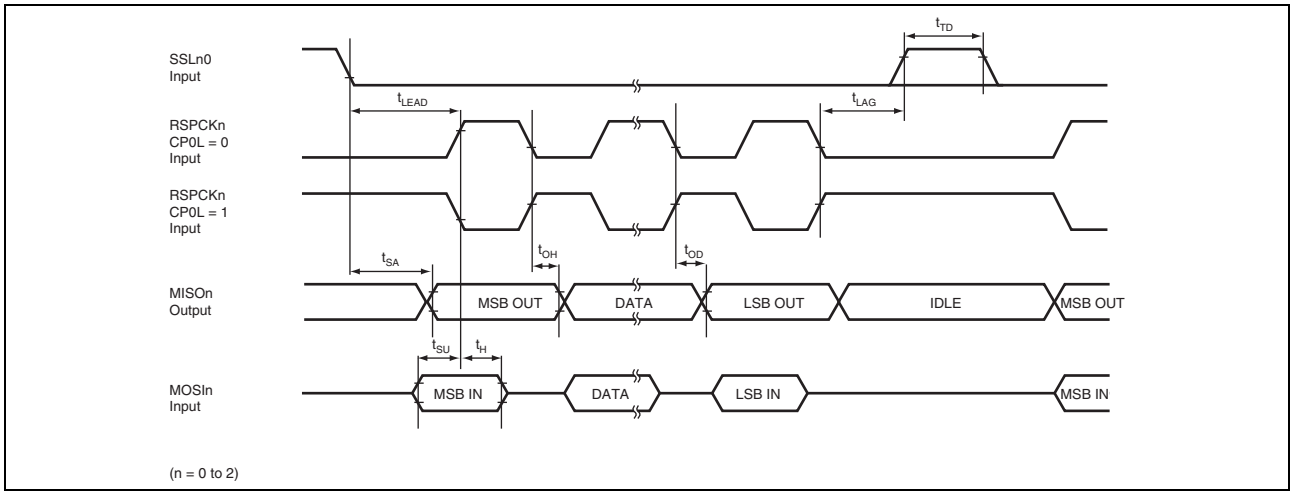


Figure 3.44 Transmission and Reception Timing (Slave, CPHA = 0)

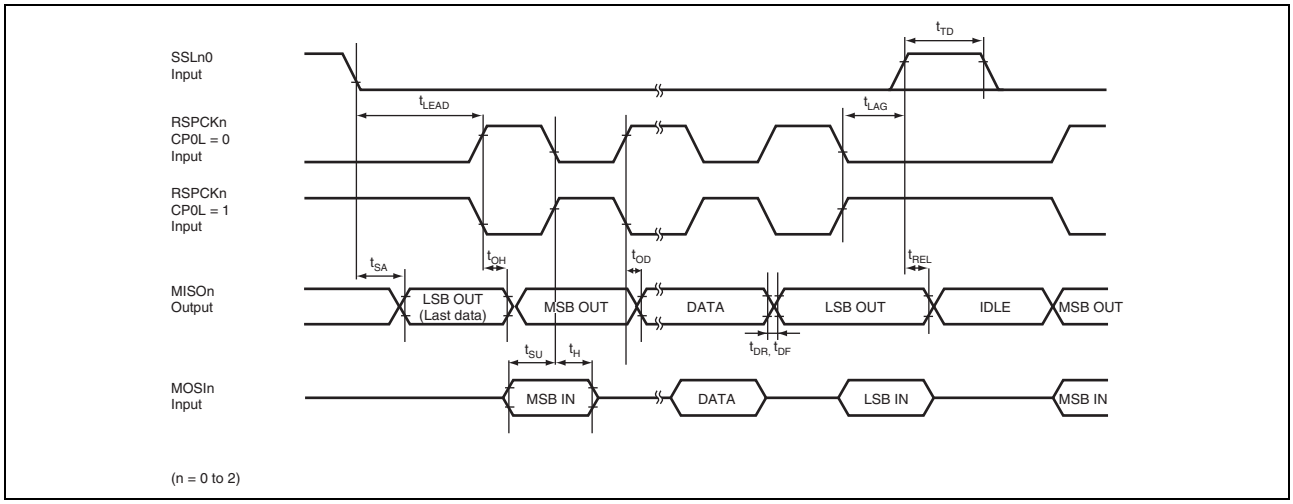


Figure 3.45 Transmission and Reception Timing (Slave, CPHA = 1)

3.4.10 SPI Multi I/O Bus Controller Timing

Table 3.14 SPI Multi I/O Bus Controller Timing

Item		Symbol	Min.	Max.	Unit	Figure
SPBCLK clock cycle		t_{SPBcyc}	2	4080	t_{bcyc}	Figure 3.46
SPBCLK high pulse width		t_{SPBWH}	0.475	0.525	t_{SPBcyc}	
SPBCLK low pulse width		t_{SPBWL}	0.475	0.525	t_{SPBcyc}	
SPBCLK rise time		t_{SPBR}	—	3	ns	
SPBCLK fall time		t_{SPBF}	—	3	ns	
Data input setup time	CKDLY = B'0100 (initial value)	t_{SU}	5.0	—	ns	Figure 3.47, Figure 3.48, Figure 3.49, and Figure 3.50
	CKDLY = B'1010 (RZ/A1LU only)		2.0*2	—		
Data input hold time	CKDLY = B'0100	t_H	0.0	—	ns	
	CKDLY = B'1010 (RZ/A1LU only)		1.0*2	—		
SSL setup time		t_{LEAD}	1 × t_{SPBcyc} - 3	8 × t_{SPBcyc} + 3	ns	
SSL hold time		t_{LAG}	1.5 × t_{SPBcyc}	8.5 × t_{SPBcyc} + 3	ns	
Continuous transfer delay time		t_{TD}	1	8	t_{SPBcyc}	
Data output delay time	SPODLY = H'0000 (initial value)	t_{OD}	—	4.0	ns	
	SPODLY = H'1111 (RZ/A1LU only)		—	5.0*2		
Data output hold time	SPODLY = H'0000 (initial value)	t_{OH}	–2.0	—	ns	
	SPODLY = H'1111 (RZ/A1LU only)		1.0*2	—		
Data output buffer on time	SPODLY = H'0000 (initial value)	t_{BON}	—	4.0	ns	Figure 3.47, Figure 3.48, Figure 3.49, Figure 3.50, Figure 3.51, and Figure 3.52
	SPODLY = H'1111 (RZ/A1LU only)		—	5.0*2		
Data output buffer off time	SPODLY = H'0000 (initial value)	t_{BOFF}	–9.0	0	ns	
	SPODLY = H'1111 (RZ/A1LU only)		1.5*2	7.5*2		

Note 1. t_{bcyc} indicates the bus clock (Bϕ) cycle.
Note 2. Value when the output load is 15 pF

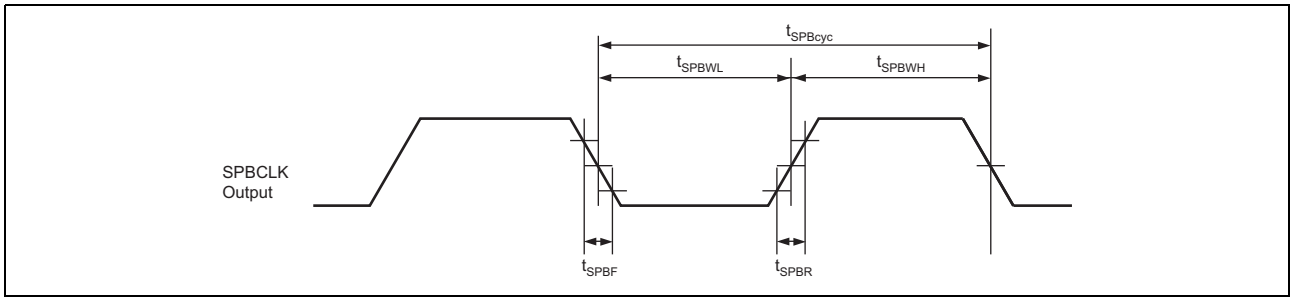


Figure 3.46 Clock Timing

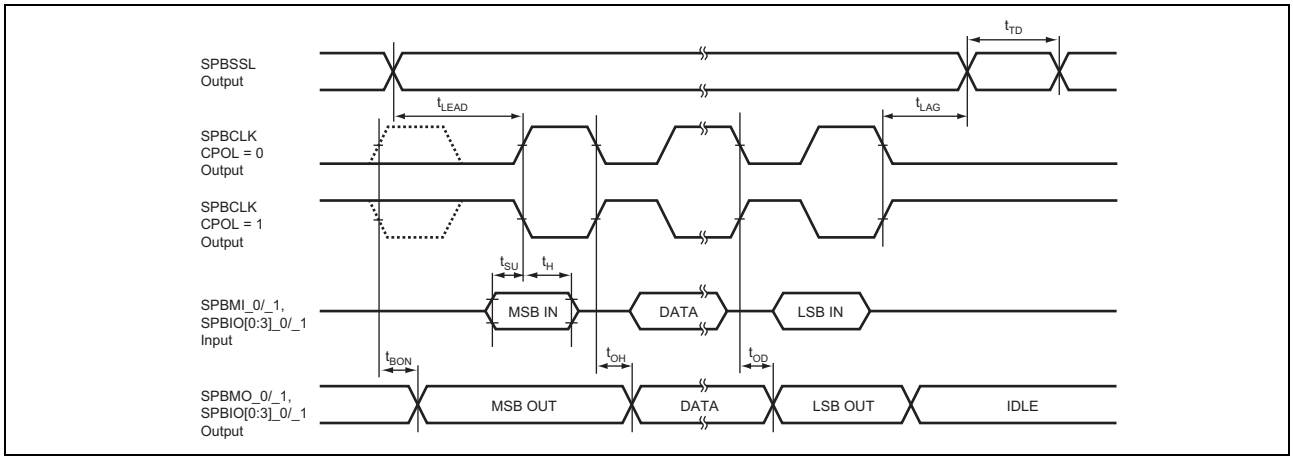


Figure 3.47 SDR Transfer Format Transmission and Reception Timing (CPHAT = 0, CPHAR = 0)

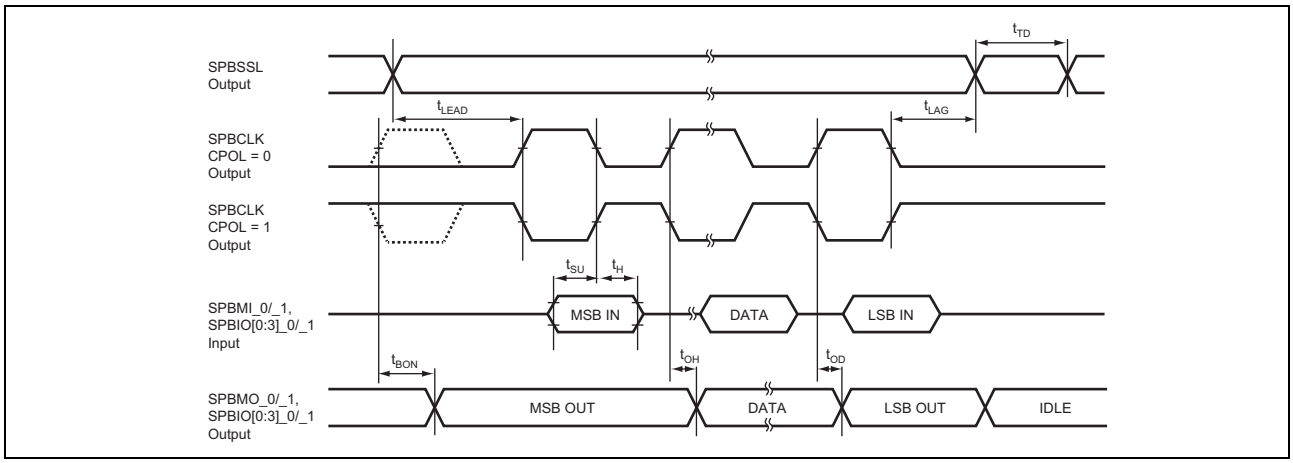


Figure 3.48 SDR Transfer Format Transmission and Reception Timing (CPHAT = 1, CPHAR = 1)

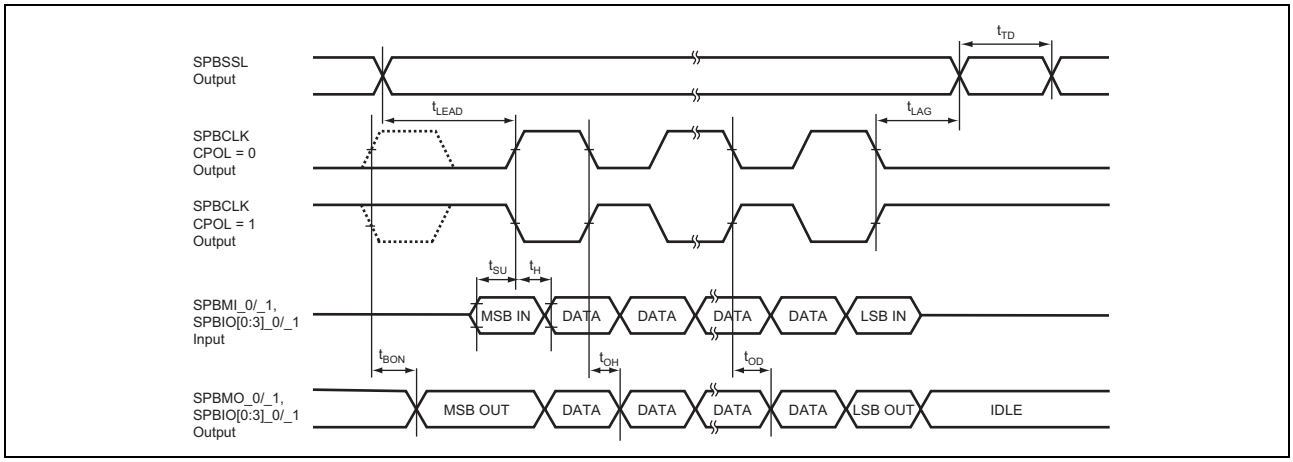


Figure 3.49 DDR Transfer Format Transmission and Reception Timing (CPHAT = 0, CPHAR = 0) (RZ/A1LU only)

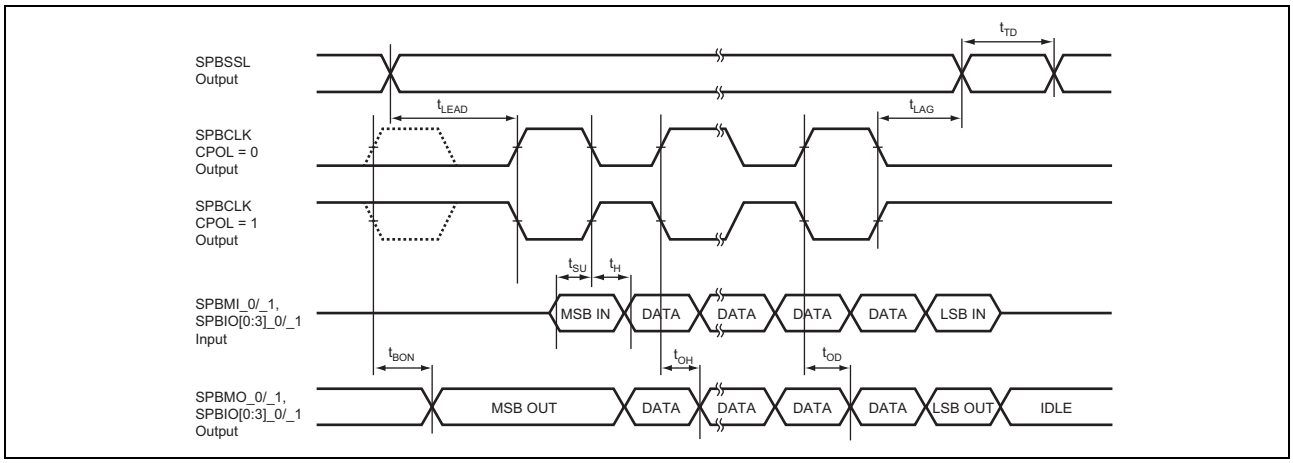


Figure 3.50 DDR Transfer Format Transmission and Reception Timing (CPHAT = 1, CPHAR = 1) (RZ/A1LU only)

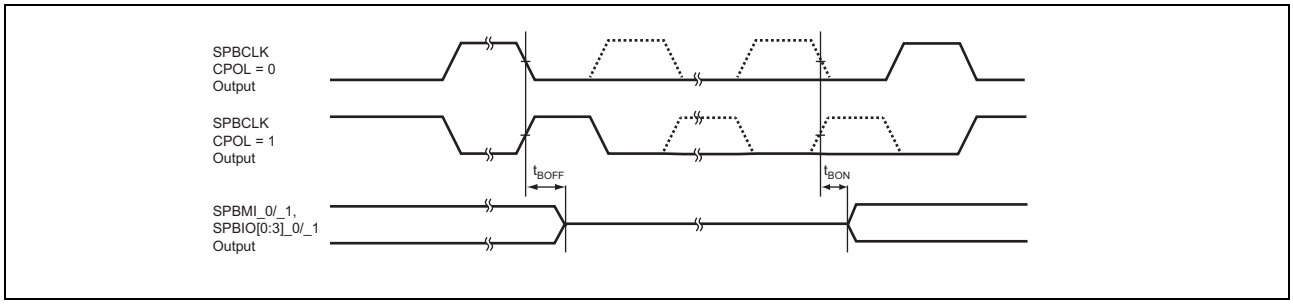


Figure 3.51 Timing for Switching the Buffers on and off (CPHAT = 0, CPHAR = 0)

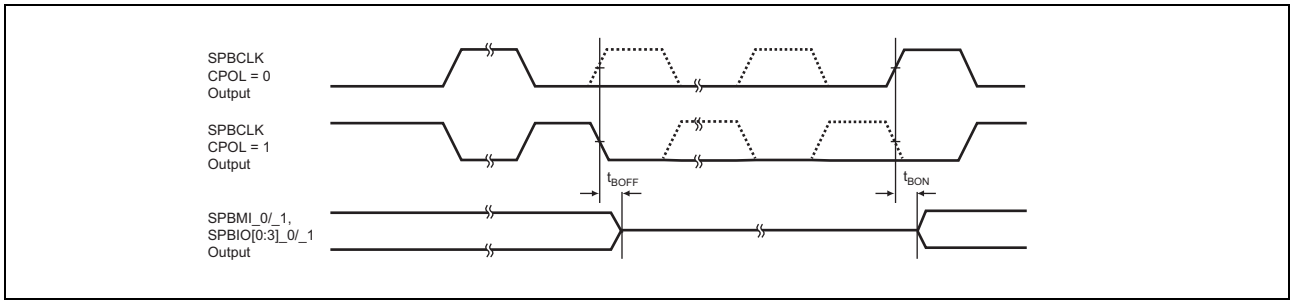


Figure 3.52 Timing for Switching the Buffers on and off (CPHAT = 1, CPHAR = 1)

3.4.11 I²C Bus Interface Timing

Table 3.15 I²C Bus Interface Timing

			Standard mode (Sm)		Fast mode (Fm)		
Item	**Symbol**	**I/O**	**Min.**	**Max.**	**Min.**	**Max.**	**Unit**
SCL clock frequency	f_{CLK}	I/O	0	100	0	400	kHz
Bus free time (between stop and start condition)	t_{BUF}	I/O	4.7	-	1.3	-	µs
Hold time*1	$t_{HD:STA}$	I/O	4.0	-	0.6	-	µs
Low period of SCL clock	t_{LOW}	I/O	4.7	-	1.3	-	µs
High period of SCL clock	t_{HIGH}	I/O	4.0	-	0.6	-	µs
Setup time for start/restart condition	$t_{SU:STA}$	I/O	4.7	-	0.6	-	µs
Data hold time (I²C bus device)	$t_{HD:DAT}$	I/O	0*2	-	0*2	-	µs
Data setup time	$t_{SU:DAT}$	I/O	250	-	100*3	-	ns
SDA and SCL signal rise time	t_R	Input	-	1000	20	300	ns
SDA and SCL signal fall time*3	t_F	Input	-	300	20 × (PV_{CC}/5.5V)	300	ns
		Output	-	250	20 × (PV_{CC}/5.5V)	250	ns
Setup time for STOP condition	$t_{SU:STO}$	I/O	4.0	-	0.6	-	µs
Capacitive load for each bus line	C_b	-	-	400*4	-	400*4	pF
Pulse width of spikes that must be suppressed by the input filter	t_{SP}	Input	-	-	0	50*5	ns

In the above table and subsequently, SCL and SDA refer to the RIICnSCL and RIICnSDA signals, respectively.

Note 1. The first clock pulse is generated on the SCL line after the start condition has been issued and the hold time has elapsed.

Note 2. This module requires a minimum of 300 ns hold time internally for the SDA signal to handle the period over which the falling edge of SCL has not reached a defined level (time until the SCL signal reaches V_{IL} (max.) from V_{IH} (min.)).

Note 3. The fast-mode I²C bus device can be used in the standard mode I²C bus system. In this case, the minimum value of the data setup time ($t_{SU:DAT}$ 250 [ns]) must be satisfied.
If the system does not extend the low period of SCL clock (t_{LOW}), this condition is automatically satisfied. If the system extends the low period of SCL clock (t_{LOW}), transmit the subsequent data bit to the SDA line before the SCL line is released ($t_R$max. + $t_{SU:DAT}$ = 1000 + 250 = 1250 [ns]: (standard mode I²C bus specification)).

Note 4. Total capacitance of one bus line. The allowable maximum bus capacitance may differ from this specification, depending on the actual operating voltage and frequency of an application. For techniques to cope with a large bus capacitance, see the I²C bus specification provided by NXP Semiconductors.

Note 5. Noise is removed by the analog and digital input filters. The level of noise reduction of the digital input filter is determined by the period of internal reference clock (IICφ) and the NF[1:0] bits in RIICnMR3. For details, refer to section 18, I²C Bus Interface, in the RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group User's Manual.

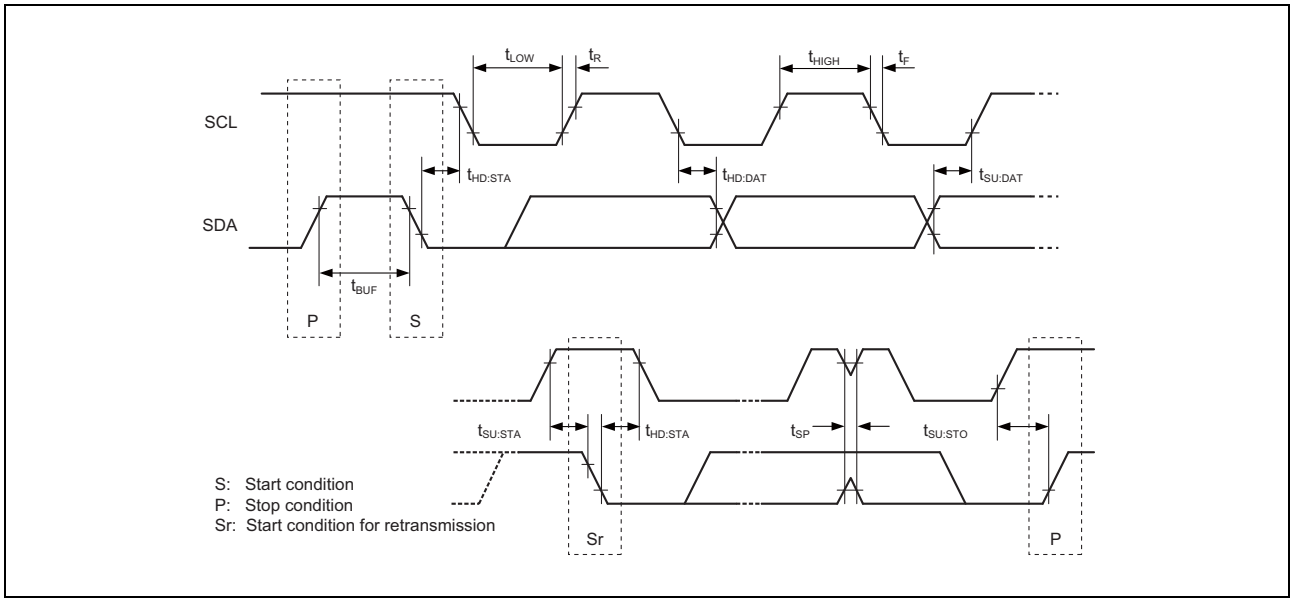


Figure 3.53 Input/Output Timing

3.4.12 Serial Sound Interface Timing

Table 3.16 Serial Sound Interface Timing

Item		Symbol	Min.	Max.	Unit	Remarks	Figure
Output clock cycle		t_O	80	64000	ns	Output	Figure 3.54
Input clock cycle		t_I	80	64000	ns	Input	
Clock high		t_{HC}	32	—	ns	Bidirectional	
Clock low		t_{LC}	32	—	ns		
Clock rise time		t_{RC}	—	25	ns	Output	
Delay	Noise canceler not in use	t_{DTR}	–5	25	ns		Figure 3.55, Figure 3.56, Figure 3.57, Figure 3.58, and Figure 3.59
	Noise canceler in use		10	45			
SSIWS delay (RZ/A1LU and RZ/A1LC only)*			–5	15			
Setup time		t_{SR}	25	—	ns		
Hold time		t_{HTR}	5	—	ns		

Note: * For SSIWS delay of the RZ/A1L, refer to the values in the entry on “Delay (Noise canceler not in use)”.

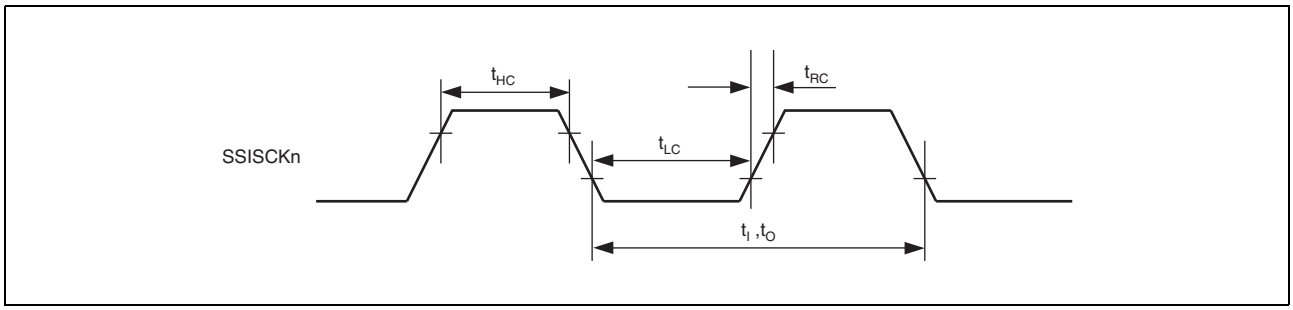


Figure 3.54 Clock Input/Output Timing

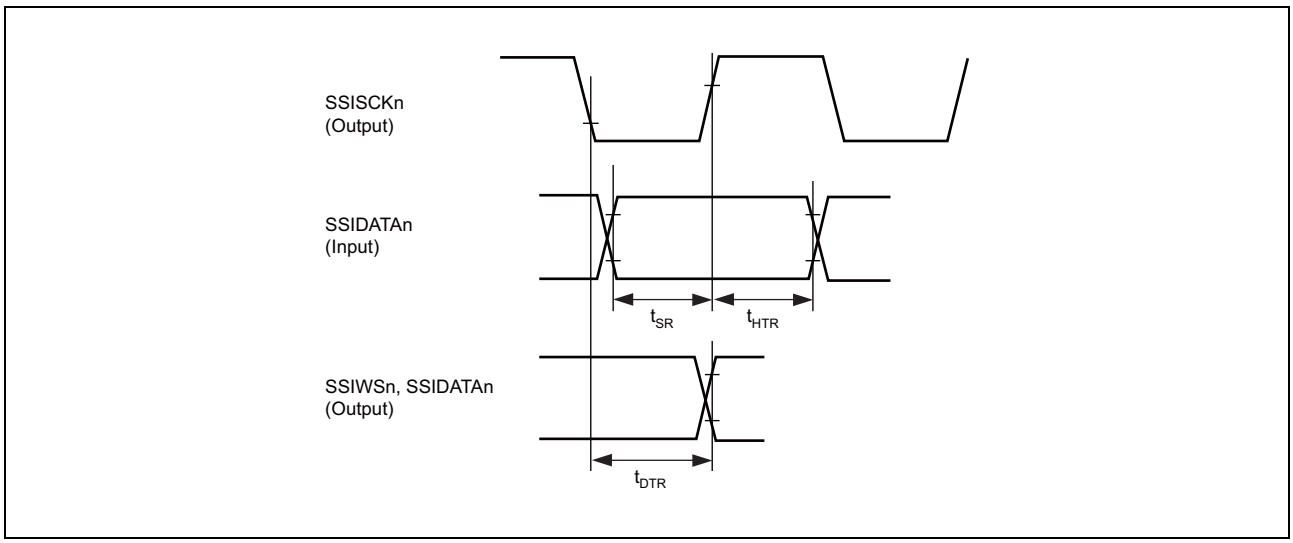


Figure 3.55 Transmission and Reception Timing (Master, SSICR_n.SCKP = 0)

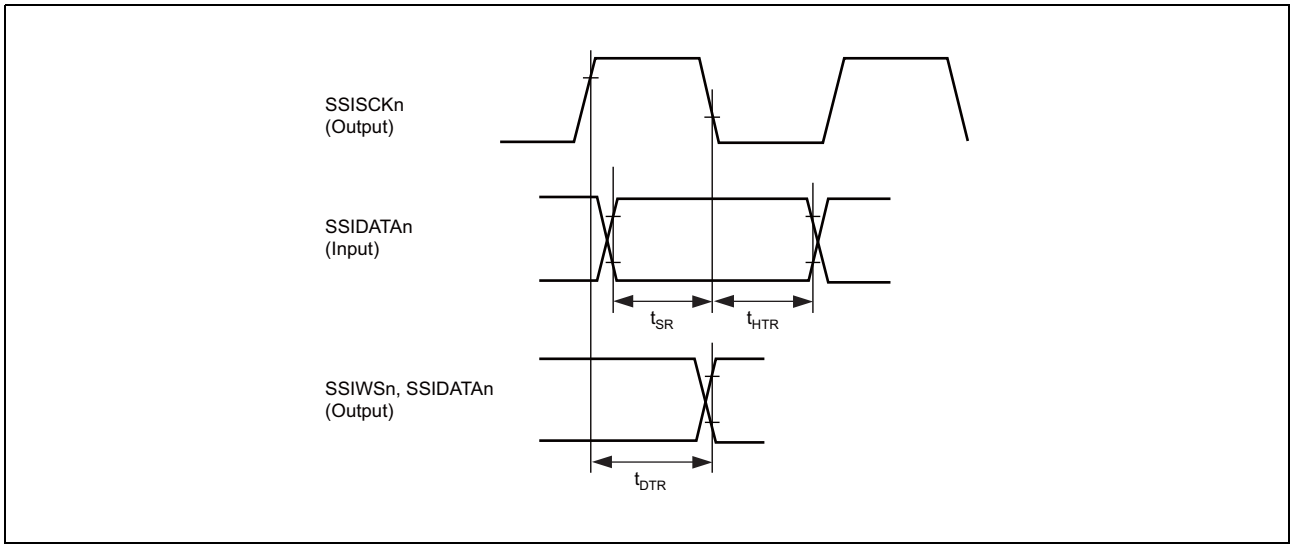


Figure 3.56 Transmission and Reception Timing (Master, SSICR_n.SCKP = 1)

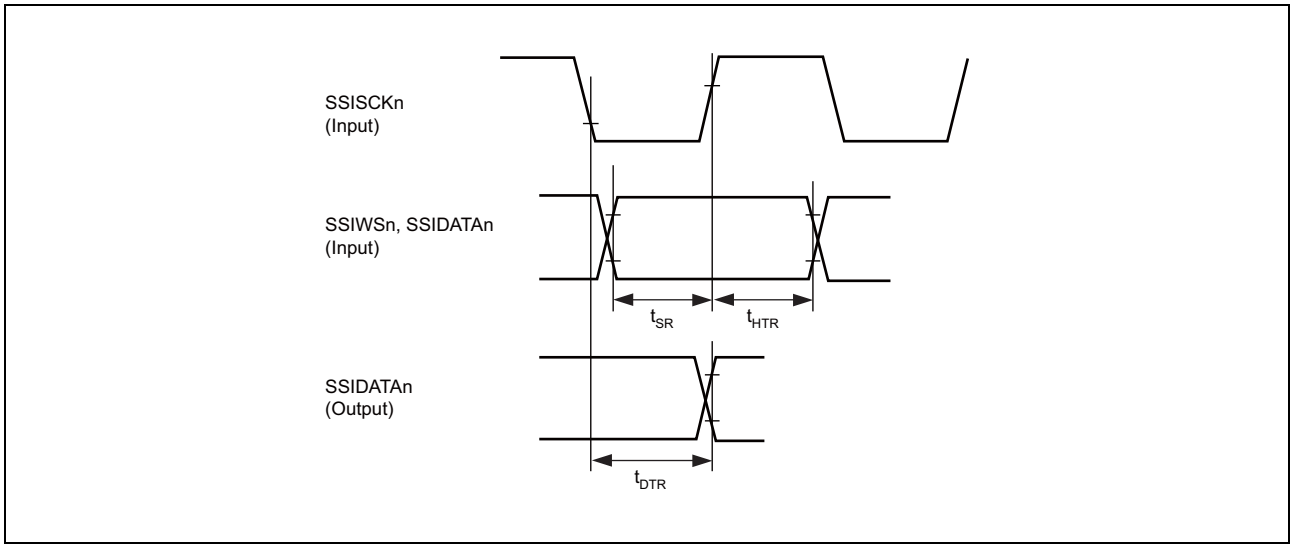


Figure 3.57 Transmission and Reception Timing (Slave, SSICR_n.SCKP = 0)

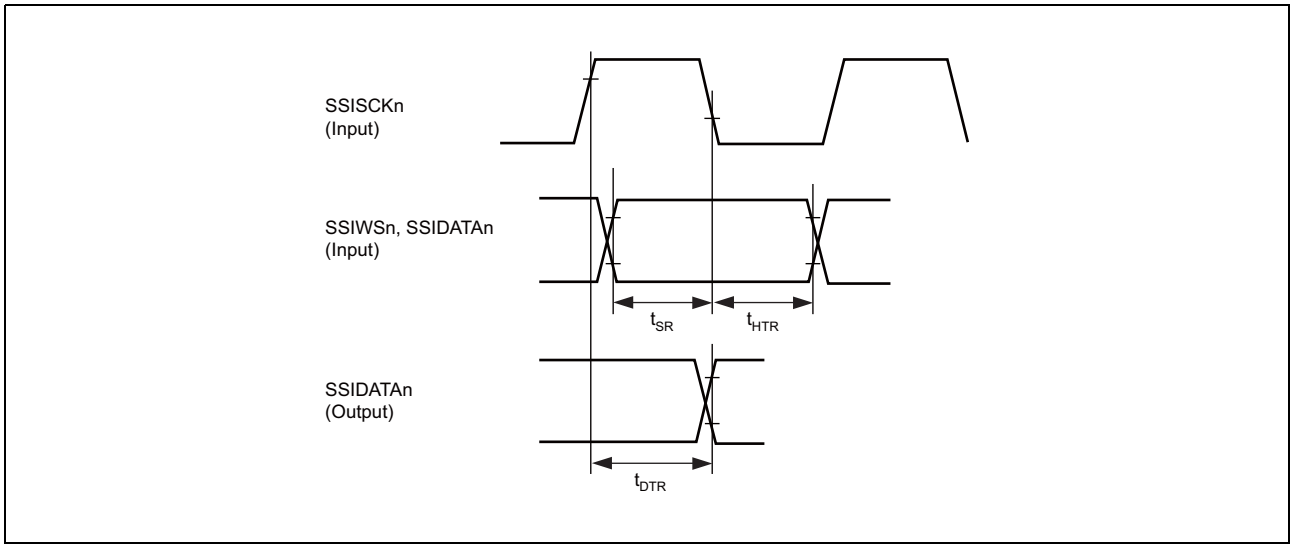
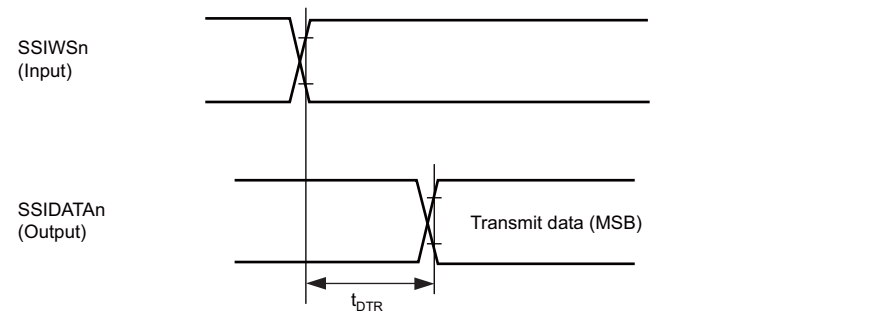


Figure 3.58 Transmission and Reception Timing (Slave, SSICR_n.SCKP = 1)



Note: MSB output timing of when either of the following condition a) or b) is satisfied in slave transmission.
a) SSICR_n.DEL = 1, SSICR_n.SDATA = 0
b) SSICR_n.DEL = 1, SSICR_n.SDATA = 1, with no padding bit

Figure 3.59 Transmission Timing (Slave, in Synchronization with SSIWSn)

3.4.13 Media Local Bus Timing

This module is only incorporated in the RZ/A1L.

Table 3.17 Media Local Bus Timing

Item	Symbol	Min.	Typ	Max.	Unit	Remarks	Figure
Input clock frequency (256 × FS)	f_I	11.2640	12.2880	12.3136	MHz		Figure 3.60
Input clock cycle (256 × FS)	t_I	—	81	—	ns		
Input clock high level (256 × FS)	t_{HC}	30	36.5	—	ns		
Input clock low level (256 × FS)	t_{LC}	30	35.5	—	ns		
Input clock frequency (512 × FS)	f_I	22.5280	24.5760	24.6272	MHz		
Input clock cycle (512 × FS)	t_I	—	40	—	ns		
Input clock high level (512 × FS)	t_{HC}	14	16.5	—	ns		
Input clock low level (512 × FS)	t_{LC}	14	16.5	—	ns		
Input clock frequency (1024 × FS)	f_I	45.0560	49.1520	49.2544	MHz		
Input clock cycle (1024 × FS)	t_I	—	20.3	—	ns		
Input clock high level (1024 × FS)	t_{HC}	9.3	10.2	—	ns		
Input clock low level (1024 × FS)	t_{LC}	6.1	7.3	—	ns		
Input clock rise time	t_{RC}	—	—	1	ns	V_{IL} to V_{IH}	
Input clock fall time	t_{FC}	—	—	1	ns	V_{IH} to V_{IL}	
Delay time (clock signal rising)	t_{DTR}	—	—	8.0	ns	Output load: 20 pF	
Delay time (clock signal falling)	t_{DTF}	0	—	t_{LC}	ns		
Setup time	t_{SR}	1	—	—	ns		
Hold time	t_{HTR}	2	—	—	ns		

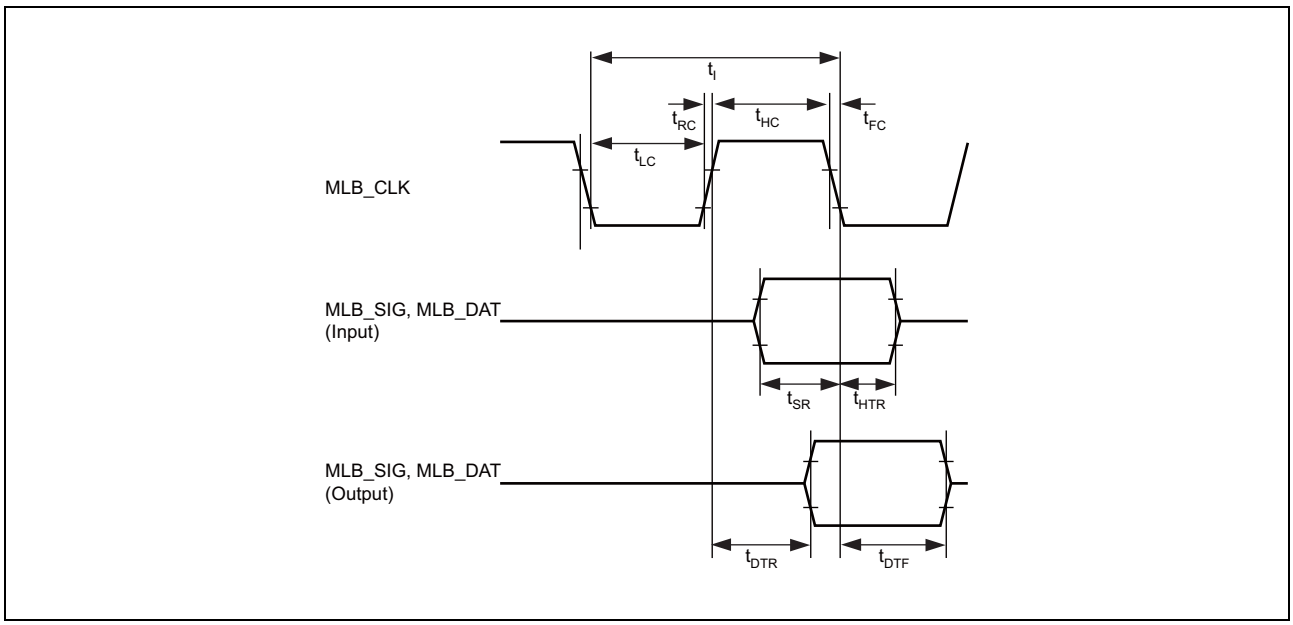


Figure 3.60 Interface Timing

3.4.14 CAN Interface Timing

Table 3.18 CAN Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
Internal delay time	tnode	—	100	ns	Figure 3.61
Transmission rate		—	1	Mbps	

Internal delay time (tnode) = Internal transfer delay time (toutput) + Internal receive delay time (tinput)

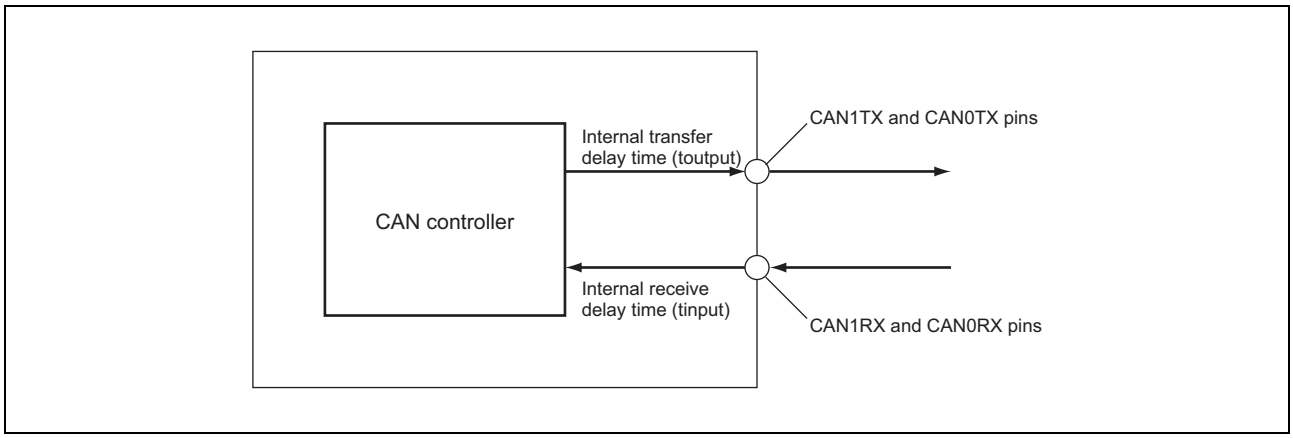


Figure 3.61 CAN Interface Condition

3.4.15 Ethernet Controller and EthernetAVB Timing

The EthernetAVB is only incorporated in the RZ/A1LU.

Table 3.19 Ethernet Controller and EthernetAVB Timing

Item	Symbol	Min.	Max.	Unit	Figure
ET_TXCLK cycle time	t_{Tcyc}	40	—	ns	Figure 3.62, Figure 3.63, Figure 3.64, Figure 3.65, and Figure 3.66
ET_TXCLK high level width	t_{TCKWH}	0.35 × t_{Tcyc}	—	ns	
ET_TXCLK low level width	t_{TCKWL}	0.35 × t_{Tcyc}	—	ns	
ET_TXEN output delay time	t_{TEND}	0	25	ns	
ET_TXD[3:0] output delay time	t_{TDD}	0	25	ns	
ET_RXCLK cycle time	t_{Rcyc}	40	—	ns	
ET_RXCLK high level width	t_{RCKWH}	0.35 × t_{Rcyc}	—	ns	
ET_RXCLK low level width	t_{RCKWL}	0.35 × t_{Rcyc}	—	ns	
ET_RXDV setup time	t_{RDVS}	10	—	ns	
ET_RXDV hold time	t_{RDVH}	10	—	ns	
ET_RXD[3:0] setup time	t_{RDDS}	10	—	ns	
ET_RXD[3:0] hold time	t_{RDDH}	10	—	ns	
ET_RXER setup time	t_{RERS}	10	—	ns	
ET_RXER hold time	t_{RERH}	10	—	ns	
AVB_GPTP_EXTERN cycle time (RZ/A1LU only)	t_{Gcyc}	40	—	ns	
AVB_GPTP_EXTERN high level width (RZ/A1LU only)	t_{GCKWH}	0.35 × t_{Gcyc}	—	ns	
AVB_GPTP_EXTERN low level width (RZ/A1LU only)	t_{GCKWL}	0.35 × t_{Gcyc}	—	ns	
AVB_CAPTURE high level width (RZ/A1LU only)	t_{CAPWH}	2 × t_{Ccyc}*	—	ns	

Note: * This is the cycle time of the clock selected by the CSEL bit in the AVB-DMAC mode register (CCC).

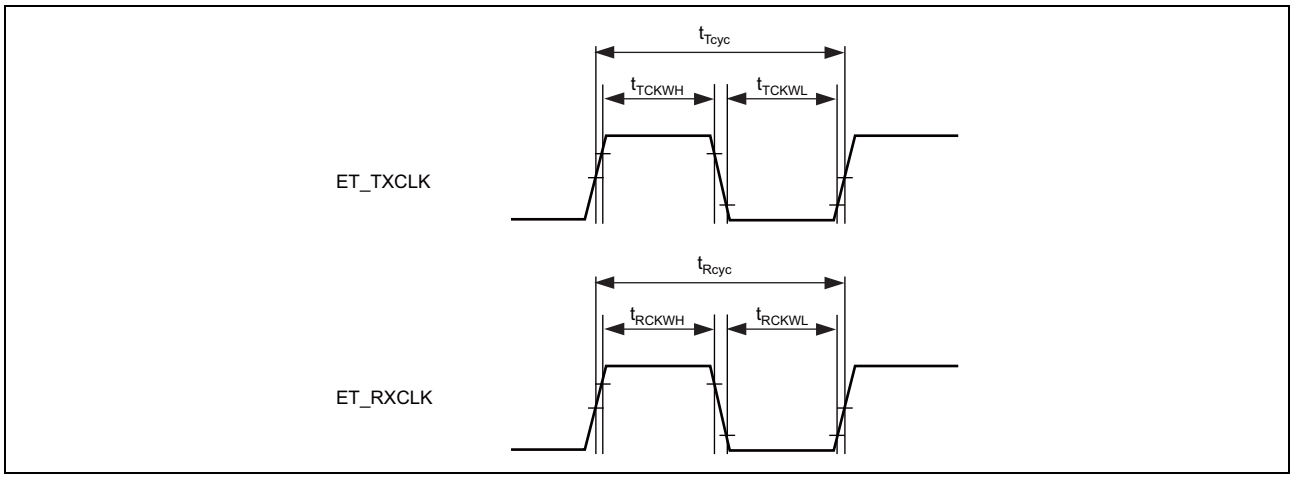


Figure 3.62 MII Clock Timing

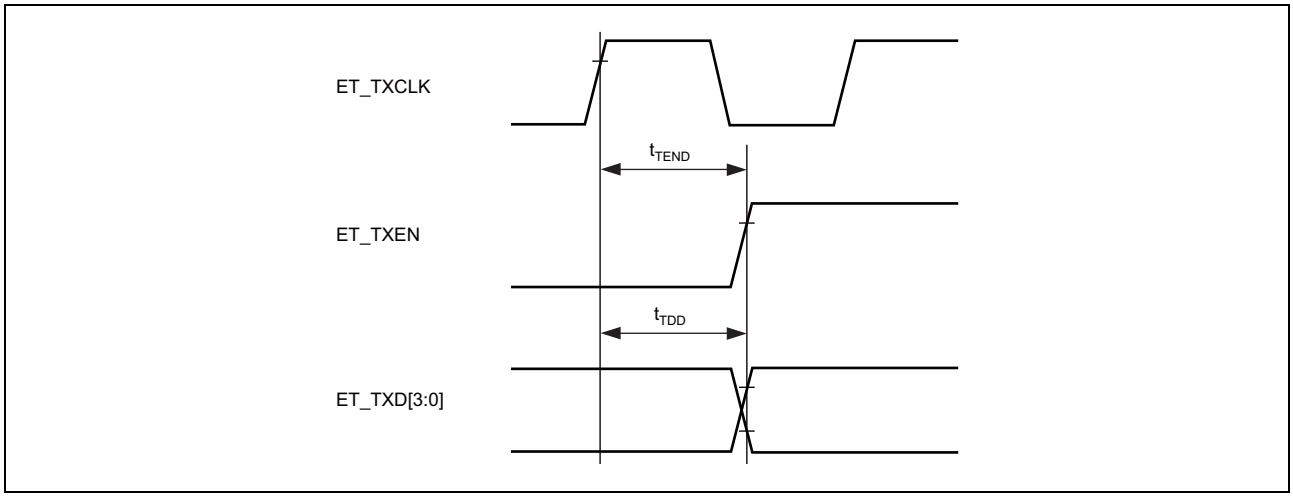


Figure 3.63 MII Transmit Data Timing

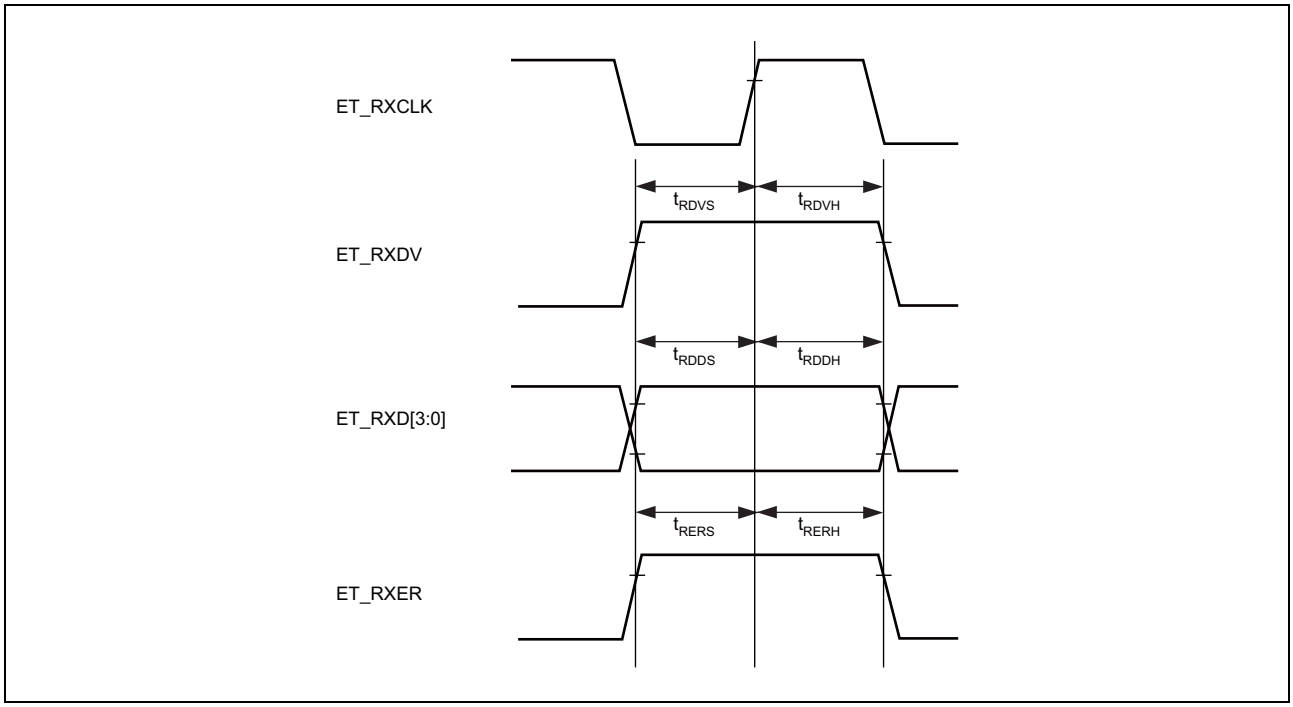


Figure 3.64 MII Receive Data Timing

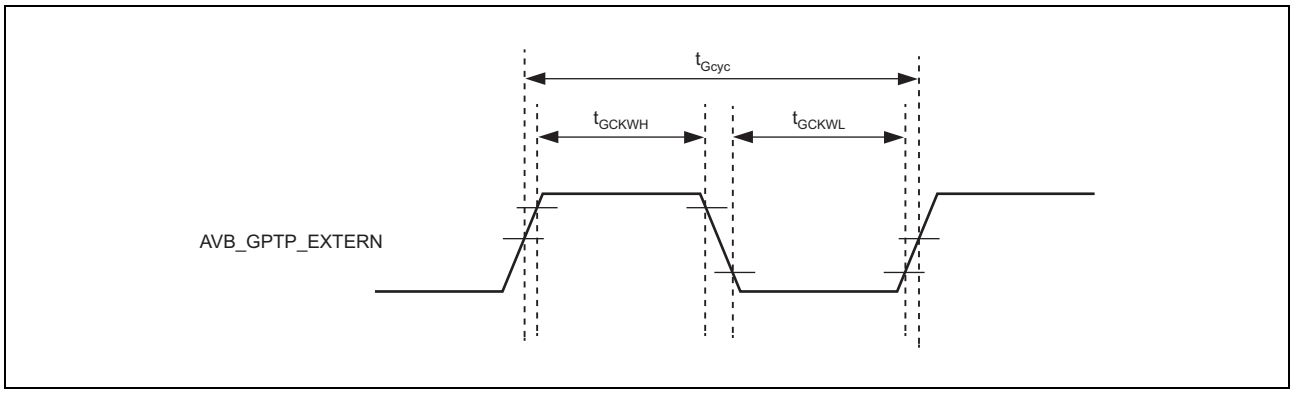


Figure 3.65 gPTP Timer External Clock Timing

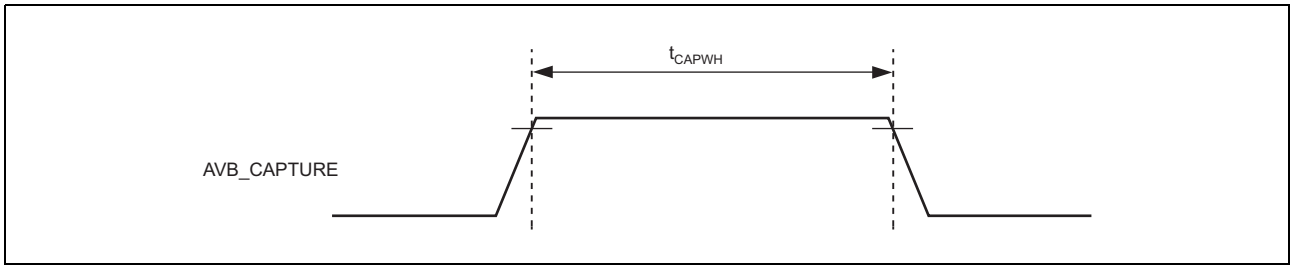


Figure 3.66 Timer Capture Signal Timing

3.4.16 A/D Converter Timing

Table 3.20 A/D Converter Timing

Module	Item	Symbol	Min.	Max.	Unit	Figure
A/D converter	Trigger input setup time	t_{TRGS}	17	—	ns	Figure 3.67

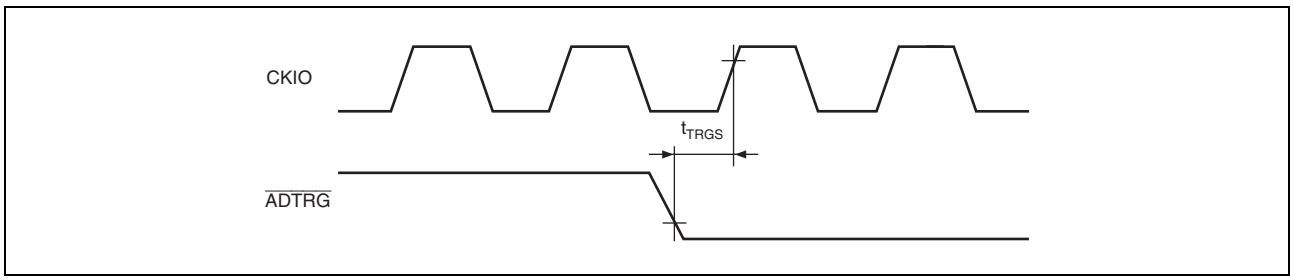


Figure 3.67 A/D Converter External Trigger Input Timing

3.4.17 USB 2.0 Host/Function Module Timing

Table 3.21 USB Transceiver Timing (Low-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{LR}	75	300	ns	Figure 3.68
Fall time	t_{LF}	75	300	ns	
Rise/fall time lag	t_{LR}/t_{LF}	80	125	%	

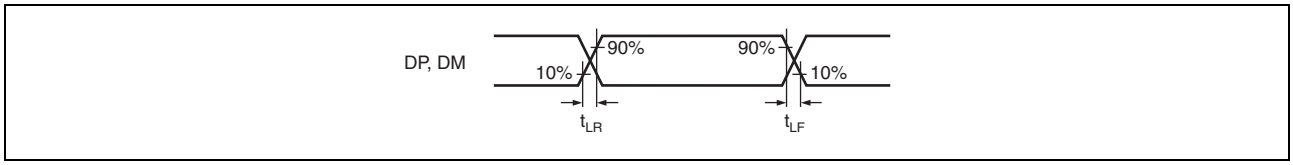


Figure 3.68 DP1, DP0, DM1, and DM0 Output Timing (Low-Speed)

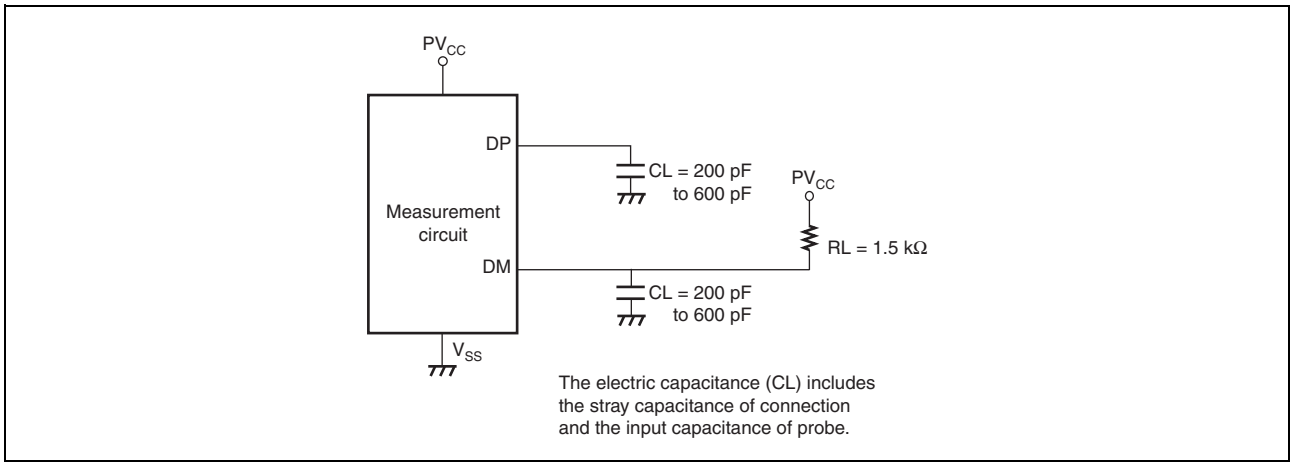


Figure 3.69 Measurement Circuit (Low-Speed)

Table 3.22 USB Transceiver Timing (Full-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{FR}	4	20	ns	Figure 3.70
Fall time	t_{FF}	4	20	ns	
Rise/fall time lag	t_{FR}/t_{FF}	90	111.11	%	

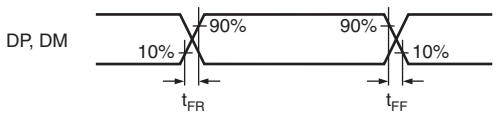
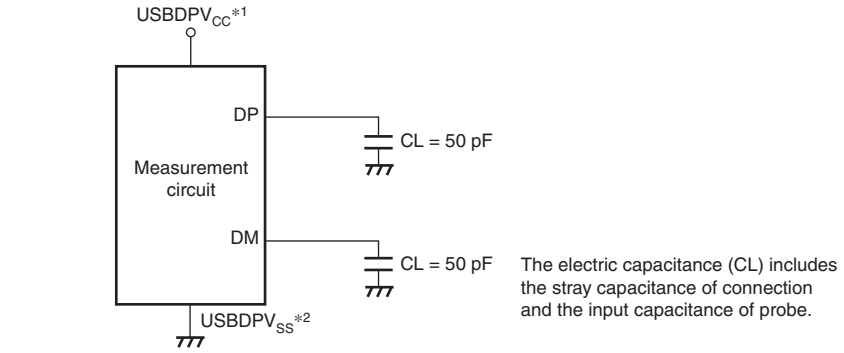


Figure 3.70 DP1, DP0, DM1, and DM0 Output Timing (Full-Speed)



Note 1. The PVcc pin is used in the products in BGA packages.
Note 2. The Vss pin is used in the products in BGA packages.

Figure 3.71 Measurement Circuit (Full-Speed)

Table 3.23 USB Transceiver Timing (High-Speed)

Item	Symbol	Min.	Max.	Unit	Figure
Rise time	t_{HSR}	500	—	ps	Figure 3.72
Fall time	t_{HSF}	500	—	ps	
Output driver resistance	Z_{HSDRV}	40.5	49.5	Ω	

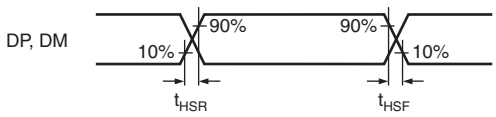
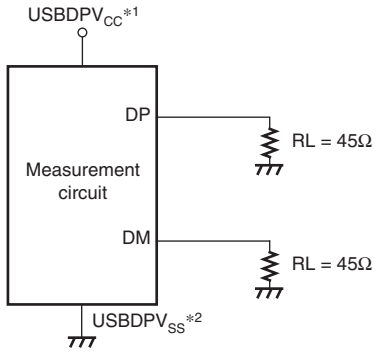


Figure 3.72 DP1, DP0, DM1, and DM0 Output Timing (High-Speed)



Note 1. The PVcc pin is used in the products in BGA packages.
Note 2. The Vss pin is used in the products in BGA packages.

Figure 3.73 Measurement Circuit (High-Speed)

3.4.18 Video Display Controller 5 Timing

Table 3.24 Video Display Controller 5 Timing

Item	Symbol	Min.	Max.	Unit	Figure
DV0_CLK input clock frequency	t_{Dcyc}	—	87.00	MHz	Figure 3.74
DV0_CLK input clock low pulse width	t_{WIL}	0.4	—	t_{Dcyc}	
DV0_CLK input clock high pulse width	t_{WIH}	0.4	—		
CD0_EXTCLK input clock frequency	t_{Ecyc}	—	87.00	MHz	
LCD0_EXTCLK input clock low pulse width	t_{WIL}	0.4	—	t_{Ecyc}	
LCD0_EXTCLK input clock high pulse width	t_{WIH}	0.4	—		
LCD0_CLK output clock frequency	t_{Lcyc}	—	87.00	MHz	Figure 3.75
LCD0_CLK clock output low pulse width*1	t_{LOL}	t_{WIL} - 0.95	t_{WIL} + 0.95	ns	
LCD0_CLK clock output high pulse width*1	t_{LOH}	t_{WIH} - 0.95	t_{WIH} + 0.95	ns	
LCD0_CLK clock output low pulse width*2	t_{LOL}	$t_{Lcyc}/2$ - 1.06	$t_{Lcyc}/2$ + 1.06	ns	
LCD0_CLK clock output high pulse width*2	t_{LOH}	$t_{Lcyc}/2$ - 1.06	$t_{Lcyc}/2$ + 1.06	ns	
LCD0_CLK clock output rise time	t_{LOR}	—	3	ns	
LCD0_CLK clock output fall time	t_{LOF}	—	3	ns	
Input data setup time	t_{VS}	2	—	ns	Figure 3.76
Input data hold time	t_{VH}	4	—	ns	
Output data delay time	t_{DD}	–3	3	ns	Figure 3.77

Note 1. This is the case when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.
Note 2. This is for cases other than when the video image clock or an external clock is selected as the clock for frequency division and the division ratio is set to 1/1.

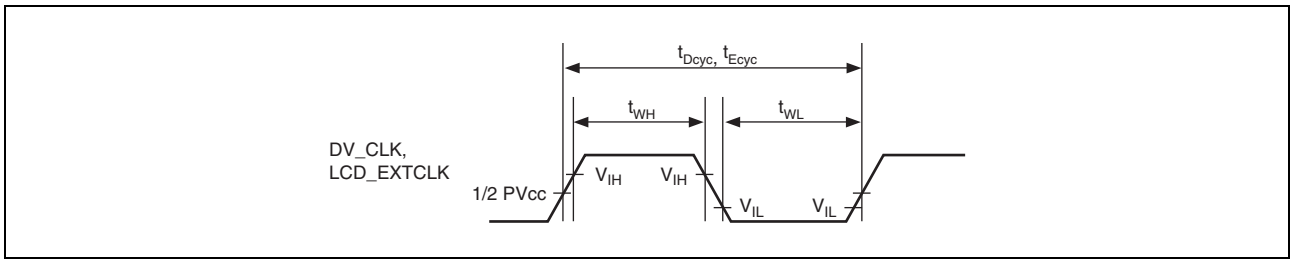


Figure 3.74 DV0_CLK and LCD0_EXTCLK Clock Input Timing

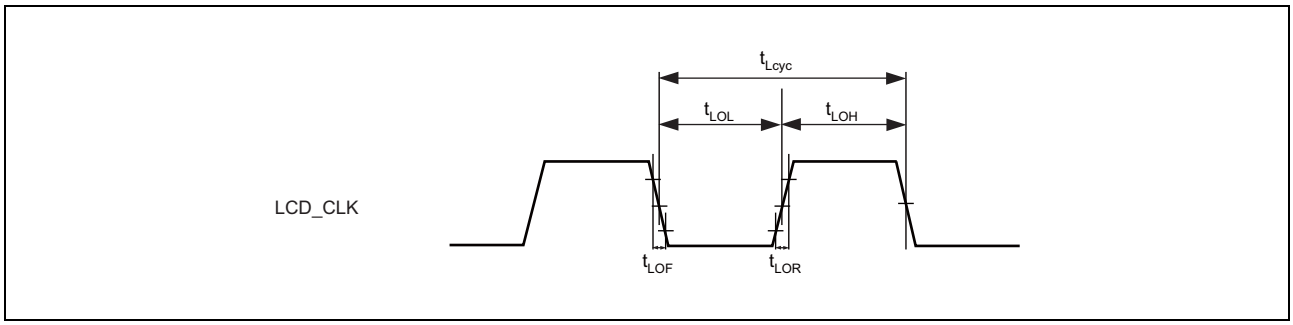


Figure 3.75 LCD0_CLK Clock Output Timing

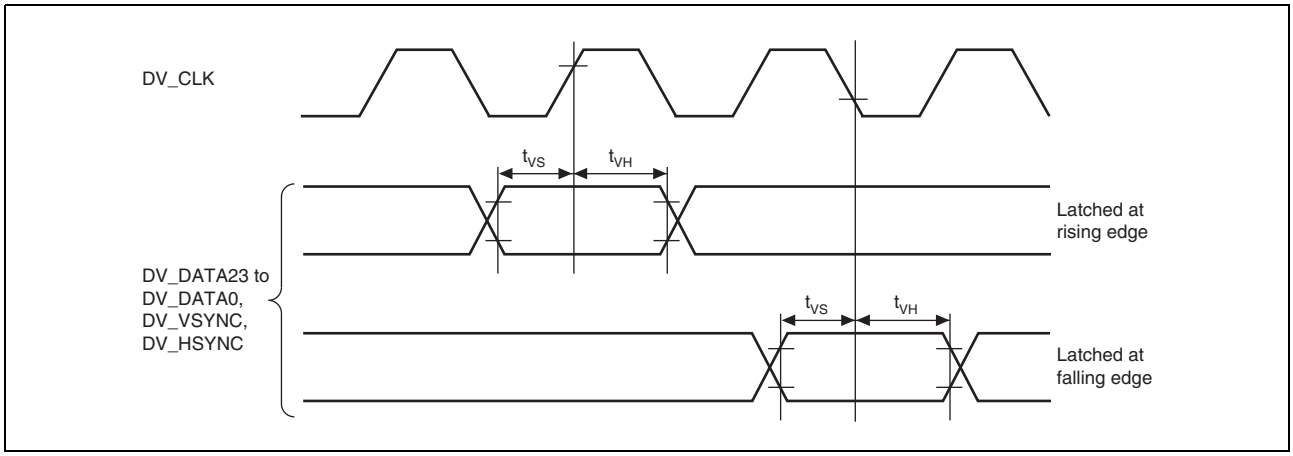


Figure 3.76 Video Input Timing

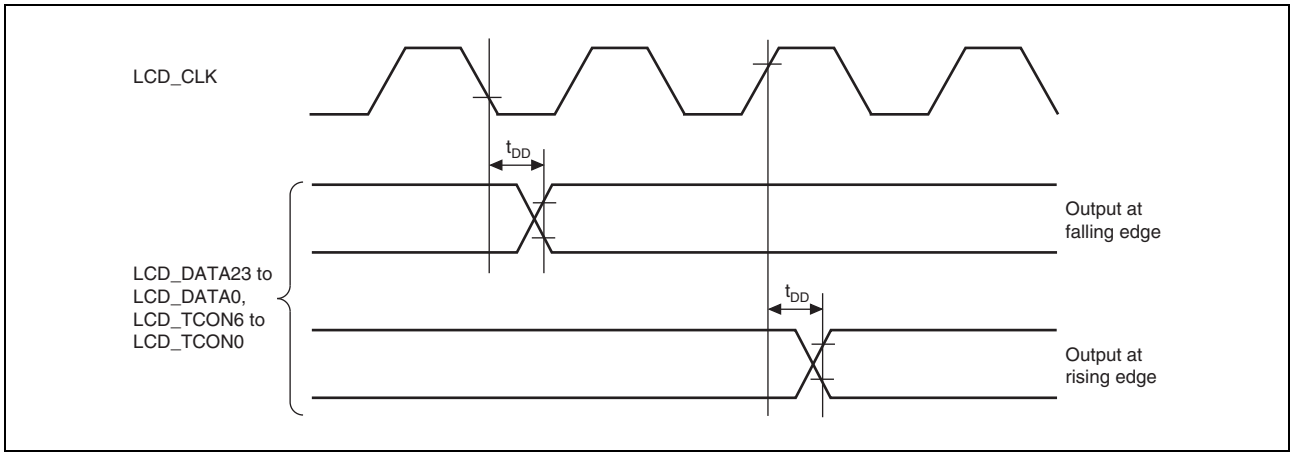


Figure 3.77 Display Output Timing

3.4.19 Capture Engine Unit Module Signal Timing

Table 3.25 Capture Engine Unit Module Signal Timing

Item	Symbol	Min.	Max.	Unit	Figure
Vertical sync (VIO_VD) setup time (when data is captured at the rising edges of the camera clock)	t_{VVDS}	2	—	ns	Figure 3.78 (1) and Figure 3.78 (2)
Vertical sync (VIO_VD) setup time (when data is captured at the falling edges of the camera clock) (RZ/A1LU and RZ/A1LC only)	t_{VVDS}	2.5	—	ns	
Vertical sync (VIO_VD) hold time	t_{VVDH}	3.5	—	ns	
Horizontal sync (VIO_HD) setup time (when data is captured at the rising edges of the camera clock)	t_{VHDS}	2	—	ns	
Horizontal sync (VIO_HD) setup time (when data is captured at the falling edges of the camera clock) (RZ/A1LU and RZ/A1LC only)	t_{VHDS}	2.5	—	ns	
Horizontal sync (VIO_HD) hold time	t_{VHDH}	3.5	—	ns	
Capture image data (VIO_D) setup time (when data is captured at the rising edges of the camera clock)	t_{VDTS}	2	—	ns	
Capture image data (VIO_D) setup time (when data is captured at the falling edges of the camera clock) (RZ/A1LU and RZ/A1LC only)	t_{VDTS}	2.5	—	ns	
Capture image data (VIO_D) hold time	t_{VDTH}	3.5	—	ns	
Camera clock cycle	t_{VCYC}	—	87	MHz	
Camera clock high level	t_{VHW}	0.4 × t_{VCYC}	—	ns	
Camera clock low level	t_{VLW}	0.4 × t_{VCYC}	—	ns	
Field identification signal (VIO_FLD) setup time (when data is captured at the rising edges of the camera clock)	t_{VFDS}	2	—	ns	
Field identification signal (VIO_FLD) setup time (when data is captured at the falling edges of the camera clock) (RZ/A1LU and RZ/A1LC only)	t_{VFDS}	2.5	—	ns	
Field identification signal (VIO_FLD) hold time	t_{VFDH}	3.5	—	ns	

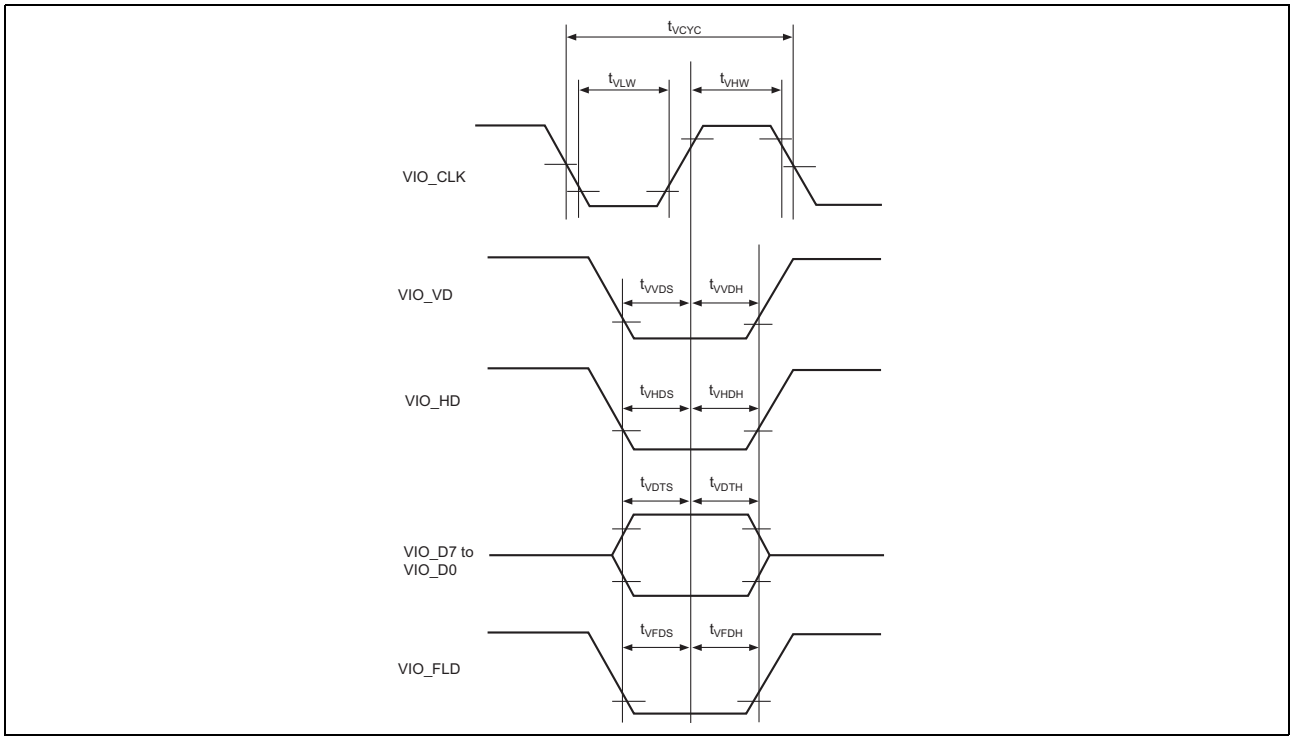


Figure 3.78 (1) Capture Engine Unit Module Signal Timing when Data is Captured at the Rising Edges of VIO_CLK

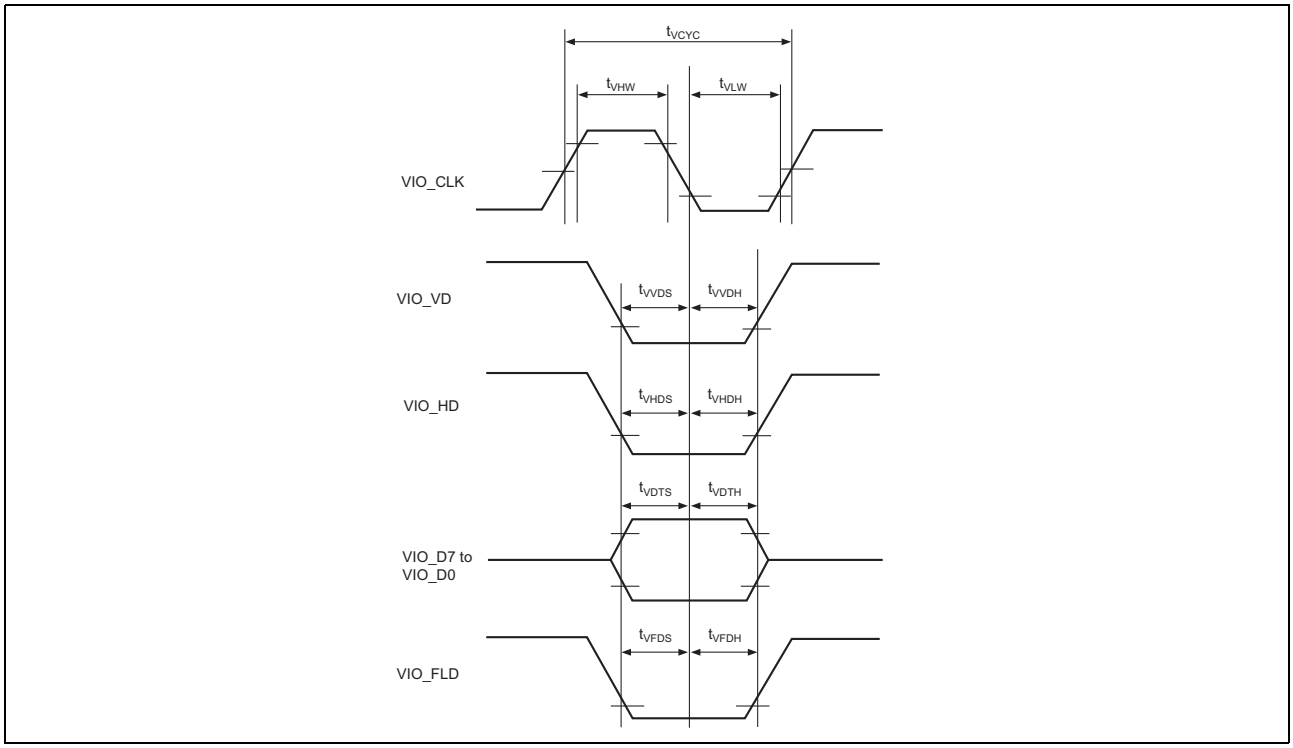


Figure 3.78 (2) Capture Engine Unit Module Signal Timing when Data is Captured at the Falling Edge of VIO_CLK (RZ/A1LU and RZ/A1LC Only)

3.4.20 SD Host Interface Timing

Table 3.26 SD Host Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
SD_CLK clock cycle	t_{SDPP}	2 × t_{p1cyc}	—	ns	Figure 3.79
SD_CLK clock high level width	t_{SDWH}	0.4 × t_{SDPP}	—	ns	
SD_CLK clock low level width	t_{SDWL}	0.4 × t_{SDPP}	—	ns	
SD_CLK clock rise time	t_{SDLH}	—	3	ns	
SD_CLK clock fall time	t_{SDHL}	—	3	ns	
SD_CMD, SD_D3 to SD_D0 output data delay time (data transfer mode)	t_{SDODLY}	—	4	ns	
SD_CMD, SD_D3 to SD_D0 input data setup time	t_{SDISU}	5	—	ns	
SD_CMD, SD_D3 to SD_D0 input data hold time	t_{SDIH}	2	—	ns	

Note: • t_{p1cyc} indicates peripheral clock 1 (P1ϕ) cycle.

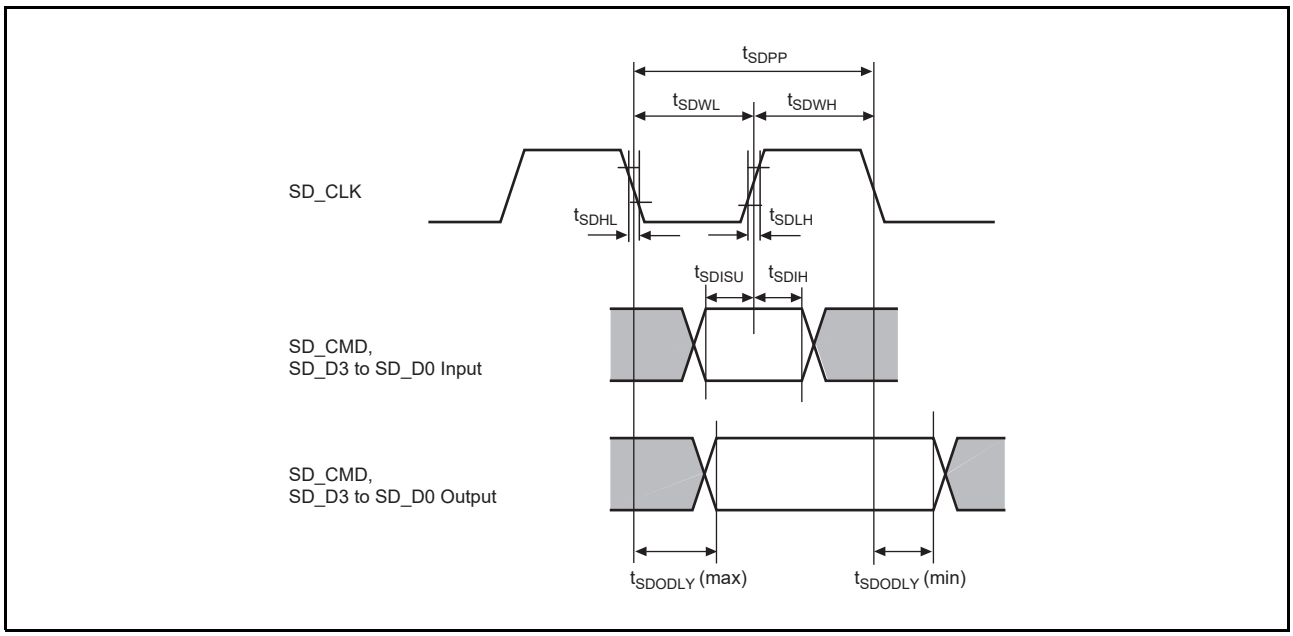


Figure 3.79 SD Host Interface

3.4.21 MMC Host Interface Timing

Table 3.27 MMC Host Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
MMC_CLK clock cycle	t_{MMCPP}	2 × t_{p1cyc}	—	ns	Figure 3.80
MMC_CLK clock high level width	t_{MMCWH}	6.5	—	ns	
MMC_CLK clock low level width	t_{MMCWL}	6.5	—	ns	
MMC_CLK clock rise time	t_{MMCLH}	—	3	ns	
MMC_CLK clock fall time	t_{MMCHL}	—	3	ns	
MMC_CMD, MMC_D7 to MMC_D0 output data delay time (data transfer mode)	$t_{MMCODLY}$	– 6.5	6.5	ns	
MMC_CMD, MMC_D7 to MMC_D0 input data setup time	t_{MMCISU}	4.5	—	ns	
MMC_CMD, MMC_D7 to MMC_D0 input data hold time	t_{MMCIH}	2	—	ns	

Note: • t_{p1cyc} indicates peripheral clock 1 (P1ϕ) cycle.

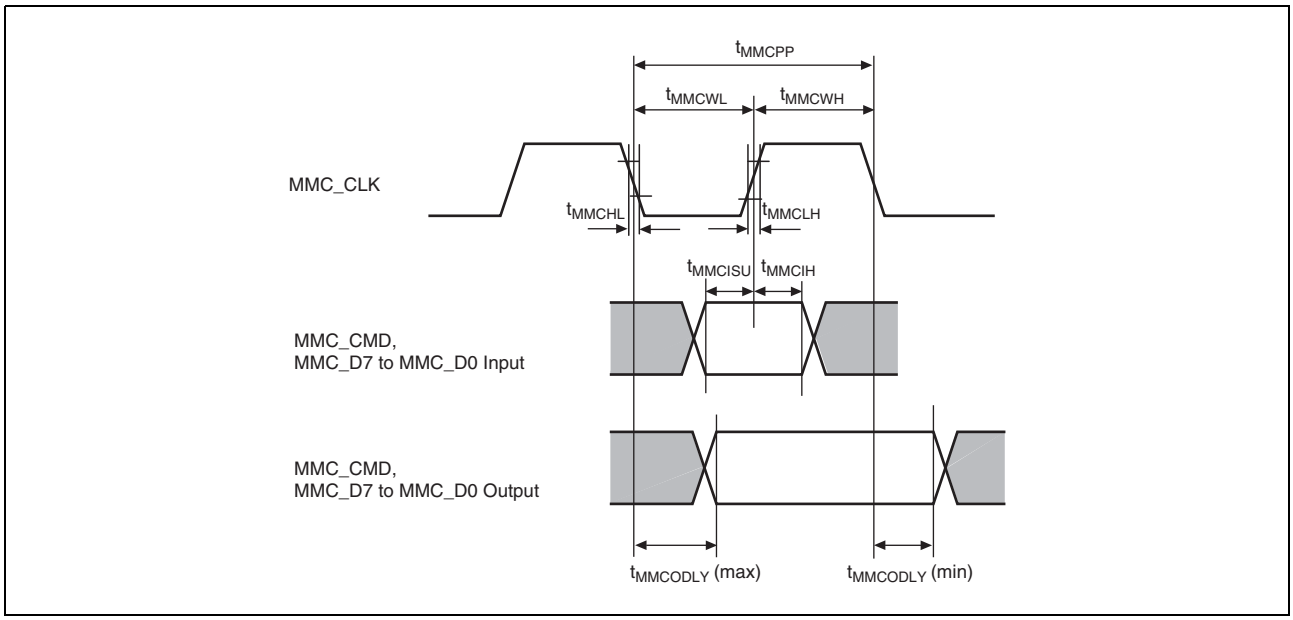


Figure 3.80 MMC Interface

3.4.22 General Purpose I/O Ports Timing

Table 3.28 General Purpose I/O Ports Timing

Item	Symbol	Min.	Max.	Unit	Figure
Output data delay time	t_{PORTD}	—	100	ns	Figure 3.81
Input data setup time	t_{PORTS}	100	—		
Input data hold time	t_{PORTH}	100	—		

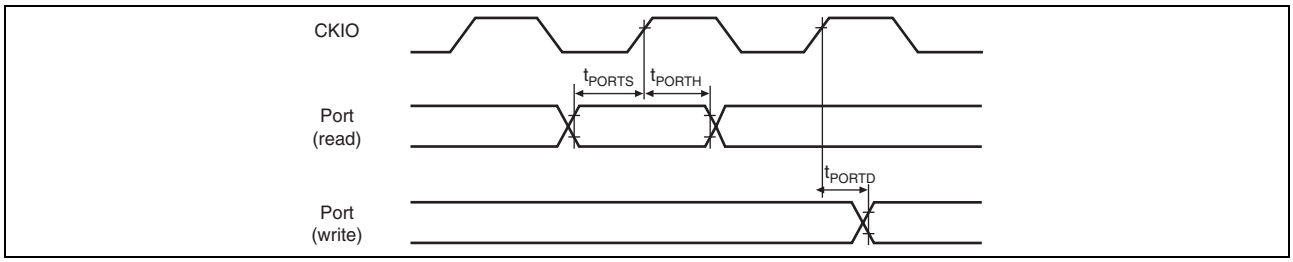


Figure 3.81 General I/O Ports Timing

3.4.23 Debugger Interface Timing

Table 3.29 Debugger Interface Timing

Item	Symbol	Min.	Max.	Unit	Figure
TCK cycle time	t_{TCKcyc}	50*1	—	ns	Figure 3.82
TCK high pulse width	t_{TCKH}	0.4	0.6	t_{TCKcyc}	
TCK low pulse width	t_{TCKL}	0.4	0.6	t_{TCKcyc}	
TDI setup time	t_{TDIS}	10	—	ns	Figure 3.83
TDI hold time	t_{TDIH}	10	—	ns	
TMS/SWDIO setup time	t_{TMSS}	10	—	ns	
TMS/SWDIO hold time	t_{TMSH}	10	—	ns	
SWDIO delay time	t_{SWDO}	—	16	ns	
TDO delay time	t_{TDOD}	—	16	ns	
Capture register setup time	t_{CAPTS}	10	—	ns	Figure 3.84
Capture register hold time	t_{CAPTH}	10	—	ns	
Update register delay time	$t_{UPDATED}$	—	20	ns	
Trace clock cycle	t_{TCYC}	30*2	—	ns	Figure 3.85 Output load: 15 pF
Trace clock high level	t_{THC}	12	—	ns	
Trace clock low level	t_{TLC}	12	—	ns	
Trace data delay time	t_{TDT}	3	$0.3 \times t_{TCYC} + 3$	ns	

Note 1. Should be greater than the peripheral clock 0 (P0ϕ) cycle time.
Note 2. Generated by dividing the frequency of the peripheral clock (P1ϕ) by 2.

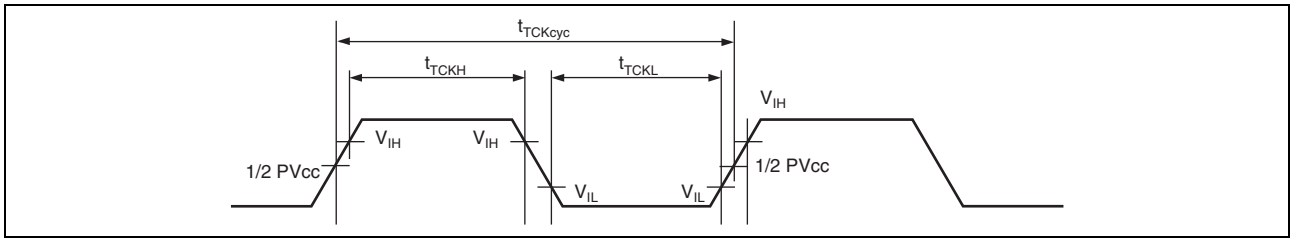


Figure 3.82 TCK Input Timing

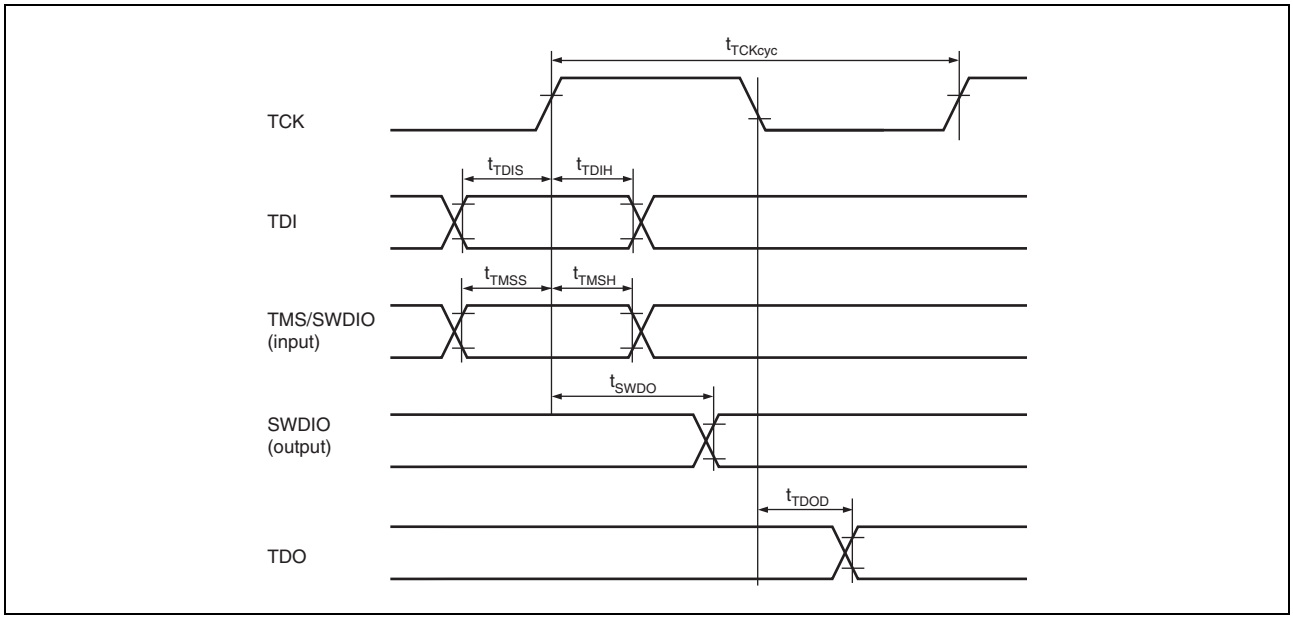


Figure 3.83 Data Transfer Timing

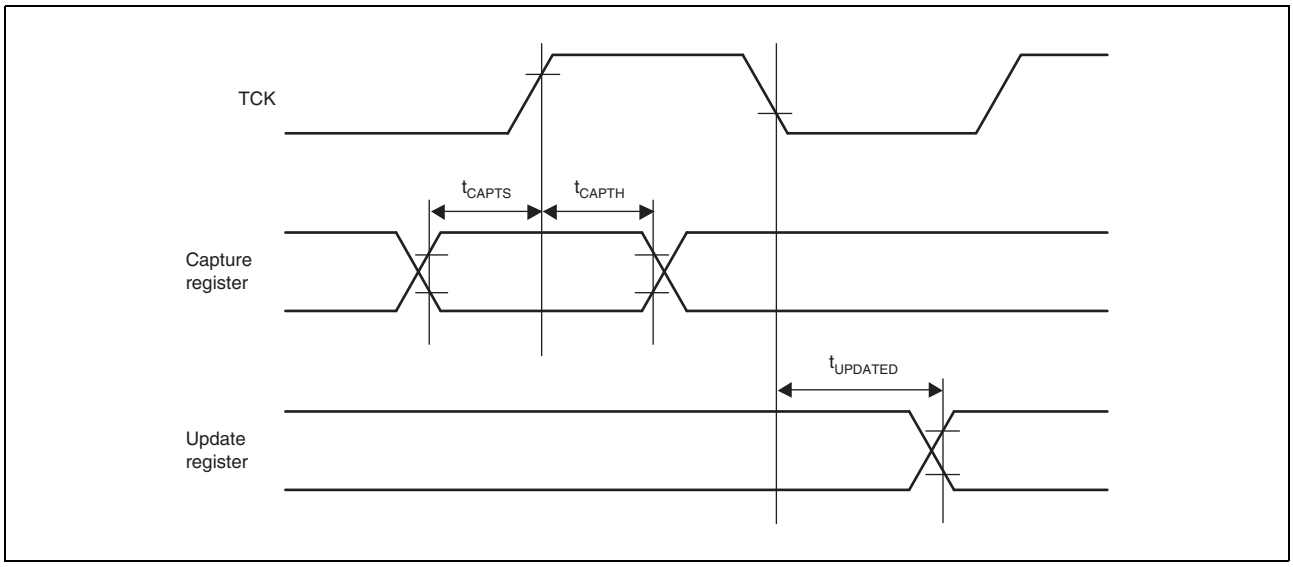


Figure 3.84 Boundary Scan Input/Output I/O Timing

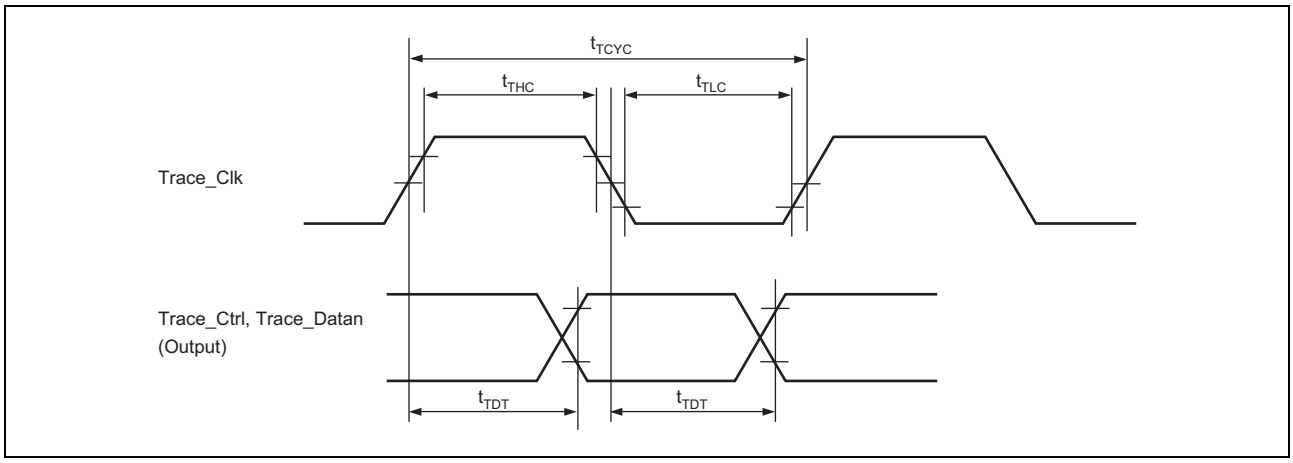
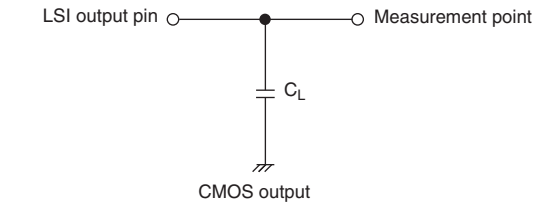


Figure 3.85 Trace Interface Timing

3.4.24 AC Characteristics Measurement Conditions

- I/O signal reference level: $PV_{CC}/2$, the minimum values of V_{IH}, V_{T+}, and V_{OH}, and the maximum values of V_{IL}, V_{T-}, and V_{OL} (refer to the individual timing chart)
- Input pulse level: PV_{CC}
- Input rise and fall times: 1 ns



Note: C_L is the total value that includes the capacitance of measurement tools.
C_L = 30 pF

Figure 3.86 Output Load Circuit

3.5 A/D Converter Characteristics

Conditions: V_{CC} = $USBDV_{CC}$ = $USBUV_{CC}$ = 1.10 to 1.26 V, PV_{CC} = $USBDPV_{CC}$ = 3.0 to 3.6 V,
$PLLV_{CC}$ = 1.10 to 1.26 V, AV_{CC} = 3.0 to 3.6 V, $USBAPV_{CC}$ = 3.0 to 3.6 V, $USBAV_{CC}$ = 1.10 to 1.26 V,
V_{SS} = AV_{SS} = $USBDV_{SS}$ = $USBAV_{SS}$ = $USBDPV_{SS}$ = $USBAPV_{SS}$ = $USBUV_{SS}$ = 0 V,
Ta = –40 to 85 °C

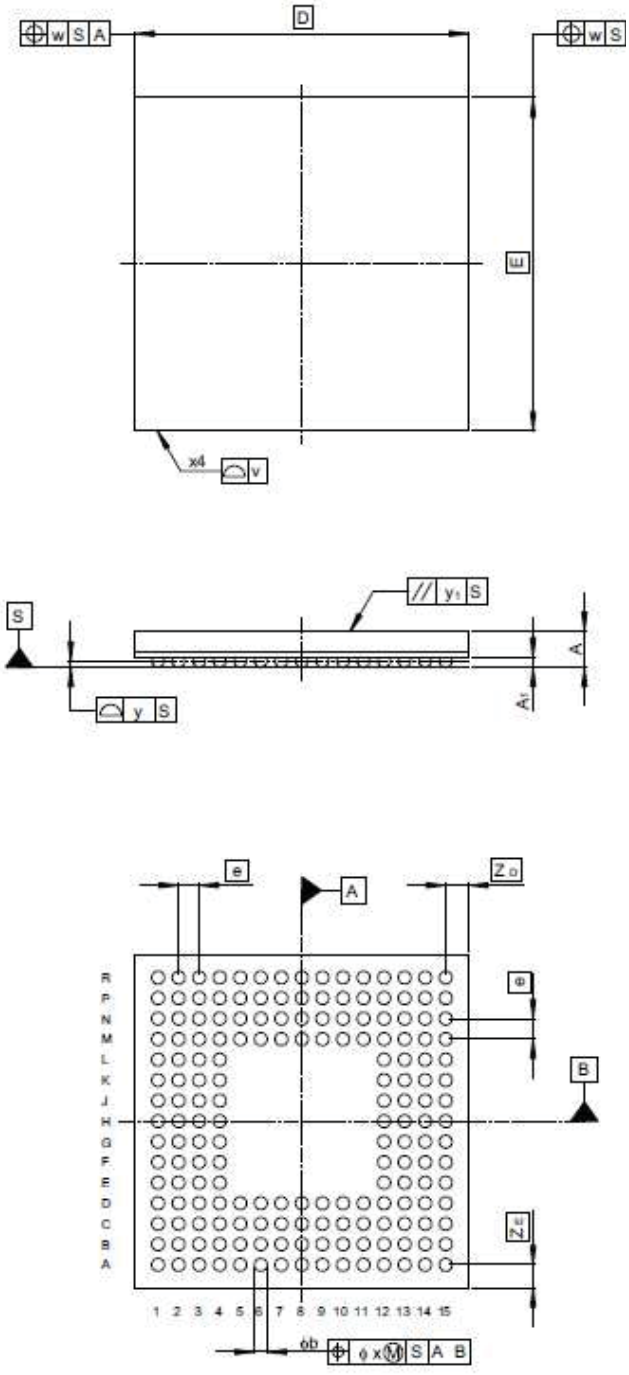
Note: Products in BGA packages do not have $USBDV_{CC}$, $USBUV_{CC}$, $USBDPV_{CC}$, $USBDV_{SS}$, $USBAV_{SS}$, $USBDPV_{SS}$, $USBAPV_{SS}$, and $USBUV_{SS}$ pins.

Table 3.30 A/D Converter Characteristics

Item		Min.	Typ.	Max.	Unit
Resolution		12	12	12	bits
Conversion time	12-bit	5	—	—	μs
	10-bit				
Analog input capacitance		—	—	20	pF
Permissible signal-source impedance		—	—	3	kΩ
DNL	12-bit	—	—	±1.0	LSB
	10-bit	—	—	±1.0	LSB
INL	12-bit	—	—	±4.0	LSB
	10-bit	—	—	±4.0	LSB
Offset error	12-bit	—	—	±8.0	LSB
	10-bit	—	—	±2.0	LSB
Full-scale error	12-bit	—	—	±8.0	LSB
	10-bit	—	—	±2.0	LSB
Absolute accuracy	12-bit	—	—	±11.0	LSB
	10-bit	—	—	±5.0	LSB

4. Package Dimensions

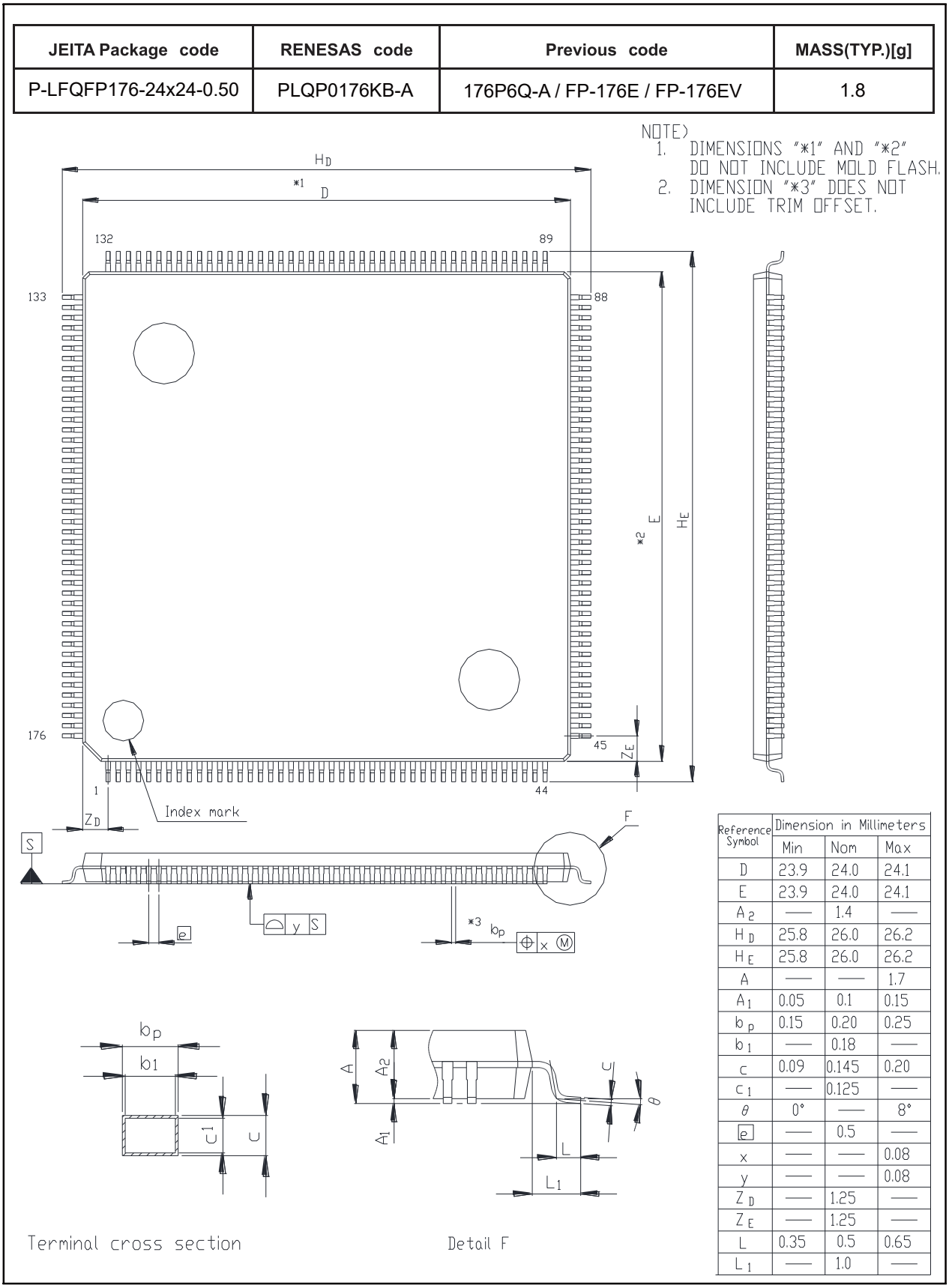
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFBGA176-8x8-0.50	PLBG0176KA-A	-	0.14



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	—	8.0	—
E	—	8.0	—
v	—	—	0.15
w	—	—	0.20
A	—	—	1.40
A_1	0.20	0.25	0.30
e	—	0.50	—
b	0.25	0.30	0.35
x	—	—	0.05
y	—	—	0.08
y_1	—	—	0.20
S_D	—	—	—
S_E	—	—	—
Z_D	—	0.50	—
Z_E	—	0.50	—

Figure 4.1 Dimensions of 176-Pin BGA Package

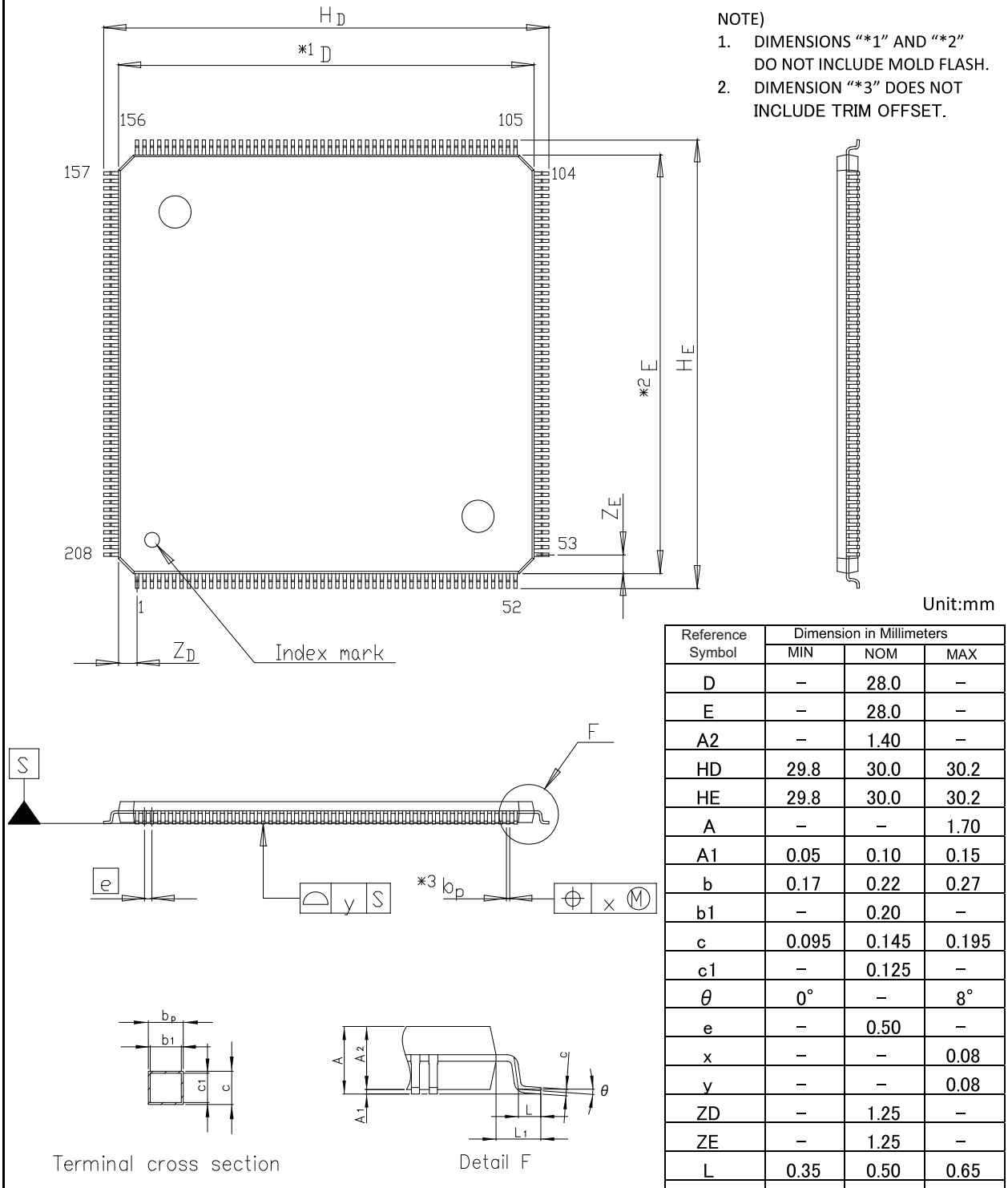
JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LFQFP176-24x24-0.50	PLQP0176KB-A	176P6Q-A / FP-176E / FP-176EV	1.8



Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	23.9	24.0	24.1
E	23.9	24.0	24.1
A_2	—	1.4	—
H_D	25.8	26.0	26.2
H_E	25.8	26.0	26.2
A	—	—	1.7
A_1	0.05	0.1	0.15
b_p	0.15	0.20	0.25
b_1	—	0.18	—
c	0.09	0.145	0.20
c_1	—	0.125	—
θ	0°	—	8°
e	—	0.5	—
x	—	—	0.08
y	—	—	0.08
Z_D	—	1.25	—
Z_E	—	1.25	—
L	0.35	0.5	0.65
L_1	—	1.0	—

Figure 4.2 Dimensions of 176-Pin QFP Package

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-LQFP208-2828-0.50	PLQP0208KB-A	-	2.7g



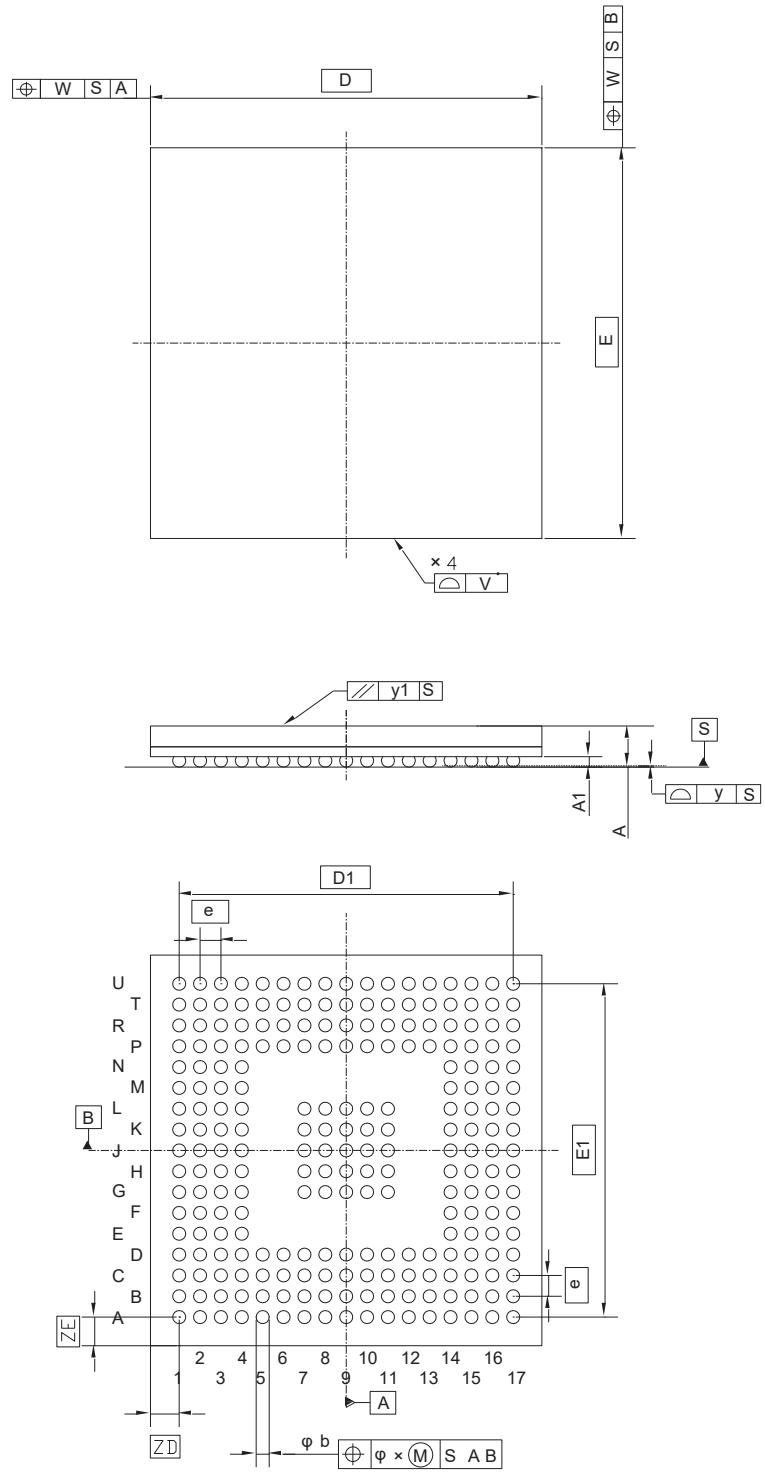
Unit:mm

Reference Symbol	Dimension in Millimeters		
	MIN	NOM	MAX
D	-	28.0	-
E	-	28.0	-
A2	-	1.40	-
HD	29.8	30.0	30.2
HE	29.8	30.0	30.2
A	-	-	1.70
A1	0.05	0.10	0.15
b	0.17	0.22	0.27
b1	-	0.20	-
c	0.095	0.145	0.195
c1	-	0.125	-
θ	0°	-	8°
e	-	0.50	-
x	-	-	0.08
y	-	-	0.08
ZD	-	1.25	-
ZE	-	1.25	-
L	0.35	0.50	0.65
L1	-	1.00	-

Figure 4.3 Dimensions of 208-Pin QFP Package (PLQP0208KB-A)

JEITA Package code	RENESAS code	Previous code	MASS(TYP.)[g]
P-FBGA233-15x15-0.80	PRBG0233GA-A	—	0.75

Unit:mm



Reference Symbol	Dimension in Millimeters		
	Min	Mon	Max
D	—	15.00	—
D1	—	12.80	—
E	—	15.00	—
E1	—	12.80	—
v	—	—	0.15
w	—	—	0.20
e	—	0.80	—
A	—	1.58	1.90
A1	0.30	0.35	0.40
b	0.49	0.54	0.59
x	—	—	0.08
y	—	—	0.10
y1	—	—	0.20
ZD	—	1.10	—
ZE	—	1.10	—

Figure 4.4 Dimensions of 233-Pin BGA Package

REVISION HISTORY	RZ/A1L Group, RZ/A1LU Group, RZ/A1LC Group Datasheet

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 25, 2024	—	First edition, issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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