SLG46108-EV

Extended Temperature Range GreenPAK Ultra-Small Programmable Mixed-Signal Matrix

The SLG46108-EV provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the IO pins, and the macrocells of the SLG46108-EV. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit.

Features

- Logic and mixed-signal circuits
- Highly versatile macrocells
- Four combinatorial look up tables (LUTs)
  - Two 2-bit LUTs
  - Two 3-bit LUTs
- Seven combination function macrocell
  - Two selectable D Flip-Flop/LATCHES (DFF) or 2-bit LUTs
  - Two selectable D Flip-Flop/LATCHES (DFF) or 3-bit LUTs
  - One selectable Pipe Delay or 3-bit LUT
    - Pipe Delay – 8 stage/2 output
  - One selectable counter/delay (CNT/DLY) or 4-bit LUT
  - One programmable delay/deglitch filter
- Three 8-bit counter/delay generators (CNT/DLY) with external clock/reset
- RC oscillator (RC OSC)
- Power-on reset (POR)
- 1.8 V (±5 %) to 5 V (±10 %) supply
- Operating temperature range: -40 °C to 105 °C
- RoHS compliant/Halogen-free
- Pb-free 8-pin STQFN: 1.0 mm x 1.2 mm x 0.55 mm, 0.4 mm pitch

Applications

- Personal computers and servers
- PC peripherals
- Consumer electronics
- Data communications equipment
- Automotive display clusters
- Handheld and portable electronics

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1. Block Diagram

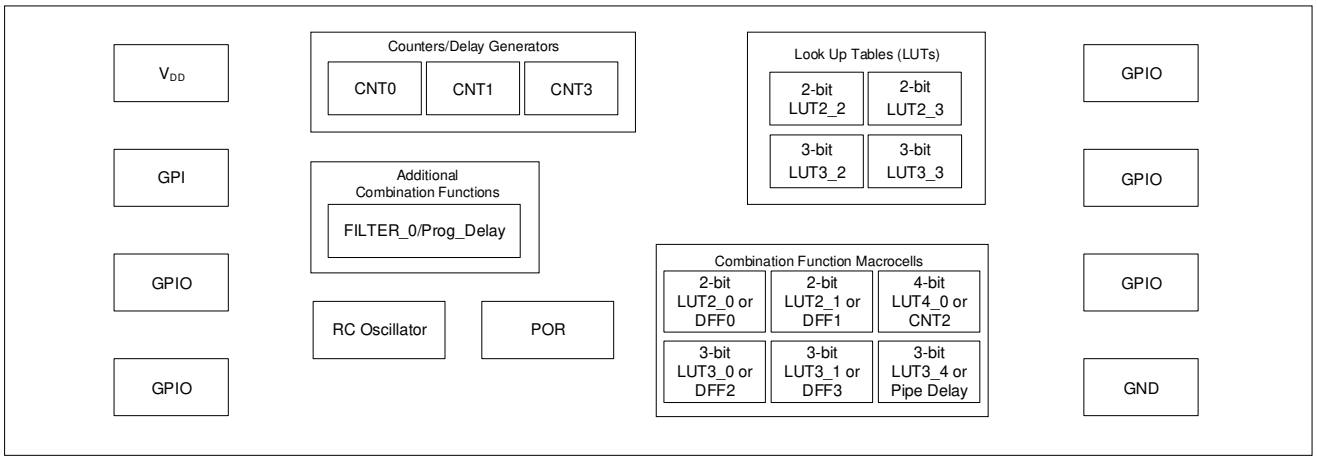


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

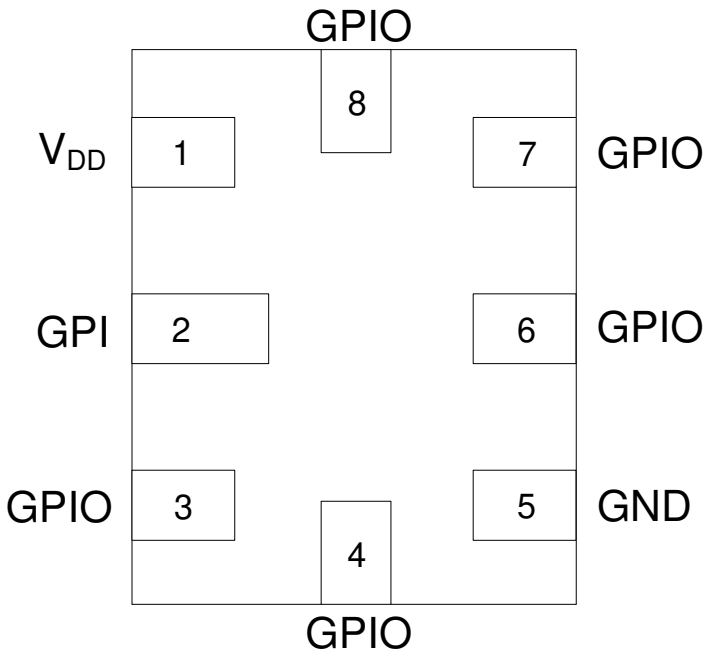


Figure 2. Pin Assignments - STQFN-8 (Top View)

2.2 Pin Descriptions

Table 1. Functional Pin Description

Pin Number	Pin Type	Function
1	V_{DD}	Power Supply
2	GPI	General Purpose Input
3	GPIO	General Purpose IO
4	GPIO	General Purpose IO
5	GND	GND
6	GPIO	General Purpose IO
7	GPIO	General Purpose IO
8	GPIO	General Purpose IO

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7.0	V
DC Input Voltage	GPIO	GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitivity Level		1		

3.2 Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		1.8	5.0	V
Operating Temperature		-40	105	°C
Maximal Voltage Applied to any Pin in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF

3.4 Electrical Specifications

3.4.1 Logic IO Characteristics

V_{DD} = 1.71 V to 1.89 V, T_A = -40 °C to +105 °C, Typical Values are at T_A = +25 °C, Unless Otherwise Noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		1.71	1.80	1.89	V
Quiescent Current	I_Q	Static inputs and outputs (when OSC is powered down and non-operational)	--	0.28	--	µA
Operating Temperature	T_A		-40	25	105	°C
High-level Input Voltage	V_{IH}	Logic input	1.043	--	V_{DD}	V
		Logic input with Schmitt trigger	1.231	--	V_{DD}	V
		Low-level logic input	0.873	--	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	--	--	0.753	V
		Logic input with Schmitt trigger	--	--	0.521	V
		Low-level logic input	--	--	0.528	V
Schmitt Trigger Hysteresis Voltage	V_{HYS}	Logic input with Schmitt Trigger,	0.353	0.460	0.590	V
Input Leakage (Absolute Value)	I_{LKG}		--	0.001	1	µA
High-level Output Voltage	V_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, I_{OH} = 100 µA	1.693	1.788	--	V
		Push-Pull 2x, Open-Darin PMOS 2x, I_{OH} = 100 µA	1.701	1.794	--	V
Low-level Output Voltage	V_{OL}	Push-Pull 1x, I_{OL} = 100 µA	--	0.010	0.015	V
		Push-Pull 2x, I_{OL} = 100 µA	--	0.005	0.007	V
		Open-Darin NMOS 1x, I_{OL} = 100 µA	--	0.005	0.007	V
		Open-Darin NMOS 2x, I_{OL} = 100 µA	--	0.003	0.004	V
High-level Output Current [1]	I_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, $V_{OH} = V_{DD}$ - 0.2	0.979	1.355	--	mA
		Push-Pull 2x, Open-Darin PMOS 2x, $V_{OH} = V_{DD}$ - 0.2	1.944	2.678	--	mA
Low-level Output Current [1]	I_{OL}	Push-Pull 1x, V_{OL} = 0.15 V	0.905	1.333	--	mA
		Push-Pull 2x, V_{OL} = 0.15 V	1.818	2.669	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.15 V	1.826	2.678	--	mA
		Open-Drain NMOS 2x, V_{OL} = 0.15 V	3.635	5.334	--	mA
Maximum Average or DC Current Through V_{DD} Pin (Per chip side [2])	I_{VDD}	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
Maximum Average or DC Current Through GND Pin (Per chip side [2])	I_{GND}	T_J = 85 °C	--	--	90	mA
		T_J = 110 °C	--	--	44	mA
Maximal Voltage Applied to any PIN in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	--	0.84	ms
Power-On Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.342	1.510	1.664	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Power-Off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.656	0.875	1.157	V
Pull-up or Pull-down Resistance	R_{PULL}	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
Decoupling Capacitor	C_{VDD}	Capacitor value at V_{DD}	--	0.1	--	µF

[1] DC or average current through any pin should not exceed value given in Absolute maximum conditions.
[2] The GreenPAK's power rails are divided into two sides. Pins 2,3, and 4 are connected to one side, pins 6,7, and 8 to another.

V_{DD} = 3 V to 3.6 V, T_A = -40 °C to +105 °C, Typical Values are at T_A = +25 °C, Unless Otherwise Noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		3.0	3.3	3.6	V
Quiescent Current	I_Q	Static inputs and outputs (when OSC is powered down and non-operational)	--	0.52	--	µA
Operating Temperature	T_A		-40	25	105	°C
High-level Input Voltage	V_{IH}	Logic input	1.793	--	V_{DD}	V
		Logic input with Schmitt trigger	2.119	--	V_{DD}	V
		Low-level logic input	1.050	--	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	--	--	1.289	V
		Logic input with Schmitt trigger	--	--	0.953	V
		Low-level logic input	--	--	0.659	V
Schmitt Trigger Hysteresis Voltage	V_{HYS}	Logic input with Schmitt Trigger,	0.530	0.704	0.873	V
Input Leakage (Absolute Value)	I_{LKG}		--	0.001	1.000	µA
High-level Output Voltage	V_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, I_{OH} = 3 mA	2.707	3.100	--	V
		Push-Pull 2x, Open-Darin PMOS 2x, I_{OH} = 3 mA	2.858	3.201	--	V
Low-level Output Voltage	V_{OL}	Push-Pull 1x, I_{OL} = 3 mA	--	0.179	0.267	V
		Push-Pull 2x, I_{OL} = 3 mA	--	0.088	0.129	V
		Open-Darin NMOS 1x, I_{OL} = 3 mA	--	0.088	0.129	V
		Open-Darin NMOS 2x, I_{OL} = 3 mA	--	0.044	0.065	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
High-level Output Current [1]	I_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, V_{OH} = 2.4 V	5.309	10.078	--	mA
		Push-Pull 2x, Open-Darin PMOS 2x, V_{OH} = 2.4 V	10.462	19.848	--	mA
Low-level Output Current [1]	I_{OL}	Push-Pull 1x, V_{OL} = 0.4 V	4.158	6.254	--	mA
		Push-Pull 2x, V_{OL} = 0.4 V	8.205	12.463	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V	8.357	12.505	--	mA
		Open-Drain NMOS 2x, V_{OL} = 0.4 V	16.572	24.718	--	mA
Maximum Average or DC Current Through V_{DD} Pin (Per chip side [2])	I_{VDD}	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
Maximum Average or DC Current Through GND Pin (Per chip side [2])	I_{GND}	T_J = 85 °C	--	--	90	mA
		T_J = 110 °C	--	--	44	mA
Maximal Voltage Applied to any PIN in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	--	0.84	ms
Power-On Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.342	1.510	1.664	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.656	0.875	1.157	V
Pull-up or Pull-down Resistance	R_{PULL}	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
Decoupling Capacitor	C_{VDD}	Capacitor value at V_{DD}	--	0.1	--	µF

[1] DC or average current through any pin should not exceed value given in Absolute maximum conditions.
[2] The GreenPAK's power rails are divided into two sides. Pins 2,3, and 4 are connected to one side, pins 6,7, and 8 to another.

V_{DD} = 4.5 V to 5.5 V, T_A = -40 °C to +105 °C, Typical Values are at T_A = +25 °C, Unless Otherwise Noted

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}		4.5	5.0	5.5	V
Quiescent Current	I_Q	Static inputs and outputs (when OSC is powered down and non-operational)	--	0.81	--	µA
Operating Temperature	T_A		-40	25	105	°C
High-level Input Voltage	V_{IH}	Logic input	2.655	--	V_{DD}	V
		Logic input with Schmitt trigger	3.153	--	V_{DD}	V
		Low-level logic input	1.147	--	V_{DD}	V
Low-level Input Voltage	V_{IL}	Logic input	--	--	1.944	V
		Logic input with Schmitt trigger	--	--	1.519	V
		Low-level logic input	--	--	0.749	V

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Schmitt Trigger Hysteresis Voltage	V_{HYS}	Logic input with Schmitt Trigger,	0.729	0.934	1.167	V
Input Leakage (Absolute Value)	I_{LKG}		--	0.001	1	µA
High-level Output Voltage	V_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, I_{OH} = 5 mA	4.300	4.856	--	V
		Push-Pull 2x, Open-Darin PMOS 2x, I_{OH} = 5 mA	4.400	4.927	--	V
Low-level Output Voltage	V_{OL}	Push-Pull 1x, I_{OL} = 5 mA	--	0.136	0.192	V
		Push-Pull 2x, I_{OL} = 5 mA	--	0.068	0.095	V
		Open-Darin NMOS 1x, I_{OL} = 5 mA	--	0.068	0.096	V
		Open-Darin NMOS 2x, I_{OL} = 5 mA	--	0.034	0.049	V
High-level Output Current [1]	I_{OH}	Push-Pull 1x, Open-Darin PMOS 1x, V_{OH} = 2.4 V	19.370	28.850	--	mA
		Push-Pull 2x, Open-Darin PMOS 2x, V_{OH} = 2.4 V	37.973	56.502	--	mA
Low-level Output Current [1]	I_{OL}	Push-Pull 1x, V_{OL} = 0.4 V	5.731	8.414	--	mA
		Push-Pull 2x, V_{OL} = 0.4 V	11.286	16.710	--	mA
		Open-Drain NMOS 1x, V_{OL} = 0.4 V	11.453	16.756	--	mA
		Open-Drain NMOS 2x, V_{OL} = 0.4 V	22.591	32.926	--	mA
Maximum Average or DC Current Through V_{DD} Pin (Per chip side [2])	I_{VDD}	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
Maximum Average or DC Current Through GND Pin (Per chip side [2])	I_{GND}	T_J = 85 °C	--	--	90	mA
		T_J = 110 °C	--	--	44	mA
Maximal Voltage Applied to any PIN in High-Impedance State	V_O		--	--	V_{DD} + 0.3	V
Startup Time	T_{SU}	From V_{DD} rising past PON_{THR}	--	--	0.84	ms
Power-On Threshold	PON_{THR}	V_{DD} level required to start up the chip	1.342	1.510	1.664	V
Power-Off Threshold	$POFF_{THR}$	V_{DD} level required to switch off the chip	0.656	0.875	1.157	V
Pull-up or Pull-down Resistance	R_{PULL}	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
Decoupling Capacitor	C_{VDD}	Capacitor value at V_{DD}	--	0.1	--	µF

[1] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
[2] The GreenPAK's power rails are divided into two sides. Pins 2,3, and 4 are connected to one side, pins 6,7, and 8 to another.

3.4.2 Estimated Typical Current of Macrocell Configurations

Typical values are at T_A = +25 °C, unless otherwise specified

Parameter	Symbol	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Current	I_{DD}	Chip Quiescent	0.28	0.53	0.81	µA
		OSC 2 MHz, pre-divider = 1, divide = 1	24.90	36.16	52.97	µA
		OSC 2 MHz, pre-divider = 1, divide = 8	24.76	35.87	52.45	µA
		OSC 2 MHz, pre-divider = 1, divide = 64	24.67	35.70	52.21	µA
		OSC 2 MHz, pre-divider = 2, divide = 1	21.02	28.47	40.54	µA
		OSC 2 MHz, pre-divider = 2, divide = 8	20.95	28.33	40.28	µA
		OSC 2 MHz, pre-divider = 2, divide = 64	20.91	28.24	40.16	µA
		OSC 2 MHz, pre-divider = 4, divide = 1	19.10	24.66	34.37	µA
		OSC 2 MHz, pre-divider = 4, divide = 8	19.07	24.59	34.24	µA
		OSC 2 MHz, pre-divider = 4, divide = 64	19.04	24.55	34.18	µA
		OSC 2 MHz, pre-divider = 8, divide = 1	18.12	22.72	31.23	µA
		OSC 2 MHz, pre-divider = 8, divide = 8	18.11	22.68	31.17	µA
		OSC 2 MHz, pre-divider = 8, divide = 64	18.09	22.66	31.14	µA
		OSC 25 kHz, pre-divider = 1, divide = 1, 8, 64	5.01	5.38	6.24	µA
		OSC 25 kHz, pre-divider = 2, divide = 1, 8, 64	4.96	5.29	6.09	µA
		OSC 25 kHz, pre-divider = 4, divide = 1, 8, 64	4.93	5.24	6.01	µA
		OSC 25 kHz, pre-divider = 8, divide = 1, 8, 64	4.92	5.22	5.97	µA

3.4.3 Estimated Typical Delay for Each Macrocell

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Delay	tpd	Digital Input to PP 1x	36	38	15	16	11	12	ns
Delay	tpd	Digital Input to PP 2x	32	35	13	15	10	11	ns
Delay	tpd	Digital Input with Schmitt Trigger to PP 1x	35	37	15	15	10	11	ns
Delay	tpd	Low Voltage Digital input - to PP 1x (V_{IH} = min)	42	631	20	240	16	152	ns
Delay	tpd	Digital Input without Schmitt Trigger - 1x NMOS	--	84	--	30	--	19	ns
Delay	tpd	Digital Input without Schmitt Trigger - 1x PMOS	35	--	15	--	11	--	ns
Delay	tpd	Digital Input without Schmitt Trigger - 2x NMOS	--	74	--	26	--	17	ns
Delay	tpd	Digital Input without Schmitt Trigger - 2x PMOS	32	--	13	--	10	--	ns
Delay	tpd	Output enable from pin, OE Hi-Z to 1	36	--	15	--	11	--	ns
Delay	tpd	Output enable from pin, OE Hi-Z to 0	--	38	--	16	--	12	ns
Delay	tpd	2-bit LUT (LATCH shared macrocell inputs)	23	22	10	9	7	6	ns
Delay	tpd	LATCH (2-bit LUT shared macrocell inputs)	22	24	10	9	7	6	ns

Parameter	Symbol	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
Delay	tpd	3-bit LUT (LATCH shared macrocell inputs)	28	25	11	10	8	7	ns
Delay	tpd	LATCH with nRST/nSET (3-bit LUT shared macrocell inputs)	25	26	11	10	8	7	ns
Delay	tpd	4-bit LUT (shared macrocell inputs)	32	30	13	12	9	8	ns
Delay	tpd	2-bit LUT	17	19	7	7	5	5	ns
Delay	tpd	3-bit LUT	20	22	8	8	6	6	ns
Delay	tpd	CNT/DLY Logic	47	42	20	17	14	12	ns
Delay	tpd	CNT/DLY (shared macrocell inputs)	46	41	19	17	14	12	ns
Delay	tpd	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	109	--	49	--	34	--	ns
Delay	tpd	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	108	--	49	--	34	ns
Delay	tpd	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	109	108	49	49	34	34	ns
Pulse Width	tw	CNT3/DLY3 Rising Edge Detect (shared macrocell inputs)	50	--	21	--	15	--	ns
Pulse Width	tw	CNT3/DLY3 Falling Edge Detect (shared macrocell inputs)	--	51	--	21	--	14	ns
Pulse Width	tw	CNT3/DLY3 Both Edge Detect (shared macrocell inputs)	48	49	20	20	14	14	ns
Delay	tpd	DFF	27	19	11	8	8	6	ns
Delay	tpd	DFF nReset	--	29	--	12	--	8	ns
Delay	tpd	DFF nSet	--	35	--	14	--	9	ns
Delay	tpd	Filter	188	191	75	75	49	49	ns
Delay	tpd	CNT/DLY (non-delayed edge, 25 kHz/ 2 MHz OSC)	47	47	20	20	14	14	ns

3.4.4 Programmable Delay Typical Delays and Widths

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	Symbol	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Width, 1 cell	Width	mode: (any) edge detect, edge detect output	308	140	104	ns
Width, 2 cell	Width	mode: (any) edge detect, edge detect output	618	280	208	ns
Width, 3 cell	Width	mode: (any) edge detect, edge detect output	929	421	313	ns
Width, 4 cell	Width	mode: (any) edge detect, edge detect output	1240	562	418	ns
Delay, 1 cell	time1	mode: (any) edge detect, edge detect output	39	16	11	ns
Delay, 2 cell	time1	mode: (any) edge detect, edge detect output	39	16	11	ns
Delay, 3 cell	time1	mode: (any) edge detect, edge detect output	39	16	11	ns
Delay, 4 cell	time1	mode: (any) edge detect, edge detect output	39	16	11	ns
Delay, 1 cell	time2	mode: both edge delay, edge detect output	355	159	117	ns
Delay, 2 cell	time2	mode: both edge delay, edge detect output	665	299	222	ns
Delay, 3 cell	time2	mode: both edge delay, edge detect output	976	440	326	ns
Delay, 4 cell	time2	mode: both edge delay, edge detect output	1287	581	431	ns

3.4.5 Typical Filter Rejection Pulse Width

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 155	< 60	< 38	ns

3.5 Oscillators Specification

3.5.1 Oscillators Frequency Settling Characteristics

Typical values are at T_A = +25 °C, unless otherwise specified.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Frequency Settling Time	25 kHz	auto	76.565	71.852	52.759	µs
Frequency Settling Time	2 MHz	auto	1.936	1.311	1.770	µs
Variable (CLK Period)	25 kHz	forced	0-40	0-40	0-40	µs
Variable (CLK Period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs

3.5.2 25 kHz Oscillator Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5 %	24.646	25.506	23.994	25.701	23.994	26.156
3.3 V ±10 %	24.540	25.570	23.843	25.782	23.843	26.196
5.0 V ±10 %	24.544	25.667	23.845	25.918	23.845	26.368
2.5 V to 4.5 V	24.526	25.604	23.834	25.807	23.834	26.250
1.71 V to 5.5 V	24.526	25.773	23.834	26.020	23.834	26.467

3.5.3 25 kHz Oscillator Frequency Error

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-1.42	2.02	-4.02	2.80	-4.02	4.62
3.3 V ±10 %	-1.84	2.28	-4.63	3.13	-4.63	4.78
5.0 V ±10 %	-1.83	2.67	-4.62	3.67	-4.62	5.47
2.5 V to 4.5 V	-1.90	2.42	-4.66	3.23	-4.66	5.00
1.71 V to 5.5 V	-1.90	3.09	-4.66	4.08	-4.66	5.87

3.5.4 2 MHz Oscillator Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5 %	1.948	2.041	1.910	2.056	1.893	2.065
3.3 V ±10 %	1.974	2.025	1.941	2.043	1.904	2.043
5.0 V ±10 %	1.938	2.149	1.910	2.163	1.863	2.182
2.5 V to 4.5 V	1.955	2.033	1.921	2.055	1.888	2.055
1.71 V to 5.5 V	1.805	2.212	1.771	2.226	1.749	2.246

3.5.5 2 MHz Oscillator Frequency Error

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +105 °C		-40 °C to +105 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-2.59	2.06	-4.50	2.79	-5.34	3.26
3.3 V ±10 %	-1.31	1.24	-2.95	2.16	-4.81	2.16
5.0 V ±10 %	-3.10	7.44	-4.48	8.15	-6.84	9.08
2.5 V to 4.5 V	-2.24	1.66	-3.93	2.74	-5.59	2.74
1.71 V to 5.5 V	-9.77	10.59	-11.44	11.30	-12.53	12.28

3.5.6 OSCs Power-On Delay

T_A = 25 °C, OSC Power Setting: "Auto Power-on", unless otherwise specified.

Power Supply Range (V_{DD}) V	2 MHz		2 MHz Fast Start-Up Mode		25 kHz		25 kHz Fast Start-Up Mode	
	Typ Value, ns	Max Value, ns	Typ Value, ns	Max Value, ns	Typ Value, µs	Max Value, µs	Typ Value, µs	Max Value, µs
1.71	151	175	104	120	0.180	0.208	0.495	0.685
1.80	134	154	93	107	0.160	0.183	0.471	0.655
1.89	120	137	84	96	0.143	0.163	0.451	0.629
2.30	81	91	59	66	0.098	0.109	0.388	0.546
2.50	70	78	52	57	0.084	0.093	0.367	0.518
2.70	62	69	46	51	0.074	0.081	0.353	0.498
3.00	54	59	41	44	0.064	0.070	0.347	0.470
3.30	47	52	36	39	0.056	0.061	6.300	31.141
3.60	43	46	33	35	0.051	0.055	11.508	61.758
4.20	36	39	29	31	0.043	0.046	19.649	20.061
4.50	34	36	27	29	0.281	4.289	19.632	20.035
5.00	31	33	25	27	1.035	10.195	19.582	19.995
5.50	29	31	23	25	1.585	7.961	19.487	19.979

4. Summary of Macrocell Function

4.1 IO Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open-Drain Outputs (NMOS and PMOS, 1x and 2x)
- Push-Pull Outputs (1x and 2x)
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- Pins 4 and 8 can be configured as bidirectional IO.

4.2 Connection Matrix

- Digital matrix for circuit connections based on user design.

4.3 Combinational Logic Look Up Tables (LUTs – 4 Total)

- Two 2-bit Look up Tables
- Two 3-bit Look up Tables.

4.4 Combination Function Macrocells (7 Total)

- Two Selectable DFF/LATCH or 2-bit LUTs
- Two Selectable DFF/LATCH or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- One Selectable CNT/DLY or 4-bit LUT
- One Programmable Delay or Deglitch Filter.

4.5 Delays/Counters (3 Total)

- Three 8-bit delays/counters with external clock/reset: range 1-255 clock cycles.

4.6 Pipe Delay (Part of Combination Function Macrocell)

- 8 stage/2 output
- Two 1 to 8 stage selectable outputs.

4.7 Programmable Delay

- 140 ns/280 ns/420 ns/560 ns at V_{DD} = 3.3 V
- Includes Edge Detection function.

4.8 Additional Logic Functions (Part of Combination Function Macrocell)

- One Deglitch filter macrocell.

4.9 RC Oscillator

- 25 kHz or 2 MHz selectable frequency
- First Stage Clock pre-divider: OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider control with two outputs, OUT0 and OUT1: selectable (OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, or OSC/64).

4.10 Power-On Reset

5. User Programmability

Non-volatile memory (NVM) is used to configure the SLG46108-EV's connection matrix routing and macrocells. The NVM is One Time Programmable (OTP). However, GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas Electronics Corporation to integrate into the production process.

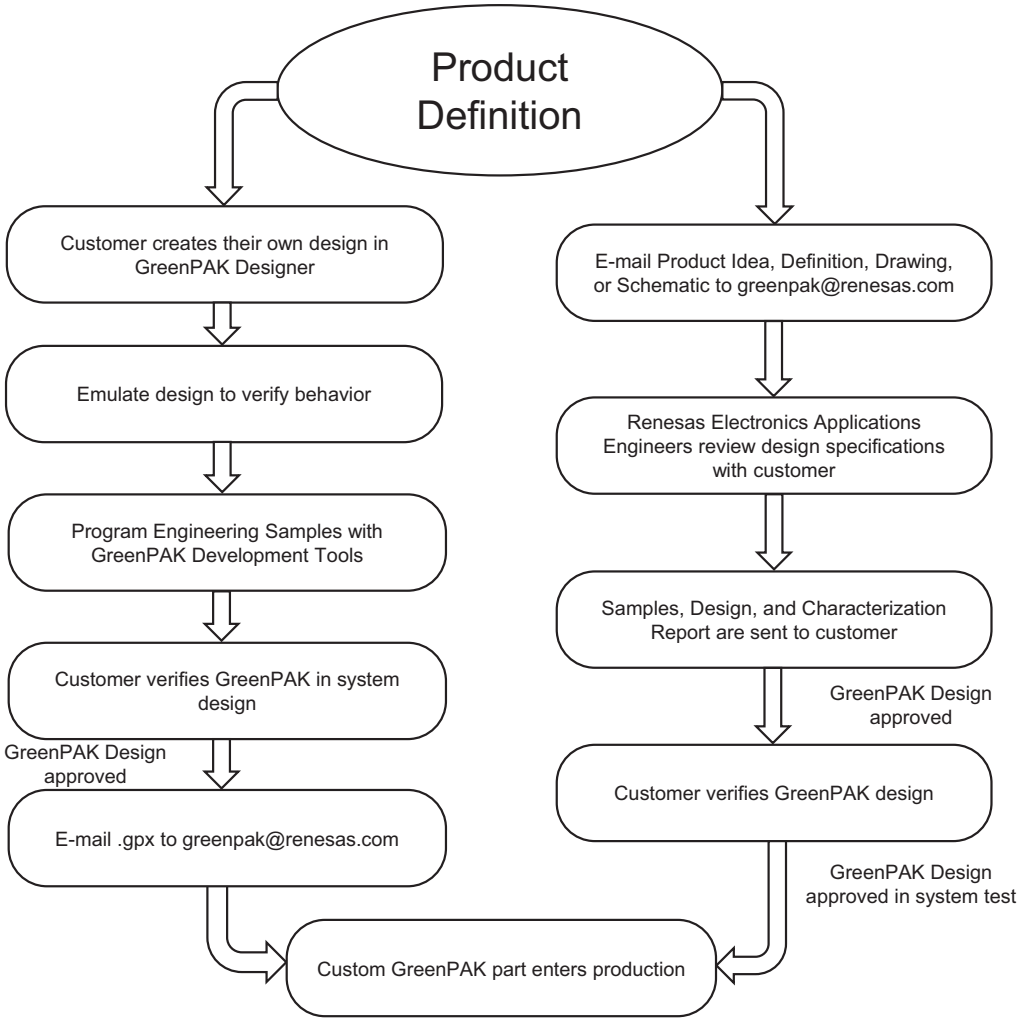


Figure 3. Steps to Create a Custom GreenPAK Device

6. IO Pins

The SLG46108-EV has a total of multi-function IO pins which can function as either a user defined Input. Refer to section 2. Pin Information pin definitions.

Of the 6 user defined IO pins on the SLG46108-EV, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

6.1 Input Modes

Each IO pin can be configured as a digital input pin with/without buffered Schmitt trigger, or can also be configured as a low voltage digital input.

6.2 Output Modes

Pins 3, 4, 6, 7, and 8 can all be configured as digital output pins.

6.3 Pull-Up/Down Resistors

All IO pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other IO pins, the internal resistors can be configured as either pull-up or pull-downs.

6.4 IO Register Settings

6.4.1 PIN 2 Register Settings

Table 2. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	Registers [350:349]	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low voltage digital input 11: Reserved
PIN 2 Pull-Down Resistor Value Selection	Registers [352:351]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor

6.4.2 PIN 3 Register Settings

Table 3. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	Registers [355:353]	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
PIN 3 Pull-Up/Down Resistor Value Selection	Registers [357:356]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
PIN 3 Pull-Up/Down Resistor Selection	Register [358]	0: Pull-down resistor 1: Pull-up resistor
PIN 3 Driver Strength Selection	Register [359]	0: 1x 1: 2x

6.4.3 PIN 4 Register Settings

Table 4. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control (sig_PIN4_oe = 0)	Registers [361:360]	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 11: Low voltage digital input 10: Reserved
PIN 4 Mode Control (sig_PIN4_oe = 1)	Registers [363:362]	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain NMOS 1x 11: Open-drain NMOS 2x
PIN 4 Pull-Up/Down Resistor Value Selection	Registers [365:364]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
PIN 4 Pull-Up/Down Resistor Selection	Register [366]	0: Pull-down resistor 1: Pull-up resistor

6.4.4 PIN 6 Register Settings

Table 5. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control	Registers [370:368]	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
PIN 6 Pull-Up/Down Resistor Value Selection	Registers [372:371]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
PIN 6 Pull-Up/Down Resistor Value Selection	Register [373]	0: Pull-down resistor 1: Pull-up resistor
PIN 6 Pull-Up/Down Resistor Selection	Register [374]	0: 1x 1: 2x

6.4.5 PIN 7 Register Settings

Table 6. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control	Registers [377:375]	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
PIN 7 Pull-Up/Down Resistor Value Selection	Registers [379:378]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
PIN 7 Pull-Up/Down Resistor Selection	Register [380]	0: Pull-down resistor 1: Pull-up resistor
PIN 7 Driver Strength Selection	Register [381]	0: 1x 1: 2x

6.4.6 PIN 8 Register Settings

Table 7. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control (sig_PIN8_oe = 0)	Registers [383:382]	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 11: Low voltage digital input 10: Reserved
PIN 8 Mode Control (sig_PIN8_oe = 1)	Registers [385:384]	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain NMOS 1x 11: Open-drain NMOS 2x
PIN 8 Pull-Up/Down Resistor Value Selection	Registers [386:387]	00: Floating 01: 10 kΩ resistor 10: 100 kΩ resistor 11: 1 MΩ resistor
PIN 8 Pull-Up/Down Resistor Selection	Register [388]	0: Pull-down resistor 1: Pull-up resistor

6.5 GPI IO Structure

6.5.1 GPI IO Structure (for Pin 2)

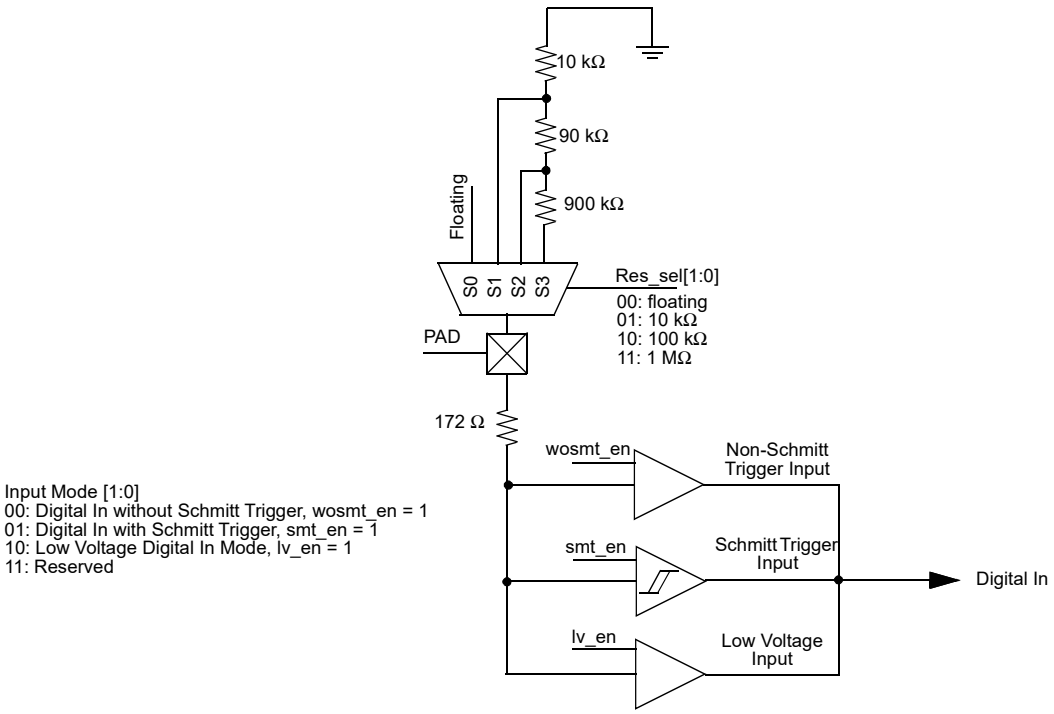


Figure 4. PIN 2 GPI IO Structure Diagram

6.6 Matrix OE IO Structure

6.6.1 Matrix OE IO Structure (for Pins 4, 8)

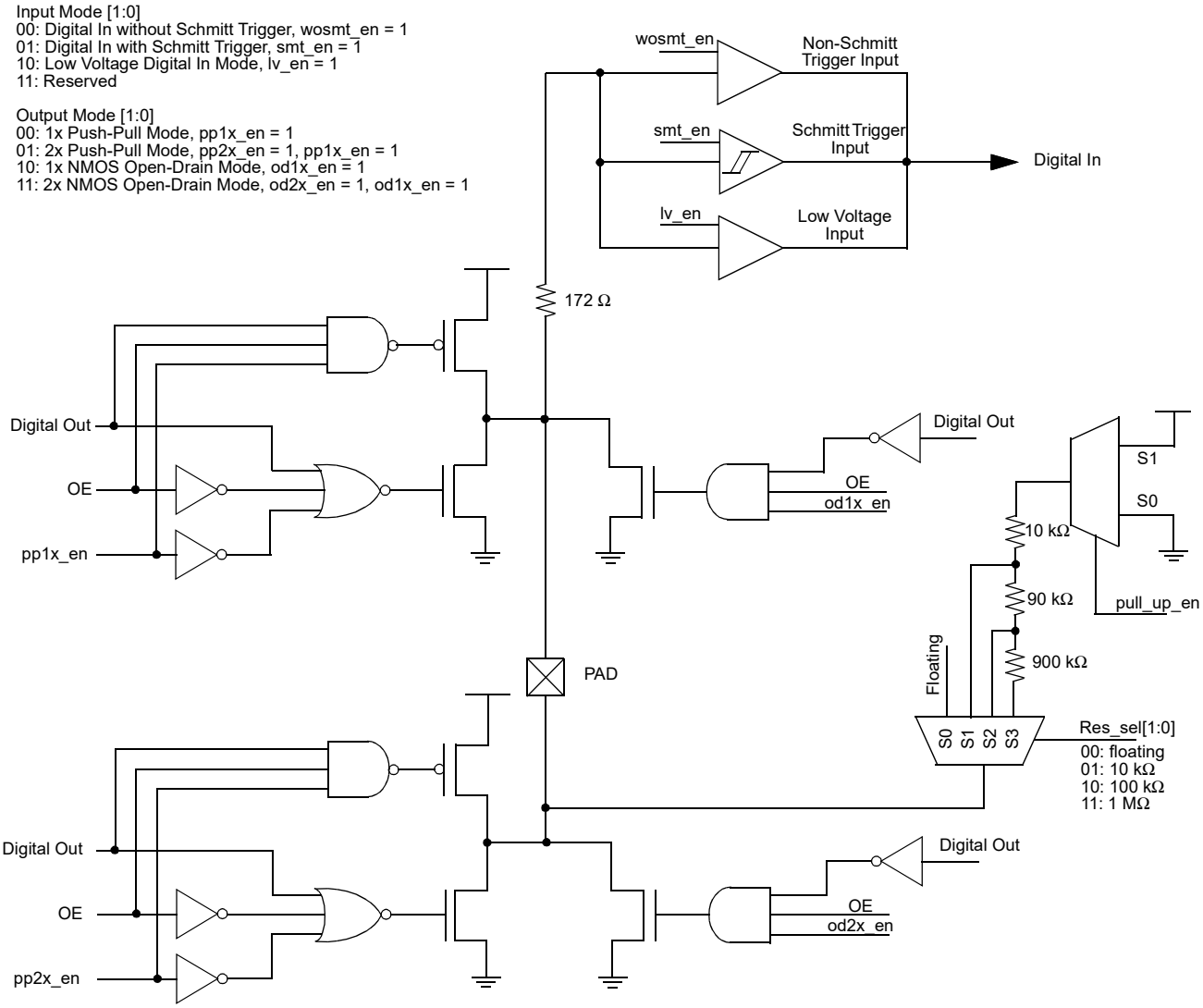


Figure 5. Matrix OE IO Structure Diagram

6.7 Register OE IO Structure

6.7.1 Register OE IO Structure (for Pins 3, 6, 7)

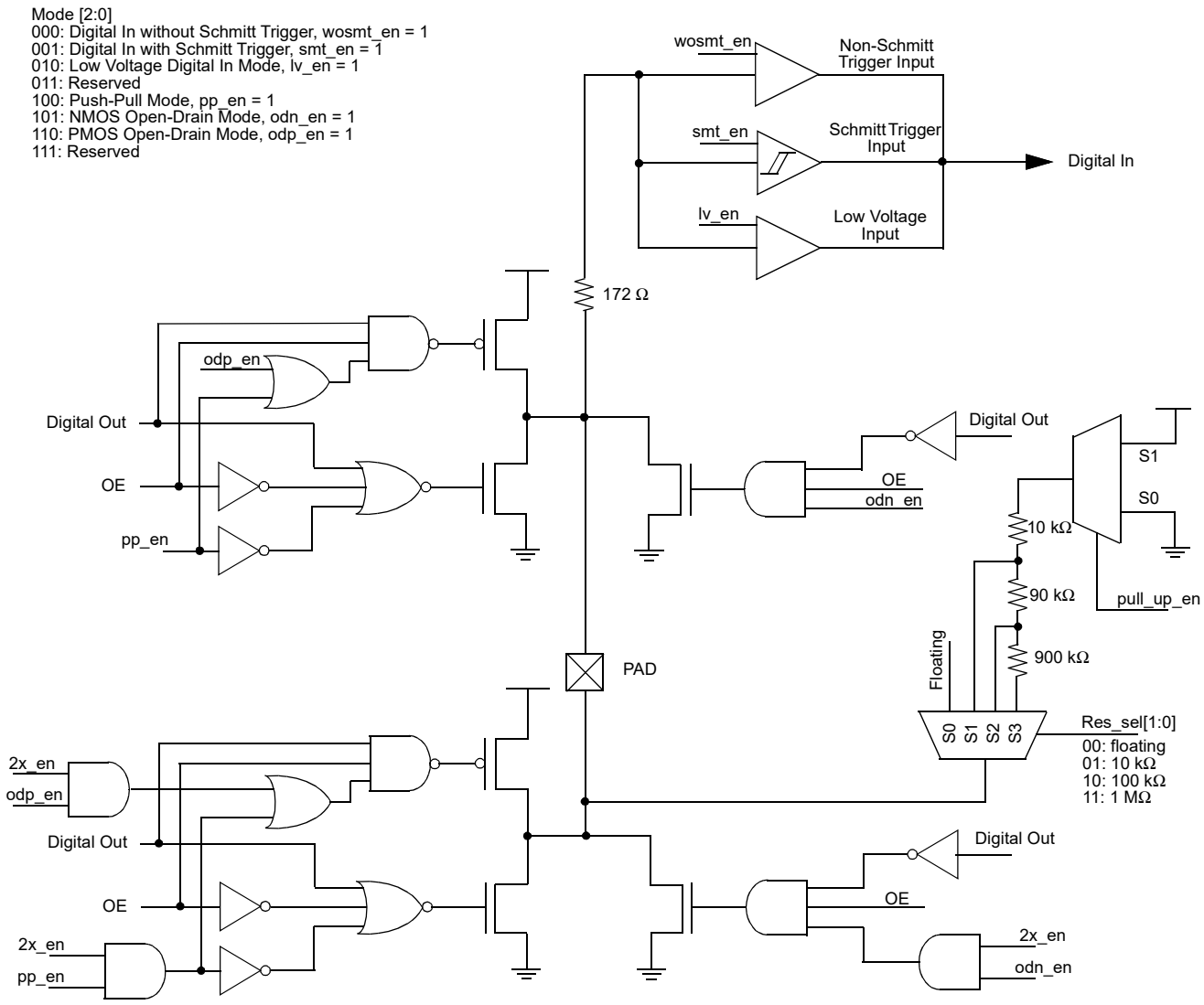


Figure 6. Register OE IO Structure Diagram

7. Connection Matrix

The Connection Matrix in the SLG46108-EV is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46108-EV has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 463 register bits within the SLG46108-EV are programmed a fully custom circuit will be created.

The Connection Matrix has 32 inputs and 40 outputs. Each of the 32 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including IO pins, LUTs, other digital resources, such as V_{DD} and V_{SS}. The input to a digital macrocell uses a 5-bit register to select one of these 32 input lines.

For a complete list of the SLG46108-EV’s register table, see section 13. Register Definitions.

Matrix Input Signal Functions	N
VSS	0
Pin 2 Digital In	1
Pin 3 Digital In	2
Pin 4 Digital In	3
⋮	⋮
DFF3 nQ Output	30
V_{DD}	31

Matrix Inputs

Matrix Outputs

N	0	1	2	⋯	39
Registers	reg <4:0>	reg <9:5>	reg <14:10>	⋯	Regs [199:195]
Function	PIN3 Digital Output Source	PIN4Digital Output Source	PIN4 Digital Output Enable	⋯	PIN8 Digital Output Enable

Figure 7. Connection Matrix

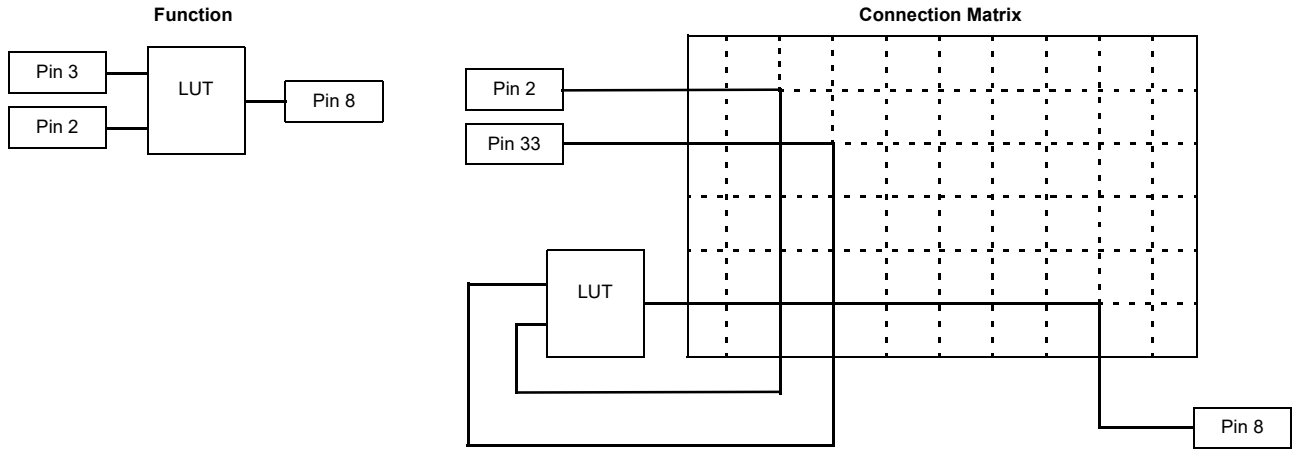


Figure 8. Connection Matrix Example

7.1 Matrix Input Table

Table 8. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode				
		4	3	2	1	0
0	GND	0	0	0	0	0
1	Pin2 digital Input	0	0	0	0	1
2	Pin3 digital Input	0	0	0	1	0
3	Pin4 digital Input	0	0	0	1	1
4	LUT2_0 output (DFF/LATCH_0 output)	0	0	1	0	0
5	LUT2_1 output (DFF/LATCH_1 output)	0	0	1	0	1
6	LUT2_2 output	0	0	1	1	0
7	LUT2_3 output	0	0	1	1	1
8	LUT3_0 output (DFF/LATCH_2 output with nRST or nSET)	0	1	0	0	0
9	LUT3_1 output (DFF/LATCH_3 output with nRST or nSET)	0	1	0	0	1
10	LUT3_2 output	0	1	0	1	0
11	LUT3_3 output	0	1	0	1	1
12	LUT3_4 output (Pipe Delay ouput0)	0	1	1	0	0
13	Pipe Delay ouput1	0	1	1	0	1
14	LUT4_0 output (CNT_DLY2 output (8 bit w/ ext CK, reset))	0	1	1	1	0
15	CNT_DLY0 output (8 bit w/ ext CK (shared with CNT_DLY1 ext CK), reset)	0	1	1	1	1
16	CNT_DLY1 output (8 bit w/ ext CK (shared with CNT_DLY0 ext CK), reset)	1	0	0	0	0
17	CNT_DLY3(8 bit) output	1	0	0	0	1
18	CNT_DLY3(8 bit) edge detect output	1	0	0	1	0
19	Programmable delay with edge detector output (deglitch filter output)	1	0	0	1	1
20	Internal oscillator output0 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	0	0
21	Internal oscillator output1 (one of /1,/2,/3,/4,/8,12/,24/,64/ selected by REG)	1	0	1	0	1
22	GND	1	0	1	1	0
23	Resetb_core POR as matrix input	1	0	1	1	1
24	Pin6 digital Input	1	1	0	0	0
25	Pin7 digital Input	1	1	0	0	1
26	Pin8 digital Input	1	1	0	1	0
27	DFF0 nQ output	1	1	0	1	1
28	DFF1 nQ output	1	1	1	0	0
29	DFF2 nQ output	1	1	1	0	1
30	DFF3 nQ output	1	1	1	1	0
31	V_{DD}	1	1	1	1	1

7.2 Matrix Output Table

Table 9. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[4:0]	Pin 3 digital out source	0
[9:5]	Pin 4 digital out source	1
[14:10]	Pin 4 output enable	2
[19:15]	in0 of LUT2_0 (Clock Input of DFF0)	3
[24:20]	in1 of LUT2_0 (Data Input of DFF0)	4
[29:25]	in0 of LUT2_1 (Clock Input of DFF1)	5
[34:30]	in1 of LUT2_1 (Data Input of DFF1)	6
[39:35]	in0 of LUT2_2	7
[44:40]	in1 of LUT2_2	8
[49:45]	in0 of LUT2_3	9
[54:50]	in1 of LUT2_3	10
[59:55]	in0 of LUT3_0 (Clock Input of DFF2 with nReset/nSet)	11
[64:60]	in1 of LUT3_0 (Data input of DFF2 with nReset/nSet)	12
[69:65]	in2 of LUT3_0 (nRST or nSET of DFF2 with nReset/nSet)	13
[74:70]	in0 of LUT3_1 (Clock Input of DFF3 with nReset/nSet)	14
[79:75]	in1 of LUT3_1 (Data input of DFF3 with nReset/nSet)	15
[84:80]	in2 of LUT3_1 (nRST or nSET of DFF3 with nReset/nSet)	16
[89:85]	in0 of LUT3_2	17
[94:90]	in1 of LUT3_2	18
[99:95]	in2 of LUT3_2	19
[104:100]	in0 of LUT3_3	20
[109:105]	in1 of LUT3_3	21
[114:110]	in2 of LUT3_3	22
[119:115]	in0 of LUT3_4 (Input of Pipe Delay)	23
[124:120]	in1 of LUT3_4 (nRST of Pipe Delay)	24
[129:125]	in2 of LUT3_4 (Clock of Pipe Delay)	25
[134:130]	in0 of LUT4_0 (Input for Delay2 external clock or Counter2 external clock)	26
[139:135]	in1 of LUT4_0 (Input for Delay2 or Counter2 reset input)	27
[144:140]	in2 of LUT4_0 (Input for Counter2 FSM keep signal)	28
[149:145]	in3 of LUT4_0 (Input for Counter2 FSM up signal)	29
[154:150]	Input for Delay0 or Counter0 reset input	30
[159:155]	Input for Delay1 or Counter1 reset input	31
[164:160]	Input for Delay 0/1(Counter 0/1) external clock	32
[169:165]	Input for Delay3 or Counter3 reset input	33
[174:170]	Input for programmable delay (deglitch filter input)	34

Table 9. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[179:175]	Power down for osc (higher priority) (high = power down)	35
[184:180]	Pin 6 digital out source	36
[189:185]	Pin 7 digital out source	37
[194:190]	Pin 8 digital out source	38
[199:195]	Pin 8 output enable	39

8. Combinatorial Logic

Combinatorial logic is supported via four Lookup Tables (LUTs) within the SLG46108-EV. There are two 2-bit LUTs and two 3-bit LUTs. The device also includes six Combination Function Macrocells that can be used as LUTs. For more details, please see section 9. Combination Function Macrocells.

Inputs/Outputs for the four LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 2-Bit LUT

The two 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

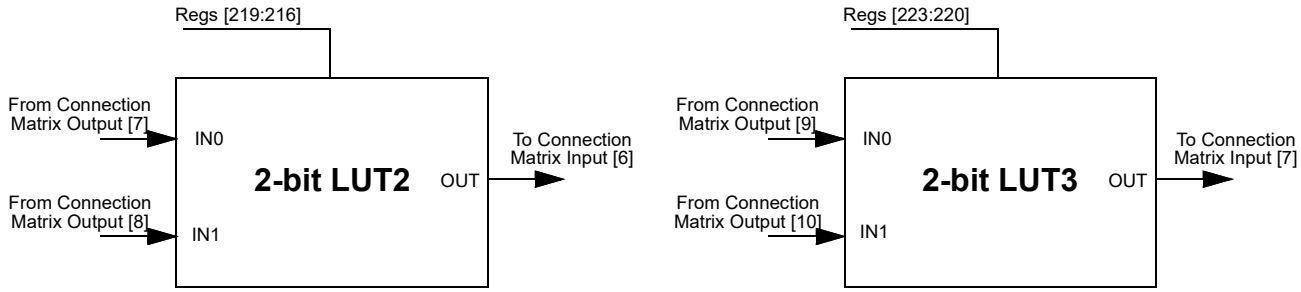


Figure 9. 2-bit LUTs

Table 10. 2-bit LUT2 Truth Table

IN0	IN1	OUT	
0	0	register [216]	LSB
0	1	register [217]	
1	0	register [218]	
1	1	register [219]	MSB

Table 11. 2-bit LUT3 Truth Table

IN2	IN1	OUT	
0	0	register [220]	LSB
0	1	register [221]	
1	0	register [222]	
1	1	register [223]	MSB

Each 2-bit LUT uses a 4-bit register signal to define their output functions:

- 2-Bit LUT2 is defined by registers [219:216]
- 2-Bit LUT3 is defined by registers [223:220].

Table 12 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 12. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

8.2 3-Bit LUT

The two 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

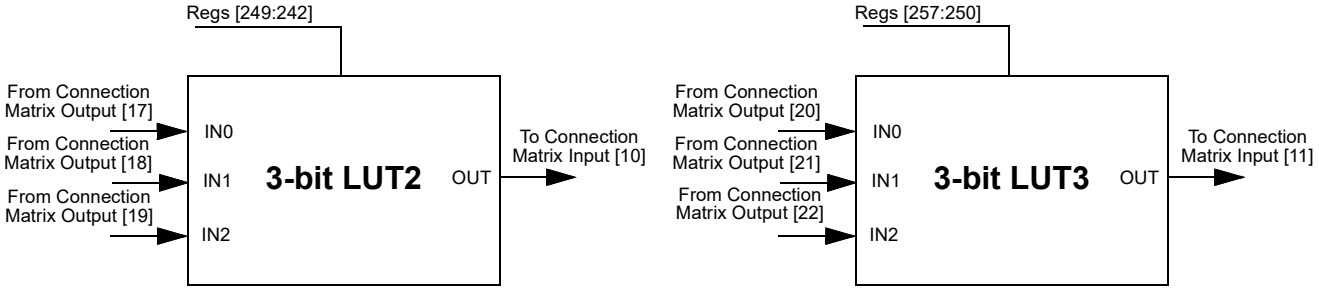


Figure 10. 3-bit LUTs

Table 13. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [242]	LSB
0	0	1	register [243]	
0	1	0	register [244]	
0	1	1	register [245]	
1	0	0	register [246]	
1	0	1	register [247]	
1	1	0	register [248]	
1	1	1	register [249]	MSB

Table 14. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [250]	LSB
0	0	1	register [251]	
0	1	0	register [252]	
0	1	1	register [252]	
1	0	0	register [254]	
1	0	1	register [255]	
1	1	0	register [256]	
1	1	1	register [257]	MSB

Each 3-bit LUT uses an 8-bit register signal to define their output functions:

- 3-Bit LUT2 is defined by registers [249:242]
- 3-Bit LUT3 is defined by registers [257:250].

Table 15 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 3-bit LUT logic cells.

Table 15. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

9. Combination Function Macrocells

The SLG46108-EV has seven combination function macrocells that can serve more than one logic or timing function. In six of these cases, they can serve as a Look Up Table (LUT), or as another logic or timing function. In the last case, it can serve as either a programmable delay or deglitch filter. See the list below for the functions that can be implemented in these macrocells:

- Two macrocells that can serve as either 2-bit LUTs or as DFF/LATCH;
- Two macrocells that can serve as either 3-bit LUTs or as DFF/LATCH;
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay;
- One macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter/Delay;
- One macrocell that can serve as either a Programmable Delay or as a Deglitch Filter.

Inputs/Outputs for the seven combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

When used as a D Flip-Flop/LATCH, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/LATCH macrocells have user selection for initial state, and all have the option to connect both the Q and nQ outputs to the connection matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: if CLK = 1, then Q latches D value.

9.1 2-Bit LUT or D Flip-Flops Macrocells

There are two macrocells that can serve as either 2-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

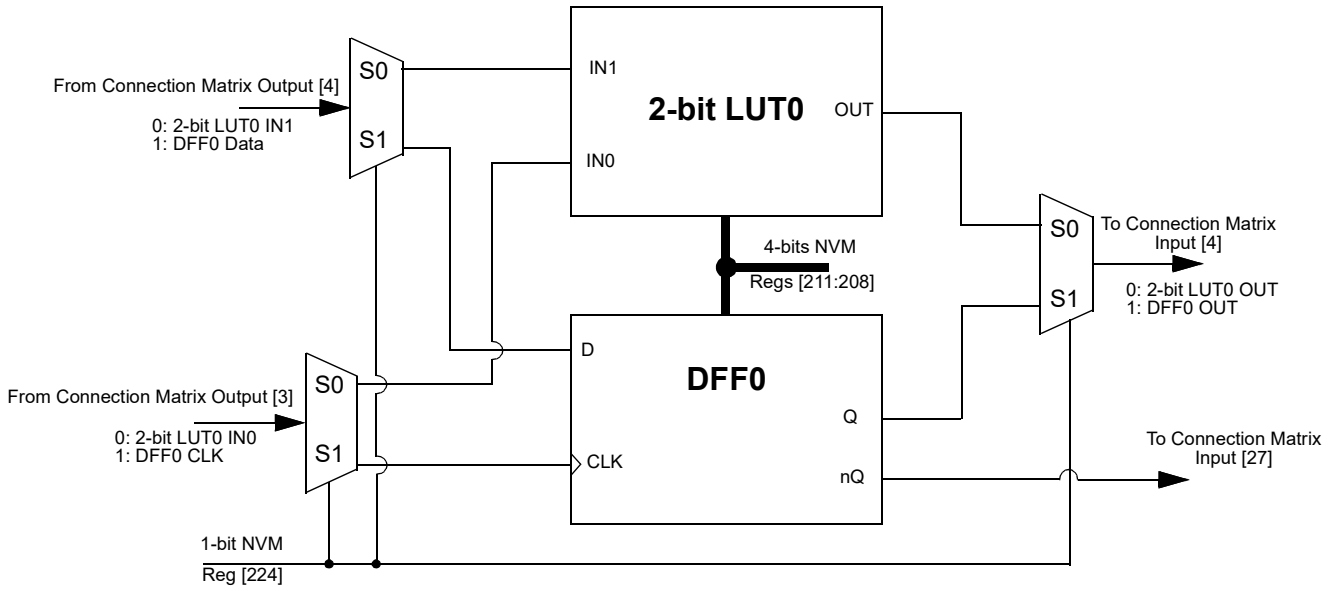


Figure 11. 2-bit LUT0 or DFF0

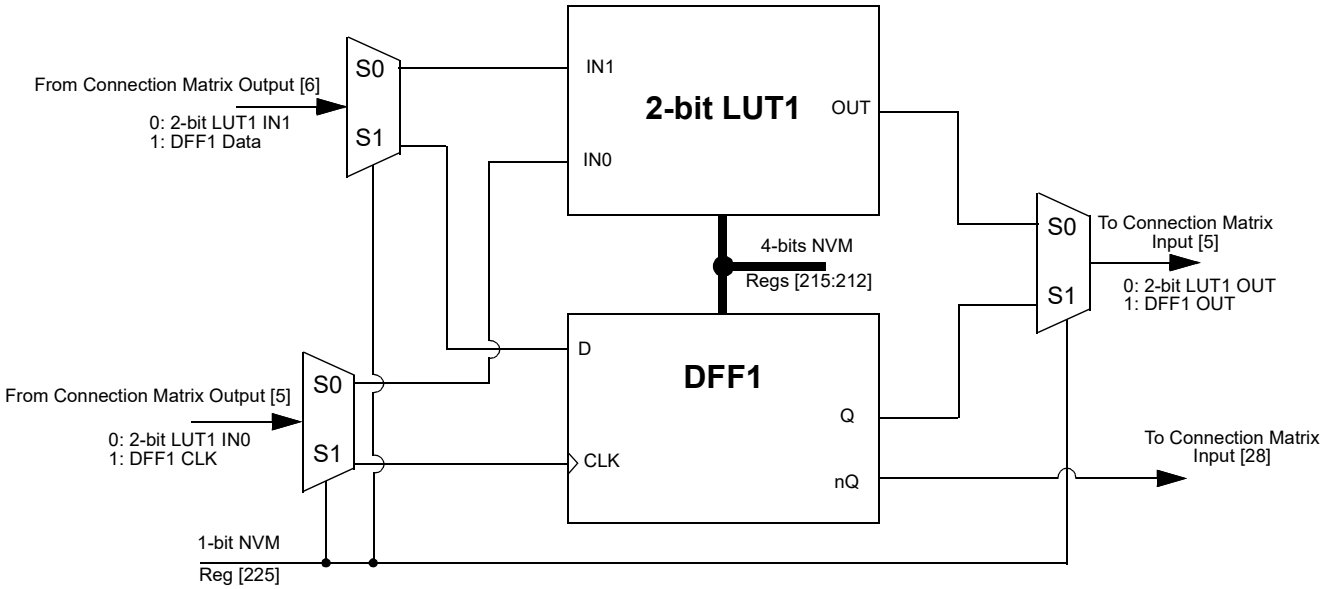


Figure 12. 2-bit LUT1 or DFF1

9.1.1 2-Bit LUT or D Flip-Flop Macrocells Used as 2-Bit LUTs

Table 16. 2-bit LUT0 Truth Table

IN0	IN1	OUT	
0	0	register [208]	LSB
0	1	register [209]	
1	0	register [210]	
1	1	register [211]	MSB

Table 17. 2-bit LUT1 Truth Table

IN2	IN1	OUT	
0	0	register [212]	LSB
0	1	register [213]	
1	0	register [214]	
1	1	register [215]	MSB

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

- 2-Bit LUT0 is defined by registers [211:208]
- 2-Bit LUT1 is defined by registers [215:212].

9.1.2 2-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 18. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF0 or LATCH Select	Register [208]	0: DFF function 1: LATCH function
DFF0 Initial Polarity Select	Register [210]	0: Low 1: High
LUT2_0 Data	Registers [211:208]	LUT2_0 data
LUT2_0 or DFF0 Select	Register [224]	0: LUT2_0 1: DFF0

Table 19. DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF1 or LATCH Select	Register [212]	0: DFF function 1: LATCH function
DFF1 Initial Polarity Select	Register [214]	0: Low 1: High
LUT2_1 Data	Registers [215:212]	LUT2_1 data
LUT2_1 or DFF1 Select	Register [225]	0: LUT2_1 1: DFF1

9.2 3-Bit LUT or D Flip-Flop with nSet/nReset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip-Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Set/Reset (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

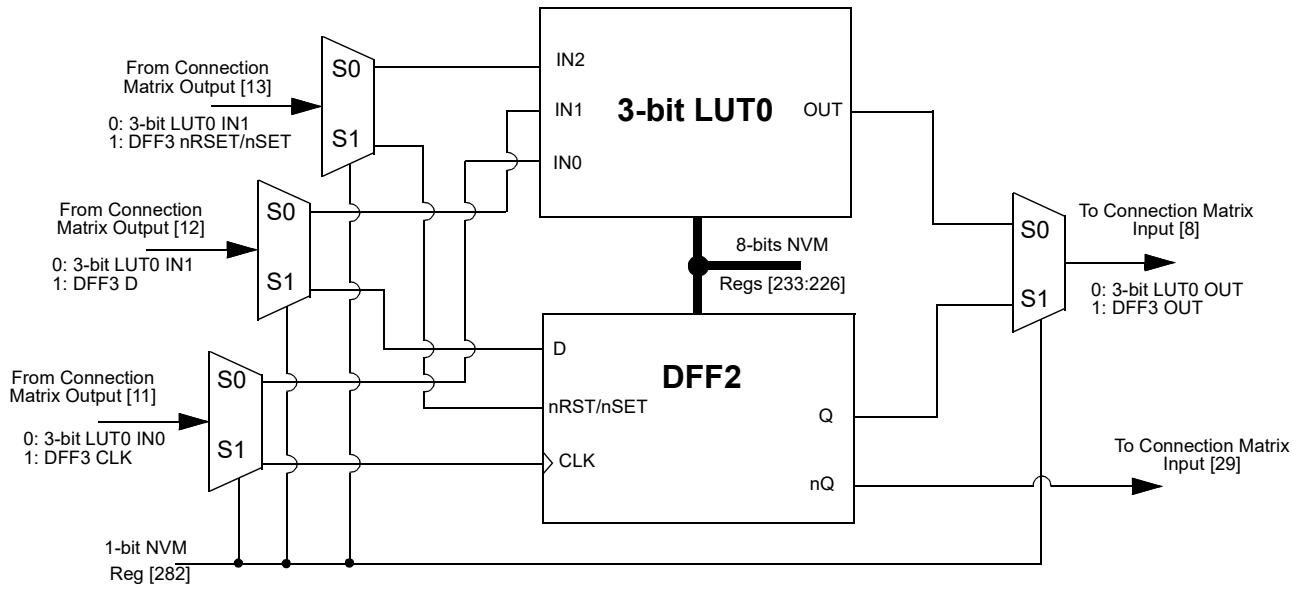


Figure 13. 3-bit LUT0 or DFF2

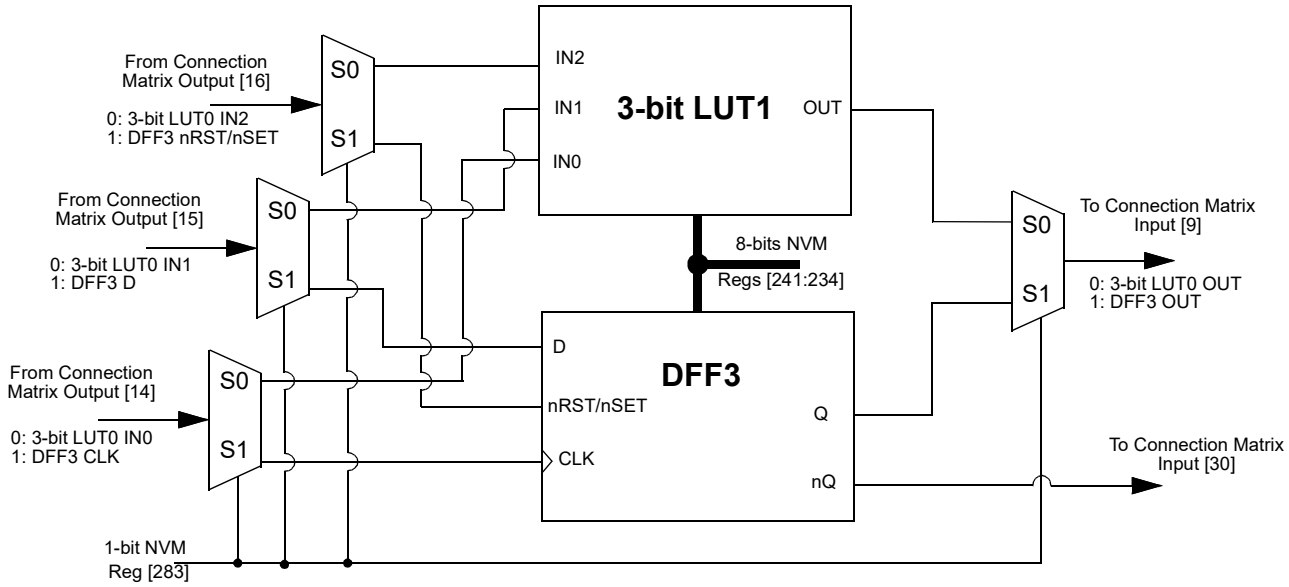


Figure 14. 3-bit LUT1 or DFF3

9.2.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 20. 3-bit LUT20 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [226]	LSB
0	0	1	register [227]	
0	1	0	register [228]	
0	1	1	register [229]	
1	0	0	register [230]	
1	0	1	register [231]	
1	1	0	register [232]	
1	1	1	register [233]	MSB

Table 21. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [234]	LSB
0	0	1	register [235]	
0	1	0	register [236]	
0	1	1	register [237]	
1	0	0	register [238]	
1	0	1	register [239]	
1	1	0	register [240]	
1	1	1	register [241]	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-Bit LUT2 is defined by registers [233:226]
- 3-Bit LUT3 is defined by registers [241:234].

9.2.2 3-Bit LUT or D Flip-Flop Macrocells Used as D Flip-Flop Register Settings

Table 22. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF2 or LATCH Select	Register [226]	0: DFF function 1: LATCH function
DFF2 nRST/nSET Select	Register [228]	1: nSET from matrix out 0: nRST from matrix out
DFF2 Initial Polarity Select	Register [229]	0: Low 1: High
LUT3_0 Data	Registers [233:226]	LUT3_0 data
LUT3_0 or DFF2 Select	Register [266]	0: LUT3_0 1: DFF2

Table 23. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
DFF3 or LATCH Select	Register [234]	0: DFF function 1: LATCH function
DFF3 nRST/nSET Select	Register [236]	1: nSET from matrix out 0: nRST from matrix out
DFF3 Initial Polarity Select	Register [237]	0: Low 1: High
LUT3_1 Data	Registers [241:234]	LUT3_1 data
LUT3_1 or DFF3 Select	Register [267]	0: LUT3_1 1: DFF3

9.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT take in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as an 8-stage Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CK), and Reset (nRST). The Pipe Delay cell is built from D Flip-Flop logic cells that provide the two user selectable output options (OUT0 and OUT1). The DFF cells are tied in series where the output of each delay cell goes to the next DFF cell. There are delay output points for each set of the OUT0 and OUT1 outputs to a 3-input MUX that is controlled by registers [260:258] for OUT0 and registers [263:261] for OUT1. The 3-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46108-EV design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46108-EV). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

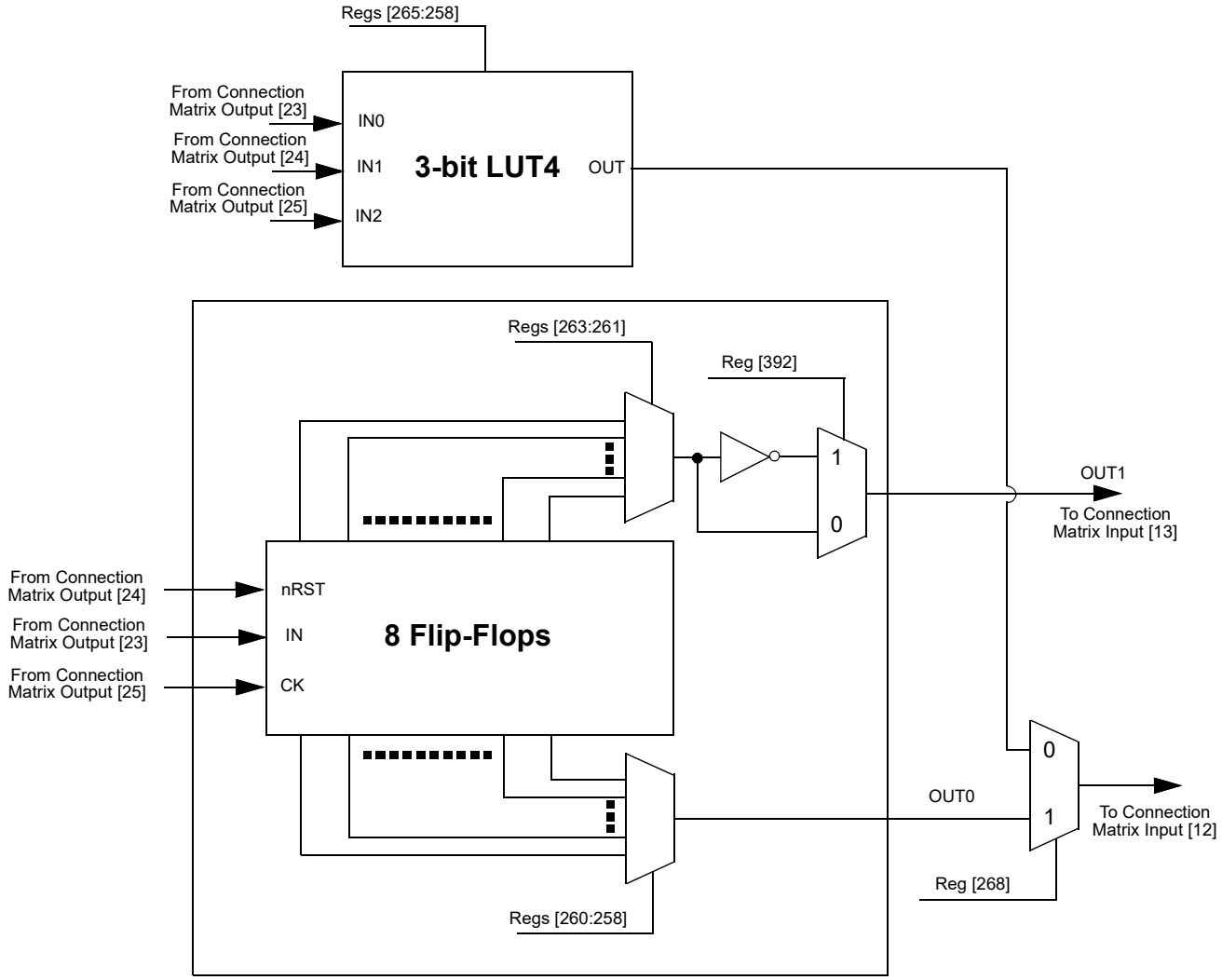


Figure 15. 3-bit LUT4 or Pipe Delay

9.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 24. 3-Bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [258]	LSB
0	0	1	register [259]	
0	1	0	register [260]	
0	1	1	register [261]	
1	0	0	register [262]	
1	0	1	register [263]	
1	1	0	register [264]	
1	1	1	register [265]	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

- 3-Bit LUT4 is defined by registers [265:258].

9.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 25. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 Select	Registers [260:258]	Data (pipe number)
OUT1 Select	Registers [263:261]	Data (pipe number)
LUT3_4 or Pipe Delay Output Select	Register [268]	0: LUT3_4 1: Pipe Delay

9.4 4-Bit LUT or 8-Bit Counter/Delay Macrocells

There is one macrocell that can serve as either a 4-bit LUT or as a Counter/Delay. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the clock (CLK) and reset (DLY_IN/Reset_IN) inputs for the counter/delay, with the output going back to the connection matrix. This macrocell has an optional Finale State Machine (FSM) function. It has two additional matrix inputs for Up and Keep to support FSM functionality. The counter is counting down by default. Logic 1 on input Up reverses counting. Logic 1 on input Keep pauses counting.

Note: Counters initialize with counter data after POR.

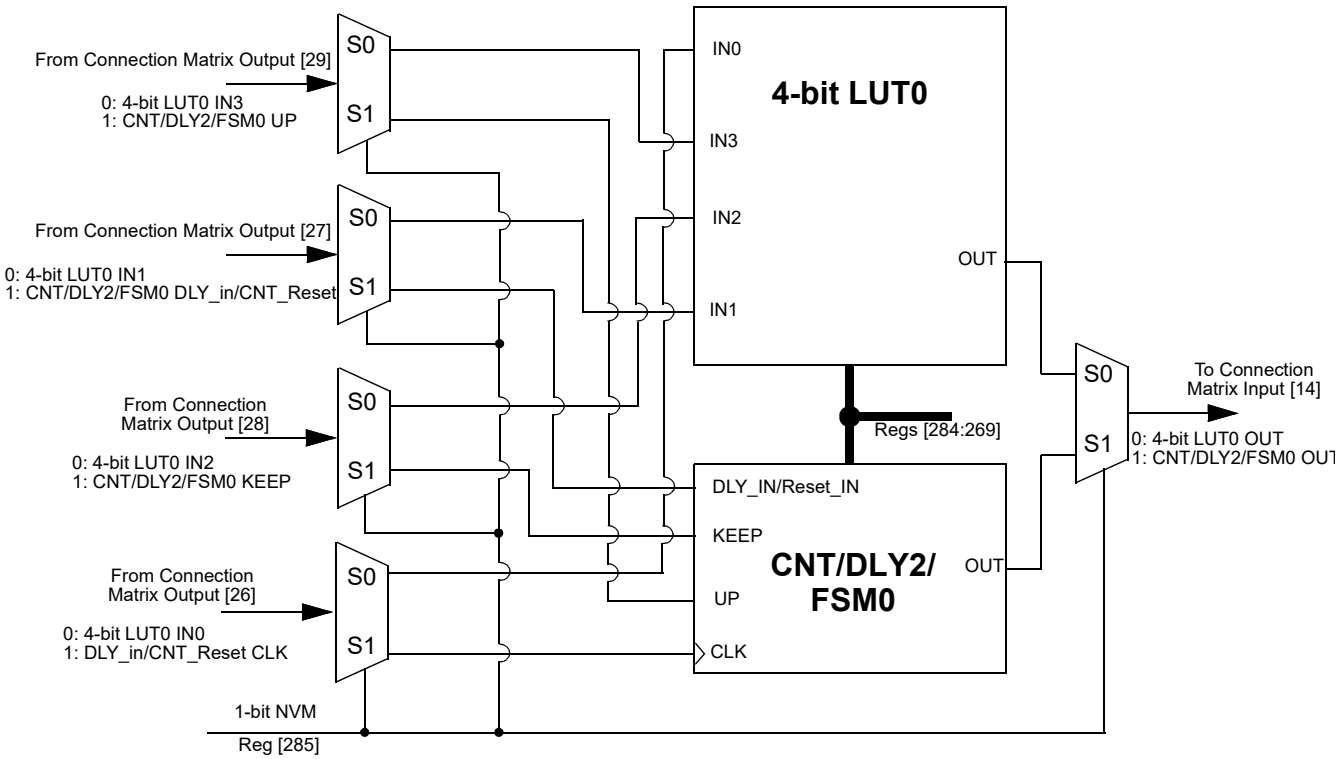


Figure 16. 4-bit LUT1 or CNT/DLY2/FSM0

9.4.1 Counter Mode

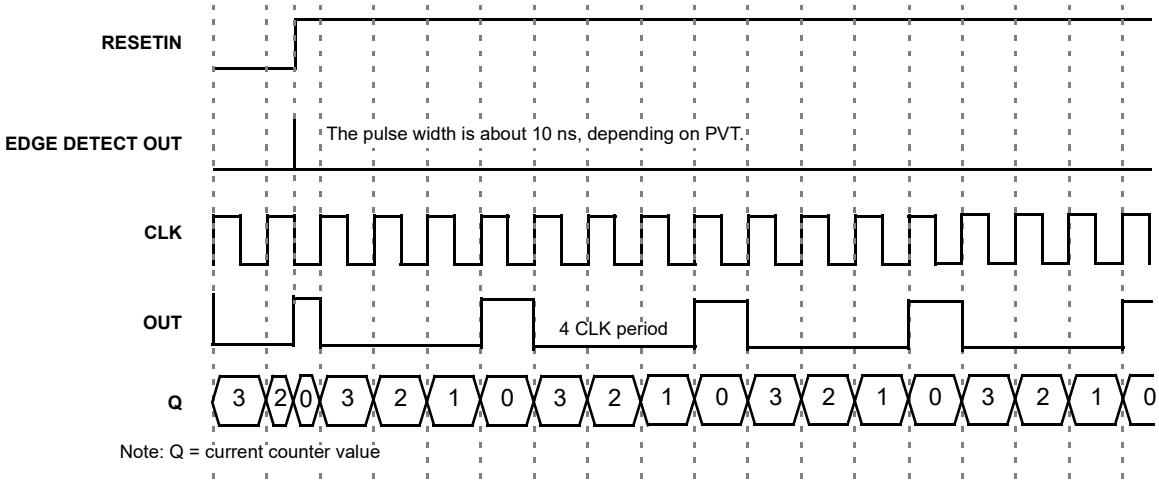


Figure 17. Timing (Reset Rising Edge Mode, Oscillator is Forced On) for Count Data = 3

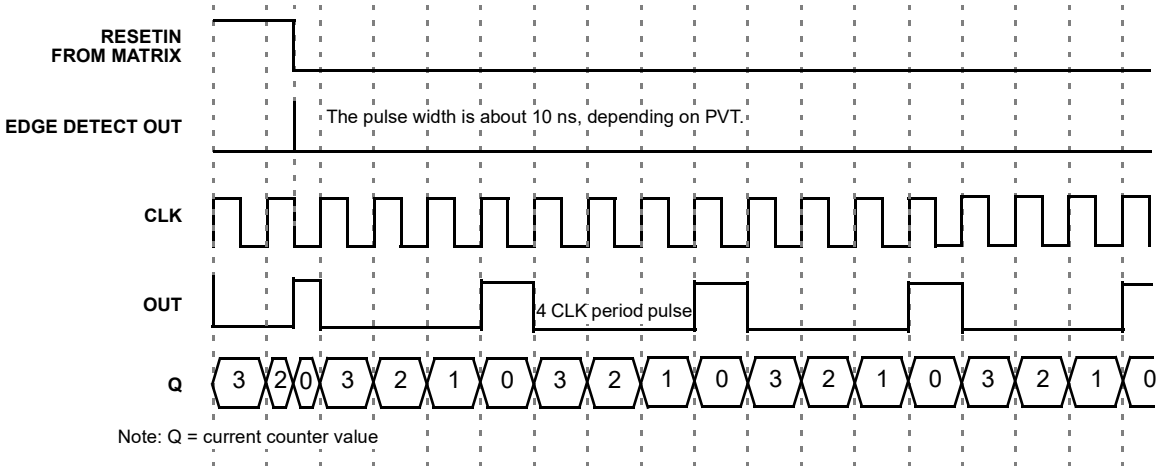


Figure 18. Timing (Reset Falling Edge Mode, Oscillator is Forced On) for Count Data = 3

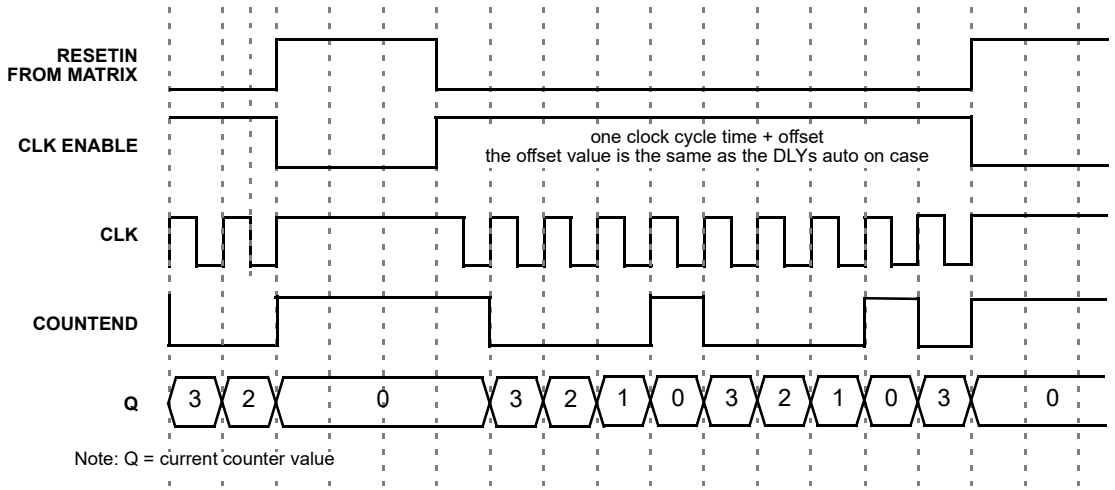


Figure 19. Timing (Reset High Level Mode, Oscillator is Auto Powered On (Controlled by Reset)) for Count Data = 3

9.4.2 FSM Mode

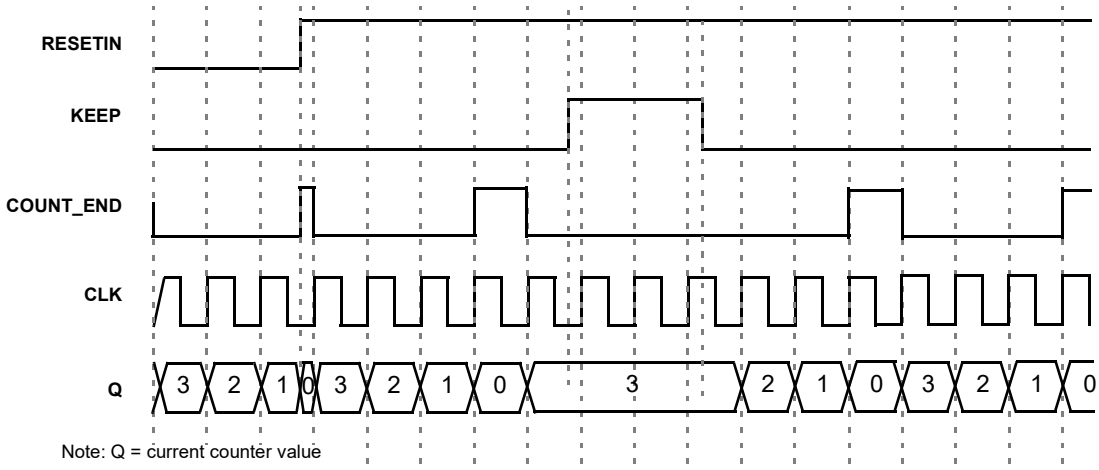


Figure 20. Timing (Reset Rising Edge Mode, Oscillator is Forced On, Up = 0) for Count Data = 3

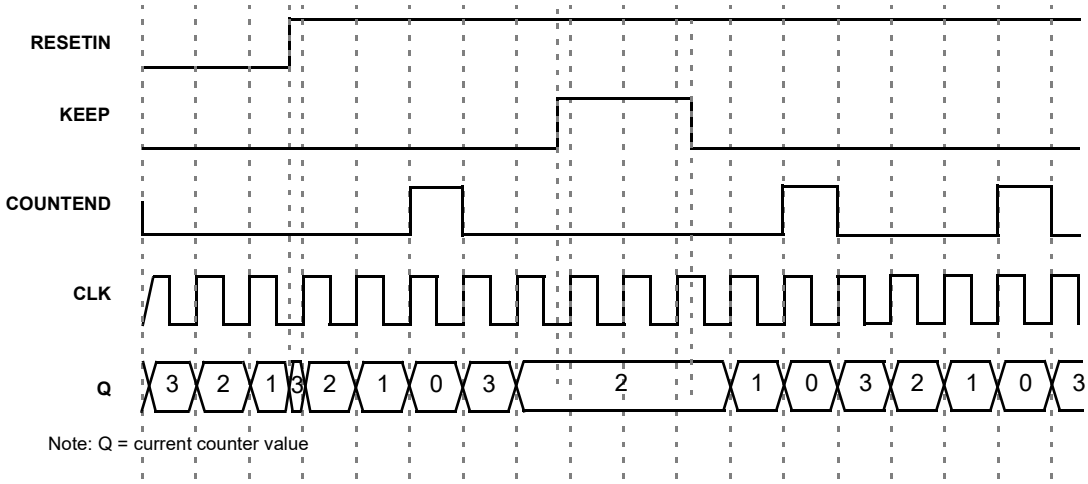


Figure 21. Timing (Set Rising Edge Mode, Oscillator is Forced On, Up = 0) for Count Data = 3

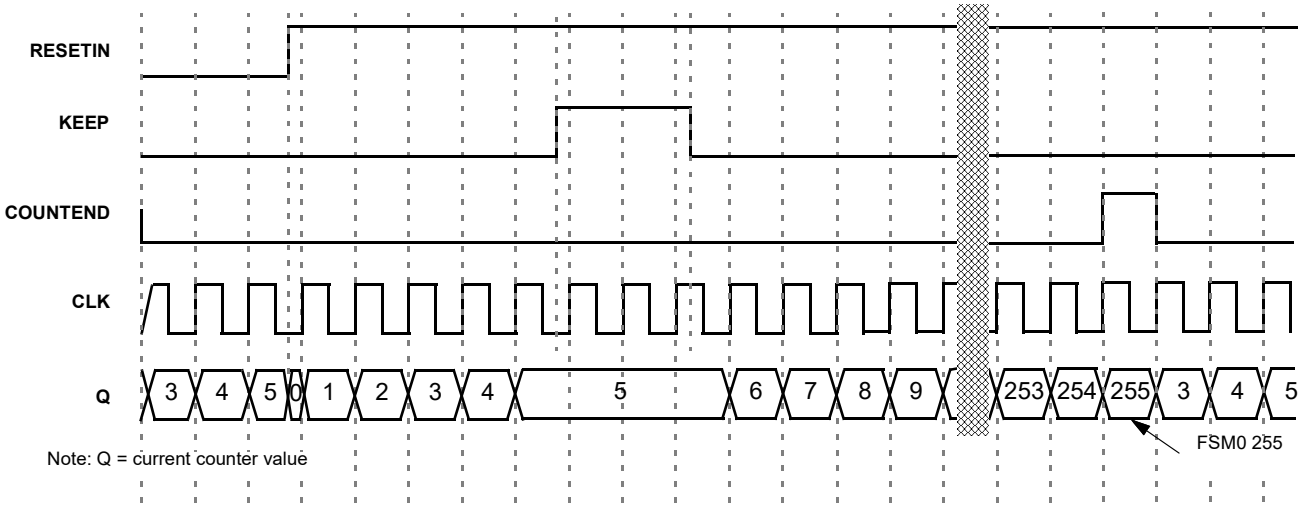


Figure 22. Timing (Reset Rising Edge Mode, Oscillator is Forced On, Up = 1) for Count Data = 3

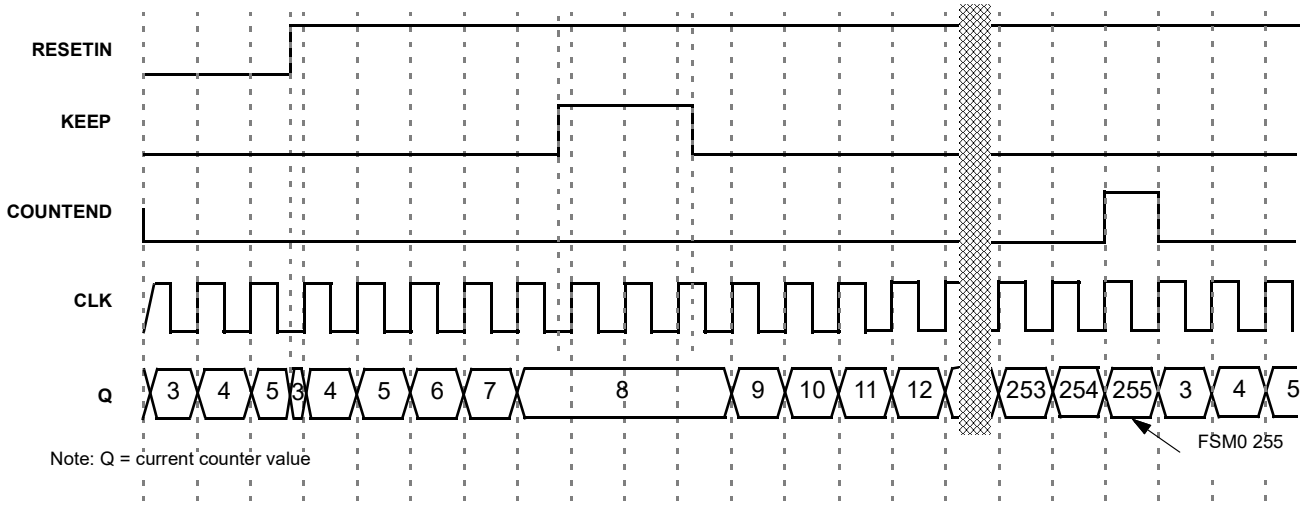


Figure 23. Timing (Set Rising Edge Mode, Oscillator is Forced On, Up = 1) for Count Data = 3

9.4.3 4-Bit LUT or 8-Bit Counter/Delay Macrocell Used as 4-Bit LUT

Table 26. 4-Bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [269]	LSB
0	0	0	1	register [270]	
0	0	1	0	register [271]	
0	0	1	1	register [272]	
0	1	0	0	register [273]	
0	1	0	1	register [274]	
0	1	1	0	register [275]	
0	1	1	1	register [276]	
1	0	0	0	register [277]	
1	0	0	1	register [278]	
1	0	1	0	register [279]	
1	0	1	1	register [280]	
1	1	0	0	register [281]	
1	1	0	1	register [282]	
1	1	1	0	register [283]	
1	1	1	1	register [284]	MSB

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

- 4-Bit LUT0 is defined by registers [284:269].

Table 27. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

9.4.4 4-Bit LUT or 8-Bit Counter/Delay Macrocells Used as 8-Bit Counter/Delay Register Settings

Table 28. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay2 Mode Selection	Register [269]	0: Delay mode 1: Counter mode
Counter/Delay2 Clock Source Select	Registers [272:270]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter1 overflow
Counter/Delay2 Control Data	Registers [280:273]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay2 Mode Select or Asynchronous Counter Reset	Registers [282:281]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high level reset for counter mode
LUT4_0 or Counter2 Select	Register [285]	0: LUT4_0 1: Counter2

9.5 Programmable Delay/Edge Detector

The SLG46108-EV has a programmable time delay logic cell (P DLY) available that can generate a delay that is selectable from one of four timings (width/time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. See Figure 24 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

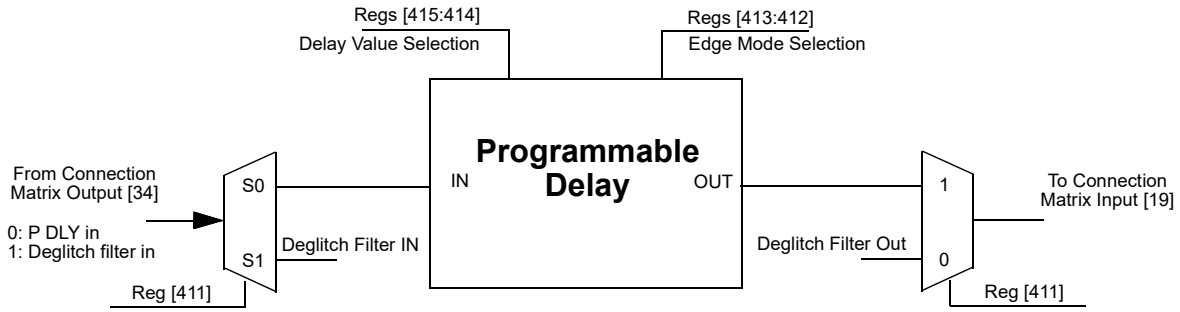


Figure 24. Programmable Delay

9.5.1 Programmable Delay Timing Diagram - Edge Detector Output

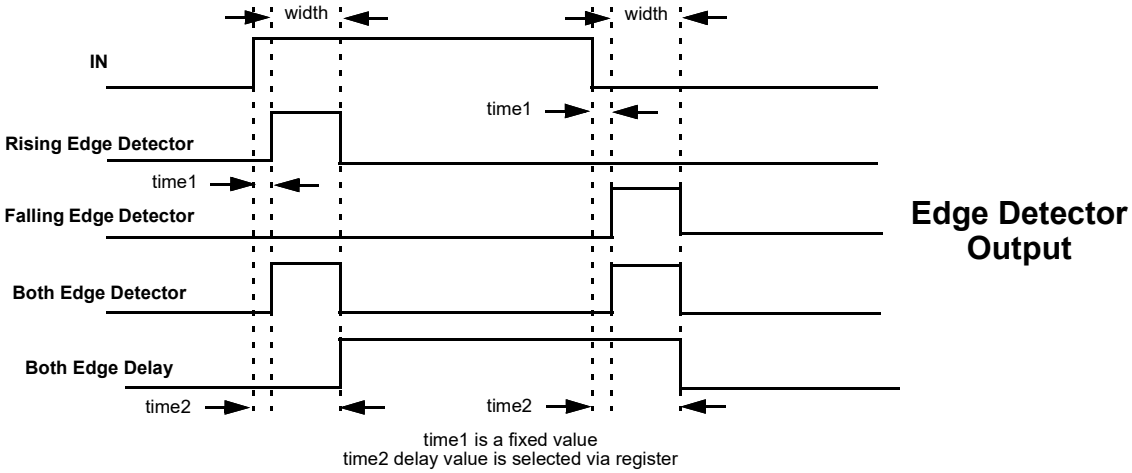


Figure 25. Edge Detector Output

9.5.2 Programmable Delay Register Settings

Table 29. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Programmable Delay or Filter Output Select	Register [411]	0: Programmable delay output 1: Filter output
Select the Edge Mode of Programmable Delay and Edge Detector	Registers [413:412]	00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
Delay Value Select for Programmable Delay and Edge Detector (V_{DD} = 3.3 V, Typical Condition)	Registers [415:414]	00: 140 ns 01: 280 ns 10: 420 ns 11: 560 ns

9.6 Deglitch Filter

The SLG46108-EV has an additional logic function that is connected directly to the Connection Matrix inputs and outputs. There is one deglitch filter. The typical filtered pulse width is shown in section 3.4.5 Typical Filter Rejection Pulse Width.

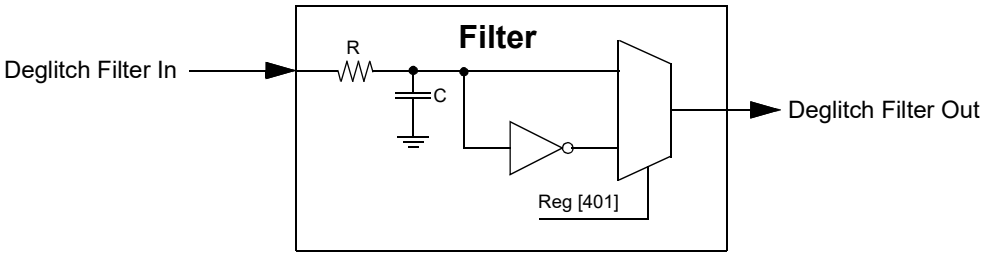


Figure 26. Deglitch Filter

10. Counters/Delay Generators

There are three configurable counters/delay (CNT/DLY) generators in the SLG46108-EV. The three counters/delay generators (CNT/DLY 0, 1, 3) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits.

Two of the counter/delay generator macrocells (CNT/DLY0 and CNT/DLY1) have two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. One of the counter/delay generator macrocells (CNT/DLY3) has one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

Note that there is also one Combination Function Macrocells that can implement either 4-bit LUTs or 8-bit counter/delays. For more information please see section 9.4 4-Bit LUT or 8-Bit Counter/Delay Macrocells.

Note: Counters initialize with counter data after POR.

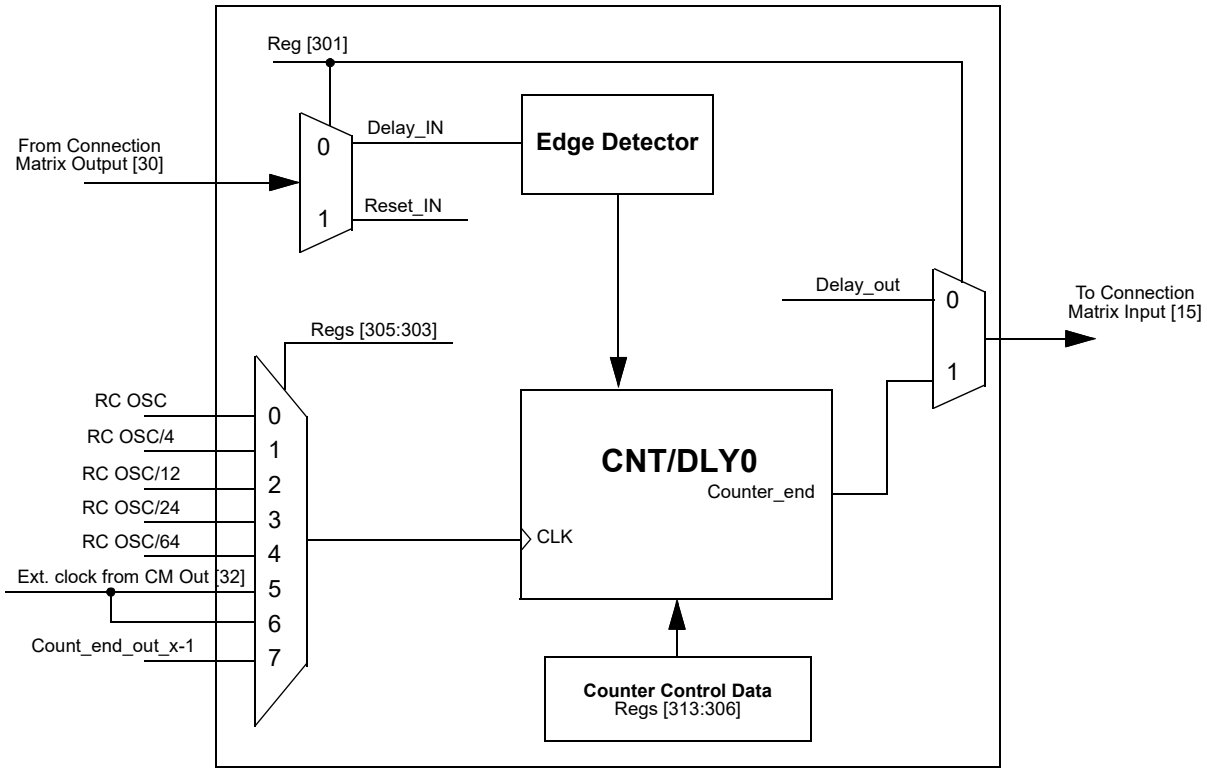


Figure 27. CNT/DLY0

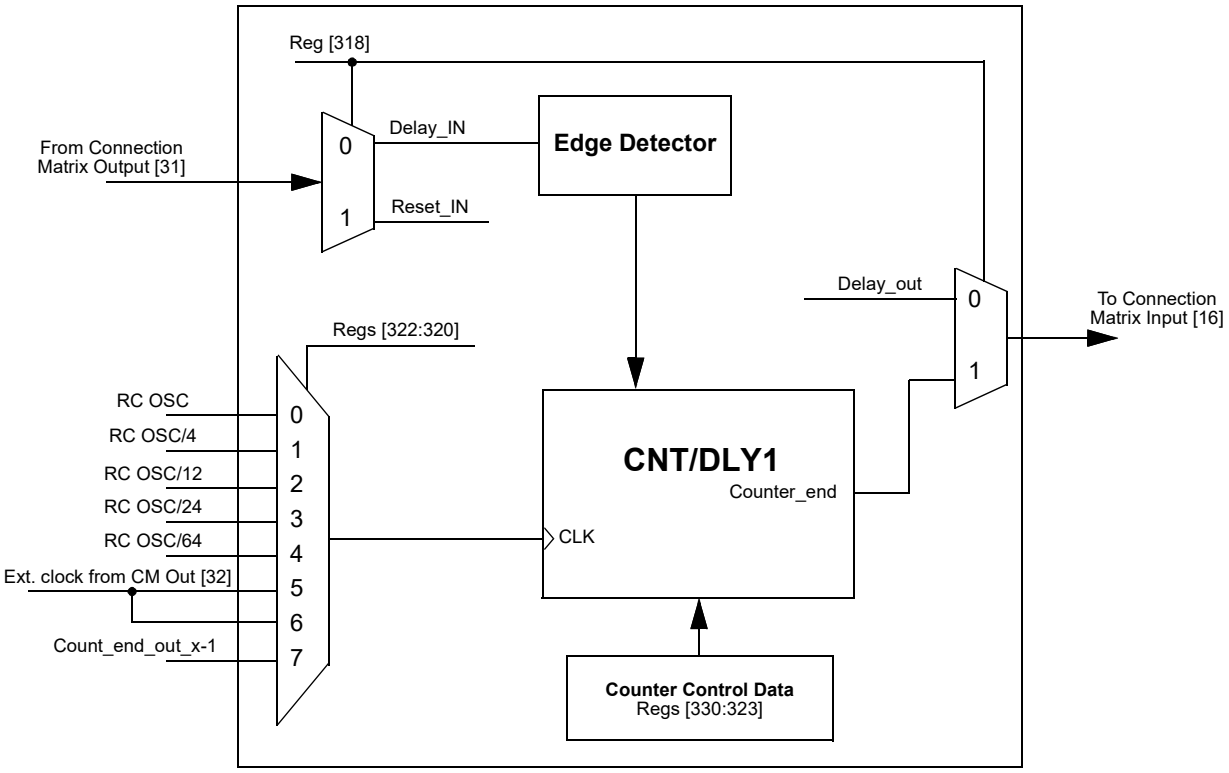


Figure 28. CNT/DLY1

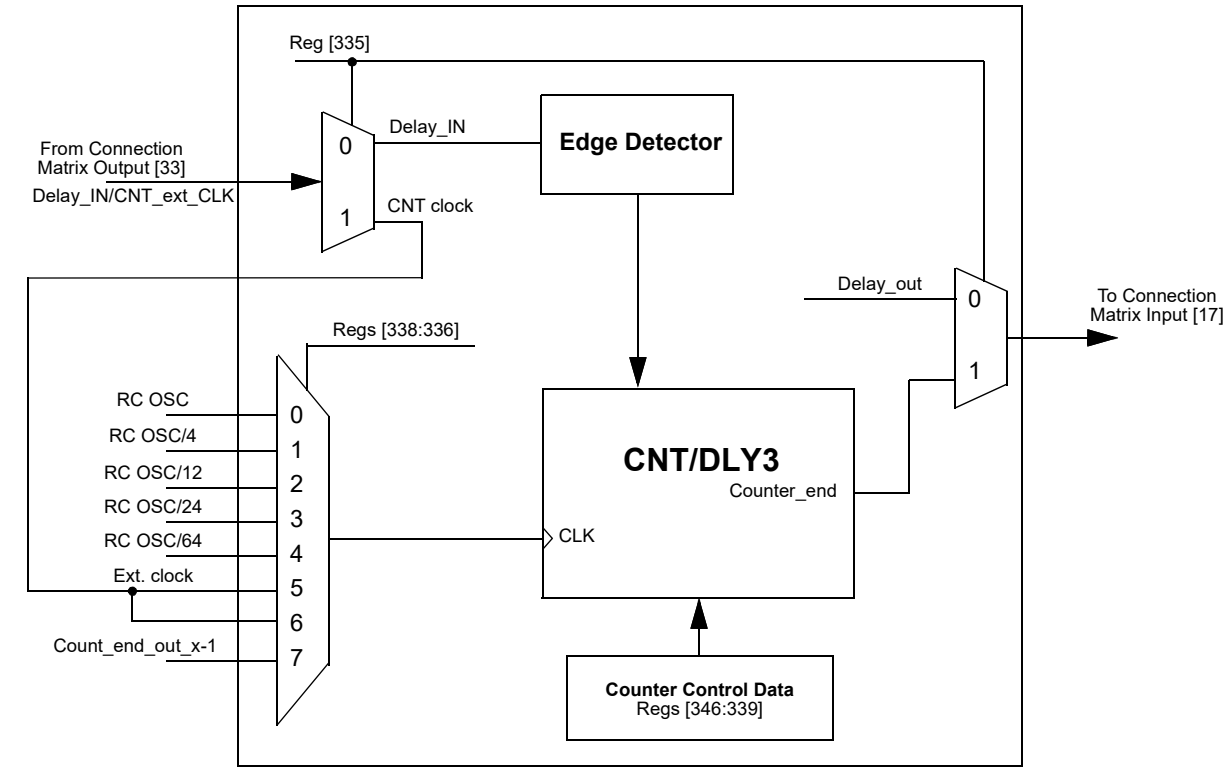


Figure 29. CNT/DLY3

10.1 CNT/DLY0 Register Settings

Table 30. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	Register [301]	0: Delay mode 1: Counter mode
Counter/Delay0 Clock Source Select	Registers [305:303]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter3 overflow
Counter0 Control Data/Delay0 Time Control	Registers [313:306]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay0 Mode Select or Asynchronous Counter Reset	Registers [315:314]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high level reset for counter mode

10.2 CNT/DLY1 Register Settings

Table 31. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	Register [318]	0: Delay mode 1: Counter mode
Counter/Delay1 Clock Source Select (External Clock is only for Counter Mode)	Registers [322:320]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter0 overflow
Counter1 Control Data/Delay1 Time Control	Registers [330:323]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay1 Mode Select or Asynchronous Counter Reset	Registers [332:331]	00: Delay on both falling and rising edges (for delay and counter reset) 01: Delay on falling edge only (for delay and counter reset) 10: Delay on rising edge only (for delay and counter reset) 11: No delay on either falling or rising edges/high level reset for counter mode

10.3 CNT/DLY3 Register Settings

Table 32. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay3 Mode Select	Register [335]	0: Delay mode 1: Counter mode
Counter/Delay3 Clock Source Select (External Clock is only for Counter Mode)	Registers [338:336]	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter2 overflow
Counter3 Control Data/Delay3 Time Control	Registers [346:339]	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay3 Mode Select	Registers [348:347]	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

11. Oscillator

11.1 Oscillator Overview

The SLG46108-EV has two internal RC oscillators (RC OSC), one that runs at 25 kHz and one that runs at 2 MHz. When using the chip internal RC OSC, a choice is available to “Force Power-On”, meaning that the RC OSC will always run, or “Auto Power-On”, meaning that the RC OSC will have an associated startup and settling time associated with it (offset).

The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (Pin 8). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider (pre-divider) allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. There are two second stage divider controls (OUT0 and OUT1). Each has its own input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines [20] and [21]. See Figure 30 for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

11.2 RC OSC Block Diagram

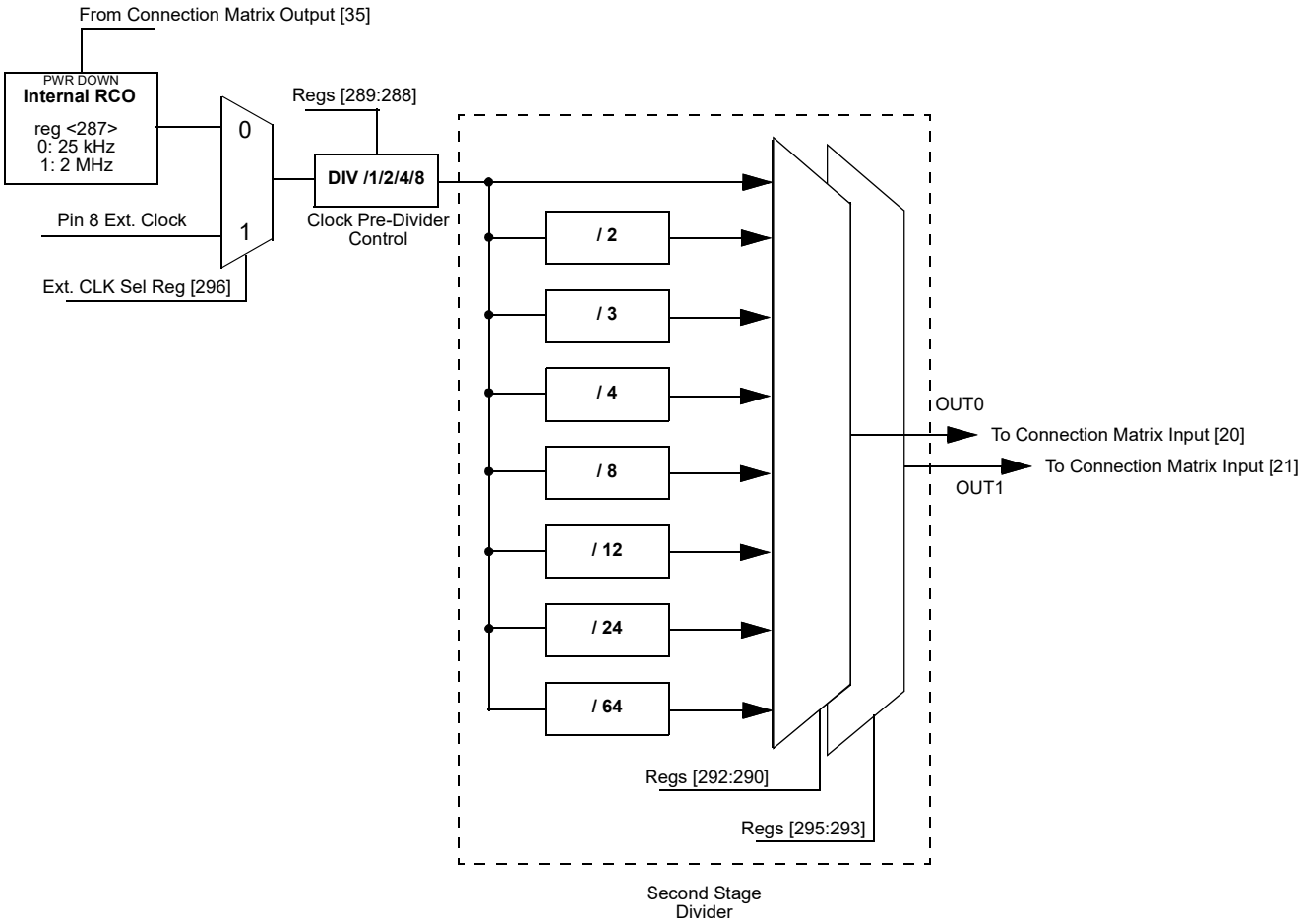


Figure 30. RC OSC Block Diagram

11.3 Oscillator Power-On Delay

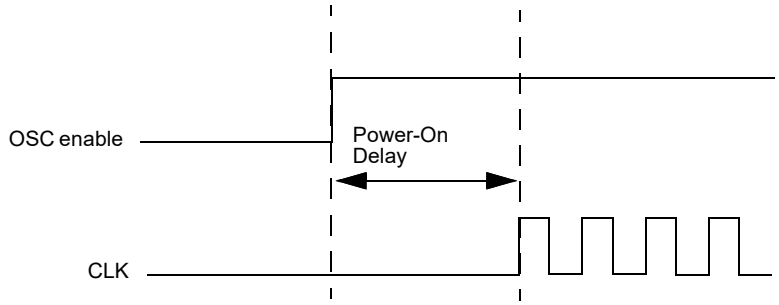


Figure 31. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.
Note 2: OSC enable” signal appears when any macrocell that uses OSC is powered on.

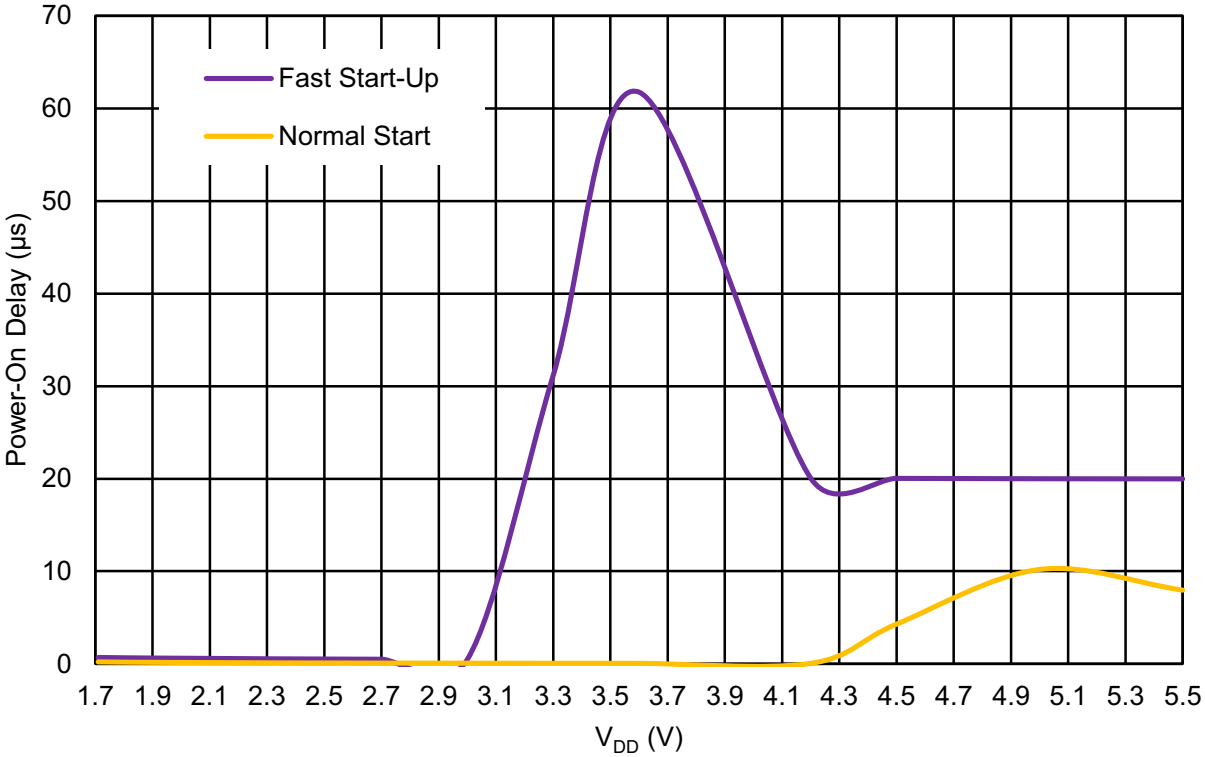


Figure 32. Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC = 25 kHz

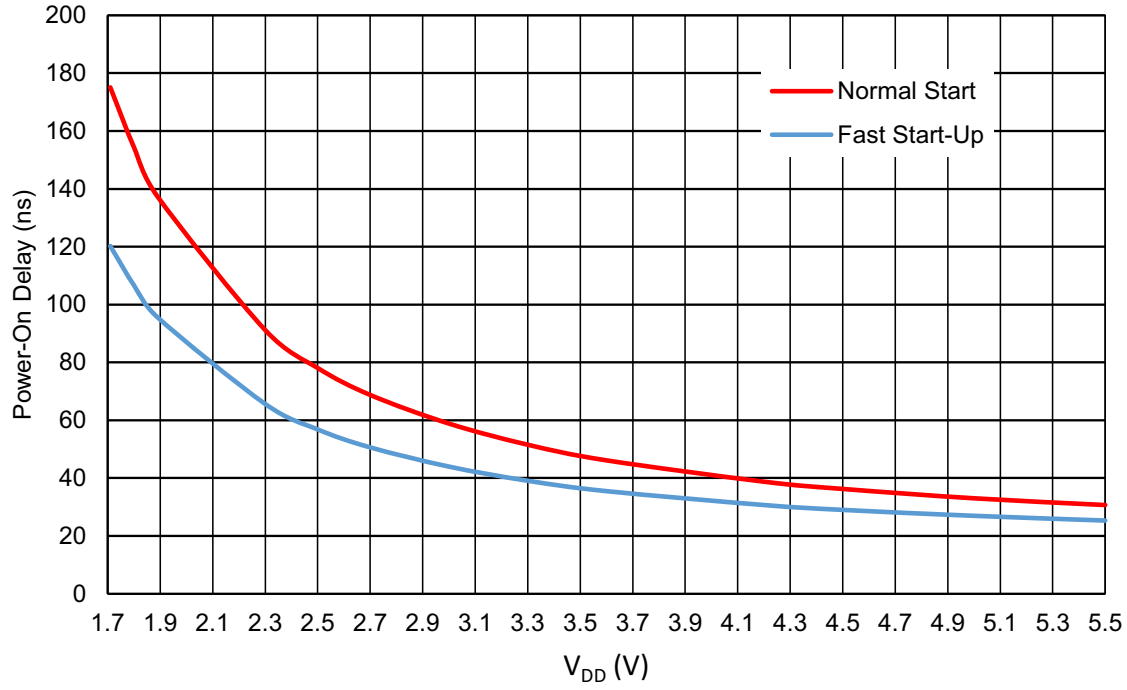


Figure 33. Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC = 2 MHz

11.4 Oscillator Accuracy

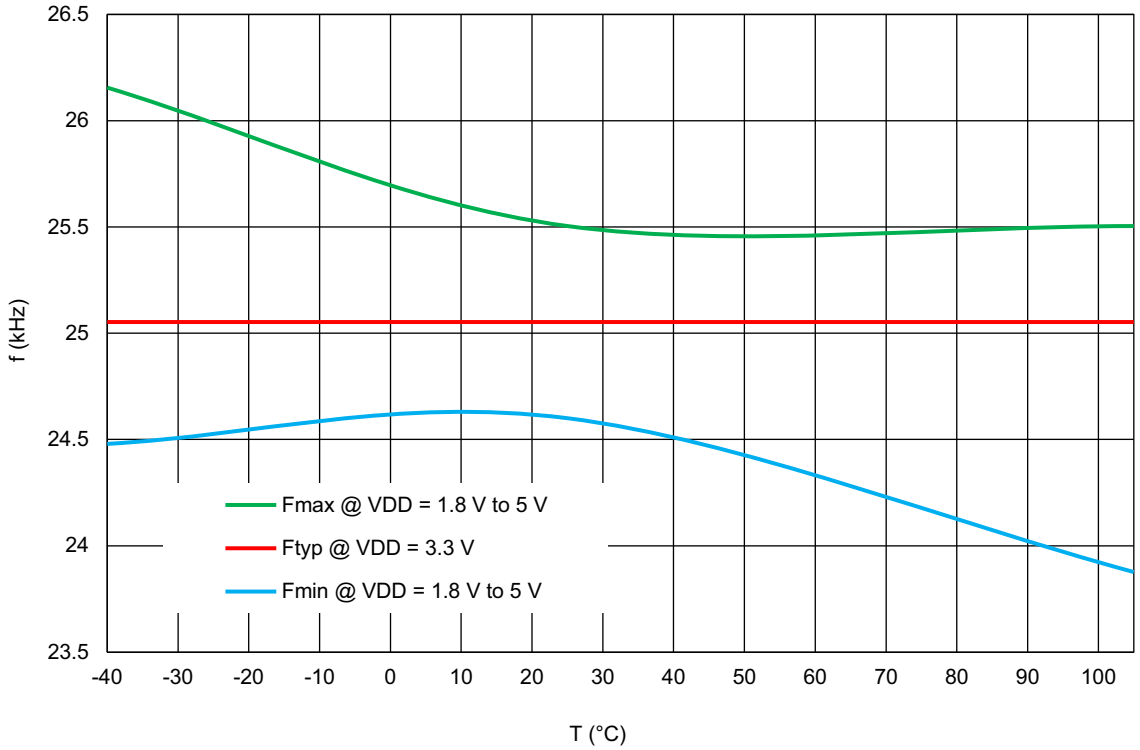


Figure 34. RC Oscillator Frequency vs. Temperature, OSC = 25 kHz

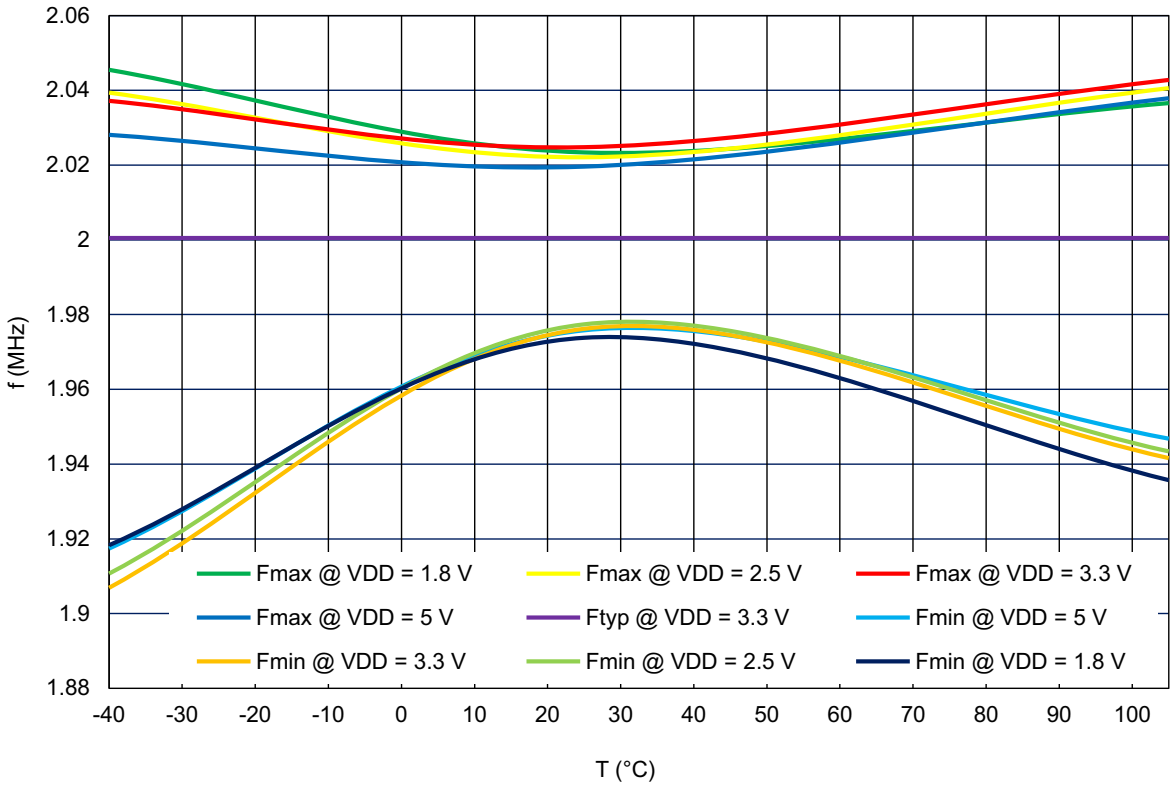


Figure 35. Oscillator Frequency vs. Temperature, OSC = 2 MHz

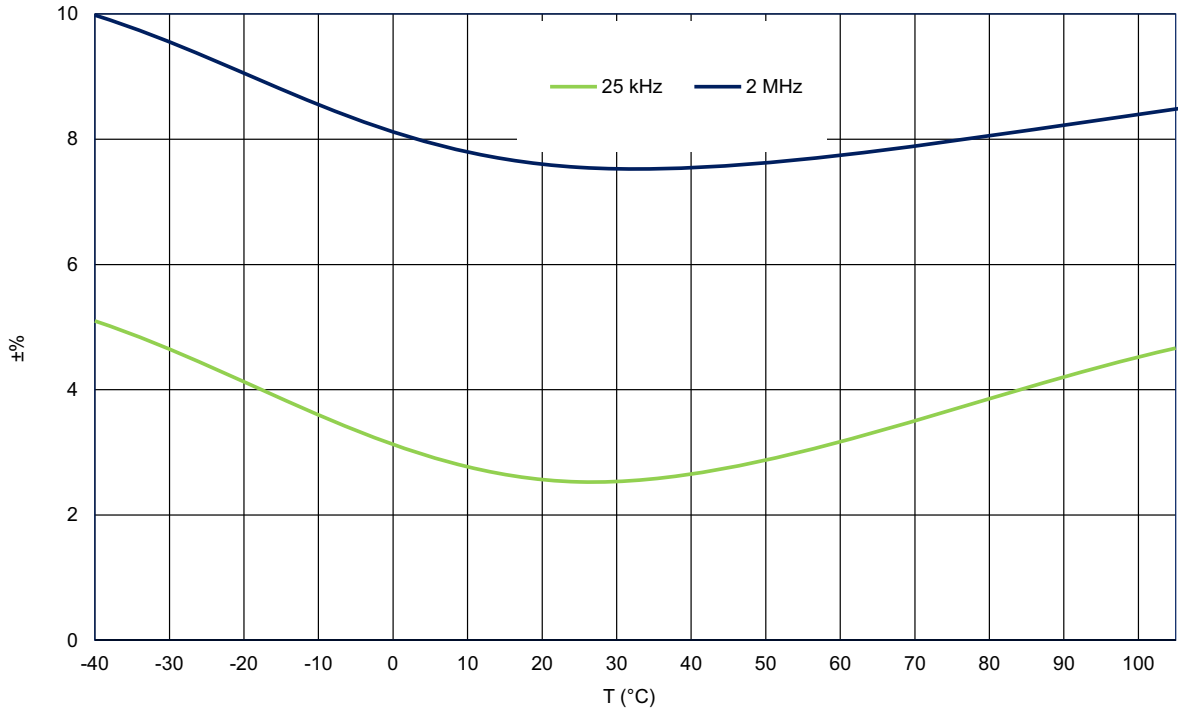


Figure 36. Oscillators Total Error vs. Temperature

11.5 Oscillator Settling Time

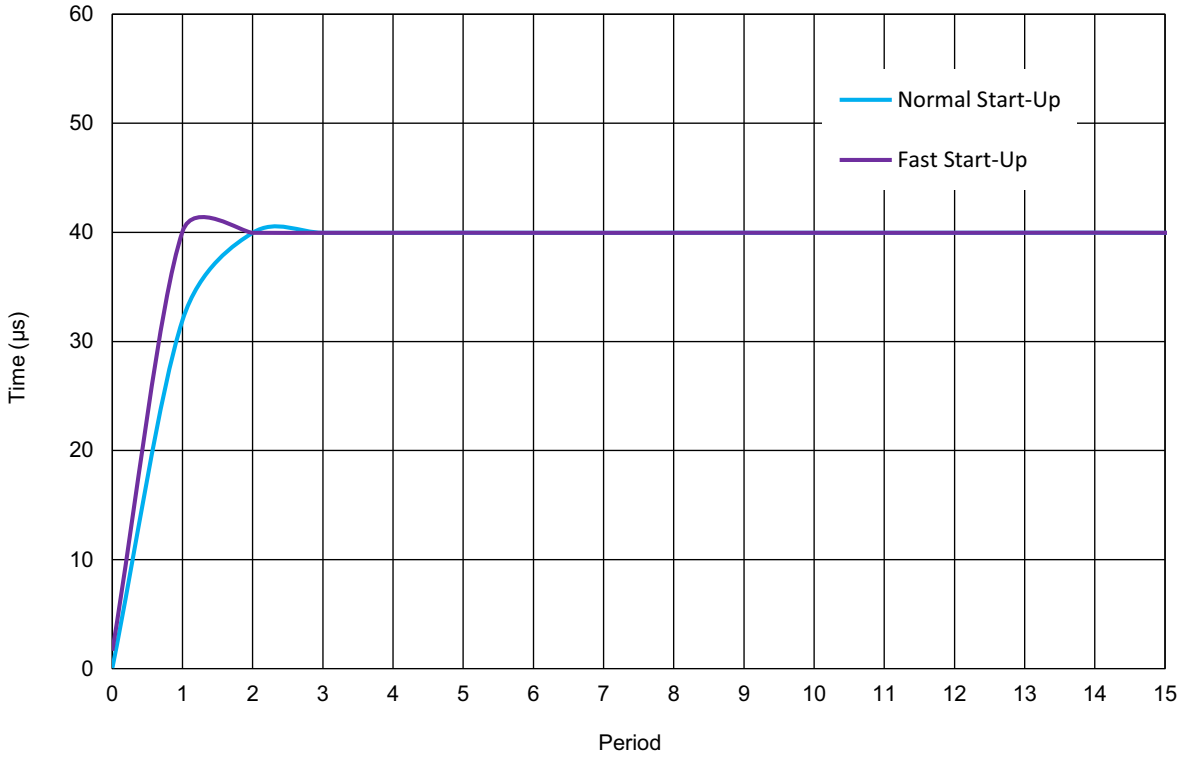


Figure 37. Oscillator Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC = 25 kHz

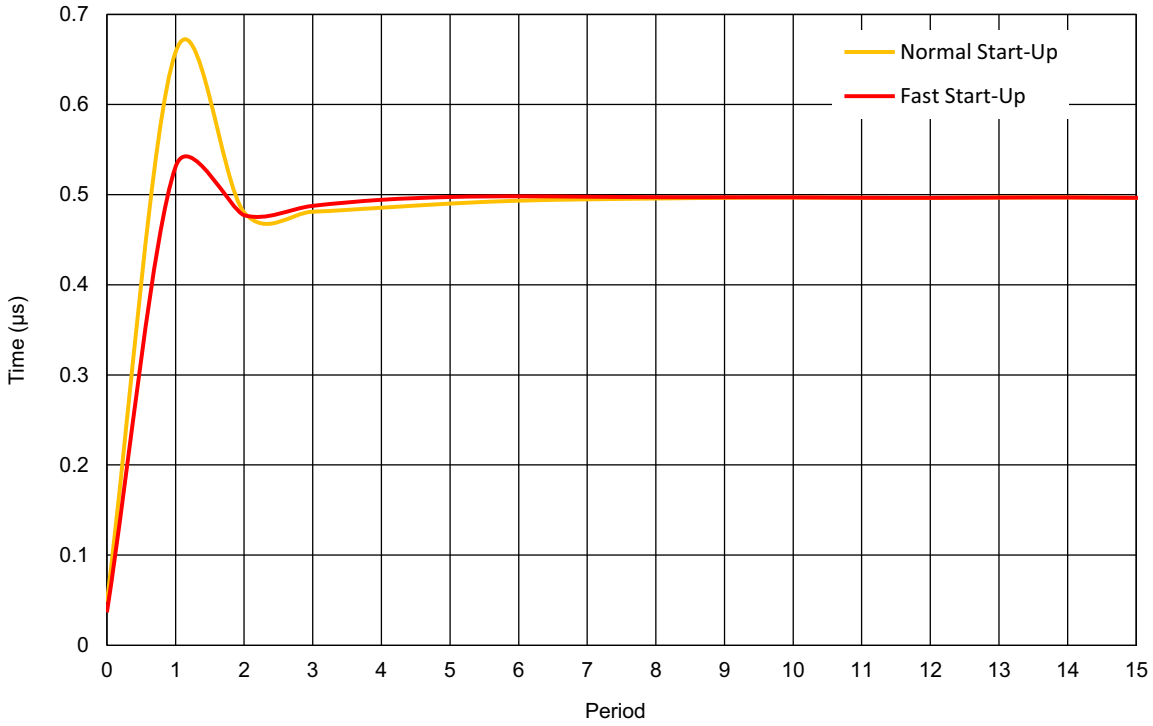


Figure 38. Oscillator Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC = 2 MHz

12. Power-On Reset

The SLG46108-EV has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IO pins.

12.1 General Operation

To start the POR sequence in the SLG46108-EV, the voltage applied on the V_{DD} should be higher than the Power-On Threshold **(Note 1)**. The full operational V_{DD} range for the SLG46108-EV is 1.71 V – 5.5 V (1.8 V ±5 % - 5 V±10 %). This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG46108-EV will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

The SLG46108-EV is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN1) is less than 0.6 V, but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher **(Note 2)** than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: The Power-On Threshold can vary by PVT, but typically it is 1.6 V.

Note 2: There is a 0.5 V margin due to forward drop voltage of the ESD protection diodes.

To power down the chip, the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than 0.6 V.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on PINs cannot be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

12.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 39.

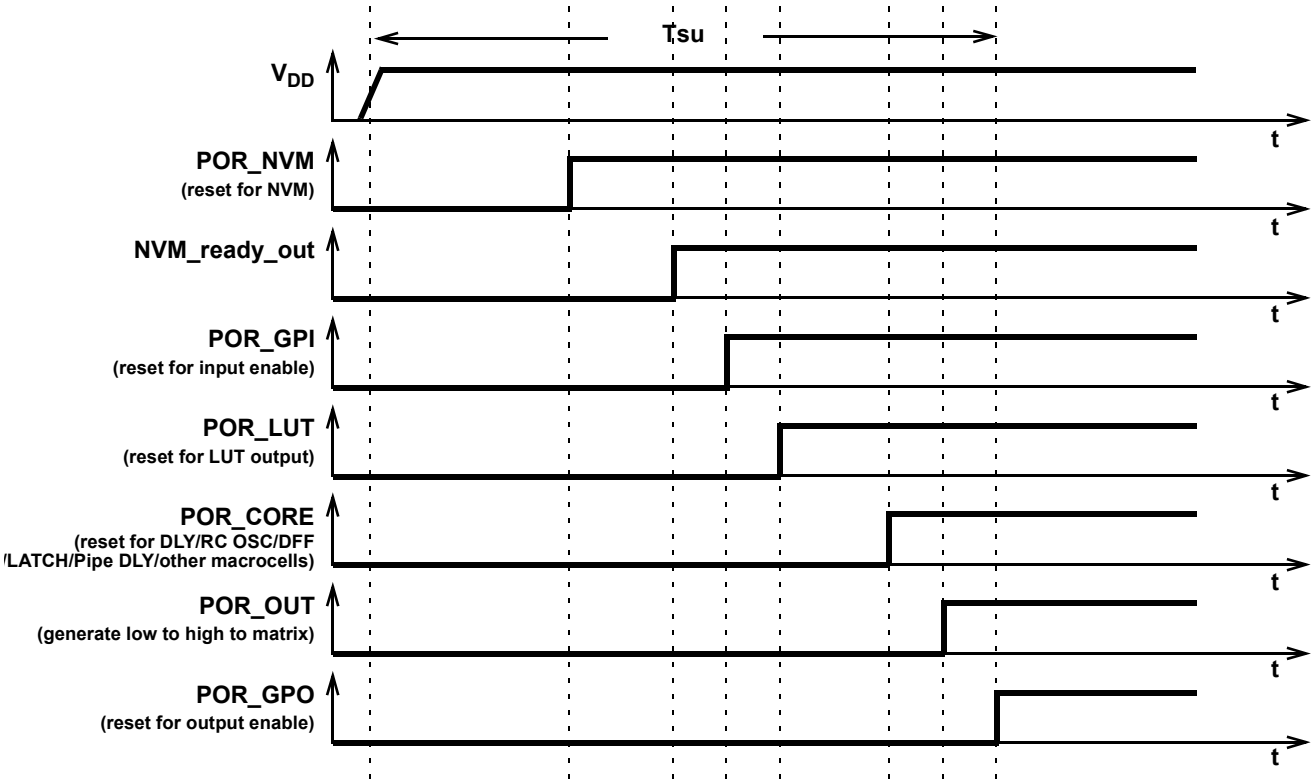


Figure 39. POR Sequence

As can be seen from Figure 39 after the V_{DD} has start ramping up and crosses the Power-On Threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to SRAM registers that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs, the Delay cells, RC OSC, DFFs, LATCHEs, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

12.3 Macrocells Output States during POR Sequence

To have a full picture of SLG46108-EV operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 40 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P DLY macrocell configured as edge detector becomes active at this time. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

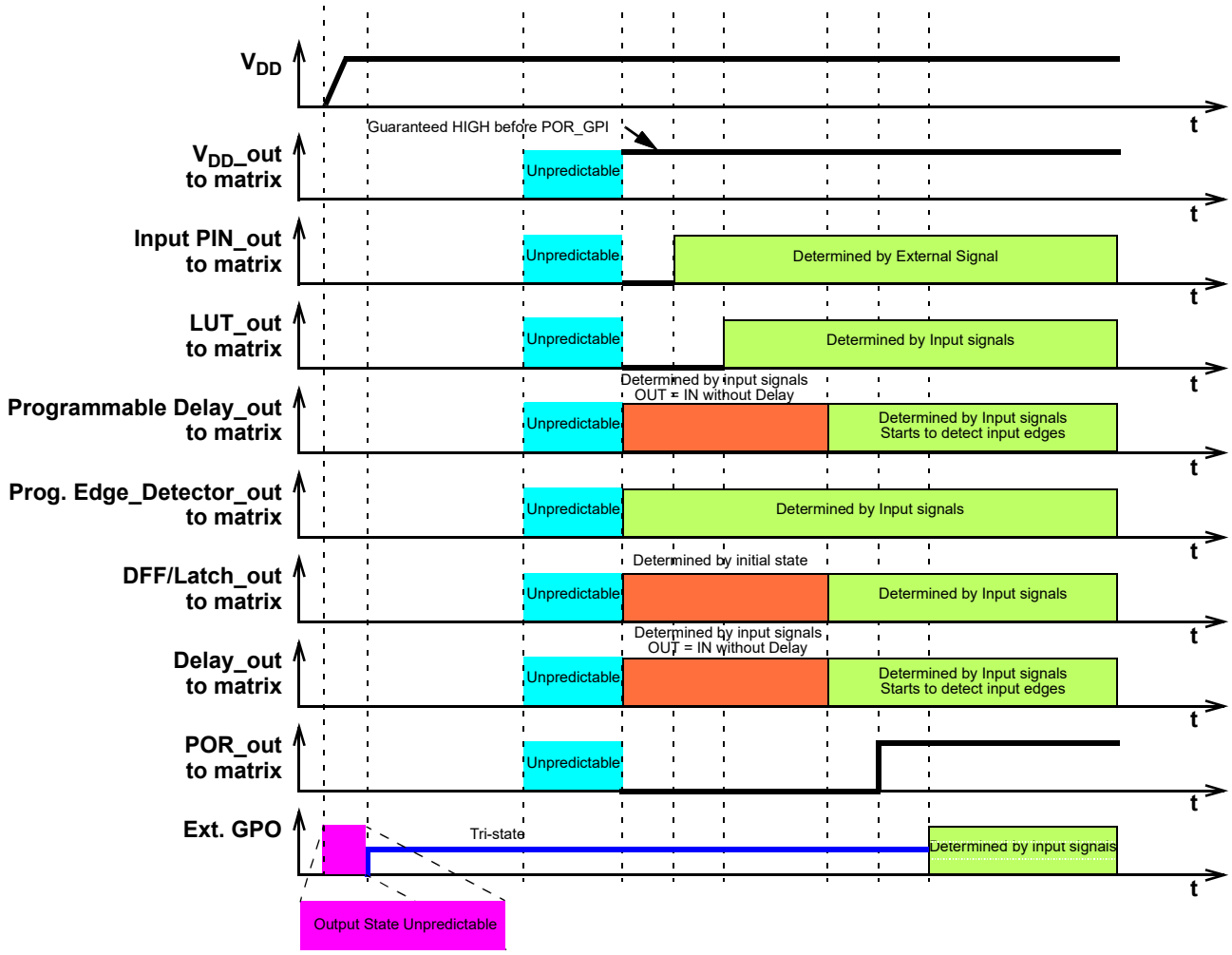


Figure 40. Internal Macrocell States during POR Sequence

13. Register Definitions

13.1 Register Map

Table 33. Register Map

Register Bit Address	Signal Function	Register Bit Definition
4:0	Pin3 digital out source	
9:5	Pin4 digital out source	
14:10	Pin4 output enable	
19:15	in0 of LUT2_0 (Clock Input of DFF0)	
24:20	in1 of LUT2_0 (Data Input of DFF0)	
29:25	in0 of LUT2_1 (Clock Input of DFF1)	
34:30	in1 of LUT2_1 (Data Input of DFF1)	
39:35	in0 of LUT2_2	
44:40	in1 of LUT2_2	
49:45	in0 of LUT2_3	
54:50	in1 of LUT2_3	
59:55	in0 of LUT3_0 (Clock Input of DFF2 with nReset/nSet)	
64:60	in1 of LUT3_0 (Data input of DFF2 with nReset/nSet)	
69:65	in2 of LUT3_0 (Resetb or Setb of DFF2 with nReset/nSet)	
74:70	in0 of LUT3_1 (Clock Input of DFF3 with nReset/nSet)	
79:75	in1 of LUT3_1 (Data input of DFF3 with nReset/nSet)	
84:80	in2 of LUT3_1 (Resetb or Setb of DFF3 with nReset/nSet)	
89:85	in0 of LUT3_2	
94:90	in1 of LUT3_2	
99:95	in2 of LUT3_2	
104:100	in0 of LUT3_3	
109:105	in1 of LUT3_3	
114:110	in2 of LUT3_3	
119:115	in0 of LUT3_4 (Input of Pipe Delay)	
124:120	in1 of LUT3_4 (Resetb of Pipe Delay)	
129:125	in2 of LUT3_4 (Clock of Pipe Delay)	
134:130	in0 of LUT4_0 (Input for Delay2 ext. clock or Counter2 external Clock)	
139:135	in1 of LUT4_0 (Input for delay2 or counter2 reset input)	
144:140	in2 of LUT4_0 (Input for counter2 FSM keep signal)	
149:145	in3 of LUT4_0 (Input for counter2 FSM up signal)	
154:150	Input for delay0 or counter0 reset input	

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
159:155	Input for delay1 or counter1 reset input	
164:160	Input for Delay 0/1(Counter 0/1) external clock	
169:165	Input for delay3 or counter3 reset input	
174:170	Input for programmable delay (deglitch filter input)	
179:175	Power down for osc. (higher priority) (high = power down).	
184:180	Pin6 digital out source	
189:185	Pin7 digital out source	
194:190	Pin8 digital out source	
199:195	Pin8 output enable	
207:200	Reserved	
LUT2		
208	DFF0 or LATCH select/LUT 2_0 <0>	0: DFF function 1: Latch function
209	LUT 2_0 <1>	
210	DFF0 initial polarity select/LUT 2_0 <2>	0: Low 1: High
211	LUT 2_0 <3>	
212	DFF1 or Latch select/LUT 2_1 <0>	0: DFF function 1: Latch function
213	LUT 2_1 <1>	
214	DFF1 initial polarity select/LUT 2_1 <2>	0: Low 1: High
215	LUT 2_1 <3>	
219:216	LUT2_2 data	
223:220	LUT2_3 data	
224	LUT2_0 or DFF/Latch_0 select	0: LUT2_0 1: DFF4
225	LUT2_1 or DFF/Latch_1 select	0: LUT2_1 1: DFF5
LUT3		
226	DFF2 or LATCH select/LUT 3_0 <1>	0: DFF function 1: LATCH function
227	LUT 3_0 <2>	
228	DFF2 rstb/setb select/LUT 3_0 <3>	0:resetb from matrix output 1:setb from matrix output
229	DFF2 initial polarity select/LUT 3_0 <4>	0: Low 1: High
233:230	LUT 3_0 <7:5>	

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
234	DFF3 or LATCH select / LUT 3_1 <1>	0: DFF function 1: Latch function
235	LUT 3_1 <2>	
236	DFF3 rstb/setb select/LUT 3_1 <3>	0: resetb from matrix output 1: setb from matrix output
237	DFF3 initial polarity select/LUT 3_1 <4>	0: Low 1: High
241:238	LUT 3_1 <7:5>	
249:242	LUT3_2 data	
257:250	LUT3_3 data	
265:258	LUT3_4 data or pipe number select	registers [260:258]: OUT0 select registers [263:261]: OUT1 select
266	LUT3_0 or DFF/Latch_2 (with nReset/nSet) select	0:LUT3_0 1:DFF2
267	LUT3_1 or DFF/Latch_3 (with nReset/nSet) select	0: LUT3_1 1: DFF3
268	LUT3_4 or Pipe Delay select	0: LUT3_4 1: Pipe Delay
LUT4		
284:269	LUT4_0 data or:	
269	Counter/Delay2 mode selection	0: Delay mode 1: Counter mode
272:270	Counter/Delay2 Clock Source select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter1 overflow
280:273	Counter/Delay2 Control Data	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
282:281	Delay2 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay and counter reset) 01: on falling edge only (for delay and counter reset) 10: on rising edge only (for delay and counter reset) 11: no delay on either falling or rising edges/high level reset for counter mode
283	Counter2/FSM2's Q are set to Data or Reset to 0s selection	0: Reset to 0 1: Set to data
285	LUT4_0 or counter_2 select	0: LUT4_0 1: Counter2

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
OSC		
286	Force oscillator on	0: Auto Power-on 1: Force Power-on
287	Oscillator frequency control	0: 25 k 1: 2 M
289:288	OSC clock pre-divider	00: div1 01: div2 10: div4 11: div8
292:290	Internal oscillator divider frequency control 1	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
295:293	Internal oscillator divider frequency control 2	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64
296	External Clock Source Select	0: Internal oscillator 1: External clock from Pin8
297	Reserved	
298	OSC Clock 25 KHz/2 MHz to matrix input [20] enable	
299	OSC Clock 25 KHz/2 MHz to matrix input [21] enable	
300	OSC Fast Start-Up Enable for 25 KHz/2 MHz	
CNT/DLY		
301	Counter/Delay0 (8bits) mode select	0: Delay mode 1: Counter mode
302	Reserved	
305:303	Counter/delay0 Clock Source select	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter3 overflow

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
313:306	Counter0 Control Data/Delay0 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
315:314	Delay0 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay and counter reset) 01: on falling edge only (for delay and counter reset) 10: on rising edge only (for delay and counter reset) 11: no delay on either falling or rising edges/high level reset for counter mode
317:316	Reserved	
318	Counter/Delay1 (8bits) mode select	0: Delay mode 1: Counter mode
319	Reserved	
322:320	Counter/Delay1 Clock Source select (external clock is only for counter mode)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter0 overflow
330:323	Counter1 Control Data/Delay1 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
332:331	Delay1 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay and counter reset) 01: on falling edge only (for delay and counter reset) 10: on rising edge only (for delay and counter reset) 11: no delay on either falling or rising edges/high level reset for counter mode
334:333	Reserved	
335	Counter/Delay3 (8bits) mode select	0: Delay mode 1: Counter mode
338:336	Counter/Delay3 Clock Source select (external clock is only for counter mode)	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External clock 110: Reserved 111: Counter2 Ooverflow
346:339	Counter3 Control Data/Delay3 Time Control	1-255: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
348:347	Delay3 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
PIN 2		
350:349	Pin2 Mode control	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low voltage digital input 11: Reserved
352:351	Pin2 Pull-down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
PIN 3		
355:353	Pin3 Mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
357:356	Pin3 Pull-up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
358	Pin3 Pull-up/down resistor enable.	0: Pull-down resistor enable 1: Pull-up resistor enable
359	Pin3 Driver strength selection	0: 1x 1: 2x
PIN 4		
361:360	Pin4 Mode control (sig_pin4_oe = 0)	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low voltage digital input 11: Reserved
363:362	Pin4 Mode control (sig_pin4_oe = 1)	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain NMOS 1x 11: Open-drain NMOS 2x
365:364	Pin4 Pull-up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
366	Pin4 Pull-up/down resistor enable	0: Pull-down resistor enable 1: Pull-up resistor enable
367	Reserved	
PIN 6		
370:368	Pin6 Mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
372:371	Pin6 Pull-up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
373	Pin6 Pull-up/down resistor enable.	0: Pull-down resistor enable 1: Pull-up resistor enable
374	Pin6 Driver strength selection	0: 1x 1: 2x
PIN 7		
377:375	Pin7 Mode control	000: Digital input without Schmitt trigger 001: Digital input with Schmitt trigger 010: Low voltage digital input 011: Reserved 100: Push-pull 101: Open-drain NMOS 110: Open-drain PMOS 111: Reserved
379:378	Pin7 Pull-up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
380	Pin7 Pull-up/down resistor enable.	0: Pull-down resistor enable 1: Pull-up resistor enable
381	Pin7 Driver strength selection	0: 1x 1: 2x
PIN 8		
383:382	Pin8 Mode control (sig_pin8_oe = 0)	00: Digital input without Schmitt trigger 01: Digital input with Schmitt trigger 10: Low voltage digital input 11: Reserved

Table 33. Register Map (Cont.)

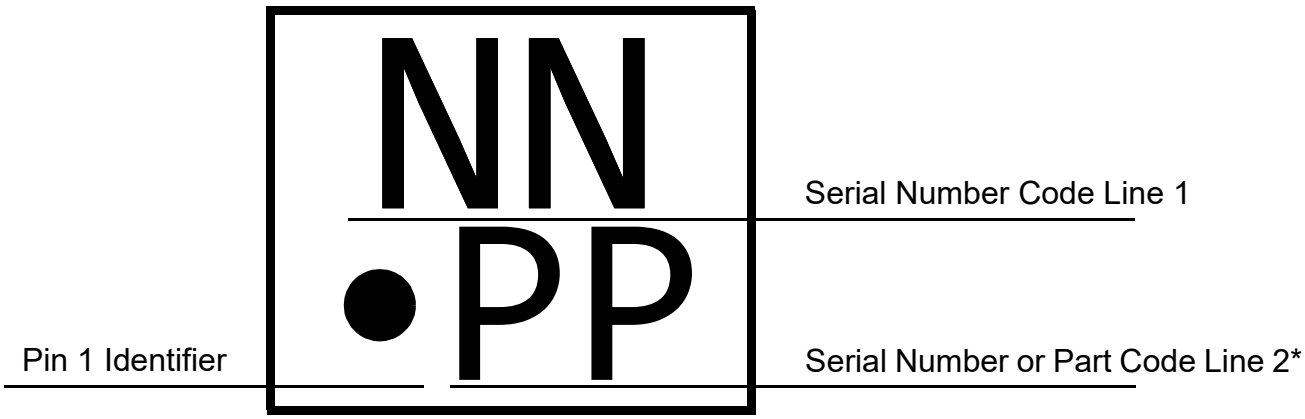
Register Bit Address	Signal Function	Register Bit Definition
385:384	Pin8 Mode control (sig_pin8_oe = 1)	00: Push-pull 1x 01: Push-pull 2x 10: Open-drain NMOS 1x 11: Open-drain NMOS 2x
387:386	Pin8 Pull-up/down resistor value selection.	00: Floating 01: 10 K 10: 100 K 11: 1 M
388	Pin8 Pull-up/down resistor enable.	0: Pull-down resistor enable 1: Pull-up resistor enable
390:389	Reserved	
Quick Charge		
391	GPIO quick charge enable	0: Disable 1: Enable
Pipe Delay		
392	Pipe Delay OUT1 polarity select bit	0: Non-inverted 1: Inverted
Pattern ID		
400:393	8-bit pattern id	
Deglitch Filter		
401	Deglitch filter out polarity selection	0: Non-inverted 1: Inverted
Misc.		
402	NVM data read disable	0: Disable (read enable) 1: Enable (read disable)
403	NVM power-down (or NVM data programming disable)	0: None (or programming enable) 1: Power-down (or programming disable)
405:404	Reserved	
406	Reserved	
407	Reserved	
Pipe Delay and Edge Detector		
408	Pin2 Edge Detect Mode	0: Rising edge 1: Falling edge
409	Pin2 Bypass the pin2	0: PIN2 edge active 1: PIN2 high active
410	PIN2 Reset enable	0: Disable 1: Enable
411	Programmable delay or filter output select	0: Programmable delay output 1: Filter output

Table 33. Register Map (Cont.)

Register Bit Address	Signal Function	Register Bit Definition
413:412	Select the edge mode of programmable delay with edge detector	00: Rising edge detector 01: Falling edge detector 10: Both edge detector 11: Both edge delay
415:414	Delay value select for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	00: 135 ns 01: 270 ns 10: 405 ns 11: 540 ns
423:416	Reserved	
431:424	Reserved	
437:432	Reserved	
439:438	Reserved	
445:440	Reserved	
447:446	Reserved	
448	Reserved	
449	Reserved	
450	Reserved	
451	Reserved	
455:452	Reserved	
463:456	Reserved	

14. Package Top Marking Definitions

14.1 STQFN-8L 1.0 mm x 1.2 mm 0.4P FC Green Package



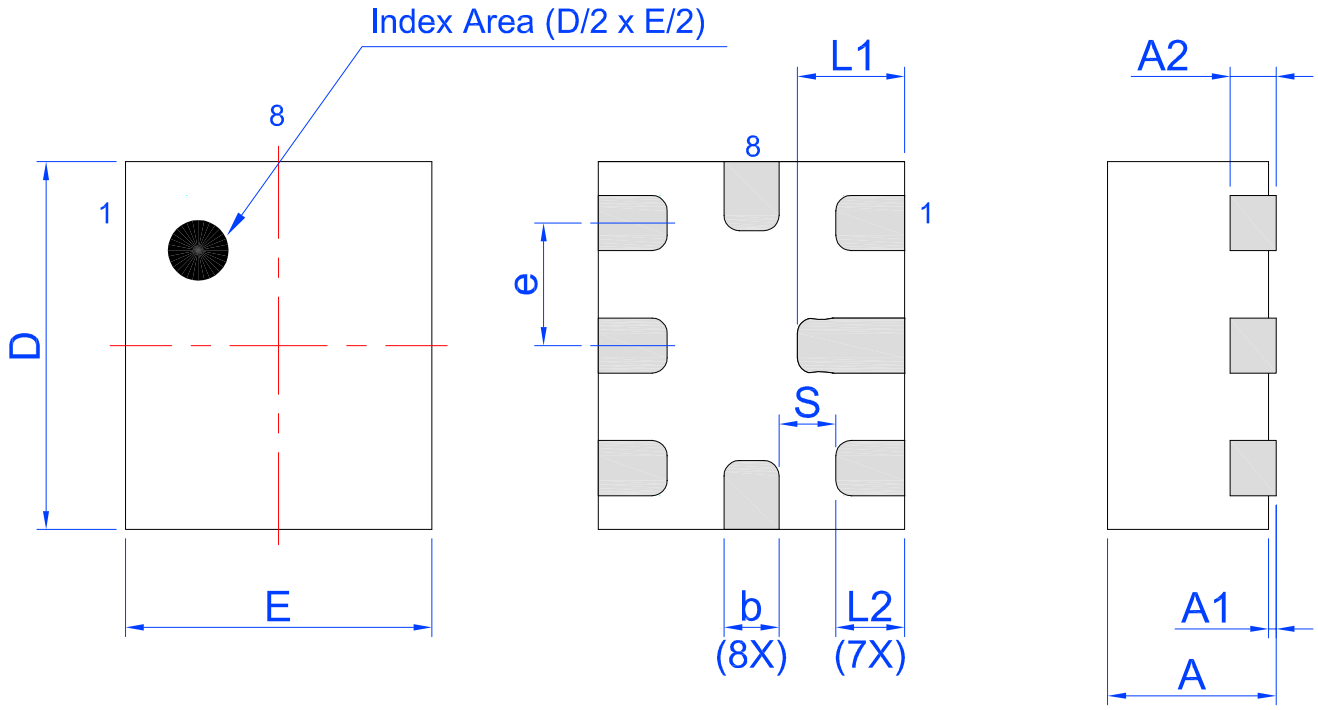
* PP may consist of the special characters +, -, and = for a total of 9 different combinations, or may consist of two character alphanumeric Part Code (A-Z and 0-9), depending on time of marking.

Note: The SN Code (Line 1 and Line 2) is generated during production, and encodes information including part number, programming code number, date code, and lot code. This same information is provided in plain text form on a label placed on the reel. If you need assistance in decoding the SN Code, please contact Renesas Electronics Corporation.

15. Package Information

15.1 Package Outlines for STQFN-8L 1.0 mm x 1.2 mm 0.4P FC Green Package

IC Net Weight: 0.0017 g



TOP View **BTM View** **SIDE View**

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.15	1.20	1.25
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L1	0.30	0.35	0.40
b	0.13	0.18	0.23	L2	0.175	0.225	0.275
e	0.40 BSC			S	0.185 REF		

15.2 STQFN Handling

Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

15.3 Soldering Information

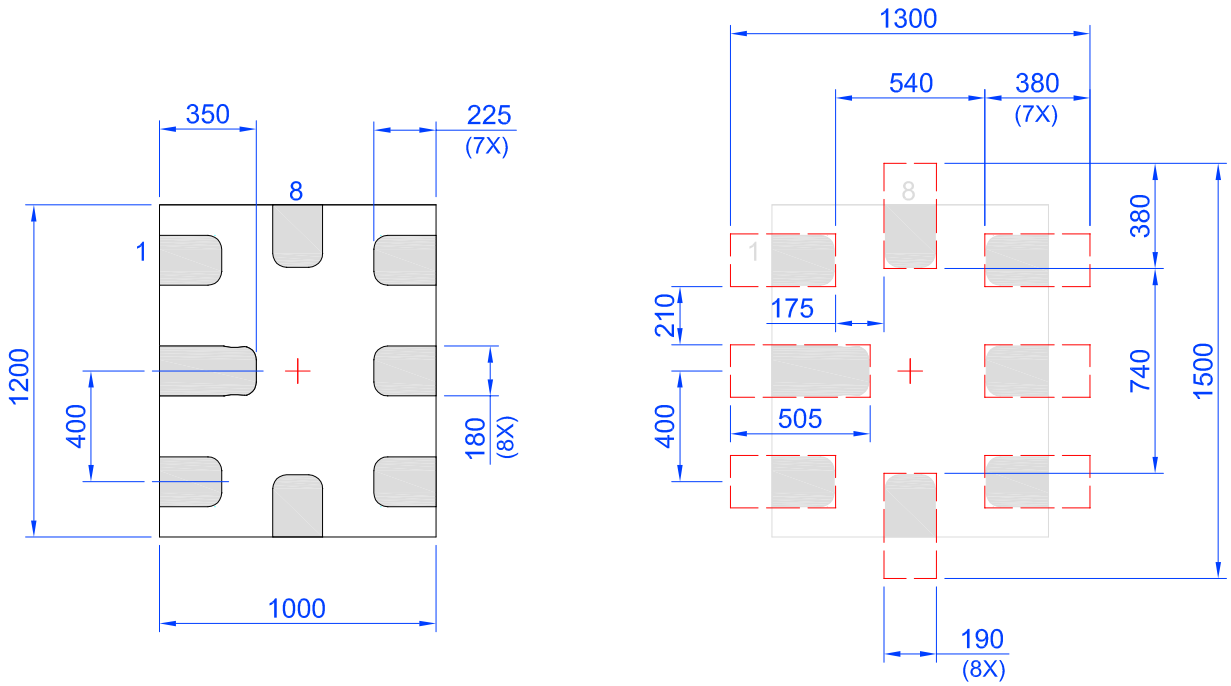
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.66 mm^3 (nominal). More information can be found at www.jedec.org.

16. Layout Guidelines

16.1 STQFN-8L 1.0 mm x 1.2 mm 0.4P FC Green Package

Exposed Pad
(PKG face down)

Recommended Landing Pattern
(PKG face down)



Unit: um

17. Ordering Information

Part Number	Type
SLG46108-EV	8-pin STQFN

Note: Use SLG46108-EV to order. Shipments are automatically in Tape and Reel.

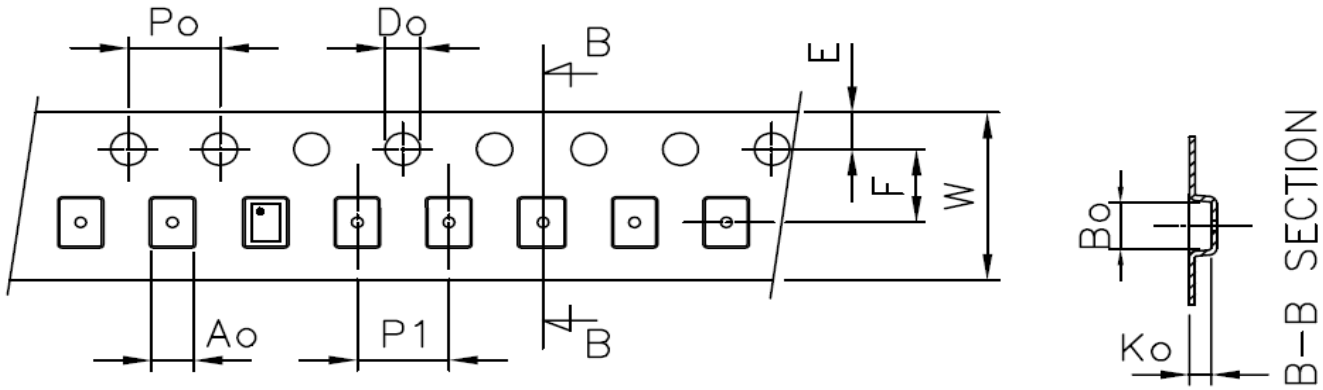
17.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel and Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 8L 1.0 mm x 1.2 mm 0.4P FC Green	8	1.0 x 1.2 x 0.55	3000	3000	178/60	100	400	100	400	8	4

17.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 8L 1.0 mm x 1.2 mm 0.4P FC Green	1.16	1.38	0.71	4	4	1.5	1.75	3.5	8

17.3 STQFN-8L



Glossary

C

CLK	Clock
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic Discharge

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LSB	Least Significant Bit
LUT	Look Up Table

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NMOS	N-Channel MOSFET
nRST	Reset
nSET	Set
NVM	Non-Volatile Memory

O

OD	Open-Drain

OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PMOS	P-Channel MOSFET
POR	Power-On Reset
PP	Push-Pull
PWR	Power
P DLY	Programmable Delay

Revision History

Revision	Date	Description
1.00	Aug 21, 2024	Initial version

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.