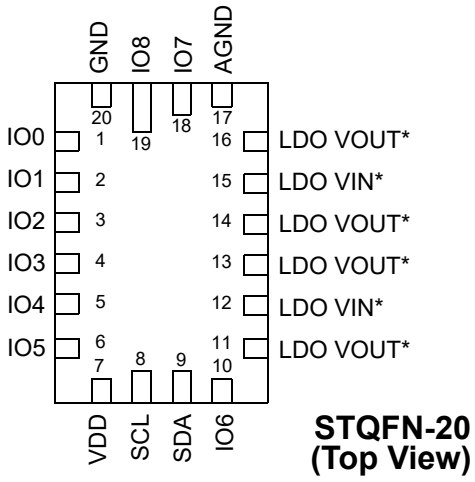
SLG46580/82/83

GreenPAK
Programmable Mixed-signal Matrix with Asynchronous State Machine and LDOs

Features

- Programmable Asynchronous State Machine
- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- Four 150 mA LDO Regulators (SLG46580)
- Two 300 mA LDO Regulators (SLG46582)
- One 600 mA LDO Regulators (SLG46583)
- I^2C Interface
- 2.5 V (±8%) to 5 V (±10%) Supply
- Operating Temperature Range: -40°C to 85°C
- RoHS Compliant / Halogen-Free
- 20-pin STQFN: 2 x 3 x 0.55 mm, 0.4 mm pitch

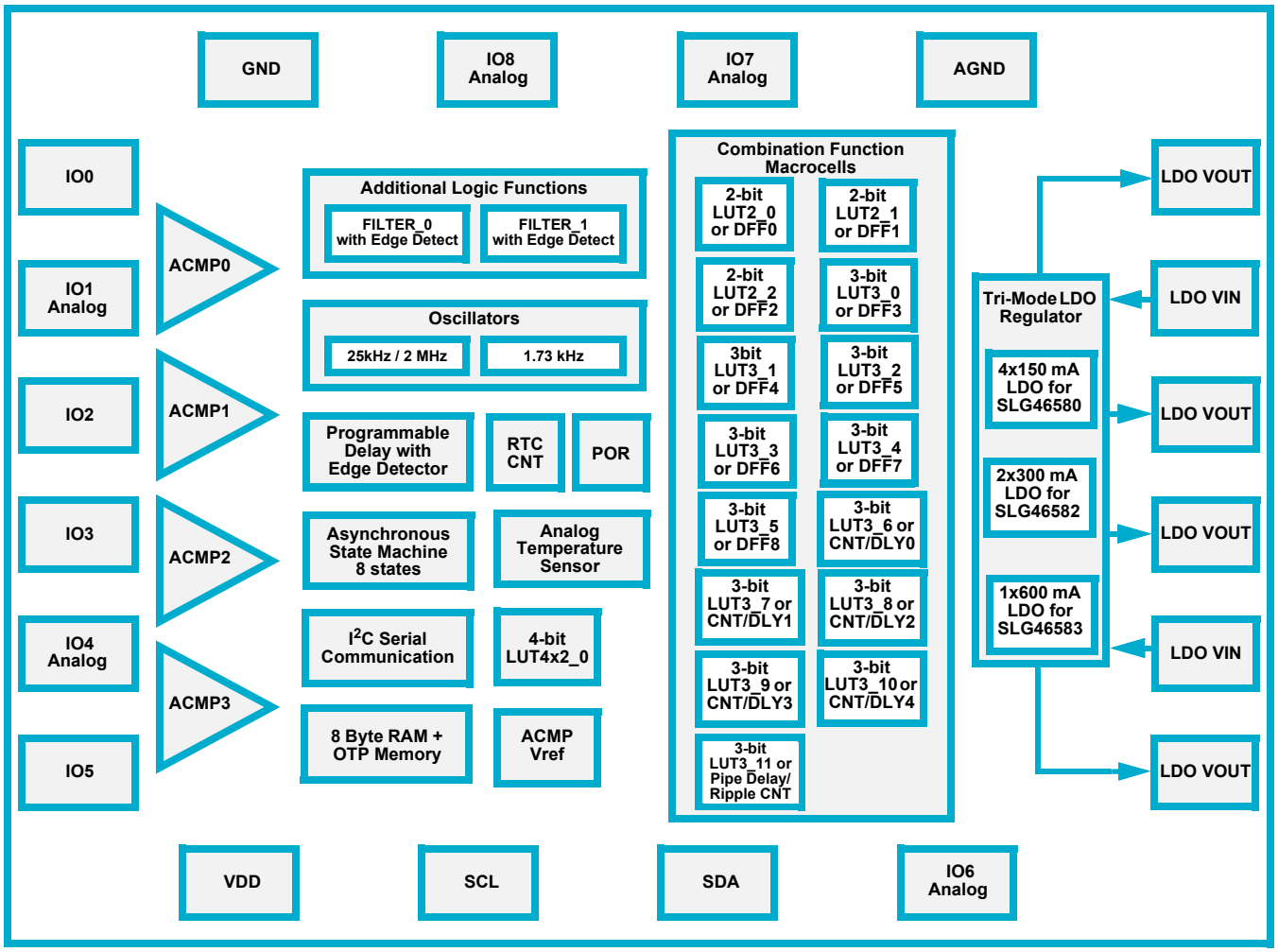
Pin Configuration



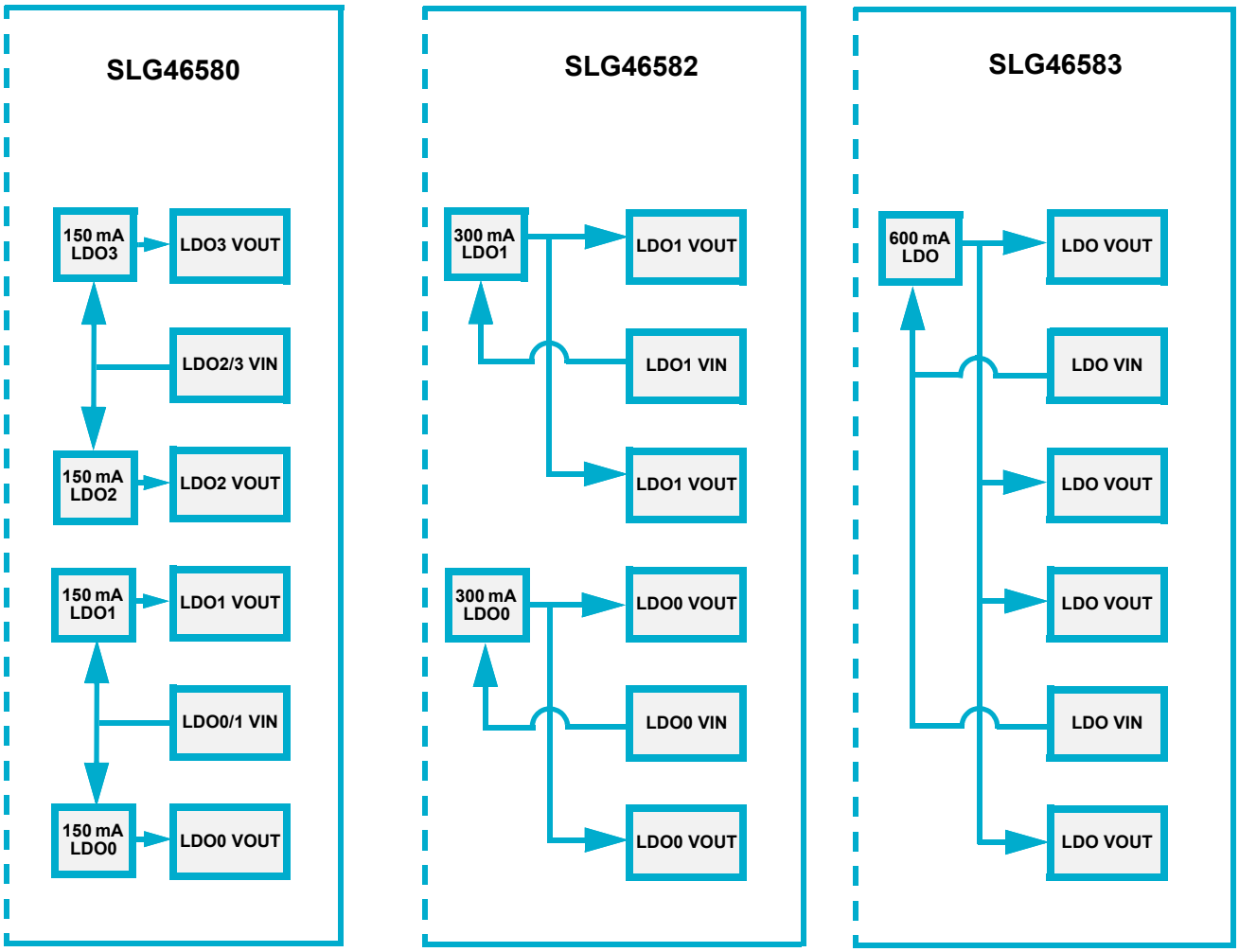
STQFN-20 (Top View)

Note: See LDO Connection Block Diagram*

Block Diagram



LDO Connection Block Diagram



Note 1: For SLG46582 both LDO0 VOUT (Pins 11 and 13) must be connected together externally, both LDO1 VOUT (Pins 14 and 16) must be connected together externally.

Note 2: For SLG46583 both LDO VIN (Pins 12 and 15) must be connected together externally. All four LDO VOUT (Pins 11, 13, 14 and 16) must be connected together externally.

1.0 Overview

The SLG46580/82/83 is a small, low power component commonly used to integrate mixed-signal functions under control of an asynchronous state machine. The user creates the circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46580/82/83. This highly versatile device allows a wide variety of functions and control logic to be designed within a very small, low power monolithic integrated circuit. The macrocells in the device include the following:

- Four Analog Comparators (ACMP)
- Voltage Reference (Vref) for ACMPs
- Analog Temperature Sensor
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/Latch or 2-bit LUTs
  - Six Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - Five 8-bit delays/counters or 3-bit LUTs
- Combinatorial Logic
  - One 4-bit LUT with two outputs
- Asynchronous State Machine
  - Eight States
  - Flexible input logic from state transitions
- Real Time Clock (RTC) Binary Counter
- Four Tri-Mode 150 mA LDO Regulators (for SLG46580):
  - High Power Mode (HP Mode): 150 mA output, see *Table 17.*
  - Low Power Mode (LP Mode): 100 µA output, see *Table 17.*
  - Power Switch Mode: Acts like a load switch
- Two Tri-Mode 300 mA LDO Regulators (for SLG46582):
  - High Power Mode (HP Mode): 300 mA output, see *Table 17.*
  - Low Power Mode (LP Mode): 200 µA output, see *Table 17.*
  - Power Switch Mode: Acts like a load switch
- One Tri-Mode 600 mA LDO Regulators (for SLG46583):
  - High Power Mode (HP Mode): 600 mA output, see *Table 17.*
  - Low Power Mode (LP Mode): 400 µA output, see *Table 17.*
  - Power Switch Mode: Acts like a load switch
- Serial Communications
  - I^2C Slave Protocol Interface
- Programmable Delay with Edge Detector Output
- Additional Logic Functions
  - 2 Deglitch Filters with Edge Detectors
- Two Oscillators (OSC)
  - Configurable 25 kHz/2 MHz
  - 1.73 kHz Low Power Oscillator
- Eight Byte RAM + OTP User Memory
  - RAM Memory space that is readable and writable via I^2C
  - User defined initial values transferred from OTP
- POR

2.0 Pin Description

2.1 Functional Pin Description for SLG46580

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	IO0	IO0	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
			EXT_CLK	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
2	IO1	IO1	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
3	IO2	IO2	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
4	IO3	IO3	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
5	IO4	IO4	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
6	IO5	IO5	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
7	VDD	VDD	Power Supply	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
		ACMP0-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1-	Analog Comparator 1 Negative Input	Analog	--
		ACMP2-	Analog Comparator 2 Negative Input	Analog	--
		ACMP3-	Analog Comparator 3 Negative Input	Analog	--
8	SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
		SCL	I^2C Serial Clock	Digital Input with Schmitt Trigger	--
		SCL	I^2C Serial Clock	Low Voltage Digital Input	--
9	SDA	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open Drain NMOS
		SDA	I^2C Serial Data	Digital Input with Schmitt Trigger	--
		SDA	I^2C Serial Data	Low Voltage Digital Input	--
10	IO6	IO6	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_VREF	All Analog Comparators Negative Input	Analog	--
11	LDO0 VOUT	LDO0 VOUT	LDO0 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
12	LDO0/1 VIN	LDO0/1 VIN	LDO0/LDO1 Input Voltage	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
13	LDO1 VOUT	LDO1 VOUT	LDO1 Output Voltage	--	--
14	LDO2 VOUT	LDO2 VOUT	LDO2 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
15	LDO2/3 VIN	LDO2/3 VIN	LDO2/LDO3 Input Voltage	--	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
16	LDO3 VOUT	LDO3 VOUT	LDO3 Output Voltage	--	--
17	AGND	AGND	Analog Ground for LDOs	--	--

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
18	IO7	IO7	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP2+	Analog Comparator 2 Positive Input	Analog	--
19	IO8	IO8	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
20	GND	GND	Ground	--	--

*Note *: General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*

2.2 Functional Pin Description for SLG46582

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	IO0	IO0	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
			EXT_CLK	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
2	IO1	IO1	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
3	IO2	IO2	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
4	IO3	IO3	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
5	IO4	IO4	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
6	IO5	IO5	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
7	VDD	VDD	Power Supply	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
		ACMP0-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1-	Analog Comparator 1 Negative Input	Analog	--
		ACMP2-	Analog Comparator 2 Negative Input	Analog	--
		ACMP3-	Analog Comparator 3 Negative Input	Analog	--
8	SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
		SCL	I^2C Serial Clock	Digital Input with Schmitt Trigger	--
		SCL	I^2C Serial Clock	Low Voltage Digital Input	--
9	SDA	SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	Open Drain NMOS
		SDA	I^2C Serial Data	Digital Input with Schmitt Trigger	--
		SDA	I^2C Serial Data	Low Voltage Digital Input	--
10	IO6	IO6	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_VREF	All Analog Comparators Negative Input	Analog	--
11**	LDO0 VOUT**	LDO0 VOUT	LDO0 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
12	LDO0 VIN	LDO0 VIN	LDO0 Input Voltage	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
13**	LDO0 VOUT**	LDO0 VOUT	LDO0 Output Voltage	--	--
14**	LDO1 VOUT**	LDO1 VOUT	LDO1 Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
15	LDO1 VIN	LDO1 VIN	LDO1 Input Voltage	--	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
16**	LDO1 VOUT**	LDO1 VOUT	LDO1 Output Voltage	--	--
17	AGND	AGND	Analog Ground for LDOs	--	--
18	IO7	IO7	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP2+	Analog Comparator 2 Positive Input	Analog	--
19	IO8	IO8	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
20	GND	GND	Ground	--	--

*Note 1: * General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*
*Note 2: ** All LDO0 VOUT pins should be connected together externally, and all LDO1 VOUT pins should also be connected together externally for reliable operation.*

2.3 Functional Pin Description or SLG46583

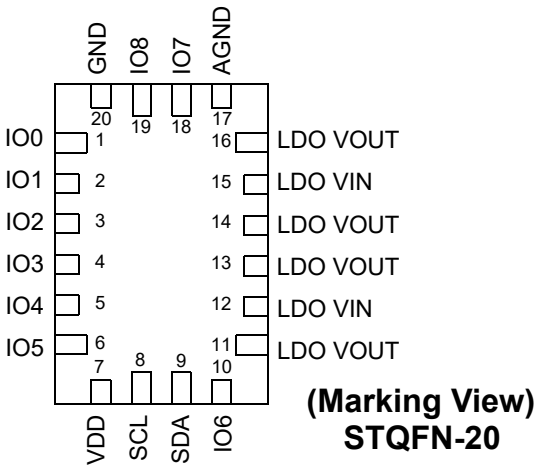
STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	IO0	IO0	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
			EXT_CLK	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
2	IO1	IO1	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
3	IO2	IO2	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
4	IO3	IO3	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
5	IO4	IO4	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
6	IO5	IO5	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
7	VDD	VDD	Power Supply	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
		ACMP0-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1-	Analog Comparator 1 Negative Input	Analog	--
		ACMP2-	Analog Comparator 2 Negative Input	Analog	--
		ACMP3-	Analog Comparator 3 Negative Input	Analog	--
8	SCL	SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
		SCL	I^2C Serial Clock	Digital Input with Schmitt Trigger	--
		SCL	I^2C Serial Clock	Low Voltage Digital Input	--

STQFN 20L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
9	SDA	SDA	I²C Serial Data	Digital Input without Schmitt Trigger	Open Drain NMOS
		SDA	I²C Serial Data	Digital Input with Schmitt Trigger	--
		SDA	I²C Serial Data	Low Voltage Digital Input	--
10	IO6	IO6	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		EXT_VREF	All Analog Comparators Negative Input	Analog	--
11***	LDO VOUT***	LDO VOUT	LDO Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
12**	LDO VIN**	LDO VIN	LDO Input Voltage	--	--
		ACMP0+	Analog Comparator 0 Positive Input	Analog	--
13***	LDO VOUT***	LDO VOUT	LDO Output Voltage	--	--
14***	LDO VOUT***	LDO VOUT	LDO Output Voltage	--	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
15**	LDO VIN **	LDO VIN	LDO Input Voltage	--	--
		ACMP1+	Analog Comparator 1 Positive Input	Analog	--
16***	LDO VOUT***	LDO VOUT	LDO Output Voltage	--	--
17	AGND	AGND	Analog Ground for LDOs	--	--
18	IO7	IO7	General Purpose I/O	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	Open Drain PMOS (1x) (2x)
		ACMP2+	Analog Comparator 2 Positive Input	Analog	--
19	IO8	IO8	General Purpose I/O with OE*	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3+	Analog Comparator 3 Positive Input	Analog	--
20	GND	GND	Ground	--	--

*Note 1: * General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*
*Note 2: ** All LDO VIN pins should be connected together externally for reliable operation.*
*Note 3: *** All LDO VOUT pins should be connected together externally for reliable operation.*

2.4 Pin Configuration - STQFN20L



(Marking View)
STQFN-20

Pin #	Signal Name	Pin Functions
1	IO0	GPIO with OE* / EXT_CLK
2	IO1	GPIO / ACMP0+
3	IO2	GPIO
4	IO3	GPIO
5	IO4	GPIO with OE*/ ACMP1+
6	IO5	GPI
7	VDD	Power Supply
8	SCL	SCL
9	SDA	SDA
10	IO6	GPIO with OE* / EXT_VREF
11**	LDO0 VOUT (SLG46580)	LDO0 Output Voltage
	LDO0 VOUT (SLG46582)	LDO0 Output Voltage
	LDO VOUT (SLG46583)	LDO Output Voltage
12**	LDO0/1 VIN (SLG46580)	LDO0/LDO1 Input Voltage
	LDO0 VIN (SLG46582)	LDO0 Input Voltage
	LDO VIN (SLG46583)	LDO Input Voltage
13**	LDO1 VOUT (SLG46580)	LDO1 Output Voltage
	LDO0 VOUT (SLG46582)	LDO0 Output Voltage
	LDO VOUT (SLG46583)	LDO Output Voltage
14**	LDO2 VOUT (SLG46580)	LDO2 Output Voltage
	LDO1 VOUT (SLG46582)	LDO1 Output Voltage
	LDO VOUT (SLG46583)	LDO Output Voltage
15**	LDO2/3 VIN (SLG46580)	LDO2/LDO3 Input Voltage
	LDO1 VIN (SLG46582)	LDO1 Input Voltage
	LDO VIN (SLG46583)	LDO Input Voltage
16**	LDO3 VOUT (SLG46580)	LDO3 Output Voltage
	LDO1 VOUT (SLG46582)	LDO1 Output Voltage
	LDO VOUT (SLG46583)	LDO Output Voltage
17	AGND	Analog Ground for LDOs
18	IO7	GPIO / ACMP2+
19	IO8	GPIO with OE*/ ACMP3+
20	GND	Ground

Note: General Purpose I/O's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in I/O structure.*
*Note**: For SLG46582 both LDO0 VOUT (Pins 11 and 13) must be connected together externally, both LDO1 VOUT (Pins 14 and 16) must be connected together externally. For SLG46583 both LDO VIN (Pins 12 and 15) must be connected together externally. All four LDO VOUT (Pins 11, 13, 14 and 16) must be connected together externally.*

3.0 User Programmability

The SLG46580/82/83 is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

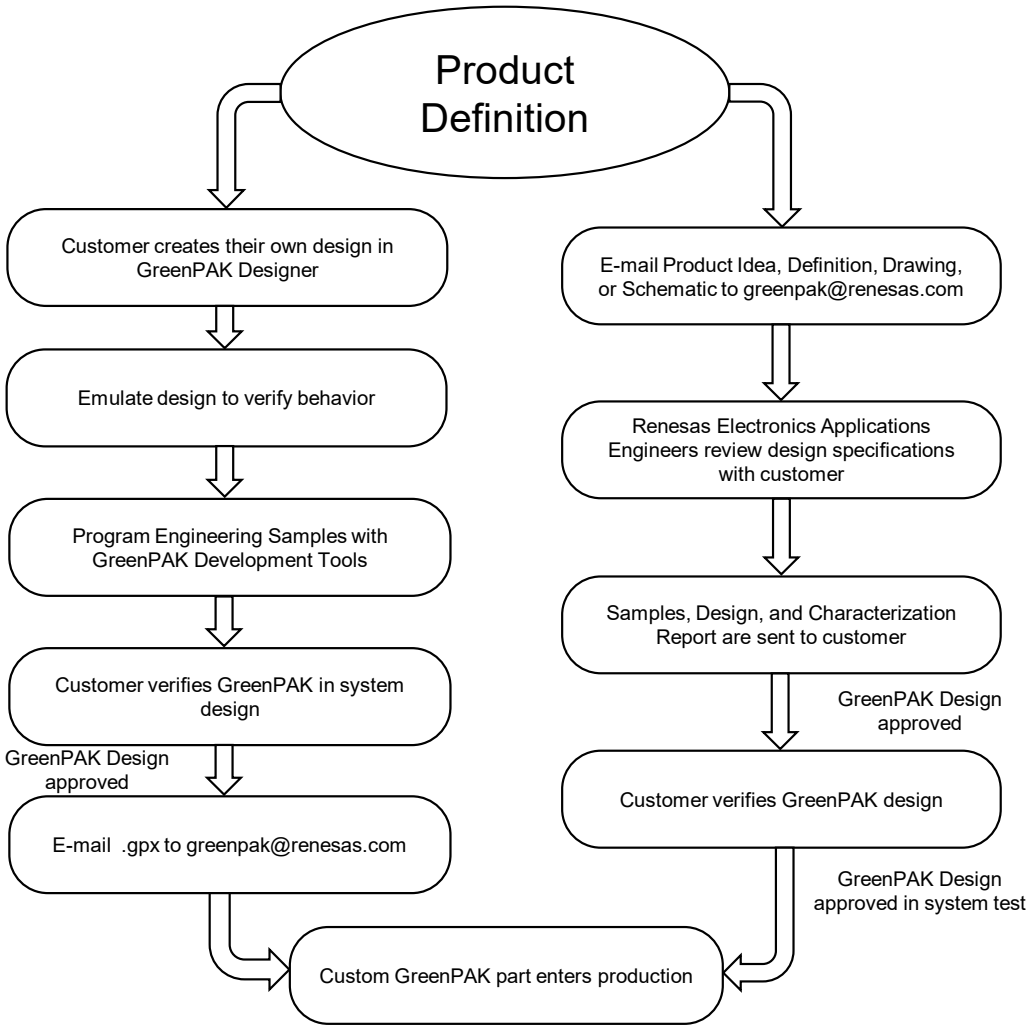


Figure 1. Steps to create a custom GreenPAK device

4.0 Ordering Information

Part Number	Type	Status*
SLG46580V	20-pin STQFN	ACTIVE
SLG46580VTR	20-pin STQFN - Tape and Reel (3k units)	ACTIVE
SLG46582V	20-pin STQFN	ACTIVE
SLG46582VTR	20-pin STQFN - Tape and Reel (3k units)	ACTIVE
SLG46583V	20-pin STQFN	ACTIVE
SLG46583VTR	20-pin STQFN - Tape and Reel (3k units)	ACTIVE

Note 1: Use SLG46580V or SLG46582V, or SLG46583V to order. Shipments are automatically in Tape and Reel.

Note 2: "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

Note: The marketing status values are defined as follows:*

***ACTIVE**: Product device recommended for new designs.*

***LIFEBUY**: Renesas Electronics Corporation has announced that the device will be discontinued, and a lifetime-buy period is in effect.*

***NRND**: Not recommended for new designs. Device is in production to support existing customers, but Renesas Electronics Corporation does not recommend using this part in a new design.*

***PREVIEW**: Device has been announced but is not in production. Samples may or may not be available.*

***OBSOLETE**: Renesas Electronics Corporation has discontinued the production of the device.*

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	VDD + 0.5 V	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	31	mA
	Push-Pull 2x	--	43	
	OD 1x	--	41	
	OD 2x	--	65	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage (see Note 1)		2.3	3.3	5.5	V
V_{PP}	Programming Voltage		7.25	7.50	7.75	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at V_{DD}		--	0.1	--	µF
V_{AIR}	Analog Input Common Mode Range	Negative ACMP Input	0	--	1.2	V
V_{AIH}	Analog Input Voltage HIGH-Level	Allowable Input Voltage at Analog Pins	0	--	V_{DD}	V
V_{IH}	HIGH-Level Input Voltage	Logic Input (see Note 2)	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input (see Note 2)	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input (see Note 2)	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input (see Note 2)	GND- 0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.5 V +/- 8%	0.4	0.6	0.8	V
		V_{DD} = 3.3 V +/- 10%	0.5	0.7	0.9	V
		V_{DD} = 5 V +/- 10%	0.7	1.0	1.2	V
V_O	Maximal Voltage Applied to any PIN in High Impedance State		--	--	V_{DD}+ 0.3	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1X Drive, V_{DD} = 2.5 V +/- 8%, I_{OH} = 100 µA	2.29	2.49	--	V
		Push-Pull, 1X Drive, V_{DD} = 3.3 V +/- 10%, I_{OH} = 3 mA	2.73	3.12	--	V
		Push-Pull, 1X Drive, V_{DD} = 5 V +/- 10%, I_{OH} = 5 mA	4.19	4.78	--	V
		Push-Pull, 2X Drive, V_{DD} = 2.5 V +/- 8%, I_{OH} = 100 µA	2.29	2.50	--	V
		Push-Pull, 2X Drive, V_{DD} = 3.3 V +/- 10%, I_{OH} = 3 mA	2.87	3.21	--	V
		Push-Pull, 2X Drive, V_{DD} = 5 V +/- 10%, I_{OH} = 5 mA	4.32	4.89	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1X Drive, V_{DD} = 2.5 V +/- 8%, I_{OL}= 100 µA	--	0.06	0.13	V
		Push-Pull, 1X Drive, V_{DD} = 3.3 V +/- 10%, I_{OL} = 3 mA	--	0.13	0.23	V
		Push-Pull, 1X Drive, V_{DD} = 5 V +/- 10%, I_{OL}= 5 mA	--	0.16	0.27	V
		Push-Pull, 2X Drive, V_{DD} = 2.5 V +/- 8%, I_{OL} = 100 µA	--	0.03	0.06	V
		Push-Pull, 2X Drive, V_{DD} = 3.3 V +/- 10%, I_{OL}= 3 mA	--	0.06	0.11	V
		Push-Pull, 2X Drive, V_{DD} = 5 V +/- 10%, I_{OL} = 5 mA	--	0.08	0.14	V
		NMOS OD, 1X Drive, V_{DD} = 2.5 V +/- 8%, I_{OL} = 100 µA	--	0.03	0.06	V
		NMOS OD, 1X Drive, V_{DD} = 3.3 V +/- 10%, I_{OL} = 3 mA	--	0.08	0.15	V
		NMOS OD, 1X Drive, V_{DD} = 5 V +/- 10%, I_{OL} = 5 mA	--	0.10	0.18	V
		NMOS OD, 2X Drive, V_{DD} = 2.5 V +/- 8%, I_{OL} = 100 µA	--	0.02	0.03	V
		NMOS OD, 2X Drive, V_{DD} = 3.3 V +/- 10%, I_{OL} = 3 mA	--	0.04	0.08	V
		NMOS OD, 2X Drive, V_{DD} = 5 V +/- 10%, I_{OL} = 5 mA	--	0.05	0.11	V
I_{OH}	HIGH-Level Output Current	Push-Pull, 1X Drive, V_{DD} = 2.5 V +/- 8%, V_{OH} = V_{DD} - 0.2	1.07	1.70	--	mA
		Push-Pull, 1X Drive, V_{DD} = 3.3 V +/- 10%, V_{OH} = 2.4 V	6.05	12.08	--	mA
		Push-Pull, 1X Drive, V_{DD} = 5 V +/- 10%, V_{OH} = 2.4 V	22.08	34.04	--	mA
		Push-Pull, 2X Drive, V_{DD} = 2.5 V +/- 8%, V_{OH} = V_{DD} - 0.2	2.22	3.41	--	mA
		Push-Pull, 2X Drive, V_{DD} = 3.3 V +/- 10%, V_{OH} = 2.4 V	11.54	24.16	--	mA
		Push-Pull, 2X Drive, V_{DD} = 5 V +/- 10%, V_{OH} = 2.4 V	41.46	68.08	--	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OL}	LOW-Level Output Current	Push-Pull, 1X Drive, V_{DD} = 2.5 V +/- 8%, V_{OL} = 0.15 V	0.92	1.69	--	mA
		Push-Pull, 1X Drive, V_{DD} = 3.3 V +/- 10%, V_{OL} = 0.4 V	4.87	8.24	--	mA
		Push-Pull, 1X Drive, V_{DD} = 5 V +/- 10%, V_{OL} = 0.4 V	7.21	11.58	--	mA
		Push-Pull, 2X Drive, V_{DD} = 2.5 V +/- 8%, V_{OL} = 0.15 V	1.83	3.38	--	mA
		Push-Pull, 2X Drive, V_{DD} = 3.3 V +/- 10%, V_{OL} = 0.4 V	9.75	16.49	--	mA
		Push-Pull, 2X Drive, V_{DD} = 5 V +/- 10%, V_{OL} = 0.4 V	13.83	23.16	--	mA
		NMOS OD, 1X Drive, V_{DD} = 2.5 V +/- 8%, V_{OL} = 0.15 V	1.37	2.53	--	mA
		NMOS OD, 1X Drive, V_{DD} = 3.3 V +/- 10%, V_{OL} = 0.4 V	7.31	12.37	--	mA
		NMOS OD, 1X Drive, V_{DD} = 5 V +/- 10%, V_{OL} = 0.4 V	10.82	17.38	--	mA
		NMOS OD, 2X Drive, V_{DD} = 2.5 V +/- 8%, V_{OL} = 0.15 V	2.75	5.07	--	mA
		NMOS OD, 2X Drive, V_{DD} = 3.3 V +/- 10%, V_{OL} = 0.4 V	14.54	24.74	--	mA
		NMOS OD, 2X Drive, V_{DD} = 5 V +/- 10%, V_{OL} = 0.4 V	17.34	34.76	--	mA
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 3)	T_J = 85°C	--	--	73	mA
		T_J = 110°C	--	--	35	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 3)	T_J = 85°C	--	--	152	mA
		T_J = 110°C	--	--	72	mA
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	1.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.34	1.55	1.74	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.05	1.25	1.45	V
R_{PUP}	Pull Up Resistance	1 M Pull Up	--	1	--	MΩ
		100 k Pull Up	--	100	--	kΩ
		10 k Pull Up	--	10	--	kΩ
R_{PDWN}	Pull Down Resistance	1 M Pull Down	--	1	--	MΩ
		100 k Pull Down	--	100	--	kΩ
		10 k Pull Down	--	10	--	kΩ
C_{IN}	Input Capacitance		--	4	--	pF
T_{PW_RTC}	RTC Clock Pulse Width	Minimum Pulse Width for the RTC's Clock Input	1	--	--	µs

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: No hysteresis.
Note 3: The GreenPAK's power rails are divided in two sides. IOs 0, 1, 2, 3, 4 and 5 are connected to one side, IOs 6, 7, 8, SCL and SDA to another.

5.3 I²C Specifications

Table 1. EC of the I²C Pins at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Fast-Mode		Fast-Mode Plus		Unit
			Min.	Max.	Min.	Max.	
V_{IL}	LOW-level Input Voltage		-0.5	$0.3V_{DD}$	-0.5	$0.3\ V_{DD}$	V
V_{IH}	HIGH-level Input Voltage		$0.7V_{DD}$	5.5	$0.7V_{DD}$	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		$0.05V_{DD}$	--	$0.05V_{DD}$	--	V
V_{OL1}	LOW-Level Output Voltage 1	(open drain or open collector) at 3mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(open drain or open collector) at 2 mA sink current $V_{DD} \le 2$ V	0	$0.2V_{DD}$	0	$0.2V_{DD}$	V
I_{OL}	LOW-Level Output Current (see Note 1)	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	12.6	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	16.1	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	17.6	--	mA
		V_{OL}= 0.6 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} (see Note 1)		14x (VDD/5.5V)	250	10x (VDD/5.5V)	120	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns
I_i	Input Current each IO Pin	$0.1V_{DD} < V_I < 0.9V_{DDmax}$	-10	+10	-10	+10	µs
C_i	Capacitance for each IO Pin		--	10	--	10	pF

Note 1: Does not meet standard I²C specifications: t_{of} = 20x(VDD/5.5V) (min); For Fast-mode Plus I_{OL}= 20 mA (min) at V_{OL} = 0.4 V.
Note 2: For Fast-mode Plus SDA pin must be configured as 2x NMOS open drain, see table *Table 30. SCL Register Settings*.

Table 2. I²C Pins Timing Characteristics at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Fast-Mode		Fast-Mode Plus		Unit
			Min.	Max.	Min.	Max.	
F_{SCL}	Clock Frequency, SCL		--	400	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	500	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	260	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)	V_{DD} = 2.5 V ± 8%	--	95	--	168	ns
		V_{DD} = 3.3 V ± 10%	--	95	--	157	
		V_{DD} = 5.0 V ± 10%	--	111	--	156	
t_{AA}	Clock Low to Data Out Valid		--	900	--	450	ns

Table 2. I^2C Pins Timing Characteristics at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Condition/Note	Fast-Mode		Fast-Mode Plus		Unit
			Min.	Max.	Min.	Max.	
t_{BUF}	Bus Free Time between Stop and Start		1300	--	500	--	ns
t_{HD_STA}	Start Hold Time		600	--	260	--	ns
t_{SU_STA}	Start Set-up Time		600	--	260	--	ns
t_{HD_DAT}	Data Hold Time		0	--	0	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	50	--	ns
t_R	Inputs Rise Time		--	300	--	120	ns
t_F	Inputs Fall Time		--	300	--	120	ns
t_{SU_STD}	Stop Set-up Time		600	--	260	--	ns
t_{DH}	Data Out Hold Time		50	--	50	--	ns
Note: Timing diagram can be found in the Figure 87. .							

5.4 Asynchronous State Machine (ASM) Specifications at T = 25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
$t_{st\_out\_delay}$	Asynchronous State Machine Output Delay Time	V_{DD} = 2.5 V ± 8%	82	--	108	ns
		V_{DD} = 3.3 V ± 10%	57	--	74	
		V_{DD} = 5.0 V ± 10%	40	--	49	
t_{st_out}	Asynchronous State Machine Output Transition Time	V_{DD} = 2.5 V ± 8%	--	--	89	ns
		V_{DD} = 3.3 V ± 10%	--	--	61	
		V_{DD} = 5.0 V ± 10%	--	--	39	
t_{st_pulse}	Asynchronous State Machine Input Pulse Acceptance Time	V_{DD} = 2.5 V ± 8%	12	--	--	ns
		V_{DD} = 3.3 V ± 10%	9	--	--	
		V_{DD} = 5.0 V ± 10%	6	--	--	
t_{st_comp}	Asynchronous State Machine Input Compete Time	V_{DD} = 2.5 V ± 8%	--	--	13	ns
		V_{DD} = 3.3 V ± 10%	--	--	9	
		V_{DD} = 5.0 V ± 10%	--	--	6	

5.5 IDD Estimator

Table 3. Typical Current Estimated for Each Macrocell at T = -40 °C to +85 °C.

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent (POR, BG auto power on)	0.06	0.08	0.13	µA
		BG Force On	12.85	14.07	17.15	µA
		LP OSC (1.73 kHz)	0.28	0.35	0.61	µA
		Configurable OSC (25 kHz), predivide = 1	5.12	5.32	6.14	µA
		Configurable OSC (25 kHz), predivide = 8	4.98	5.13	5.83	µA
		Configurable OSC (2 MHz), predivide = 1	34.66	42.18	61.05	µA
		Configurable OSC (2 MHz), predivide = 8	22.23	25.26	34.01	µA
		Real Time Clock (RTC), RTC Clocked by Counter Divider Clock (see Note)	0.18	0.24	0.40	µA
		1st ACMP used with LB enabled	53.22	46.60	56.37	µA
		1st ACMP used (includes Vref)	56.50	49.89	59.65	µA
		Each additional ACMP add	3.35	3.35	3.35	µA
		ACMP0 or ACMP1 used with Input Buffer	66.93	60.47	70.59	µA
		ACMP1 used with 100 µA enabled	71.99	65.37	75.13	µA
		ACMP2 used with Temp Sensor	62.94	56.38	66.26	µA
		1x push-pull + 4 pF @ 2 MHz	40	47	106	µA
		1x push-pull + 4 pF @ 25 kHz	4.5	5	16	µA

Note: The RTC current measurements were taken with an external 32.768 kHz clock with the GPIO current consumption extracted. VDD = 2.5 V average taken from 2.3 V to 2.7 V, VDD = 3.3 V average taken from 3.0 V to 3.6 V, VDD = 5.0 V average taken from 4.5 V to 5.5 V.

5.6 Macrocells Timing

Table 4. Typical Delay Estimated for Each Macrocell at T=25°C.

Symbol	Parameter	Note	V_{DD} = 2.5 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital Input to PP 1X	26	28	19	20	14	14	ns
tpd	Delay	Digital Input to PP 2X	25	27	18	19	13	14	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	25	27	18	20	13	14	ns
tpd	Delay	Low Voltage Digital Input to PP 1X	33	307	25	207	19	131	ns
tpd	Delay	Digital input to NMOS 1x	--	46	--	31	--	20	ns
tpd	Delay	Digital input to NMOS 2x	--	42	--	28	--	18	ns
tpd	Delay	Digital input to PMOS 1x	26	--	19	--	14	--	ns
tpd	Delay	Digital input to PMOS 2x	25	--	18	--	13	--	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	28	--	20	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	--	27	--	20	--	14	ns
tpd	Delay	1x3 State Hi-Z to 1	28	--	20	--	15	--	ns
tpd	Delay	1x3 State Hi-Z to 0	--	27	--	20	--	14	ns
tpd	Delay	2x3 State Hi-Z to 1	27	--	20	--	14	--	ns
tpd	Delay	2x3 State Hi-Z to 0	--	26	--	19	--	14	ns
tpd	Delay	CNT/DLY Counter Mode	54	54	38	38	27	27	ns
tpd	Delay	CNT/DLY Freq. Detect	39	39	28	28	20	20	ns
tpd	Delay	CNT/DLY One Shot	38	38	27	27	19	19	ns
tpd	Delay	CNT/DLY Delay Mode	36	38	26	27	18	19	ns
tpd	Delay	CNT/DLY Edge Detect	36	36	26	25	18	18	ns
tpd	Delay	CNT/DLY High Level Reset	40	--	28	--	20	--	ns
tpd	Delay	Latch Q	19	20	14	14	10	9	ns
tpd	Delay	Latch nQ	20	20	14	14	10	10	ns
tpd	Delay	Latch nRESET Q	20	21	15	15	11	10	ns
tpd	Delay	Latch nRESET nQ	21	21	15	15	11	11	ns
tpd	Delay	Latch nSET Q	21	22	15	15	10	11	ns
tpd	Delay	Latch nSET nQ	22	22	16	15	11	10	ns
tpd	Delay	LUT2bit	17	17	13	12	9	8	ns
tpd	Delay	LUT3bit	20	20	14	14	10	9	ns
tpd	Delay	LUT4bit	18	18	13	12	9	8	ns
tpd	Delay	EDGE DETECT	27	27	19	19	13	13	ns
tpd	Delay	EDGE DETECT Delayed	214	212	158	156	117	115	ns
tpd	Width	EDGE DETECT	182	182	136	136	101	101	ns
tpd	Delay	Ripple CLK DOWN CNT Q0	21	20	15	14	11	10	ns
tpd	Delay	Ripple CLK DOWN CNT Q1	29	25	21	18	15	13	ns
tpd	Delay	Ripple CLK DOWN CNT Q2	29	31	21	22	15	16	ns
tpd	Delay	Ripple CLK UP CNT Q0	21	20	15	15	11	10	ns
tpd	Delay	Ripple CLK UP CNT Q1	26	26	19	19	13	13	ns
tpd	Delay	Ripple CLK UP CNT Q2	31	26	23	19	16	14	ns
tpd	Delay	Ripple nRESET DOWN CNT Q0	25	48	18	34	13	25	ns
tpd	Delay	Ripple nRESET DOWN CNT Q1	24	54	17	39	12	28	ns

Table 4. Typical Delay Estimated for Each Macrocell at T=25°C.

Symbol	Parameter	Note	V_{DD} = 2.5 V		V_{DD} = 3.3V		V_{DD} = 5.0V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Ripple nRESET DOWN CNT Q2	24	54	17	39	13	28	ns
tpd	Delay	Ripple nRESET UP CNT Q0	25	48	18	34	13	25	ns
tpd	Delay	Ripple nRESET UP CNT Q1	24	52	17	38	12	27	ns
tpd	Delay	Ripple nRESET UP CNT Q2	25	57	18	41	13	30	ns
tpd	Delay	DFF Q	19	20	13	14	10	10	ns
tpd	Delay	DFF nQ	20	19	14	14	10	10	ns
tpd	Delay	DFF nRESET Q	--	21	--	15	--	10	ns
tpd	Delay	DFF nRESET nQ	21	--	15	--	11	--	ns
tpd	Delay	DFF nSET Q	21	--	15	--	11	--	ns
tpd	Delay	DFF nSET nQ	--	22	--	15	--	10	ns
tpd	Delay	Pipe Delay Out	24	23	17	17	13	12	ns
tpd	Delay	Pipe Delay nRESET Out	25	26	18	19	13	13	ns
tpd	Delay	Filter	111	112	77	77	50	50	ns
tpd	Delay	ACMP (100 mV overdrive, low bandwidth disabled, input gain = 1, IN- = 600 mV)	0.49	0.45	0.42	0.38	0.40	0.36	µs
tpd	Delay	ACMP (10 mV overdrive, low bandwidth disabled, input gain = 1, IN- = 600 mV)	1.26	1.16	1.17	1.08	1.14	1.06	µs
tpd	Delay	ACMP (100 mV overdrive, low bandwidth enabled, input gain = 1, IN- = 600 mV)	3.89	3.55	3.82	3.48	3.78	3.44	µs
tpd	Delay	ACMP (10 mV overdrive, low bandwidth enabled, input gain = 1, IN- = 600 mV)	10.04	10.82	9.88	10.76	9.77	10.68	µs
tw	Width	filter (min transmitted)	79	78	55	55	35	35	ns

Table 5. Typical Propagations Delays and Pulse Widths at T = 25°C.

Symbol	Parameter	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode:(any)edge detect, edge detect output	185	137	101	ns
tw	Pulse Width, 2 cell	mode:(any)edge detect, edge detect output	373	277	205	ns
tw	Pulse Width, 3 cell	mode:(any)edge detect, edge detect output	561	417	308	ns
tw	Pulse Width, 4 cell	mode:(any)edge detect, edge detect output	748	556	411	ns
time1	Delay, 1 cell	mode:(any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 2 cell	mode:(any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 3 cell	mode:(any)edge detect, edge detect output	28	20	15	ns
time1	Delay, 4 cell	mode:(any)edge detect, edge detect output	28	20	15	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	218	161	119	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	405	300	222	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	593	440	325	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	780	579	427	ns

Table 6. Typical Pulse Width that will be Filtered out by Filter Macrocell (at T=25°C).

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
Filtered Pulse Width	< 75	< 55	< 35	ns

5.7 Counter/Delay Specifications

Table 7. Typical Counter/Delay Offset at T = 25°C.

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3V	V_{DD} = 5.0V	Unit
offset	25kHz	auto	16	2.5	2.5	µs
offset	2MHz	auto	1	0.6	0.4	µs
offset	1.73 kHz	auto	247	232	198	µs
frequency settling time	25kHz	auto	16	14	12	µs
frequency settling time	2MHz	auto	14	14	14	µs
frequency settling time	1.73 kHz	auto	250	200	150	µs
variable (CLK period)	25kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	1.73 kHz	forced	0-0.5	0-0.5	0-0.5	ms
tpd (non-delayed edge)	25kHz/2MHz	either	25	14	10	ns

5.8 OSC Specifications

Table 8. 25 kHz RC OSC0 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
2.5 V ±5%	24.705	25.342	23.724	25.932	23.357	26.888
3.3 V ±10%	24.710	25.289	23.690	25.932	23.334	26.836
5 V ±10%	24.650	25.801	23.661	26.249	23.376	26.987
2.5 V ... 4.5 V	24.650	25.334	23.659	25.932	23.334	26.879
2.3 V… 5.5 V	24.650	25.801	23.659	26.249	23.334	26.987

Table 9. 25 kHz RC OSC0 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±5%	-1.18%	1.37%	-5.10%	3.73%	-6.57%	7.55%
3.3 V ±10%	-1.16%	1.16%	-5.24%	3.73%	-6.66%	7.34%
5 V ±10%	-1.40%	3.20%	-5.36%	5.00%	-6.50%	7.95%
2.5 V ... 4.5 V	-1.40%	1.34%	-5.36%	3.73%	-6.66%	7.52%
2.3 V… 5.5 V	-1.40%	3.20%	-5.36%	5.00%	-6.66%	7.95%

5.8.1 2 MHz RC Oscillator

Table 10. 2 MHz RC OSC0 frequency limits

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
2.5 V ±5%	1.916	2.082	1.859	2.128	1.859	2.128
3.3 V ±10%	1.967	2.032	1.908	2.082	1.828	2.125
5 V ±10%	1.947	2.262	1.897	2.268	1.820	2.268
2.5 V ... 4.5 V	1.935	2.066	1.873	2.117	1.814	2.125
2.3 V… 5.5 V	1.916	2.262	1.859	2.268	1.814	2.268

Table 11. 2 MHz RC OSC0 frequency error (error calculated relative to nominal value)

Power Supply Range (VDD) V	Temperature Range					
	+25 °C		0 °C ... +85 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±5%	-4.22%	4.09%	-7.06%	6.40%	-7.06%	6.40%
3.3 V ±10%	-1.64%	1.60%	-4.62%	4.10%	-8.62%	6.24%
5 V ±10%	-2.67%	13.09%	-5.14%	13.39%	-9.01%	13.39%
2.5 V ... 4.5 V	-3.26%	3.31%	-6.37%	5.84%	-9.31%	6.24%
2.3 V… 5.5 V	-4.22%	13.09%	-7.06%	13.39%	-9.31%	13.39%

5.8.2 1.73 kHz RC Oscillator

Table 12. 1.73 kHz RC OSC1 Frequency Limits

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
2.5 V ±8%	1.390	2.017	1.330	2.020	1.180	2.022
3.3 V ±10%	1.339	2.011	1.276	2.017	1.125	2.021
5 V ±10%	1.318	2.034	1.255	2.037	1.099	2.037
2.5 V to 4.5 V	1.318	2.016	1.255	2.019	1.099	2.022
2.5 to 5.5 V	1.318	2.034	1.255	2.037	1.099	2.037

Table 13: 1.73 kHz RC OSC1 Frequency Error (Error Calculated Relative to Nominal Value)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
2.5 V ±8%	-19.65%	16.58%	-23.12%	16.77%	-31.75%	16.85%

Table 13: 1.73 kHz RC OSC1 Frequency Error (Error Calculated Relative to Nominal Value) (continued)

Power Supply Range (V_{DD}), V	Temperature Range					
	+25 °C		0 °C to +85 °C		-40 °C to +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
3.3 V ±10%	-22.57%	16.23%	-26.21%	16.58%	-34.93%	16.85%
5 V ±10%	-23.79%	17.54%	-27.44%	17.73%	-36.47%	17.73%
2.5 V to 4.5 V	-23.79%	16.51%	-27.44%	16.73%	-36.47%	16.85%
2.5 V to 5.5 V	-23.79%	17.54%	-27.44%	17.73%	-36.47%	17.73%

5.8.3 OSC Power On delay

Table 14. Oscillators Power On delay at T = 25°C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC OSC Clock to Matrix Input: "Enable"

Power Supply Range (VDD) V	RC OSC0 2 MHz		RC OSC0 25 kHz		RC OSC1 1.73 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
2.30	691	1029	14.95	17.97	227.87	300.39
2.50	619	905	14.35	17.57	222.53	296.85
2.70	563	813	13.76	16.98	217.52	293.04
3.00	500	709	12.94	16.61	210.43	287. 82
3.30	454	638	9.67	36.51	203.51	283. 89
3.60	419	582	1.82	19.46	196.79	280. 17
4.20	370	510	1.79	2.70	183.73	272.25
4.50	352	484	1.89	2.94	177.64	267.27
5.00	328	454	2.09	3.28	169.40	258.96
5.50	309	428	2.21	3.45	165.60	248.45

Table 15. Oscillators Power On delay at T = 25°C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On", RC osc clock to matrix input: "Enable", Fast Start-up Time Mode

Power Supply Range (VDD) V	RC OSC0 2 MHz		RC OSC1 25 kHz	
	Typical Value, ns	Maximum Value, ns	Typical Value, µs	Maximum Value, µs
2.30	244	384	20.68	22.72
2.50	216	313	20.61	22.61
2.70	197	286	20.58	22.47
3.00	178	254	20.52	22.43
3.30	166	234	20.49	22.28
3.60	158	222	20.46	22.42
4.20	150	209	20.39	22.20
4.50	147	207	20.32	22.12
5.00	142	201	20.20	21.83
5.50	138	194	19.97	21.33

5.9 ACMP Specifications

Table 16. ACMP Specifications at T = -40 °C to +85 °C, VDD = 2.3 V to 5.5 V Unless Otherwise Noted

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input set to GPIO or VDD		0	--	V_{DD}	V
		Positive Input set to LDO VIN		0	--	V_{DD} - 0.4	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = (50..1200) mV	T = 25°C	-9.0	--	9.4	mV
				-12.3	--	12.8	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = (50..1200) mV	T = 25°C	-12.6	--	8.0	mV
				-9.2	--	9.9	mV
t_{start}	ACMP Start Time	ACMP Power On delay, Minimal required wake time for the “Wake and Sleep function”	T = 25°C	--	140	667	µS
				--	143	1369	µS
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled, T = 25°C	3.48	--	38.4	mV
			LB - Disabled, T = 25°C	14.6	--	36.7	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	43.9	--	57.1	mV
			LB - Disabled, T = 25°C	44.1	--	53.7	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled, T = 25°C	194.0	--	206.8	mV
			LB - Disabled, T = 25°C	194.4	--	203.3	mV
		V_{HYS} = 25 mV V_{IL} = Vin - V_{HYS}/2 V_{IH} = Vin + V_{HYS}/2	LB - Enabled	0.0	--	41.1	mV
			LB - Disabled	2.4	--	41.4	mV
		V_{HYS} = 50 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	37.7	--	64.9	mV
			LB - Disabled	43.6	--	55.4	mV
		V_{HYS} = 200 mV V_{IL} = Vin - V_{HYS} V_{IH} = V_{HYS}	LB - Enabled	187.5	--	214.0	mV
			LB - Disabled	192.4	--	205.1	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
PROP	Propagation Delay, Response Time for ACMP0 to ACMP3	Low Bandwidth - Enable, Gain = 1, Overdrive=10 mV	Low to High	--	11.2	51.9	µS
			High to Low	--	12.2	58	µS
		Low Bandwidth - Disable, Gain = 1, Overdrive=10 mV	Low to High	--	1.0	4.2	µS
			High to Low	--	1.0	3.7	µS
		Low Bandwidth - Enable, Gain = 1, Overdrive=100 mV	Low to High	--	4.8	22.8	µS
			High to Low	--	4.4	22.4	µS
		Low Bandwidth - Disable, Gain = 1, Overdrive=100 mV	Low to High	--	0.4	2.2	µS
			High to Low	--	0.4	0.7	µS
G	Gain error (including threshold and internal Vref error)	G = 1,		--	1	--	
		G = 0.5,		-0.81%	--	0.76%	
		G = 0.33,		-1.33%	--	1.4%	
		G = 0.25,		-1.43%	--	1.63%	

5.10 Low Drop Out “LDO” Regulator Electrical Specifications

All four LDO regulators within SLG46580 have the same electrical specification. Some circuits are common to all LDOs and so the current consumption varies depending on the number of Active LDOs. Each LDO has three modes – HP MODE is a typical 150 mA LDO regulator mode, and LP MODE is an ultra-low current regulator mode. The LDO also has an LDO Power Switch Mode when the LDO MOSFET simply turns into a load switch passing VIN to VOUT.

Both LDO regulators within SLG46582 have the same electrical specification. Some circuits are common to both LDOs so the current consumption varies depending on the number of Active LDOs. Each LDO has three modes – HP MODE is a typical 300 mA LDO regulator mode, and LP MODE is an ultra-low current regulator mode. The LDO also has an LDO Power Switch Mode when the LDO MOSFET simply turns into a load switch passing VIN to VOUT.

The LDO within SLG46583 has three modes – HP MODE is a typical 600 mA LDO regulator mode, and LP MODE is an ultra-low current regulator mode. The LDO also has an LDO Power Switch Mode when the LDO MOSFET simply turns into a load switch passing VIN to VOUT.

Table 17. LDO Current Consumption for SLG46580 at T = 25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	One LDO Regulator in HP Mode	--	32	--	µA
		Two LDO Regulators in HP Mode	--	48	--	µA
		Three LDO Regulators in HP Mode	--	64	--	µA
		Four LDO Regulators in HP Mode	--	80	--	µA
I_Q	Quiescent Current	One LDO Regulator in LP Mode	--	2	--	µA
		Two LDO Regulators in LP Mode	--	3	--	µA
		Three LDO Regulators in LP Mode	--	4	--	µA
		Four LDO Regulators in LP Mode	--	5	--	µA
Note: Typ. means under VDD = VIN = 3.3 V, VOUT = 2.0 V, no load.						

Table 18. LDO Current Consumption for SLG46582

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	One LDO Regulator in HP Mode	--	48	--	µA
		Two LDO Regulators in HP Mode	--	80	--	µA
I_Q	Quiescent Current	One LDO Regulator in LP Mode	--	3	--	µA
		Two LDO Regulators in LP Mode	--	5	--	µA
Note: Typ. means under VDD = VIN = 3.3 V, VOUT = 2.0 V, no load.						

Table 19. LDO Current Consumption for SLG46583

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_Q	Quiescent Current	LDO Regulator in HP Mode	--	80	--	µA
I_Q	Quiescent Current	LDO Regulator in LP Mode	--	5	--	µA

Note:
1. Typical values given are for VDD = 3.3 V, VIN = 3.3 V, VOUT = 2.1 V, @ room temperature

Table 20. LDO Regulator Thermal Limitations

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
IC_{TL}	Thermal Limitation	85 °C ambient, Total IC package	--	--	0.6	W
		70 °C ambient, Total IC package	--	--	0.8	W
Shutdown[2]	Thermal Shutdown[1]		89	103	117	°C
	Thermal Shutdown Recovery		83	87	91	°C

Note:
1. Lower Thermal shutdown levels may be achieved by using the temperature sensor and comparator.
2. T_A = 85 °C

Table 21. LDO HP MODE Electrical Specifications at T = 25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OUT}	Output Current Rating	per LDO (SLG46580)	--	--	150	mA
		per LDO (SLG46582)	--	--	300	mA
		SLG46583	--	--	600	mA
V_{IN}	Voltage Input		2.3	--	VDD	V
V_{DO}	Voltage Dropout		--	250	300	mV
ΔV_{OUT}	Output Voltage Accuracy (see Note 1)	over PVT of V_{OUT} > 1.5 V	-3	--	+3	%
		over PVT of $V_{OUT} \leq$ 1.5 V	-60	--	+60	mV
e_N	Noise Voltage (rms)	10 Hz to 100 kHz	--	75	--	µVrms
PSRR	Power Supply Rejection Ratio (see Note 2)	100 Hz to 100 kHz	--	50	--	dB
CTRR	Crosstalk Rejection Ratio	LDO0 to LDO1 regulation perturbation, and LDO2 to LDO3 perturbation at 0 to 150 mA at 1 kHz at 1.8 V V_{OUT}	--	50	--	dB
ΔV_{LINE}	Line Regulation	V_{OUT} + 0.5 V < $V_{IN} \leq$ 5.5 V	-1%	--	+1%	%/V

Table 21. LDO HP MODE Electrical Specifications at T = 25°C

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
ΔV_{LOAD}	Load Regulation	1 mA < I_{OUT} < 150 mA (SLG46580)	--	--	0.3	mV/mA
		1 mA < I_{OUT} < 300 mA (SLG46582)	--	--	0.15	mV/mA
		1 mA < I_{OUT} < 600 mA (SLG46583)	--	--	0.075	mV/mA
ΔV_{TC}	V_{OUT} Temp Coefficient		--	100	--	ppm/C
C_{IN}	External Input Capacitance (see Note 2)	per LDO (SLG46580)	2	--	--	µF
		per LDO (SLG46582)	2	--	--	µF
		SLG46583	4	--	--	µF
C_{OUT}	External Output Capacitance (see Note 2)	per LDO (SLG46580)	2	--	--	µF
		per LDO (SLG46582)	4	--	--	µF
		SLG46583	8	--	--	µF
SS0	SS Slew Rate 0	V_{OUT} = 5% to 95%	--	10	--	V/ms
SS1	SS Slew Rate 1	V_{OUT} = 5% to 95%	--	20	--	V/ms
SS2	SS Slew Rate 2	V_{OUT} = 5% to 95%	--	1.25	--	V/ms
SS3	SS Slew Rate 3	V_{OUT} = 5% to 95%	--	2.50	--	V/ms
OCL	Over-Current Limit	per LDO (SLG46580)	--	189	--	mA
		per LDO (SLG46582)	--	429	--	mA
		SLG46583	--	820	--	mA
SCD	Short-Circuit Detection Current Limit	V_{OUT} < 0.5 V, per LDO (SLG46580)	--	20	--	mA
		V_{OUT} < 0.5 V, per LDO (SLG46582)	--	40	--	mA
		V_{OUT} < 0.5 V, SLG46583	--	72	--	mA
t_{WAIT}	Wait Time	Time from EN=1 to V_{OUT} start rise	--	420	--	µs
R_D	Output Discharge Pull-down Resistance	Enable = 1, Disable = 0	--	300	--	Ω

Note:
1. *Accuracy specifies all the effects of line regulation (ΔV_{LINE}), load regulation (ΔV_{LOAD}), and temperature coefficient (ΔV_{TC}).*
2. *X7R-type and X5R-type capacitors are recommended.*

Table 22. LDO LP MODE Electrical Specifications at T = 25°C

Soft Start and Short Circuit protection circuits are not available in LDO LP MODE

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OUT}	Output Current Rating	per LDO (SLG46580)	--	--	100	µA
		per LDO (SLG46582)	--	--	200	µA
		SLG46583	--	--	400	µA
V_{IN}	Voltage Input		2.3	--	VDD	V
V_{DO}	Voltage Dropout		--	500	750	mV
ΔV_{OUT}	Output Voltage Accuracy	over PVT	-10	--	+10	%
C_{IN}	External Input Capacitance (see Note 1)	per LDO (SLG46580)	2	--	--	µF
		per LDO (SLG46582)	2	--	--	µF
		SLG46583	4	--	--	µF

Table 22. LDO LP MODE Electrical Specifications at T = 25°C

Soft Start and Short Circuit protection circuits are not available in LDO LP MODE

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
C_{OUT}	External Output Capacitance (see Note 1)	per LDO (SLG46580)	2	--	--	µF
		per LDO (SLG46582)	4	--	--	µF
		SLG46583	8	--	--	µF
R_D	Output Discharge Pull-down Resistance	Enable = 1, Disable = 0	--	300	--	Ω

Note:
1. X7R-type and X5R-type capacitors are recommended.

Table 23. LDO Power Switch Mode Electrical Specifications at T = 25°C

Soft Start and Short Circuit protection circuits are not available in LDO Power Switch Mode

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I_{OUT}	Output Current Rating	per LDO (SLG46580)	--	--	150	mA
		per LDO (SLG46582)	--	--	300	mA
		SLG46583	--	--	600	mA
V_{IN}	Voltage Input		2.3	--	VDD	V
RDS_{ON}	MOSFET ON resistance	P-Channel with V_{IN} at 2.3, per LDO (SLG46580)	--	1	--	Ω
		P-Channel with V_{IN} at 2.3, per LDO (SLG46582)	--	0.5	--	Ω
		P-Channel with V_{IN} at 2.3 (SLG46583)	--	0.3	--	Ω
I_Q	Quiescent Current	No load, per LDO (SLG46580)	--	1.1	--	µA
		No load, per LDO (SLG46582)	--	2	--	µA
		No load (SLG46583)	--	3.8	--	µA

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs (NMOS and PMOS)
- Push Pull Outputs (1x and 2x)
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- IO0, IO4, IO6 and IO8 can be configured as bidirectional I/O

6.2 Low Dropout Regulators

- Four Tri-Mode 150 mA LDO Regulators (for SLG46580):
  - High Power Mode (HP Mode): 150 mA output with Quiescent Current at ~32 µA per LDO
  - Low Power Mode (LP Mode): 100 µA output with Quiescent Current at ~2 µA per LDO
  - Power Switch Mode: Acts like a load switch
- Two Tri-Mode 300 mA LDO Regulators (for SLG46582):
  - High Power Mode (HP Mode): 300 mA output with Quiescent Current at ~48 µA per LDO
  - Low Power Mode (LP Mode): 200 µA output with Quiescent Current at ~3 µA per LDO
  - Power Switch Mode: Acts like a load switch
- One Tri-Mode 600 mA LDO Regulators (for SLG46583):
  - High Power Mode (HP Mode): 600 mA output with Quiescent Current at ~80 µA
  - Low Power Mode (LP Mode): 400 µA output with Quiescent Current at ~5 µA
  - Power Switch Mode: Acts like a load switch

6.3 Connection Matrix

- Digital matrix for circuit connections based on user design

6.4 Analog Comparators (4 total)

- Selectable hysteresis 0 mV / 25 mV / 50 mV / 200 mV
  - Additionally ACMP2 and ACMP3 support 100 mV and 150 mV
- Wake and Sleep Control (Part of Combination Function Macrocell)

6.5 Voltage Reference

- Used for references on Analog Comparators

6.6 Combination Function Macrocells (15 total)

- Three Selectable DFF/Latch or 2-bit LUTs
- Six Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
- Five Selectable 8-bit CNT/DLY or 3-bit LUT

6.7 Combinatorial Logic (1 total)

- One 4-bit LUT with two outputs

6.8 Asynchronous State Machine

- Eight States
- Flexible input logic from state transitions

6.9 Serial Communications

- I^2C Protocol compliant - Fast-Mode, and Fast-Mode Plus

6.10 Programmable Delay

- 125 ns/250 ns/375 ns/500 ns @ 3.3 V
- Includes Edge Detection function

6.11 Additional Logic Functions (2 total)

- Two Deglitch filter macrocells with Edge Detection function

6.12 Oscillators

- 25 kHz and 2 MHz selectable frequency
  - First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
  - Second stage divider for 25 kHz and 2 MHz (5): Output to Matrix: OSC/1, OSC/2, OSC/3, OSC/4, OSC/8, OSC/12, OSC/24, OSC/64
- 1.73 kHz Low Power Oscillator
  - First stage divider (4): LPOSC/1, LPOSC/2, LPOSC/4 and LPOSC/16

6.13 Eight byte RAM + OTP User Memory

- RAM with I^2C interface
- User defined initial values transferred from OTP

6.14 Real Time Clock (RTC) Binary Counter

6.15 Power On Reset

7.0 I/O Pins

The SLG46580/82/83 has a total of 9 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- IO0: General Purpose Input or Output with OE
- IO1 General Purpose Input or Output or Analog Comparator 0(+)
- IO2: General Purpose Input or Output
- IO3: General Purpose Input or Output
- IO4: General Purpose Input or Output with OE or Analog Comparator 1(+)
- IO5: General Purpose Input
- VDD: V_{DD} Power supply
- SCL: I2C_SCL
- SDA: I2C_SDA
- IO6: General Purpose Input or Output with OE or Analog Comparator (-)
- SLG46580:
  - LDO0 VOUT: LDO0 Output or Analog Comparator 3(+)
  - LDO0/1 VIN: LDO0 & LDO1 Input or Analog Comparator 0(+)
  - LDO1 VOUT: LDO1 Output
  - LDO2 VOUT: LDO2 Output or Analog Comparator 3(+)
  - LDO2/3 VIN: LDO2 & LDO3 Input or Analog Comparator 1(+)
  - LDO3 VOUT: LDO3 Output
- SLG46582:
  - LDO0 VOUT: LDO0 Output or Analog Comparator 3(+)
  - LDO0 VIN: LDO0 Input or Analog Comparator 0(+)
  - LDO0 VOUT: LDO0 Output
  - LDO1 VOUT: LDO1 Output or Analog Comparator 3(+)
  - LDO1 VIN: LDO1 Input or Analog Comparator 1(+)
  - LDO1 VOUT: LDO1 Output
- SLG46583:
  - LDO VOUT: LDO Output or Analog Comparator 3(+)
  - LDO VIN: LDO Input or Analog Comparator 0(+)
  - LDO VOUT: LDO Output
  - LDO VOUT: LDO Output or Analog Comparator 3(+)
  - LDO VIN: LDO Input or Analog Comparator 1(+)
  - LDO VOUT: LDO Output
- AGND: LDO Ground
- IO7: General Purpose Input or Output or Analog Comparator 2(+)
- IO8: General Purpose Input or Output with OE or Analog Comparator 3(+)
- GND: Ground

Programming Mode pin definitions are as follows:

- IO5: V_{PP} Programming voltage
- VDD: V_{DD} Power supply
- SCL: Programming SCL
- SDA: Programming SDA
- IO7: Programming Mode Control
- GND: Ground

Of the 9 user defined I/O pins on the SLG46580/82/83, all but one of the pins (IO5) can serve as both digital input and digital output. IO5 can only serve as a digital input pin with RESET function, which has settings as follows:

- Level polarity:
  - Non-inverted
  - Inverted
- Reset mode:
  - Level sensitive
  - Edge triggered
- Edge detection:
  - Rising edge
  - Falling edge

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without Schmitt Trigger and low voltage input. IO1, IO4, IO7, and IO8 can also be configured to serve as analog inputs to the on-chip comparators. IO6 can also be configured as ACMP reference voltage input.

7.2 Output Modes

Pins IO0, IO1, IO2, IO3, IO4, IO6, IO7, and IO8 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of IO5, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 IO0 Register Settings

Table 24. IO0 Register Settings

Signal Function	Register Bit Address	Register Definition
IO0 Pull Up/Down Resistor Selection	<1025>	0: Pull Down Resistor 1: Pull Up Resistor
IO0 Pull Up/Down Resistor Value Selection	<1027:1026>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO0 Mode Control (sig_io0_oe =0)	<1029:1028>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO0 Mode Control (sig_io0_oe =1)	<1031:1030>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

7.4.2 IO1Register Settings

Table 25. IO1 Register Settings

Signal Function	Register Bit Address	Register Definition
IO1 Driver Strength Selection	<1033>	0: 1X 1: 2X
IO1 Pull Up/Down Resistor Selection	<1034>	0: Pull Down Resistor 1: Pull Up Resistor
IO1 Pull Down Resistor Value Selection	<1036:1035>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO1 Mode Control	<1039:1037>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input and Open Drain

7.4.3 IO2 Register Settings

Table 26. IO2 Register Settings

Signal Function	Register Bit Address	Register Definition
IO2 Driver Strength Selection	<1041>	0: 1X 1: 2X
IO2 Pull Up/Down Resistor Selection	<1042>	0: Pull Down Resistor 1: Pull Up Resistor
IO2 Pull Down Resistor Value Selection	<1044:1043>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO2 Mode Control	<1047:1045>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved

7.4.4 IO3 Register Settings

Table 27. IO3 Register Settings

Signal Function	Register Bit Address	Register Definition
IO3 Driver Strength Selection	<1049>	0: 1X 1: 2X
IO3 Pull Up/Down Resistor Selection	<1050>	0: Pull Down Resistor 1: Pull Up Resistor
IO3 Pull Down Resistor Value Selection	<1052:1051>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO3 Mode Control	<1055:1053>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS

7.4.5 IO4 Register Settings

Table 28. IO4 Register Settings

Signal Function	Register Bit Address	Register Definition
IO4 Pull Up/Down Resistor Selection	<1057>	0: Pull Down Resistor 1: Pull Up Resistor
IO4 Pull Up/Down Resistor Value Selection	<1059:1058>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO4 Mode Control (sig_io4_oe =0)	<1061:1060>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO4 Mode Control (sig_io4_oe =1)	<1063:1062>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

7.4.6 IO5 Register Settings

Table 29. IO5 Register Settings

Signal Function	Register Bit Address	Register Definition
IO5 Pull Down Resistor Value Selection	<1069:1068>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO5 Mode Control	<1071:1070>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
IO5 reset level polarity selection	reg<1304>	0: Non-inverted 1: Inverted
IO5 reset bypass selection	reg<1305>	0: Edge selection 1: Level selection
IO5 reset edge selection	reg<1306>	0: Rising edge 1: Falling edge
IO5 reset enable	reg<1307>	0: Disable 1: Enable

7.4.7 SCL Register Settings

Table 30. SCL Register Settings

Signal Function	Register Bit Address	Register Definition
SCL Mode Control	<1078:1077>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

7.4.8 SDA Register Settings

Table 31. SDA Register Settings

Signal Function	Register Bit Address	Register Definition
SDA Driver Strength Selection	<1081>	0: 1X 1: 2X
SDA Mode Control	<1086:1085>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

7.4.9 IO6 Register Settings

Table 32. IO6 Register Settings

Signal Function	Register Bit Address	Register Definition
IO6 Pull Up/Down Resistor Selection	<1089>	0: Pull Down Resistor 1: Pull Up Resistor
IO6 Pull Up/Down Resistor Value Selection	<1091:1090>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO6 Mode Control (sig_io6_oe =0)	<1093:1092>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO6 Mode Control (sig_io6_oe =1)	<1095:1094>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

7.4.10 IO7 Register Settings

Table 33. IO7 Register Settings

Signal Function	Register Bit Address	Register Definition
IO7 Driver Strength Selection	<1097>	0: 1X 1: 2X
IO7 Pull Up/Down Resistor Selection	<1098>	0: Pull Down Resistor 1: Pull Up Resistor
IO7 Pull Up/Down Resistor Value Selection	<1100:1099>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO7 Mode Control	<1103:1101>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input and Open Drain

7.4.11 IO8 Register Settings

Table 34. IO8 Register Settings

Signal Function	Register Bit Address	Register Definition
IO8 Pull Up/Down Resistor Selection	<1105>	0: Pull Down Resistor 1: Pull Up Resistor
IO8 Pull Up/Down Resistor Value Selection	<1107:1106>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
IO8 Mode Control (sig_io8_oe =0)	<1109:1108>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
IO8 Mode Control (sig_io8_oe =1)	<1111:1110>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

7.5 GPI Structure

7.5.1 GPI Structure (for IO5)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note 1: OE cannot be selected by user
Note 2: OE is Matrix output, Digital In is Matrix input

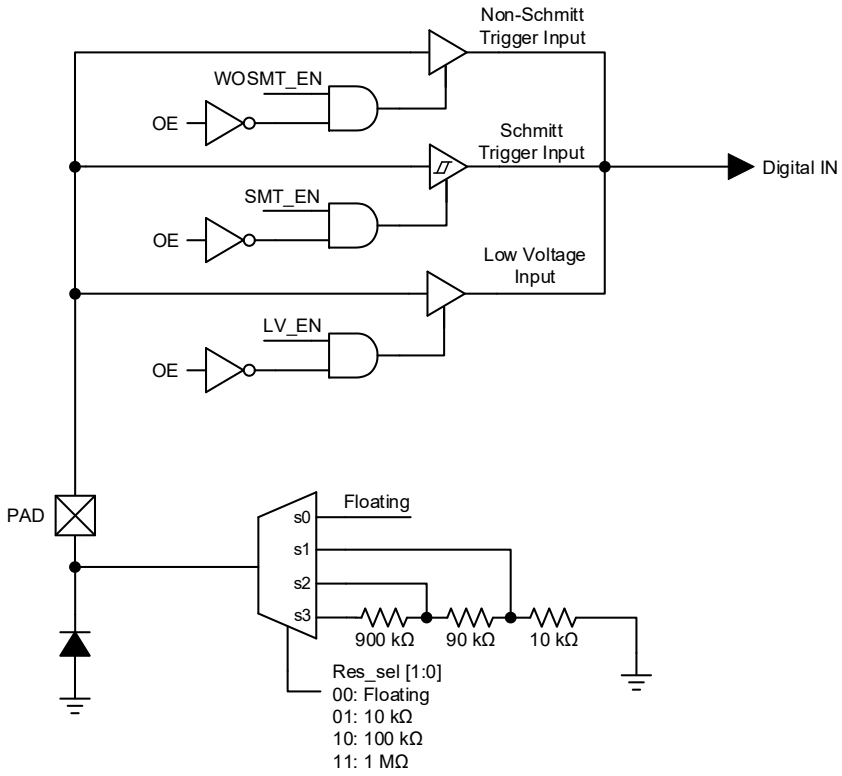


Figure 2. IO5 GPI Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for IO0, IO4, IO6, IO8)

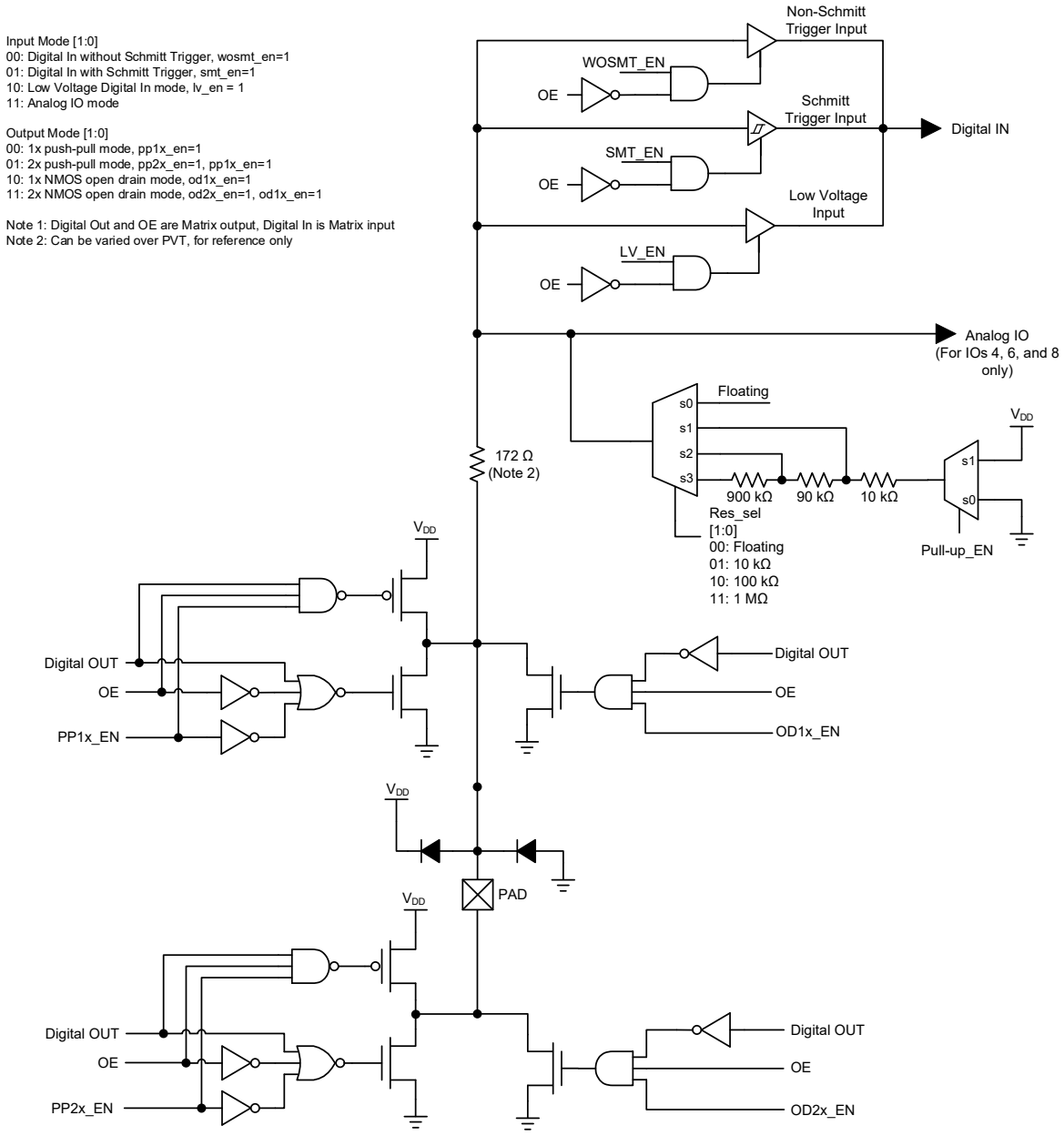


Figure 3. Matrix OE IO Structure Diagram

7.6.2 Matrix OE IO Structure (for SCL and SDA)

SCL, SDA Mode[1:0]
00: Digital Input without Schmitt Trigger, wosmt_en=1
01: Digital Input with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital Input, lv_en = 1
11: Reserved

Note 1: Digital Out and OE are Matrix output, Digital In is Matrix input
Note 2: Output mode is fixed as OD for SDA only

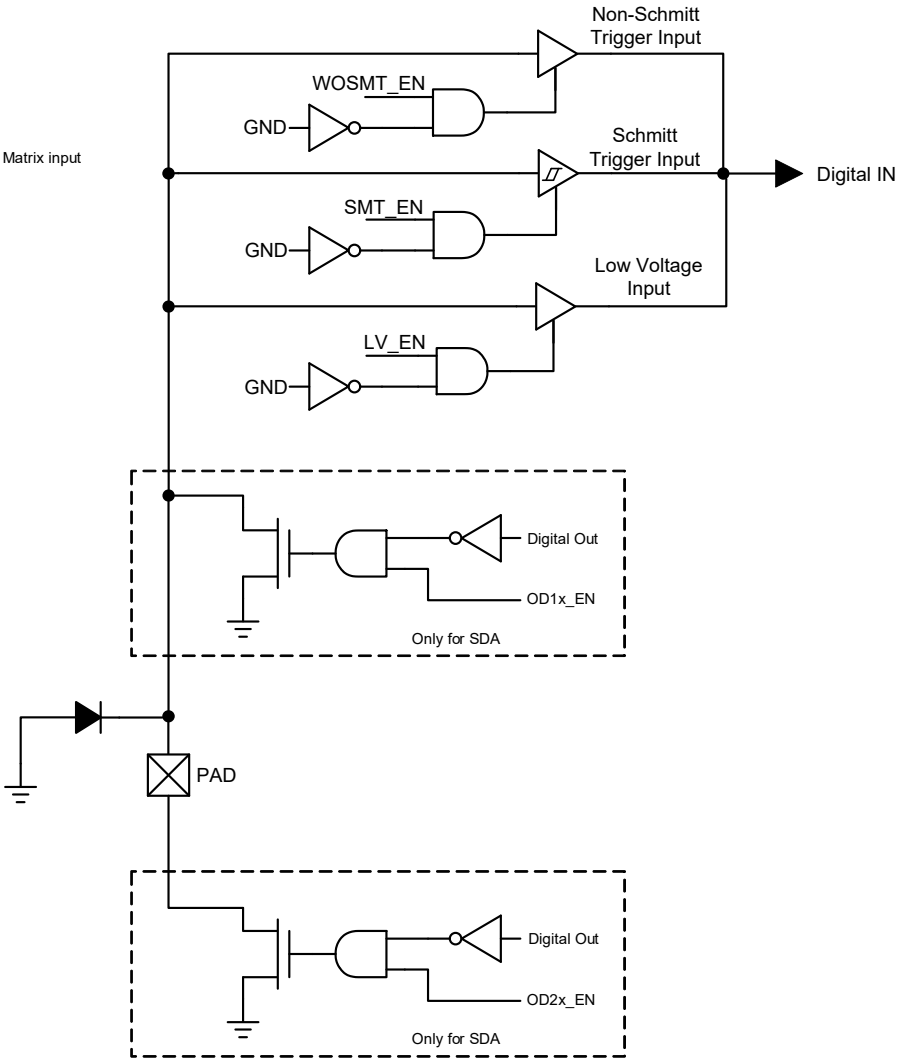


Figure 4. Matrix OE IO Structure Diagram

7.7 IO Structure

7.7.1 IO Structure (for IO1, IO2, IO3, and IO7)

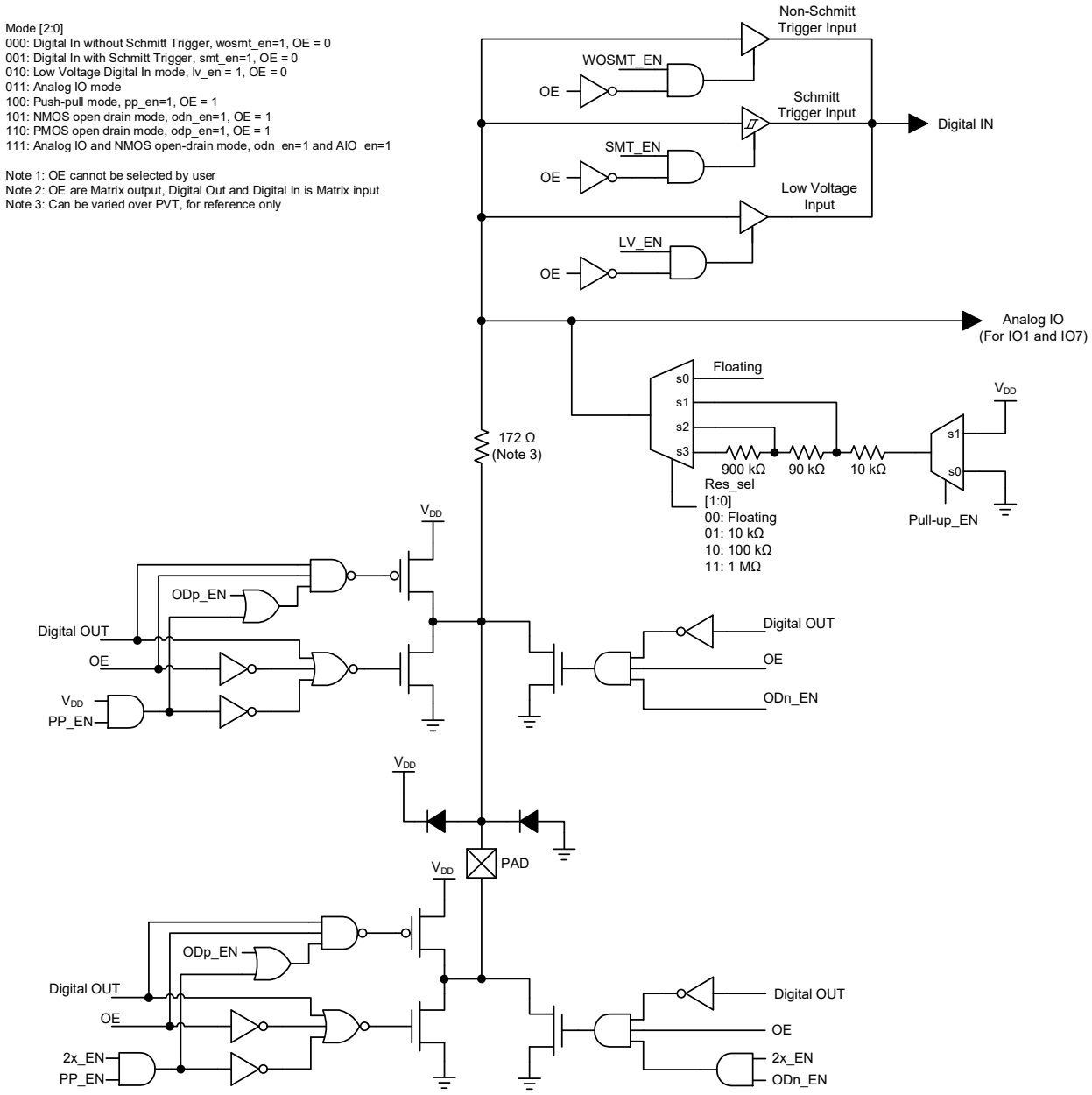


Figure 5. IO Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46580/82/83 is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46580/82/83 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 2048 register bits within the SLG46580/82/83 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 104 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and VDD and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46580/82/83’s register table, see Section *25.0 Appendix A - SLG46580/82/83 Register Definition*.

Matrix Input Signal Functions	N
GND	0
IO0 Digital In	1
IO1 Digital In	2
IO2 Digital In	3
⋮	⋮
nRST_core (POR)	62
VDD	63

Matrix Inputs / Matrix Outputs	N	0	1	2	⋯	104
	Registers	reg<5:0>	reg<13:8>	reg<21:16>	⋯	reg<839:832>
	Function	Matrix OUT: ASM-state0-EN0	Matrix OUT: ASM-state0-EN1	Matrix OUT: ASM-state0-EN2	⋯	Reserved

Figure 6. Connection Matrix

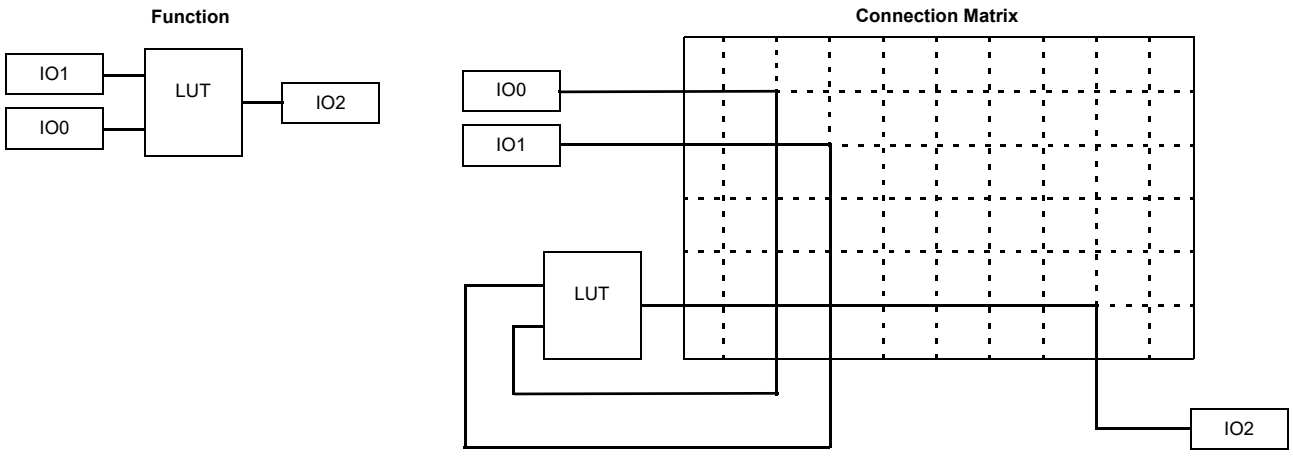


Figure 7. Connection Matrix Example

8.1 Matrix Input Table

Table 35. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	IO0 Digital Input	0	0	0	0	0	1
2	IO1 Digital Input	0	0	0	0	1	0
3	IO2 Digital Input	0	0	0	0	1	1
4	IO3 Digital Input	0	0	0	1	0	0
5	IO4 Digital Input	0	0	0	1	0	1
6	LUT2_0 / DFF0 Output	0	0	0	1	1	0
7	LUT2_1 / DFF1 Output	0	0	0	1	1	1
8	LUT2_2 / DFF2 Output	0	0	1	0	0	0
9	LUT3_0 / DFF3 Output	0	0	1	0	0	1
10	LUT3_1 / DFF4 Output	0	0	1	0	1	0
11	LUT3_2 / DFF5 Output	0	0	1	0	1	1
12	LUT3_3 / DFF6 Output	0	0	1	1	0	0
13	LUT3_4 / DFF7 Output	0	0	1	1	0	1
14	LUT3_6 / CNT_DLY0(8bit) Output	0	0	1	1	1	0
15	LUT3_7 / CNT_DLY1(8bit) Output	0	0	1	1	1	1
16	LUT3_8 / CNT_DLY2(8bit) Output	0	1	0	0	0	0
17	LUT3_9 / CNT_DLY3(8bit) Output	0	1	0	0	0	1
18	LUT3_10 / CNT_DLY4(8bit) Output	0	1	0	0	1	0
19	LUT3_11 / Pipe Delay (1st stage) Output / Ripple CNT Output0	0	1	0	0	1	1
20	LUT3_5 / DFF8 Output	0	1	0	1	0	0
21	LUT4X2_0 Output0	0	1	0	1	0	1
22	LUT4X2_0 Output1	0	1	0	1	1	0
23	RTC CNT 1 second Output	0	1	0	1	1	1
24	RTC DCOMP Output	0	1	1	0	0	0
25	Pipe Delay Output0 / Ripple CNT Output1	0	1	1	0	0	1
26	Pipe Delay Output1 / Ripple CNT Output2	0	1	1	0	1	0
27	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz)	0	1	1	0	1	1
28	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz)	0	1	1	1	0	0
29	LPOSC Output	0	1	1	1	0	1
30	Filter0 / Edge Detect0 Output	0	1	1	1	1	0
31	Filter1 / Edge Detect1 Output	0	1	1	1	1	1
32	I2C_virtual_0 Input	1	0	0	0	0	0
33	I2C_virtual_1 Input	1	0	0	0	0	1
34	I2C_virtual_2 Input	1	0	0	0	1	0
35	I2C_virtual_3 Input	1	0	0	0	1	1

Table 35. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
36	I2C_virtual_4 Input	1	0	0	1	0	0
37	I2C_virtual_5 Input	1	0	0	1	0	1
38	I2C_virtual_6 Input	1	0	0	1	1	0
39	I2C_virtual_7 Input	1	0	0	1	1	1
40	ASM-stateX-dout0	1	0	1	0	0	0
41	ASM-stateX-dout1	1	0	1	0	0	1
42	ASM-stateX-dout2	1	0	1	0	1	0
43	ASM-stateX-dout3	1	0	1	0	1	1
44	ASM-stateX-dout4	1	0	1	1	0	0
45	ASM-stateX-dout5	1	0	1	1	0	1
46	ASM-stateX-dout6	1	0	1	1	1	0
47	ASM-stateX-dout7	1	0	1	1	1	1
48	BG_OK Output	1	1	0	0	0	0
49	LDO0 nFault (SLG46580 and SLG46582) LDO nFault (SLG46583)	1	1	0	0	0	1
50	LDO1 nFault (SLG46580 and SLG46582)	1	1	0	0	1	0
51	LDO2 nFault (SLG46580)	1	1	0	0	1	1
52	LDO3 nFault (SLG46580)	1	1	0	1	0	0
53	IO5 Digital Input (GPI)	1	1	0	1	0	1
54	IO6 Digital Input	1	1	0	1	1	0
55	IO7 Digital Input	1	1	0	1	1	1
56	IO8 Digital Input	1	1	1	0	0	0
57	ACMP_0 Output	1	1	1	0	0	1
58	ACMP_1 Output	1	1	1	0	1	0
59	ACMP_2 Output	1	1	1	0	1	1
60	ACMP_3 Output	1	1	1	1	0	0
61	Programmable Delay with Edge Detector Output	1	1	1	1	0	1
62	nRST_core (POR) as matrix input	1	1	1	1	1	0
63	VDD	1	1	1	1	1	1

8.2 Matrix Output Table

Table 36. Matrix Output Table

Register Bit Address	Matrix Output Signal Function Note: For each Address, the two most significant bits are unused)	Matrix Output Number
reg <7:0>	Matrix OUT: ASM-state0-EN0	0
reg <15:8>	Matrix OUT: ASM-state0-EN1	1
reg <23:16>	Matrix OUT: ASM-state0-EN2	2
reg <31:24>	Matrix OUT: ASM-state1-EN0	3
reg <39:32>	Matrix OUT: ASM-state1-EN1	4
reg <47:40>	Matrix OUT: ASM-state1-EN2	5
reg <55:48>	Matrix OUT: ASM-state2-EN0	6
reg <63:56>	Matrix OUT: ASM-state2-EN1	7
reg <71:64>	Matrix OUT: ASM-state2-EN2	8
reg <79:72>	Matrix OUT: ASM-state3-EN0	9
reg <87:80>	Matrix OUT: ASM-state3-EN1	10
reg <95:88>	Matrix OUT: ASM-state3-EN2	11
reg <103:96>	Matrix OUT: ASM-state4-EN0	12
reg <111:104>	Matrix OUT: ASM-state4-EN1	13
reg <119:112>	Matrix OUT: ASM-state4-EN2	14
reg <127:120>	Matrix OUT: ASM-state5-EN0	15
reg <135:128>	Matrix OUT: ASM-state5-EN1	16
reg <143:136>	Matrix OUT: ASM-state5-EN2	17
reg <151:144>	Matrix OUT: ASM-state6-EN0	18
reg <159:152>	Matrix OUT: ASM-state6-EN1	19
reg <167:160>	Matrix OUT: ASM-state6-EN2	20
reg <175:168>	Matrix OUT: ASM-state7-EN0	21
reg <183:176>	Matrix OUT: ASM-state7-EN1	22
reg <191:184>	Matrix OUT: ASM-state7-EN2	23
reg <199:192>	Matrix OUT: ASM-state-nRST	24
reg <207:200>	Matrix OUT: IN0 of LUT3_6 or Delay0 Input (or Counter0 RST Input)	25
reg <215:208>	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay0 (or Counter0)	26
reg <223:216>	Matrix OUT: IN2 of LUT3_6	27
reg <231:224>	Matrix OUT: IN0 of LUT3_7 or Delay1 Input (or Counter1 RST Input)	28
reg <239:232>	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay1 (or Counter1)	29
reg <247:240>	Matrix OUT: IN2 of LUT3_7	30
reg <255:248>	Matrix OUT: IN0 of LUT3_8 or Delay2 Input (or Counter2 RST Input)	31
reg <263:256>	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay2 (or Counter2)	32
reg <271:264>	Matrix OUT: IN2 of LUT3_8	33
reg <279:272>	Matrix OUT: IN0 of LUT3_9 or Delay3 Input (or Counter3 RST Input)	34
reg <287:280>	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay3 (or Counter3)	35
reg <295:288>	Matrix OUT: IN2 of LUT3_9	36
reg <303:296>	Matrix OUT: IN0 of LUT3_10 or Delay4 Input (or Counter4 RST Input)	37

Table 36. Matrix Output Table

Register Bit Address	Matrix Output Signal Function Note: For each Address, the two most significant bits are unused)	Matrix Output Number
reg <311:304>	Matrix OUT: IN1 of LUT3_10 or External Clock Input of Delay4 (or Counter4)	38
reg <319:312>	Matrix OUT: IN2 of LUT3_10	39
reg <327:320>	Matrix OUT: IO0 Digital Output Source	40
reg <335:328>	Matrix OUT: IO0 Output Enable	41
reg <343:336>	Matrix OUT: IO1 Digital Output Source	42
reg <351:344>	Matrix OUT: IO2 Digital Output Source	43
reg <359:352>	Matrix OUT: IO3 Digital Output Source	44
reg <367:360>	Matrix OUT: IO4 Digital Output Source	45
reg <375:368>	Matrix OUT: IO4 Output Enable	46
reg <383:376>	Matrix OUT: IO6 Digital Output Source	47
reg <391:384>	Matrix OUT: IO6 Output Enable	48
reg <399:392>	Matrix OUT: IO7 Digital Output Source	49
reg <407:400>	Matrix OUT: IO8 Digital Output Source	50
reg <415:408>	Matrix OUT: IO8 Output Enable	51
reg <423:416>	Matrix OUT: ACMP0 PD (Power Down)	52
reg <431:424>	Matrix OUT: ACMP1 PD (Power Down)	53
reg <439:432>	Matrix OUT: ACMP2 PD (Power Down)	54
reg <447:440>	Matrix OUT: ACMP3 PD (Power Down)	55
reg <455:448>	Matrix OUT: Input of Filter_0 with fixed time edge detector	56
reg <463:456>	Matrix OUT: Input of Filter_1 with fixed time edge detector	57
reg <471:464>	Matrix OUT: Input of Programmable Delay & Edge Detector	58
reg <479:472>	Matrix OUT: OSC 25KHz/2MHz PD (Power Down)	59
reg <487:480>	Matrix OUT: LPOSC PD (Power Down)	60
reg <495:488>	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0	61
reg <503:496>	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0	62
reg <511:504>	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1	63
reg <519:512>	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1	64
reg <527:520>	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2	65
reg <535:528>	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2	66
reg <543:536>	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3	67
reg <551:544>	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3	68
reg <559:552>	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3	69
reg <567:560>	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4	70
reg <575:568>	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4	71
reg <583:576>	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4	72
reg <591:584>	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5	73
reg <599:592>	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5	74
reg <607:600>	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5	75
reg <615:608>	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6	76

Table 36. Matrix Output Table

Register Bit Address	Matrix Output Signal Function Note: For each Address, the two most significant bits are unused)	Matrix Output Number
reg <623:616>	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6	77
reg <631:624>	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6	78
reg <639:632>	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7	79
reg <647:640>	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7	80
reg <655:648>	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7	81
reg <663:656>	Matrix OUT: IN0 of LUT3_11 or Input of Pipe Delay or Up/Down selection of Ripple Counter	82
reg <671:664>	Matrix OUT: IN1 of LUT3_11 or nRST of Pipe Delay or nRST of Ripple Counter	83
reg <679:672>	Matrix OUT: IN2 of LUT3_11 or Clock of Pipe Delay or Clock of Ripple Counter	84
reg <687:680>	Matrix OUT: IN0 of LUT3_5 or Clock Input of DFF8	85
reg <695:688>	Matrix OUT: IN1 of LUT3_5 or Data Input of DFF8	86
reg <703:696>	Matrix OUT: IN2 of LUT3_5 or nRST (nSET) of DFF8	87
reg <711:704>	Matrix OUT: IN0 of LUT4X2_0	88
reg <719:712>	Matrix OUT: IN1 of LUT4X2_0	89
reg <727:720>	Matrix OUT: IN2 of LUT4X2_0	90
reg <735:728>	Matrix OUT: IN3 of LUT4X2_0	91
reg <743:736>	Matrix OUT: LDO LP Mode Enable for LDO0/1/2/3 (SLG46580) for LDO0/1 (SLG46582) for LDO (SLG46583)	92
reg <751:744>	Matrix OUT: LDO0_EN (SLG46580 and SLG46582) LDO_EN (SLG46583)	93
reg <759:752>	Matrix OUT: LDO1_EN (SLG46580)	94
reg <767:760>	Matrix OUT: LDO2_EN (SLG46580) Matrix OUT: LDO1_EN (SLG46582)	95
reg <775:768>	Matrix OUT: LDO3_EN (SLG46580)	96
reg <783:776>	Matrix OUT: LDO0 2nd VOUT Selection Enable (SLG46580 and SLG46582) LDO 2nd VOUT Selection Enable (SLG46583)	97
reg <791:784>	Matrix OUT: LDO1 2nd VOUT Selection Enable (SLG46580)	98
reg <799:792>	Matrix OUT: LDO2 2nd VOUT Selection Enable (SLG46580) Matrix OUT: LDO1 2nd VOUT Selection Enable (SLG46582)	99
reg <807:800>	Matrix OUT: LDO3 2nd VOUT Selection Enable (SLG46580)	100
reg <815:808>	Matrix OUT: RTC Clock	101
reg <823:816>	Matrix OUT: RTC Trigger signal to read/write RTC CNT values	102
reg <831:824>	Reserved	103
reg <839:832>	Reserved	104

8.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0xF4 (0244).

Eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

See table below for Connection Matrix Virtual Inputs.

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I2C_virtual_0 Input	reg<1952>
33	I2C_virtual_1 Input	reg<1953>
34	I2C_virtual_2 Input	reg<1954>
35	I2C_virtual_3 Input	reg<1955>
36	I2C_virtual_4 Input	reg<1956>
37	I2C_virtual_5 Input	reg<1957>
38	I2C_virtual_6 Input	reg<1958>
39	I2C_virtual_7 Input	reg<1959>

8.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are 0x70 (0112) to 0x71 (0113). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at 0xF4 (0244)).

9.0 Combination Function Macrocells

The SLG46580/82/83 has 15 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- Three macrocells that can serve as either 2-bit LUTs or as D Flip Flops.
- Six macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay or as a Ripple Counter
- Five macrocells that can serve as either 3-bit LUTs or as 8-Bit Counter / Delays

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT or D Flip Flop Macrocells

There are three macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

- DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change
- Latch: if CLK = 0, then Q = D

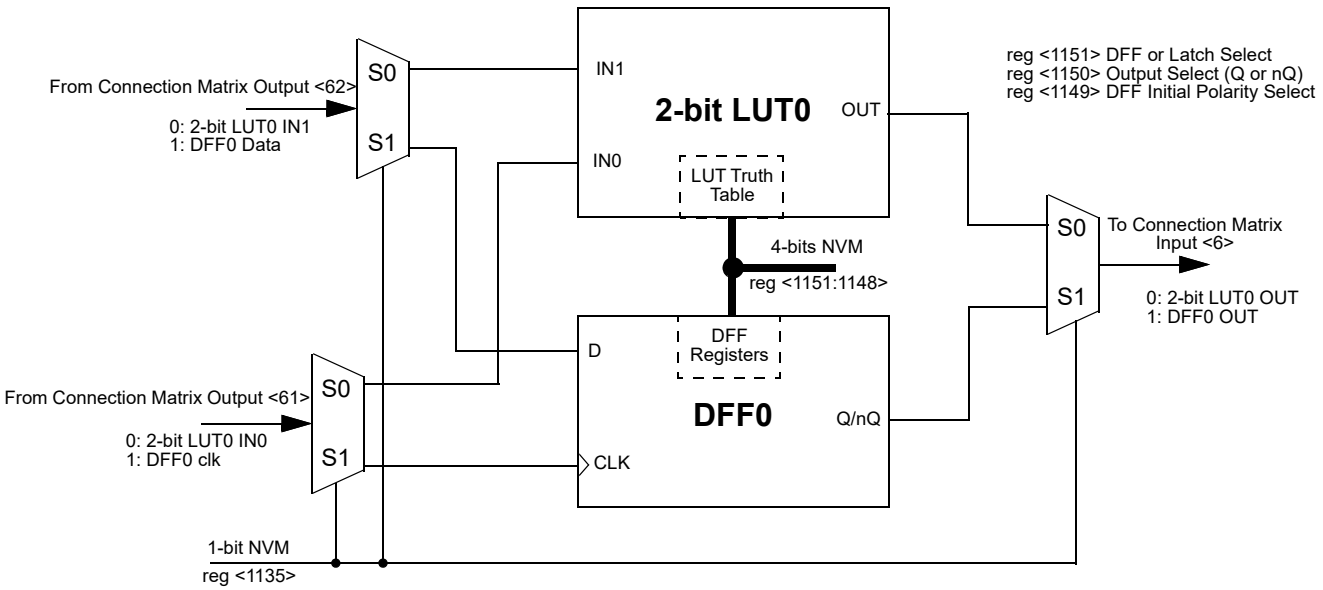


Figure 8. 2-bit LUT0 or DFF0

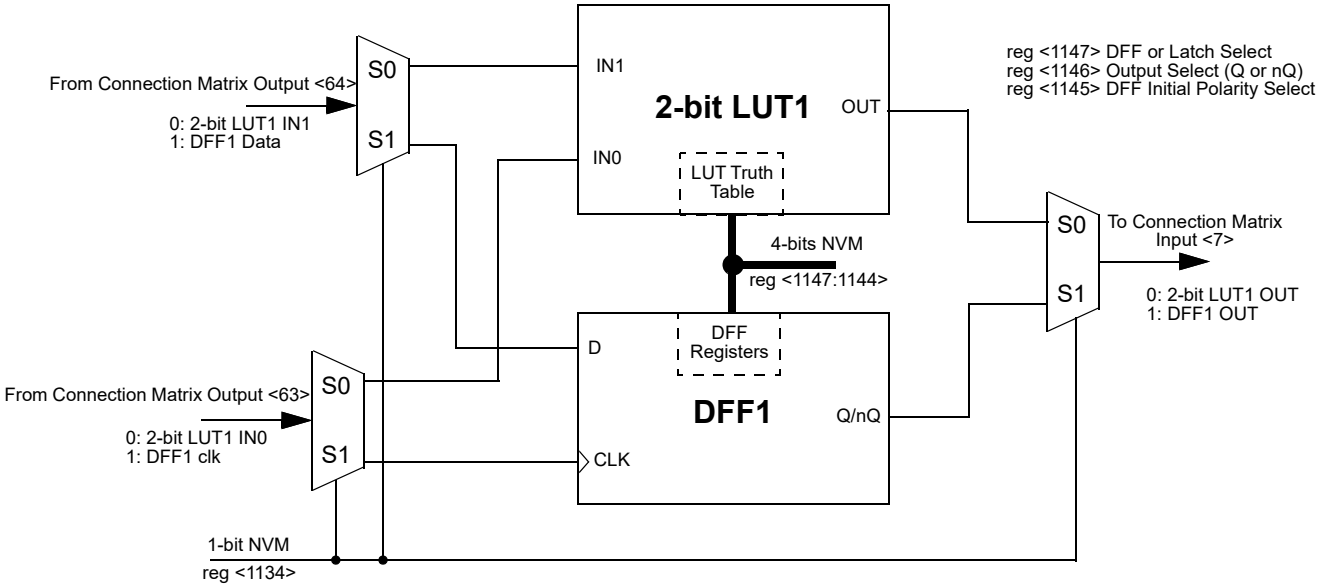


Figure 9. 2-bit LUT1 or DFF1

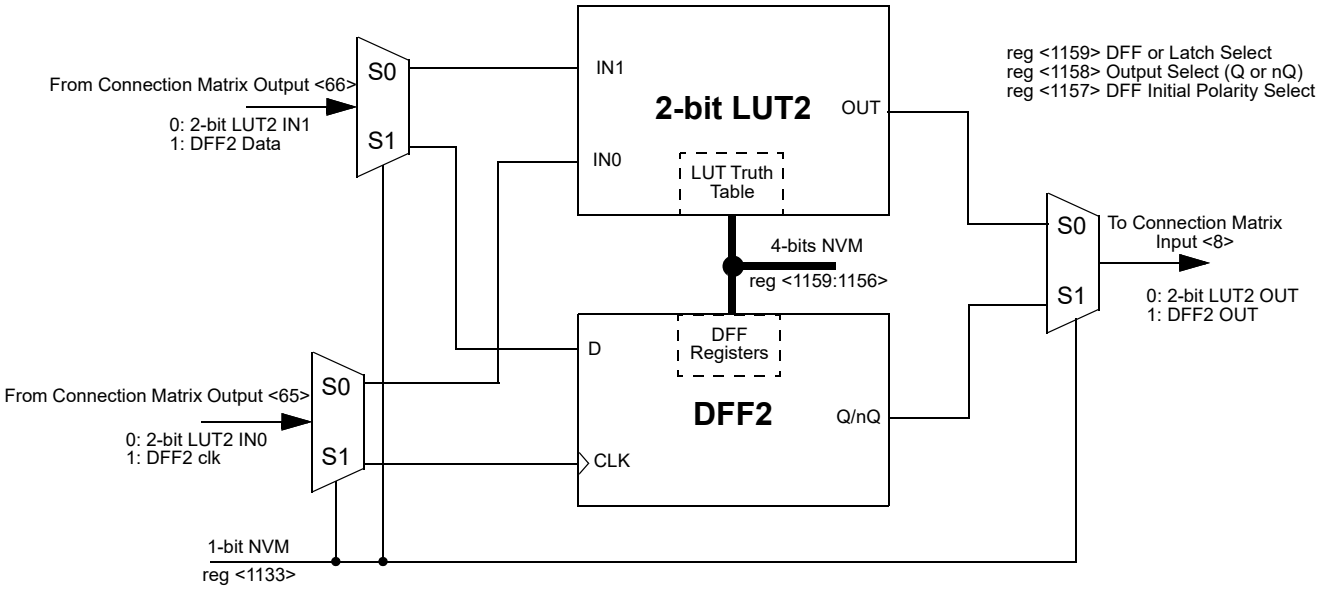


Figure 10. 2-bit LUT2 or DFF2

9.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 37. 2-bit LUT0 Truth Table.

IN1	IN0	OUT	
0	0	reg <1148>	LSB
0	1	reg <1149>	
1	0	reg <1150>	
1	1	reg <1151>	MSB

Table 38. 2-bit LUT1 Truth Table.

IN1	IN0	OUT	
0	0	reg <1144>	LSB
0	1	reg <1145>	
1	0	reg <1146>	
1	1	reg <1147>	MSB

Table 39. 2-bit LUT2 Truth Table.

IN1	IN0	OUT	
0	0	reg <1156>	LSB
0	1	reg <1157>	
1	0	reg <1158>	
1	1	reg <1159>	MSB

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg<1151:1148>

2-Bit LUT1 is defined by reg<1147:1144>

2-Bit LUT2 is defined by reg<1159:1156>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the three 2-bit LUT logic cells.

Table 40. 2-bit LUT Standard Digital Functions.

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 41. DFF0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_0 or DFF0 Select	reg<1135>	0: LUT2_0 1: DFF0
DFF0 Initial Polarity Select	reg<1149>	0: Low 1: High
DFF0 Output Select	reg<1150>	0: Q output 1: nQ output
DFF0 or Latch Select	reg<1151>	0: DFF function 1: Latch function

Table 42. DFF1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_1 or DFF1 Select	reg<1134>	0: LUT2_1 1: DFF1
DFF1 Initial Polarity Select	reg<1145>	0: Low 1: High
DFF1 Output Select	reg<1146>	0: Q output 1: nQ output
DFF1 or Latch Select	reg<1147>	0: DFF function 1: Latch function

Table 43. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_2 or DFF2 Select	reg<1133>	0: LUT2_2 1: DFF2
DFF2 Initial Polarity Select	reg<1157>	0: Low 1: High
DFF2 Output Select	reg<1158>	0: Q output 1: nQ output
DFF2 or Latch Select	reg<1159>	0: DFF function 1: Latch function

9.2 Initial Polarity Operations

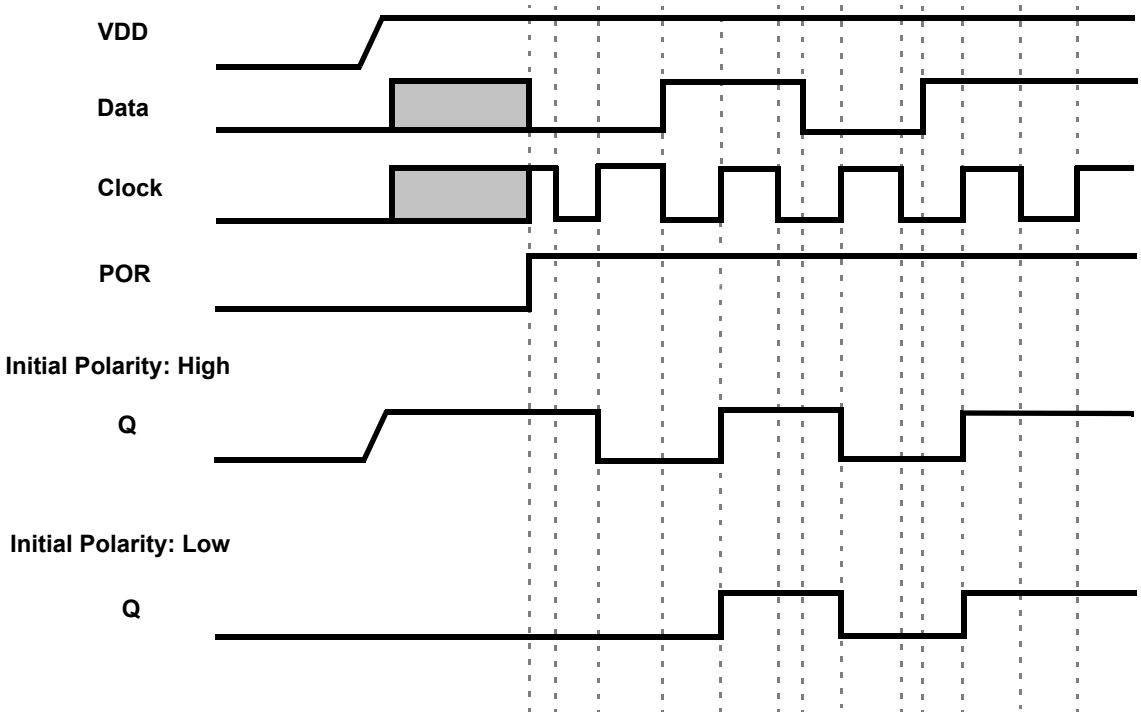


Figure 11. DFF Polarity Operations

9.3 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are six macrocells that can serve as either 3-bit LUTs or as D Flip Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

DFF3 has a user selectable option to allow the macrocell output to either come from the Q/nQ output of one D Flip Flop, or two D Flip Flops in series, with the first D Flip Flop triggering on the rising clock edge, and the second D Flip Flop triggering on the falling clock edge.

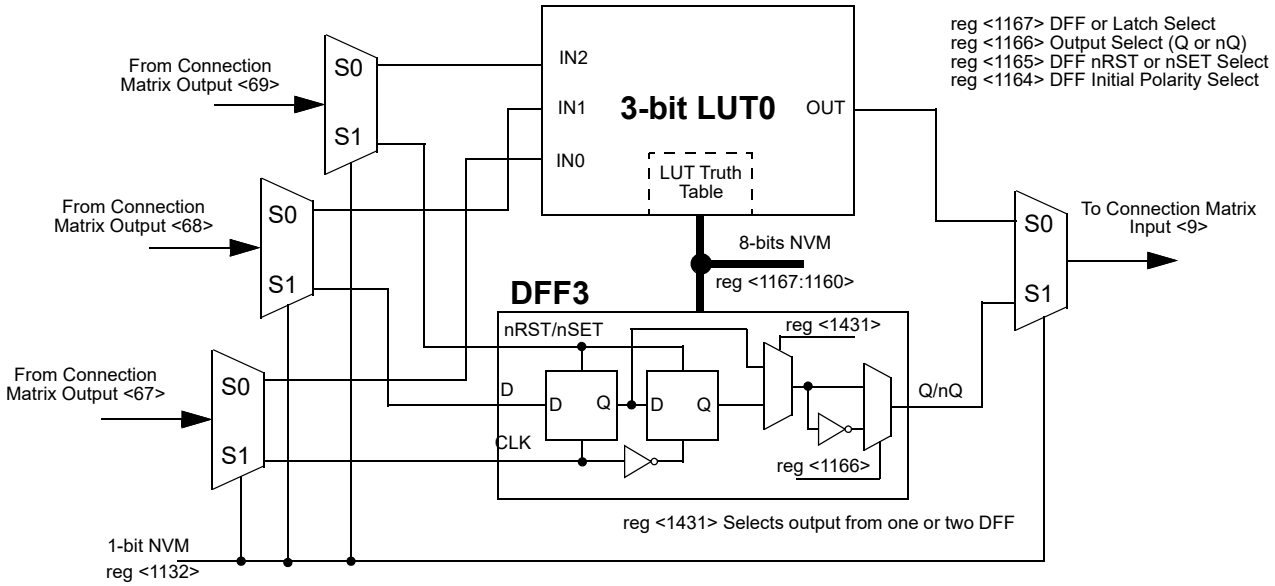


Figure 12. 3-bit LUT0 or DFF3

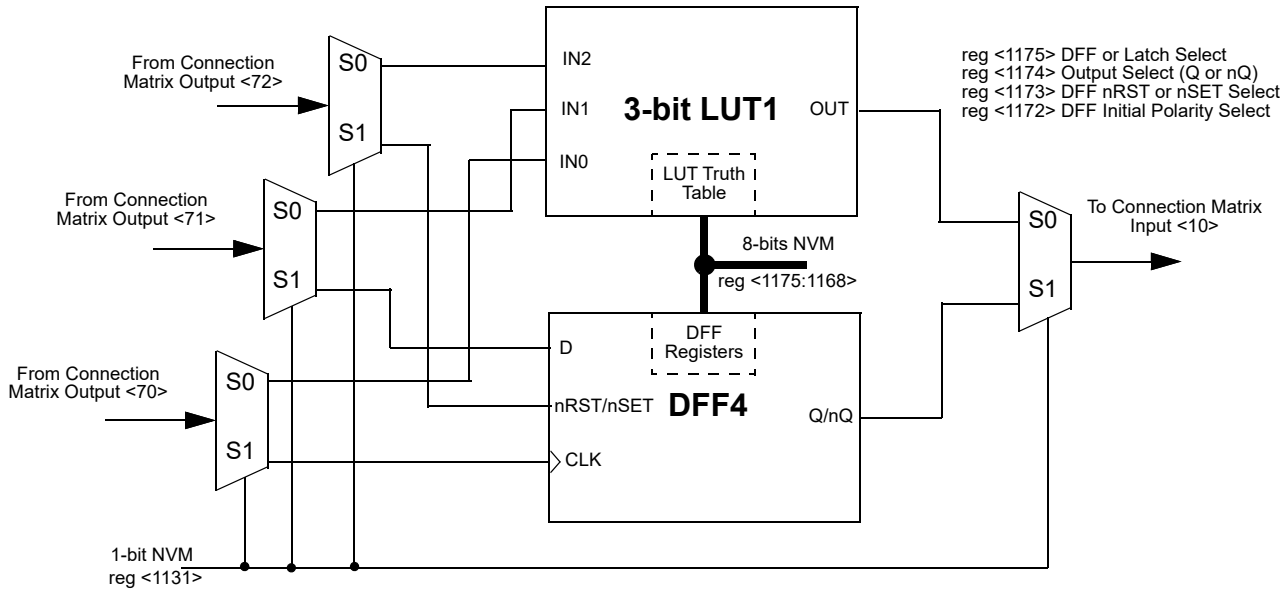


Figure 13. 3-bit LUT1 or DFF4

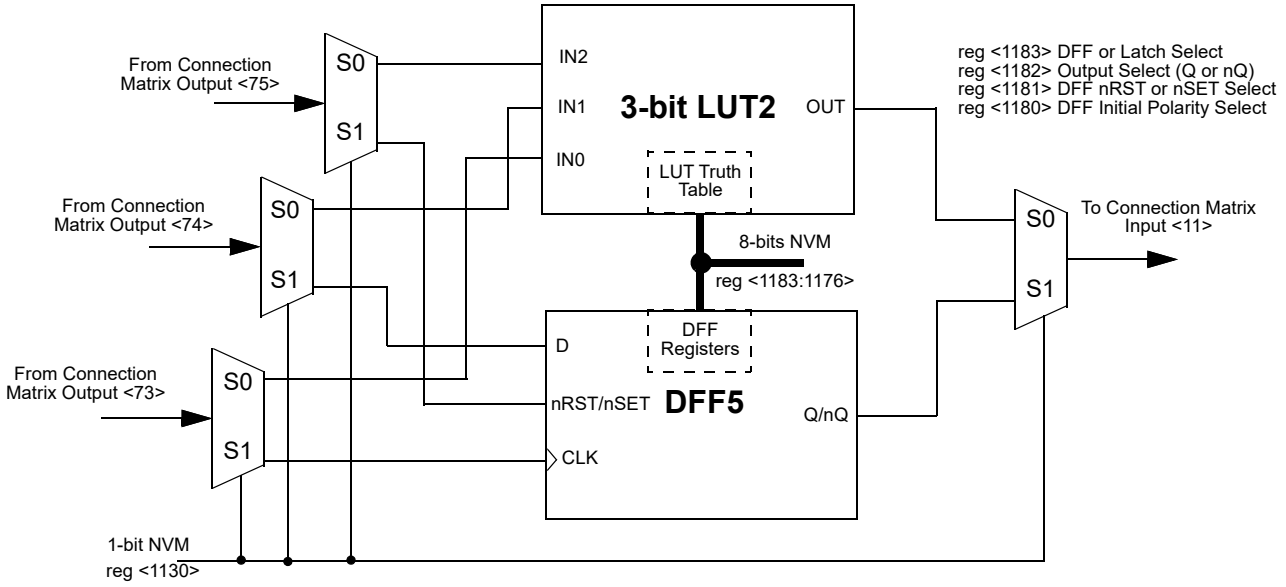


Figure 14. 3-bit LUT2 or DFF5

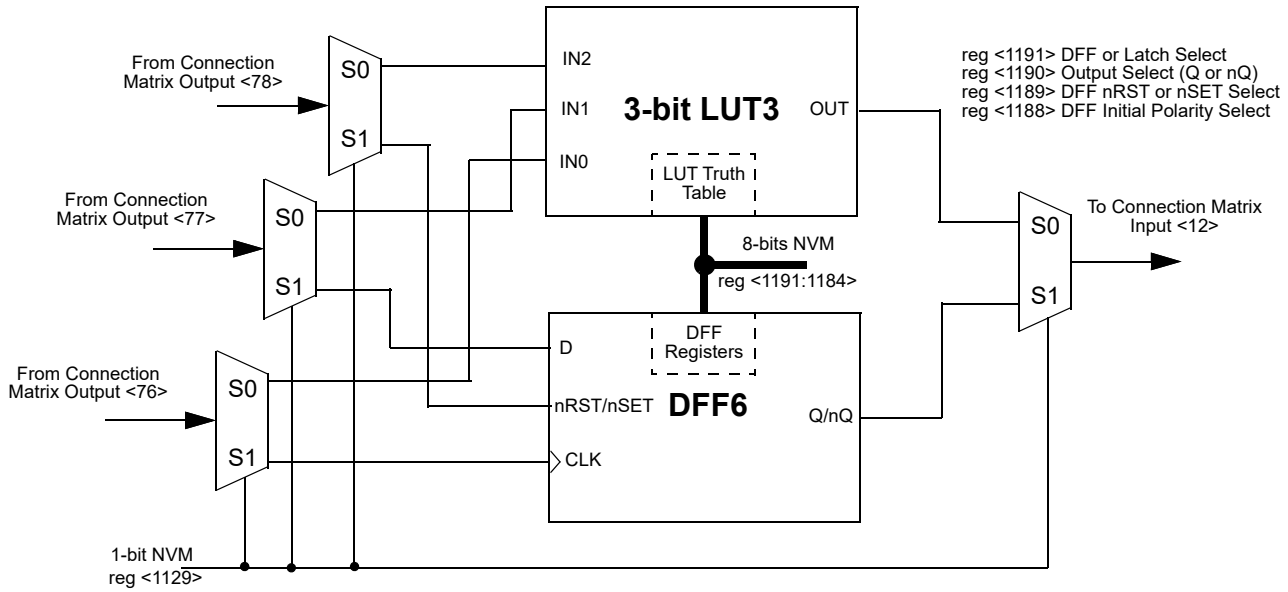


Figure 15. 3-bit LUT3 or DFF6

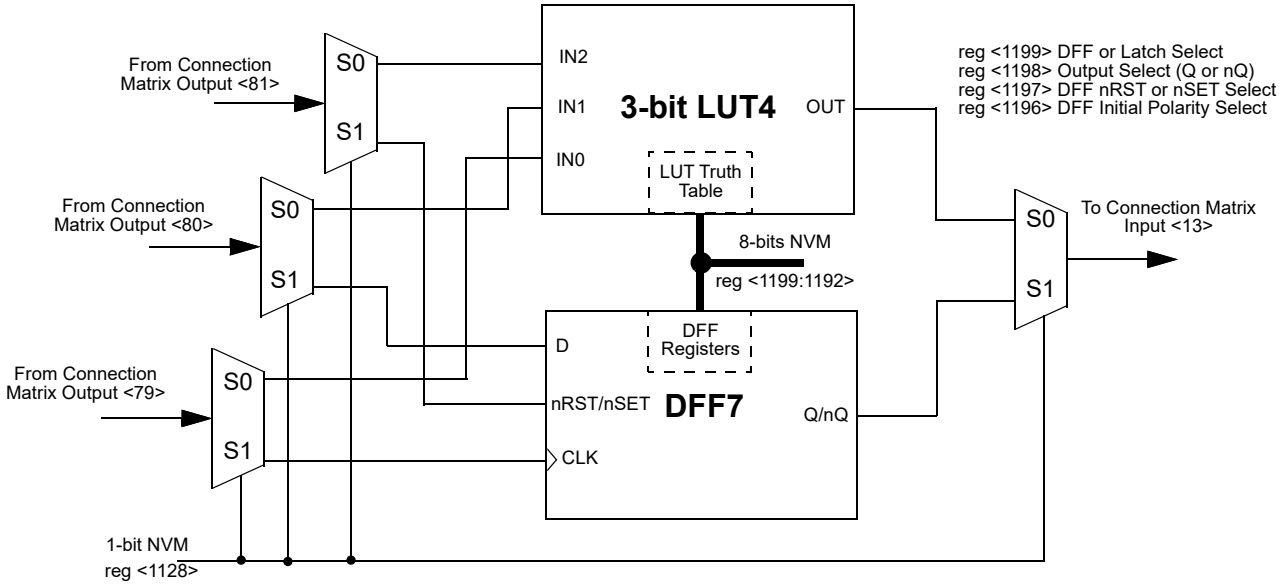


Figure 16. 3-bit LUT4 or DFF7

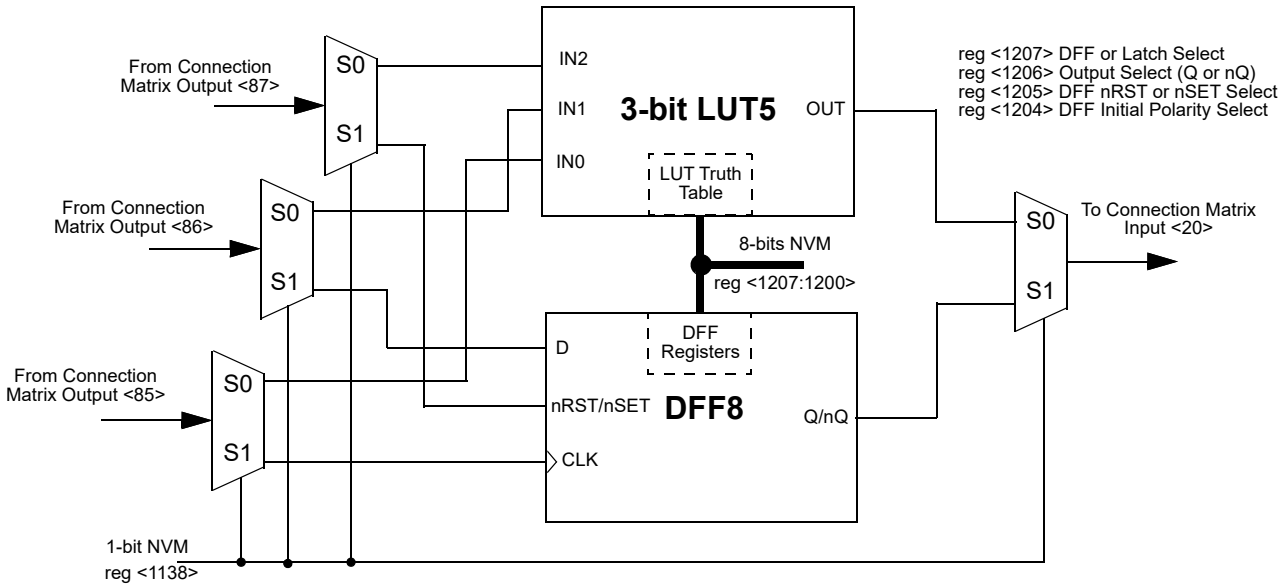


Figure 17. 3-bit LUT5 or DFF8

9.3.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 44. 3-bit LUT0 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1160>	LSB
0	0	1	reg <1161>	
0	1	0	reg <1162>	
0	1	1	reg <1163>	
1	0	0	reg <1164>	
1	0	1	reg <1165>	
1	1	0	reg <1166>	
1	1	1	reg <1167>	MSB

Table 45. 3-bit LUT1 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1168>	LSB
0	0	1	reg <1169>	
0	1	0	reg <1170>	
0	1	1	reg <1171>	
1	0	0	reg <1172>	
1	0	1	reg <1173>	
1	1	0	reg <1174>	
1	1	1	reg <1175>	MSB

Table 46. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1176>	LSB
0	0	1	reg <1177>	
0	1	0	reg <1178>	
0	1	1	reg <1179>	
1	0	0	reg <1180>	
1	0	1	reg <1181>	
1	1	0	reg <1182>	
1	1	1	reg <1183>	MSB

Table 47. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1184>	LSB
0	0	1	reg <1185>	
0	1	0	reg <1186>	
0	1	1	reg <1187>	
1	0	0	reg <1188>	
1	0	1	reg <1189>	
1	1	0	reg <1190>	
1	1	1	reg <1191>	MSB

Table 48. 3-bit LUT4 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1192>	LSB
0	0	1	reg <1193>	
0	1	0	reg <1194>	
0	1	1	reg <1195>	
1	0	0	reg <1196>	
1	0	1	reg <1197>	
1	1	0	reg <1198>	
1	1	1	reg <1199>	MSB

Table 49. 3-bit LUT5 Truth Table.

IN2	IN1	IN0	OUT	
0	0	0	reg <1200>	LSB
0	0	1	reg <1201>	
0	1	0	reg <1202>	
0	1	1	reg <1203>	
1	0	0	reg <1204>	
1	0	1	reg <1205>	
1	1	0	reg <1206>	
1	1	1	reg <1207>	MSB

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT0 is defined by reg<1167:1160>

3-Bit LUT1 is defined by reg<1175:1168>

3-Bit LUT2 is defined by reg<1183:1176>

3-Bit LUT3 is defined by reg<1191:1184>

3-Bit LUT4 is defined by reg<1199:1192>

3-Bit LUT5 is defined by reg<1207:1200>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 50. 3-bit LUT Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

9.3.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 51. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_0 or DFF3 Select	reg<1132>	0: LUT3_0 1: DFF3
DFF3 Initial Polarity Select	reg<1164>	0: Low 1: High
DFF3 nRST/nSET Select	reg<1165>	0: nRST from matrix out 1: nSET from matrix out
DFF3 Output Select	reg<1166>	0: Q output 1: nQ output
DFF3 or Latch Select	reg<1167>	0: DFF function 1: Latch function

Table 52. DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_1 or DFF4 Select	reg<1131>	0: LUT3_1 1: DFF4
DFF4 Initial Polarity Select	reg<1172>	0: Low 1: High
DFF4 nRST/nSET Select	reg<1173>	0: nRST from matrix out 1: nSET from matrix out
DFF4 Output Select	reg<1174>	0: Q output 1: nQ output
DFF4 or Latch Select	reg<1175>	0: DFF function 1: Latch function

Table 53. DFF5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_2 or DFF5 Select	reg<1130>	0: LUT3_2 1: DFF5
DFF5 Initial Polarity Select	reg<1180>	0: Low 1: High
DFF5 nRST/nSET Select	reg<1181>	0: nRST from matrix out 1: nSET from matrix out
DFF5 Output Select	reg<1182>	0: Q output 1: nQ output
DFF5 or Latch Select	reg<1183>	0: DFF function 1: Latch function

Table 54. DFF6 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_3 or DFF6 Select	reg<1129>	0: LUT3_3 1: DFF6
DFF6 Initial Polarity Select	reg<1188>	0: Low 1: High
DFF6 nRST/nSET Select	reg<1189>	0: nRST from matrix out 1: nSET from matrix out
DFF6 Output Select	reg<1190>	0: Q output 1: nQ output
DFF6 or Latch Select	reg<1191>	0: DFF function 1: Latch function

Table 55. DFF7 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_4 or DFF7 Select	reg<1128>	0: LUT3_4 1: DFF7
DFF7 Initial Polarity Select	reg<1196>	0: Low 1: High
DFF7 nRST/nSET Select	reg<1197>	0: nRST from matrix out 1: nSET from matrix out
DFF7 Output Select	reg<1198>	0: Q output 1: nQ output
DFF7 or Latch Select	reg<1199>	0: DFF function 1: Latch function

Table 56. DFF8 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_5 or DFF8 Select	reg<1138>	0: LUT3_5 1: DFF8
DFF8 Initial Polarity Select	reg<1204>	0: Low 1: High
DFF8 nRST/nSET Select	reg<1205>	0: nRST from matrix out 1: nSET from matrix out
DFF8 Output Select	reg<1206>	0: Q output 1: nQ output
DFF8 or Latch Select	reg<1207>	0: DFF function 1: Latch function

9.4 Initial Polarity Operations

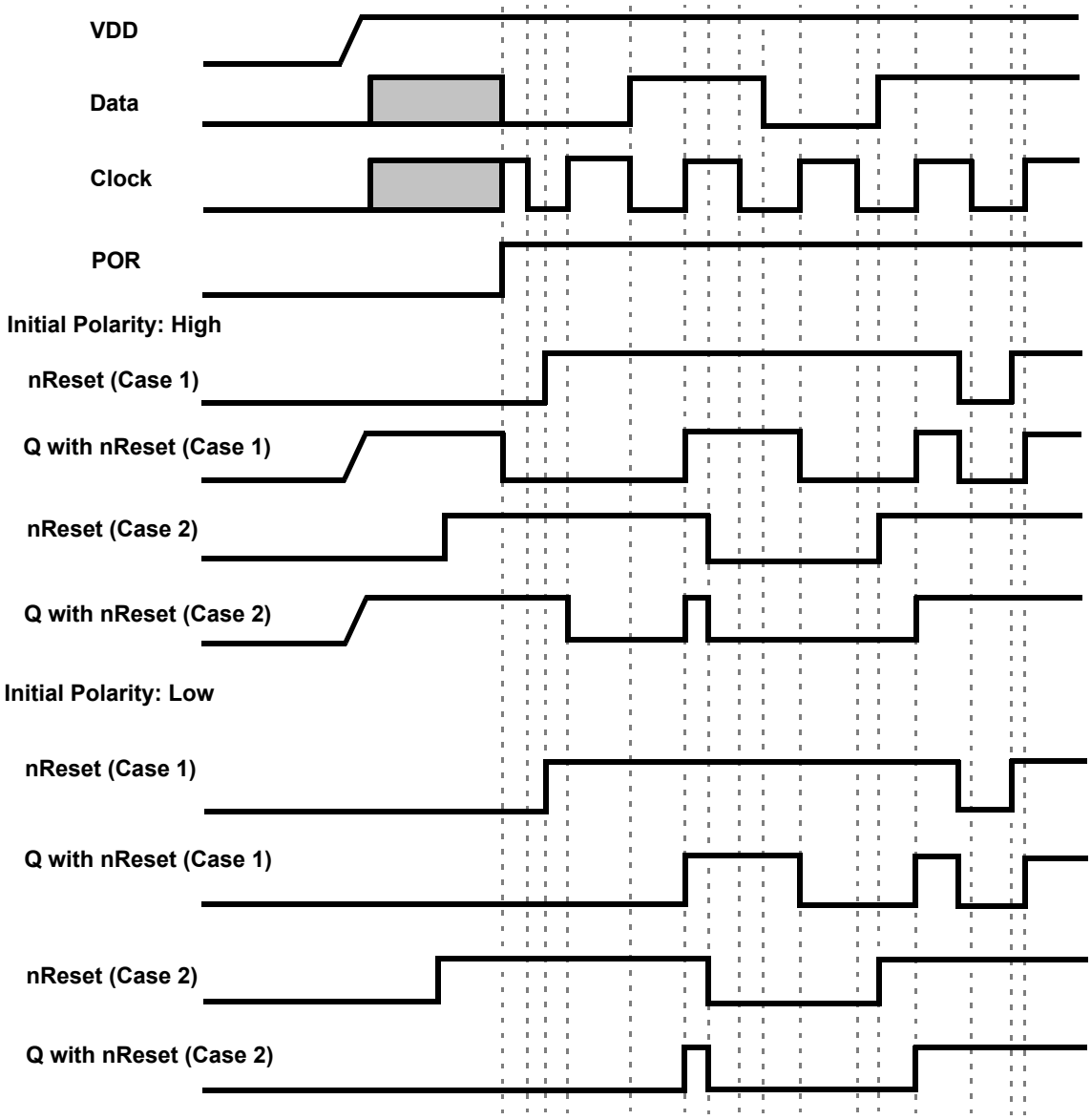


Figure 18. DFF Polarity Operations with nReset

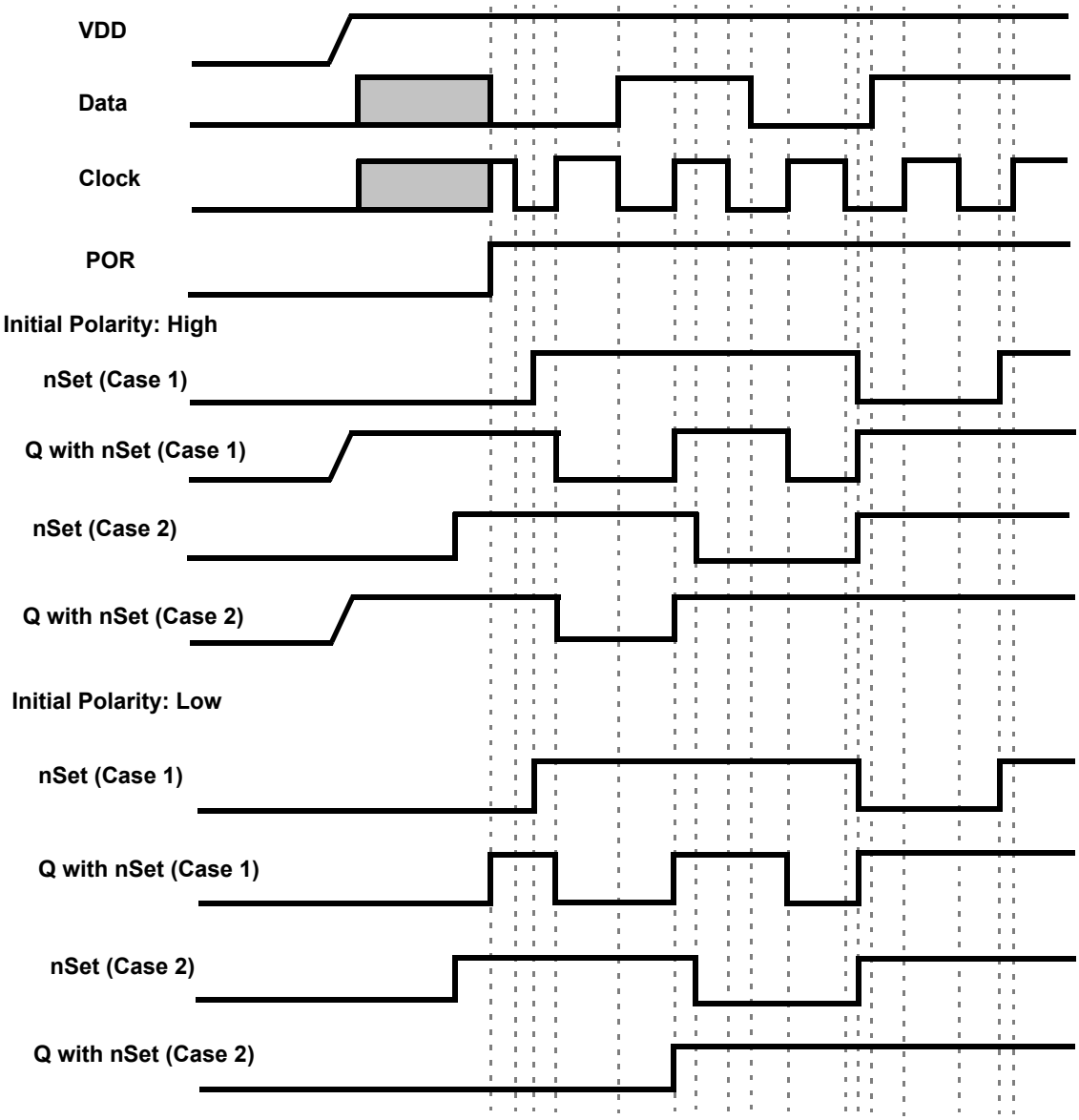


Figure 19. DFF Polarity Operations with nSet

9.5 3-Bit LUT or Pipe Delay / Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay / Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 16-input MUX that is controlled by reg <1227:1224> for OUT0 and reg <1231:1228> for OUT1. The 16-input MUX is used to select the amount of delay.

The overall time of the delay is based on the clock used in the SLG46580/82/83 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46580/82/83). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by reg <1239>)

In the Ripple Counter mode there are 3 options for setting, which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

We can select one of the functionality modes by the register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV->EV->EV-1….SV+1->SV etc. (if SV is smaller than EV) or SV->SV-1….EV+1->EV->SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV etc.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0 etc.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV etc. Please see Ripple counter functionality example in *Figure 21.* .

Every step is executed by the rising edge on CLK input.

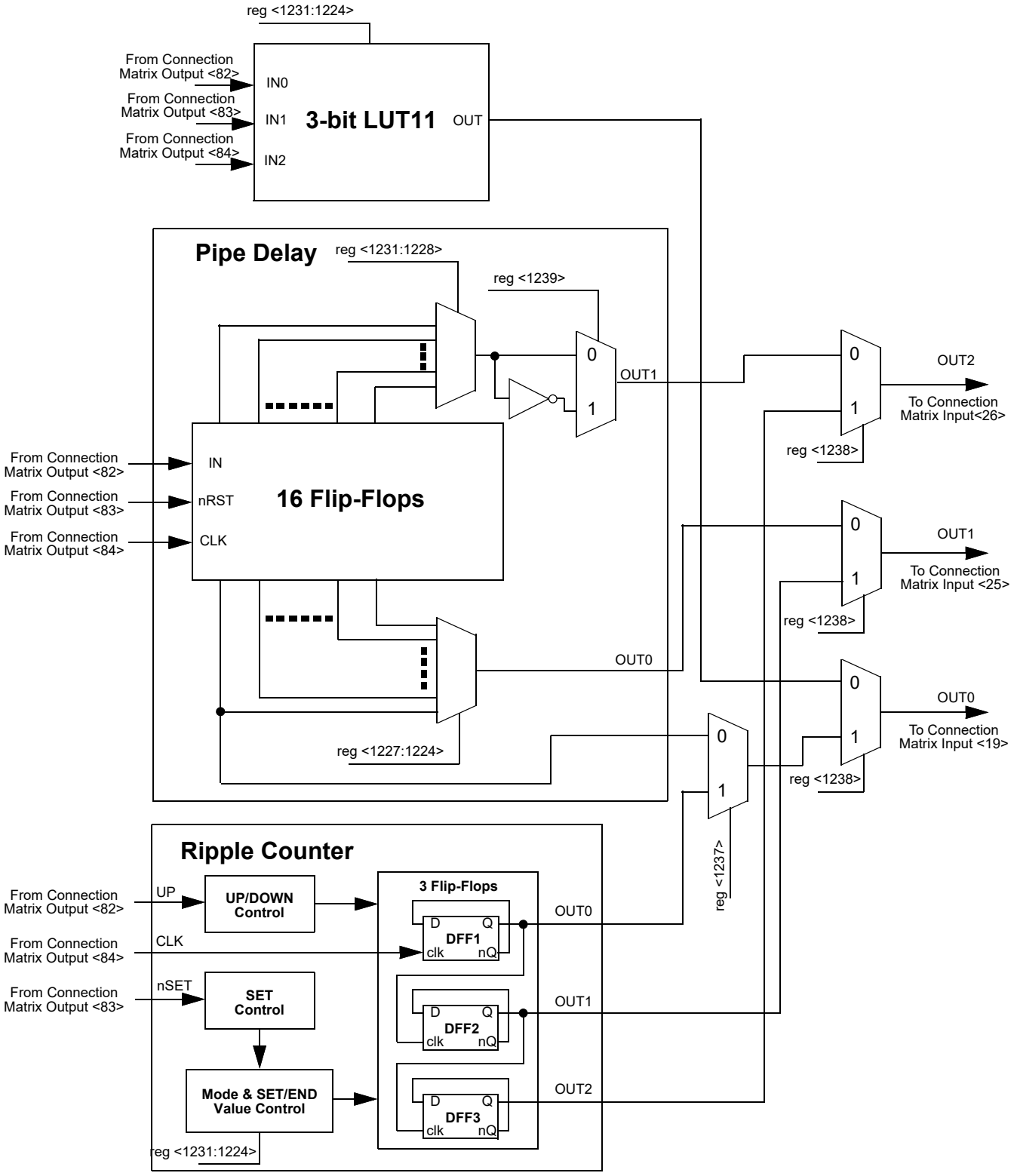


Figure 20. 3-bit LUT11 / Pipe Delay / Ripple Counter

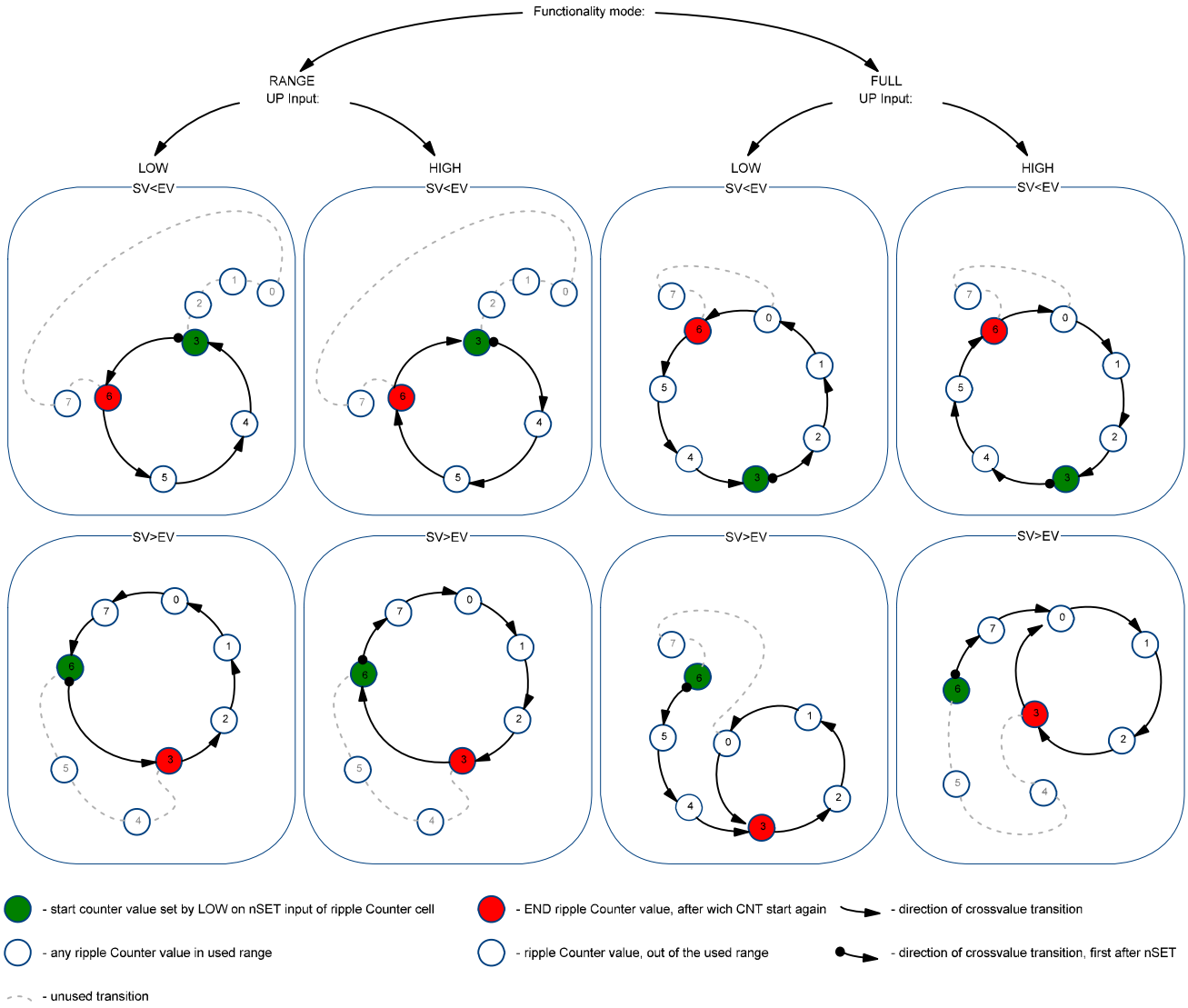


Figure 21. Example: Ripple Counter Functionality

9.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 57. 3-bit LUT11 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1224>
0	0	1	reg <1225>
0	1	0	reg <1226>
0	1	1	reg <1227>
1	0	0	reg <1228>
1	0	1	reg <1229>
1	1	0	reg <1230>
1	1	1	reg <1231>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT11 is defined by reg<1231:1224>

9.5.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 58. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
OUT0 select	reg<1227:1224>	
OUT1 select	reg<1231:1228>	
Pipe Delay or Ripple Counter select	reg<1237>	0: Pipe Delay 1: Ripple Counter
LUT3_11 or Pipe Delay Output select	reg<1238>	0: LUT3_11 1: Pipe Delay/Ripple Counter by reg <1237>
Pipe delay OUT1 Polarity Select Bit	reg<1239>	0: Non-inverted 1: Inverted

9.6 3-Bit LUT or 8- Bit Counter / Delay Macrocells

There are five macrocells that can serve as either 3-bit LUTs or as Counter / Delays. When used to implement LUT function, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delay function, two of the three input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_In/CNT_Reset) for the counter/delay, with the output going back to the connection matrix.

These macrocells can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

These macrocells can also operate in a frequency detection or edge detection mode.

Two of the five macrocells can have their active count value read via I^2C (CNT2 and CNT4). See Section *21.4.7.3 Reading Counter Data via I2C* for further details

9.6.1 3-Bit LUT or 8- Bit CNT/DLY Block Diagrams

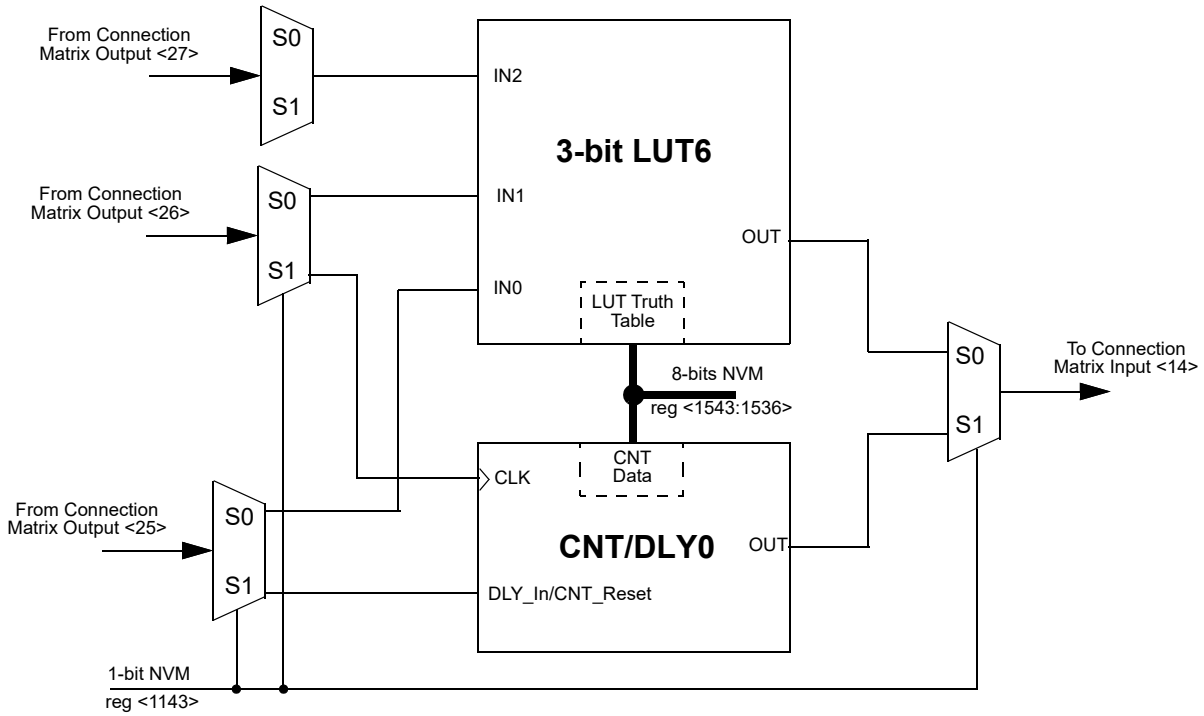


Figure 22. 3-bit LUT6 or CNT/DLY0

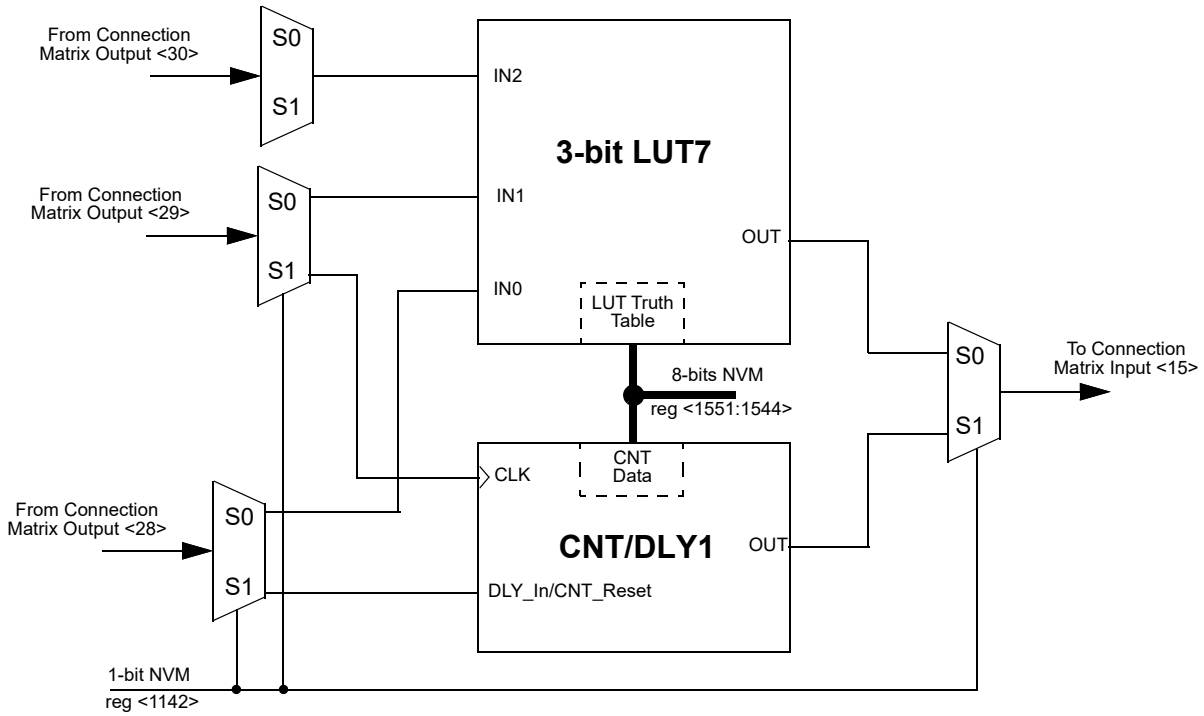


Figure 23. 3-bit LUT7 or CNT/DLY1

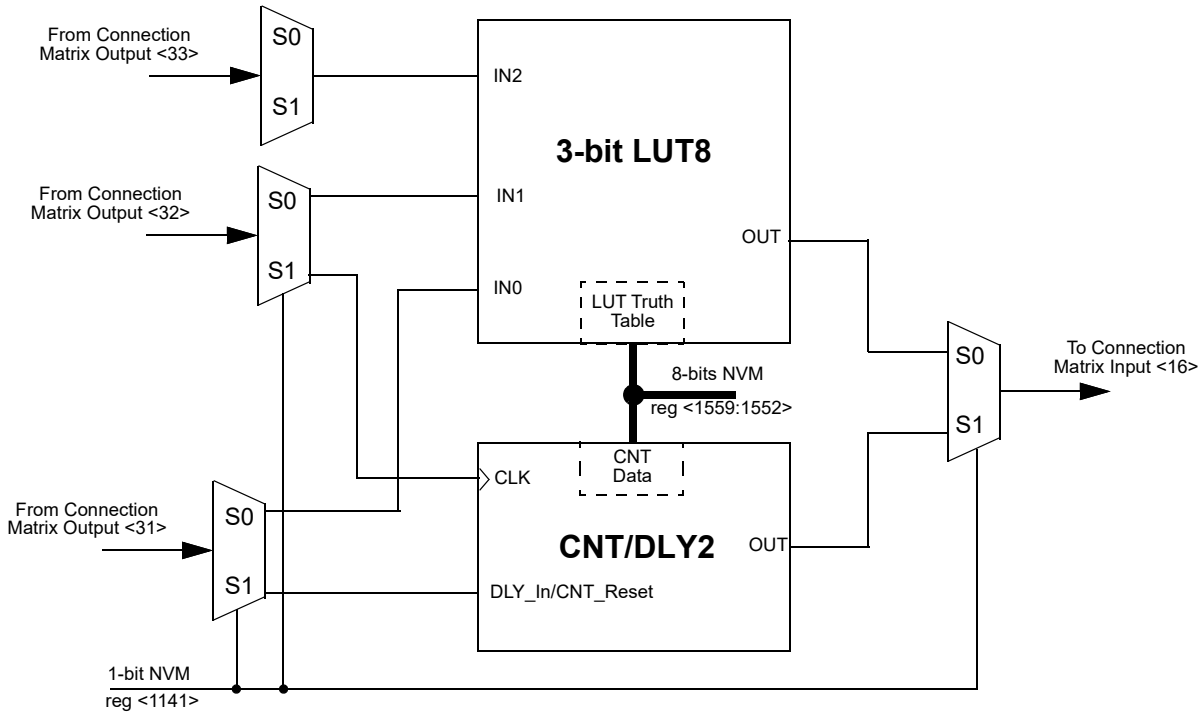


Figure 24. 3-bit LUT8 or CNT/DLY2

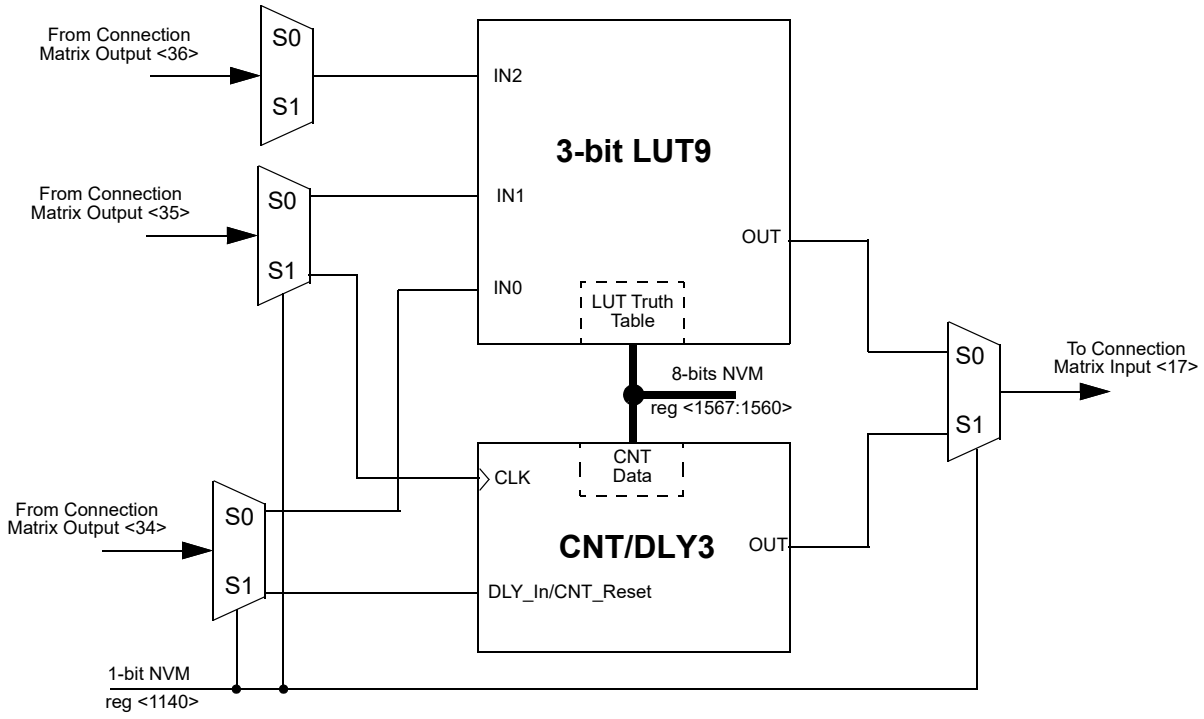


Figure 25. 3-bit LUT9 or CNT/DLY3

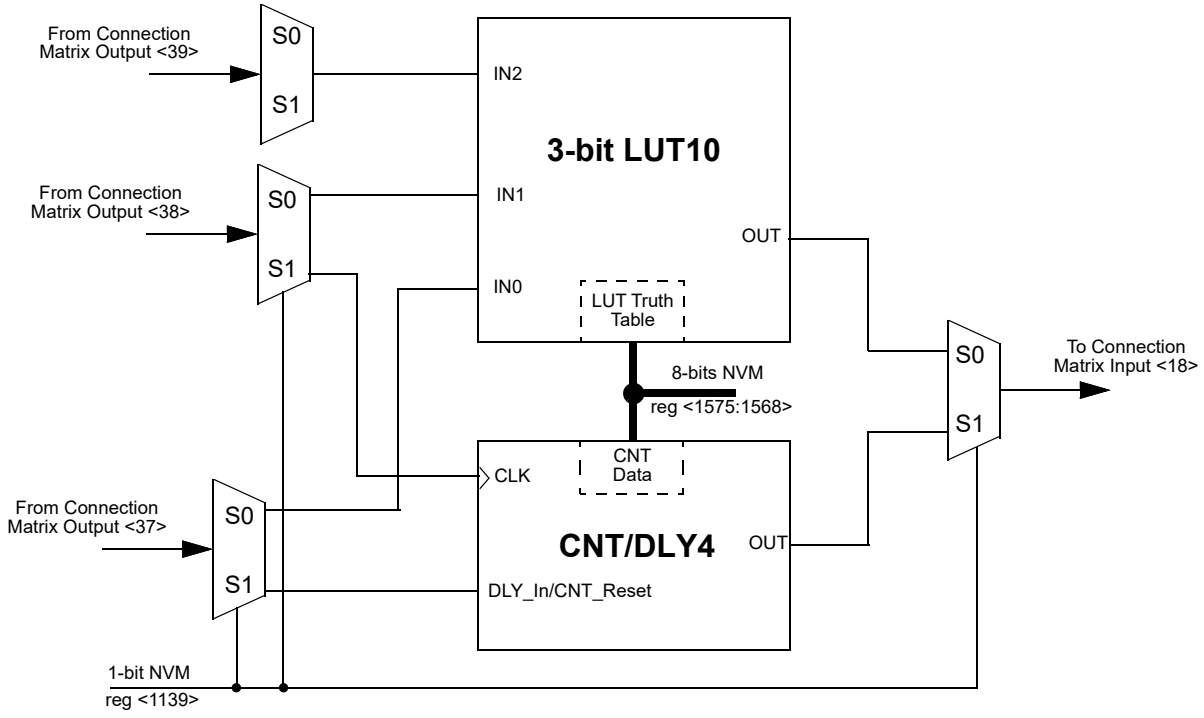


Figure 26. 3-bit LUT10 or CNT/DLY4

9.6.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 59. 3-bit LUT6 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1536>
0	0	1	reg <1537>
0	1	0	reg <1538>
0	1	1	reg <1539>
1	0	0	reg <1540>
1	0	1	reg <1541>
1	1	0	reg <1542>
1	1	1	reg <1543>

Table 60. 3-bit LUT7 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1544>
0	0	1	reg <1545>
0	1	0	reg <1546>
0	1	1	reg <1547>
1	0	0	reg <1548>
1	0	1	reg <1549>
1	1	0	reg <1550>
1	1	1	reg <1551>

Table 61. 3-bit LUT8 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1552>
0	0	1	reg <1553>
0	1	0	reg <1554>
0	1	1	reg <1555>
1	0	0	reg <1556>
1	0	1	reg <1557>
1	1	0	reg <1558>
1	1	1	reg <1559>

Table 62. 3-bit LUT9 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1560>
0	0	1	reg <1561>
0	1	0	reg <1562>
0	1	1	reg <1563>
1	0	0	reg <1564>
1	0	1	reg <1565>
1	1	0	reg <1566>
1	1	1	reg <1567>

Table 63. 3-bit LUT10 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <1568>
0	0	1	reg <1569>
0	1	0	reg <1570>
0	1	1	reg <1571>
1	0	0	reg <1572>
1	0	1	reg <1573>
1	1	0	reg <1574>
1	1	1	reg <1575>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT6 is defined by reg<1543:1536>

3-Bit LUT7 is defined by reg<1551:1544>

3-Bit LUT8 is defined by reg<1559:1552>

3-Bit LUT9 is defined by reg<1567:1560>

3-Bit LUT10 is defined by reg<1575:1568>

9.6.3 3-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 64. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_6 or Counter0 Select	reg<1143>	0: LUT3_6 1: Counter0
Delay0 Mode Select or asynchronous counter reset	reg<1241:1240>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
Counter/delay0 Clock Source Select	reg<1244:1242>	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter4 Overflow
CNT0's Q are Set to data or Reset to 0s Selection (8 bits)	reg<1245>	0: Reset to 0s 1: Set to data (Reg<1543:1536>)
Counter/delay0 Mode Selection	reg<1247:1246>	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay0 Control Data	reg<1543:1536>	1 – 256 (delay time = (counter control data +1) /freq)

Table 65. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_7 or Counter1 Select	reg<1142>	0: LUT3_7 1: Counter1
Delay1 Mode Select or asynchronous counter reset	reg<1249:1248>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
Counter/delay1 Clock Source Select	reg<1252:1250>	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter0 Overflow
Counter/delay1 Output Selection for Counter mode	reg<1253>	0: Default Output 1: Edge Detector Output
Counter/delay1 Delayed Edge Output Selection	reg<1236>	0: Default Output from reg <1253> 1: Delayed Edge Detect
Counter/delay1 Mode Selection	reg<1255:1254>	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode

Table 65. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay1 Control Data	reg<1551:1544>	1 – 256 (delay time = (counter control data +1) /freq)

Table 66. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_8 or Counter2 Select	reg<1141>	0: LUT3_8 1: Counter2
Delay2 Mode Select or asynchronous counter reset	reg<1257:1256>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
Counter/delay2 Clock Source Select	reg<1260:1258>	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter1 Overflow
Counter/delay2 Output Selection for Counter mode	reg<1261>	0: Default Output 1: Edge Detector Output
Counter/delay2 Delayed Edge Output Selection	reg<1235>	0: Default Output from reg <1261> 1: Delayed Edge Detect
Counter/delay2 Mode Selection	reg<1263:1262>	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay2 Control Data	reg<1559:1552>	1 – 256 (delay time = (counter control data +1) /freq)

Table 67. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_9 or Counter3 Select	reg<1140>	0: LUT3_9 1: Counter3
Delay3 Mode Select or asynchronous counter reset	reg<1265:1264>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
Counter/delay3 Clock Source Select	reg<1268:1266>	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter2 Overflow

Table 67. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/delay3 Output Selection for Counter mode	reg<1269>	0: Default Output 1: Edge Detector Output
Counter/delay3 Delayed Edge Output Selection	reg<1234>	0: Default Output from reg <1269> 1: Delayed Edge Detect
Counter/delay3 Mode Selection	reg<1271:1270>	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay3 Control Data	reg<1567:1560>	1 – 256 (delay time = (counter control data +1) /freq)

Table 68. CNT/DLY4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_10 or Counter4 Select	reg<1139>	0: LUT3_10 1: Counter4
Delay4 Mode Select or asynchronous counter reset	reg<1273:1272>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
Counter/delay4 Clock Source Select	reg<1276:1274>	000: Internal OSC clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC 110: External Clock 111: Counter1 Overflow
Counter/delay4 Output Selection for Counter mode	reg<1277>	0: Default Output 1: Edge Detector Output
Counter/delay4 Delayed Edge Output Selection	reg<1233>	0: Default Output from reg <1277> 1: Delayed Edge Detect
Counter/delay4 Mode Selection	reg<1279:1278>	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode
Counter/delay4 Control Data	reg<1575:1568>	1 – 256 (delay time = (counter control data +1) /freq)

Table 69. DLY/CNT Polarity Select

Signal Function	Register Bit Address	Register Definition
Select the polarity of DLY/CNT0's output	reg<1287>	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT1's output	reg<1286>	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT2's output	reg<1285>	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT3's output	reg<1284>	0: Default Output 1: Inverted Output
Select the polarity of DLY/CNT4's output	reg<1283>	0: Default Output 1: Inverted Output

9.6.4 CNT/DLY Timing Diagrams

9.6.4.1 Delay mode

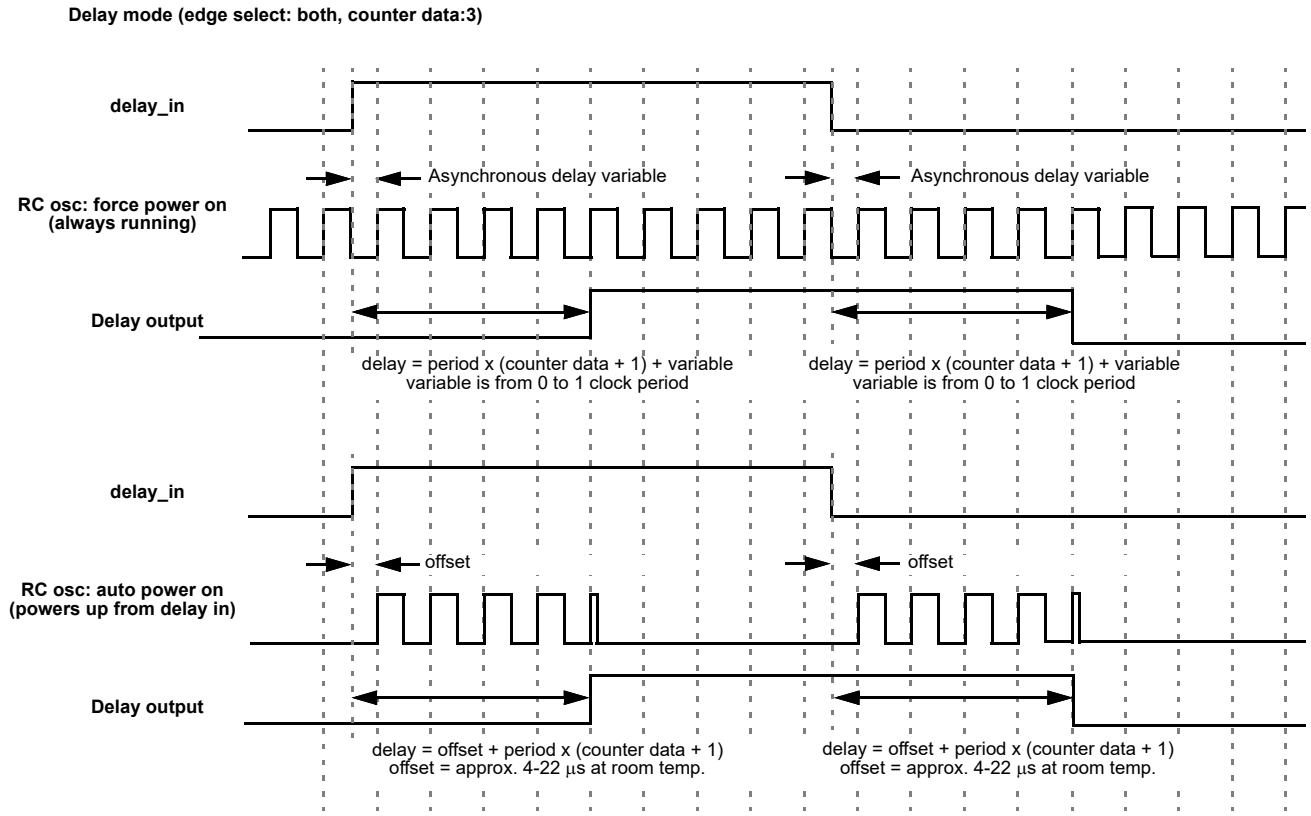


Figure 27. Delay Mode Timing Diagram

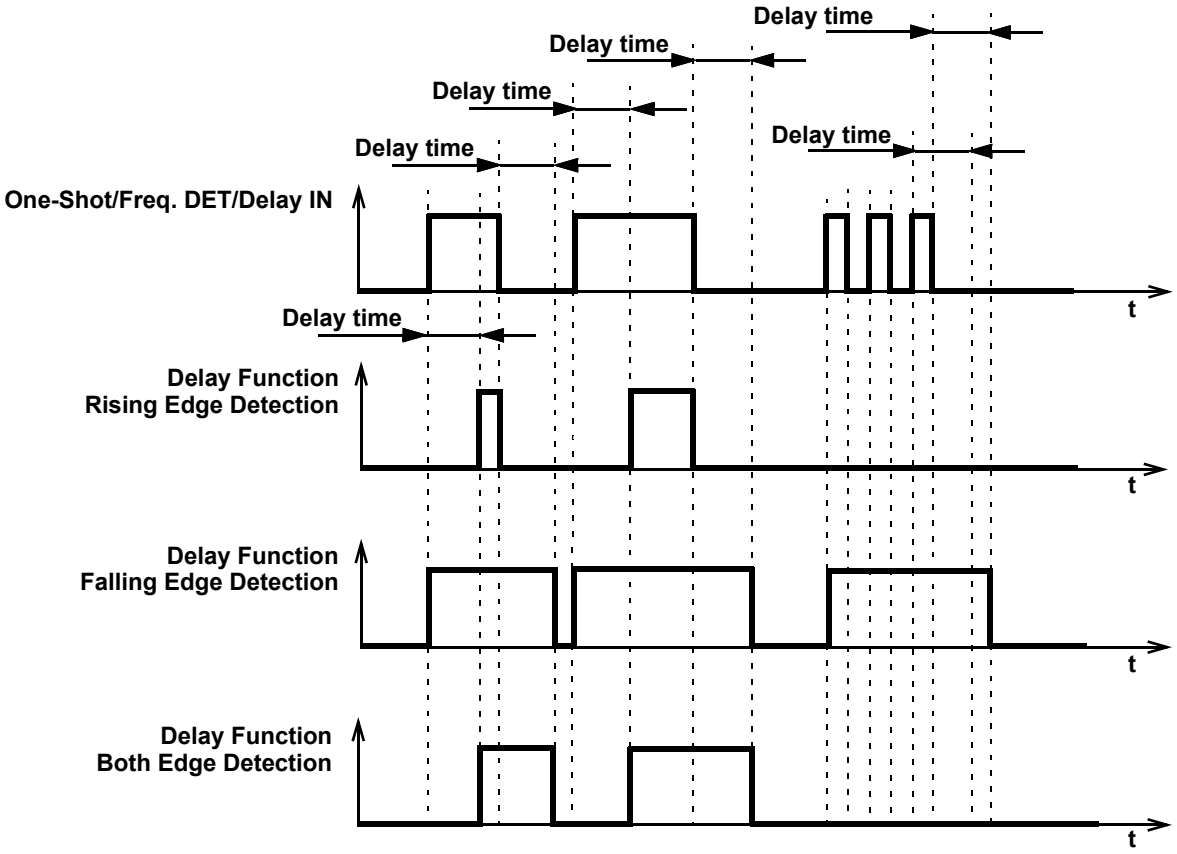


Figure 28. Delay Mode Timing Diagram for Different Edge Select Modes

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

9.6.4.2 Counter Mode

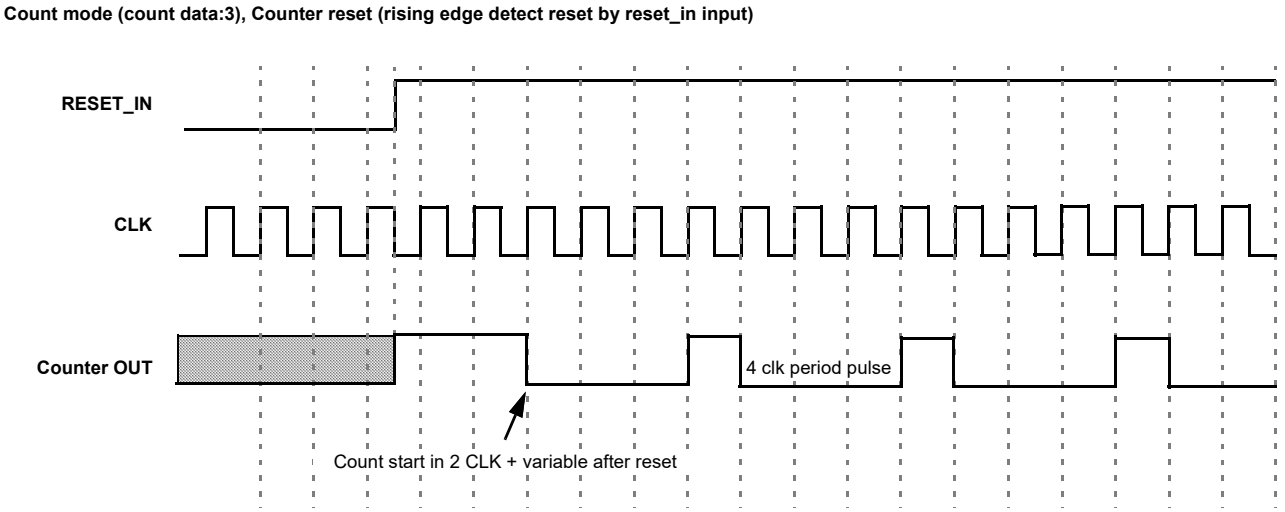


Figure 29. Counter Mode Timing with Reset Signal (only for DLY/CNT0)

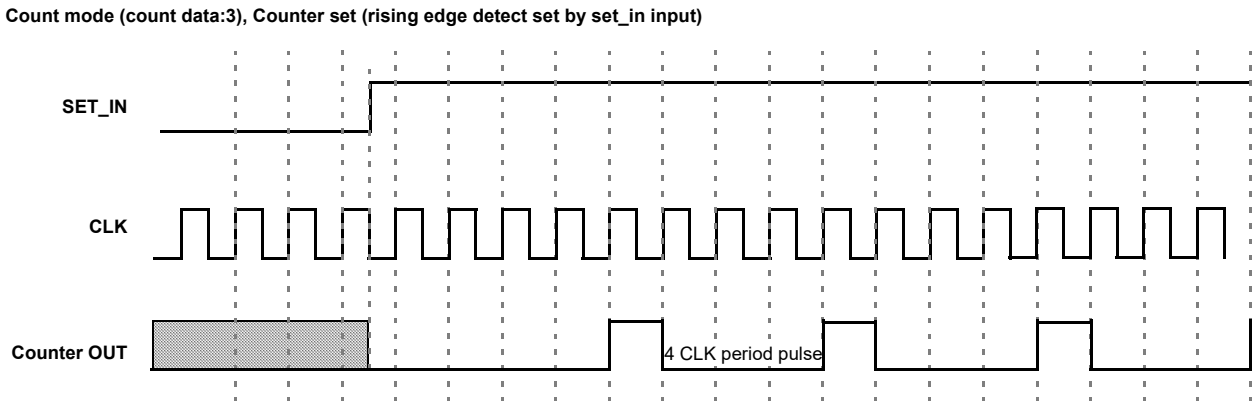


Figure 30. Counter Mode Timing with SET Signal (only for DLY/CNT0)

9.6.4.3 One-shot mode

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. There is also an option to ignore or detect selected edge during pulse is outputting. The following diagram is showing one-shot function for non-inverted output.

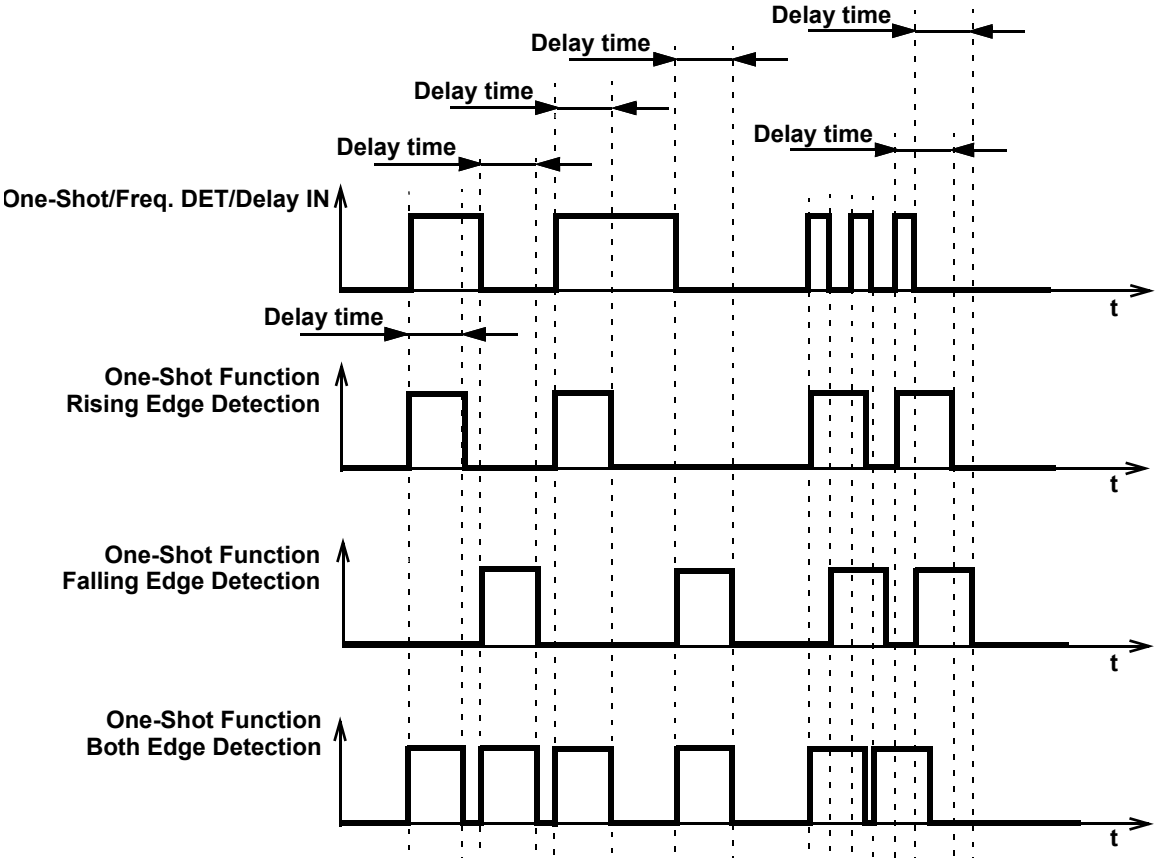


Figure 31. One-Shot Function Timing Diagram

This macrocell generates a high level pulse with a set width (defined by counter data and clock selection properties) when detecting the respective edge. It does not restart while pulse is high.

9.6.4.4 Frequency Detection Mode

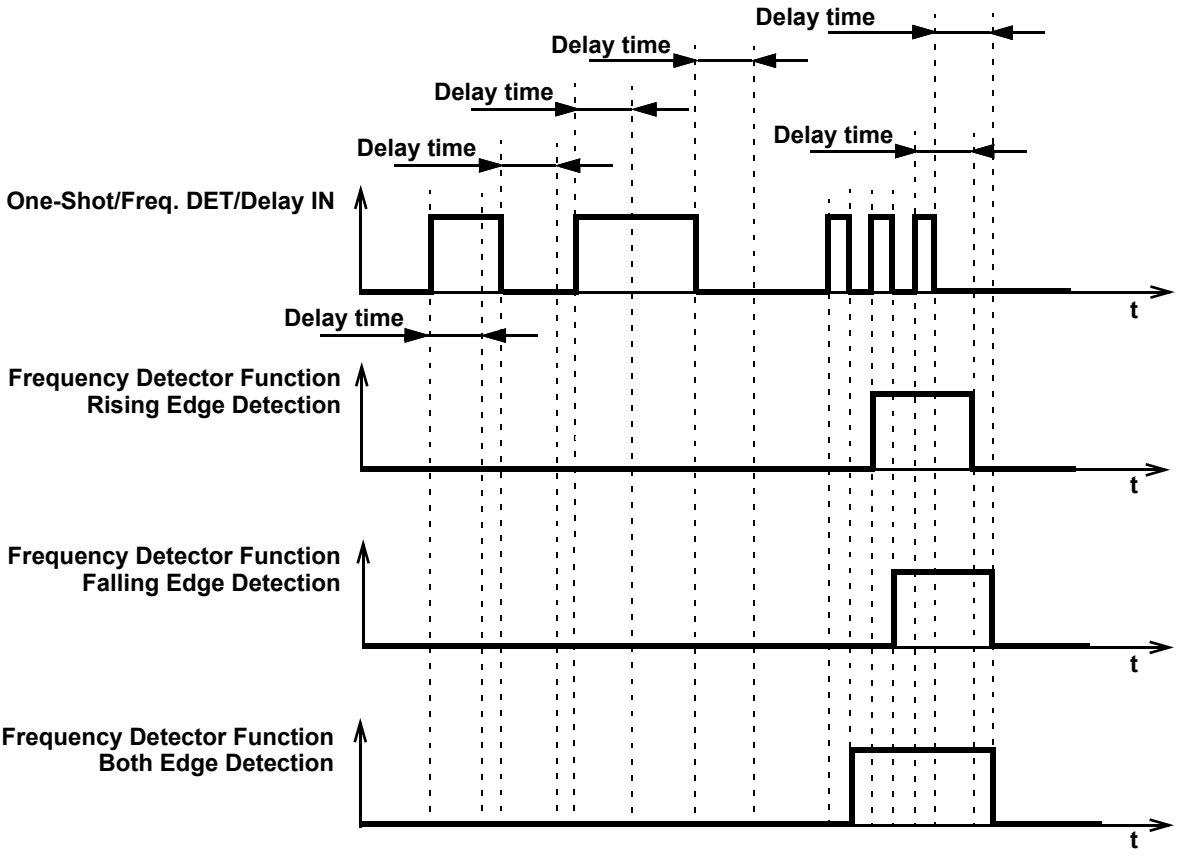


Figure 32. Frequency Detection Mode Timing Diagram

Rising Edge: The output goes high if the time between two successive rising edges is less than the set time. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two successive falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

9.6.4.5 Edge Detection Mode

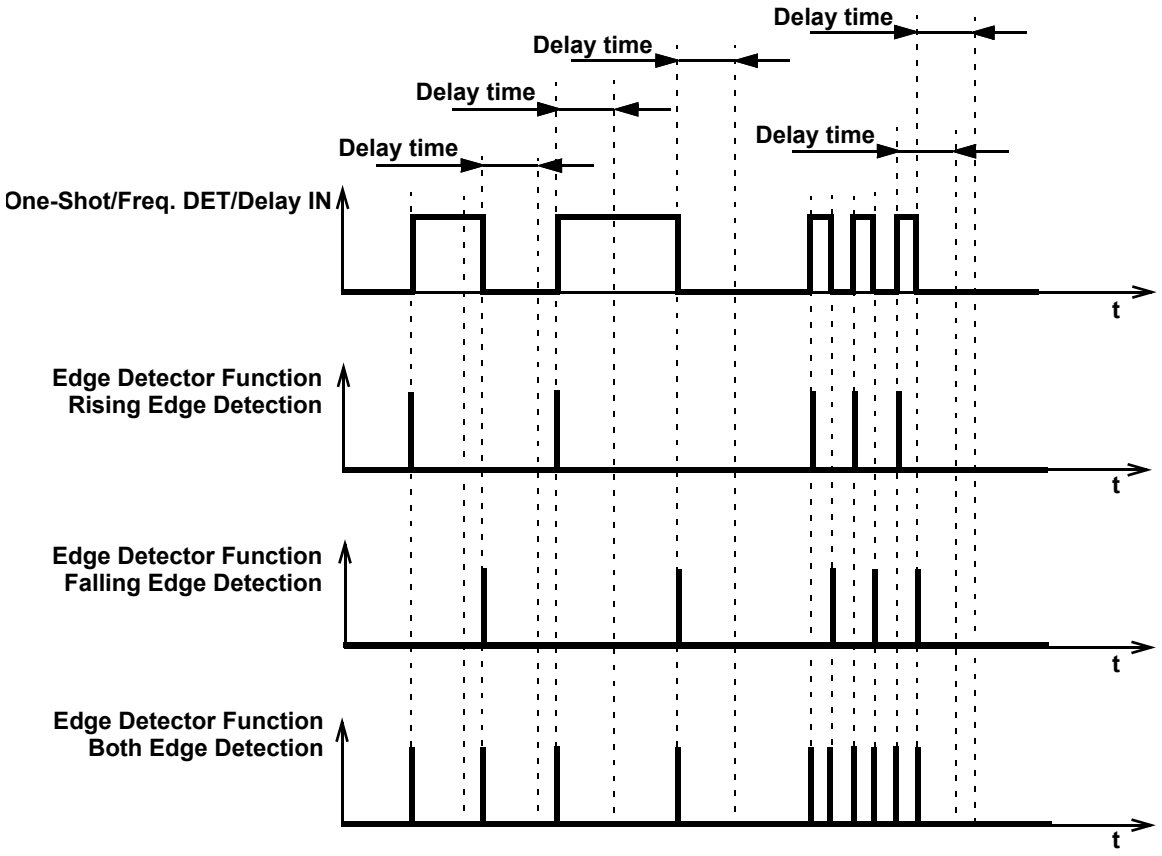


Figure 33. Edge Detection Mode Timing Diagram (except DLY/CNT0)

The macrocell generates high level short pulse when detecting the respective edge.

9.6.4.6 Delayed Edge Detection Mode

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See *Figure 34.* .

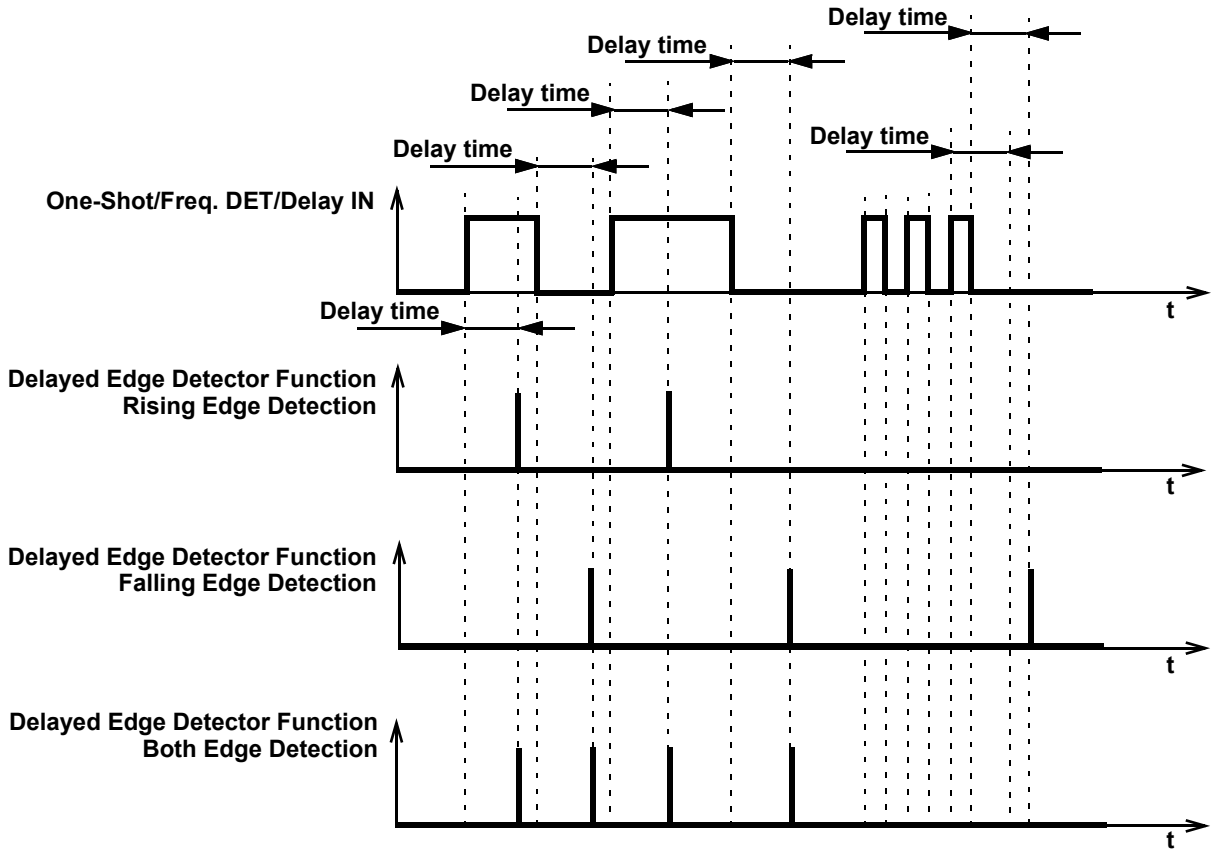


Figure 34. Delayed Edge Detection Mode Timing Diagram (Except DLY/CNT0)

9.7 Wake and Sleep controller (WS)

The SLG46580/82/83 has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose reg<1247:1246>=11 and reg<1447>=1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 8-bit counter.

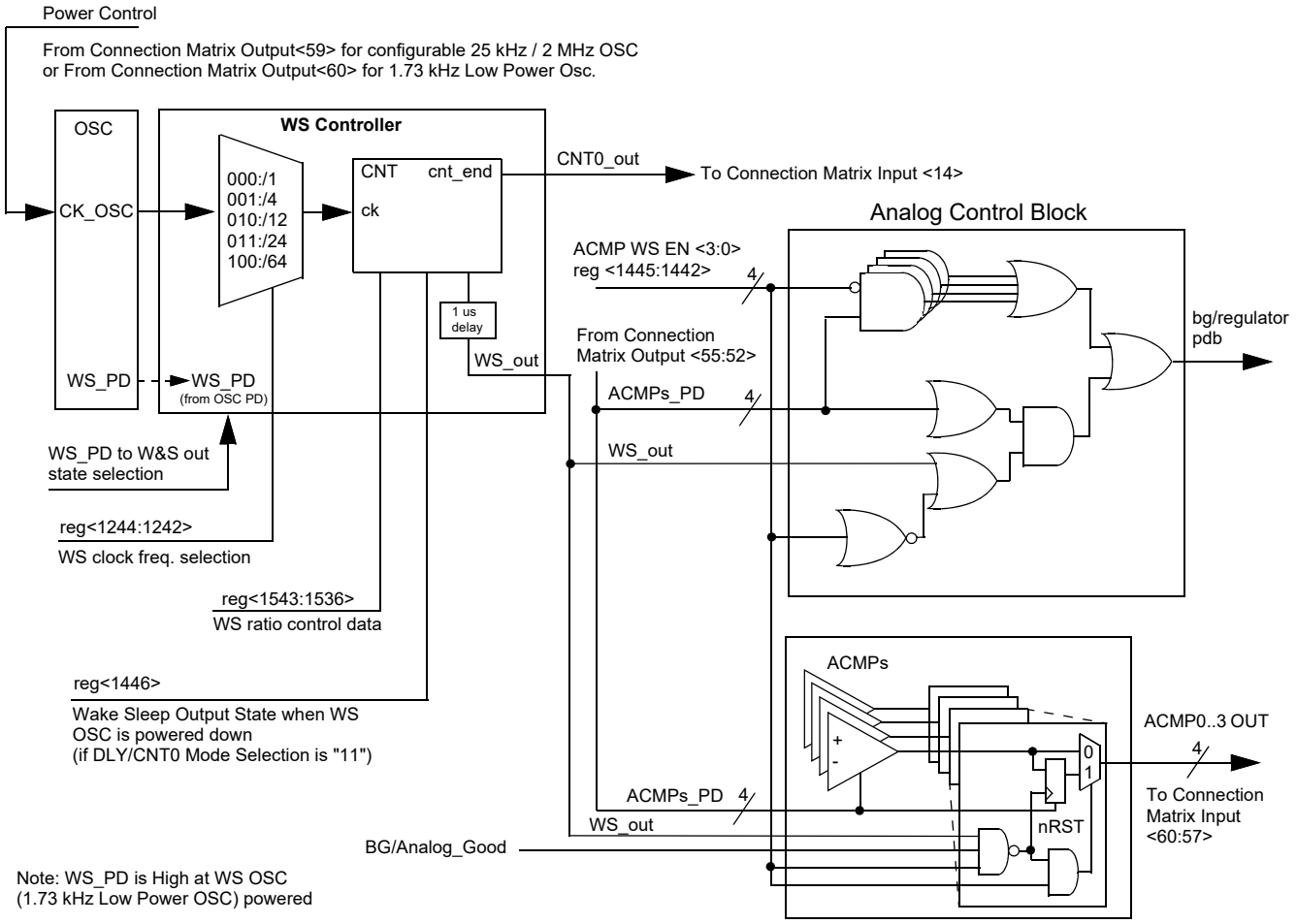
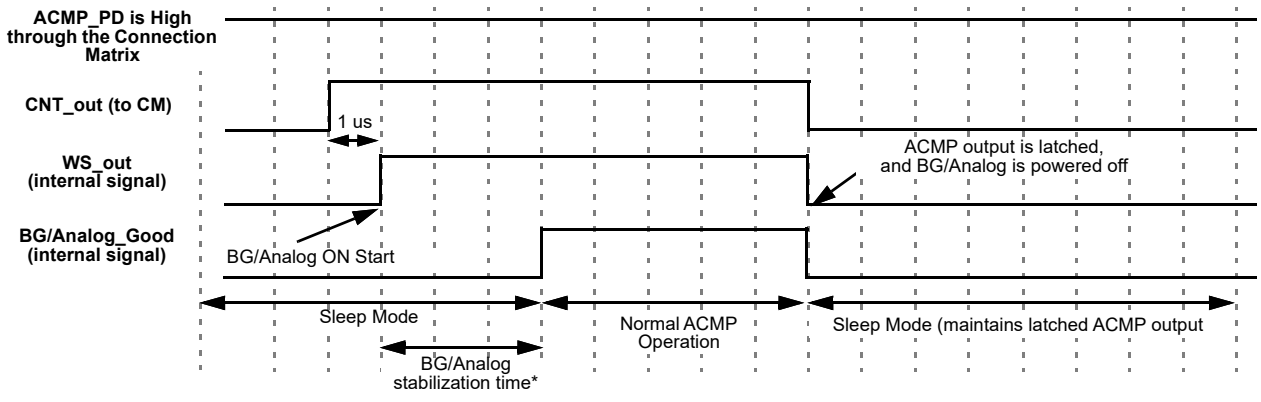


Figure 35. Wake/Sleep controller



Note: * Refer to Electrical Spec (ACMP Start Time)

Figure 36. Wake/Sleep Timing Diagram

To use any ACMP under WS controller the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately)
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS => enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs)

For the OSC, any oscillator with any pre-divider can be used. The user can select a period of time while the ACMPs are sleeping in a range of 1 - 255 clock cycles. Before they are sent to sleep their outputs are latched so the ACMPs remain their state (High or Low) while sleeping. When the WS signal is High, it takes a BG time (Refer to electrical spec) to turn the ACMPs on. The wake time must be longer than BG/Analog power on time.

Note: If 25 kHz / 2 MHz Oscillator is used for WS, the 1.73 kHz Low Power Osc must be set to Force Power On.

The WS controller has the following settings:

- Wake and Sleep Output State (High/Low)
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on
  If OSC is powered off (Power Down option is selected; power down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off
  Both cases WS function is turned off

- Counter Data (Range: 1 - 255)
  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time

- Q mode - defines the state of WS counter data when Set/Reset signal appears
  Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn the ACMPs on. When Reset signal goes out, the WS counter will go Low and turn the ACMPs off until the counter counts up to the end
  Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn the ACMPs off. When Set signal goes out, the WS counter will go on counting and High level signal will turn the ACMPs on while counter is counting up to the end

- Edge Select defines the edge for Q mode
  High level Set/Reset - switches mode Set/Reset when level is High
  Note: Q mode operates only in case of "High Level Set/Reset"

10.0 Combinatorial Logic

10.1 4-bit LUT with two outputs

There is one 4-bit LUT with two outputs. The device also includes fifteen Combination Function Macrocells that can be used as LUTs. For more details, please see Section *9.0 Combination Function Macrocells*.

Inputs/Outputs for the nine LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

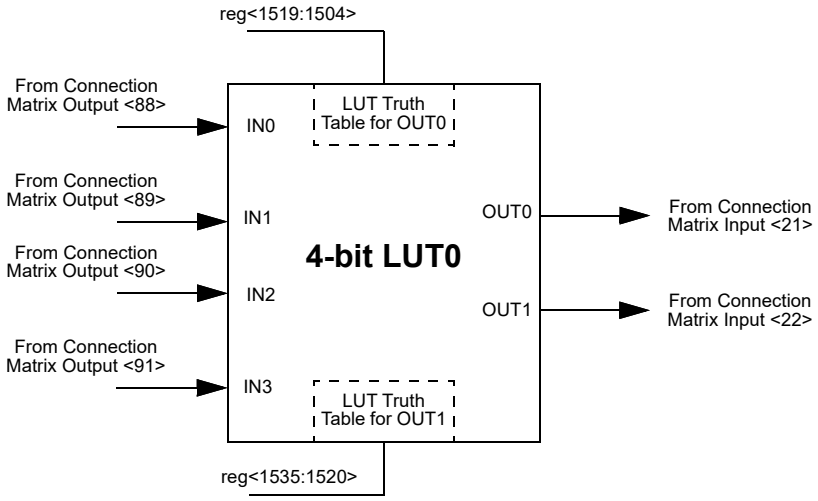


Figure 37. 4-bit LUT0 with two outputs

Table 70. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT0	OUT1	
0	0	0	0	reg <1504>	reg <1520>	LSB
0	0	0	1	reg <1505>	reg <1521>	
0	0	1	0	reg <1506>	reg <1522>	
0	0	1	1	reg <1507>	reg <1523>	
0	1	0	0	reg <1508>	reg <1524>	
0	1	0	1	reg <1509>	reg <1525>	
0	1	1	0	reg <1510>	reg <1526>	
0	1	1	1	reg <1511>	reg <1527>	
1	0	0	0	reg <1512>	reg <1528>	
1	0	0	1	reg <1513>	reg <1529>	
1	0	1	0	reg <1514>	reg <1530>	
1	0	1	1	reg <1515>	reg <1531>	
1	1	0	0	reg <1516>	reg <1532>	
1	1	0	1	reg <1517>	reg <1533>	
1	1	1	0	reg <1518>	reg <1534>	
1	1	1	1	reg <1519>	reg <1535>	MSB

This Macrocell uses a 16-bit register to define their output function. The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within the 4-bit LUT logic cell.

4-Bit LUT0 OUT0 is defined by reg<1519:1504>

4-Bit LUT0 OUT1 is defined by reg<1535:1520>

Table 71. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

11.0 Analog Comparators (ACMP)

There are four Analog Comparator (ACMP) macrocells in the SLG46580/82/83. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0_pd, ACMP1_pd, ACMP2_pd and ACMP3_pd) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is LOW.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain low, and then become valid 2 ms (max) after ACMP power up signal goes HIGH. If VDD is greater than 2.7 V, then power up time will decrease.

Vref accuracy is optimized near 1000 mV selection.

Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 1 MΩ resistors. IN- voltage range: 0 - 1.2 V. Can use Vref selection VDD/4 and VDD/3 to maintain this input range.

To ensure proper chip startup operation, it is recommended to enable the ACMPs with the POR signal, and not the VDD signal.

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator.

Low bandwidth: For VDD 2.3 V or less, this option will connect a low pass filter with 180 kHz upper frequency. And if input frequency > 200 kHz, the output will retain its previous value.

Note that power supply control options have influence on Analog macrocells operation.

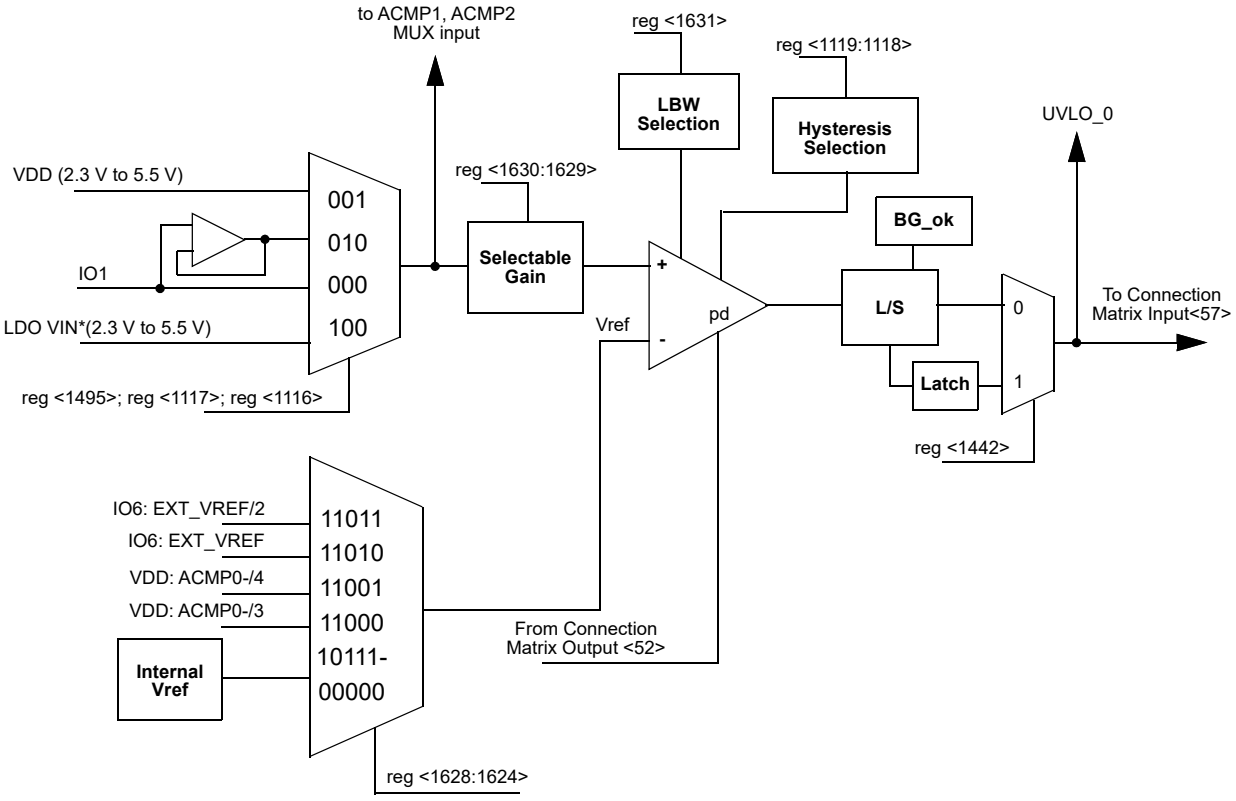
Note: Any ACMP powered ON enables the BandGap circuit as well, and an analog voltage will appear on Vref (even when Force BandGap is disabled).

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV. ACMP2 and ACMP3 has additional hysteresis options for 100 mV and 150 mV.

Note: the 25 mV hysteresis option works with either internal or external Vref, while all other options work with internal Vref only. The 50 mV, 100 mV, 150 mV, and 200 mV hysteresis options are one way hysteresis. This means that actual thresholds will be Vref (high threshold) and Vref - hysteresis (low threshold). The ACMP output will retain its output value if the input voltage is within the threshold window (between Vref and Vref - hysteresis). The 25 mV hysteresis option threshold levels will be Vref + hysteresis/2 (high threshold) and Vref - hysteresis /2 (low threshold).

Hysteresis: Input signal hysteresis options are disable, 25 mV, 50 mV, 200 mV (and additionally 100 mV and 150 mV for ACMP2 and ACMP3).
ACMP0 IN+ options are IO1, buffered IO1, VDD, LDO0/1 VIN for SLG46580, LDO0 VIN for SLG46582, LDO VIN for SLG46583.
ACMP1 IN+ options are IO4, buffered IO4, ACMP0 IN+, LDO2/3 VIN for SLG46580, LDO1 VIN for SLG46582, LDO VIN 0 for SLG46583.
ACMP2 IN+ options are IO7, ACMP0 IN+, Temp. Sensor.
ACMP3 IN+ options are IO8, ACMP2 IN+, LDO0 VOUT and LDO2 VOUT for SLG46580, LDO0 VOUT and LDO1 VOUT for SLG46582, LDO VOUT for SLG46583.

11.1 ACMP0 Block Diagram



Note*: See sections 2.2 to 2.4.

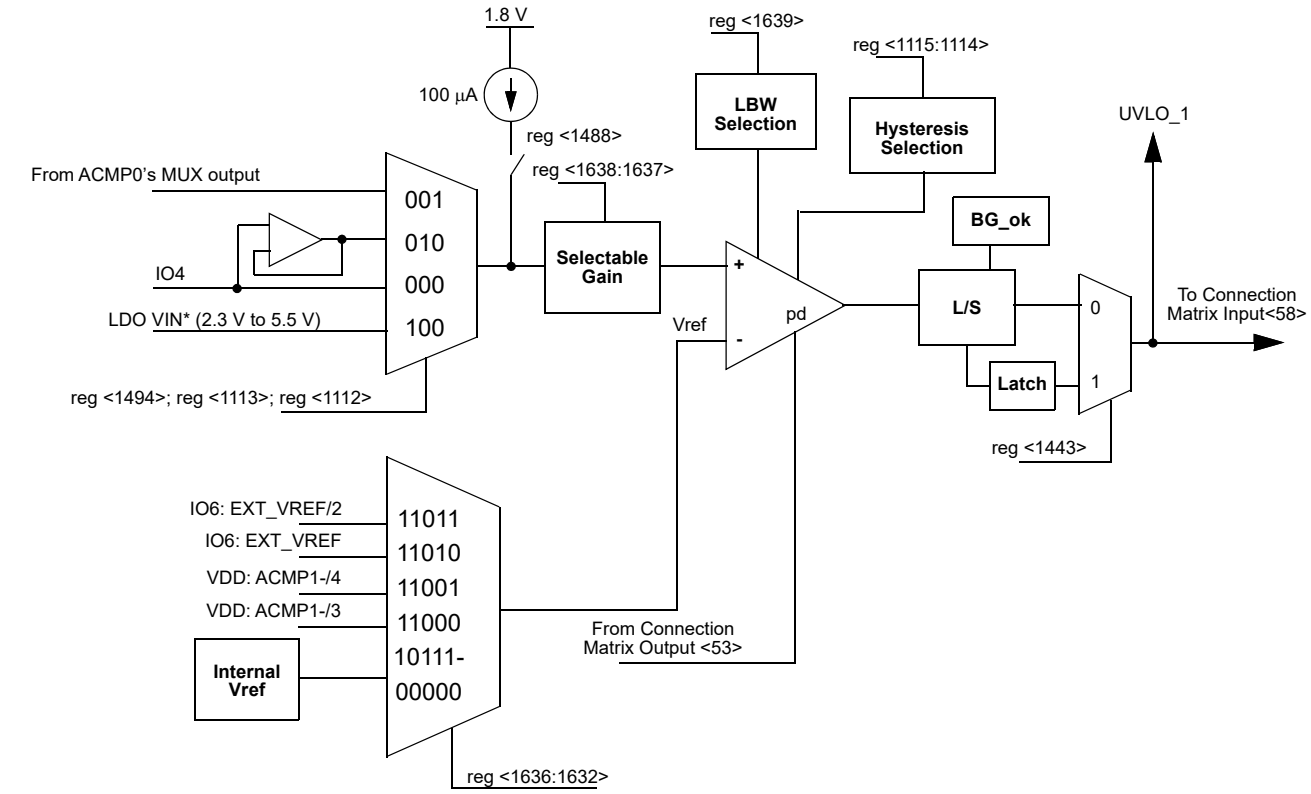
Figure 38. ACMP0 Block Diagram

11.2 ACMP0 Register Settings

Table 72. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP0 Positive Input Source Select VDD	reg<1116>	0: Disable 1: Enable
Analog Buffer at ACMP0 Enable (Max. BW 1 MHz)	reg<1117>	0: Disable analog buffer 1: Enable analog buffer
ACMP0 Hysteresis Enable	reg<1119:1118>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50 mV & 200 mV hysteresis.)
ACMP0 Wake & Sleep function Enable	reg<1442>	0: Disable 1: Enable
LDO0/1 VIN connection enable to ACMP0	reg<1495>	0: Default ACMP function 1: Enable UVLO0 function
ACMP0 In Voltage Select	reg<1628:1624>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP0- /3 11001: VDD: ACMP0- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2
ACMP0 Positive Input Divider	reg<1630:1629>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg<1631>	0: Off 1: On

11.3 ACMP1 Block Diagram



Note*: See sections 2.2 to 2.4.

Figure 39. ACMP1 Block Diagram

11.4 ACMP1 Register Settings

Table 73. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP1 Positive Input Source Select - ACMP0 IN+ Source	reg<1112>	0: Disable 1: Enable
Analog Buffer at ACMP1 Enable (Max. BW 1 MHz)	reg<1113>	0: Disable analog buffer 1: Enable analog buffer
ACMP1 Hysteresis Enable	reg<1115:1114>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV) (01: for both external & internal VREF; 10 & 11: for only internal VREF; External VREF will not have 50 mV & 200 mV hysteresis.)
ACMP1 Wake & Sleep function Enable	reg<1443>	0: Disable 1: Enable
ACMP1 100 uA Current Source Enable	reg<1488>	0: Disable 1: Enable
LDO2/3 VIN connection enable to ACMP1	reg<1494>	0: Default ACMP function 1: Enable UVLO1 function
ACMP1 In Voltage Select	reg<1636:1632>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP1- /3 11001: VDD: ACMP1- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2
ACMP1 Positive Input Divider	reg<1638:1637>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg<1639>	0: Off 1: On

11.5 ACMP2 Block Diagram

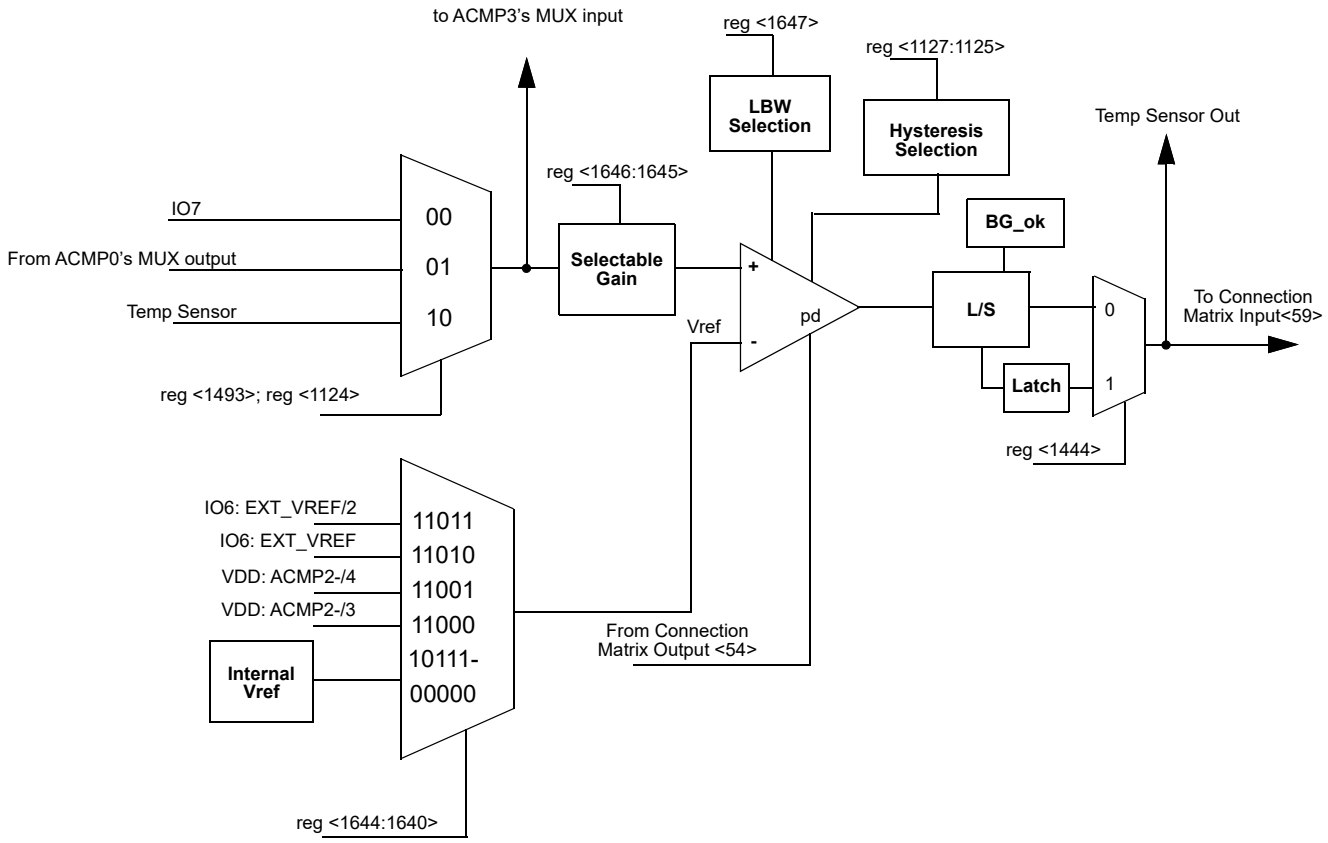


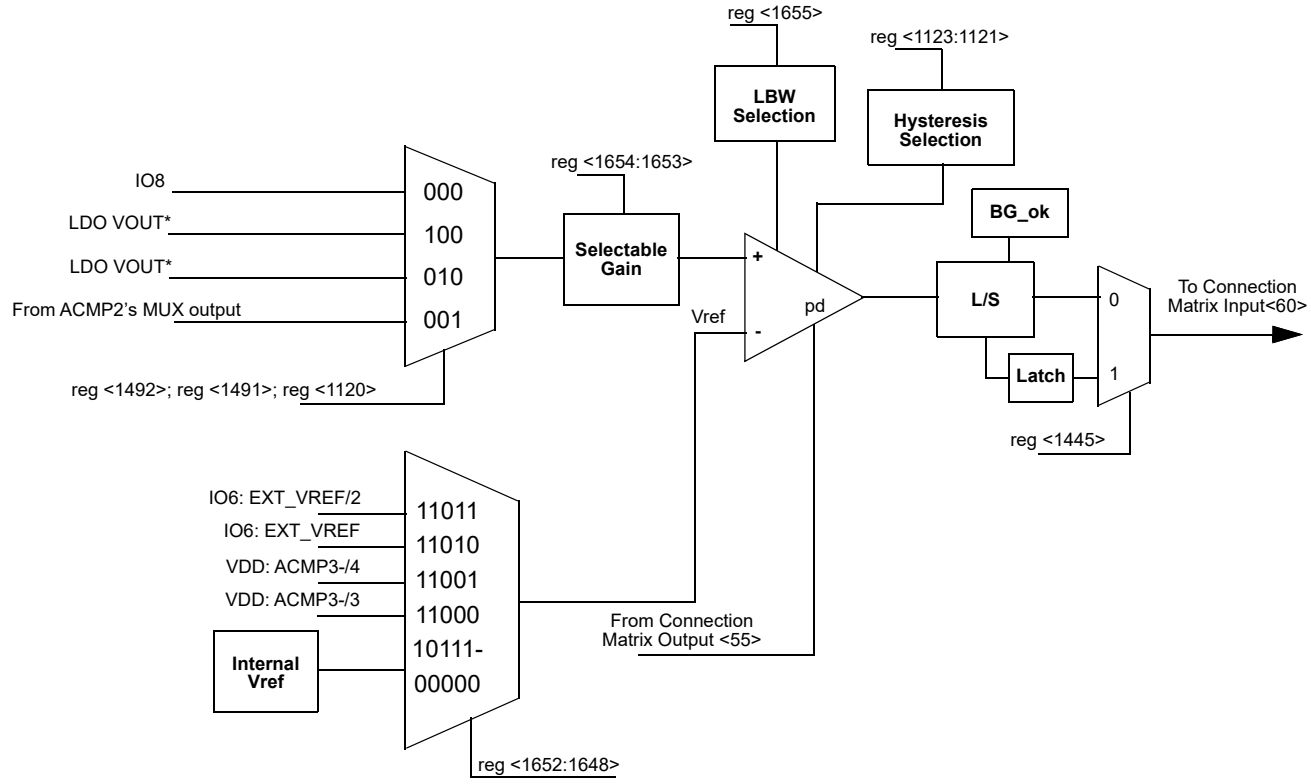
Figure 40. ACMP2 Block Diagram

11.6 ACMP2 Register Settings

Table 74. ACMP2 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP2 Positive Input Source Select - ACMP0 IN+ Source	reg<1124>	0: Disable 1: Enable
ACMP2 Hysteresis Enable	reg<1127:1125>	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal VREF, 010 & 011 & 110 & 111: for only internal VREF, External VREF will not have 50 mV, 100 mV, 150 mV & 200 mV hysteresis.)
ACMP2 Wake & Sleep function Enable	reg<1444>	0: Disable 1: Enable
TS output connection enable to ACMP2	reg<1493>	0: Default ACMP function 1: Enable TS function
ACMP2 In Voltage Select	reg<1644:1640>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP2- /3 11001: VDD: ACMP2- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2
ACMP2 Positive Input Divider	reg<1646:1645>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP2 Low Bandwidth (Max: 1 MHz) Enable	reg<1647>	0: Off 1: On

11.7 ACMP3 Block Diagram



Note*: See sections 2.2 to 2.4.

Figure 41. ACMP3 Block Diagram

11.8 ACMP3 Register Settings

Table 75. ACMP3 Register Settings

Signal Function	Register Bit Address	Register Definition
ACMP3 Positive Input Source Select - ACMP2 IN+ Source	reg<1120>	0: Disable 1: Enable
ACMP3 Hysteresis Enable	reg<1123:1121>	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal VREF, 010 & 011 & 110 & 111: for only internal VREF, External VREF will not have 50 mV, 100 mV, 150 mV & 200 mV hysteresis.)
ACMP3 Wake & Sleep function Enable	reg<1445>	0: Disable 1: Enable
LDO2 VOUT output connection enable to ACMP3	reg<1491>	0: Default ACMP function 1: Enable LDO2 VOUT function
LDO0 VOUT output connection enable to ACMP3	reg<1492>	0: Default ACMP function 1: Enable LDO0 VOUT function
ACMP3 In Voltage Select	reg<1652:1648>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP3- /3 11001: VDD: ACMP3- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2
ACMP3 Positive Input Divider	reg<1654:1653>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP3 Low Bandwidth (Max: 1 MHz) Enable	reg<1655>	0: Off 1: On

11.9 ACMPs Typical Performance

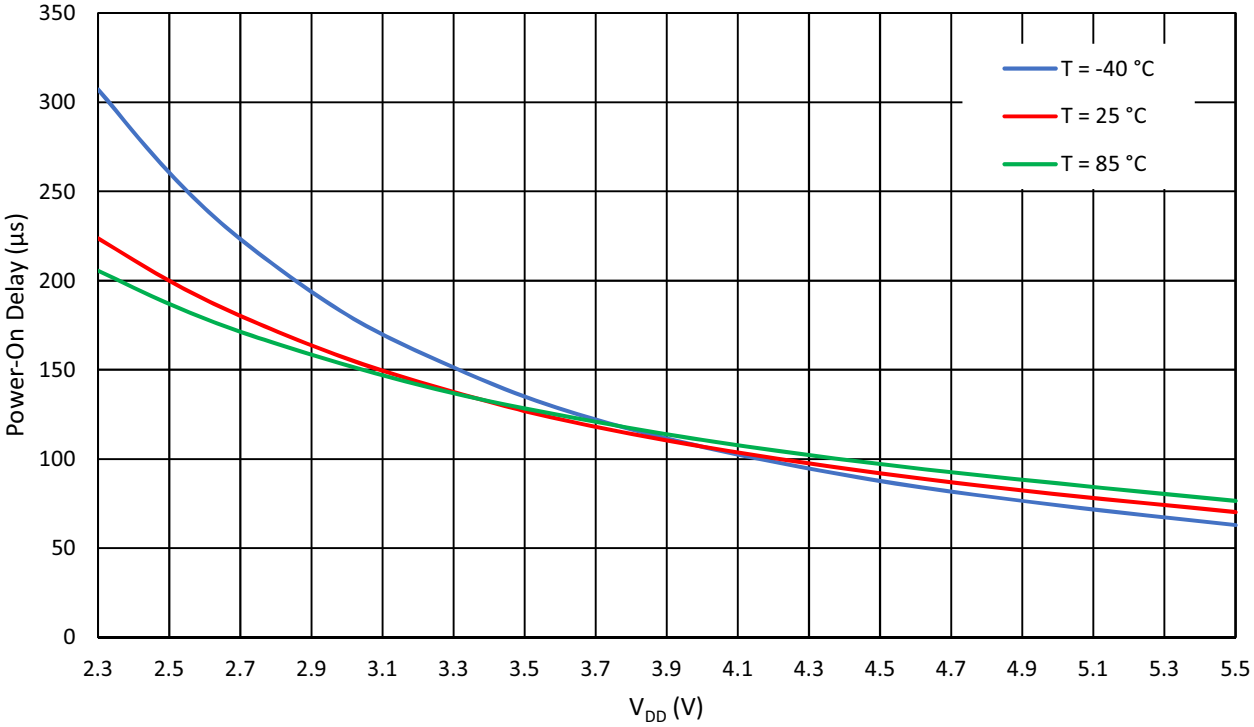


Figure 42. ACMPs Power-On Delay vs. V_{DD}

12.0 Pipe Delay (PD)

The SLG46580/82/83 has a pipe delay logic cell that is shared with the 3-bit LUT11 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section *9.5 3-Bit LUT or Pipe Delay / Ripple Counter Macrocell* for the description of this Combination Function macrocell.

13.0 Programmable Delay / Edge Detector

The SLG46580/82/83 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

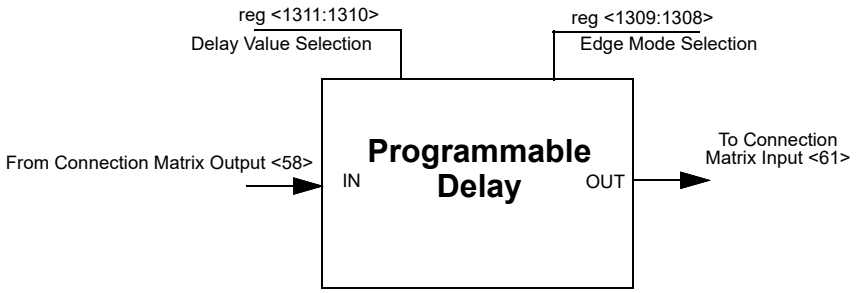


Figure 43. Programmable Delay

13.1 Programmable Delay Timing Diagram - Edge Detector Output

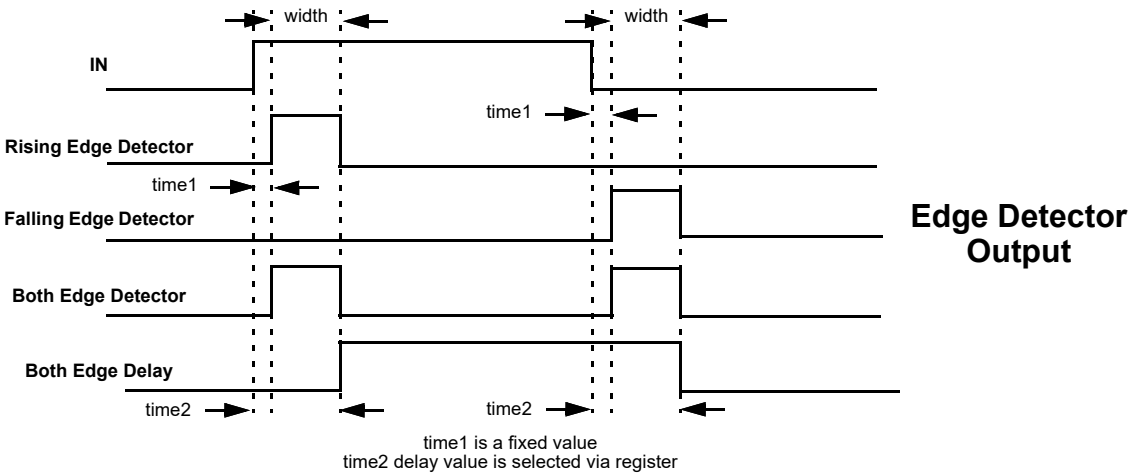


Figure 44. Edge Detector Output

Please refer to *Table 5. Typical Propagations Delays and Pulse Widths at T = 25°C*

13.2 Programmable Delay Register Settings

Table 76. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Select the edge mode of programmable delay & edge detector	reg<1309:1308>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Delay value select for programmable delay & edge detector (VDD = 3.3V, typical condition)	reg<1311:1310>	00: 165 ns 01: 300 ns 10: 440 ns 11: 575 ns

14.0 Additional Logic Functions

The SLG46580/82/83 has two additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two deglitch filters, each with edge detector functions.

14.1 Deglitch Filter / Edge Detector

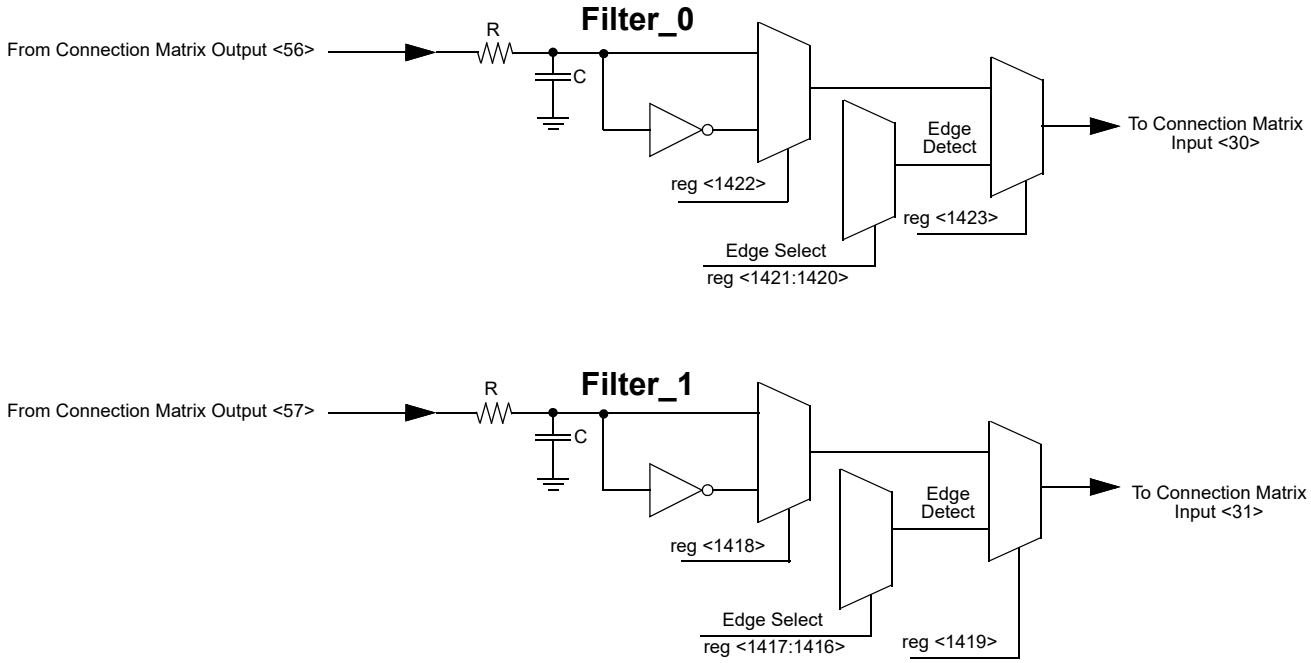


Figure 45. Deglitch Filter / Edge Detector

14.2 Deglitch Filter Register Settings

Table 77. Deglitch Filter Register Settings

Signal Function	Register Bit Address	Register Definition
Filter_1/Edge Detector_1 Edge Select	reg<1417:1416>	00: Rising Edge Detector 01: Fall Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Filter_1/Edge Detector_1 output Polarity Select	reg<1418>	0: Filter_1 output 1: Filter_1 output inverted
Filter_1 or Edge Detector_1 Select (Typ. 50nS @VDD=3.3V)	reg<1419>	0: Filter_1 1: Edge Detector_1
Filter_0/Edge Detector_0 Edge Select	reg<1421:1420>	00: Rising Edge Detector 01: Fall Edge Detector 10: Both Edge Detector 11: Both Edge Delay

Table 77. Deglitch Filter Register Settings

Signal Function	Register Bit Address	Register Definition
Filter_0/Edge Detector_0 output Polarity Select	reg<1422>	0: Filter_0 output 1: Filter_0 output inverted
Filter_0 or Edge Detector_0 Select (Typ. 70nS @VDD=3.3V)	reg<1423>	0: Filter_0 1: Edge Detector_0

15.0 RTC Binary Counter

The SLG46580/82/83 includes a 47-bit binary Real Time Counter (RTC) designed to continuously count time. This counter consists of three components and can be programmed serially through an I^2C serial interface.

The first component is a 15-bit Counter Divider used to divide the external clock, which generates a high level pulse (with width equal to the RTC clock period) to Connection Matrix Input <23> when the counter reaches the end of the count. Since the RTC counter is used for time keeping, the most common expected use case is to connect this 15-bit counter divider to a 32.768 kHz clock source, in which case the output will be a pulse at 1 second intervals, with high time of ~30.5 µS.

The second component is the 32-bit Time Counter, which takes its clock input from either the output of the 15-bit counter divider, or directly from Connection Matrix Output <101>. If the input clock comes from the 15-bit counter divider, and this counter divider is used to count time in seconds (most common use case), then the count value in this 32-bit time counter will be the number of seconds elapsed since it was loaded. The contents are read / write accessible via the address range 0x75 – 0x7A. When the counter is read, the current time is latched into a shadow buffer register, which is output on the serial data line while the counter continues to increment.

The third component is a 32-bit Alarm Digital Comparator (DCMP). This generates an alarm signal to Connection Matrix Input <24> when the time counter value matches the DCMP alarm value, which is set via I^2C serial interface. An I^2C bus Master is used to write to the 32-bit Alarm DCMP register bits in order to define the next wake up time. The 32-bit Alarm DCMP loads its initial value from reg <1023:992> at POR, and can be changed at any time by I^2C. The Alarm DCMP output is high for one clock period of the 32-bit Time Counter.

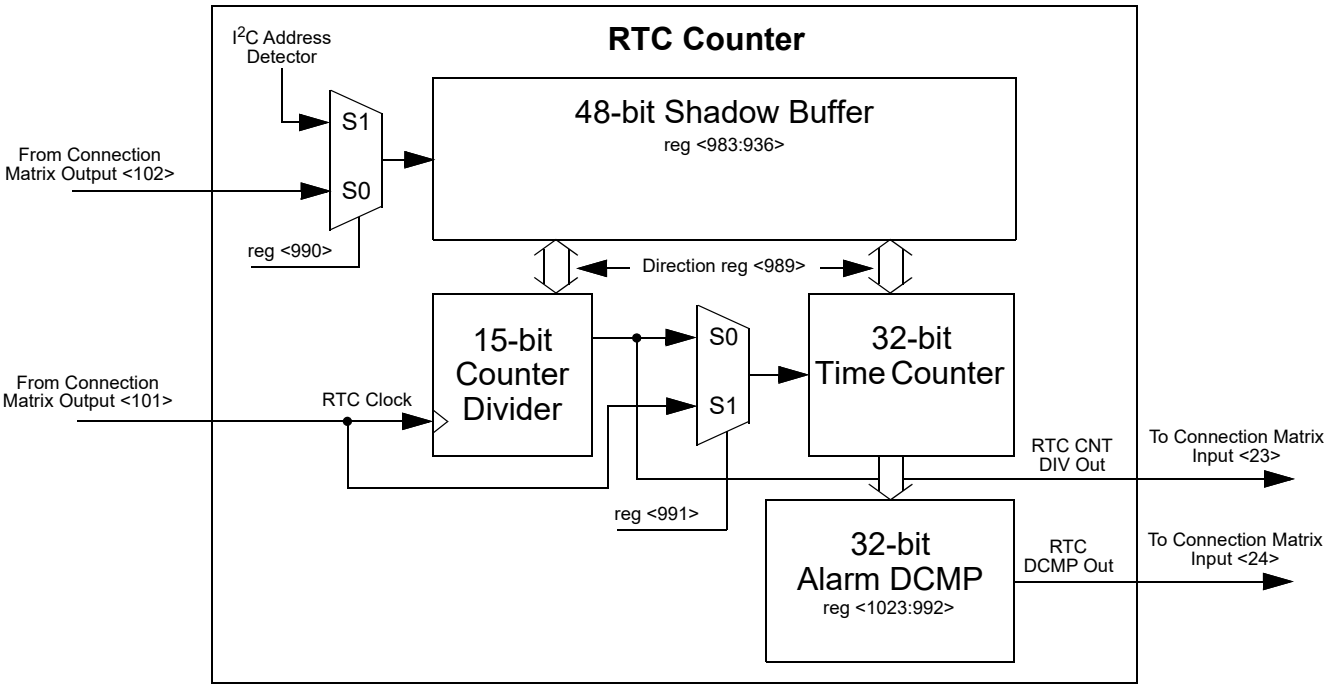


Figure 46. RTC Counter Macrocell

15.1 RTC Binary Counter Shadow Buffer

All reading or writing of data to this macrocell goes through the 48-bit Shadow Buffer. In order to read the current RTC counter value through the I^2C, the RTC counter value must first be copied to the shadow buffer. The RTC Counter's value can be copied to the 48-bit shadow buffer by either rising edge trigger signal through the Connection Matrix Output <102> or by a trigger signal generated by reading the I^2C address at 0x75 – 0x7A. The same trigger signals are used to transfer data in the opposite direction (from the shadow buffer to RTC counter).

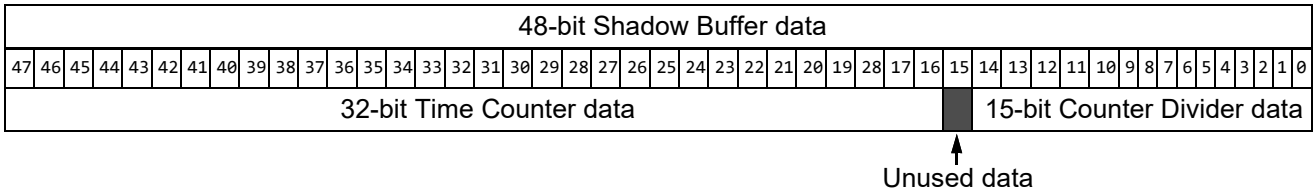


Figure 47. RTC Counter Shadow Buffer bits

- Reg <990> defines the source of the trigger signal for the copy to shadow buffer, either from the Connection Matrix or from the designated I^2C address read. The trigger source can be changed though an I2C write command to change this bit setting.
- Reg <989> defines the direction of whether RTC Counter data will be copied to 48-bit shadow buffer or the 48-bit shadow buffer data will be copied to the RTC Counter. The direction can be changed though an I^2C write command to change this bit setting.

15.1.1 RTC Binary Counter Shadow Buffer Operating Modes

The combined values in reg <990> and reg<989> provide four modes of operation for the shadow buffer, allowing the user to latch the shadow buffer data into the RTC counter, or to latch data the RTC counter data into the shadow buffer, and to choose the signal that will latch the data.

Table 78. Shadow Buffer Register Settings

Reg <989>	Reg <990>	Shadow Buffer Operating Modes
0	0	RTC data will be latched in the shadow buffer by rising edge on Connection Matrix Output <102>
0	1	RTC data will be latched in the shadow buffer by reading any I^2C address in the range 0x75 – 0x7A. The latch signal is activated when the I^2C address comparison circuit indicates a matching address in an incoming command. All bytes of one RTC data sample can be read using Sequential Read Command.
1	0	Shadow buffer data will be latched in the RTC by rising edge on Connection Matrix Output <102>
1	1	Shadow buffer data will be latched in the RTC at the completion of a write command to I^2C address in the range 0x75 – 0x7A. All bytes of one shadow buffer data sample can be written using Sequential Write Command.

16.0 Voltage Reference (VREF)

16.1 Voltage Reference Overview

The SLG46580/82/83 has a Voltage Reference Macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from IO6. See table below for the available selections for each analog comparator.

16.2 VREF Selection Table

Table 79. VREF Selection Table.

SEL<4:0>	ACMP0_VREF	ACMP1_VREF	ACMP2_VREF	ACMP3_VREF
11011	IO6: EXT_VREF /2	IO6: EXT_VREF /2	IO6: EXT_VREF /2	IO6: EXT_VREF /2
11010	IO6: EXT_VREF	IO6: EXT_VREF	IO6: EXT_VREF	IO6: EXT_VREF
11001	VDD: ACMP0- / 4	VDD: ACMP1- / 4	VDD: ACMP2- / 4	VDD: ACMP3- / 4
11000	VDD: ACMP0- / 3	VDD: ACMP1- / 3	VDD: ACMP2- / 3	VDD: ACMP3- / 3
10111	1.20	1.20	1.20	1.20
10110	1.15	1.15	1.15	1.15
10101	1.10	1.10	1.10	1.10
10100	1.05	1.05	1.05	1.05
10011	1.00	1.00	1.00	1.00
10010	0.95	0.95	0.95	0.95
10001	0.90	0.90	0.90	0.90
10000	0.85	0.85	0.85	0.85
01111	0.80	0.80	0.80	0.80
01110	0.75	0.75	0.75	0.75
01101	0.70	0.70	0.70	0.70
01100	0.65	0.65	0.65	0.65
01011	0.60	0.60	0.60	0.60
01010	0.55	0.55	0.55	0.55
01001	0.50	0.50	0.50	0.50
01000	0.45	0.45	0.45	0.45
00111	0.40	0.40	0.40	0.40
00110	0.35	0.35	0.35	0.35
00101	0.30	0.30	0.30	0.30
00100	0.25	0.25	0.25	0.25
00011	0.20	0.20	0.20	0.20
00010	0.15	0.15	0.15	0.15
00001	0.10	0.10	0.10	0.10
00000	0.05	0.05	0.05	0.05

Note: the ACMP external reference voltage (IN-) is limited by 1.2 V for full power supply range.

17.0 Analog Temperature Sensor

The SLG46580/82/83 has an analog temperature sensor (TS) with an output voltage linearly-proportional to Centigrade temperature. This feature was designed with a range from 50°C to 150°C as a tool to protect the chip from overheating. The TS's operates based on the temperature coefficient of a Silicon diode (~-2.1 mV/°C). As the chip temperature increases, the TS's analog output voltage decreases.

If the junction temperature exceeds the thresholds of ACMP2 or ACMP3, the ACMP outputs toggle and can shut down both internal and external circuitry. Since most of the GreenPAK's self-heating originates within the LDO regulation circuitry, ACMP2's output can lower the chip's junction temperature by disabling the LDOs.

The equation below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input. It is important to note that there will be a chip to chip variation of about ±2°C.

$$V_{TS} = -4.935 \times T + 1467.03$$

where:

V_{TS} (mV) - TS Output Voltage

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis. Many of the applicable ACMP reference voltages are listed in *Table 80*, but for those that are not, use the previous equation to approximate the temperature level.

Table 80. Temperature Sensor Voltage for VDD = 2.3..5.5 V

Vref, mV	T_{IL} - Typ., °C	T_{IH} - Typ., °C
700	154.84	155.06
750	144.82	145.47
800	134.87	135.61
850	124.87	125.65
900	114.89	115.63
950	104.85	105.56
1000	94.75	95.42
1050	84.64	85.22
1100	74.45	74.98
1150	64.26	64.73
1200	54.01	54.22

To enable the TS, set the TS enable register high in the "Temp Sensor" macrocell or the "ACMP2" macrocell's IN+ source settings. In addition, the PWR UP matrix connection of ACMP2 or ACMP3 must be set high. See *Figure 48.* for the TS block diagram when used with ACMP2 and ACMP3.

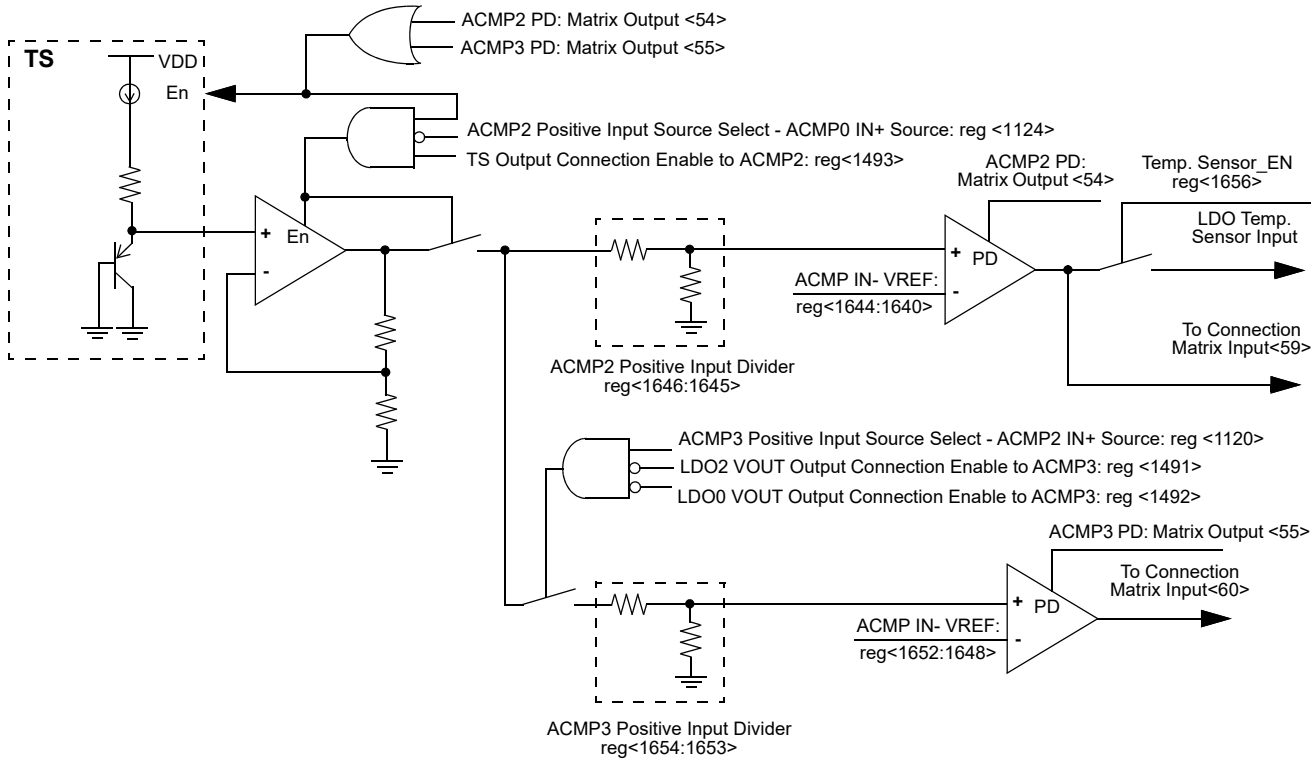


Figure 48. Analog Temperature Sensor Structure Diagram

Note: If ACMP2 or/and ACMP3 is/are used for TS function, IO7 or/and IO8 should not be used as "Analog IO"

18.0 Clocking

The SLG46580/82/83 has two internal oscillators to support a variety of applications:

- Low Power Oscillator (1.73 kHz)
- Configurable Oscillator (25 kHz or 2 MHz)

There are two divider stages that give the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The predivider (first stage) for Configurable Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the predivider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines <27> and <28>. The second stage divider is available to the configurable OSC (25 kHz or 2 MHz) only while the Low Power OSC is connected to Connection Matrix Input <29> directly after the pre-divider /1, /2, /4 or /16 for LP OSC.

The Matrix Power Down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power Down/Force On (Connection Matrix Output <59> and <60) signal has the highest priority. The OSC operates according to the following table:

Table 81. Oscillator Operation Mode Configuration Settings

Power Down/Force ON matrix control selection reg<1658>, reg<1657	From Connection Matrix Output <59>, <60>	OSC POWER MODE selection reg<1295>, reg<1290>	OSC operation mode
0	0	0	Auto Power On*
0	0	1	ON
0	1	0	OFF
0	1	1	OFF
1	0	0	Auto Power On*
1	0	1	ON
1	1	0	ON
1	1	1	ON
*Note *: the OSC will run only when any macrocell that uses OSC is powered on.*			

The SLG46580/82/83 has a 25 kHz / 2 MHz OSC Fast Start-up option up function controlled by reg <1293> (1: Enabled; 0: Disabled). It allows the OSC to have faster start up time, less than one OSC cycle when this option is enabled).

Note: The quiescent current consumption will increase when the OSC Fast Start-up option is enabled.

18.1 Low Power OSC (1.73 kHz)

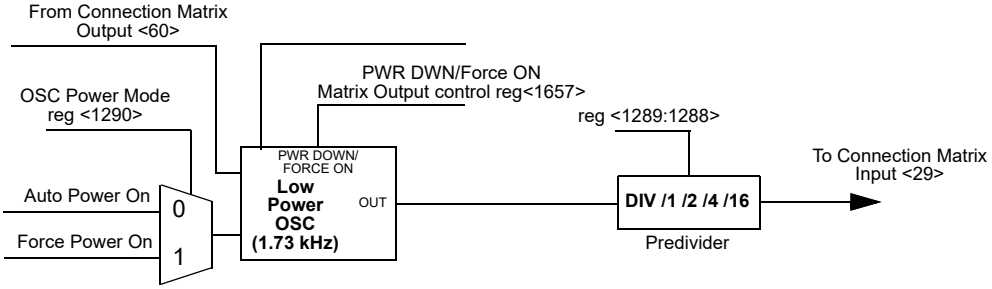


Figure 49. Low Power Oscillator Block Diagram

18.2 Configurable OSC (25 kHz / 2 MHz)

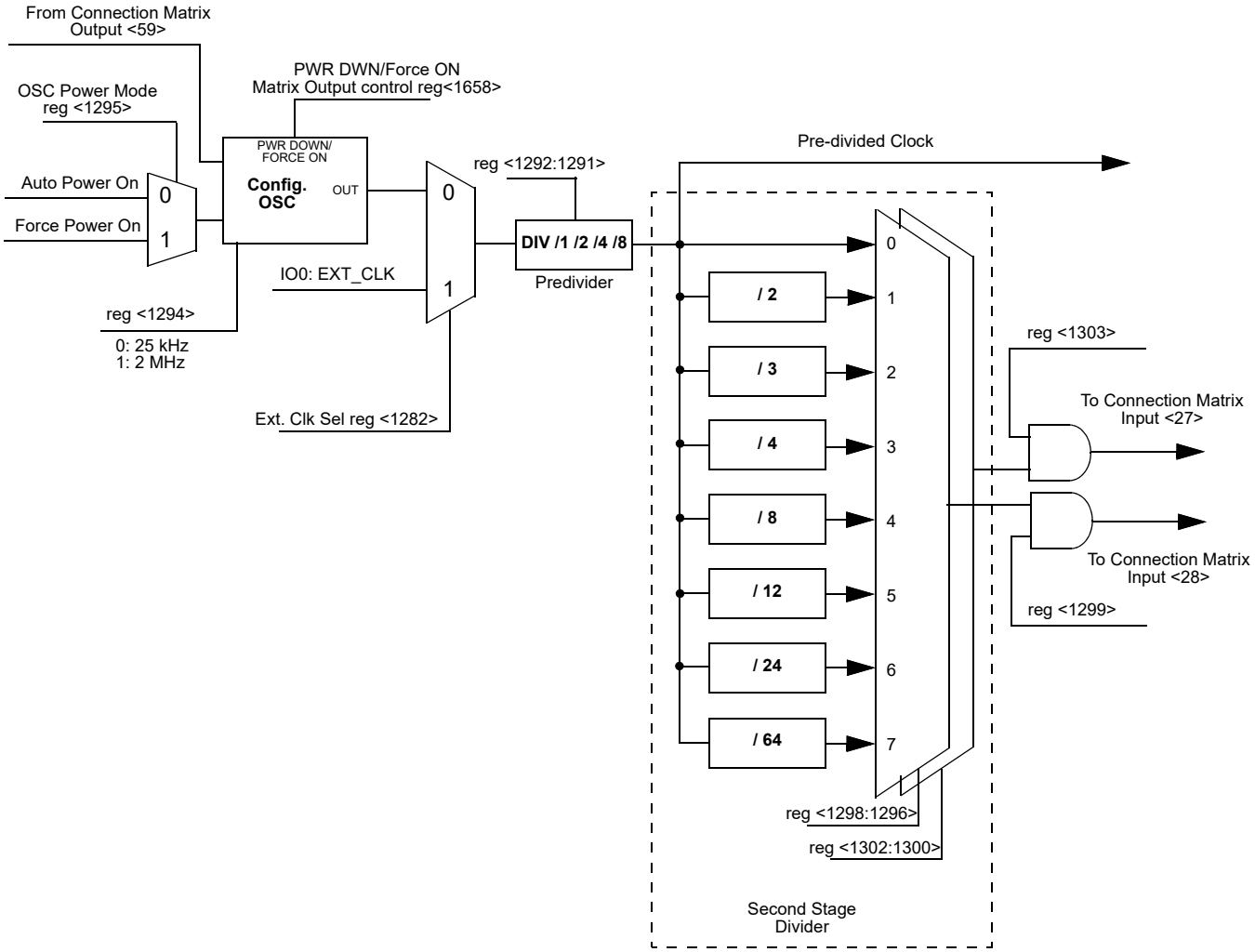


Figure 50. Configurable OSC Block Diagram

18.3 Oscillator Power On delay

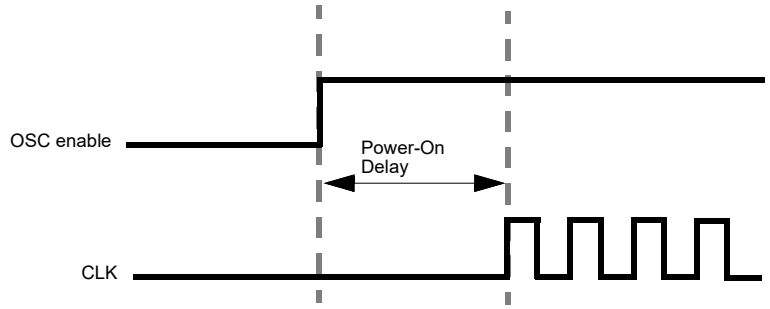


Figure 51. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power On".

Note 2: 'OSC enable' signal appears when any macrocell that uses OSC is powered on.

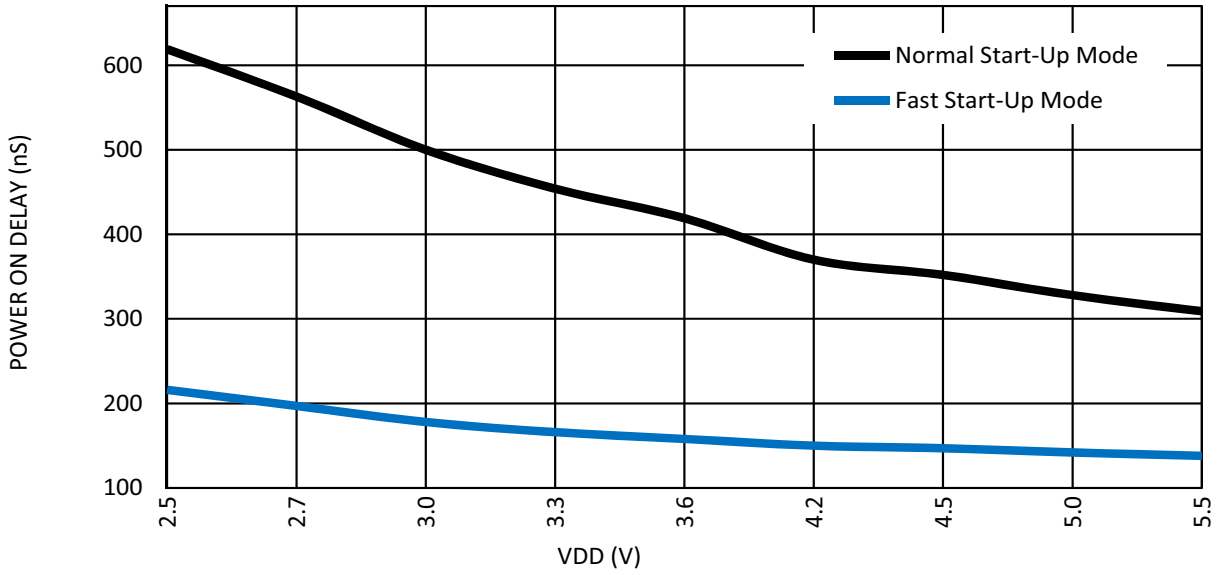


Figure 52: RC Oscillator Maximum Power-On Delay vs. V_{DD}, T = +25 °C, OSC0 = 2 MHz

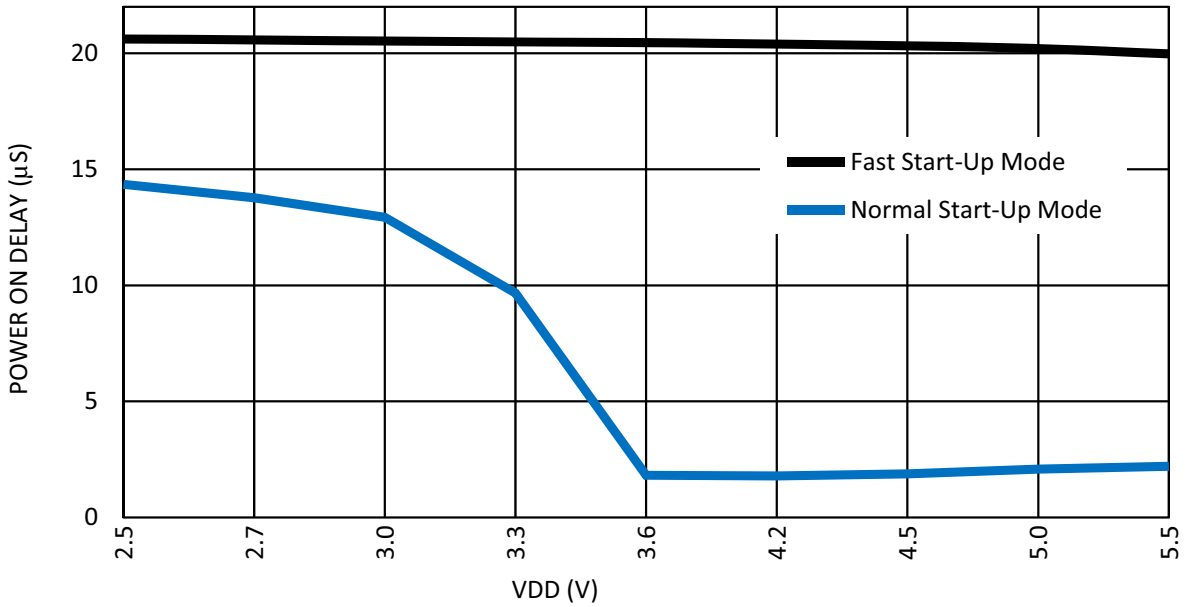


Figure 53. RC Oscillator Maximum Power On Delay vs. VDD at 85°C, OSC0 = 25 kHz

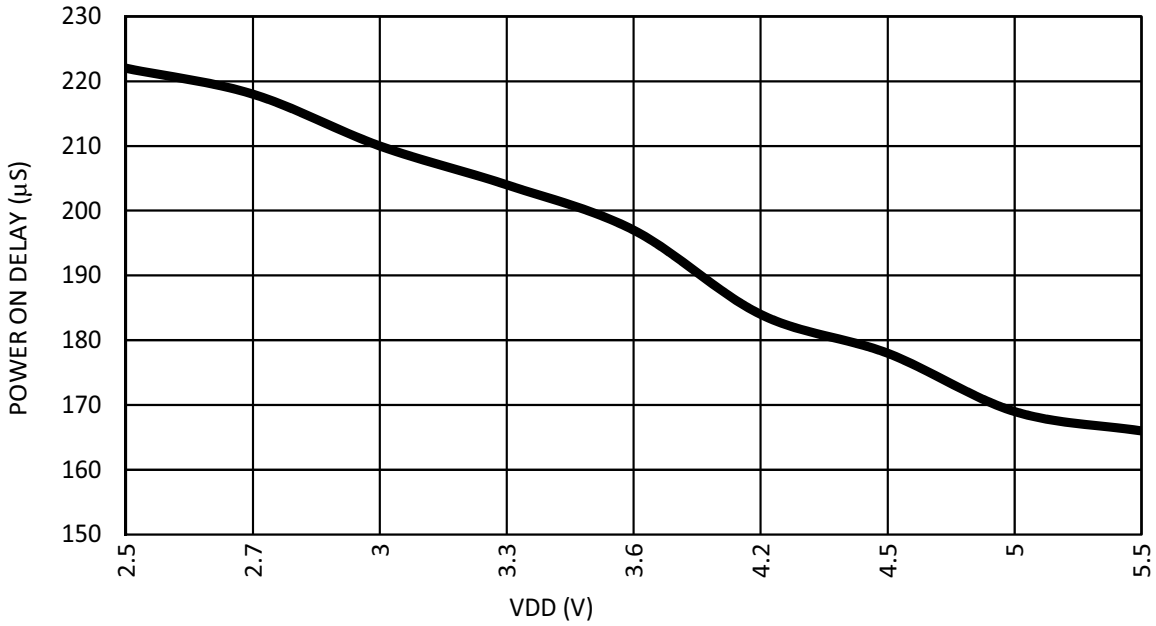


Figure 54. OSC1 (1.73 kHz) Maximum Power On Delay vs. VDD at 85°C

18.4 Oscillator Accuracy

Note 1: OSC power setting: Force Power On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

Note 2: For more information see section 5.8 OSC Specifications.

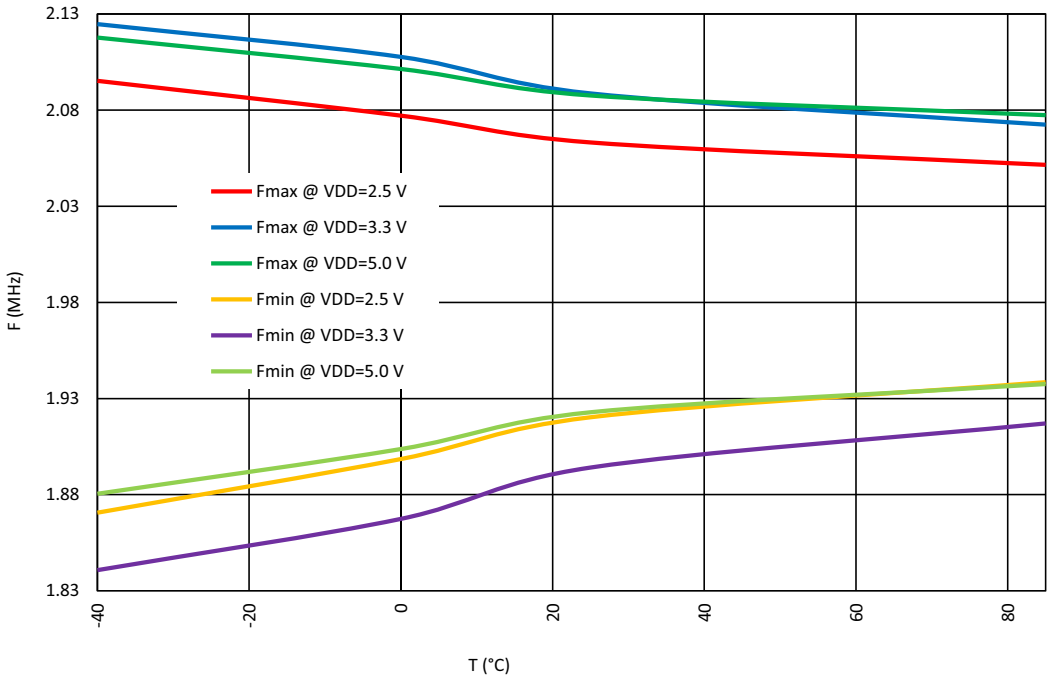


Figure 55. Oscillator Frequency vs. Temperature, OSC0 = 2 MHz

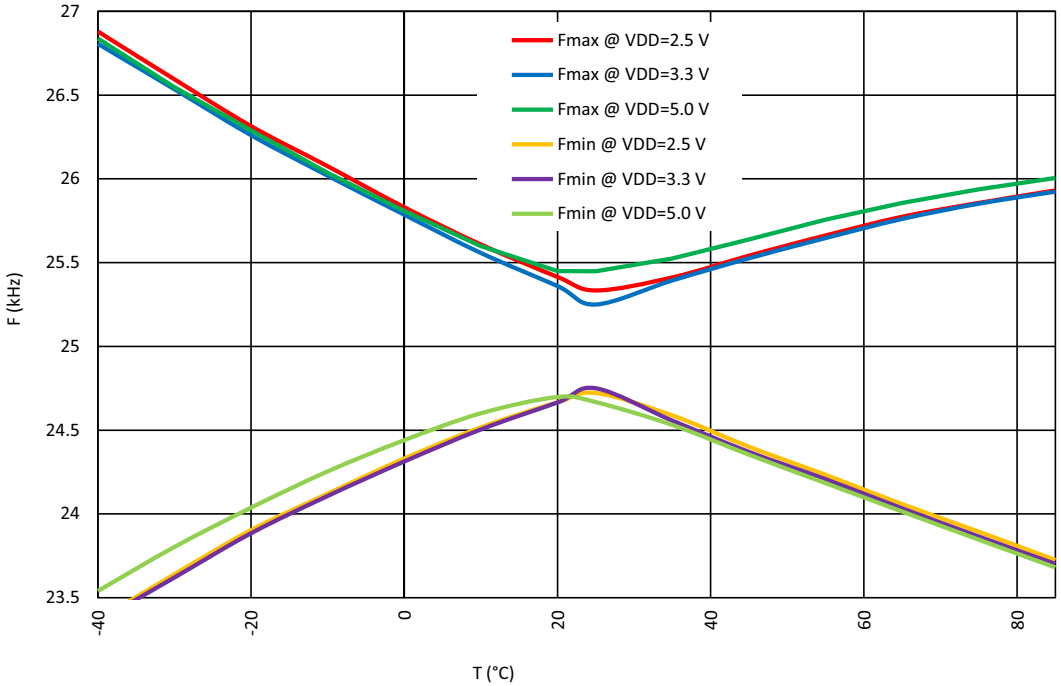


Figure 56. Oscillator Frequency vs. Temperature, OSC0 = 25 kHz

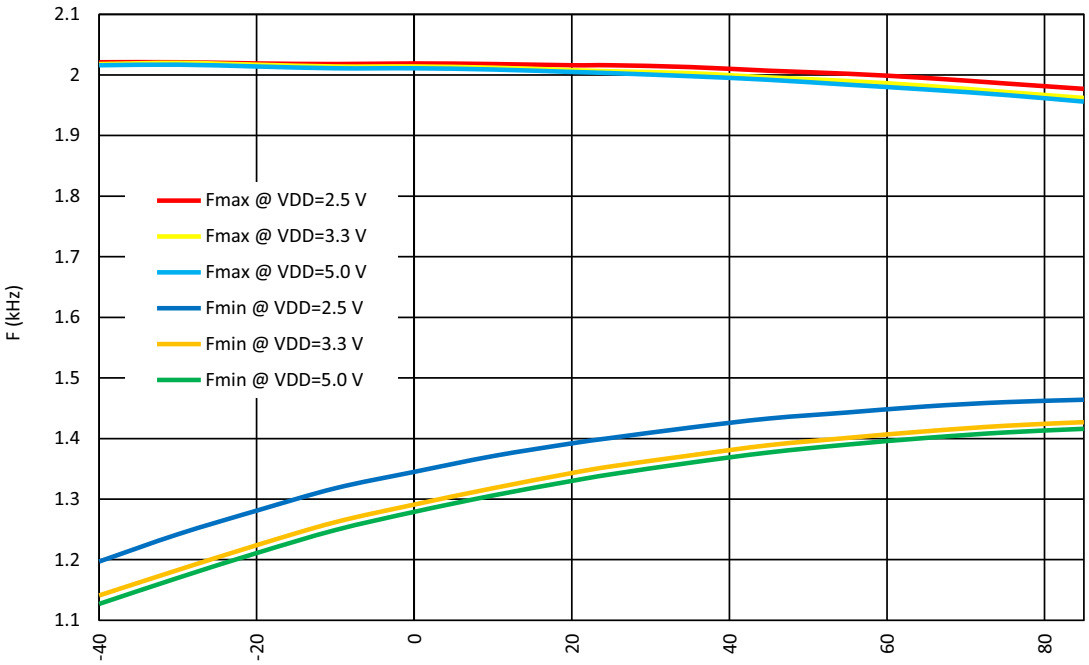


Figure 57. Oscillator Frequency vs. Temperature, OSC1 = 1.73 kHz

19.0 Power On Reset (POR)

The SLG46580/82/83 has a power-on reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the VDD power is first ramping to the device, and also while the VDD is falling during power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the I/O pins.

19.1 General Operation

The SLG46580/82/83 is guaranteed to be powered down and non-operational when the VDD voltage (voltage on VDD pin) is less than Power Off Threshold (see in Electrical Characteristics table), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (see Note 1) than the VDD voltage is applied to any other PIN. For example, if VDD voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect and can lead to incorrect or unexpected device behavior.

Note 1: There is a 0.6V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46580/82/83, the voltage applied on the VDD should be higher than the Power_ON threshold (see Note 2). The full operational VDD range for the SLG46580/82/83 is 2.3 V – 5.5 V (2.5 V ±8% - 5 V ±10%). This means that the VDD voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the VDD voltage rises to the Power_ON threshold. After the POR sequence has started, the SLG46580/82/83 will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device), and will be ready and completely operational after the POR sequence is complete.

Note 2: The Power_ON threshold is defined in Electrical Characteristics table.

Note 3: LDOs begin to operate when VDD ≥ 2.3 V.

To power down the chip the VDD voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the I/O structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also as it was mentioned before the voltage on PINs can’t be bigger than the VDD, this rule also applies to the case when the chip is powered on.

19.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in *Figure 58.* .

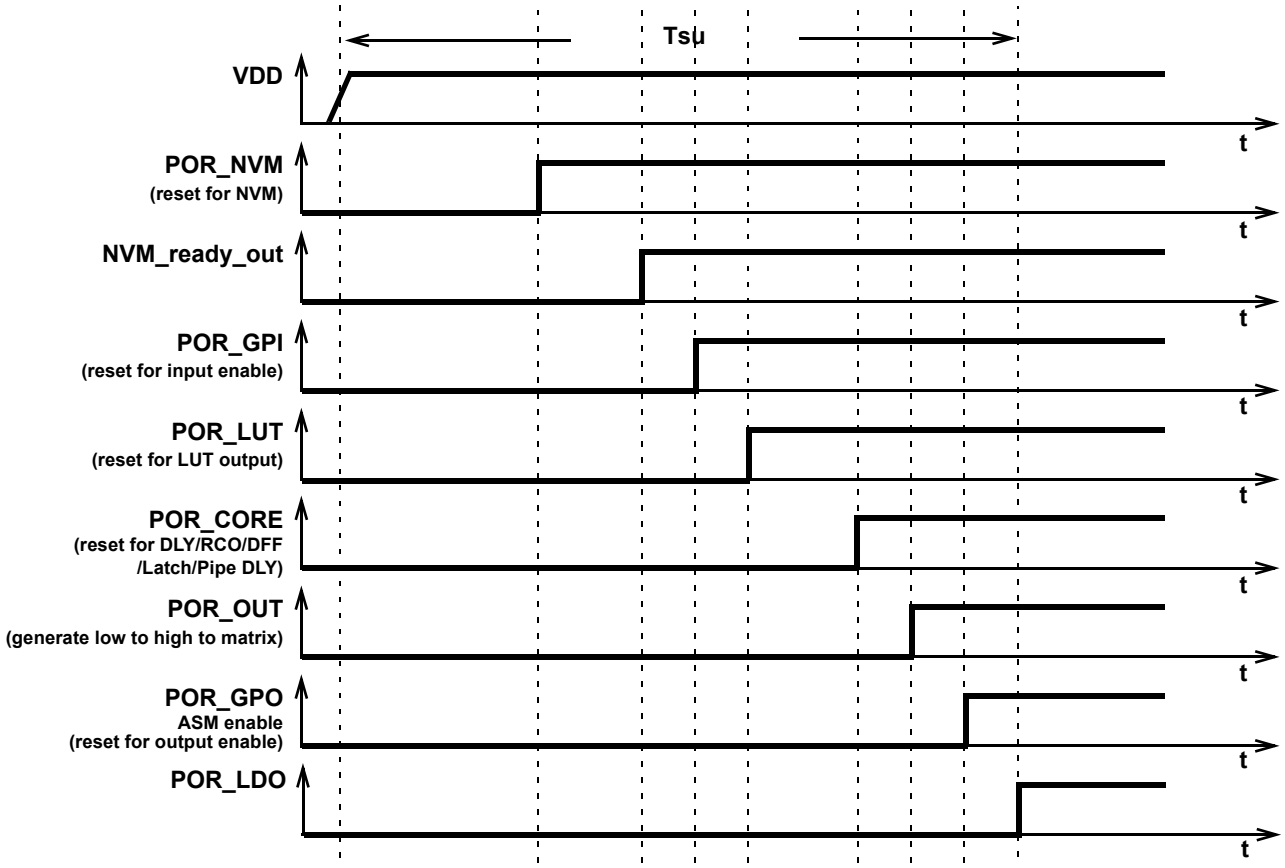


Figure 58. POR sequence

As can be seen from *Figure 58.* after the VDD has start ramping up and crosses the Power_ON threshold, first, the on-chip NVM memory is reset. Next the chip reads the data from NVM, and transfers this information to CMOS Latch that serve to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, RC OSC, DFFs, Latches and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last but one portion of the device to be initialized are the output PINs, which transition from high impedance to active at this point. LDOs begin to operate in 500 μs after PINs become active.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, VDD value, temperature and even will vary from chip to chip (process influence).

19.3 Macrocells Output States During POR Sequence

To have a full picture of SLG46580/82/83 operation during powering and POR sequence, review the overview of macrocell output states during the POR sequence (*Figure 59.* describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output PINs which are in high impedance state). Before the NVM is ready, all macrocell outputs are unpredictable (except the output PINs). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. After that input PINs are enabled. Next, only LUTs are configured. Next, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output PINs that become active and determined by the input signals.

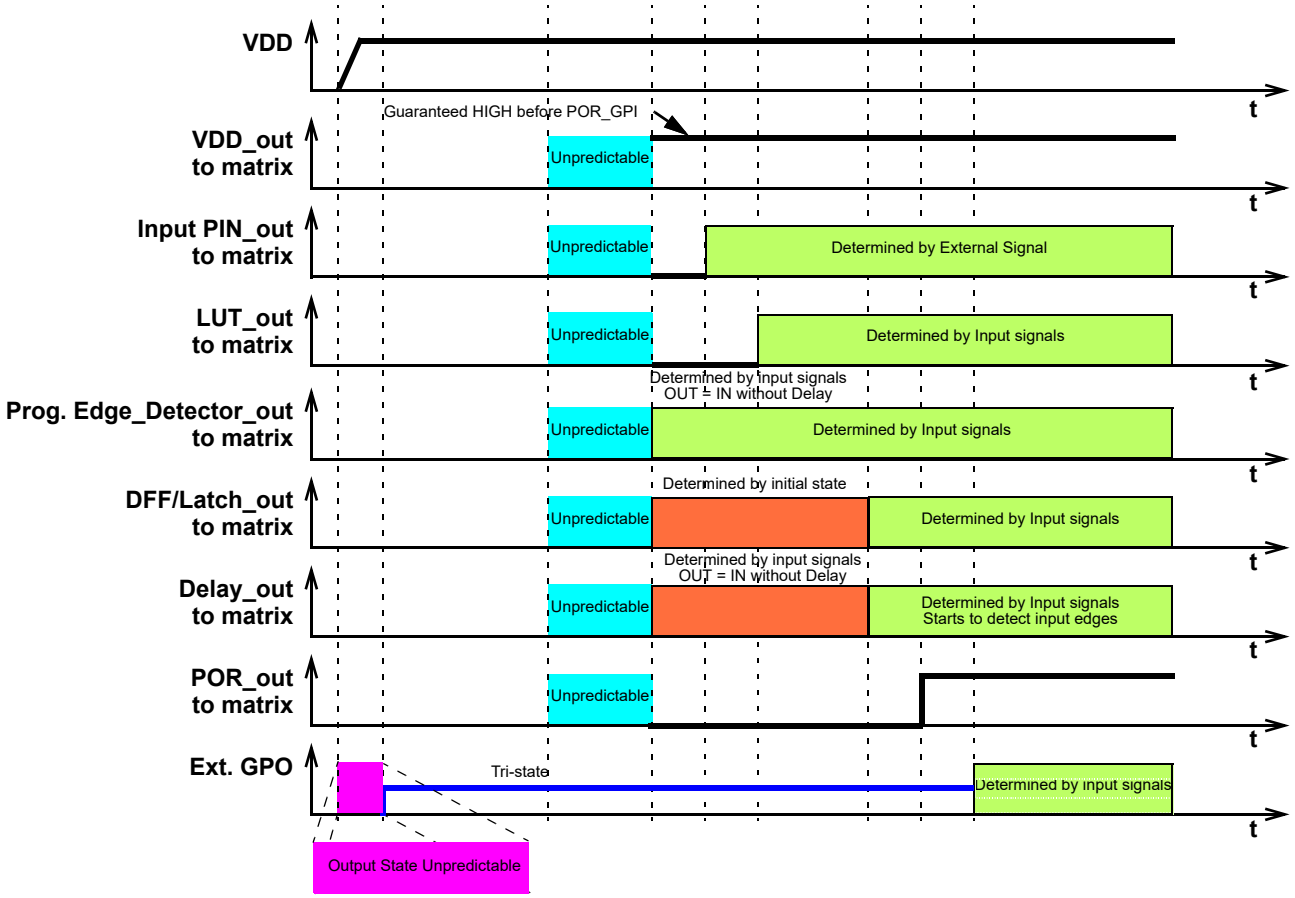


Figure 59. Internal Macrocell States during POR sequence

19.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.15 V - 1.6 V, macrocells are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input PINs, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output PIN corresponds to the internal logic
6. LDOs

Note 1: LDOs begin to operate above 2.3 V.

Note 2: The maximum voltage applied to any PIN should not be higher than the VDD level. There are ESD Diodes between PIN –> VDD and PIN –> GND on each PIN. So if the input signal applied to PIN is higher than VDD, then current will sink through the diode to VDD. Exceeding VDD results in leakage current on the input PIN, and VDD will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as VDD.

19.3.2 Power Down

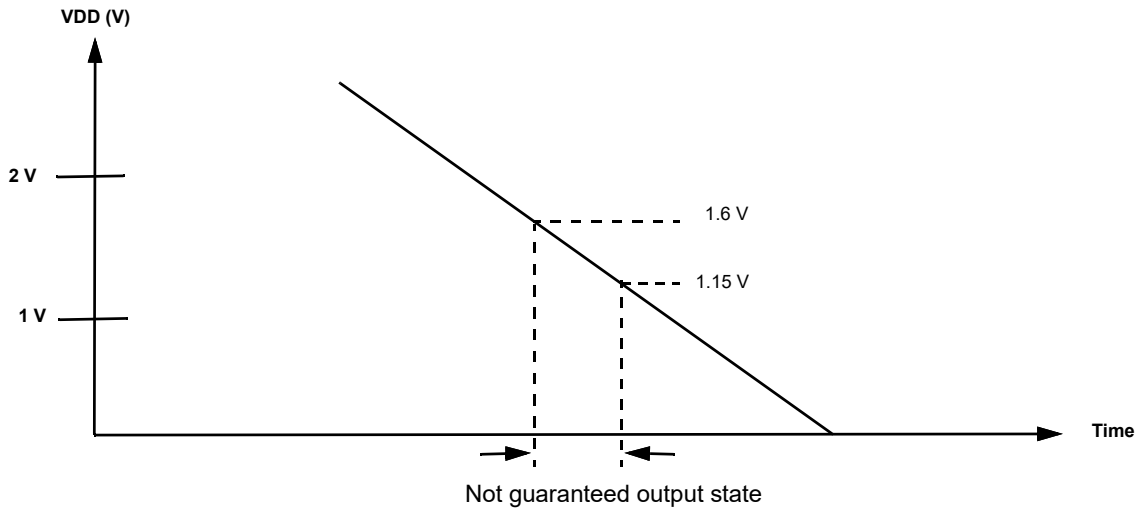


Figure 60. Power Down

During powerdown, macrocells in SLG46580/82/83 are powered off after VDD falling down below Power Off threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

19.4 External reset

The SLG46580/82/83 has an optional External Reset function on IO5. It allows to reset the chip while powered on.
IO5 must be configured as Digital Input reg<1071:1070> and function Reset must be enabled also, reg<1307>: 0 - disabled, 1 -enabled. Unlike POR, External Reset affects only GPI, LUTs, DLY, RC OSC, DFFs, Latches, Pipe Delay, Matrix and GPO. While NVM remains its previous state, see *Figure 61.* to *Figure 63.* .

Note that during External Reset the output pin's status will depend on the OE control circuits and current consumption is determined by the design.

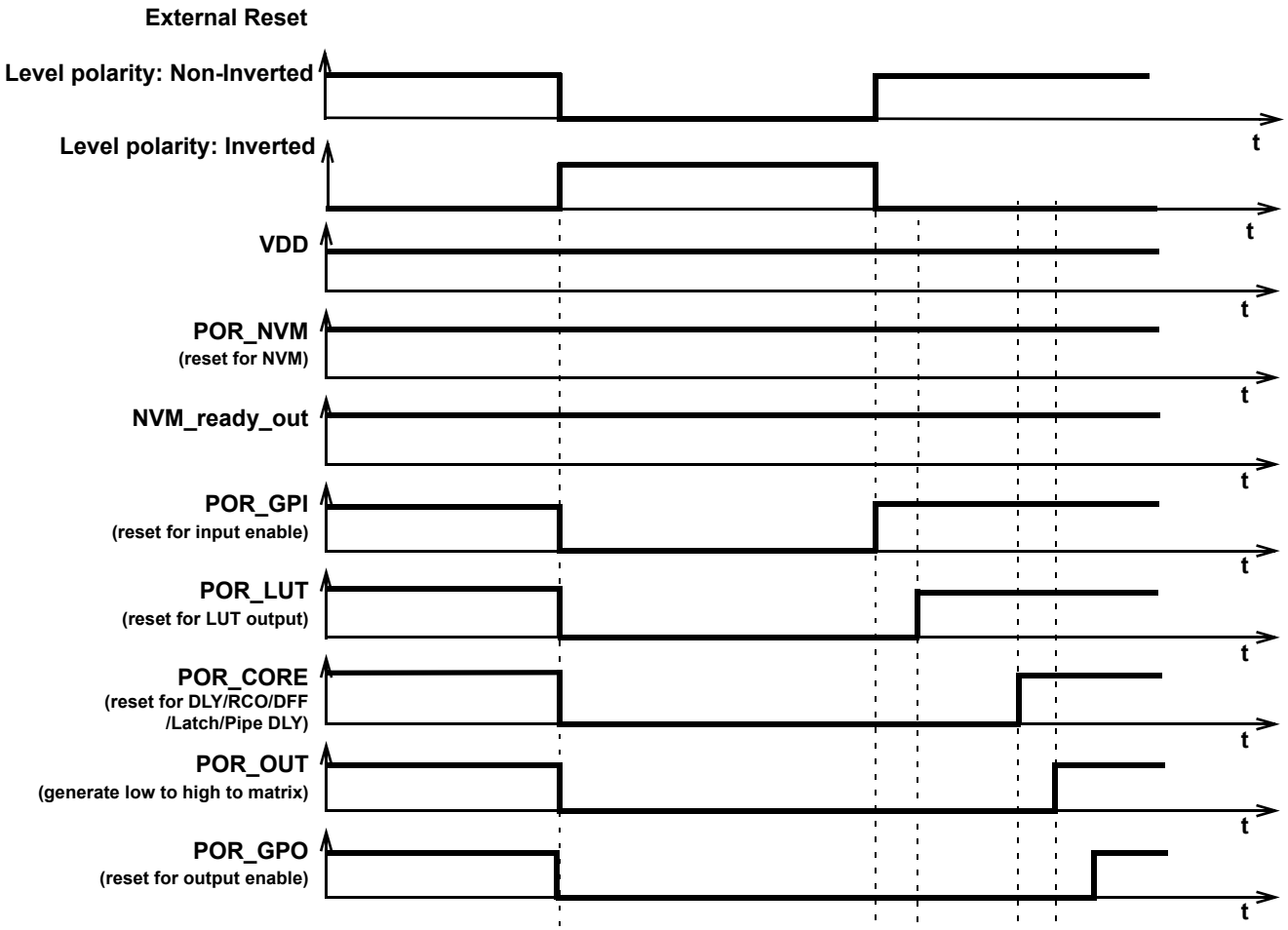


Figure 61. External Reset Sequence (Level Sensitive)

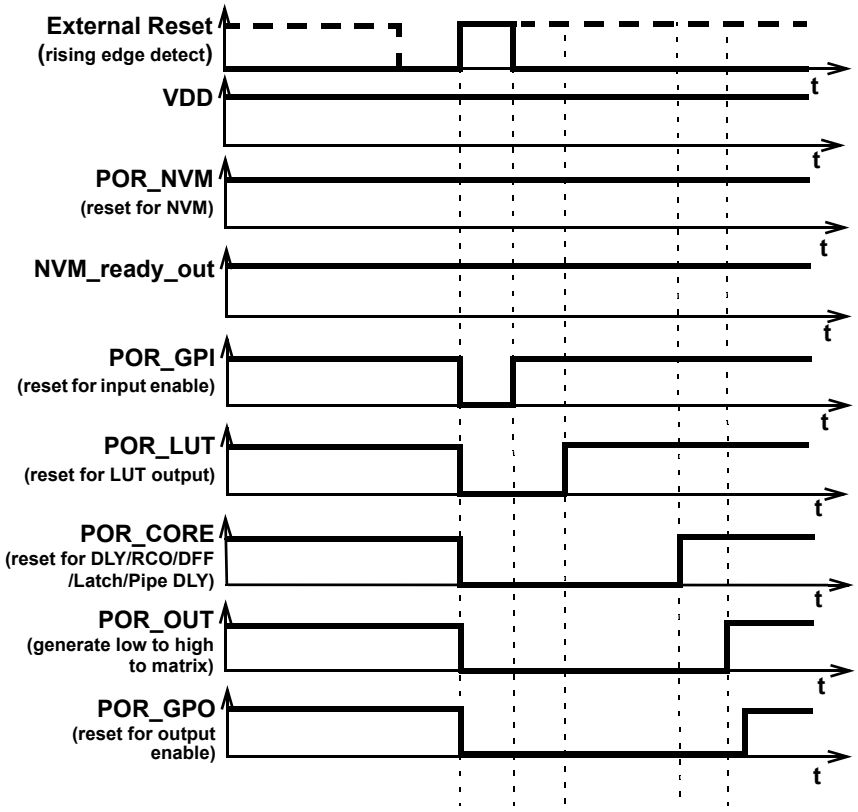


Figure 62. External reset sequence (Rising edge detect).

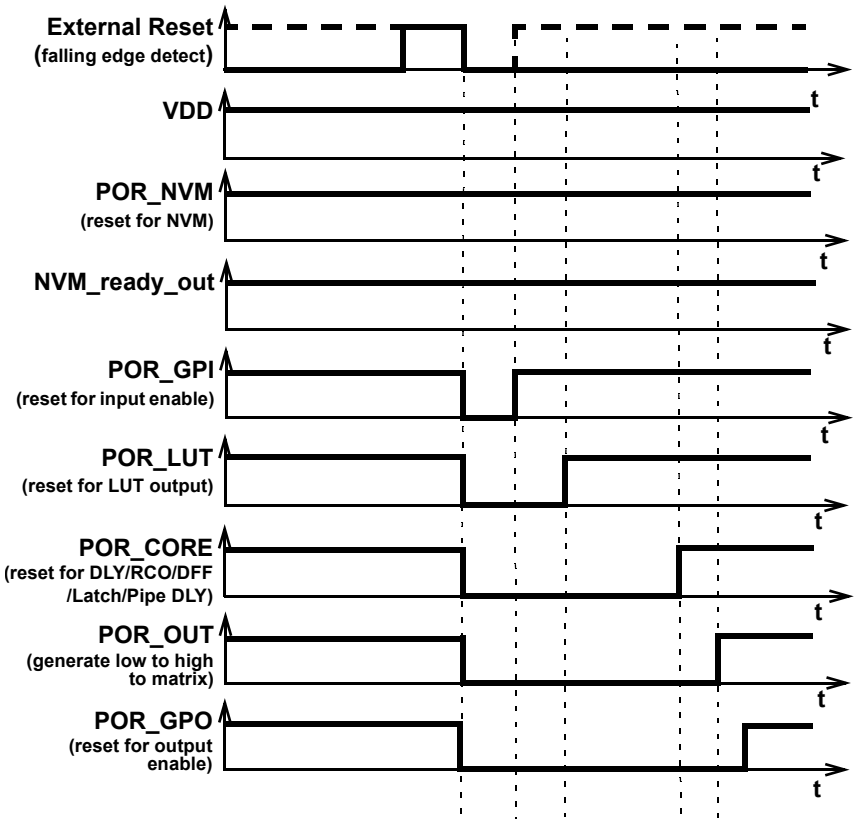


Figure 63. External reset sequence (Falling edge detect).

Table 82. External reset Register Settings

Signal Function	Register Bit Address	Register Definition
IO5 Reset level polarity selection	reg<1304>	0: Non-inverted 1: Inverted
IO5 edge reset enable	reg<1305>	0: Edge reset enable (controlled by reg<1306>) 1: High level reset
IO5 rising/falling edge reset	reg<1306>	0: Rising 1: Falling
IO5 reset function	reg<1307>	0: Disable 1: Enable

20.0 Asynchronous State Machine (ASM) Macrocell

20.1 ASM Macrocell Overview

The Asynchronous State Machine (ASM) macrocell is designed to allow the user to create state machines with between 2 to 8 states. The user has flexibility to define the available states, the available state transitions, and the input signals (a, b, c …) that will cause transitions from one state to another state, as shown in *Figure 64.* .

This macrocell has a total of 25 inputs, as shown in *Figure 65.* , which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial / Reset state. Each of the 24 inputs is level sensitive and active high, meaning that a high level input will drive the user selected transition from one state to another. Additionally, 8 out of the 24 inputs (one per state) has an option to select whether the input is rising edge sensitive, meaning that a rising level input signal will drive the user selected transition from one state to another. The fact that there are 24 inputs puts the upper bound of 24 possible state transitions total in the user defined state machine design. There is a nReset input which will drive an immediate state transition to the user-defined Initial / Reset state when active, shown in red, in the *Figure 64.* .

There are a total of 8 outputs, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states. This information is held in the Connection Matrix Output RAM.

In using this macrocell, the user must take into consideration the critical timing required on all input and output signals. The timing waveforms and timing specifications for this macrocell are all measured relative to the input signals (which come into the macrocell on the Connection Matrix outputs) and on the outputs from the macrocell (which are direct connections to Connection Matrix inputs). The user must consider any delays from other logic and internal chip connections, including I/O delays, to ensure that signals are properly processed, and state transitions are deterministic.

The GPAK Designer development tools support user designs for the ASM macrocell at both the physical level and logic level. *Figure 64.* is a representation of the user design at the logical level, and *Figure 65.* shows the physical resources inside the macrocell. To best utilize this macrocell, the user must develop a logical representation of their desired state machine, as well as a physical mapping of the input and outputs required for the desired functionality.

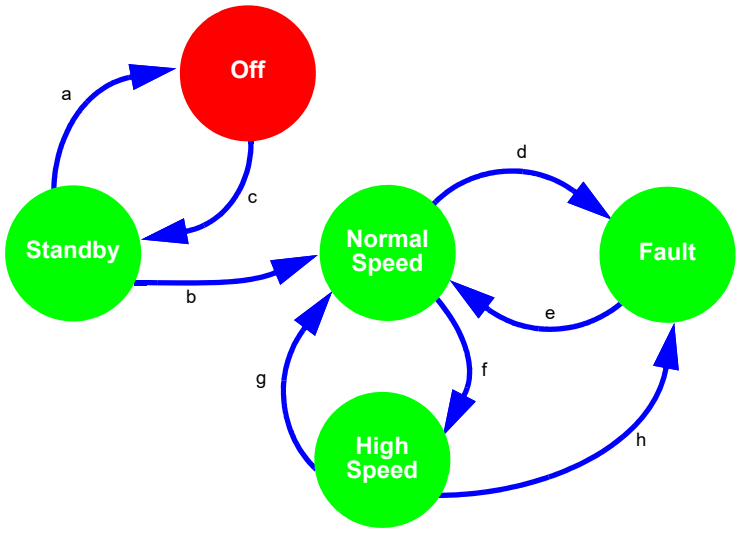


Figure 64. Asynchronous State Machine States and Transitions Diagram

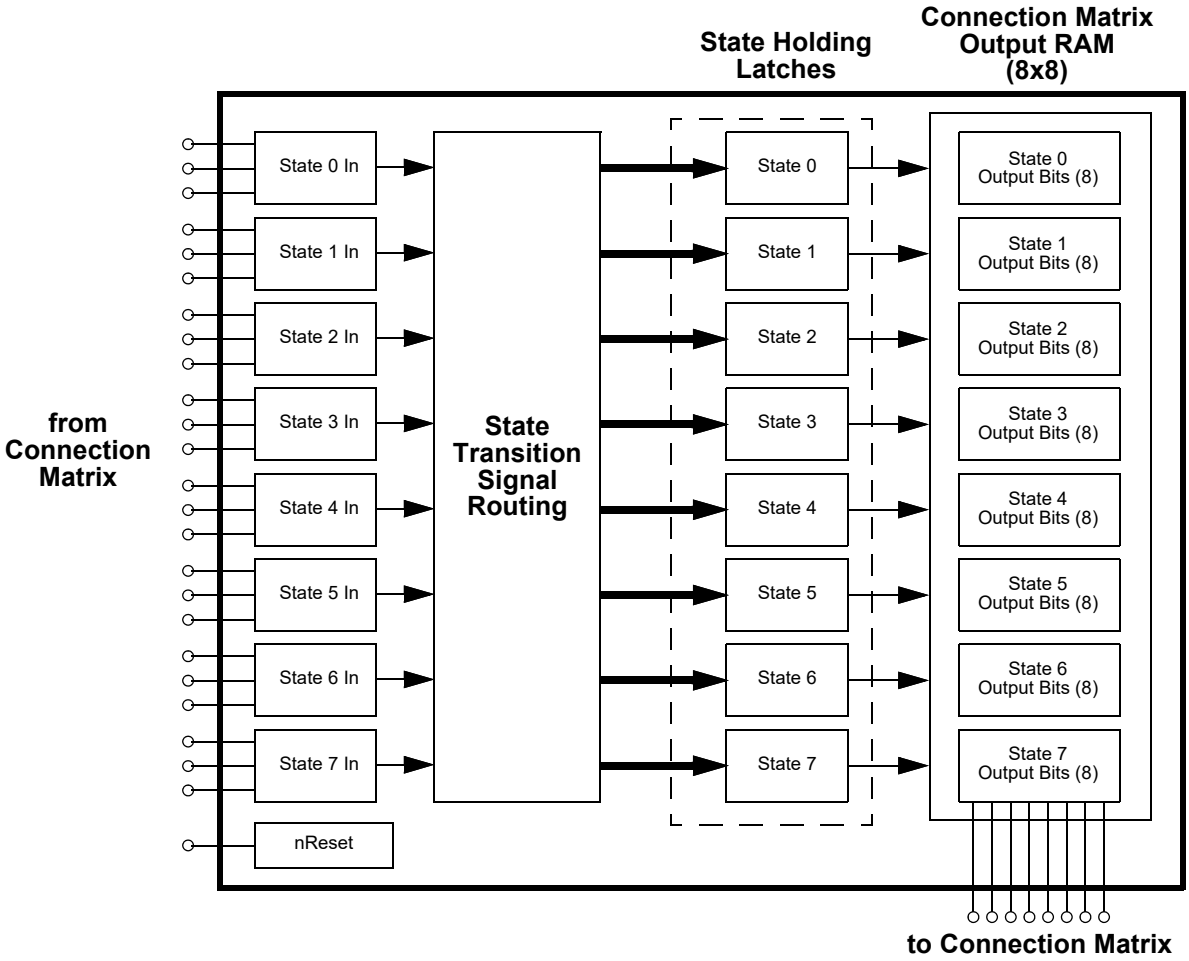


Figure 65. Asynchronous State Machine

20.2 ASM Inputs

The ASM macrocell has a total of 25 inputs which come from the Connection Matrix outputs. Of these 25 inputs, 24 are user selectable for driving general state transitions, and 1 is for driving a state transition to an Initial / Reset state.

There are a total of 24 inputs to the ASM macrocell for general state transitions, highlighted in red in *Figure 66.* . Each of these inputs is level sensitive, and active high. A high level input will trigger a state transition. Additionally, 8 out of the 24 inputs (one per state) has an option to select whether the input is rising edge sensitive, meaning that a rising level input signal will drive the user selected transition from one state to another, shown in *Figure 67.* .

These inputs are grouped so that each set of 3 inputs can drive a state transition **going into** a particular state. As an example, there are three inputs that can drive a state transition to State 1. This sets an upper bound on the number of transitions that the user can select going into a particular state to be 3, shown in *Figure 68.* .

There is no limitation on the number of transitions that can be supported coming out of a particular state, the user can select to have transitions going from a state to all other states, shown in *Figure 69.* .

The ASM macrocell also has a nReset input highlighted in blue in *Figure 66.* . This input is level sensitive and active low. An active signal on this input will drive an immediate state transition to the user-defined Initial / Reset state. The user can choose which state within the ASM Editor inside GPAK Designer is the initial state.

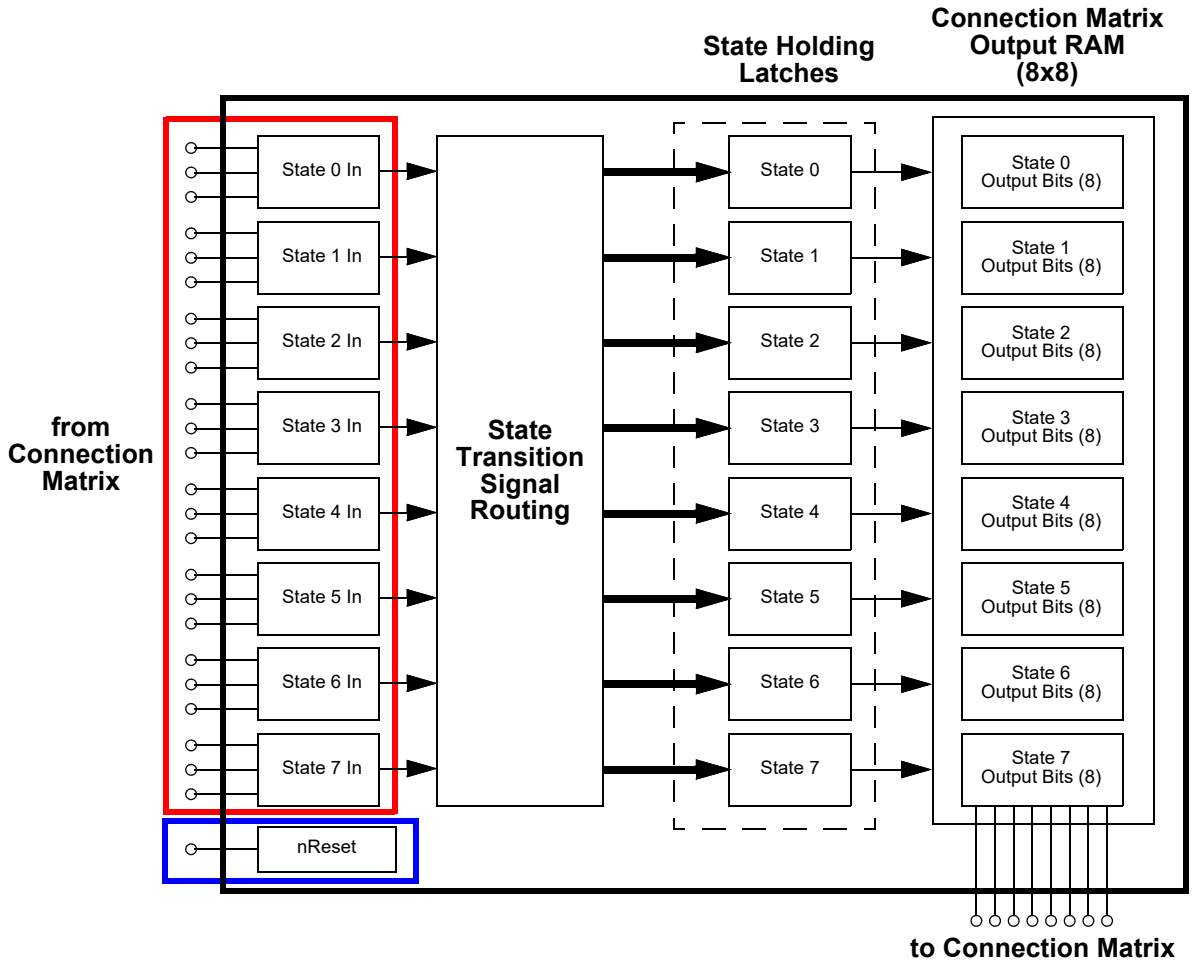


Figure 66. Asynchronous State Machine Inputs

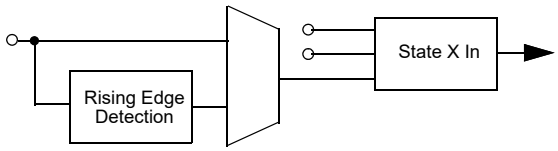


Figure 67. Rising Edge State Transition Selection (for each state X)

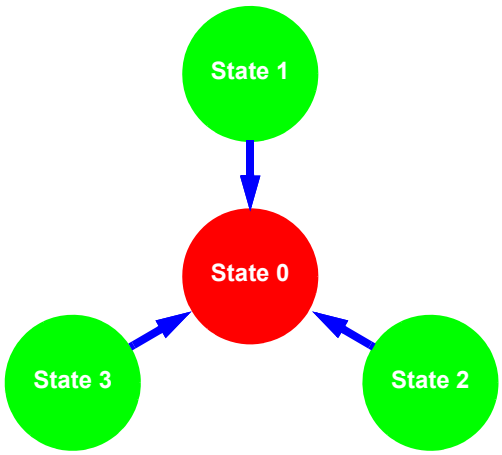


Figure 68. Maximum 3 State Transitions into Given State

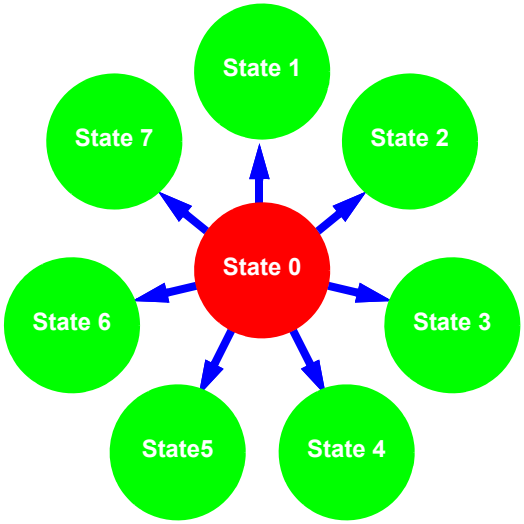


Figure 69. Maximum 7 State Transitions out of a Given State

20.3 ASM Outputs

There are a total of 8 outputs from the ASM macrocell, which go to the Connections Matrix inputs, and from there can be routed to other internal macrocells or pins. The 8 outputs are user defined for each of the possible 8 states, this information is held in the Connection Matrix Output RAM, shown in *Figure 70.* . The Connection Matrix Output RAM has a total of 64 bits, arranged as 8 bits per state. The values loaded in each of the 8 bits define the signal level on each of the 8 ASM macrocell outputs.

The ASM Editor inside the GPAK Designer software allows the user to make their selections for the value of each bit in the Connection Matrix Output RAM, which selects the level of the macrocell outputs based on the current state of the ASM macrocell, as shown in *Figure 65.* .

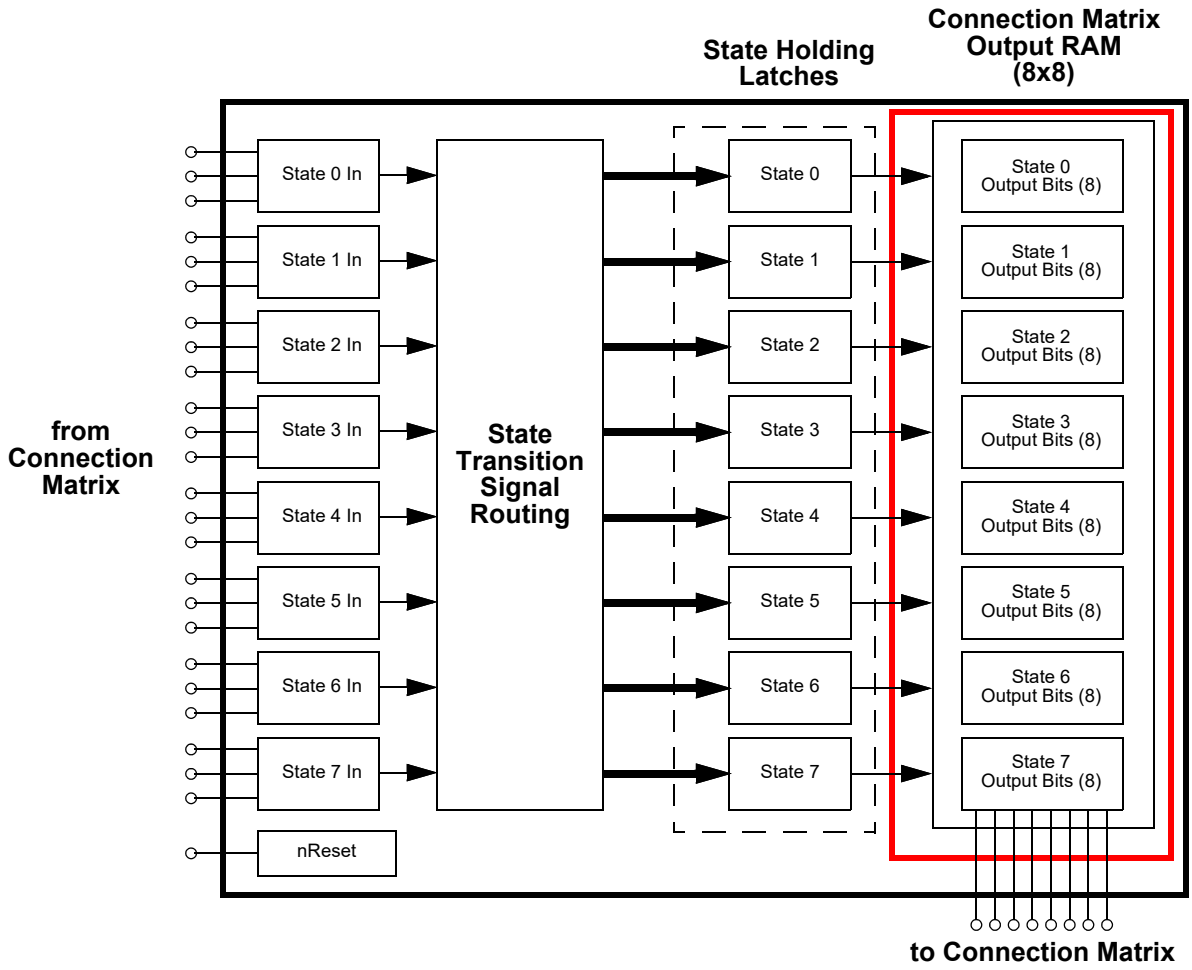


Figure 70. Connection Matrix Output RAM

Table 83. ASM Editor - Connection Matrix Output RAM

RAM								
State name	**Connection Matrix Output RAM**							
	OUT7	**OUT6**	**OUT5**	**OUT4**	**OUT3**	**OUT2**	**OUT1**	**OUT0**
State 0	0	0	0	0	0	0	0	1
State 1	0	0	0	0	0	0	1	0
State 2	0	0	0	0	0	1	0	0
State 3	0	0	0	0	1	0	0	0
State 4	0	0	0	1	0	0	0	0
State 5	0	0	1	0	0	0	0	0
State 6	0	1	0	0	0	0	0	0
State 7	1	0	0	0	0	0	0	0

Note: Each state output is user configurable.

20.4 Basic ASM Timing

The basic state transition timing from input on Matrix Connection output to output on Matrix Connection input is shown in *Figure 71.* and *Figure 72.* . The time from a valid input signal to the time that there is a valid change of state and valid signals being available on the state outputs is State Machine Output Delay Time (Tst_out_delay). The minimum and maximum values of Tst_out_delay define the differential timing between the shortest state transition (input on matrix output and output on matrix input) and the longest state transition (input on matrix output and output on matrix input).

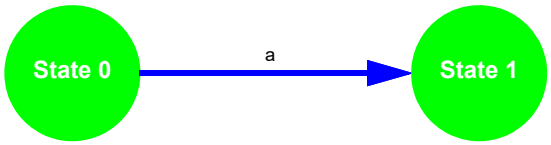


Figure 71. State Transition

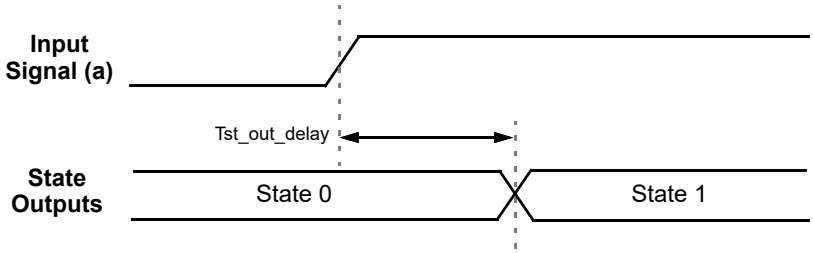


Figure 72. State Transition Timing

20.5 Asynchronous State Machines vs. Synchronous State Machines

It is important to note that this macrocell is designed for asynchronous operation, which means the following:

1. No clock source is needed, it reacts only to input signals
2. The input signals do not have to be synchronized to each other, the macrocell will react to the earliest valid signal for state transition.
3. This macrocell does not have traditional set-up and hold time specifications which are related to incoming clock, as this macrocell has no clock source.
4. The macrocell only consumes power while in state transition.

20.6 ASM Power Considerations

A benefit of the asynchronous nature of this macrocell is that it will consume power only during state transitions. Shown in *Figure 71.* and *Figure 73.* below, the current consumption of the macrocell will be a fraction of a µA between state transitions, and will rise only during state transitions. See Section *5.5 IDD Estimator* to find average current during state transitions.

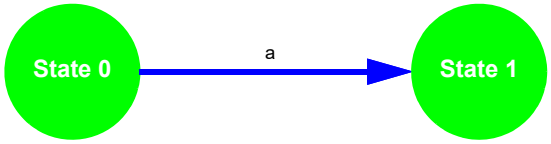


Figure 73. State Transition

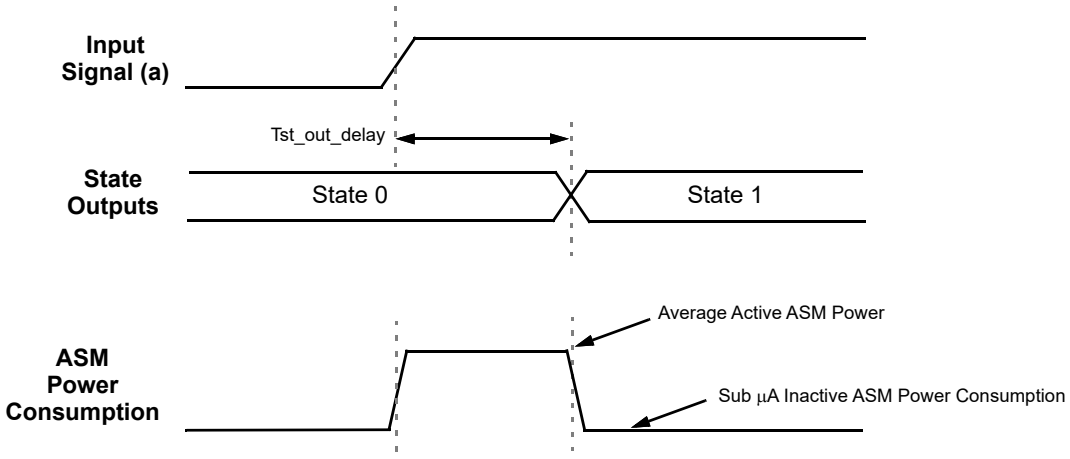


Figure 74. State Transition Timing and Power Consumption

20.7 ASM Logical vs. Physical Design

A successful design with the ASM macrocell must include both the logic level design as well as the physical level design. The GPAK Designer development software support user designs for the ASM macrocell at both the logic level and physical level. The logic level design of the user defined state machine takes place inside the ASM Editor. In the ASM Editor, the user can select and name states, define and name allowed state transitions, define the Initial / Reset state and define the output values for the 8 outputs in the Output RAM Matrix. The physical level design takes place in the general GPAK Designer window, and here the user makes connections for the sources for ASM input signals, as well as making connections for destinations for ASM output signals.

20.8 ASM Special Case Timing Considerations

20.8.1 State Transition Pulse Input Timing

All inputs to the ASM macrocell are level sensitive. If the input to the state machine macrocell for a state transition is a pulse, there is a minimum pulse width on the input to the state machine macrocell (as measured at the matrix input to the macrocell) which is guaranteed to result in a state transition shown in *Figure 75.* and *Figure 76.* . This pulse width is defined by the State Machine Input Pulse Acceptance Time (Tst_pulse). If a pulse width that is shorter than Tst_pulse is input to the state machine macrocell, it is indeterminate whether the state transition will happen or not. If a pulse that is rejected (invalid due to the pulse width being narrower than the guaranteed minimum of Tst_pulse), this will not stop a valid pulse on another state transition input that does meet minimum pulse width.

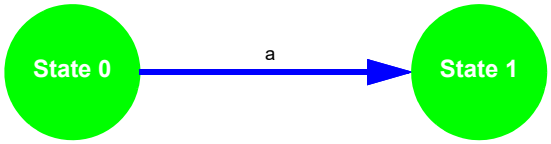


Figure 75. State Transition

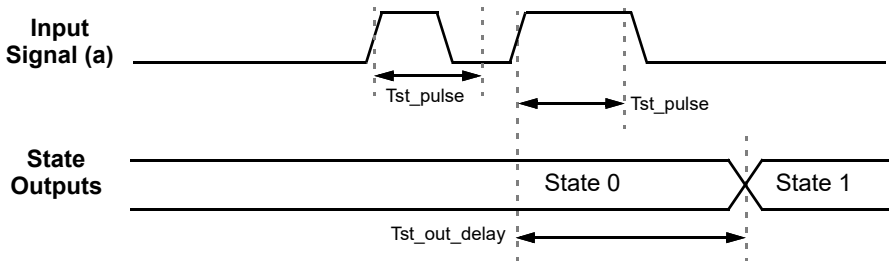


Figure 76. State Transition Pulse Input Timing

20.8.2 State Transition Competing Input Timing

There will be situations where two input signals can be valid inputs that will drive two different state transitions from a given state. In that sense, the two signals are “competing” (signals a and b in *Figure 77.*), and the signal that arrives sooner should drive the state transition that will “win”, or drive the state transition. If one signal arrives Tst_comp before the other one, it is guaranteed to win, and the state transition that it codes for will be taken, as shown in *Figure 78.* . If the two signals arrive within Tst_comp of each other, it will be indeterminate which state transition will win, but one of the transitions will take place as long as the winning signal satisfies the pulse width criteria described in the paragraph above, as shown in *Figure 79.* .

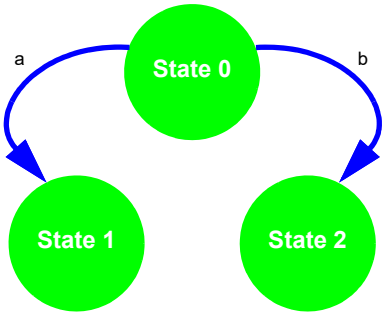


Figure 77. State Transition - Competing Inputs

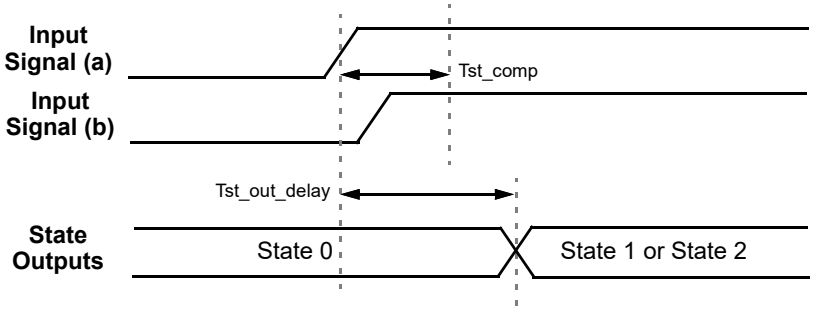


Figure 78. State Transition Timing - Competing Inputs Indeterminate

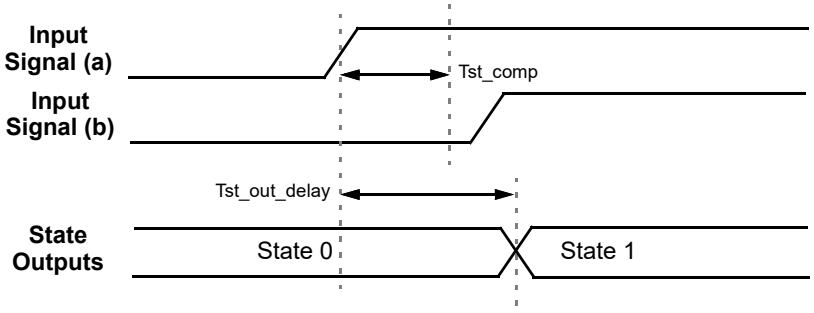


Figure 79. State Transition Timing - Competing Inputs Determinable

20.8.3 ASM State Transition Sequential Timing

It is possible to have a valid input signal for a transition out from a particular state be active before the state is active. If this is the case, the macrocell will only stay in that particular state for Tst_out_delay time before making the transition to the next state. An example of this sequential behavior is shown in *Figure 80.* and the associated timing is shown in *Figure 81.* .

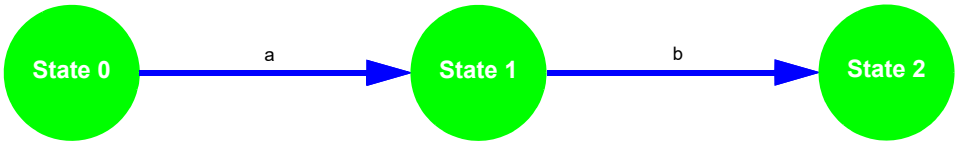


Figure 80. State Transition - Sequential

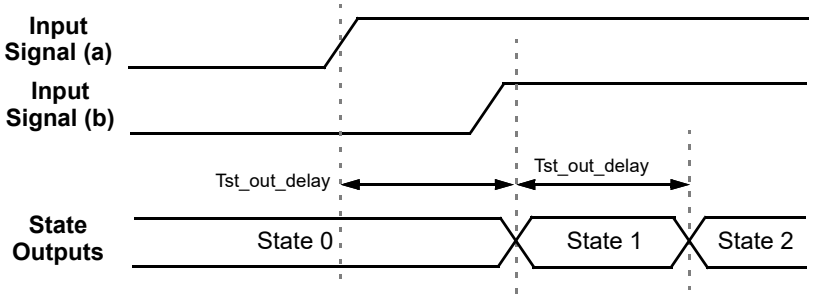


Figure 81. State Transition - Sequential Timing

20.8.4 State Transition Closed Cycling

It is possible to have a closed cycle of state transitions that will run continuously if there if there are valid inputs that are active at the same time. The rate at which the state transitions will take place is determined by Tst_out_delay. The example shown here in *Figure 82.* involves cycling between two states, but any number of two – eight states can be included in state transition closed cycling of this nature. *Figure 83.* shows the associated timing for closed cycling.

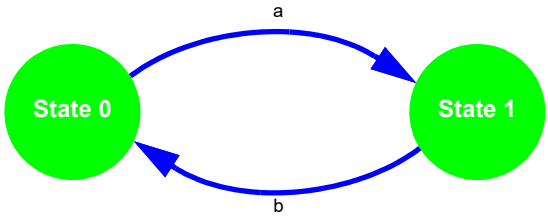


Figure 82. State Transition - Closed Cycling

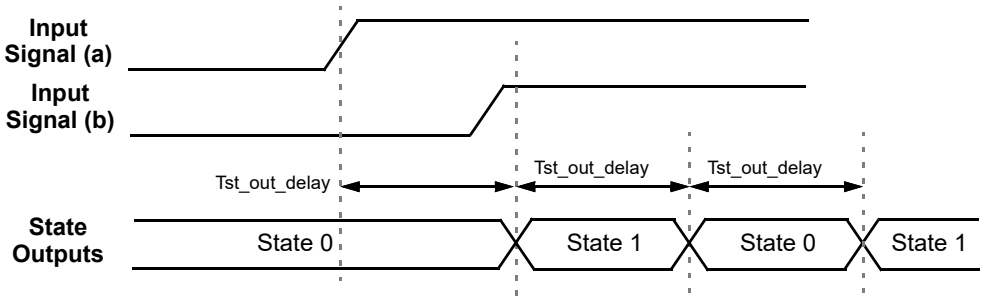


Figure 83. State Transition - Closed Cycling Timing

20.8.5 ASM State Transition Using Edge Detector Option

It is possible to use a rising edge detector option for state transitions. In this case, state transition happens on low to high signal transition as shown in *Figure 84.* and *Figure 85.* .

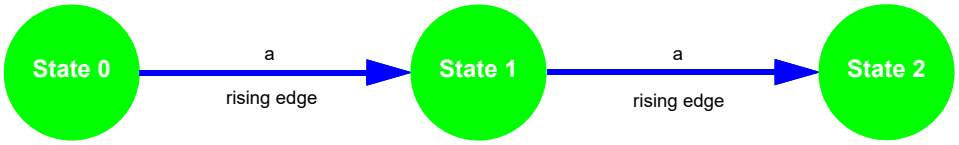


Figure 84. State Transition - Rising Edge Transition

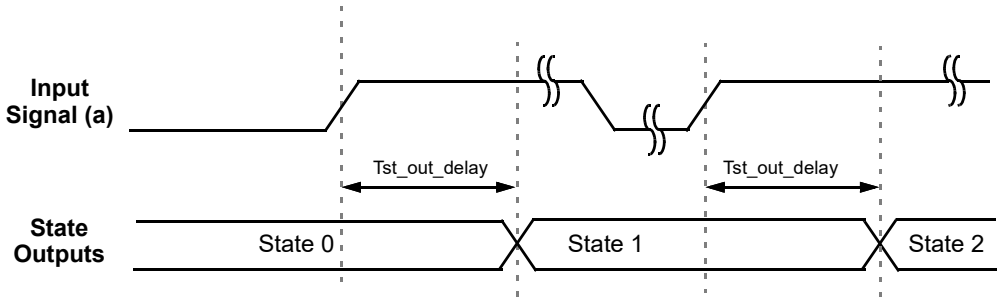


Figure 85. State Transition - Rising Edge Transition Timing

21.0 I²C Serial Communications Macrocell

21.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM). This information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The SLG46580/82/83 supports both 400 kHz (Fast-mode I²C bus) and 1 MHz (Fast-mode Plus I²C bus) I²C bus interfaces, which is selected by reg<1868>.

The user has the flexibility to control read access and write access via registers bits reg<1832> and reg<1871>. See section *21.4.7.1 Register Read/Write Protection* for more details on I²C read/write memory protection.

Note: GreenPAK I²C is fully compatible with standard I²C protocol.

21.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in *Figure 86.* . After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10,A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/$\overline{W}$ bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46580/82/83 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9 and A8) will be "0" for all commands to the SLG46580/82/83.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. *Figure 86.* shows this basic command structure.

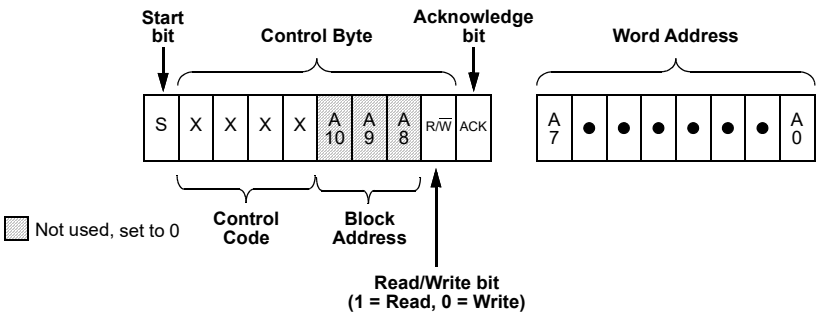


Figure 86. Basic Command Structure

21.3 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in *Figure 87.* . Timing specifications can be found in the AC Characteristics section.

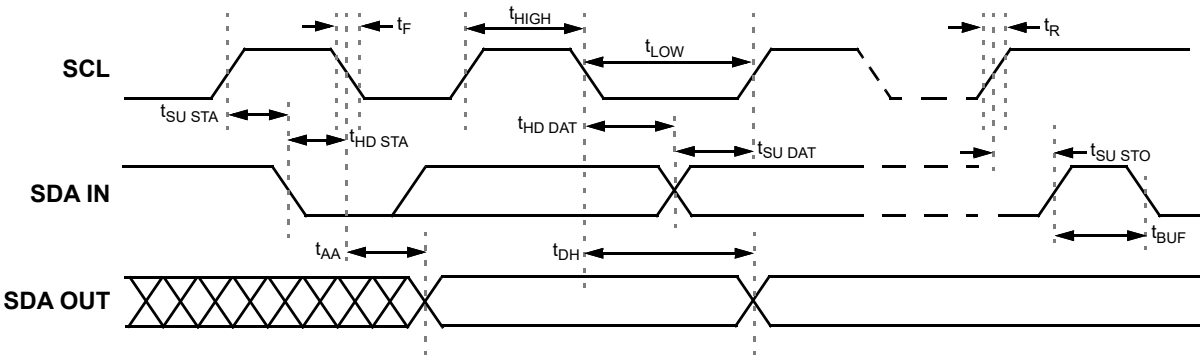


Figure 87. I²C General Timing Characteristics

21.4 I²C Serial Communications Commands

21.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits] and the R/$\overline{W}$ bit (set to “0”), are placed onto the I²C bus by the Master. After the SLG46580/82/83 sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46580/82/83 where the data byte is to be written. After the SLG46580/82/83 sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46580/82/83 again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46580/82/83 generates the Acknowledge bit.

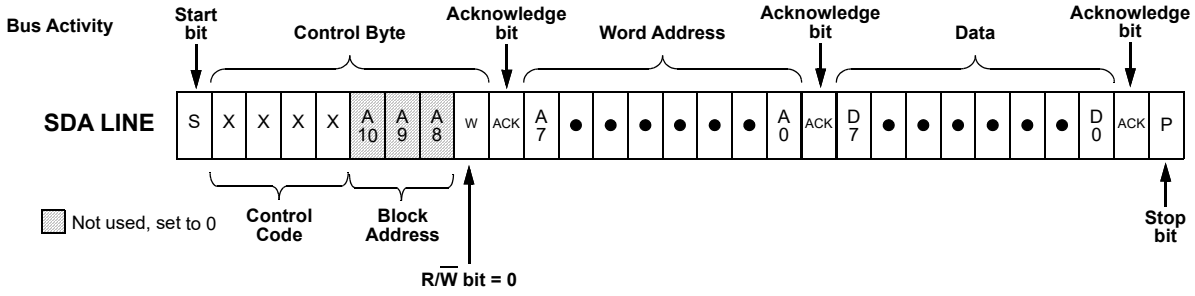


Figure 88. Byte Write Command, R/$\overline{W}$ = 0

21.4.2 Sequential Write Command

The write Control Byte, Word Address and the first data byte are transmitted to the SLG46580/82/83 in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Master continues to transmit data bytes to the SLG46580/82/83. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46580/82/83 generates the Acknowledge bit.

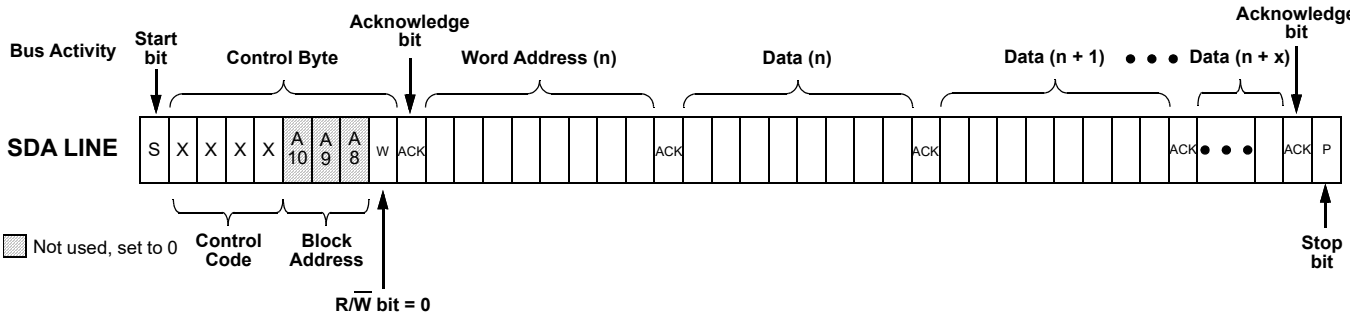


Figure 89. Sequential Write Command, R/$\overline{W}$ = 0

21.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Write or Random Read (which contains a write control byte) writes or reads data up to address n, the address pointer would get incremented to n+1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n+1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/$\overline{W}$ bit = “1”. The SLG46580/82/83 will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

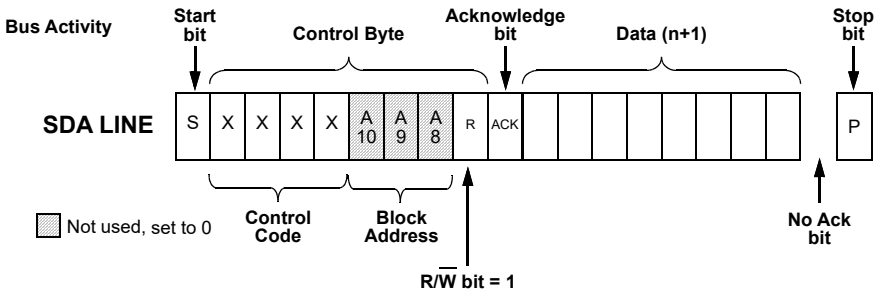


Figure 90. Current Address Read Command, R/$\overline{W}$ = 1

21.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/$\overline{W}$ bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Master issues a second control byte with the R/$\overline{W}$ bit set to “1”, after which the SLG46580/82/83 issues an Acknowledge bit, followed by the requested eight data bits.

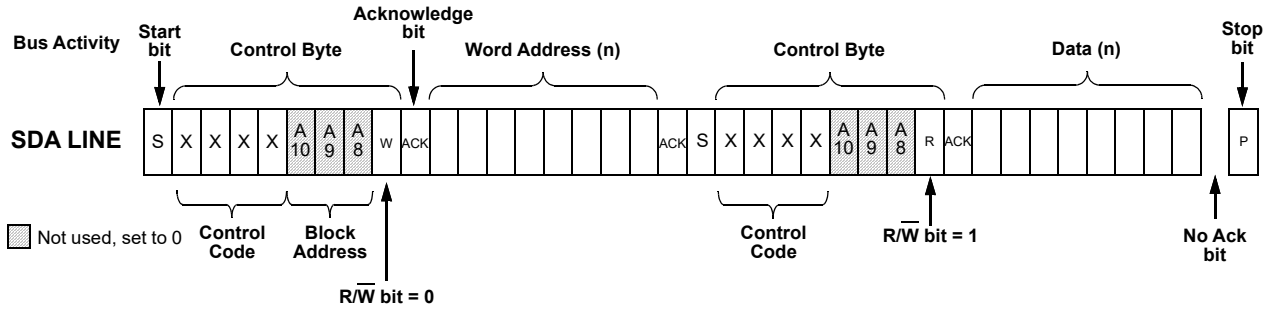


Figure 91. Random Read Command

21.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Current Address Read or Random Read command, except that once the SLG46580/82/83 transmits the first data byte, the Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

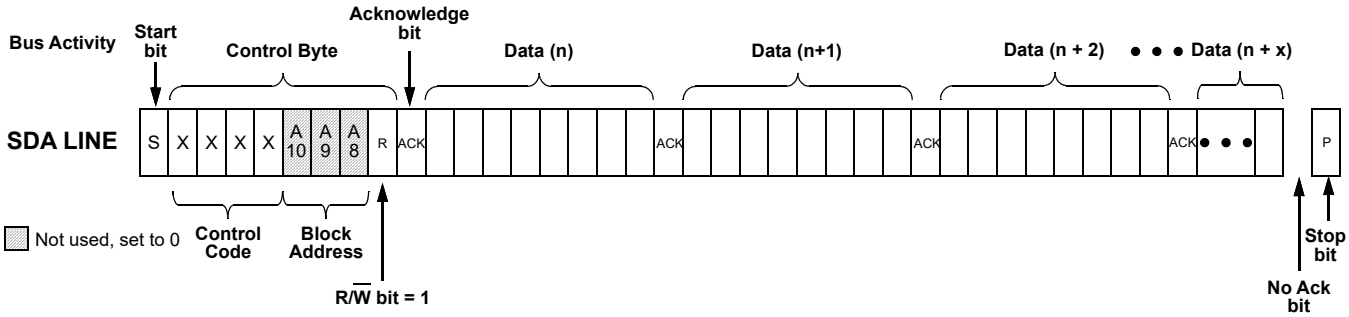


Figure 92. Sequential Read Command

21.4.6 I²C Serial Command Address Space

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46580/82/83 are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9 and A8) will be “0” for all commands to the SLG46580/82/83.

21.4.7 I²C Serial Command Register Map

21.4.7.1 Register Read/Write Protection

There are several read/write protect modes for the design sequence from being corrupted or copied. See *Table 84* for details.

Table 84: Read/Write Protection Options

Configurations	Protection Modes Configuration						Data Output From	Register Address (HEX)
	Unlocked	Locked for read bits	Locked for write bits	Locked for write all bits	Locked for read and write bits	Locked for read bits and write all bits		
	Register [1832]=0 Register [1871]=0 Register [1870]=0	Register [1832]=1 Register [1871]=0 Register [1870]=0	Register [1832]=0 Register [1871]=1 Register [1870]=0	Register [1832]=0 Register [1871]=x Register [1870]=1	Register [1832]=1 Register [1871]=1 Register [1870]=0	Register [1832]=1 Register [1871]=x Register [1870]=1		
I²C Serial Reset Command	R/W	R/W	R/W	R	R/W	R	Memory	CF,b'6
Outputs Latching During I²C Write	R	R	R	R	R	R	Memory	CF,b'7
Connection Matrix Virtual Inputs	R/W	R/W	R/W	R	R/W	R	Macrocell	F4
Configuration Bits for All Macrocells (IO Pins, Combination Function Macrocells, ASM, etc.)	R/W	W	R	R	-	-	Memory	80-BF
Macrocells Inputs Configuration (Connection Matrix Outputs)	R/W	W	R	R	-	-	Memory	00-67
LDO settings, RAM, ACMP settings, DLY/ CNT control data, RTC settings	R/W	R/W	R/W	R	R/W	R		6E, D0-E3; CF,b'0-b'2; C6-CE; C0-C4; 75-7F
Macrocells Output Values (Connection Matrix Inputs)	R	R	R	R	R	R	Macrocell	F0-F3; F5-F7
Counter Current Value	R	R	R	R	R	R	Macrocell	70-71
ASM Current State	R	R	R	R	R	R	Macrocell	EF
Silicon Identification Service Bits	R	R	R	R	R	R	Memory	E8
Pattern ID0/1	R/W	R/W	R/W	R	R/W	R	Memory	E6, E4
I²C Control Code	R	R	R	R	R	R	Memory	E9,b'0-b3;
Protection Read Configuration (Register [1832])	R	R	R	R	R	R	Memory	E5,b'0
Protection Write Configuration (Register [1870], Register [1871])	R	R	R	R	R	R	Memory	E9,b'6-b'7

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, ASM current state, connection matrix, and connection matrix virtual inputs. The I^2C write does not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allow identifying silicon family, its revision, etc.

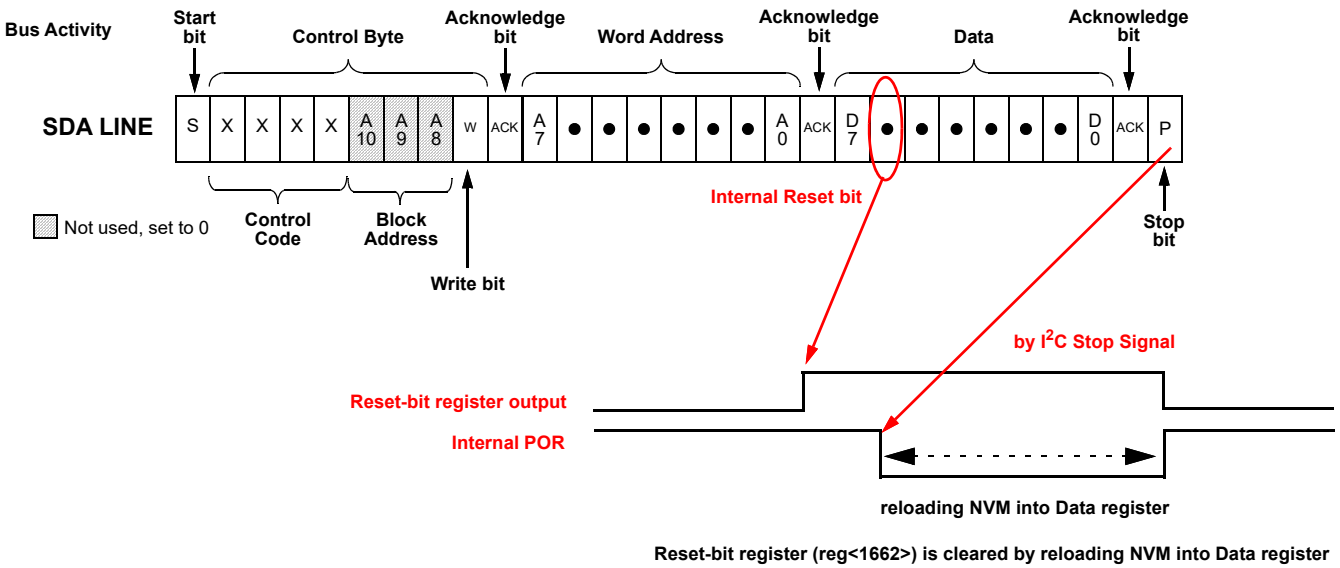
Note 1: If reg<1663> = 1, all outputs are latched while inputs and internal macrocells retain their status during I^2C write.

Note 2: Any write commands that come to the device via I^2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM.

See Section *25.0 Appendix A - SLG46580/82/83 Register Definition* for detailed information on all registers

21.4.7.2 I^2C Serial Reset Command

If I^2C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting reg<1662> I^2C reset bit to “1”, which causes the device to re-enable the Power On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of reg<1662> will be set to “0” automatically. The timing diagram shown below illustrates the sequence of events for this reset function.



1) I²C write with reg<1662>=1 (I²C reset bit with reloading NVM into Data register)
2) POR go to LOW and reloading NVM into Data register start after "STOP" of I²C
3) POR go to HIGH after reloading NVM into Data register

Figure 93. Reset Command Timing

21.4.7.3 Reading Counter Data via I²C

The current count value in the RTC counter and two counters in the device can be read via I²C. The counters that have this additional functionality are 8-bit counters CNT2 and CNT4.

21.4.7.4 User RAM and OTP Memory Array

There are eight bytes of RAM memory that can be read and written remotely by I²C commands. The initial contents of this memory space can be selected by the user, and this information will be transferred from OTP memory to the RAM memory space during the power-up sequence. The lowest order byte in this array (User Configurable RAM/OTP Byte 0) is located at I²C address 0xD8, and the highest order byte in this array is located at I²C address 0xDF.

Table 85. RAM Array Table

I2C Address (hex)	Highest Bit Address	Lowest Bit Address	Memory Byte
D8	1735	1728	User Configurable RAM/OTP Byte 0
D9	1743	1736	User Configurable RAM/OTP Byte 1
DA	1751	1744	User Configurable RAM/OTP Byte 2
DB	1759	1752	User Configurable RAM/OTP Byte 3
DC	1767	1760	User Configurable RAM/OTP Byte 4
DD	1775	1768	User Configurable RAM/OTP Byte 5
DE	1783	1776	User Configurable RAM/OTP Byte 6
DF	1791	1784	User Configurable RAM/OTP Byte 7

22.0 SLG46580 Low Dropout Regulators

22.1 LDO Regulator Description

The SLG46580 comes with four low dropout regulators each rated at 150 mA. Each LDO regulator has 3 modes which are: HP MODE is the standard active mode supporting full 150 mA output; LP MODE is a low power mode with maximum 100 µA and finally Power Switch Mode in which the LDO regulator ceases to regulate and the Regulator MOSFET is turned on as a power switch, passing the voltage applied to VIN directly to VOUT.

The LDO regulators are paired together with LDO0 and LDO1 sharing the same V_{IN} called LDO0/1 VIN, likewise LDO2 and LDO3 share the same V_{IN} called LDO2/3 VIN.

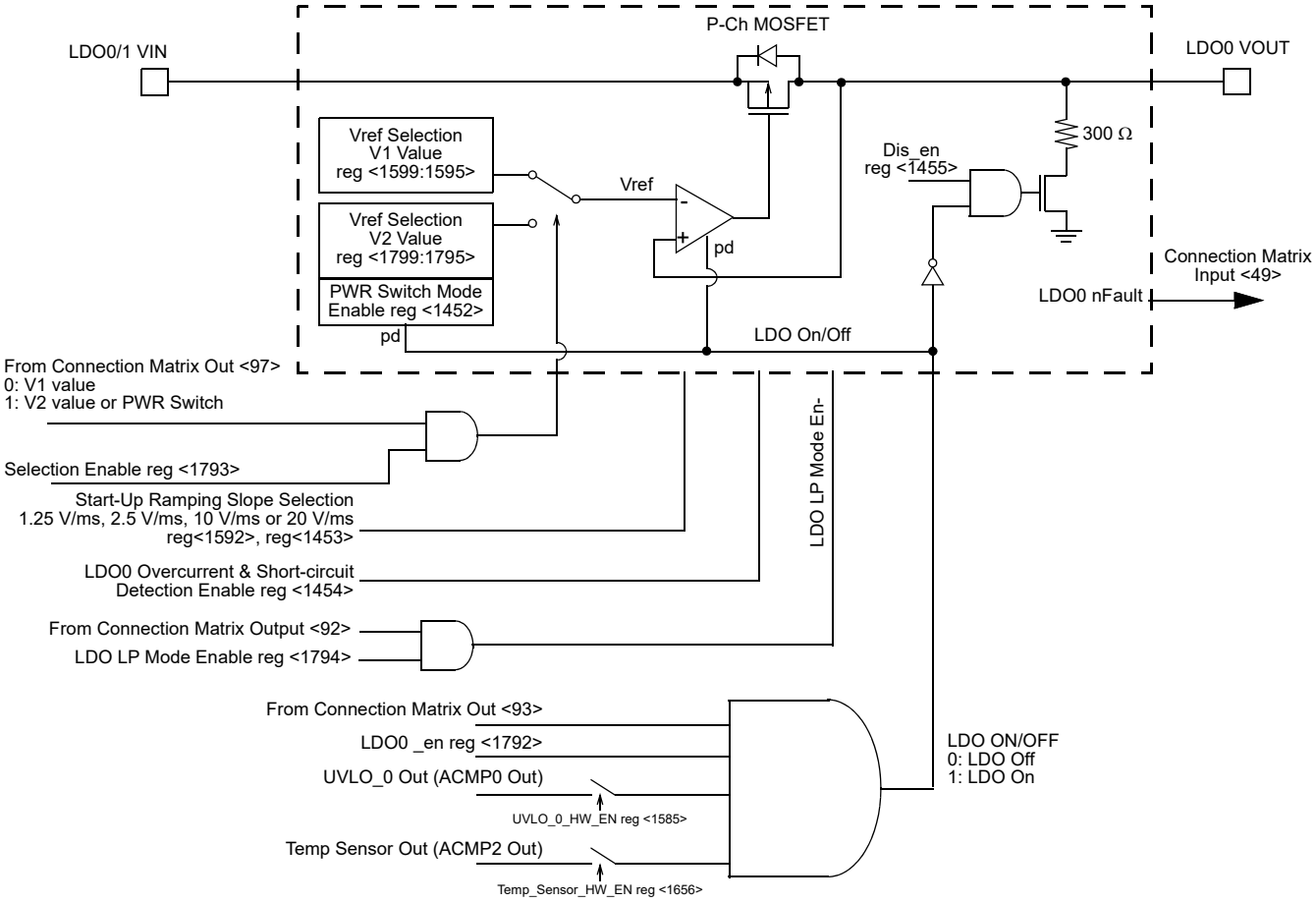


Figure 94. LDO0 Regulator Block Diagram

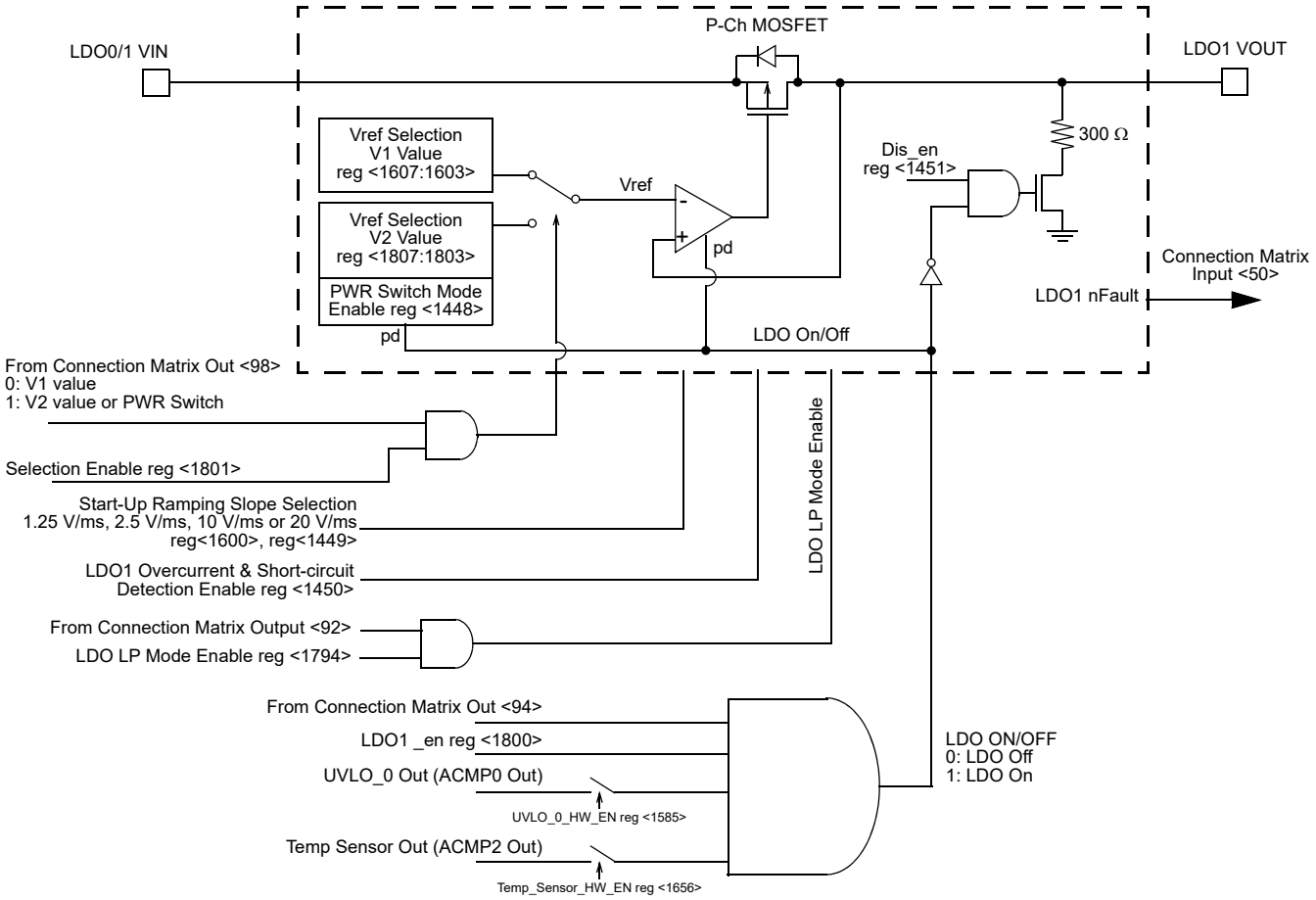


Figure 95. LDO1 Regulator Block Diagram

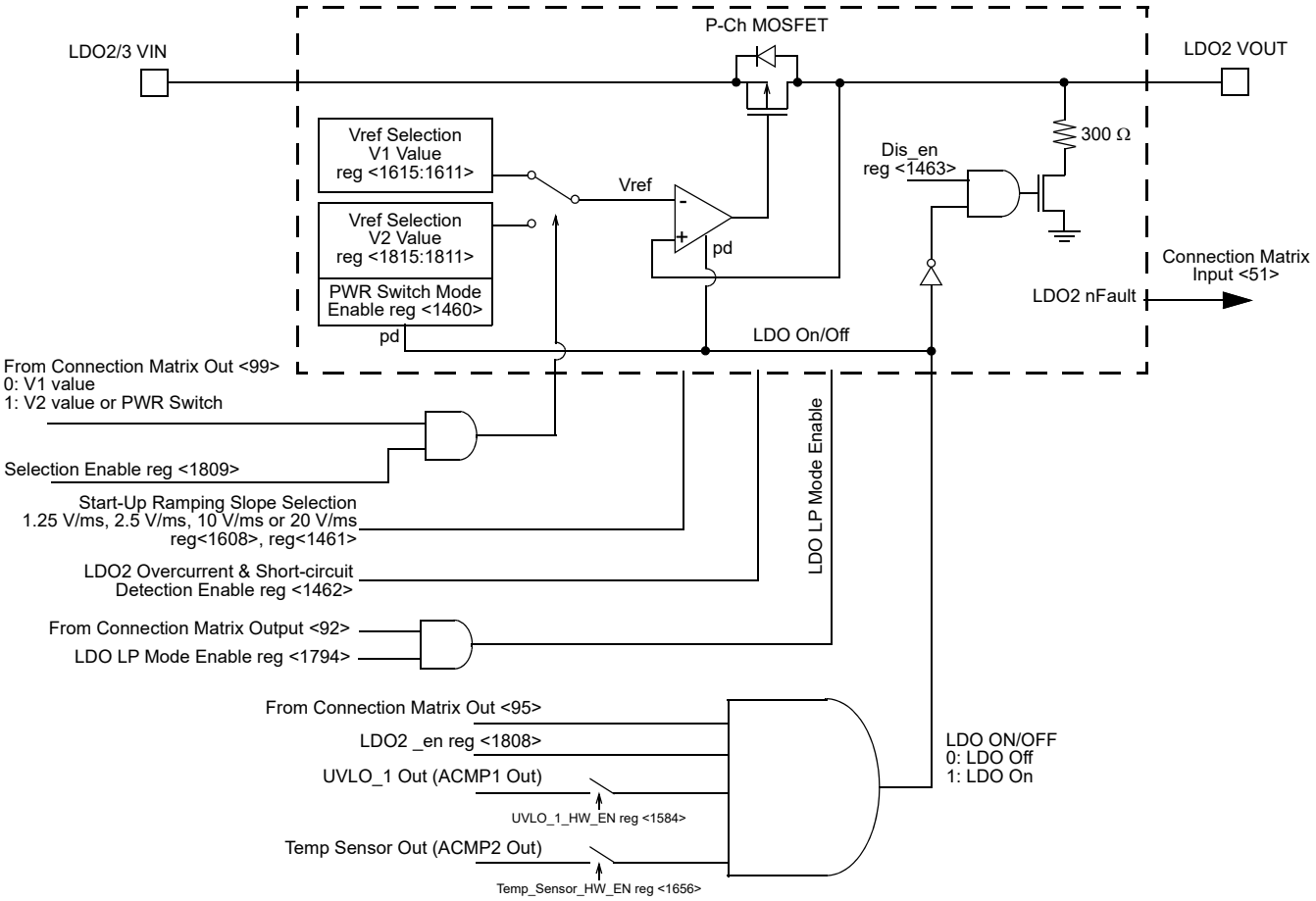


Figure 96. LDO2 Regulator Block Diagram

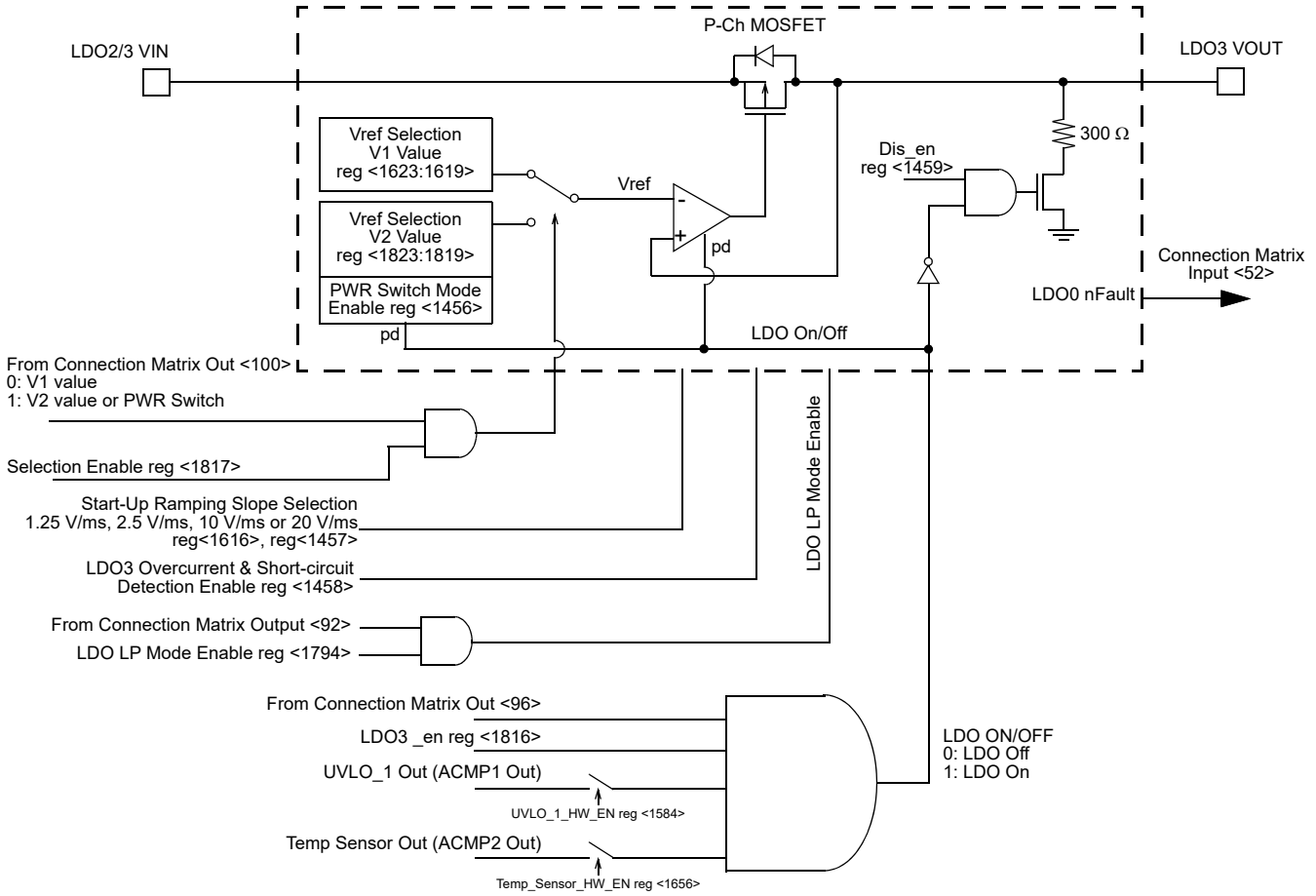


Figure 97. LDO3 Regulator Block Diagram

22.1.1 Voltage Selection

Each LDO has access to 32 voltage levels derived from a bandgap voltage reference.

It is possible to select two different output voltage levels (V1 and V2) per LDO. The voltage levels can be changed through the Connection Matrix, after V1/V2 selection is enabled through the register bit. It is also possible to change the LDO output voltage level through the I^2C by writing the corresponding LDO output voltage selection number according to *Table 86*.

Table 86. LDO Output Voltage Selection

Selection #	LDO VOUT (V)	LDO Min. VIN (V)	Min. VDD (V)
0	0.90	2.30	2.30
1	1.00	2.30	2.30
2	1.05	2.30	2.30
3	1.10	2.30	2.30
4	1.20	2.30	2.30
5	1.25	2.30	2.30
6	1.35	2.30	2.30
7	1.50	2.30	2.30

Table 86. LDO Output Voltage Selection (continued)

Selection #	LDO VOUT (V)	LDO Min. VIN (V)	Min. VDD (V)
8	1.67	2.30	2.30
9	1.80	2.30	2.30
10	1.90	2.30	2.30
11	2.00	2.30	2.30
12	2.10	2.40	2.80
13	2.20	2.50	2.80
14	2.30	2.60	2.80
15	2.40	2.70	2.80
16	2.50	2.80	2.80
17	2.60	2.90	3.00
18	2.70	3.00	3.00
19	2.80	3.10	3.30
20	2.90	3.20	3.30
21	3.00	3.30	3.30
22	3.10	3.40	3.60
23	3.20	3.50	3.60
24	3.30	3.60	3.60
25	3.40	3.70	3.90
26	3.50	3.80	3.90
27	3.60	3.90	3.90
28	4.00	4.30	4.50
29	4.10	4.40	4.50
30	4.20	4.50	4.50
31	4.35	4.65	4.65

Note1: The combination of VIN, VDD and VOUT must satisfy the rule: VDD ≥ VIN ≥ VOUT + 0.3 V.
Note2: VIN and VDD should not exceed 5.5 V.

22.1.2 LDO HP Mode Operation

HP Mode is the standard active LDO mode with a 150 mA per LDO output loading capability.*VDD ≥ 2.3 V.*

A high level signal should be applied to Connection Matrix Outputs <93>, <94>, <95> and <96> together with the register enable bits <1792>, <1800>, <1808> and <1816> to enable LDO0, LDO1, LDO2 and LDO3, respectively. The LDO requires a wait time to enable analog circuitry before the LDO output starts to rise with the desired ramping slope selected through the register bits.

22.1.3 LDO LP Mode Operation

It is possible to enable ultra-low power LP Mode in which max output loading is 100 μA and quiescent current consumption is ~2μA per LDO (without load). LP Mode can be enabled through Connection Matrix Output <92> together with the register enable bit <1794> and have an impact for all LDOs enabled in the SLG46580 chip.

22.1.4 Power Switch Mode Operation

Each LDO has an additional option to operate in power switch mode. In this case, all LDO related circuitry will be disabled. The quiescent current consumption is ~1 μA in power switch mode.

The power switch option is available in each LDO and can be used instead of the VOUT2 output voltage level selected by the following register bits: reg <1452> for LDO0, reg <1448> for LDO1, reg <1460> for LDO2, and reg <1456> for LDO3.

The Power Switch Mode can be selected by applying a high-level signal to the Connection Matrix Output <97>, <98>, <99>, and <100> for LDO0, LDO1, LDO2 and LDO3 respectively.

22.2 Over-Current Limit and Short-Circuit Detection

Each LDO has an option to enable OCL (Over-Current Limit, if the output current rises above 189 mA) and SCD (Short-Circuit Detection, if output voltage drops below 0.5 V with the current limited by 20 mA).

These options are available for the LDO in HP Mode only. The nFAULT signal per LDO will generate a low-level signal to the connection matrix input when the short-circuit is detected.

Note: OCL and SCD are disabled by default, reg <1454> for LDO0, reg <1450> for LDO1, reg <1462> for LDO2, and reg <1458> for LDO3.

22.3 LDO Efficiency

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows:

$$\eta_{EF} = \frac{I_{OUT} \times V_{OUT}}{(I_{OUT} + I_Q) \times V_{IN}} \times 100$$

where:

η_{EF} = LDO efficiency, in percents (%)
I_{OUT} = Output current, in Amps (A)
V_{OUT} = Output voltage, in Volts (V)
I_Q = Quiescent current, in Amps (A)
V_{IN} = Input voltage, in Volts (V)

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for efficiency:

$$PD = V_{DO} \times I_{OUT}$$

where:

PD = Power Dissipation, in Watts (W)
V_{DO} = Drop out voltage, in Volts (V)
I_{OUT} = Output current, in Amps (A)

The Input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

22.4 LDO Thermal Considerations

The thermal limitations must be taken into consideration during regulator design. The SLG46580 is rated at 0.6 W of power dissipation at 85 °C ambient and 0.8 W of power dissipation at 70 °C ambient. If a regulator is connected to 5.0 V and then is programmed to output 1.8 V, the power dissipation at 150 mA is 0.48 W or almost the entire thermal budget of the SLG46580. In this case we recommend putting an external resistor between the application's power source (battery or wall power) and the SLG46580's LDO VIN to help distribute the thermal load. A 10 Ω, ¼ watt resistor would cut the IC thermal dissipation about in half without impacting overall performance. However, because the LDO VIN voltage is shared between two LDOs the resistor should be properly selected for the higher of the desired LDO output voltages.

If is possible to use the temperature sensor together with ACMP2 to automatically shut down all LDOs if the die temperature rises to a predetermined threshold level. The LDOs will automatically restart when the chip has cooled down within the hysteresis range for ACMP2. Other temperature shut off levels may be achieved by incorporating the temperature sensor into ACMP3's input.

Note: LDO Thermal Protection is disabled by default, reg <1656>.

22.5 Soft Start Function (SS)

Table 87 to *Table 90* show the bit settings and slew rate selection options for each LDO.

Table 87. LDO0 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1453>	reg <1592>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 88. LDO1 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1449>	reg <1600>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 89. LDO2 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1461>	reg <1608>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 90. LDO3 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1457>	reg <1616>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

22.6 ACMPs: Under Voltage Lockout capability, Power Good

LDO0/1 VIN and LDO2/3 VIN are sensed by ACMP0 and ACMP1 respectively as one of their input options. The sense line can be divided by 2, 3, or 4 for the common mode voltage input limitation of ACMP0 and ACMP1. ACMP0 and ACMP1 can be set to the customers desired under voltage lockout (UVLO) level. The undervoltage lockout can be set by either hardware connection to control the LDO or through the Connection Matrix. The UVLO_0 hardware connection to the LDO can be enabled by reg <1585>. for LDO0 and LDO1, and UVLO_1 by reg <1584> for LDO2 and LDO3.

Note 1: ACMP0 needs to be properly configured to use UVLO_0 for LDO0 and LDO1. ACMP1 needs to be properly configured to use UVLO_1 for LDO2 and LDO3.

A lockout level below 2.3 V is not useful as the lowest acceptable power supply voltage is 2.3 V.

ACMP3 has a selectable input from the output of LDO0 or 2 for the purpose of a power good.

The ACMPs connection to VDD may be reused for the purpose stated above.

Note 2: LDO Under Voltage Lockout is disabled by default.

22.7 Regulator Stability Considerations

The regulators are only stable in HP MODE when a 2 µF (min) capacitor or greater is attached to each LDOs V_{OUT}. The recommended capacitor is a 2 µF (min) X5R capacitor rated for 6 V or greater. The X5R capacitor varies with temperature, DC bias voltage, and process; however the SLG46580 LDOs have taken this variance into consideration when recommending the 2 µF (min) X5R from -40 to +85C.

22.8 LDO Regulator Cold Start up

When the SLG46580 VDD goes high, then the fastest that an LDO regulator can begin to power up under the control of the SLG46580 is ~2 ms typical, and 3 ms max.

During this cold start period the P Channel MOSFET gate is 0V so the MOSFET is automatically turning on if LDO VIN is also coming up.

22.9 LDO Regulator Hot Start up

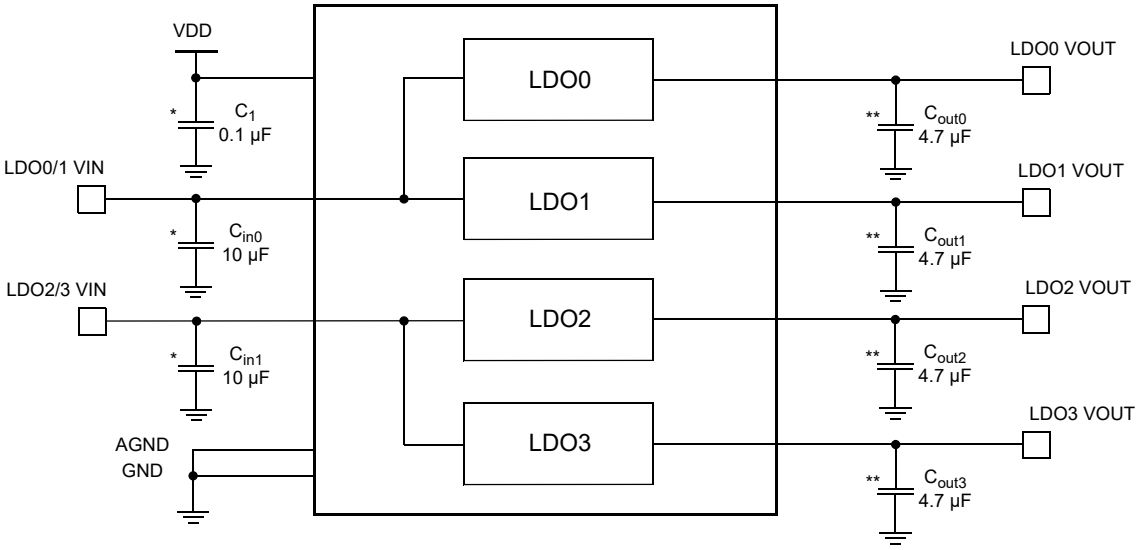
When the SLG46580 VDD is already high, then the fastest than an LDO regulator can begin to power up is around 500 µs + soft start ramping.

22.10 Discharge Resistors

Each LDO comes with a program selectable 300 Ohm discharge resistor. For applications that desire a power rail to be brought to near zero during shutdown, then the 300 Ohm discharge resistor is useful. For applications that desire to keep remaining charge on a V_{OUT} capacitor the discharge resistor should not be selected.

The discharge resistor is set by reg <1455> for LDO0, reg <1451> for LDO1, reg <1463> for LDO2, and reg <1459> for LDO3.

22.11 SLG46580 LDO Typical Application Circuit



Note: All internal connections shown inside the SLG46580 are hardwired connections that cannot be changed.
Note: Keep decoupling capacitors close to the SLG46580.*
*Note**: Keep output capacitors close to the SLG46580. Long distances negatively impact LDO stability.*

Figure 98. SLG46580 LDO Typical Application Circuit

22.12 SLG46580 LDO Typical Performance

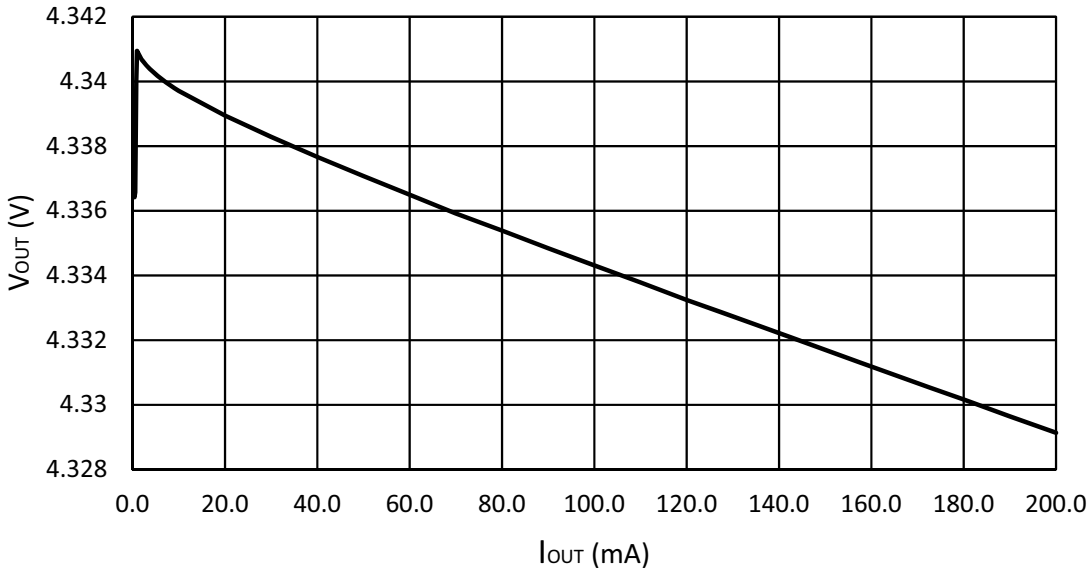


Figure 99. SLG46580 LDO Load Regulation, HIGH POWER Mode, T = 25°C, V_{DD} = 5V, VOUT = 4.35 V

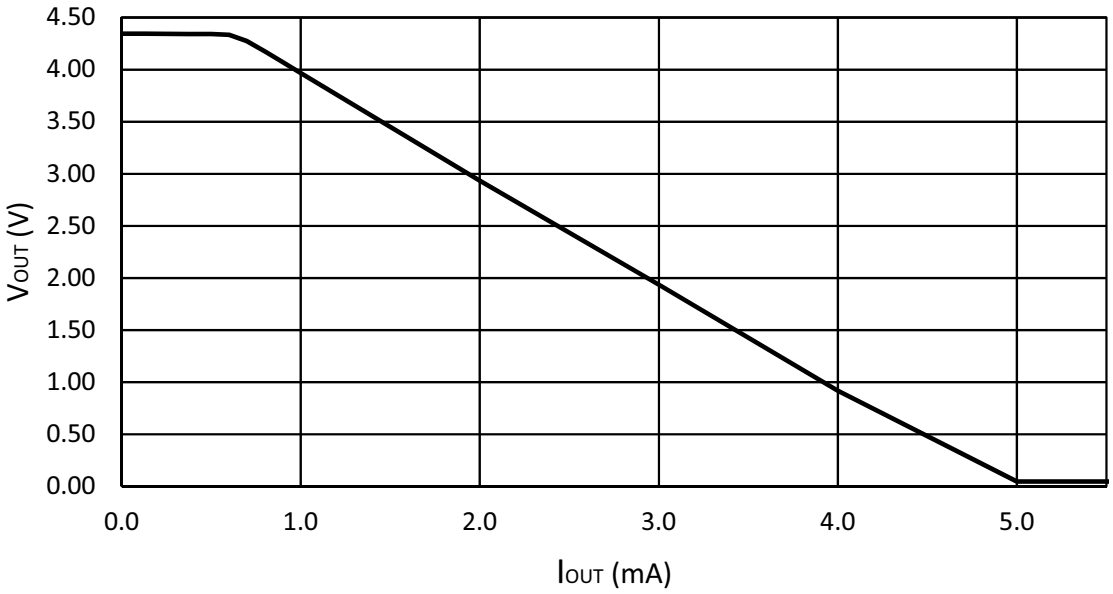


Figure 100. SLG46580 LDO Load Regulation, LOW POWER Mode, T = 25°C, V_{DD} = 5V, VOUT = 4.35 V

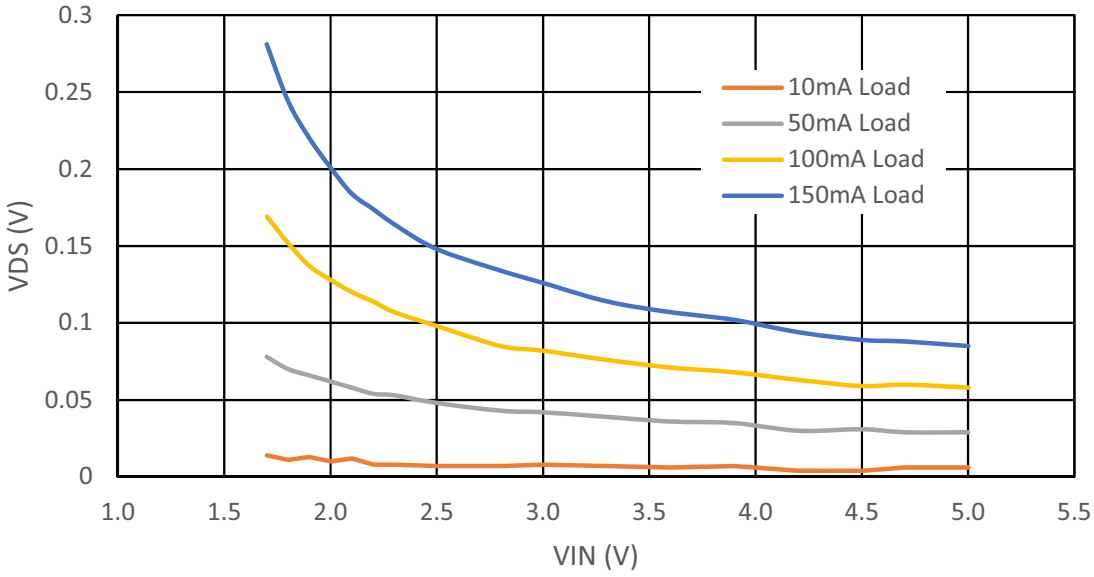


Figure 101. SLG46580 LDO Dropout Voltage vs. VIN

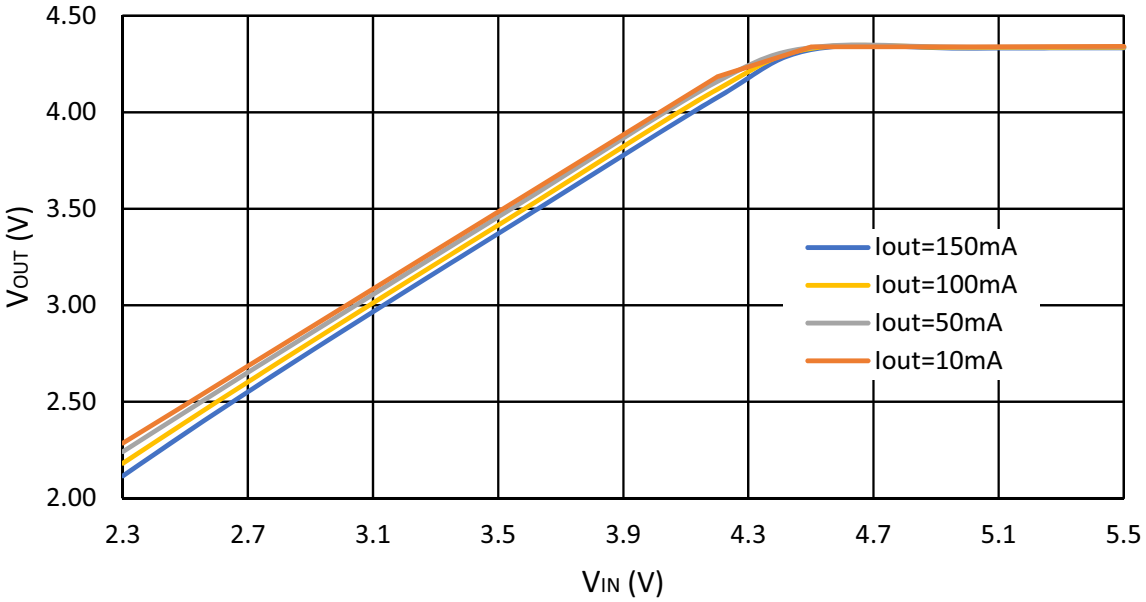


Figure 102. SLG46580 LDO High Power Mode VOUT vs. VIN, T = 25°C, V_{DD} = 5V

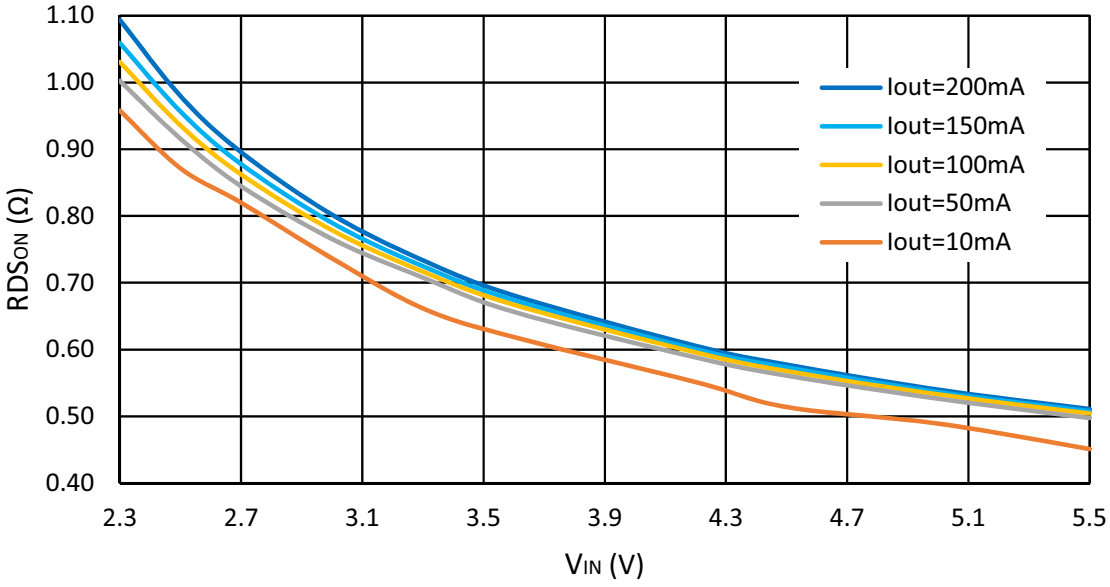


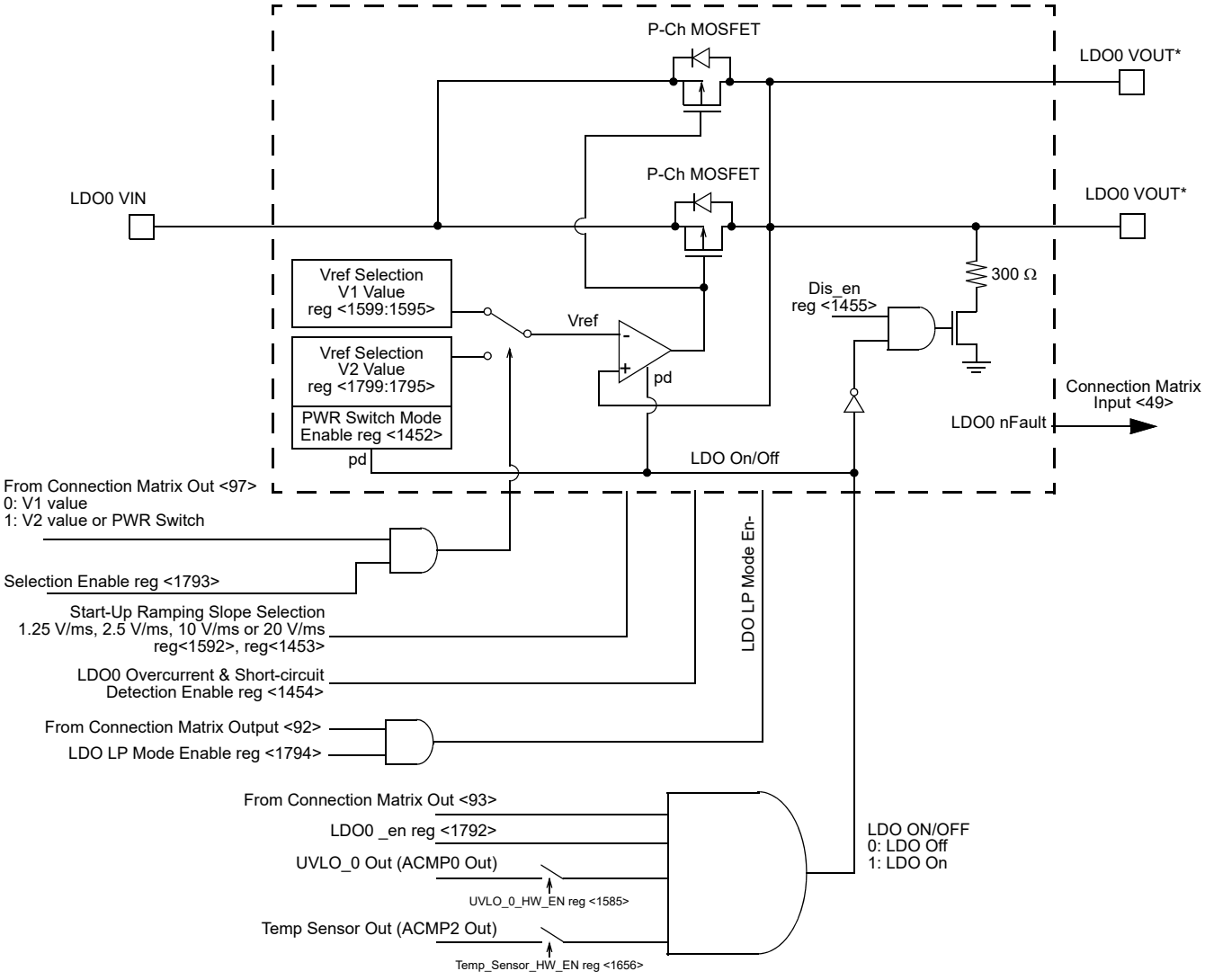
Figure 103. SLG46580 LDO P-channel ON resistance RDSon vs. VIN, Power Switch Mode, T = 25°C

23.0 SLG46582 Low Dropout Regulators

23.1 LDO Regulator Description

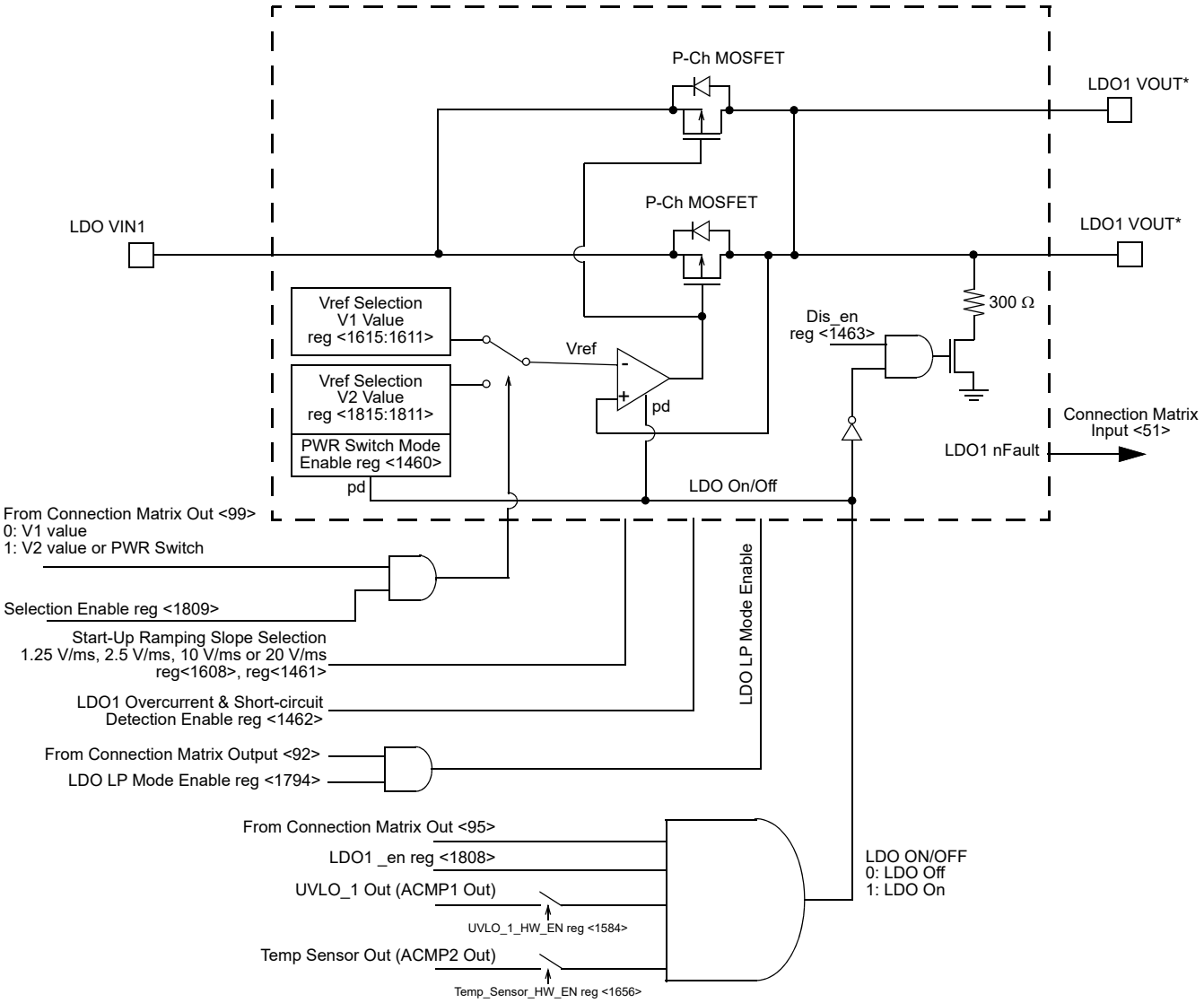
The SLG46582 comes with two low dropout regulators each rated at 300 mA. Each LDO regulator has 3 modes which are: HP MODE is the standard active mode supporting full 300 mA output; LP MODE is a low power mode with maximum 200 µA; and finally Power Switch Mode in which the LDO regulator ceases to regulate and the Regulator MOSFET is turned on as a power switch, passing the voltage applied to VIN directly to VOUT.

The LDO regulators each have a V_{IN} called LDO0 VIN for LDO0 and LDO1 VIN for LDO1.



Note*: Both LDO0 VOUT (Pins 11 and 13) must be connected together externally.

Figure 104. LDO0 Regulator Block Diagram



Note*: Both LDO1 VOUT (Pins 14 and 16) must be connected together external-

Figure 105. LDO1 Regulator Block Diagram

23.1.1 Voltage Selection

Each LDO has access to 32 voltage levels derived from a bandgap voltage reference.

It is possible to select two different output voltage levels (V1 and V2) per LDO. The voltage levels can be changed through the Connection Matri0x, after V1/V2 selection is enabled through the register bit. It is also possible to change the LDO output voltage level through the I^2C by writing the corresponding LDO output voltage selection number according to *Table 88*.

Table 91. LDO Output Voltage Selection

Selection #	LDO VOUT (V)	LDO Min. VIN (V)	Min. VDD (V)
0	0.90	2.30	2.30

Table 91. LDO Output Voltage Selection (continued)

Selection #	LDO VOUT (V)	LDO Min. VIN (V)	Min. VDD (V)
1	1.00	2.30	2.30
2	1.05	2.30	2.30
3	1.10	2.30	2.30
4	1.20	2.30	2.30
5	1.25	2.30	2.30
6	1.35	2.30	2.30
7	1.50	2.30	2.30
8	1.67	2.30	2.30
9	1.80	2.30	2.30
10	1.90	2.30	2.30
11	2.00	2.30	2.30
12	2.10	2.40	2.80
13	2.20	2.50	2.80
14	2.30	2.60	2.80
15	2.40	2.70	2.80
16	2.50	2.80	2.80
17	2.60	2.90	3.00
18	2.70	3.00	3.00
19	2.80	3.10	3.30
20	2.90	3.20	3.30
21	3.00	3.30	3.30
22	3.10	3.40	3.60
23	3.20	3.50	3.60
24	3.30	3.60	3.60
25	3.40	3.70	3.90
26	3.50	3.80	3.90
27	3.60	3.90	3.90
28	4.00	4.30	4.50
29	4.10	4.40	4.50
30	4.20	4.50	4.50
31	4.35	4.65	4.65

Note1: The combination of VIN, VDD and VOUT must satisfy the rule: VDD ≥ VIN ≥ VOUT + 0.3 V.
Note2: VIN and VDD should not exceed 5.5 V.

23.1.2 LDO HP Mode Operation

HP Mode is the standard active LDO mode with a 300 mA per LDO output loading capability.

A high level signal should be applied to Connection Matrix Outputs <93> and <95> together with the register enable bits <1792> and <1808> to enable LDO0 and LDO1, respectively. The LDO requires a wait time to enable analog circuitry before the LDO output starts to rise with the desired ramping slope selected through the register bits.

23.1.3 LDO LP Mode Operation

It is possible to enable ultra-low power LP Mode in which max output loading is 200 µA and quiescent current consumption is ~3 µA per LDO (without load). LP Mode can be enabled through Connection Matrix Output <92> together with the register enable bit <1794> and have an impact for all LDOs enabled in the SLG46582 chip.

23.1.4 Power Switch Mode Operation

Each LDO has an additional option to operate in power switch mode. In this case, all LDO related circuitry will be disabled. The quiescent current consumption is ~2 µA in power switch mode.

The power switch option is available in each LDO and can be used instead of the VOUT2 output voltage level selected by the following register bits: reg <1452> for LDO0 and reg <1460> for LDO1.

The Power Switch Mode can be selected by applying a high-level signal to the Connection Matrix Output <97> and <99> for LDO0 and LDO1, respectively.

23.2 Over-Current Limit and Short-Circuit Detection

Each LDO has an option to enable OCL (Over-Current Limit, if the output current rises above 429 mA) and SCD (Short-Circuit Detection, if output voltage drops below 0.5 V with the current limited by 40 mA).

These options are available for the LDO in HP Mode only. The nFAULT signal per LDO will generate a low-level signal to the connection matrix input when the short-circuit is detected.

Note: OCL and SCD are disabled by default, reg <1454> for LDO0 and reg <1462> for LDO1.

23.3 LDO Efficiency

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows:

$$\eta_{EF} = \frac{I_{OUT} \times V_{OUT}}{(I_{OUT} + I_Q) \times V_{IN}} \times 100$$

where:
η_{EF} = LDO efficiency, in percents (%)
I_{OUT} = Output current, in Amps (A)
V_{OUT} = Output voltage, in Volts (V)
I_Q = Quiescent current, in Amps (A)
V_{IN} = Input voltage, in Volts (V)

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for efficiency:

$$PD = V_{DO} \times I_{OUT}$$

where:
PD = Power Dissipation, in Watts (W)
V_{DO} = Drop out voltage, in Volts (V)
I_{OUT} = Output current, in Amps (A)

The Input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

23.4 LDO Thermal Considerations

The thermal limitations must be taken into consideration during regulator design. The SLG46582 is rated at 0.6 W of power dissipation at 85 °C ambient and 0.8 W of power dissipation at 70 °C ambient. If a regulator is connected to 5.0 V and then is programmed to output 1.8 V, the power dissipation at 150 mA is 0.48 W or almost the entire thermal budget of the SLG46582. In this case we recommend putting an external resistor between the application's power source (battery or wall power) and the SLG46582's LDO VIN to help distribute the thermal load. A 10 Ω, ¼ watt resistor would cut the IC thermal dissipation about in half without impacting overall performance. However, because the LDO VIN voltage is shared between two LDOs the resistor should be properly selected for the higher of the desired LDO output voltages.

If is possible to use the temperature sensor together with ACMP2 to automatically shut down all LDOs if the die temperature rises to a predetermined threshold level. The LDOs will automatically restart when the chip has cooled down within the hysteresis range for ACMP2. Other temperature shut off levels may be achieved by incorporating the temperature sensor into ACMP3's input.

Note: LDO Thermal Protection is disabled by default, reg <1656>.

23.5 Soft Start Function

Table 92 to *Table 93* below show the bit settings and slew rate selection options for each LDO.

Table 92. LDO0 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1453>	reg <1592>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

Table 93. LDO1 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1461>	reg <1608>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

23.6 ACMPs: Under Voltage Lockout capability, Power Good

LDO0 VIN and LDO1 VIN are sensed by ACMP0 and ACMP1 respectively as one of their input options. The sense line can be divided by 2, 3, or 4 for the common mode voltage input limitation of ACMP0 and ACMP1. ACMP0 and ACMP1 can be set to the customers desired under voltage lockout (UVLO) level. The undervoltage lockout can be set by either hardware connection to control the LDO or through the Connection Matrix. The UVLO_0 hardware connection to the LDO can be enabled by reg <1585>. for LDO0, and UVLO_1 by reg <1584> for LDO1.

Note 1: ACMP0 needs to be properly configured to use UVLO_0 for LDO0. ACMP1 needs to be properly configured to use UVLO_1 for LDO1.

A lockout level below 2.3 V is not useful as the lowest acceptable power supply voltage is 2.3 V.

ACMP3 has a selectable input from the output of LDO0 for the purpose of a power good.

The ACMPs connection to VDD may be reused for the purpose stated above.

Note 2: LDO Under Voltage Lockout is disabled by default.

23.7 Regulator Stability Considerations

The regulators are only stable in HP MODE when a 4 µF (min) capacitor or greater is attached to each LDOs V_{OUT}. The recommended capacitor is a 4 µF (min) X5R capacitor rated for 6 V or greater. The X5R capacitor varies with temperature, DC bias voltage, and process; however the SLG46582 LDOs have taken this variance into consideration when recommending the 4 µF (min) X5R from -40 to +85C.

23.8 LDO Regulator Cold Start up

When the SLG46582 VDD goes high, then the fastest that an LDO regulator can begin to power up under the control of the SLG46582 is ~2 ms typical, and 3 ms max.

During this cold start period the P Channel MOSFET gate is 0V so the MOSFET is automatically turning on if LDO VIN is also coming up. If the desired state of the LDO is off after cold start up, then a voltage glitch maybe present on V_{OUT} between cold start and the ~2-3 ms when SLG46582 takes control.

23.9 LDO Regulator Hot Start up

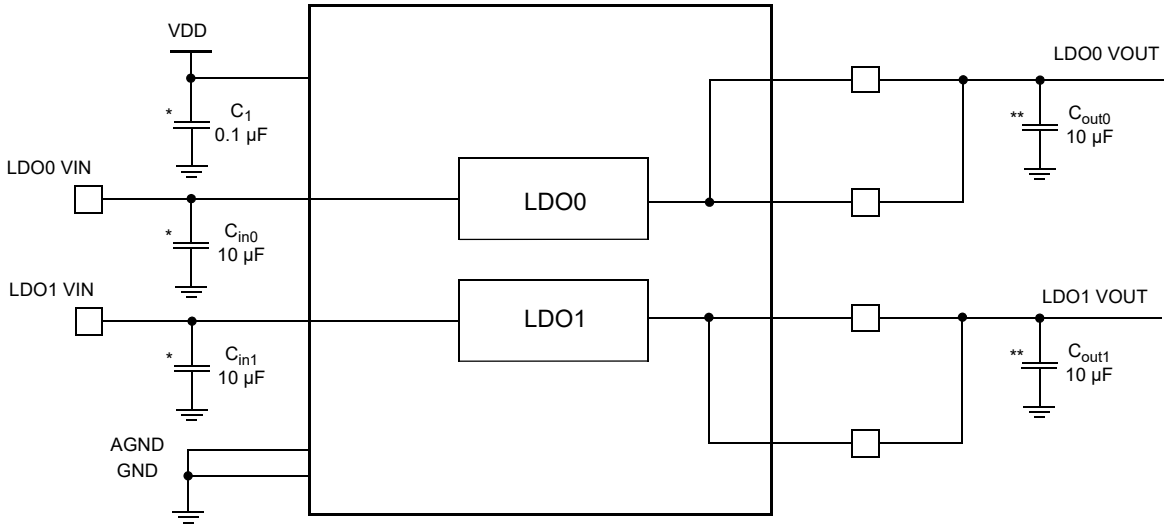
When the SLG46582 VDD is already high, then the fastest than an LDO regulator can begin to power up is around 500 µs + soft start ramping.

23.10 Discharge Resistors

Each LDO comes with a program selectable 300 ohm discharge resistor. For applications that desire a power rail to be brought to near zero during shutdown, then the 300 ohm discharge resistor is useful. For applications that desire to keep remaining charge on a V_{OUT} capacitor the discharge resistor should not be selected.

The discharge resistor is set by reg <1455> for LDO0 and reg <1463> for LDO1.

23.11 SLG46582 LDO Typical Application Circuit



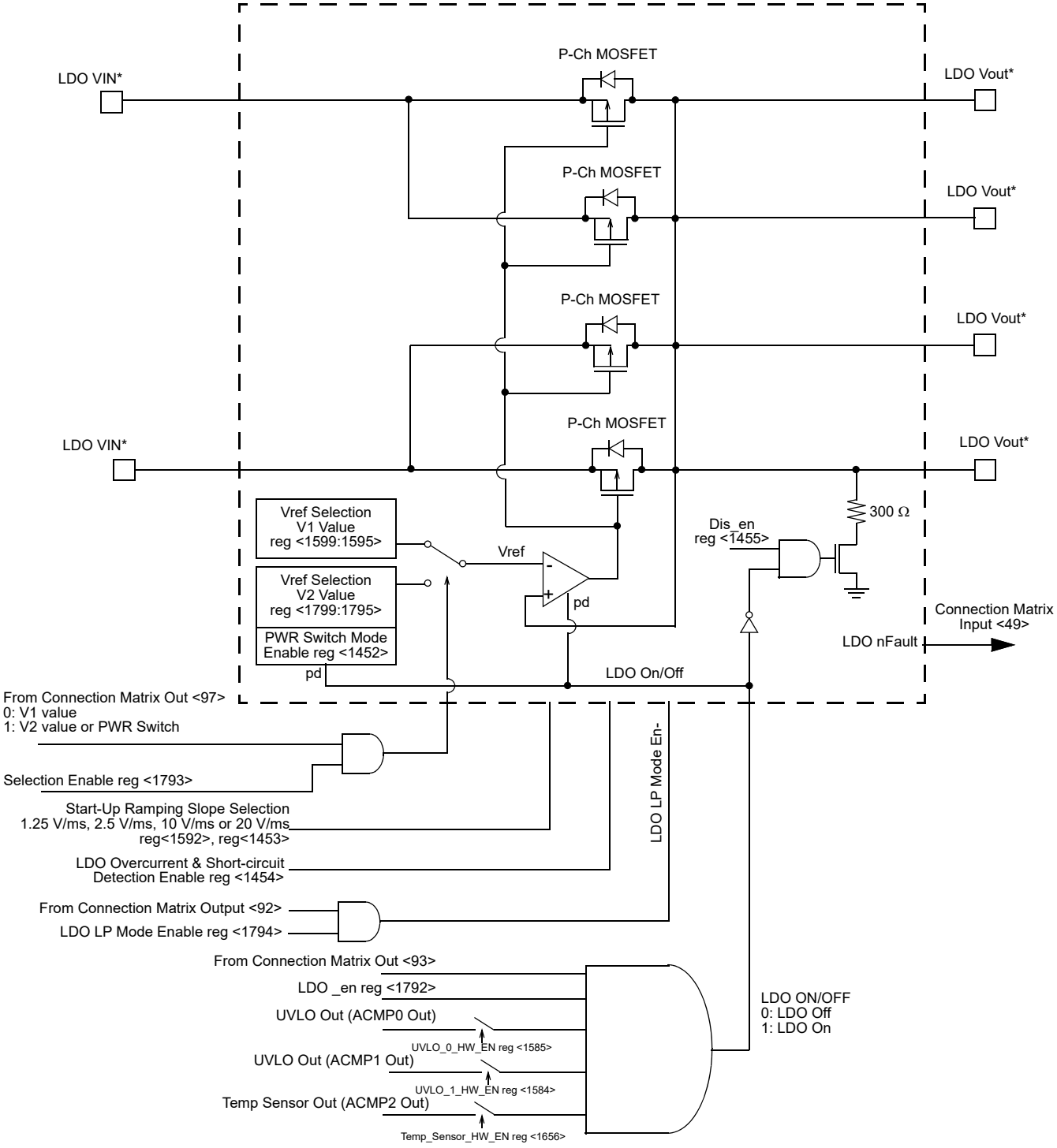
Note: All internal connections shown inside the SLG46582 are hardwired connections that cannot be changed.
Note: Keep decoupling capacitors close to the SLG46582.*
*Note**: Keep output capacitors close to the SLG46582. Long distances negatively impact LDO stability.*

Figure 106. SLG46582 LDO Typical Application Circuit

24.0 SLG46583 Low Dropout Regulator

24.1 LDO Regulator Description

The SLG46583 comes with a single low dropout regulators rated at 600 mA. The LDO regulator has 3 modes which are: HP MODE is the standard active mode supporting full 600 mA output; LP MODE is a low power mode with maximum 400 µA and finally Power Switch Mode in which the LDO regulator ceases to regulate and the Regulator MOSFET is turned on as a power switch, passing the voltage applied to VIN directly to VOUT.



Note*: Both LDO VIN (Pins 12 and 15) must be connected together externally. All four LDO VOUT (Pins 11, 13, 14 and 16) must be connected together externally.

Figure 107. LDO Regulator Block Diagram

24.1.1 Voltage Selection

The LDO has access to 32 voltage levels derived from a bandgap voltage reference.It is possible to select two different output voltage levels (V1 and V2) per LDO. The voltage levels can be changed through the Connection Matrix, after V1/V2 selection is enabled through the register bit. It is also possible to change the LDO output voltage level through the I^2C by writing the corresponding LDO output voltage selection number according to *Table 91*.

Table 94. LDO Output Voltage Selection

Selection #	LDO VOUT (V)	LDO Min. VIN (V)	Min. VDD (V)
0	0.90	2.30	2.30
1	1.00	2.30	2.30
2	1.05	2.30	2.30
3	1.10	2.30	2.30
4	1.20	2.30	2.30
5	1.25	2.30	2.30
6	1.35	2.30	2.30
7	1.50	2.30	2.30
8	1.67	2.30	2.30
9	1.80	2.30	2.30
10	1.90	2.30	2.30
11	2.00	2.30	2.30
12	2.10	2.40	2.80
13	2.20	2.50	2.80
14	2.30	2.60	2.80
15	2.40	2.70	2.80
16	2.50	2.80	2.80
17	2.60	2.90	3.00
18	2.70	3.00	3.00
19	2.80	3.10	3.30
20	2.90	3.20	3.30
21	3.00	3.30	3.30
22	3.10	3.40	3.60
23	3.20	3.50	3.60
24	3.30	3.60	3.60
25	3.40	3.70	3.90
26	3.50	3.80	3.90
27	3.60	3.90	3.90
28	4.00	4.30	4.50
29	4.10	4.40	4.50
30	4.20	4.50	4.50
31	4.35	4.65	4.65

Note1: The combination of VIN, VDD and VOUT must satisfy the rule: VDD ≥ VIN ≥ VOUT + 0.3 V.
Note2: VIN and VDD should not exceed 5.5 V.

24.1.2 LDO HP Mode Operation

HP Mode is the standard active LDO mode with a 600 mA per LDO output loading capability.

A high level signal should be applied to Connection Matrix Outputs <93> together with the register enable bits <1792> to enable this mode for LDO The LDO requires a wait time to enable analog circuitry before the LDO output starts to rise with the desired ramping slope selected through the register bits.

24.1.3 LDO LP Mode Operation

It is possible to enable ultra-low power LP Mode in which max output loading is 400 µA and quiescent current consumption is ~6µA per LDO (without load). LP Mode can be enabled through Connection Matrix Output <92> together with the register enable bit <1794> in the SLG46583 chip.

24.1.4 Power Switch Mode Operation

The LDO has an additional option to operate in power switch mode. In this case, all LDO related circuitry will be disabled. The quiescent current consumption is ~4 µA in power switch mode.

The power switch option is available in each LDO and can be used instead of the VOUT2 output voltage level selected by reg <1452>.

The Power Switch Mode can be selected by applying a high-level signal to the Connection Matrix Output <97>.

24.2 Over-Current Limit and Short-Circuit Detection

The LDO has an option to enable OCL (Over-Current Limit, if the output current rises above 820 mA) and SCD (Short-Circuit Detection, if output voltage drops below 0.5 V with the current limited by 72 mA).

These options are available for the LDO in HP Mode only. The nFAULT signal per LDO will generate a low-level signal to the connection matrix input when the short-circuit is detected.

Note: OCL and SCD are disabled by default, reg <1454>.

24.3 LDO Efficiency

The efficiency of LDO regulators is limited by the quiescent current and input/output voltages as follows:

$$\eta_{EF} = \frac{I_{OUT} \times V_{OUT}}{(I_{OUT} + I_Q) \times V_{IN}} \times 100$$

where:

η_{EF} = LDO efficiency, in percents (%)
I_{OUT} = Output current, in Amps (A)
V_{OUT} = Output voltage, in Volts (V)
I_Q = Quiescent current, in Amps (A)
V_{IN} = Input voltage, in Volts (V)

To have a high efficiency, drop out voltage and quiescent current must be minimized. In addition, the voltage difference between input and output must be minimized, since the power dissipation of LDO regulators accounts for efficiency:

$$PD = V_{DO} \times I_{OUT}$$

where:

PD = Power Dissipation, in Watts (W)
V_{DO} = Drop out voltage, in Volts (V)
I_{OUT} = Output current, in Amps (A)

The Input/output voltage difference is an intrinsic factor in determining the efficiency, regardless of the load conditions.

24.4 LDO Thermal Considerations

The thermal limitations must be taken into consideration during regulator design. The SLG46583 is rated at 0.6 W of power dissipation at 85 °C ambient and 0.8 W of power dissipation at 70 °C ambient. If a regulator is connected to 5.0 V and then is programmed to output 1.8 V, the power dissipation at 150 mA is 0.48 W or almost the entire thermal budget of the SLG46583. In this case we recommend putting an external resistor between the application's power source (battery or wall power) and the SLG46583's LDO VIN to help distribute the thermal load. A 10 Ω, ¼ watt resistor would cut the IC thermal dissipation about in half without impacting overall performance. However, because the LDO VIN voltage is shared between two LDO connections the resistor should be properly selected for the higher of the desired LDO output voltages.

If is possible to use the temperature sensor together with ACMP2 to automatically shut down the LDO if the die temperature rises to a predetermined threshold level. The LDO will automatically restart when the chip has cooled down within the hysteresis range for ACMP2. Other temperature shut off levels may be achieved by incorporating the temperature sensor into ACMP3's input.

Note: LDO Thermal Protection is disabled by default, reg <1656>.

24.5 Soft Start Function

Table 95 shows the bit settings and slew rate selection options for the LDO.

Table 95. LDO0 Ramp Rate Selection Table

Symbol	Parameter	Typical Value	reg <1453>	reg <1592>
SS0	SS Slew Rate 0	10 V/ms	0	0
SS1	SS Slew Rate 1	20 V/ms	0	1
SS2	SS Slew Rate 2	1.25 V/ms	1	0
SS3	SS Slew Rate 3	2.50 V/ms	1	1

24.6 ACMPs: Under Voltage Lockout capability, Power Good

LDO VIN is sensed by ACMP0 or ACMP1 respectively as one of their input options. The sense line can be divided by 2, 3, or 4 for the common mode voltage input limitation of ACMP0 or ACMP1. ACMP0 or ACMP1 can be set to the customers desired under voltage lockout (UVLO) level. The undervoltage lockout can be set by either hardware connection to control the LDO or through the Connection Matrix. The UVLO_0 hardware connection to the LDO can be enabled by reg <1585> for ACMP0, and UVLO_1 by reg <1584> for ACMP1.

Note 1: ACMP0 needs to be properly configured to use UVLO_0. ACMP1 needs to be properly configured to use UVLO_1.

A lockout level below 2.3 V is not useful as the lowest acceptable power supply voltage is 2.3 V.

ACMP3 has a selectable input from the output of LDO for the purpose of a power good.

The ACMPs connection to VDD may be reused for the purpose stated above.

Note 2: LDO Under Voltage Lockout is disabled by default.

24.7 Regulator Stability Considerations

The regulators are only stable in HP MODE when a 8 µF (min) capacitor or greater is attached to each LDOs V_{OUT}. The recommended capacitor is a 8 µF (min) X5R capacitor rated for 6 V or greater. The X5R capacitor varies with temperature, DC bias voltage, and process; however the SLG46583 LDOs have taken this variance into consideration when recommending the 8 µF (min) X5R from -40 to +85C.

24.8 LDO Regulator Cold Start up

When the SLG46583 VDD goes high, then the fastest that an LDO regulator can begin to power up under the control of the SLG46583 is ~2 ms typical, and 3 ms max.

During this cold start period the P Channel MOSFET gate is 0V so the MOSFET is automatically turning on if LDO VIN is also coming up. If the desired state of the LDO is off after cold start up, then a voltage glitch maybe present on V_{OUT} between cold start and the ~2-3 ms when SLG46583 takes control.

24.9 LDO Regulator Hot Start up

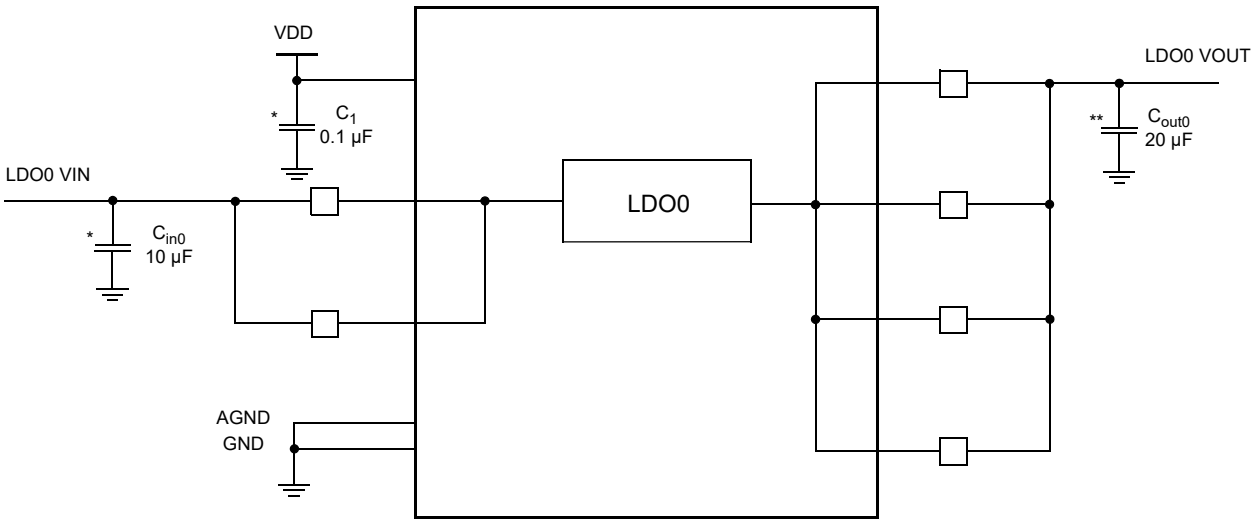
When the SLG46583 VDD is already high, then the fastest than an LDO regulator can begin to power up is around 500 µs + soft start ramping.

24.10 Discharge Resistors

The LDO comes with a program selectable 300 ohm discharge resistor. For applications that desire a power rail to be brought to near zero during shutdown, then the 300 ohm discharge resistor is useful. For applications that desire to keep remaining charge on a V_{OUT} capacitor the discharge resistor should not be selected.

The discharge resistor is set by reg <1455>.

24.11 SLG46583 LDO Typical Application Circuit



Note: All internal connections shown inside the SLG46583 are hardwired connections that cannot be changed.
Note: Keep decoupling capacitors close to the SLG46583.*
*Note**: Keep output capacitors close to the SLG46583. Long distances negatively impact LDO stability.*

Figure 108. SLG46583 LDO Typical Application Circuit

25.0 Appendix A - SLG46580/82/83 Register Definition

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
Note: For reg<0> to reg<1495>, I²C Read is valid (assuming reg <1832> = 0), I²C Write is valid (assuming reg <1871> = 0)				
Matrix Output				
reg<5:0>	Matrix OUT: ASM-state0-EN0		Valid	Valid
reg<7:6>	Reserved		Valid	Valid
reg<13:8>	Matrix OUT: ASM-state0-EN1		Valid	Valid
reg<15:14>	Reserved		Valid	Valid
reg<21:16>	Matrix OUT: ASM-state0-EN2		Valid	Valid
reg<23:22>	Reserved		Valid	Valid
reg<29:24>	Matrix OUT: ASM-state1-EN0		Valid	Valid
reg<31:30>	Reserved		Valid	Valid
reg<37:32>	Matrix OUT: ASM-state1-EN1		Valid	Valid
reg<39:38>	Reserved		Valid	Valid
reg<45:40>	Matrix OUT: ASM-state1-EN2		Valid	Valid
reg<47:46>	Reserved		Valid	Valid
reg<53:48>	Matrix OUT: ASM-state2-EN0		Valid	Valid
reg<55:54>	Reserved		Valid	Valid
reg<61:56>	Matrix OUT: ASM-state2-EN1		Valid	Valid
reg<63:62>	Reserved		Valid	Valid
reg<69:64>	Matrix OUT: ASM-state2-EN2		Valid	Valid
reg<71:70>	Reserved		Valid	Valid
reg<77:72>	Matrix OUT: ASM-state3-EN0		Valid	Valid
reg<79:78>	Reserved		Valid	Valid
reg<85:80>	Matrix OUT: ASM-state3-EN1		Valid	Valid
reg<87:86>	Reserved		Valid	Valid
reg<93:88>	Matrix OUT: ASM-state3-EN2		Valid	Valid
reg<95:94>	Reserved		Valid	Valid
reg<101:96>	Matrix OUT: ASM-state4-EN0		Valid	Valid
reg<103:102>	Reserved		Valid	Valid
reg<109:104>	Matrix OUT: ASM-state4-EN1		Valid	Valid
reg<111:110>	Reserved		Valid	Valid
reg<117:112>	Matrix OUT: ASM-state4-EN2		Valid	Valid
reg<119:118>	Reserved		Valid	Valid
reg<125:120>	Matrix OUT: ASM-state5-EN0		Valid	Valid
reg<127:126>	Reserved		Valid	Valid
reg<133:128>	Matrix OUT: ASM-state5-EN1		Valid	Valid
reg<135:134>	Reserved		Valid	Valid
reg<141:136>	Matrix OUT: ASM-state5-EN2		Valid	Valid
reg<143:142>	Reserved		Valid	Valid
reg<149:144>	Matrix OUT: ASM-state6-EN0		Valid	Valid
reg<151:150>	Reserved		Valid	Valid
reg<157:152>	Matrix OUT: ASM-state6-EN1		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<159:158>	Reserved		Valid	Valid
reg<165:160>	Matrix OUT: ASM-state6-EN2		Valid	Valid
reg<167:166>	Reserved		Valid	Valid
reg<173:168>	Matrix OUT: ASM-state7-EN0		Valid	Valid
reg<175:174>	Reserved		Valid	Valid
reg<181:176>	Matrix OUT: ASM-state7-EN1		Valid	Valid
reg<183:182>	Reserved		Valid	Valid
reg<189:184>	Matrix OUT: ASM-state7-EN2		Valid	Valid
reg<191:190>	Reserved		Valid	Valid
reg<197:192>	Matrix OUT: ASM-state-nRST		Valid	Valid
reg<199:198>	Reserved		Valid	Valid
reg<205:200>	Matrix OUT: IN0 of LUT3_6 or Delay0 Input (or Counter0 RST Input)		Valid	Valid
reg<207:206>	Reserved		Valid	Valid
reg<213:208>	Matrix OUT: IN1 of LUT3_6 or External Clock Input of Delay0 (or Counter0)		Valid	Valid
reg<215:214>	Reserved		Valid	Valid
reg<221:216>	Matrix OUT: IN2 of LUT3_6		Valid	Valid
reg<223:222>	Reserved		Valid	Valid
reg<229:224>	Matrix OUT: IN0 of LUT3_7 or Delay1 Input (or Counter1 RST Input)		Valid	Valid
reg<231:230>	Reserved		Valid	Valid
reg<237:232>	Matrix OUT: IN1 of LUT3_7 or External Clock Input of Delay1 (or Counter1)		Valid	Valid
reg<239:238>	Reserved		Valid	Valid
reg<245:240>	Matrix OUT: IN2 of LUT3_7		Valid	Valid
reg<247:246>	Reserved		Valid	Valid
reg<253:248>	Matrix OUT: IN0 of LUT3_8 or Delay2 Input (or Counter2 RST Input)		Valid	Valid
reg<255:254>	Reserved		Valid	Valid
reg<261:256>	Matrix OUT: IN1 of LUT3_8 or External Clock Input of Delay2 (or Counter2)		Valid	Valid
reg<263:262>	Reserved		Valid	Valid
reg<269:264>	Matrix OUT: IN2 of LUT3_8		Valid	Valid
reg<271:270>	Reserved		Valid	Valid
reg<277:272>	Matrix OUT: IN0 of LUT3_9 or Delay3 Input (or Counter3 RST Input)		Valid	Valid
reg<279:278>	Reserved		Valid	Valid
reg<285:280>	Matrix OUT: IN1 of LUT3_9 or External Clock Input of Delay3 (or Counter3)		Valid	Valid
reg<287:286>	Reserved		Valid	Valid
reg<293:288>	Matrix OUT: IN2 of LUT3_9		Valid	Valid
reg<295:294>	Reserved		Valid	Valid
reg<301:296>	Matrix OUT: IN0 of LUT3_10 or Delay4 Input (or Counter4 RST Input)		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<303:302>	Reserved		Valid	Valid
reg<309:304>	Matrix OUT: IN1 of LUT3_10 or External Clock Input of Delay4 (or Counter4)		Valid	Valid
reg<311:310>	Reserved		Valid	Valid
reg<317:312>	Matrix OUT: IN2 of LUT3_10		Valid	Valid
reg<319:318>	Reserved		Valid	Valid
reg<325:320>	Matrix OUT: IO0 Digital Output Source		Valid	Valid
reg<327:326>	Reserved		Valid	Valid
reg<333:328>	Matrix OUT: IO0 Output Enable		Valid	Valid
reg<335:334>	Reserved		Valid	Valid
reg<341:336>	Matrix OUT: IO1 Digital Output Source		Valid	Valid
reg<343:342>	Reserved		Valid	Valid
reg<349:344>	Matrix OUT: IO2 Digital Output Source		Valid	Valid
reg<351:350>	Reserved		Valid	Valid
reg<357:352>	Matrix OUT: IO3 Digital Output Source		Valid	Valid
reg<359:358>	Reserved		Valid	Valid
reg<365:360>	Matrix OUT: IO4 Digital Output Source		Valid	Valid
reg<367:366>	Reserved		Valid	Valid
reg<373:368>	Matrix OUT: IO4 Output Enable		Valid	Valid
reg<375:374>	Reserved		Valid	Valid
reg<381:376>	Matrix OUT: IO6 Digital Output Source		Valid	Valid
reg<383:382>	Reserved		Valid	Valid
reg<389:384>	Matrix OUT: IO6 Output Enable		Valid	Valid
reg<391:390>	Reserved		Valid	Valid
reg<397:392>	Matrix OUT: IO7 Digital Output Source		Valid	Valid
reg<399:398>	Reserved		Valid	Valid
reg<405:400>	Matrix OUT: IO8 Digital Output Source		Valid	Valid
reg<407:406>	Reserved		Valid	Valid
reg<413:408>	Matrix OUT: IO8 Output Enable		Valid	Valid
reg<415:414>	Reserved		Valid	Valid
reg<421:416>	Matrix OUT: ACMP0 PD (Power Down)		Valid	Valid
reg<423:422>	Reserved		Valid	Valid
reg<429:424>	Matrix OUT: ACMP1 PD (Power Down)		Valid	Valid
reg<431:430>	Reserved		Valid	Valid
reg<437:432>	Matrix OUT: ACMP2 PD (Power Down)		Valid	Valid
reg<439:438>	Reserved		Valid	Valid
reg<445:440>	Matrix OUT: ACMP3 PD (Power Down)		Valid	Valid
reg<447:446>	Reserved		Valid	Valid
reg<453:448>	Matrix OUT: Input of Filter_0 with fixed time edge detector		Valid	Valid
reg<455:454>	Reserved		Valid	Valid
reg<461:456>	Matrix OUT: Input of Filter_1 with fixed time edge detector		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<463:462>	Reserved		Valid	Valid
reg<469:464>	Matrix OUT: Input of Programmable Delay & Edge Detector		Valid	Valid
reg<471:470>	Reserved		Valid	Valid
reg<477:472>	Matrix OUT: OSC 25kHz/2MHz PD (Power Down)		Valid	Valid
reg<479:478>	Reserved		Valid	Valid
reg<485:480>	Matrix OUT: LPOSC PD (Power Down)		Valid	Valid
reg<487:486>	Reserved		Valid	Valid
reg<493:488>	Matrix OUT: IN0 of LUT2_0 or Clock Input of DFF0		Valid	Valid
reg<495:494>	Reserved		Valid	Valid
reg<501:496>	Matrix OUT: IN1 of LUT2_0 or Data Input of DFF0		Valid	Valid
reg<503:502>	Reserved		Valid	Valid
reg<509:504>	Matrix OUT: IN0 of LUT2_1 or Clock Input of DFF1		Valid	Valid
reg<511:510>	Reserved		Valid	Valid
reg<517:512>	Matrix OUT: IN1 of LUT2_1 or Data Input of DFF1		Valid	Valid
reg<519:518>	Reserved		Valid	Valid
reg<525:520>	Matrix OUT: IN0 of LUT2_2 or Clock Input of DFF2		Valid	Valid
reg<527:526>	Reserved		Valid	Valid
reg<533:528>	Matrix OUT: IN1 of LUT2_2 or Data Input of DFF2		Valid	Valid
reg<535:534>	Reserved		Valid	Valid
reg<541:536>	Matrix OUT: IN0 of LUT3_0 or Clock Input of DFF3		Valid	Valid
reg<543:542>	Reserved		Valid	Valid
reg<549:544>	Matrix OUT: IN1 of LUT3_0 or Data Input of DFF3		Valid	Valid
reg<551:550>	Reserved		Valid	Valid
reg<557:552>	Matrix OUT: IN2 of LUT3_0 or nRST (nSET) of DFF3		Valid	Valid
reg<559:558>	Reserved		Valid	Valid
reg<565:560>	Matrix OUT: IN0 of LUT3_1 or Clock Input of DFF4		Valid	Valid
reg<567:566>	Reserved		Valid	Valid
reg<573:568>	Matrix OUT: IN1 of LUT3_1 or Data Input of DFF4		Valid	Valid
reg<575:574>	Reserved		Valid	Valid
reg<581:576>	Matrix OUT: IN2 of LUT3_1 or nRST (nSET) of DFF4		Valid	Valid
reg<583:582>	Reserved		Valid	Valid
reg<589:584>	Matrix OUT: IN0 of LUT3_2 or Clock Input of DFF5		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<591:590>	Reserved		Valid	Valid
reg<597:592>	Matrix OUT: IN1 of LUT3_2 or Data Input of DFF5		Valid	Valid
reg<599:598>	Reserved		Valid	Valid
reg<605:600>	Matrix OUT: IN2 of LUT3_2 or nRST (nSET) of DFF5		Valid	Valid
reg<607:606>	Reserved		Valid	Valid
reg<613:608>	Matrix OUT: IN0 of LUT3_3 or Clock Input of DFF6		Valid	Valid
reg<615:614>	Reserved		Valid	Valid
reg<621:616>	Matrix OUT: IN1 of LUT3_3 or Data Input of DFF6		Valid	Valid
reg<623:622>	Reserved		Valid	Valid
reg<629:624>	Matrix OUT: IN2 of LUT3_3 or nRST (nSET) of DFF6		Valid	Valid
reg<631:630>	Reserved		Valid	Valid
reg<637:632>	Matrix OUT: IN0 of LUT3_4 or Clock Input of DFF7		Valid	Valid
reg<639:638>	Reserved		Valid	Valid
reg<645:640>	Matrix OUT: IN1 of LUT3_4 or Data Input of DFF7		Valid	Valid
reg<647:646>	Reserved		Valid	Valid
reg<653:648>	Matrix OUT: IN2 of LUT3_4 or nRST (nSET) of DFF7		Valid	Valid
reg<655:654>	Reserved		Valid	Valid
reg<661:656>	Matrix OUT: IN0 of LUT3_11 or Input of Pipe Delay or Up/Down selection of Ripple Counter		Valid	Valid
reg<663:662>	Reserved		Valid	Valid
reg<669:664>	Matrix OUT: IN1 of LUT3_11 or nRST of Pipe Delay or nRST of Ripple Counter		Valid	Valid
reg<671:670>	Reserved		Valid	Valid
reg<677:672>	Matrix OUT: IN2 of LUT3_11 or Clock of Pipe Delay or Clock of Ripple Counter		Valid	Valid
reg<679:678>	Reserved		Valid	Valid
reg<685:680>	Matrix OUT: IN0 of LUT3_5 or Clock Input of DFF8		Valid	Valid
reg<687:686>	Reserved		Valid	Valid
reg<693:688>	Matrix OUT: IN1 of LUT3_5 or Data Input of DFF8		Valid	Valid
reg<695:694>	Reserved		Valid	Valid
reg<701:696>	Matrix OUT: IN2 of LUT3_5 or nRST (nSET) of DFF8		Valid	Valid
reg<703:702>	Reserved		Valid	Valid
reg 709:704>	Matrix OUT: IN0 of LUT4x2_0		Valid	Valid
reg<711:710>	Reserved		Valid	Valid
reg<717:712>	Matrix OUT: IN1 of LUT4x2_0		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<719:718>	Reserved		Valid	Valid
reg<725:720>	Matrix OUT: IN2 of LUT4x2_0		Valid	Valid
reg<727:726>	Reserved		Valid	Valid
reg<733:728>	Matrix OUT: IN3 of LUT4x2_0		Valid	Valid
reg<735:734>	Reserved		Valid	Valid
reg<741:736>	Matrix OUT: LDO MODE1 Enable for LDO0/1/2/3 (for SLG46580) Matrix OUT: LDO MODE1 Enable for LDO0/1 (for SLG46582) Matrix OUT: LDO MODE1 Enable for LDO (for SLG46583)		Valid	Valid
reg<743:742>	Reserved		Valid	Valid
reg<749:744>	Matrix OUT: LDO0_EN (for SLG46580 and SLG46582) Matrix OUT: LDO_EN (for SLG46583)		Valid	Valid
reg<751:750>	Reserved		Valid	Valid
reg<757:752>	Matrix OUT: LDO1_EN (for SLG46580) Reserved (for SLG46582 and SLG46583)		Valid	Valid
reg<759:758>	Reserved		Valid	Valid
reg<765:760>	Matrix OUT: LDO2_EN (for SLG46580) Matrix OUT: LDO1_EN (for SLG46582) Reserved (for SLG46583)		Valid	Valid
reg<767:766>	Reserved		Valid	Valid
reg<773:768>	Matrix OUT: LDO3_EN (for SLG46580) Reserved (for SLG46582 and SLG46583)		Valid	Valid
reg<775:774>	Reserved		Valid	Valid
reg<781:776>	Matrix OUT: LDO0 2nd VOUT Selection Enable (for SLG46580 and SLG46582) Matrix OUT: LDO 2nd VOUT Selection Enable (for SLG46583)		Valid	Valid
reg<783:782>	Reserved		Valid	Valid
reg<789:784>	Matrix OUT: LDO1 2nd VOUT Selection Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)		Valid	Valid
reg<791:790>	Reserved		Valid	Valid
reg<797:792>	Matrix OUT: LDO2 2nd VOUT Selection Enable (for SLG46580) Matrix OUT: LDO1 2nd VOUT Selection Enable (for SLG46582) Reserved (for SLG46583)		Valid	Valid
reg<799:798>	Reserved		Valid	Valid
reg<805:800>	Matrix OUT: LDO3 2nd VOUT Selection Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)		Valid	Valid
reg<807:806>	Reserved		Valid	Valid
reg<813:808>	Matrix OUT: RTC Clock		Valid	Valid
reg<815:814>	Reserved		Valid	Valid
reg<821:816>	Matrix OUT: RTC Trigger signal to read/write RTC CNT values		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<823:822>	Reserved		Valid	Valid
reg<829:824>	Matrix OUT: ON/OFF command for BUCK		Valid	Valid
reg<831:830>	Reserved		Valid	Valid
reg<837:832>	Matrix OUT: Reserved		Valid	Valid
reg<839:838>	Reserved		Valid	Valid
reg<845:840>	Matrix OUT: Reserved		Valid	Valid
reg<847:846>	Reserved		Valid	Valid
reg<853:848>	Matrix OUT: Reserved		Valid	Valid
reg<855:854>	Reserved		Valid	Valid
reg<861:856>	Matrix OUT: Reserved		Valid	Valid
reg<863:862>	Reserved		Valid	Valid
reg<869:864>	Matrix OUT: Reserved		Valid	Valid
reg<871:870>	Reserved		Valid	Valid
reg<877:872>	Reserved		Valid	Valid
reg<879:878>	Reserved		Valid	Valid
reg<881:880>	Reserved		Valid	Valid
reg<884:882>	LDO2/3 VDD minimum Power Selection for LDO3 (for SLG46580) Reserved (for SLG46582 and SLG46583)	000: 2.3V, 001: 2.8V, 010: 3.0V, 011: 3.3V, 100: 3.6V, 101: 3.9V, 110: 4.5V, 111: 4.65V	Valid	Valid
reg<887:885>	LDO2/3 VDD minimum Power Selection for LDO2 (for SLG46580) LDO1 VDD minimum Power Selection for LDO1 (for SLG46582) Reserved (for SLG46583)	000: 2.3V, 001: 2.8V, 010: 3.0V, 011: 3.3V, 100: 3.6V, 101: 3.9V, 110: 4.5V, 111: 4.65V	Valid	Valid
reg<895:888>	Reserved		Valid	Invalid
reg<903:896>	CNT2 Counted Value for I2C read		Valid	Invalid
reg<911:904>	CNT4 Counted Value for I2C read		Valid	Invalid
reg<919:912>	Reserved		Valid	Invalid
reg<927:920>	Reserved		Valid	Invalid
reg<935:928>	Reserved (for SLG46582 and SLG46583)		Valid	Invalid
reg<943:936>	Shadow buffer for RTC counter <7:0>		Valid	Valid
reg<950:944>	Shadow buffer for RTC counter <14:8>		Valid	Valid
reg<951>	Reserved		Valid	Valid
reg<959:952>	Shadow buffer for RTC counter <23:16>		Valid	Valid
reg<967:960>	Shadow buffer for RTC counter <31:24>		Valid	Valid
reg<975:968>	Shadow buffer for RTC counter <39:32>		Valid	Valid
reg<983:976>	Shadow buffer for RTC counter <47:40>		Valid	Valid
reg<988:984>	Reserved		Valid	Valid
reg<989>	Shadow buffer data transfer direction selection		Valid	Valid
reg<990>	Shadow buffer trigger signal selection		Valid	Valid
reg<991>	RTC 32-bit time counter clock source	0: From 15-bit counter divider 1: From RTC clock	Valid	Valid
reg<999:992>	Alarm DCMP <23:16>		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1007:1000>	Alarm DCMP <31:24>		Valid	Valid
reg<1015:1008>	Alarm DCMP <39:32>		Valid	Valid
reg<1023:1016>	Alarm DCMP <47:40>		Valid	Valid
IO0				
reg<1024>	Reserved		Valid	Valid
reg<1025>	IO0 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1027:1026>	IO0 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1029:1028>	IO0 Mode Control (sig_io0_oe=0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
reg<1031:1030>	IO0 Mode Control (sig_io0_oe=1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X	Valid	Valid
IO1				
reg<1032>	Reserved		Valid	Valid
reg<1033>	IO1 Driver Strength Selection	0: 1X 1: 2X	Valid	Valid
reg<1034>	IO1 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1036:1035>	IO1 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1039:1037>	IO1 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS	Valid	Valid
IO2				
reg<1040>	Reserved		Valid	Valid
reg<1041>	IO2 Driver Strength Selection	0: 1X 1: 2X	Valid	Valid
reg<1042>	IO2 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1044:1043>	IO2 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1047:1045>	IO2 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Reserved	Valid	Valid
IO3				
reg<1048>	Reserved		Valid	Valid
reg<1049>	IO3 Driver Strength Selection	0: 1X 1: 2X	Valid	Valid
reg<1050>	IO3 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1052:1051>	IO3 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1055:1053>	IO3 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS	Valid	Valid
IO4				
reg<1056>	Reserved		Valid	Valid
reg<1057>	IO4 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1059:1058>	IO4 Pull Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1061:1060>	IO4 Mode Control (sig_io4_oe=0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
reg<1063:1062>	IO4 Mode Control (sig_io4_oe=1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X	Valid	Valid
IO5				
reg<1064>	Reserved		Valid	Valid
reg<1065>	Reserved		Valid	Valid
reg<1067:1066>	Reserved		Valid	Valid
reg<1069:1068>	IO5 Pull Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1071:1070>	IO5 Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
SCL				
reg<1072>	Reserved		Valid	Valid
reg<1073>	Reserved		Valid	Valid
reg<1074>	Reserved		Valid	Valid
reg<1076:1075>	Reserved		Valid	Valid
reg<1078:1077>	SCL Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
reg<1079>	Reserved		Valid	Valid
SDA				
reg<1080>	Reserved		Valid	Valid
reg<1081>	SDA Driver Strength Selection	0: 1X 1: 2X	Valid	Valid
reg<1082>	Reserved		Valid	Valid
reg<1084:1083>	Reserved		Valid	Valid
reg<1086:1085>	SDA Mode Control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved	Valid	Valid
reg<1087>	Reserved		Valid	Valid
IO6				
reg<1088>	Reserved		Valid	Valid
reg<1089>	IO6 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1091:1090>	IO6 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1093:1092>	IO6 Mode Control (sig_io6_oe=0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
reg<1095:1094>	IO6 Mode Control (sig_io6_oe=1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X	Valid	Valid
IO7				
reg<1096>	Reserved		Valid	Valid
reg<1097>	IO7 Driver Strength Selection	0: 1X 1: 2X	Valid	Valid
reg<1098>	IO7 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1100:1099>	IO7 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1103:1101>	IO7 Mode Control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain NMOS	Valid	Valid
IO8				
reg<1104>	Reserved		Valid	Valid
reg<1105>	IO8 Pull Up/Down Resistor Selection	0: Pull Down Resistor 1: Pull Up Resistor	Valid	Valid
reg<1107:1106>	IO8 Pull Up/Down Resistor Value Selection	00: Floating 01: 10K 10: 100K 11: 1M	Valid	Valid
reg<1109:1108>	IO8 Mode Control (sig_io8_oe=0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output	Valid	Valid
reg<1111:1110>	IO8 Mode Control (sig_io8_oe=1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X	Valid	Valid
ACMP				
reg<1112>	ACMP1 Positive Input Source Select - ACMP0 IN+ Source	0: Disable 1: Enable	Valid	Valid
reg<1113>	ACMP1 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
reg<1115:1114>	ACMP1 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV (01: for both external & internal VREF, 10 & 11: for only internal VREF, External VREF will not have 50 mV & 200 mV hysteresis.)	Valid	Valid
reg<1116>	ACMP0 Positive Input Source Select VDD	0: Disable 1: Enable	Valid	Valid
reg<1117>	ACMP0 Analog Buffer Enable (Max. BW 1MHz)	0: Disable analog buffer 1: Enable analog buffer	Valid	Valid
reg<1119:1118>	ACMP0 Hysteresis Enable	00: 0 mV 01: 25 mV 10: 50 mV 11: 200 mV (01: for both external & internal VREF, 10 & 11: for only internal VREF, External VREF will not have 50 mV & 200 mV hysteresis.)	Valid	Valid
reg<1120>	ACMP3 Positive Input Source Select - ACMP2 IN+ Source	0: Disable 1: Enable	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1123:1121>	ACMP3 Hysteresis Enable	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal VREF, 010 & 011 & 110 & 111: for only internal VREF, External VREF will not have 50 mV, 100 mV, 150 mV & 200 mV hysteresis.)	Valid	Valid
reg<1124>	ACMP2 Positive Input Source Select - ACMP0 IN+ Source	0: Disable 1: Enable	Valid	Valid
reg<1127:1125>	ACMP2 Hysteresis Enable	000: 0 mV 001: 25 mV 010: 50 mV 011: 200 mV 100: Reserved 101: Reserved 110: 100 mV 111: 150 mV (001: for both external & internal VREF, 010 & 011 & 110 & 111: for only internal VREF, External VREF will not have 50 mV, 100 mV, 150 mV & 200 mV hysteresis.)	Valid	Valid
LUT				
reg<1128>	LUT3_4 or DFF7 with nRST/nSET Select	0: LUT3_4 1: DFF7 with nRST/nSET	Valid	Valid
reg<1129>	LUT3_3 or DFF6 with nRST/nSET Select	0: LUT3_3 1: DFF6 with nRST/nSET	Valid	Valid
reg<1130>	LUT3_2 or DFF5 with nRST/nSET Select	0: LUT3_2 1: DFF5 with nRST/nSET	Valid	Valid
reg<1131>	LUT3_1 or DFF4 with nRST/nSET Select	0: LUT3_1 1: DFF4 with nRST/nSET	Valid	Valid
reg<1132>	LUT3_0 or DFF3 with nRST/nSET Select (Two consecutive DFFs if reg<1431>=1 for ASM)	0: LUT3_0 1: DFF3 with nRST/nSET	Valid	Valid
reg<1133>	LUT2_2 or DFF2 Select	0: LUT2_2 1: DFF2	Valid	Valid
reg<1134>	LUT2_1 or DFF1 Select	0: LUT2_1 1: DFF1	Valid	Valid
reg<1135>	LUT2_0 or DFF0 Select	0: LUT2_0 1: DFF0	Valid	Valid
LUT3				
reg<1136>	Reserved		Valid	Valid
reg<1137>	Reserved		Valid	Valid
reg<1138>	LUT3_5 or DFF8 with nRST/nSET Select	0: LUT3_5 1: DFF8 with nRST/nSET	Valid	Valid
reg<1139>	LUT3_10 or DLY/CNT4(8bits) Select	0: LUT3_10 1: DLY/CNT4(8bits)	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1140>	LUT3_9 or DLY/CNT3(8bits) Select	0: LUT3_9 1: DLY/CNT3(8bits)	Valid	Valid
reg<1141>	LUT3_8 or DLY/CNT2(8bits) Select	0: LUT3_8 1: DLY/CNT2(8bits)	Valid	Valid
reg<1142>	LUT3_7 or DLY/CNT1(8bits) Select	0: LUT3_7 1: DLY/CNT1(8bits)	Valid	Valid
reg<1143>	LUT3_6 or DLY/CNT0(8bits) Select	0: LUT3_6 1: DLY/CNT0(8bits)	Valid	Valid
LUT2				
reg<1144>	LUT2_1 <0>		Valid	Valid
reg<1145>	LUT2_1 <1> / DFF1 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1146>	LUT2_1 <2> / DFF1 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1147>	LUT2_1 <3> / DFF1 or Latch1 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1148>	LUT2_0 <0>		Valid	Valid
reg<1149>	LUT2_0 <1> / DFF0 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1150>	LUT2_0 <2> / DFF0 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1151>	LUT2_0 <3> / DFF0 or Latch0 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1155:1152>	Reserved		Valid	Valid
reg<1156>	LUT2_2 <0>		Valid	Valid
reg<1157>	LUT2_2 <1> / DFF2 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1158>	LUT2_2 <2> / DFF2 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1159>	LUT2_2 <3> / DFF2 or Latch2 Select	0: DFF function 1: Latch function	Valid	Valid
LUT3				
reg<1163:1160>	LUT3_0 <3:0>		Valid	Valid
reg<1164>	LUT3_0 <4> / DFF3 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1165>	LUT3_0 <5> / DFF3 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1166>	LUT3_0 <6> / DFF3 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1167>	LUT3_0 <7> / DFF3 or Latch3 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1171:1168>	LUT3_1 <3:0>		Valid	Valid
reg<1172>	LUT3_1 <4> / DFF4 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1173>	LUT3_1 <5> / DFF4 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1174>	LUT3_1 <6> / DFF4 Output Select	0: Q output 1: nQ output	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1175>	LUT3_1 <7> / DFF4 or Latch4 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1179:1176>	LUT3_2 <3:0>		Valid	Valid
reg<1180>	LUT3_2 <4> / DFF5 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1181>	LUT3_2 <5> / DFF5 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1182>	LUT3_2 <6> / DFF5 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1183>	LUT3_2 <7> / DFF5 or Latch5 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1187:1184>	LUT3_3 <3:0>		Valid	Valid
reg<1188>	LUT3_3 <4> / DFF6 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1189>	LUT3_3 <5> / DFF6 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1190>	LUT3_3 <6> / DFF6 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1191>	LUT3_3 <7> / DFF6 or Latch6 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1195:1192>	LUT3_4 <3:0>		Valid	Valid
reg<1196>	LUT3_4 <4> / DFF7 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1197>	LUT3_4 <5> / DFF7 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1198>	LUT3_4 <6> / DFF7 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1199>	LUT3_4 <7> / DFF7 or Latch7 Select	0: DFF function 1: Latch function	Valid	Valid
reg<1203:1200>	LUT3_5 <3:0>		Valid	Valid
reg<1204>	LUT3_5 <4> / DFF8 Initial Polarity Select	0: Low 1: High	Valid	Valid
reg<1205>	LUT3_5 <5> / DFF8 nRST or nSET Select	0: nRST from Matrix Output 1: nSET from Matrix Output	Valid	Valid
reg<1206>	LUT3_5 <6> / DFF8 Output Select	0: Q output 1: nQ output	Valid	Valid
reg<1207>	LUT3_5 <7> / DFF8 or Latch8 Select	0: DFF function 1: Latch function	Valid	Valid
Reserved				
reg<1215:1208>	Reserved		Valid	Valid
reg<1223:1216>	Reserved Reserved		Valid	Invalid
LUT3 & DLY/CNT				
reg<1227:1224>	LUT3_11 <3:0> / Pipe Delay OUT0 Select / Ripple Counter END<0>,nSET<2:0>		Valid	Valid
reg<1231:1228>	LUT3_11 <7:4> / Pipe Delay OUT1 Select / Ripple Counter RSVD,MODE,END<2:1>		Valid	Valid
reg<1232>	Reserved		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1233>	DLY/CNT4 Delayed Edge Output Selection	0: Default function from reg<1277> 1: Delayed edge detect	Valid	Valid
reg<1234>	DLY/CNT3 Delayed Edge Output Selection	0: Default function from reg<1269> 1: Delayed edge detect	Valid	Valid
reg<1235>	DLY/CNT2 Delayed Edge Output Selection	0: Default function from reg<1261> 1: Delayed edge detect	Valid	Valid
reg<1236>	DLY/CNT1 Delayed Edge Output Selection	0: Default function from reg<1253> 1: Delayed edge detect	Valid	Valid
reg<1237>	Pipe Delay Select or Ripple counter Select	0: Pipe Delay 1: Ripple Counter	Valid	Valid
reg<1238>	LUT3_11 or Pipe Delay Select	0: LUT3_11 1: Pipe Delay / Ripple counter by reg<1237>	Valid	Valid
reg<1239>	Pipe Delay OUT1 Polarity Select	0: Non-Inverted 1: Inverted	Valid	Valid
DLY/CNT0				
reg<1241:1240>	DLY0 Edge Select or Asynchronous CNT0 Reset	00: On both Falling and Rising Edges 01: on Falling Edge only 10: on Rising Edge only 11: No Delay on either Falling or Rising Edges / High Level Counter Reset	Valid	Valid
reg<1244:1242>	DLY/CNT0 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter4 Overflow	Valid	Valid
reg<1245>	CNT0 Q are Set to data or Reset to 0s Selection (8bits)	0: Reset to 0s 1: Set to data (Reg<1543:1536>)	Valid	Valid
reg<1247:1246>	DLY/CNT0 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT1				
reg<1249:1248>	DLY1 Edge Select or Asynchronous CNT1 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges / High Level Counter Reset	Valid	Valid
reg<1252:1250>	DLY/CNT1 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter0 Overflow	Valid	Valid
reg<1253>	DLY/CNT1 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1255:1254>	DLY/CNT1 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT2				
reg<1257:1256>	DLY2 Edge Select or Asynchronous CNT2 Reset	00: On both Falling and Rising Edges 01: on Falling Edge only 10: on Rising Edge only 11: No Delay on either Falling or Rising Edges / High Level Counter Reset	Valid	Valid
reg<1260:1258>	DLY/CNT2 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter1 Overflow	Valid	Valid
reg<1261>	DLY/CNT2 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
reg<1263:1262>	DLY/CNT2 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT3				
reg<1265:1264>	DLY3 Edge Select or Asynchronous CNT3 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges / High Level Counter Reset	Valid	Valid
reg<1268:1266>	DLY/CNT3 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter2 Overflow	Valid	Valid
reg<1269>	DLY/CNT3 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
reg<1271:1270>	DLY/CNT3 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
DLY/CNT4				
reg<1273:1272>	DLY4 Edge Select or Asynchronous CNT4 Reset	00: On both Falling and Rising Edges 01: On Falling Edge only 10: On Rising Edge only 11: No Delay on either Falling or Rising Edges / High Level Counter Reset	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1276:1274>	DLY/CNT4 Clock Source Select	000: OSC 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: LPOSC Clock 110: External Clock 111: Counter3 Overflow	Valid	Valid
reg<1277>	DLY/CNT4 Output Selection	0: Default Output 1: Edge Detector Output	Valid	Valid
reg<1279:1278>	DLY/CNT4 Mode Selection	00: Delay mode 01: One Shot 10: Freq. Detect 11: Counter mode	Valid	Valid
Reserved				
reg<1280>	Reserved		Valid	Valid
reg<1281>	Reserved		Valid	Valid
reg<1282>	External Clock Source Select instead of 25kHz/2MHz	0: Internal Oscillator, 1: External Clock (EXT_CLK)	Valid	Valid
DLY/CNT Polarity Select				
reg<1283>	Select the Polarity of DLY/CNT4's Output	0: Default Output 1: Inverted Output	Valid	Valid
reg<1284>	Select the Polarity of DLY/CNT3's Output	0: Default Output 1: Inverted Output	Valid	Valid
reg<1285>	Select the Polarity of DLY/CNT2's Output	0: Default Output 1: Inverted Output	Valid	Valid
reg<1286>	Select the Polarity of DLY/CNT1's Output	0: Default Output 1: Inverted Output	Valid	Valid
reg<1287>	Select the Polarity of DLY/CNT0's Output	0: Default Output 1: Inverted Output	Valid	Valid
OSC				
reg<1289:1288>	LPOSC Clock Pre-divider	00: Div1, 01:Div2, 10: Div4, 11: Div16	Valid	Valid
reg<1290>	Force LPOSC Oscillator ON	0: Auto Power ON (if any CNT/DLY use LPOSC source) 1: Force Power ON	Valid	Valid
reg<1292:1291>	OSC Clock Pre-divider	00: Div1 01: Div2 10: Div4 11: Div8	Valid	Valid
reg<1293>	OSC Fast Start-Up Enable	0: Disable 1: Enable	Valid	Valid
reg<1294>	Oscillator (25kHz: RC-OSC, 2M: RC-OSC) Select	0: 25 kHz RC-OSC 1: 2 MHz RC-OSC	Valid	Valid
reg<1295>	Force Oscillator ON	0: Auto Power ON (if any CNT/DLY use 25K source) 1: Force Power ON	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1298:1296>	Internal OSC 25 kHz Frequency Divider Control for matrix input <28>	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
reg<1299>	OSC Clock 25 kHz to matrix input <28> enable	0: Disable 1: Enable	Valid	Valid
reg<1302:1300>	Internal OSC 25 kHz Frequency Divider Control for matrix input <27>	000: OSC/1 001: OSC/2 010: OSC/3 011: OSC/4 100: OSC/8 101: OSC/12 110: OSC/24 111: OSC/64	Valid	Valid
reg<1303>	OSC Clock 25 kHz to matrix input <27> enable	0: Disable 1: Enable	Valid	Valid
IO5				
reg<1304>	IO5 reset level polarity selection	0: Non-inverted 1: Inverted	Valid	Valid
reg<1305>	IO5 reset bypass selection	0: Edge selection 1: Level selection	Valid	Valid
reg<1306>	IO5 reset edge selection	0: Rising edge 1: Falling edge	Valid	Valid
reg<1307>	IO5 reset enable	0: Disable 1: Enable	Valid	Valid
reg<1309:1308>	Select the Edge Mode of Programmable Delay & Edge Detector	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay	Valid	Valid
reg<1311:1310>	Delay Value Select for Programmable Delay & Edge Detector (VDD = 3.3V, typical)	00: 165 ns 01: 300 ns 10: 440 ns 11: 575 ns	Valid	Valid
ASM				
reg<1314:1312>	ASM_reg_init<2:0> for ASM state default setup bits		Valid	Valid
reg<1319:1315>	Reserved		Valid	Valid
reg<1322:1320>	ASM_state0_dec8x1_EN1		Valid	Valid
reg<1323>	Reserved		Valid	Valid
reg<1326:1324>	ASM_state0_dec8x1_EN0		Valid	Valid
reg<1327>	Reserved		Valid	Valid
reg<1330:1328>	ASM_state1_dec8x1_EN0		Valid	Valid
reg<1331>	Reserved		Valid	Valid
reg<1334:1332>	ASM_state0_dec8x1_EN2		Valid	Valid
reg<1335>	ASM Rising Edge Detect Enable on EN2 of state0	0: Disable 1: Enable	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1338:1336>	ASM_state1_dec8x1_EN2		Valid	Valid
reg<1339>	ASM Rising Edge Detect Enable on EN2 of state1	0: Disable 1: Enable	Valid	Valid
reg<1342:1340>	ASM_state1_dec8x1_EN1		Valid	Valid
reg<1343>	Reserved		Valid	Valid
reg<1346:1344>	ASM_state2_dec8x1_EN1		Valid	Valid
reg<1347>	Reserved		Valid	Valid
reg<1350:1348>	ASM_state2_dec8x1_EN0		Valid	Valid
reg<1351>	Reserved		Valid	Valid
reg<1354:1352>	ASM_state3_dec8x1_EN0		Valid	Valid
reg<1355>	Reserved		Valid	Valid
reg<1358:1356>	ASM_state2_dec8x1_EN2		Valid	Valid
reg<1359>	ASM Rising Edge Detect Enable on EN2 of state2	0: Disable 1: Enable	Valid	Valid
reg<1362:1360>	ASM_state3_dec8x1_EN2		Valid	Valid
reg<1363>	ASM Rising Edge Detect Enable on EN2 of state3	0: Disable 1: Enable	Valid	Valid
reg<1366:1364>	ASM_state3_dec8x1_EN1		Valid	Valid
reg<1367>	Reserved		Valid	Valid
reg<1370:1368>	ASM_state4_dec8x1_EN1		Valid	Valid
reg<1371>	Reserved		Valid	Valid
reg<1374:1372>	ASM_state4_dec8x1_EN0		Valid	Valid
reg<1375>	Reserved		Valid	Valid
reg<1378:1376>	ASM_state5_dec8x1_EN0		Valid	Valid
reg<1379>	Reserved		Valid	Valid
reg<1382:1380>	ASM_state4_dec8x1_EN2		Valid	Valid
reg<1383>	ASM Rising Edge Detect Enable on EN2 of state4	0: Disable 1: Enable	Valid	Valid
reg<1386:1384>	ASM_state5_dec8x1_EN2		Valid	Valid
reg<1387>	ASM Rising Edge Detect Enable on EN2 of state5	0: Disable 1: Enable	Valid	Valid
reg<1390:1388>	ASM_state5_dec8x1_EN1		Valid	Valid
reg<1391>	Reserved		Valid	Valid
reg<1394:1392>	ASM_state6_dec8x1_EN1		Valid	Valid
reg<1395>	Reserved		Valid	Valid
reg<1398:1396>	ASM_state6_dec8x1_EN0		Valid	Valid
reg<1399>	Reserved		Valid	Valid
reg<1402:1400>	ASM_state7_dec8x1_EN0		Valid	Valid
reg<1403>	Reserved		Valid	Valid
reg<1406:1404>	ASM_state6_dec8x1_EN2		Valid	Valid
reg<1407>	ASM Rising Edge Detect Enable on EN2 of state6	0: Disable 1: Enable	Valid	Valid
reg<1410:1408>	ASM_state7_dec8x1_EN2		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1411>	ASM Rising Edge Detect Enable on EN2 of state7		Valid	Valid
reg<1414:1412>	ASM_state7_dec8x1_EN1		Valid	Valid
reg<1415>	Reserved		Valid	Valid
Filter / Edge Detector				
reg<1417:1416>	Select the edge mode of Edge Detector_1	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
reg<1418>	Filter_1/Edge Detector_1 output Polarity Select	0: Filter_1 output 1: Filter_1 output inverted	Valid	Valid
reg<1419>	Filter_1 (Typ. 50nS @VDD=3.3V) or Edge Detector_1 (Typ. 125nS @VDD=3.3V) Select	0: Filter_1 1: Edge Detector_1	Valid	Valid
reg<1421:1420>	Select the edge mode of Edge Detector_0	00: Rising Edge 01: Falling Edge 10: Both Edge 11: Delay	Valid	Valid
reg<1422>	Filter_0/Edge Detector_0 output Polarity Select	0: Filter_0 output 1: Filter_0 output inverted	Valid	Valid
reg<1423>	Filter_0 (Typ. 70 ns @VDD=3.3V) or Edge Detector_0 Select (Typ. 125 ns @ VDD=3.3V)	0: Filter_0 1: Edge Detector_0	Valid	Valid
VREF / Bandgap				
reg<1424>	Reserved		Valid	Valid
reg<1426:1425>	Reserved		Valid	Valid
reg<1427>	Reserved		Valid	Valid
reg<1428>	Vref Op Amp Offset Chopper Enable	0: Disable 1: Enable	Valid	Valid
reg<1429>	Reserved	0: Disable 1: Enable	Valid	Valid
reg<1430>	Reserved	0: 2 MHz 1: 1 MHz	Valid	Valid
reg<1431>	Two consecutive DFFs enable for ASM	0: Disable 1: Enable	Valid	Valid
reg<1434:1432>	CP function selection & Power divider (VDD/3, VDD/4) ON/OFF	100: CP Auto ON/OFF (Use for 1.71V<VDD<5.5V) X10: CP always OFF (Use for 2.7V<VDD), XX1: CP always ON (Use for VDD<2.7V) 0XX: Power divider off (if there is no use of VDD/3,VDD/4 @ACMP negative in)	Valid	Valid
reg<1435>	Reserved		Valid	Valid
reg<1436>	Force Bandgap ON	0: Auto-Mode 1: Enable (if chip is Power Down, the Bandgap will Power Down even if it is Set to 1).	Valid	Valid
reg<1437>	NVM Power Down	0: None (Or Programming Enable) 1: Power Down (Or Programming Disable)	Valid	Valid
reg<1438>	Reserved		Valid	Valid
reg<1439>	GPIO Quick Charge Enable	0: Disable 1: Enable	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
Wake/Sleep				
reg<1440>	Reserved		Valid	Valid
reg<1441>	Reserved		Valid	Valid
reg<1442>	ACMP0 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
reg<1443>	ACMP1 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
reg<1444>	ACMP2 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
reg<1445>	ACMP3 Wake & Sleep function Enable	0: Disable 1: Enable	Valid	Valid
reg<1446>	Wake Sleep Output State When WS Oscillator is Power Down if DLY/CNT0 Mode Selection is "11"	0: Low 1: High	Valid	Valid
reg<1447>	Wake Sleep Ratio Control Mode Selection if DLY/CNT0 Mode Selection is "11"	0: Default Mode 1: Wake Sleep Ratio Control Mode	Valid	Valid
LDO				
reg<1448>	LDO1 PS_Mode_Gate (LDO1 turn-on/off is controlled by LDO1_EN matrix output) (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: LDO Mode Enable (for SLG46580) 1: Power switch Mode Enable (for SLG46580)	Valid	Valid
reg<1449>	LDO1 Start-up Ramping Slope Divide Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (Div 8 of reg<1600>)	Valid	Valid
reg<1450>	LDO1 Over-current & Short-current Detection Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (for SLG46580)	Valid	Valid
reg<1451>	LDO1 Discharge resistor Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: No discharge resistor (for SLG46580) 1: 300 ohm discharge resistor (for SLG46580)	Valid	Valid
reg<1452>	LDO0 PS_Mode_Gate (LDO0 turn-on/off is controlled by LDO0_EN matrix output) (for SLG46580 and SLG46582) LDO PS_Mode_Gate (LDO0 turn-on/off is controlled by LDO0_EN matrix output) (for SLG46583)	0: LDO Mode Enable 1: Power switch Mode Gate Enable	Valid	Valid
reg<1453>	LDO0 Start-up Ramping Slope Divide Enable (for SLG46580 and SLG46582) LDO Start-up Ramping Slope Divide Enable (for SLG46583)	0: Disable (for SLG46580) 1: Enable (Div 8 of reg<1592>)	Valid	Valid
reg<1454>	LDO0 Over-current & Short-current Detection Enable (for SLG46580 and SLG46582) LDO Over-current & Short-current Detection Enable (for SLG46583)	0: Disable 1: Enable	Valid	Valid
reg<1455>	LDO0 Discharge resistor Enable (for SLG46580 and SLG46582) LDO Discharge resistor Enable (for SLG46583)	0: No discharge resistor 1: 300 Ohm discharge resistor	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1456>	LDO3 PS_Mode_Gate (LDO3 turn-on/off is controlled by LDO3_EN matrix output) (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: LDO Mode Enable (for SLG46580) 1: Power switch Mode Gate Enable (for SLG46580)	Valid	Valid
reg<1457>	LDO3 Start-up Ramping Slope Divide Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (Div 8 of reg<1616>)	Valid	Valid
reg<1458>	LDO3 Over-current & Short-current Detection Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (for SLG46580)	Valid	Valid
reg<1459>	LDO3 Discharge resistor Enable (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: No discharge resistor (for SLG46580) 1: 300 Ohm discharge resistor (for SLG46580)	Valid	Valid
reg<1460>	LDO2 PS_Mode_Gate (LDO2 turn-on/off is controlled by LDO2_EN matrix output) (for SLG46580) LDO1 PS_Mode_Gate (LDO1 turn-on/off is controlled by LDO1_EN matrix output) (for SLG46582) Reserved (for SLG46583)	0: LDO Mode Enable (for SLG46580 and SLG46582) 1: Power switch Mode Gate Enable (for SLG46580 and SLG46582)	Valid	Valid
reg<1461>	LDO2 Start-up Ramping Slope Divide Enable (for SLG46580) LDO1 Start-up Ramping Slope Divide Enable (for SLG46582) Reserved (for SLG46583)	0: Disable 1: Enable (Div 8 of reg<1608>)	Valid	Valid
reg<1462>	LDO2 Over-current & Short-current Detection Enable (for SLG46580) LDO1 Over-current & Short-current Detection Enable (for SLG46582) Reserved (for SLG46583)	0: Disable (for SLG46580 and SLG46582) 1: Enable (for SLG46580 and SLG46582)	Valid	Valid
reg<1463>	LDO2 Discharge resistor Enable (for SLG46580) LDO1 Discharge resistor Enable (for SLG46582) Reserved (for SLG46583)	0: No discharge resistor (for SLG46580 and SLG46582) 1: 300 ohm discharge resistor (for SLG46580 and SLG46582)	Valid	Valid
reg<1465:1464>	Reserved		Valid	Invalid
reg<1467:1466>	Reserved		Valid	Invalid
reg<1469:1468>	Reserved		Valid	Invalid
reg<1471:1470>	Reserved		Valid	Invalid
reg<1479:1472>	Reserved (for SLG46583)		Valid	Invalid
reg<1487:1480>	Reserved		Valid	Invalid
reg<1488>	ACMP1 100 uA Current Source Enable	0: Disable 1: Enable	Valid	Valid
reg<1489>	Reserved		Valid	Valid
reg<1490>	Reserved		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1491>	LDO2 VOUT output connection enable to ACMP3 (for SLG46580) LDO1 VOUT output connection enable to ACMP3 (for SLG46582) Reserved (for SLG46583)	0: Default ACMP function 1: Enable LDO2 VOUT function	Valid	Valid
reg<1492>	LDO0 VOUT output connection enable to ACMP3 (for SLG46580 and SLG46582) LDO VOUT output connection enable to AC-MP3 (for SLG46583)	0: Default ACMP function 1: Enable LDO0 VOUT function	Valid	Valid
reg<1493>	TS output connection enable to ACMP2	0: Default ACMP function 1: Enable TS function	Valid	Valid
reg<1494>	LDO2/3 VIN connection enable to ACMP1 (for SLG46580) LDO1 VIN connection enable to ACMP1 (for SLG46582) LDO VIN connection enable to ACMP1 (for SLG46583)	0: Default ACMP function (for SLG46580 and SLG46582) 1: Enable UVLO1 function (for SLG46580 and SLG46582) 0: Default ACMP function (for SLG46583) 1: Enable UVLO function (for SLG46583)	Valid	Valid
reg<1495>	LDO0/1 VIN connection enable to ACMP0 (for SLG46580) LDO0 VIN connection enable to ACMP0 (for SLG46582) LDO VIN connection enable to ACMP0 (for SLG46583)	0: Default ACMP function (for SLG46580 and SLG46582) 1: Enable UVLO0 function (for SLG46580 and SLG46582) 0: Default ACMP function (for SLG46583) 1: Enable UVLO function (for SLG46583)	Valid	Valid
reg<1496>	Reserved		Valid	Valid
reg<1497>	Reserved		Valid	Valid
reg<1498>	Reserved		Valid	Valid
reg<1499>	Reserved		Valid	Valid
reg<1503:1500>	Reserved		Valid	Valid
reg<1519:1504>	LUT4x2_0 Output0 <15:0>		Valid	Valid
reg<1535:1520>	LUT4x2_0 Output1 <15:0>		Valid	Valid
LUT / DLY/CNT Control Data				
reg<1543:1536>	LUT3_6 <7:0> or DLY/CNT0 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1] / Freq)	Valid	Valid
reg<1551:1544>	LUT3_7 <7:0> or DLY/CNT1 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1] / Freq)	Valid	Valid
reg<1559:1552>	LUT3_8 <7:0> or DLY/CNT2 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1] / Freq)	Valid	Valid
reg<1567:1560>	LUT3_9 <7:0> or DLY/CNT3 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1] / Freq)	Valid	Valid
reg<1575:1568>	LUT3_10 <7:0> or DLY/CNT4 Control Data	1 - 255 (Delay Time = [Counter Control Data + 1] / Freq)	Valid	Valid
reg<1577:1576>	Reserved		Valid	Invalid
reg<1579:1578>	Reserved (for SLG46583)		Valid	Invalid
reg<1581:1580>	Reserved		Valid	Invalid
reg<1583:1582>	Reserved		Valid	Invalid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1584>	UVLO1_HW_enable (Enable UVLO1 output Hard-Wire connection to LDO2/3) (for SLG46580) UVLO1_HW_enable (Enable UVLO1 output Hard-Wire connection to LDO1) (for SLG46582) UVLO_HW_enable1 (Enable UVLO output from ACMP1 Hard-Wire connection to LDO) (for SLG46583)	0: Disable UVLO1 HW connect (for SLG46580 and SLG46582) 1: Enable UVLO1 HW connect (for SLG46580 and SLG46582) 0: Disable UVLO HW connect (for SLG46583) 1: Enable UVLO HW connect (for SLG46583)	Valid	Valid
reg<1585>	UVLO0_HW_enable (Enable UVLO0 output Hard-Wire connection to LDO0/1) (for SLG46580) UVLO0_HW_enable (Enable UVLO0 output Hard-Wire connection to LDO0) (for SLG46582) UVLO_HW_enable0 (Enable UVLO output from ACMP0 Hard-Wire connection to LDO) (for SLG46583)	0: Disable UVLO0 HW connect (for SLG46580 and SLG46582) 1: Enable UVLO0 HW connect (for SLG46580 and SLG46582) 0: Disable UVLO HW connect (for SLG46583) 1: Enable UVLO HW connect (for SLG46583)	Valid	Valid
reg<1588:1586>	LDO0/1 VDD minimum Power Selection for LDO1 (for SLG46580) Reserved (for SLG46582 and SLG46583)	000: 2.3 V (for SLG46580) 001: 2.8 V (for SLG46580) 010: 3.0 V (for SLG46580) 011: 3.3 V (for SLG46580) 100: 3.6 V (for SLG46580) 101: 3.9 V (for SLG46580) 110: 4.5 V (for SLG46580) 111: 4.65 V (for SLG46580)	Valid	Valid
reg<1591:1589>	LDO0/1 VDD minimum Power Selection for LDO0 (for SLG46580) LDO0 VDD minimum Power Selection for LDO0 (for SLG46582) LDO VDD minimum Power Selection for LDO (for SLG46583)	000: 2.3 V 001: 2.8 V 010: 3.0 V 011: 3.3 V 100: 3.6 V 101: 3.9 V 110: 4.5 V 111: 4.65 V	Valid	Valid
reg<1592>	LDO0 Start-up Ramping Slope Selection (for SLG46580 and SLG46582) LDO Start-up Ramping Slope Selection (for SLG46583)	0: 10 V/ms 1: 20 V/ms	Valid	Valid
reg<1594:1593>	Reserved		Valid	Valid
reg<1599:1595>	LDO0 Vref Selection (for SLG46580 and for SLG46582) LDO Vref Selection (for SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1600>	LDO1 Start-up Ramping Slope Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: 10 V/ms (for SLG46580) 1: 20 V/ms (for SLG46580)	Valid	Valid
reg<1602:1601>	Reserved		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1607:1603>	LDO1 Vref Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1608>	LDO2 Start-up Ramping Slope Selection (for SLG46580) LDO1 Start-up Ramping Slope Selection (for SLG46582) Reserved (for SLG46583)	0: 10 V/ms (for SLG46580 and SLG46582) 1: 20 V/ms (for SLG46580 and SLG46582)	Valid	Valid
reg<1610:1609>	Reserved		Valid	Valid
reg<1615:1611>	LDO2 Vref Selection (for SLG46580) LDO1 Vref Selection (for SLG46582) Reserved (for SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1616>	LDO3 Start-up Ramping Slope Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: 10 V/ms (for SLG46580) 1: 20 V/ms (for SLG46580)	Valid	Valid
reg<1618:1617>	Reserved		Valid	Valid
reg<1623:1619>	LDO3 Vref Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
ACMP0				
reg<1628:1624>	ACMP0- IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP0- /3 11001: VDD: ACMP0- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2	Valid	Valid
reg<1630:1629>	ACMP0 Positive Input Divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X	Valid	Valid
reg<1631>	ACMP0 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1:ON	Valid	Valid
ACMP1				
reg<1636:1632>	ACMP1-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP1- /3 11001: VDD: ACMP1- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2	Valid	Valid
reg<1638:1637>	ACMP1 Positive Input Divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X	Valid	Valid
reg<1639>	ACMP1 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
ACMP2				
reg<1644:1640>	ACMP2-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP2- /3 11001: VDD: ACMP2- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2	Valid	Valid
reg<1646:1645>	ACMP2 Positive Input Divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X	Valid	Valid
reg<1647>	ACMP2 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid
ACMP3				
reg<1652:1648>	ACMP3-IN Voltage Select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: VDD: ACMP3- /3 11001: VDD: ACMP3- /4 11010: IO6: EXT_VREF 11011: IO6: EXT_VREF /2	Valid	Valid
reg<1654:1653>	ACMP3 Positive Input Divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X	Valid	Valid
reg<1655>	ACMP3 Low Bandwidth (MAX: 1MHz) Enable	0: OFF 1: ON	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
Misc.				
reg<1656>	TS_HW_enable (Enable Temp sensor output Hard-Wire connection to LDO0/1/2/3) (for SLG46580) TS_HW_enable (Enable Temp sensor output Hard-Wire connection to LDO0/1) (for SLG46582) TS_HW_enable (Enable Temp sensor output Hard-Wire connection to LDO) (for SLG46583)	0: Disable TS HW connect 1: Enable TS HW connect	Valid	Valid
reg<1657>	Switch from "Matrix OUT: LPOSC PD" to "Matrix OUT: LPOSC Force On"	0: OSC PD 1: OSC Force On (Matrix Output <60>)	Valid	Valid
reg<1658>	Switch from "Matrix OUT: OSC 25KHz/2MHz PD" to "Matrix OUT: OSC 25KHz/2MHz Force On"	0: OSC PD 1: OSC Force On (Matrix Output <59>)	Valid	Valid
reg<1659>	Reserved		Valid	Invalid
reg<1660>	Reserved		Valid	Invalid
reg<1661>	Reserved		Valid	Invalid
reg<1662>	I²C reset bit with reloading NVM into Data register	0: Keep existing condition 1: Reset execution	Valid	Valid
reg<1663>	IO Latching Enable During I²C Write Interface	0: Disable 1: Enable	Valid	Invalid
reg<1671:1664>	RAM 8 outputs for ASM-state0		Valid	Valid
reg<1679:1672>	RAM 8 outputs for ASM-state1		Valid	Valid
reg<1687:1680>	RAM 8 outputs for ASM-state2		Valid	Valid
reg<1695:1688>	RAM 8 outputs for ASM-state3		Valid	Valid
reg<1703:1696>	RAM 8 outputs for ASM-state4		Valid	Valid
reg<1711:1704>	RAM 8 outputs for ASM-state5		Valid	Valid
reg<1719:1712>	RAM 8 outputs for ASM-state6		Valid	Valid
reg<1727:1720>	RAM 8 outputs for ASM-state7		Valid	Valid
reg<1735:1728>	User configurable RAM / OTP Byte 0		Valid	Valid
reg<1743:1736>	User configurable RAM / OTP Byte 1		Valid	Valid
reg<1751:1744>	User configurable RAM / OTP Byte 2		Valid	Valid
reg<1759:1752>	User configurable RAM / OTP Byte 3		Valid	Valid
reg<1767:1760>	User configurable RAM / OTP Byte 4		Valid	Valid
reg<1775:1768>	User configurable RAM / OTP Byte 5		Valid	Valid
reg<1783:1776>	User configurable RAM / OTP Byte 6		Valid	Valid
reg<1791:1784>	User configurable RAM / OTP Byte 7		Valid	Valid
reg<1792>	LDO0_EN_Gate (By this bit=1, Matrix Output: LDO0_EN will be enabled.) (for SLG46580 and SLG46582) LDO_EN_Gate (By this bit=1, Matrix Output: LDO_EN will be enabled.) (for SLG46583)	0: Disable 1: Enable	Valid	Valid
reg<1793>	LDO0 VOUT_SEL_Gate (for SLG46580 and SLG46582) LDO VOUT_SEL_Gate (for SLG46583)	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1794>	Mode1_EN_Gate (By this bit=1, Matrix Output: LDO MODE1_Enable for LDO0/1/2/3 will be enabled.) (for SLG46580) Mode1_EN_Gate (By this bit=1, Matrix Output: LDO MODE1_Enable for LDO0/1 will be enabled.) (for SLG46582) Mode1_EN_Gate (By this bit=1, Matrix Output: LDO MODE1_Enable for LDO will be enabled.) (for SLG46583)	0: Disable LDO_LP_MODE_EN matrix output (for SLG46580) 1: Enable LDO_LP_MODE_ EN matrix output (for SLG46580) 0: Disable (for SLG46582 and SLG46583) 1: Enable (for SLG46582 and SLG46583)	Valid	Valid
reg<1799:1795>	LDO0 2nd Vref Selection (for SLG46580 and SLG46582) LDO 2nd Vref Selection (for SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1800>	LDO1_EN_Gate (By this bit=1, Matrix Output: LDO1_EN will be enabled.) (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (for SLG46580)	Valid	Valid
reg<1801>	LDO1 VOUT_SEL_Gate (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Default VOUT selection (for SLG46580) 1: Enable 2nd VOUT selection (for SLG46580)	Valid	Valid
reg<1802>	Reserved		Valid	Valid
reg<1807:1803>	LDO1 2nd Vref Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1808>	LDO2_EN_Gate (By this bit=1, Matrix Output: LDO2_EN will be enabled.) (for SLG46580) LDO1_EN_Gate (By this bit=1, Matrix Output: LDO1_EN will be enabled.) (for SLG46582) Reserved (for SLG46583)	0: Disable (for SLG46580) 1: Enable (for SLG46580) 0: Disable LDO1_EN matrix output (for SLG46582) 1: Enable LDO1_EN matrix output (for SLG46582)	Valid	Valid
reg<1809>	LDO2 VOUT_SEL_Gate (for SLG46580) LDO1 VOUT_SEL_Gate (for SLG46582) Reserved (for SLG46583)	0: Default VOUT selection 1: Enable 2nd VOUT selection	Valid	Valid
reg<1810>	Reserved		Valid	Valid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1815:1811>	LDO2 2nd Vref Selection (for SLG46580) LDO1 2nd Vref Selection (for SLG46582) Reserved (for SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1816>	LDO3_EN_Gate (By this bit=1, Matrix Output: LDO3_EN will be enabled.) (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Disable (for SLG46580) 1: Enable (for SLG46580)	Valid	Valid
reg<1817>	LDO3 VOUT_SEL_Gate (for SLG46580) Reserved (for SLG46582 and SLG46583)	0: Default VOUT selection (for SLG46580) 1: Enable 2nd VOUT selection (for SLG46580)	Valid	Valid
reg<1818>	Reserved		Valid	Valid
reg<1823:1819>	LDO3 2nd Vref Selection (for SLG46580) Reserved (for SLG46582 and SLG46583)	00000:0.90v, 00001:1.00v, 00010:1.05v, 00011:1.10v, 00100:1.20v, 00101:1.25v, 00110:1.35v, 00111:1.50v, 01000:1.67v, 01001:1.80v, 01010:1.90v, 01011:2.00v, 01100:2.10v, 01101:2.20v, 01110:2.30v, 01111:2.40v, 10000:2.50v, 10001:2.60v, 10010:2.70v, 10011:2.80v, 10100:2.90v, 10101:3.00v, 10110:3.10v, 10111:3.20v, 11000:3.30v, 11001:3.40v, 11010:3.50v, 11011:3.60v, 11100:4.00v, 11101:4.10v, 11110:4.20v, 11111:4.35v	Valid	Valid
reg<1831:1824>	Reserved		Valid	Valid
reg<1832>	NVM Data Read Disable (From NVM): ID[24] for BANK0/1/2 only	0: Disable (Programmed data can be read.) 1: Enable (Programmed data can't be read.)	Valid	Invalid
reg<1833>	Reserved		Valid	Invalid
reg<1835:1834>	Reserved		Valid	Invalid
reg<1839:1836>	Reserved		Valid	Invalid
reg<1847:1840>	8-bit Pattern ID Byte 0 (From NVM): ID[23:16]		Valid	Valid
reg<1855:1848>	Reserved		Valid	Invalid
reg<1863:1856>	Reserved		Valid	Invalid
reg<1867:1864>	I²C Control Code Bit [3:0]	Value for slave address	Valid	Invalid
reg<1868>	I²C 1MHz operation enable	0: Up to 400 kHz 1: 1 MHz operation	Valid	Invalid
reg<1869>	Reserved		Valid	Invalid
reg<1870>	BANK0/1/2/3 I²C-write protection bit	0: Writable 1: Non-writable	Valid	Invalid
reg<1871>	BANK0/1/2 I²C-write protection bit	0: Writable 1: Non-writable	Valid	Invalid
reg<1872>	Reserved		Invalid	Invalid
reg<1874:1873>	Reserved		Invalid	Invalid

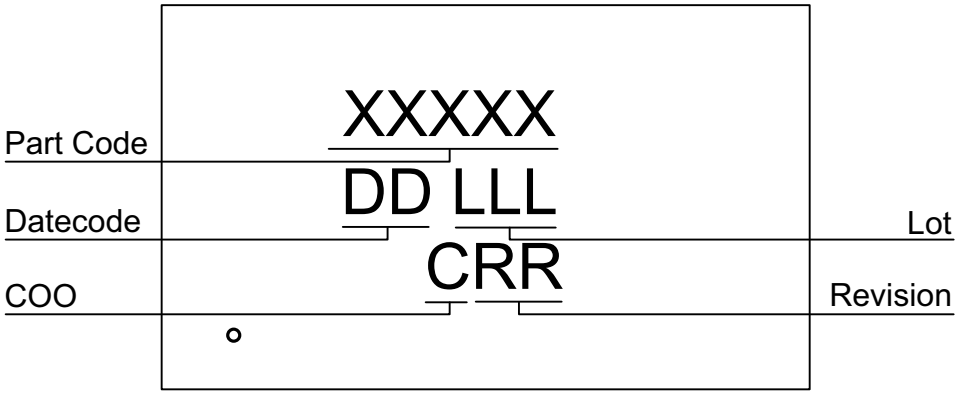
Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1876:1875>	Reserved		Invalid	Invalid
reg<1879:1877>	Reserved		Invalid	Invalid
reg<1880>	Reserved		Invalid	Invalid
reg<1881>	Reserved		Invalid	Invalid
reg<1882>	Reserved		Invalid	Invalid
reg<1887:1883>	Reserved		Invalid	Invalid
reg<1891:1888>	Reserved		Invalid	Invalid
reg<1895:1892>	Reserved		Invalid	Invalid
reg<1899:1896>	Reserved		Invalid	Invalid
reg<1903:1900>	Reserved		Invalid	Invalid
reg<1904>	Reserved		Invalid	Invalid
reg<1905>	Reserved		Invalid	Invalid
reg<1907:1906>	Reserved		Invalid	Invalid
reg<1911:1908>	Reserved		Invalid	Invalid
reg<1919:1912>	ASM State output <7:0>		Valid	Invalid
Matrix Input				
reg<1920>	Matrix Input 0	GND	Valid	Invalid
reg<1921>	Matrix Input 1	IO0 Digital Input	Valid	Invalid
reg<1922>	Matrix Input 2	IO1 Digital Input	Valid	Invalid
reg<1923>	Matrix Input 3	IO2 Digital Input	Valid	Invalid
reg<1924>	Matrix Input 4	IO3 Digital Input	Valid	Invalid
reg<1925>	Matrix Input 5	IO4 Digital Input	Valid	Invalid
reg<1926>	Matrix Input 6	LUT2_0 / DFF0 Output	Valid	Invalid
reg<1927>	Matrix Input 7	LUT2_1 / DFF1 Output	Valid	Invalid
reg<1928>	Matrix Input 8	LUT2_2 / DFF2 Output	Valid	Invalid
reg<1929>	Matrix Input 9	LUT3_0 / DFF3 Output	Valid	Invalid
reg<1930>	Matrix Input 10	LUT3_1 / DFF4 Output	Valid	Invalid
reg<1931>	Matrix Input 11	LUT3_2 / DFF5 Output	Valid	Invalid
reg<1932>	Matrix Input 12	LUT3_3 / DFF6 Output	Valid	Invalid
reg<1933>	Matrix Input 13	LUT3_4 / DFF7 Output	Valid	Invalid
reg<1934>	Matrix Input 14	LUT3_6 / CNT_DLY0(8bit) Output	Valid	Invalid
reg<1935>	Matrix Input 15	LUT3_7 / CNT_DLY1(8bit) Output	Valid	Invalid
reg<1936>	Matrix Input 16	LUT3_8 / CNT_DLY2(8bit) Output	Valid	Invalid
reg<1937>	Matrix Input 17	LUT3_9 / CNT_DLY3(8bit) Output	Valid	Invalid
reg<1938>	Matrix Input 18	LUT3_10 / CNT_DLY4(8bit) Output	Valid	Invalid
reg<1939>	Matrix Input 19	LUT3_11 / Pipe Delay (1st stage) Output / Ripple counter Q<0>	Valid	Invalid
reg<1940>	Matrix Input 20	LUT3_5 / DFF8 Output	Valid	Invalid
reg<1941>	Matrix Input 21	LUT4X2 Output0	Valid	Invalid
reg<1942>	Matrix Input 22	LUT4X2 Output1	Valid	Invalid
reg<1943>	Matrix Input 23	RTC CNT 1 second Output	Valid	Invalid
reg<1944>	Matrix Input 24	RTC DCOMP Output	Valid	Invalid
reg<1945>	Matrix Input 25	Pipe Delay Output0 / Ripple counter Q<1>	Valid	Invalid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1946>	Matrix Input 26	Pipe Delay Output1 / Ripple counter Q<2>	Valid	Invalid
reg<1947>	Matrix Input 27	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz)	Valid	Invalid
reg<1948>	Matrix Input 28	Internal OSC Post-Divided by 1/2/3/4/8/12/24/64 Output (25KHz/2MHz)	Valid	Invalid
reg<1949>	Matrix Input 29	LPOSC Output	Valid	Invalid
reg<1950>	Matrix Input 30	Filter0 / Edge Detect0 Output	Valid	Invalid
reg<1951>	Matrix Input 31	Filter1 / Edge Detect1 Output	Valid	Invalid
reg<1952>	Matrix Input 32	I2C_virtual_0 Input	Valid	Valid
reg<1953>	Matrix Input 33	I2C_virtual_1 Input	Valid	Valid
reg<1954>	Matrix Input 34	I2C_virtual_2 Input	Valid	Valid
reg<1955>	Matrix Input 35	I2C_virtual_3 Input	Valid	Valid
reg<1956>	Matrix Input 36	I2C_virtual_4 Input	Valid	Valid
reg<1957>	Matrix Input 37	I2C_virtual_5 Input	Valid	Valid
reg<1958>	Matrix Input 38	I2C_virtual_6 Input	Valid	Valid
reg<1959>	Matrix Input 39	I2C_virtual_7 Input	Valid	Valid
reg<1960>	Matrix Input 40	RAM_0 Output for ASM-state	Valid	Invalid
reg<1961>	Matrix Input 41	RAM_1 Output for ASM-state	Valid	Invalid
reg<1962>	Matrix Input 42	RAM_2 Output for ASM-state	Valid	Invalid
reg<1963>	Matrix Input 43	RAM_3 Output for ASM-state	Valid	Invalid
reg<1964>	Matrix Input 44	RAM_4 Output for ASM-state	Valid	Invalid
reg<1965>	Matrix Input 45	RAM_5 Output for ASM-state	Valid	Invalid
reg<1966>	Matrix Input 46	RAM_6 Output for ASM-state	Valid	Invalid
reg<1967>	Matrix Input 47	RAM_7 Output for ASM-state	Valid	Invalid
reg<1968>	Matrix Input 48		Valid	Invalid
reg<1969>	Matrix Input 49	LDO0 FAULTB (for SLG46580 and SLG46582) LDO FAULTB (for SLG46583)	Valid	Invalid
reg<1970>	Matrix Input 50	LDO1 FAULTB (for SLG46580) GND (for SLG46582 and SLG46583)	Valid	Invalid
reg<1971>	Matrix Input 51	LDO2 FAULTB (for SLG46580) LDO1 FAULTB (for SLG46582) GND (for SLG46583)	Valid	Invalid
reg<1972>	Matrix Input 52	LDO3 FAULTB (for SLG46580) GND (for SLG46582 and SLG46583)	Valid	Invalid
reg<1973>	Matrix Input 53	IO5 Digital Input (GPI)	Valid	Invalid
reg<1974>	Matrix Input 54	IO6 Digital Input	Valid	Invalid
reg<1975>	Matrix Input 55	IO7 Digital Input	Valid	Invalid
reg<1976>	Matrix Input 56	IO8 Digital Input	Valid	Invalid
reg<1977>	Matrix Input 57	ACMP_0 Output	Valid	Invalid
reg<1978>	Matrix Input 58	ACMP_1 Output	Valid	Invalid
reg<1979>	Matrix Input 59	ACMP_2 Output	Valid	Invalid
reg<1980>	Matrix Input 60	ACMP_3 Output	Valid	Invalid

Register Bit Address	Signal Function	Register Bit Definition	I²C Interface	
			I²C Read	I²C Write
reg<1981>	Matrix Input 61	Programmable Delay with Edge Detector Output	Valid	Invalid
reg<1982>	Matrix Input 62	nRST_core as matrix input	Valid	Invalid
reg<1983>	Matrix Input 63	VDD	Valid	Invalid
Reserved				
reg<1991:1984>	Reserved		Valid	Invalid
reg<1999:1992>	Reserved		Valid	Invalid
reg<2007:2000>	Reserved		Valid	Invalid
reg<2015:2008>	Reserved		Valid	Valid
reg<2023:2016>	Reserved		Valid	Invalid
reg<2031:2024>			Valid	Invalid
reg<2032>	Reserved		Valid	Valid
reg<2033>			Valid	Valid
reg<2034>	Reserved		Valid	Valid
reg<2035>	Reserved Reserved Reserved		Valid	Invalid
reg<:2039:2036>	Reserved		Valid	Valid
reg<2047:2040>	Reserved		Valid	Valid

26.0 Package Top Marking System Definition

26.1 STQFN 20L 2x3mm 0.4P FCD Package

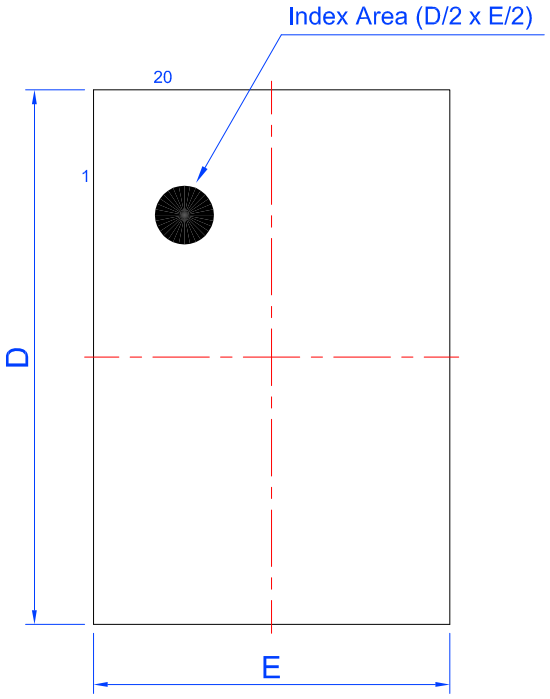


XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

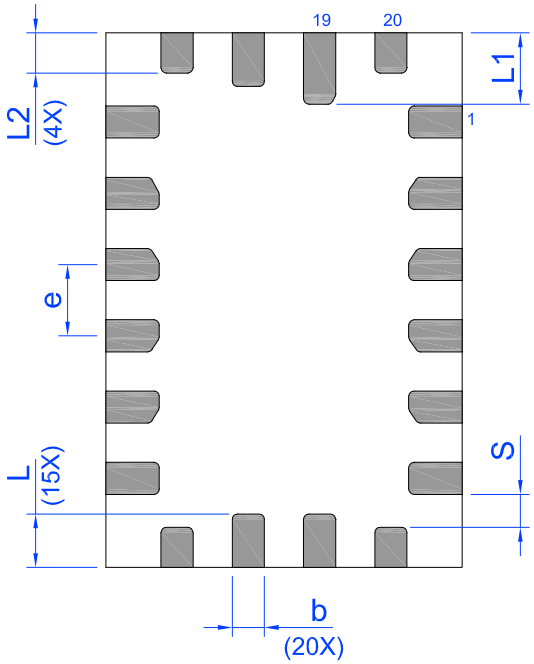
27.0 Package Drawing and Dimensions

27.1 STQFN 20L 2x3mm 0.4P FCD Package

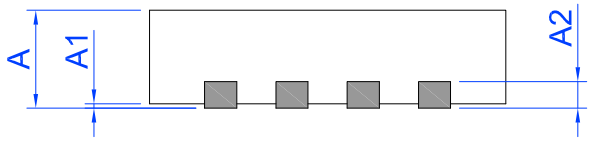
JEDEC MO-220, Variation WECE
IC Net Weight: 0.008 g



Marking View



BTM View



Side View

Unit: mm

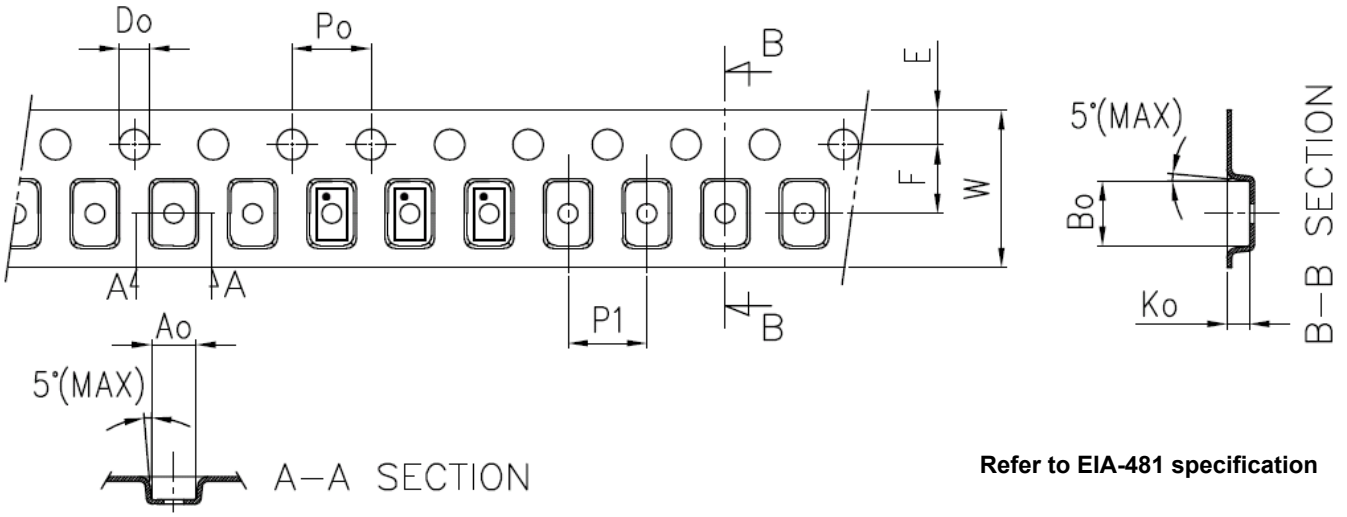
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			L2	0.175	0.225	0.275
S	0.185 TYP						

28.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3 mm 0.4P FCD	20	2 x 3 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

28.1 Carrier Tape Drawing and Dimensions

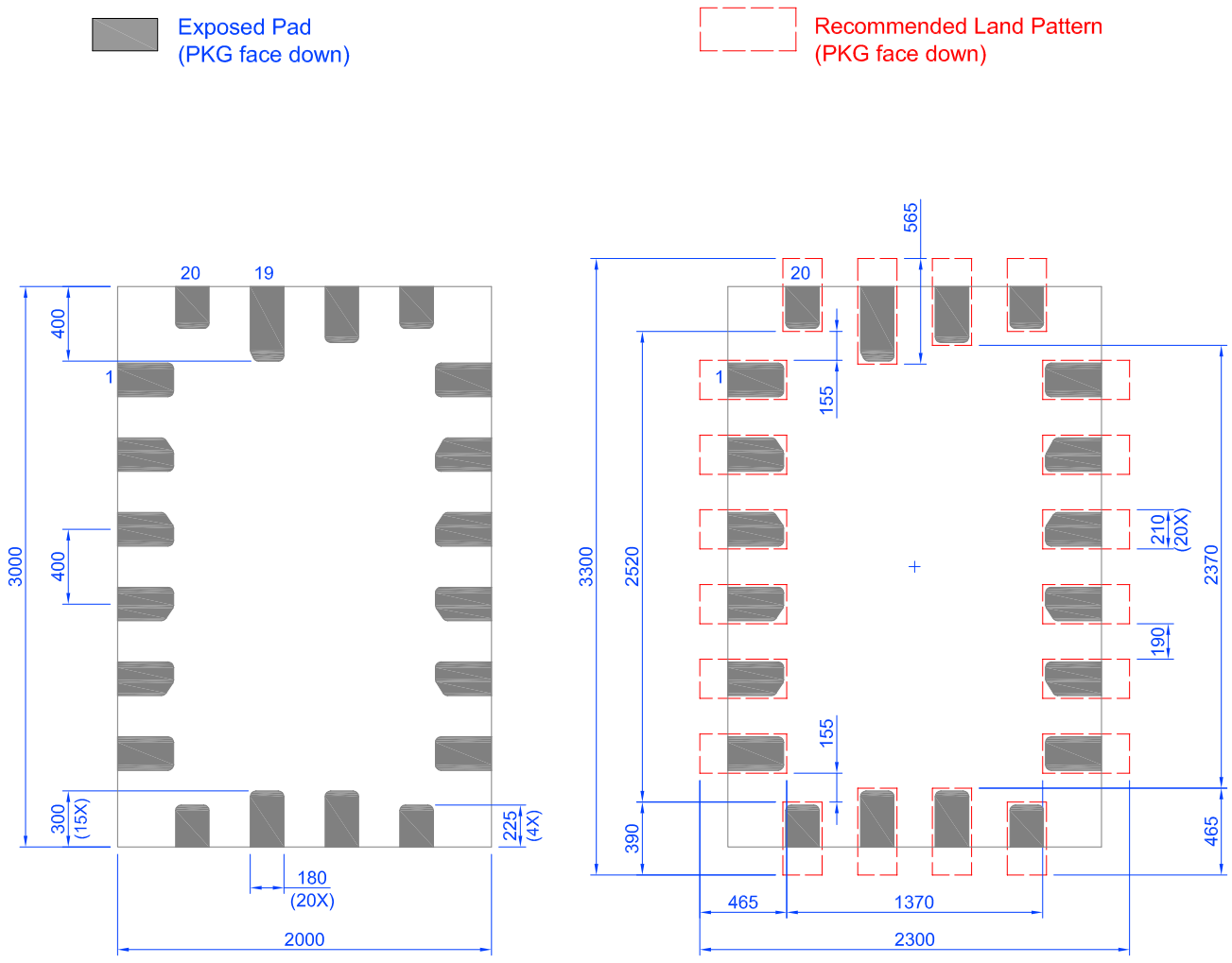
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

29.0 Recommended Land Pattern

29.1 STQFN 20L 2x3mm 0.4P FCD Package



Unit:um

Note 1: Pins 11 and 13 must be shorted externally, Pins 14 and 16 must be shorted externally for SLG46582.

Note 2: Pins 12 and 15 must be shorted externally, Pins 11, 13, 14 and 16 must be shorted externally for SLG46583.

30.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

31.0 Revision History

Date	Version	Change
3/27/2024	1.16	Corrected table 1.73 kHz RC OSC1 Frequency Limits
1/24/2024	1.15	Updated tables LDO Output Voltage Selection
12/19/2023	1.14	Updated table LDO HP MODE Electrical Spec Updated 3 LDO sections Over-Current Limit and Short-Circuit Detection
8/18/2023	1.13	Added notes to sections SLG46580/82/83 Low Dropout Regulators Fixed typos
5/29/2023	1.12	Added IC Net Weight in section Package Drawing and Dimensions
3/3/2023	1.11	Added notes to section Ordering Information
2/16/2023	1.10	Corrected tables LDO HP MODE Electrical Specifications and LDO LP MODE Electrical Specifications
9/7/2022	1.09	Updated Ordering Information
5/17/2022	1.08	Corrected sections Over-Current Limit and Short-Circuit Detection
3/4/2022	1.07	Updated R_{PUP} and R_{PDWN} in section Electrical Characteristics Renesas rebranding Updated section CNT/DLY/FSM Timing Diagrams Corrected Reset Command Timing figure Updated Pin Block Diagrams
10/25/2019	1.06	Updated disclaimer
9/18/2019	1.05	Added graphs in subsection Oscillator Accuracy Updated 1.73 kHz OSC Frequency Limits and Errors Corrected Low Power Oscillator frequency Added section ACMPs Typical Performance Corrected LDO mode name Fixed typos
3/29/2019	1.04	Corrected LDO Connection Block Diagram Updated registers <1047:1045> Added Parameter Short Circuit Protection Updated Registers Read/Write Protection Options Fixed typos
12/17/2018	1.03	Updated after review Updated Oscillator Power-On Delay graphs Added new subsections LDO efficiency
11/13/2018	1.02	Updated to Dialog style
10/23/2018	1.01	Updated SLG46853 LDO Electrical Spec Updated Oscillator Startup Diagram
8/20/2018	1.00	Production Release

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