SLG46857-A

Auto AEC-Q100 Qualified GreenPAK Programmable Mixed-Signal Matrix

The SLG46857-A provides a small, low power component for commonly used Mixed-Signal functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, and the macrocells of the SLG46857-A.

This highly versatile device allows a wide variety of Mixed-Signal functions to be designed within a very small, low power single integrated circuit.

Features

- Two High Speed General Purpose Analog Comparators (ACMPxH)
- Two Low Power General Purpose Analog Comparators (ACMPxL)
- Two Voltage References (Vref)
  - Two Vref Outputs
- Fifteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Nine Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter, or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUTs
- Eight Multi-Function Macrocells
  - Seven Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators (OSC)
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On Reset (POR)
- Read Back Protection (Read Lock)
- Power Supply
  - 2.5 V (±8 %) to 5.0 V (±10 %)
- Ambient Operating Temperature Range: -40 °C to 125 °C
- RoHS Compliant/Halogen-Free
- Available Package
- 14-pin STQFN: 3.0 mm x 3.1 mm x 0.75 mm, 0.65 mm pitch
- AEC-Q100 (T_A = -40 °C to +125 °C) Qualified

Applications

- Infotainment
- E/E Architecture
- Powertrain
- xEV
- Chassis/Body

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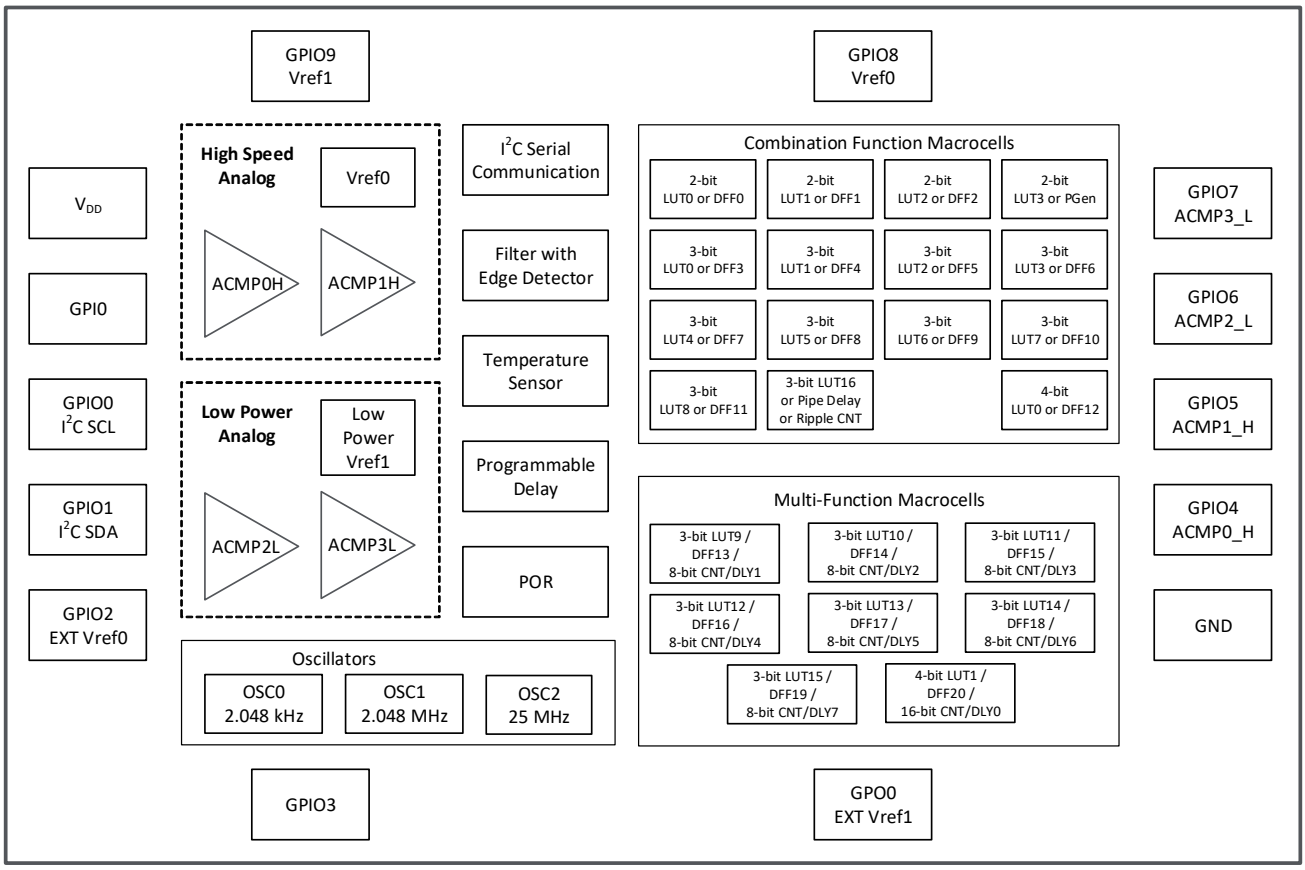

Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

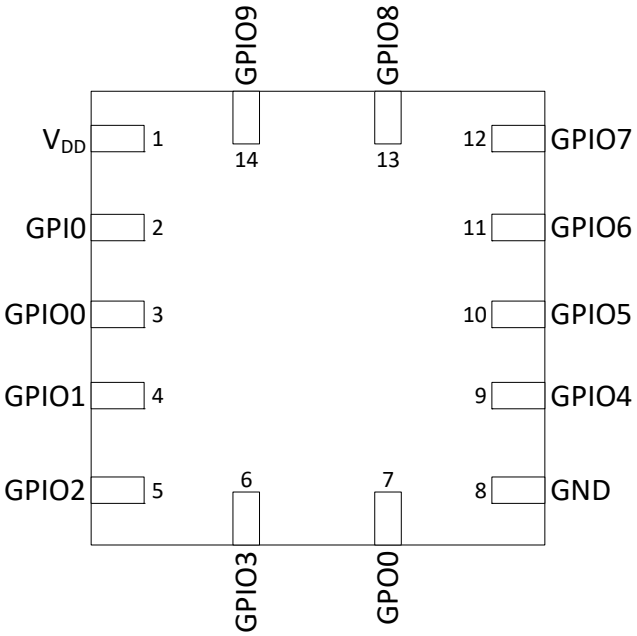

Figure 2. Pin Assignments - STQFN - 14L

2.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Description
1	V_{DD}	Power Supply
2	GPI0	GPI, SLA_0
3	GPIO0	GPIO, SCL
4	GPIO1	GPIO, SDA
5	GPIO2	GPIO with OE, EXT_Vref0, SLA_1
6	GPIO3	GPIO with OE
7	GPO0	GPO, EXT_Vref1
8	GND	Ground
9	GPIO4	GPIO with OE, ACMP0_H+, SLA_2
10	GPIO5	GPIO with OE, ACMP1_H+, SLA_3
11	GPIO6	GPIO with OE, ACMP2_L+
12	GPIO7	GPIO with OE, ACMP3_L+
13	GPIO8	GPIO with OE, Vref0_OUT, TS_OUT
14	GPIO9	GPIO with OE, Vref1_OUT

Table 2. Pin Type Definitions

Pin type	Definition
V_{DD}	Power Supply
GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output
SCL	I^2C Serial Clock Input
SDA	I^2C Serial Data Input/Output
GND	General Ground

Table 3. Functional Pin Description

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DD}	V_{DD}	Power Supply	--	--
		ACMP0_H+	Analog Comparator 0 Positive Input	Analog	--
		ACMP1_H+	Analog Comparator 1 Positive Input	Analog	--
		ACMP2_L+	Analog Comparator 2 Positive Input	Analog	--
		ACMP3_L+	Analog Comparator 3 Positive Input	Analog	--
2	GPI0	GPI0	General Purpose Input	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		Slave Address 0		--	--
3	GPIO0	GPIO0	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	
				Low Voltage Digital Input	--
		SCL	I^2C Serial Clock	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--

Table 3. Functional Pin Description (Cont.)

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
4	GPIO1	GPIO1	General Purpose IO	Digital Input without Schmitt Trigger	Open-Drain NMOS (3.2x)
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
		SDA	I^2C Serial Data	Digital Input without Schmitt Trigger	--
				Digital Input with Schmitt Trigger	--
				Low Voltage Digital Input	--
5	GPIO2	GPIO2	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Slave Address 1		--	--
		EXT_VREF0	Analog Comparator Negative Input	Analog	--
6	GPIO3	GPIO3	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
7	GPO0	GPO0	General Purpose Output	--	Push-Pull (1x) (2x)
				--	Open-Drain NMOS (1x) (2x) (4x)
		EXT_VREF1	Analog Comparator Negative Input	Analog	--
8	GND	GND	Power Supply	--	--
9	GPIO4	GPIO4	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x) (4x)
				Low Voltage Digital Input	--
		ACMP0_H+	Analog Comparator 0_H Positive Input	Analog	--
		Slave Address 2		--	--

Table 3. Functional Pin Description (Cont.)

STQFN 14L Pin #	Pin Name	Signal Name	Function	Input Options	Output Options
10	GPIO5	GPIO5	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP1_H+	Analog Comparator 1_H Positive Input	Analog	--
		Slave Address 3		--	--
11	GPIO6	GPIO6	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP2_L+	Analog Comparator 2_L Positive Input	Analog	--
12	GPIO7	GPIO7	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		ACMP3_L+	Analog Comparator 3_L Positive Input	Analog	--
13	GPIO8	GPIO8	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Vref0	Vref0 Output	Analog	--
14	GPIO9	GPIO9	General Purpose IO with OE [1]	Digital Input without Schmitt Trigger	Push-Pull (1x) (2x)
				Digital Input with Schmitt Trigger	Open-Drain NMOS (1x) (2x)
				Low Voltage Digital Input	--
		Vref1	Vref1 Output	Analog	--

[1] General Purpose IO's with OE can be used to implement bidirectional signals under user control via Connection Matrix to OE signal in IO structure.

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 4. Absolute Maximum Ratings

Parameter		Min	Max	Unit
Supply Voltage on V_{DD} relative to GND		-0.3	7	V
DC Input Voltage		GND - 0.5 V	V_{DD} + 0.5 V	V
Maximum Average or DC Current through V_{DD} pin		--	26	mA
Maximum Average or DC Current through GND pin		--	67	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	5	mA
	Push-Pull 2x	--	10	
	Push-Pull 4x	--	20	
	Open-Drain 1x	--	5	
	Open-Drain 2x	--	10	
	Open-Drain 4x	--	20	
Current at Input Pin		-1.0	1.0	mA
Input Leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Moisture Sensitive Level		1		

3.2 Electrostatic Discharge Ratings

Table 5. Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V

3.3 Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DD})		2.3	5.5	V
Operating Ambient Temperature		-40	125	°C
Maximal Voltage Applied to any PIN in High Impedance State		--	V_{DD}+ 0.3	V
Capacitor Value at V_{DD}		0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	0	V_{DD}	V

3.4 Electrical Specifications

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	HIGH-Level Input Voltage	Logic Input [1]	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic Input with Schmitt Trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-Level Logic Input [1]	1.25	--	V_{DD}+ 0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input [1]	GND-0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2x V_{DD}	V
		Low-Level Logic Input [1]	GND-0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.3 V	0.27	0.40	0.59	V
		V_{DD} = 3.3 V	0.33	0.44	0.59	V
		V_{DD} = 5.5 V	0.49	0.60	0.75	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	HIGH-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.3 V, I_{OH} = 1 mA	2.16	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, I_{OH} = 3 mA	3.00	--	--	V
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, I_{OH} = 5 mA	5.18	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, I_{OH} = 1 mA	2.23	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 3.3, I_{OH} = 3 mA	3.15	--	--	V
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, I_{OH} = 5 mA	5.33	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OH} = 1 mA	2.26	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OH} = 3mA	3.22	--	--	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OH} = 5 mA	5.41	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull, 1x Drive, V_{DD} = 2.3 V, I_{OL}= 1 mA	--	--	0.105	V
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.240	V
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, I_{OL}= 5 mA	--	--	0.286	V
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.052	V
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, I_{OL}= 3 mA	--	--	0.118	V
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.144	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.025	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OL}= 3 mA	--	--	0.058	V
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.070	V
		NMOS OD, 1x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.045	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	NMOS OD, 1x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.099	V
		NMOS OD, 1x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.123	V
		NMOS OD, 2x Drive, V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.021	V
		NMOS OD, 2x Drive, V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.049	V
		NMOS OD, 2x Drive, V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.061	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, I_{OL} = 1 mA	--	--	0.009	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, I_{OL} = 3 mA	--	--	0.023	V
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, I_{OL} = 5 mA	--	--	0.029	V
I_{OH}	HIGH-Level Output Pulse Current [2]	Push-Pull, 1x Drive, V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2	1.39	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, V_{OH} = 2.4 V	7.46	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, V_{OH} = 2.75 V	26.18	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2	2.72	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, V_{OH} = 2.4 V	14.55	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, V_{OH} = 2.75 V	50.38	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OH} = V_{DD} - 0.2	5.24	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OH} = 2.4 V	27.69	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OH} = 2.75 V	94.38	--	--	mA

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	LOW-Level Output Pulse Current [2]	Push-Pull, 1x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	1.84	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	4.78	--	--	mA
		Push-Pull, 1x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	6.78	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	3.65	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	9.46	--	--	mA
		Push-Pull, 2x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	13.26	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OL} = 0.2 V	7.14	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OL} = 0.4 V	19.02	--	--	mA
		Push-Pull, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OL} = 0.4 V	26.98	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	4.48	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	11.62	--	--	mA
		NMOS OD, 1x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	16.12	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 2.3 V, V_{OL} = 0.2 V	8.80	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 3.3 V, V_{OL} = 0.4 V	22.54	--	--	mA
		NMOS OD, 2x Drive, V_{DD} = 5.5 V, V_{OL} = 0.4 V	31.06	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 2.3 V, V_{OL} = 0.2 V	18.07	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 3.3 V, V_{OL} = 0.4 V	46.69	--	--	mA
		NMOS OD, 4x Drive (only for GPO0 and GPIO4), V_{DD} = 5.5 V, V_{OL} = 0.4 V	64.95	--	--	mA
T_{SU}	Startup Time	T_{RAMP} = 10 ms	--	1.5	2.1	ms
PON_{THR}	Power-On Threshold	V_{DD} Level Required to Start Up the Chip	1.56	1.84	2.03	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
$POFF_{THR}$	Power-Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.43	1.07	1.63	V
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{IN}	Input Capacitance			4		pF
I_{LKG}	Logic Input without Schmitt Trigger (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	14	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	16	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	20	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	11	--	nA
	Logic Input with Schmitt Trigger (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	15	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	16	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	20	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	11	--	nA
	Low-Level Logic Input (Floating) Leakage	Vin = V_{DD}, V_{DD} = 2.3 V, All Pins	--	15	--	nA
		Vin = V_{DD}, V_{DD} = 3.3 V, All Pins	--	16	--	nA
		Vin = V_{DD}, V_{DD} = 5.5 V, All Pins	--	20	--	nA
		Vin = 0, V_{DD} = 2.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 3.3 V, All Pins	--	5	--	nA
		Vin = 0, V_{DD} = 5.5 V, All Pins	--	11	--	nA

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

3.5 I²C Pins Electrical Specifications

Table 8. ES of the I²C Pins for DI Mode at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode plus		Unit
			Min	Max	Min	Max	
V_{IL}	LOW-level Input Voltage		-0.5	0.3xV_{DD}	-0.5	0.3xV_{DD}	V
V_{IH}	HIGH-level Input Voltage		0.7xV_{DD}	5.5	0.7xV_{DD}	5.5	V
V_{HYS}	Hysteresis of Schmitt Trigger Inputs		0.05xV_{DD}	--	0.05xV_{DD}	--	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3mA sink current V_{DD} > 2.3 V	0	0.4	0	0.4	V
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current V_{DD} = 2.3 V	0	0.2xV_{DD}	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current [1]	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	19.5	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	mA
		V_{OL}= 0.6 V	6	--	--	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} [1]		14x (V_{DD}/5.5V)	250	10x (V_{DD}/5.5V)	120	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	0	50	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	--	10	pF

[1] Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5V) (min); For Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V.
[2] For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [789] in section 17. Register Definitions.

Table 9. ES of the I²C Pins for DILV Mode at T_A = -40°C to +125°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted

Parameter	Description	Condition	Fast-mode		Unit
			Min	Max	
V_{IL}	LOW-level Input Voltage [1]		GND-0.3	0.5	V
V_{IH}	HIGH-level Input Voltage [1]		1.25	V_{DD}+0.3	V
V_{OL1}	LOW-Level Output Voltage 1	(Open-Drain or open collector) at 3mA sink current V_{DD} > 2.3 V	0	0.4	V

Table 9. ES of the I²C Pins for DILV Mode at T_A = -40°C to +125°C, V_{DD} = 2.3V to 5.5V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Fast-mode		Unit
			Min	Max	
V_{OL2}	LOW-Level Output Voltage 2	(Open-Drain or open collector) at 2 mA sink current V_{DD} = 2.3 V	0	0.2xV_{DD}	V
I_{OL}	LOW-Level Output Current	V_{OL} = 0.4 V, V_{DD} = 2.3 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	mA
		V_{OL}= 0.6 V	6	--	mA
t_{of}	Output Fall Time from V_{IHmin} to V_{ILmax} [1]		14x (V_{DD}/5.5V)	250	ns
t_{SP}	Pulse Width of Spikes that must be suppressed by the Input Filter		0	50	ns
I_i	Input Current each IO Pin	0.1xV_{DD} < V_I < 0.9xV_{DDmax}	-10	+10	µA
C_i	Capacitance for each IO Pin		--	10	pF

[1] Does not meet standard I²C specifications: V_{IL} = -0.5 V (min), V_{IL} = 0.3xV_{DD} (max), V_{IH} = 0.7xV_{DD} (min), V_{IH} = 5.5 V (max), t_{of} = 20x(V_{DD}/5.5V) (min).

Table 10. I²C Pins Timing Specifications, DI Mode, T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL		--	--	400	--	--	1000	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	--	500	--	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	--	260	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA)[1]	V_{DD}= 2.5 V ±8 %	--	--	80	--	--	87	ns
		V_{DD}= 3.3 V±10%	--	--	87	--	--	87	
		V_{DD}= 5.5 V±10%	--	--	89	--	--	87	
t_{VD_ACK}	Data Valid Acknowledge Time		--	--	900	--	--	450	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	500	--	--	ns
t_{HD_STA}	Start Hold Time		600	--	--	260	--	--	ns
t_{SU_STA}	Start Set-up Time		600	--	--	260	--	--	ns
t_{HD_DAT}	Data Hold Time	Rising Edge	0	--	--	0	--	--	ns
		Falling Edge	0	--	--	0	--	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	--	50	--	--	ns
t_R	Inputs Rise Time	C = 15 pF	--	--	300	--	--	120	ns
		C = 100 pF	--	--	300	--	--	120	ns
		C = 400 pF	--	--	300	--	--	120	ns

Table 10. I²C Pins Timing Specifications, DI Mode, T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed						Unit
			400 kHz			1 MHz			
			Min	Typ	Max	Min	Typ	Max	
t_F	Inputs Fall Time	C = 15 pF	--	--	300	--	--	120	ns
		C = 100 pF	--	--	300	--	--	120	ns
		C = 400 pF	--	--	300	--	--	120	ns
t_{SU_STO}	Stop Set-up Time		600	--	--	260	--	--	ns
t_{VD_DAT}	Data Valid Time		50	--	--	50	--	--	ns

[1] Does not meet standard I²C specifications: t_I = 95 ns for V_{DD} = 2.3 V, t_I = 95 ns for V_{DD} = 3.3 V, t_I = 111 ns for V_{DD} = 5.5V for 400 kHz; t_I = 168 ns for V_{DD} = 2.3 V, t_I = 157 ns for V_{DD} = 3.3 V, t_I = 156 ns for V_{DD} = 5.5 V for 1 MHz.
[2] Timing diagram can be found in the Figure 105.
[3] Please follow official I²C spec UM10204.

Table 11. I²C Pins Timing Specifications, DILV Mode, T_A = -40°C to +125°C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Speed			Unit
			400 kHz			
			Min	Typ	Max	
F_{SCL}	Clock Frequency, SCL		--	--	400	kHz
t_{LOW}	Clock Pulse Width Low		1300	--	--	ns
t_{HIGH}	Clock Pulse Width High		600	--	--	ns
t_I	Input Filter Spike Suppression (SCL, SDA) [1]	V_{DD} = 2.3 V ± 8 %	--	--	300	ns
		V_{DD} = 3.3 V ± 10 %	--	--	235	
		V_{DD} = 5.5 V ± 10 %	--	--	187	
t_{VD_ACK}	Data Valid Acknowledge Time		--	--	900	ns
t_{BUF}	Bus Free Time between Stop and Start		1300	--	--	ns
t_{HD_STA}	Start Hold Time		600	--	--	ns
t_{SU_STA}	Start Set-up Time		600	--	--	ns
t_{HD_DAT}	Data Hold Time [1]	Rising Edge	0.3	--	--	ns
		Falling Edge	0	--	--	ns
t_{SU_DAT}	Data Set-up Time		100	--	--	ns
t_R	Inputs Rise Time	C = 15 pF	--	--	300	ns
		C = 100 pF	--	--	300	ns
		C = 400pF	--	--	300	ns
t_F	Inputs Fall Time	C = 15 pF	--	--	300	ns
		C = 100 pF	--	--	300	ns
		C = 400 pF	--	--	300	ns
t_{SU_STO}	Stop Set-up Time		600	--	--	ns

Table 11. I²C Pins Timing Specifications, DILV Mode, T_A = -40°C to +125°C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Speed			Unit
			400 kHz			
			Min	Typ	Max	
t_{VD_DAT}	Data Out Hold Time		50	--	--	ns

[1] Does not meet standard I²C specifications: t_I = 95 ns for V_{DD} = 2.3 V, t_I = 95 ns for V_{DD} = 3.3 V, t_I = 111 ns for V_{DD} = 5.5 V; t_{HD_DAT} = 0 ns (min) for Rising Edge.
[2] Timing diagram can be found in the Figure 105.
[3] Please follow official I²C spec UM10204.
[4] When SCL Input is in Low-Level Logic mode max frequency is 400 kHz.

3.6 Macrocells Current Consumption

Table 12. Typical Current Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent	0.34	0.39	0.46	µA
		Vref0, SourceNone	7.61	7.67	7.88	µA
		Vref1, SourceNone	1.39	1.42	1.51	µA
		OSC2 25 MHz, pre-divider = 1, second divider = 1	50.46	62.63	90.60	µA
		OSC2 25 MHz, pre-divider = 4, second divider = 1	33.46	39.91	55.47	µA
		OSC2 25 MHz, pre-divider = 8, second divider = 1	30.35	35.75	49.03	µA
		OSC1 2.048 MHz, pre-divider = 1, second divider = 1	20.64	21.99	24.94	µA
		OSC1 2.048 MHz, pre-divider = 4, second divider = 1	18.56	19.21	20.61	µA
		OSC1 2.048 MHz, pre-divider = 8, second divider = 1	18.18	18.71	19.84	µA
		OSC0 2.048 kHz, pre-divider = 1, second divider = 1	0.62	0.66	0.77	µA
		OSC0 2.048 kHz, pre-divider = 4, second divider = 1	0.62	0.66	0.76	µA
		OSC0 2.048 kHz, pre-divider = 8, second divider = 1	0.61	0.66	0.76	µA
		Temperature Sensor, Output Range 1 (0.62 V to 0.99 V)	14.80	14.87	15.43	µA
		Temperature Sensor, Output Range 2 (0.75 V to 1.2 V)	14.94	15.02	15.43	µA
		All ACMPs (includes internal Vref, Vin+ = 0, Vref = 32 mV)	37.36	38.10	40.42	µA
		All ACMPxH (includes internal Vref, Vin+ = 0, Vref = 32 mV)	35.95	36.65	38.92	µA

Table 12. Typical Current Estimated for Each Macrocell at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	ACMP0H 100µA Enabled (includes internal Vref, Vin+ = 0, Vref = 32 mV)	48.95	50.26	53.90	µA
		Any ACMPxL (includes internal Vref, Vin+ = 0, Vref = 32 mV)	1.89	1.93	2.04	µA

3.7 Timing Specifications

Table 13. Typical Delay Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	23	26	17	19	12	15	ns
tpd	Delay	Digital Input to PP 2x	22	25	16	16	12	14	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	24	27	18	21	14	15	ns
tpd	Delay	Low Voltage Digital Input to PP 1x	38	241	26	164	18	104	ns
tpd	Delay	Digital input to NMOS 1x	--	24	--	18	--	13	ns
tpd	Delay	Digital input to NMOS 2x	--	23	--	17	--	13	ns
tpd	Delay	Digital input to NMOS 4x	--	23	--	17	--	13	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	23	--	16	--	12	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	22	--	16	--	12	ns
tpd	Delay	PP 1x 3 State Hi-Z to 1	22	--	16	--	12	--	ns
tpd	Delay	PP 1x 3 State Hi-Z to 0	--	22	--	16	--	12	ns
tpd	Delay	PP 2x 3 State Hi-Z to 1	21	--	16	--	12	--	ns
tpd	Delay	PP 2x 3 State Hi-Z to 0	--	21	--	15	--	11	ns
tpd	Delay	LATCH Q	16	18	11	13	8	9	ns
tpd	Delay	LATCH nQ	19	15	14	11	9	7	ns
tpd	Delay	LATCH nRESET High Q	25	21	17	15	12	10	ns
tpd	Delay	LATCH nRESET High nQ	22	24	16	17	11	12	ns
tpd	Delay	LATCH nRESET Low Q	22	23	15	16	11	12	ns
tpd	Delay	LATCH nRESET Low nQ	24	21	17	15	12	10	ns
tpd	Delay	LATCH nSET High Q	19	21	14	15	9	10	ns
tpd	Delay	LATCH nSET High nQ	22	19	16	13	11	9	ns
tpd	Delay	LATCH nSET Low Q	22	18	16	13	11	9	ns
tpd	Delay	LATCH nSET Low nQ	19	21	14	15	9	10	ns
tpd	Delay	Multi-Function LATCH Q	19	22	14	16	9	11	ns
tpd	Delay	Multi-Function LATCH nQ	22	19	16	13	11	9	ns
tpd	Delay	Multi-Function LATCH nRESET Q	23	27	16	19	11	14	ns
tpd	Delay	Multi-Function LATCH nRESET nQ	27	23	20	17	14	11	ns

Table 13. Typical Delay Estimated for Each Macrocell at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Multi-Function LATCH nSET Q	25	21	18	15	13	10	ns
tpd	Delay	Multi-Function LATCH nSET nQ	21	25	15	18	10	13	ns
tpd	Delay	LATCH3, LATCH12 First Q	17	19	12	14	8	9	ns
tpd	Delay	LATCH3, LATCH12 First nQ	20	17	14	12	10	8	ns
tpd	Delay	LATCH3, LATCH12 First nRESET High Q	26	23	18	16	13	11	ns
tpd	Delay	LATCH3, LATCH12 First nRESET High nQ	24	26	17	18	12	13	ns
tpd	Delay	LATCH3, LATCH12 First nRESET Low Q	23	25	16	18	11	12	ns
tpd	Delay	LATCH3, LATCH12 First nRESET Low nQ	26	23	18	16	13	11	ns
tpd	Delay	LATCH3, LATCH12 First nSET High Q	21	22	15	16	10	11	ns
tpd	Delay	LATCH3, LATCH12 First nSET High nQ	23	20	17	14	12	10	ns
tpd	Delay	LATCH3, LATCH12 First nSET Low Q	23	20	16	14	11	10	ns
tpd	Delay	LATCH3, LATCH12 First nSET Low nQ	21	23	15	16	10	11	ns
tpd	Delay	LATCH3, LATCH12 Second Q	19	19	13	13	9	9	ns
tpd	Delay	LATCH3, LATCH12 Second nQ	20	18	14	13	10	9	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET High Q	--	22	--	16	--	11	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET High nQ	23	--	17	--	12	--	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET Low Q	--	25	--	18	--	12	ns
tpd	Delay	LATCH3, LATCH12 Second nRESET Low nQ	26	--	18	--	13	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET High Q	20	--	14	--	10	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET High nQ	--	20	--	14	--	10	ns
tpd	Delay	LATCH3, LATCH12 Second nSET Low Q	23	--	16	--	11	--	ns
tpd	Delay	LATCH3, LATCH12 Second nSET Low nQ	--	22	--	16	--	11	ns
tpd	Delay	2-bit LUT	15	16	11	11	7	8	ns
tpd	Delay	3-bit LUT	16	17	11	12	8	8	ns
tpd	Delay	4-bit LUT	19	17	13	12	9	9	ns
tpd	Delay	Multi-Function 3-bit LUT	18	21	13	15	9	11	ns
tpd	Delay	Multi-Function 3-bit LUT, CNT Delay	46	47	33	34	23	24	ns
tpd	Delay	Multi-Function 4-bit LUT	21	23	15	17	10	12	ns
tpd	Delay	Multi-Function 4-bit LUT, CNT Delay	48	46	34	34	23	24	ns
tpd	Delay	Edge detect	19	20	13	14	9	9	ns

Table 13. Typical Delay Estimated for Each Macrocell at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tw	Width	Edge detect	211	212	156	157	115	115	ns
tpd	Delay	Edge detect Delayed	231	235	170	173	124	126	ns
tpd	Delay	Ripple CNT CLK DOWN Q0	18	16	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK DOWN Q1	29	22	20	16	14	11	ns
tpd	Delay	Ripple CNT CLK DOWN Q2	27	29	20	21	14	14	ns
tpd	Delay	Ripple CNT CLK UP Q0	18	16	13	11	9	8	ns
tpd	Delay	Ripple CNT CLK UP Q1	24	24	17	17	12	12	ns
tpd	Delay	Ripple CNT CLK UP Q2	29	23	21	17	15	12	ns
tpd	Delay	Ripple CNT nSET DOWN Q0	26	33	19	23	14	16	ns
tpd	Delay	Ripple CNT nSET DOWN Q1	26	41	19	29	13	21	ns
tpd	Delay	Ripple CNT nSET DOWN Q2	25	41	18	29	13	20	ns
tpd	Delay	Ripple CNT nSET UP Q0	26	33	19	23	14	16	ns
tpd	Delay	Ripple CNT nSET UP Q1	26	38	19	27	13	19	ns
tpd	Delay	Ripple CNT nSET UP Q2	25	44	18	32	13	22	ns
tpd	Delay	DFF Q	17	17	12	12	8	8	ns
tpd	Delay	DFF nQ	18	16	13	11	9	8	ns
tpd	Delay	DFF nRESET High Q	--	20	--	14	--	10	ns
tpd	Delay	DFF nRESET High nQ	21	--	15	--	10	--	ns
tpd	Delay	DFF nRESET Low Q	--	22	--	16	--	11	ns
tpd	Delay	DFF nRESET Low nQ	23	--	17	--	12	--	ns
tpd	Delay	DFF nSET High Q	21	--	15	--	10	--	ns
tpd	Delay	DFF nSET High nQ	--	20	--	14	--	10	ns
tpd	Delay	DFF nSET Low Q	23	--	16	--	12	--	ns
tpd	Delay	DFF nSET Low nQ	--	22	--	16	--	11	ns
tpd	Delay	Multi-Function DFF Q	19	19	13	13	9	9	ns
tpd	Delay	Multi-Function DFF nQ	20	19	14	13	9	9	ns
tpd	Delay	Multi-Function DFF nRESET Q	--	26	--	19	--	13	ns
tpd	Delay	Multi-Function DFF nRESET nQ	26	--	19	--	13	--	ns
tpd	Delay	Multi-Function DFF nSET Q	26	--	19	--	13	--	ns
tpd	Delay	Multi-Function DFF nSET nQ	--	26	--	19	--	14	ns
tpd	Delay	DFF3, DFF12 First Q	18	18	13	13	9	9	ns
tpd	Delay	DFF3, DFF12 First nQ	19	18	14	13	9	9	ns
tpd	Delay	DFF3, DFF12 First nRESET High Q	--	22	--	15	--	11	ns
tpd	Delay	DFF3, DFF12 First nRESET High nQ	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 First nRESET Low Q	--	24	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 First nRESET Low nQ	25	--	18	--	12	--	ns

Table 13. Typical Delay Estimated for Each Macrocell at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	DFF3, DFF12 First nSET High Q	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 First nSET High nQ	--	22	--	15	--	11	ns
tpd	Delay	DFF3, DFF12 First nSET Low Q	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 First nSET Low nQ	--	24	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 Second Q	20	21	14	15	10	10	ns
tpd	Delay	DFF3, DFF12 Second nQ	21	20	15	14	11	10	ns
tpd	Delay	DFF3, DFF12 Second nRESET High Q	--	21	--	15	--	10	ns
tpd	Delay	DFF3, DFF12 Second nRESET High nQ	22	--	16	--	11	--	ns
tpd	Delay	DFF3, DFF12 Second nRESET Low Q	--	23	--	17	--	12	ns
tpd	Delay	DFF3, DFF12 Second nRESET Low nQ	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 Second nSET High Q	22	--	15	--	11	--	ns
tpd	Delay	DFF3, DFF12 Second nSET High nQ	--	21	--	15	--	10	ns
tpd	Delay	DFF3, DFF12 Second nSET Low Q	24	--	17	--	12	--	ns
tpd	Delay	DFF3, DFF12 Second nSET Low nQ	--	23	--	17	--	12	ns
tpd	Delay	PGen CLK	16	16	12	11	8	8	ns
tpd	Delay	PGen nRESET Hi-Z to 0	--	21	--	15	--	11	ns
tpd	Delay	PGen nRESET Hi-Z to 1	20	--	14	--	10	--	ns
tpd	Delay	Pipe Delay Out	23	20	16	15	11	10	ns
tpd	Delay	Pipe Delay nRESET Out	30	28	22	21	16	15	ns
tpd	Delay	Filter Q	160	140	109	98	68	65	ns
tpd	Delay	Filter nQ	141	159	99	108	66	68	ns

Table 14. Typical Propagations Delays and Pulse Widths at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse Width, 1 cell	mode: (any)edge detect, edge detect output	221	163	119	ns
tw	Pulse Width, 2 cell	mode: (any)edge detect, edge detect output	438	322	234	ns
tw	Pulse Width, 3 cell	mode: (any)edge detect, edge detect output	652	480	349	ns
tw	Pulse Width, 4 cell	mode: (any)edge detect, edge detect output	869	639	464	ns
time1	Delay, 1 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 2 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 3 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time1	Delay, 4 cell	mode: (any)edge detect, edge detect output	18	13	9	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	240	176	128	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	455	334	243	ns

Table 14. Typical Propagations Delays and Pulse Widths at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time2	Delay, 3 cell	mode: both edge delay, edge detect output	672	493	358	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	888	673	473	ns

Table 15. Typical Propagations Delays and Pulse Widths at T_A = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width	< 127	< 86	< 54	ns
Inverter Filtered Pulse Width	< 109	< 77	< 52	ns

3.8 Counter/Delay Specifications

Table 16. Typical Counter/Delay Offset at T_A = 25 °C

Parameter	OSC freq	OSC Power-on	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-On time	25 MHz	auto	0.14	0.14	0.14	µs
Power-On time	2.048 MHz	auto	0.5	0.5	0.4	µs
Power-On time	2.048 kHz	auto	628	544	466	µs
frequency settling time	25 MHz	auto	4	4	8	µs
frequency settling time	2.048 MHz	auto	0.3	0.4	0.4	µs
frequency settling time	2.048 kHz	auto	660	570	480	µs
variable (CLK period)	25 MHz	forced	0-40	0-40	0-40	ns
variable (CLK period)	2.048 MHz	forced	0-0.5	0-0.5	0-0.5	µs
variable (CLK period)	2.048 kHz	forced	0-488	0-488	0-488	µs
tpd (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.9 Oscillator Specifications

Table 17. Oscillators Frequency Limits, V_{DD} = 2.3 V to 5.5 V

OSC	Junction Temperature Range					
	+25 °C			-40 °C to +125 °C		
	Minimum value, kHz	Maximum value, kHz	Error, %	Minimum value, kHz	Maximum value, kHz	Error, %
2.048 kHz OSC0	1.99728	2.07872	+1.500	1.6000	2.1187	+3.452
			-2.477			-21.875
2.048 MHz OSC1	2004.98	2078.72	+1.500	1936.88	2097.32	+2.408
			-2.101			-5.426
25 MHz OSC2	24457.6	25404.3	+1.617	23127.8	25602.0	+2.408
			-2.170			-7.489

3.9.1 OSC Power-On Delay

Table 18. Oscillators Power-On Delay at T_A = -40 °C to +125 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}) V	OSC0 2.048 kHz		OSC1 2.048 MHz		OSC2 25 MHz		OSC2 25 MHz Start with Delay	
	Typical value, µs	Maximum value, µs	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns
2.30	725	1165	528	567	45	64	145	167
2.50	684	1081	506	548	40	56	143	165
3.00	613	932	471	516	32	44	141	165
3.30	583	868	458	503	28	40	140	166
3.60	560	817	448	492	26	37	140	167
4.00	535	762	437	480	24	33	140	168
5.00	488	662	416	458	20	28	140	171
5.50	464	617	409	450	18	27	140	172

3.10 ACMP Specifications

Table 19. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP Input Offset	ACMPxH V_{HYS} = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV		-7.0	--	8.0	mV
		ACMPxL V_{HYS} = 0 mV, Gain = 1, Vref = 32 mV to 2016 mV		-5.0	--	7.0	mV

Table 19. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
t_{start}	ACMP Startup Time	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxH		--	--	37.3	µs
		ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL		--	--	294.1	µs
V_{HYS}	ACMP0H, ACMP1H Built-in Hysteresis [1]	V_{HYS} = 32 mV	T_A = 25 °C	23.0	--	37.0	mV
		V_{HYS} = 64 mV	T_A = 25 °C	55.0	--	69.0	mV
		V_{HYS} = 192 mV	T_A = 25 °C	183.0	--	198.0	mV
		V_{HYS} = 32 mV		22.0	--	38.0	mV
		V_{HYS} = 64 mV		53.0	--	69.0	mV
		V_{HYS} = 192 mV		181.0	--	198.0	mV
	ACMP2L, ACMP3L Built-in Hysteresis [1]	V_{HYS} = 32 mV	T_A = 25 °C	26.0	--	37.0	mV
		V_{HYS} = 64 mV	T_A = 25 °C	58.0	--	70.0	mV
		V_{HYS} = 192 mV	T_A = 25 °C	186.0	--	199.0	mV
		V_{HYS} = 32 mV		24.0	--	37.0	mV
		V_{HYS} = 64 mV		56.0	--	70.0	mV
		V_{HYS} = 192 mV		184.0	--	199.0	mV
R_{sin}	Series Input Resistance	Gain = 1x		--	10.00	--	GΩ
		Gain = 0.5x		--	2.00	--	MΩ
		Gain = 0.33x		--	2.00	--	MΩ
		Gain = 0.25x		--	2.00	--	MΩ
PROP	Propagation Delay, Response Time for ACMP0H, ACMP1H	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive =10 mV	Low to High	--	1.85	13.55	µs
			High to Low	--	2.48	10.04	µs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	0.53	2.03	µs
			High to Low	--	0.52	0.97	µs
		Gain = 1, T_A = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	1.46	--	µs
			High to Low	--	1.75	--	µs
		Gain = 1, T_A = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	0.55	--	µs
			High to Low	--	0.53	--	µs

Table 19. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
PROP	Propagation Delay, Response Time for ACMP2L, ACMP3L	Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 10 mV	Low to High	--	55.95	128.40	µs
			High to Low	--	63.01	152.94	µs
		Gain = 1, Vref = 32 mV to 2016 mV, Overdrive = 100 mV	Low to High	--	19.73	60.49	µs
			High to Low	--	19.33	60.93	µs
		Gain = 1, T_A = 25 °C, Vref = 32 mV, Overdrive = 10 mV	Low to High	--	68.15	--	µs
			High to Low	--	66.31	--	µs
		Gain = 1, T_A = 25 °C, Vref = 32 mV, Overdrive = 100 mV	Low to High	--	27.54	--	µs
			High to Low	--	27.01	--	µs
G	Gain error	G = 1	Vref = 32 mV	1.000	1.000	1.000	
		G = 0.5		0.484	0.502	0.527	
		G = 0.33		0.324	0.338	0.358	
		G = 0.25		0.238	0.250	0.263	
		G = 1	Vref = 480 mV	1.000	1.000	1.000	
		G = 0.5		0.497	0.501	0.504	
		G = 0.33		0.330	0.333	0.337	
		G = 0.25		0.248	0.250	0.253	
Vref0	Internal Vref0 error, Vref0 = 32 mV to 2016 mV, Buffer Disabled	V_{DD} = 4.0 V	T_A = +25 °C	-0.98	--	+4.95	%
	Internal Vref0 Output error, Vref0 = 320 mV to 2016 mV, Buffer Enabled	V_{DD} = 2.3 V to 5.5 V	T_A = +25 °C, I_{LOAD} = 1 µA	-8.09	--	+2.49	%
	Internal Vref0 Output error, Vref0 = 320 mV to 2016 mV, Buffer Enabled	V_{DD} = 2.3 V to 5.5 V	T_A = -40 °C to +125°C, I_{LOAD} = 1 µA	-8.58	--	+2.51	%

Table 19. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.3 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Note	Condition	Min	Typ	Max	Unit
Vref1	Internal Internal Vref1 error, Vref1 = 32 mV to 2016 mV, Buffer Disabled	V_{DD} = 4.0 V	T_A = +25 °C	-1.92	--	+5.30	%
	Internal Vref1 Output error, Vref1 = 320 mV to 2016 mV, Buffer Enabled	V_{DD} = 2.3 V to 5.5 V	T_A = +25 °C, I_{LOAD} = 1 µA	-6.17	--	+2.43	%
	Internal Vref1 Output error, Vref1 = 320 mV to 2016 mV, Buffer Enabled	V_{DD} = 2.3 V to 5.5 V	T_A = -40 °C to +125°C, I_{LOAD} = 1 µA	-6.94	--	+2.62	%
Is	Input Current Source	Vin = V_{DD} - 0.7 V	V_{DD} = 2.3 V	23.3	93.1	117.7	µA
			V_{DD} = 2.5 V	78.4	94.2	111.4	µA
			V_{DD} = 3.3 V	78.2	95.0	111.8	µA
			V_{DD} = 4.0 V	78.2	95.2	112.0	µA
			V_{DD} = 5.0 V	79.4	96.2	112.9	µA
			V_{DD} = 5.5 V	81.7	98.3	116.4	µA

[1] V_{IL} = Vin - V_{HYS}, V_{IH} = Vin.

3.11 Analog Temperature Sensor Specifications

Temperature Sensor typical nonlinearity ± 2.12 % for output range 1 and ± 2.56 % for output range 2 at V_{DD} = 2.3 V to 5.5 V.

Table 20. TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

Parameter	T_J, °C	Target V_{TS_OUT}, mV	V_{TS_OUT}, mV		Calculated T_J, °C		V_{TS_OUT} Accuracy, %		T_J Accuracy, °C	
			Min	Max	Min	Max	Min	Max	Min	Max
TS Output vs. Temperature (Output Range 1) Buffer Enabled	-40	997	985	1011	-45.9	-34.7	-1.20	1.32	-5.9	5.3
	-20	952	942	964	-25.4	-15.5	-1.09	1.28	-5.4	4.5
	0	906	897	917	-4.8	4.0	-1.02	1.22	-4.8	4.0
	20	860	852	870	15.6	23.3	-0.90	1.18	-4.4	3.3
	25	848	840	858	20.8	28.4	-0.94	1.15	-4.2	3.4
	40	813	804	824	35.4	44.1	-1.19	1.34	-4.6	4.1
	60	766	755	779	54.6	64.8	-1.49	1.67	-5.4	4.8
	80	718	705	732	74.1	85.4	-1.82	1.97	-5.9	5.4
	100	670	655	685	93.5	105.9	-2.14	2.36	-6.5	5.9
	110	645	630	662	103.3	116.1	-2.32	2.54	-6.7	6.1
	120	621	605	638	113.0	126.4	-2.53	2.77	-7.0	6.4
	130	596	580	613	123.0	136.3	-2.63	2.90	-7.0	6.3
TS Output vs. Temperature (Output Range 1) Buffer Disabled	-40	997	985	1011	-46.0	-34.6	-1.21	1.35	-6.0	5.4
	-20	952	942	964	-25.4	-15.4	-1.10	1.28	-5.4	4.6
	0	906	897	917	-4.8	4.0	-1.01	1.22	-4.8	4.0
	20	860	852	870	15.6	23.3	-0.90	1.18	-4.4	3.3
	25	848	840	858	20.9	28.5	-0.95	1.14	-4.1	3.5
	40	813	803	824	35.4	44.2	-1.21	1.33	-4.6	4.2
	60	766	754	779	54.6	64.9	-1.53	1.67	-5.4	4.9
	80	718	705	732	74.2	85.5	-1.84	1.96	-5.8	5.5
	100	670	655	685	93.6	106.0	-2.17	2.33	-6.4	6.0
	110	645	630	661	103.4	116.2	-2.36	2.51	-6.6	6.2
	120	621	605	638	113.0	126.4	-2.54	2.76	-7.0	6.4
	130	596	580	613	123.0	136.4	-2.66	2.88	-7.0	6.4

Table 20. TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V (Cont.)

Parameter	T_J, °C	Target V_{TS_OUT}, mV	V_{TS_OUT}, mV		Calculated T_J, °C		V_{TS_OUT} Accuracy, %		T_J Accuracy, °C	
			Min	Max	Min	Max	Min	Max	Min	Max
TS Output vs. Temperature (Output Range 2) Buffer Enabled	-40	1205	1180	1222	-46.2	-30.8	-2.09	1.39	-6.2	9.2
	-20	1150	1137	1164	-24.8	-15.0	-1.20	1.16	-4.8	5.0
	0	1095	1083	1108	-4.5	4.2	-1.07	1.16	-4.5	4.2
	20	1038	1029	1050	15.8	23.5	-0.94	1.16	-4.2	3.5
	25	1024	1015	1036	20.9	28.4	-0.95	1.14	-4.1	3.4
	40	981	970	995	35.2	43.9	-1.13	1.40	-4.8	3.9
	60	924	911	940	54.3	64.4	-1.37	1.77	-5.7	4.4
	80	865	851	884	73.7	84.8	-1.63	2.15	-6.3	4.8
	100	806	791	827	92.9	105.1	-1.88	2.61	-7.1	5.1
	110	777	761	799	102.5	115.2	-2.02	2.89	-7.5	5.2
	120	747	731	770	112.1	125.3	-2.15	3.16	-7.9	5.3
	130	717	701	741	122.0	135.2	-2.20	3.36	-8.0	5.2
TS Output vs. Temperature (Output Range 2) Buffer Disabled	-40	1205	1180	1223	-46.4	-30.9	-2.08	1.45	-6.4	9.1
	-20	1150	1137	1164	-24.9	-15.0	-1.21	1.17	-4.9	5.0
	0	1095	1083	1107	-4.5	4.2	-1.07	1.14	-4.5	4.2
	20	1038	1029	1050	15.8	23.5	-0.94	1.15	-4.2	3.5
	25	1024	1014	1036	20.9	28.5	-0.96	1.14	-4.1	3.5
	40	981	970	995	35.3	43.9	-1.15	1.39	-4.7	3.9
	60	924	911	940	54.4	64.4	-1.39	1.76	-5.6	4.4
	80	865	851	884	73.7	84.8	-1.64	2.14	-6.3	4.8
	100	806	791	827	92.9	105.1	-1.89	2.60	-7.1	5.1
	110	777	761	799	102.5	115.3	-2.04	2.86	-7.5	5.3
	120	747	731	770	112.2	125.4	-2.16	3.14	-7.8	5.4
	130	717	701	741	122.0	135.3	-2.22	3.35	-8.0	5.3

4. User Programmability

The SLG46857-A is a user programmable device with one time programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.gpx file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

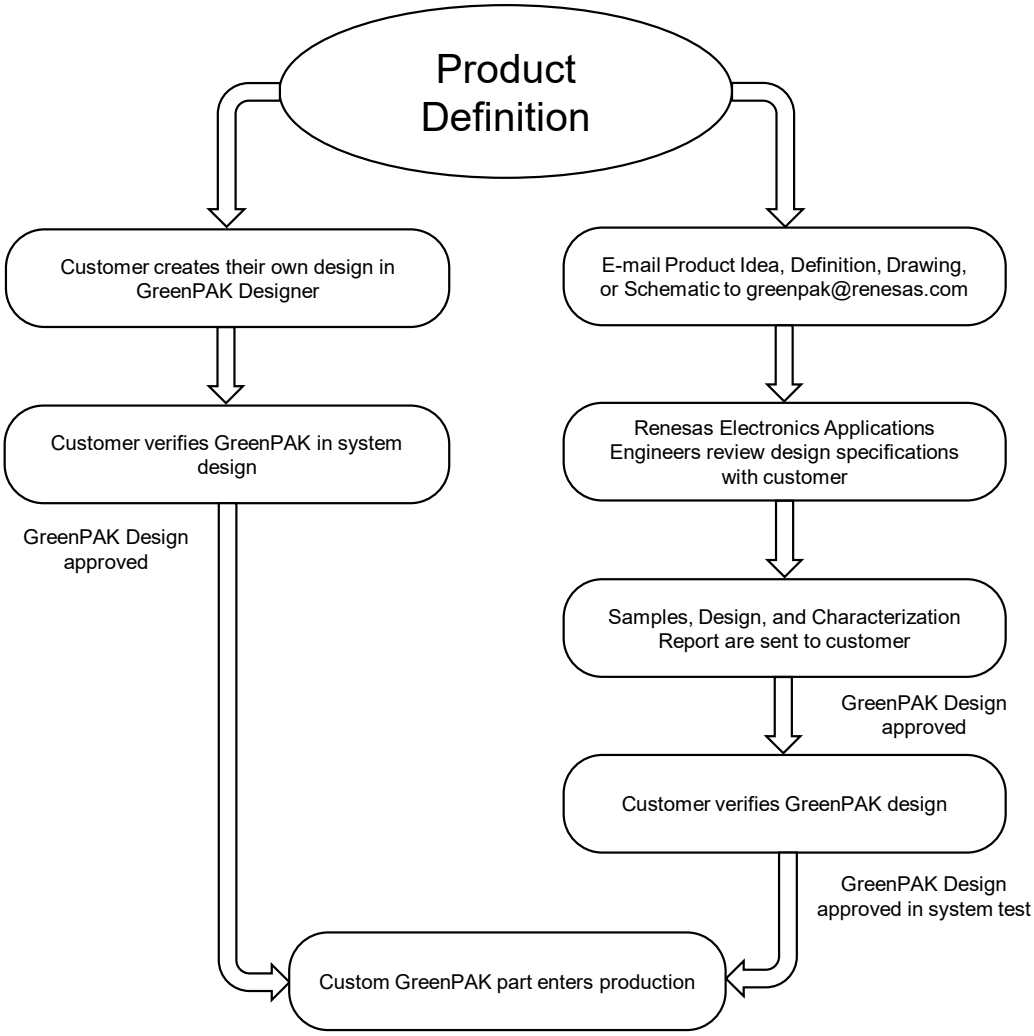

Figure 3. Steps to Create a Custom GreenPAK Device

5. Input/Output Pins

The SLG46857-A has a total of 10 GPIO, 1 GPI, and 1 GPO Pins, which can function as either a user-defined Input or Output, as well as serving as a special function (such as outputting the voltage reference).

5.1 GPIO Pins

GPIO0, GPIO1, GPIO2, GPIO3, GPIO4, GPIO5, GPIO6, GPIO7, GPIO8, and GPIO9 serve as General Purpose IO Pins.

5.2 GPI Pins

GPI0 serves as General Purpose Input Pin.

5.3 GPO Pins

GPO0 serves as General Purpose Output Pin.

5.4 Pull-Up/Down Resistors

All IO Pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either Pull-Up or Pull-Downs.

5.5 Fast Pull-Up/Down During Power-Up

During power-up, IO Pull-Up/Down resistance will switch to 2.6 kΩ initially and then it will switch to the normal setting value. This function is enabled by register [778].

5.6 GPI Structure

5.6.1 GPI Structure (for GPI0)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1, OE=0
01: Digital In with Schmitt Trigger, smt_en = 1, OE = 0
10: Low Voltage Digital In mode, lv_en = 1, OE = 0
11: Reserved

Note: OE cannot be selected by user and is controlled by register. Digital In is Matrix input.

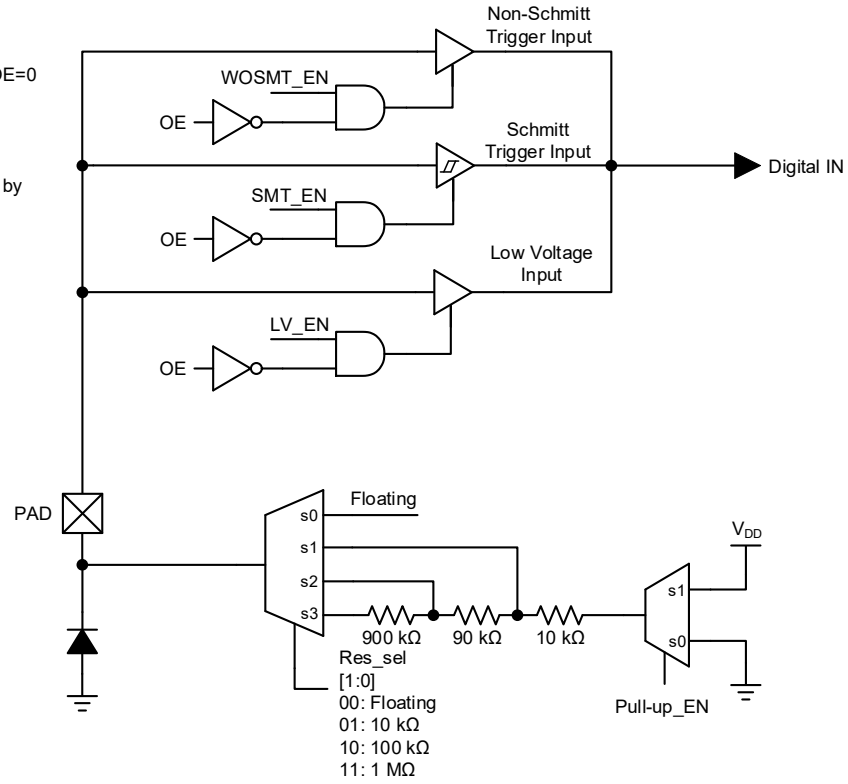

Figure 4. IO0 GPI Structure Diagram

5.7 GPIO with I²C Mode IO Structure

5.7.1 GPIO with I²C Mode Structure (for GPIO0 and GPIO1)

IO6, IO7 Mode [2:0]
00: Digital Input without Schmitt Trigger
01: Digital Input with Schmitt Trigger
10: Low Voltage Digital Input
11: Reserved

register [790]=1: Open-Drain NMOS for GPIO0
register [796]=1: Open-Drain NMOS for GPIO1

Note 1: OE cannot be selected by user and is controlled by register. Digital In is Matrix input.
Note 2: GPIO0 and GPIO1 do not support Push-Pull and PMOS Open-Drain modes.
Note 3: It is possible to apply an input voltage higher than V_{DD} to GPIO0 and GPIO1. However, this voltage should not exceed 5.5 V.
Note 4: Can be varied over PVT, for reference only

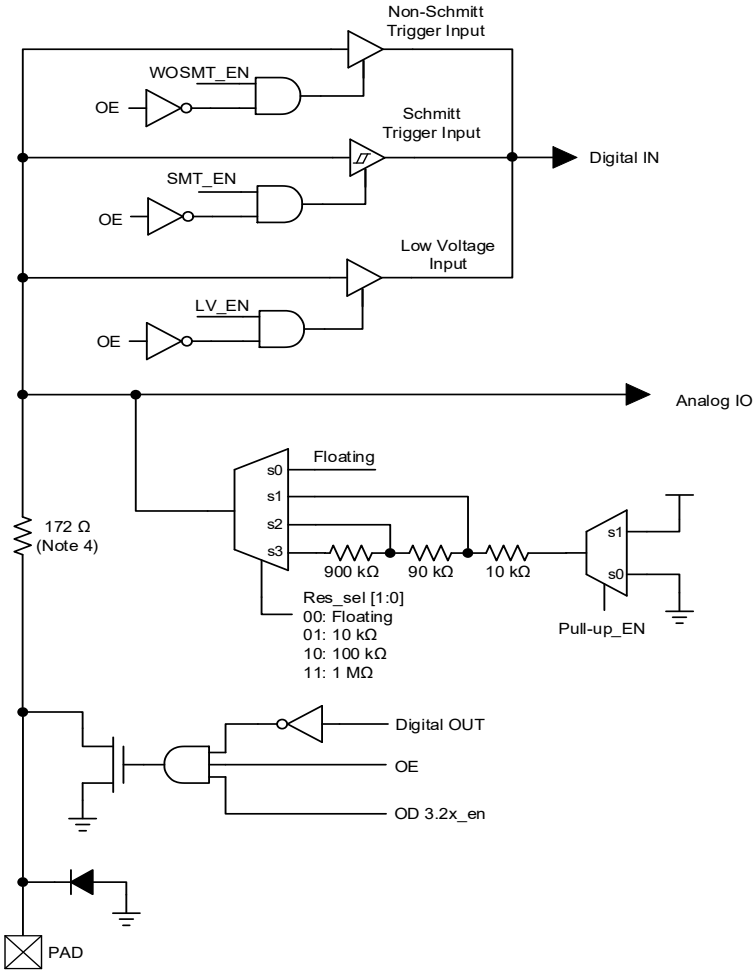

Figure 5. GPIO with I²C Mode IO Structure Diagram

5.8 Matrix OE IO Structure

5.8.1 Matrix OE IO Structure (for GPIO2, GPIO3, GPIO5, GPIO6, GPIO7, GPIO8, and GPIO9)

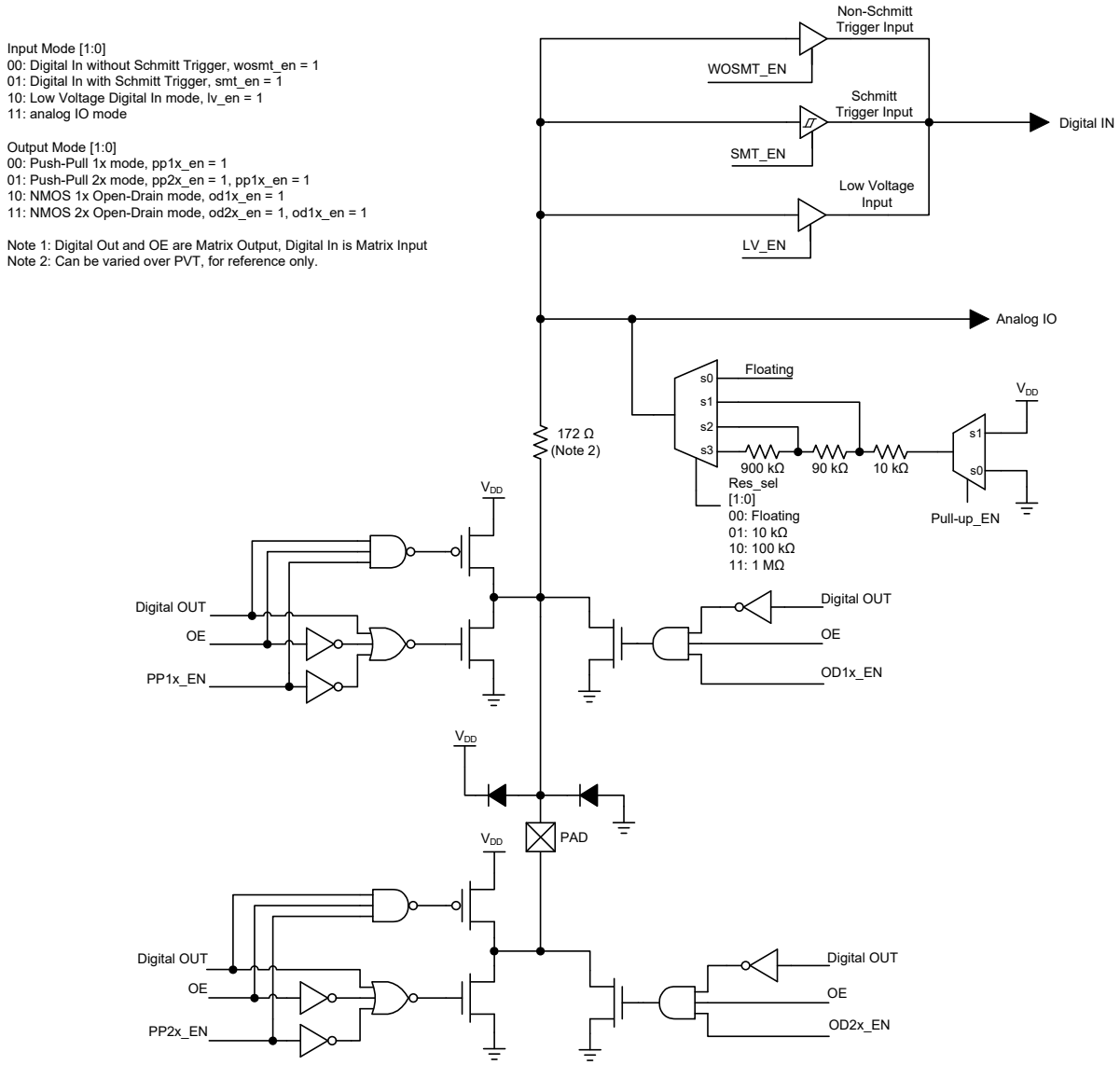

Figure 6. Matrix OE IO Structure Diagram

5.8.2 Matrix OE 4x Drive Structure (for GPIO4)

Input Mode [1:0]
00: Digital In without Schmitt Trigger, wosmt_en = 1
01: Digital In with Schmitt Trigger, smt_en = 1
10: Low Voltage Digital In mode, lv_en = 1
11: Analog IO mode

Output Mode [2:0]
Registers [828], [824:823]
000: Push-Pull 1x mode (pp1x_en)
001: Push-Pull 2x mode (pp2x_en)
010: NMOS 1x Open-Drain mode (od1x_en)
011: NMOS 2x Open-Drain mode (od2x_en)
100: Reserved
101: Push-Pull 4x mode (pp4x_en)
110: Reserved
111: NMOS 4x Open-Drain mode (od4x_en)

Note 1: Digital Out and OE are Matrix output, Digital In is Matrix input
Note 2: Can be varied over PVT, for reference only

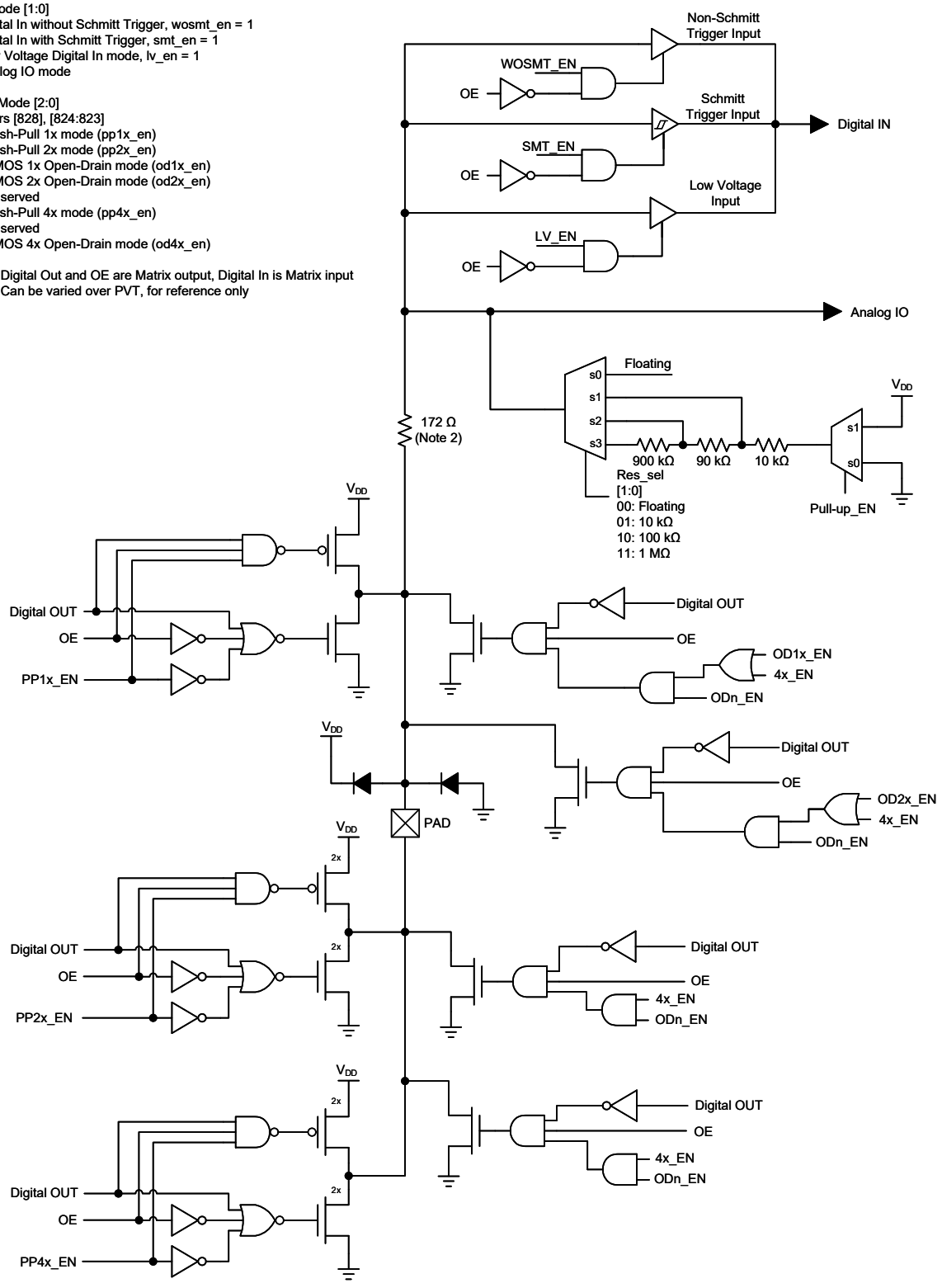

Figure 7. Matrix OE IO 4x Drive Structure Diagram

5.9 GPO Structure

5.9.1 GPO Register OE Structure (for GPO0)

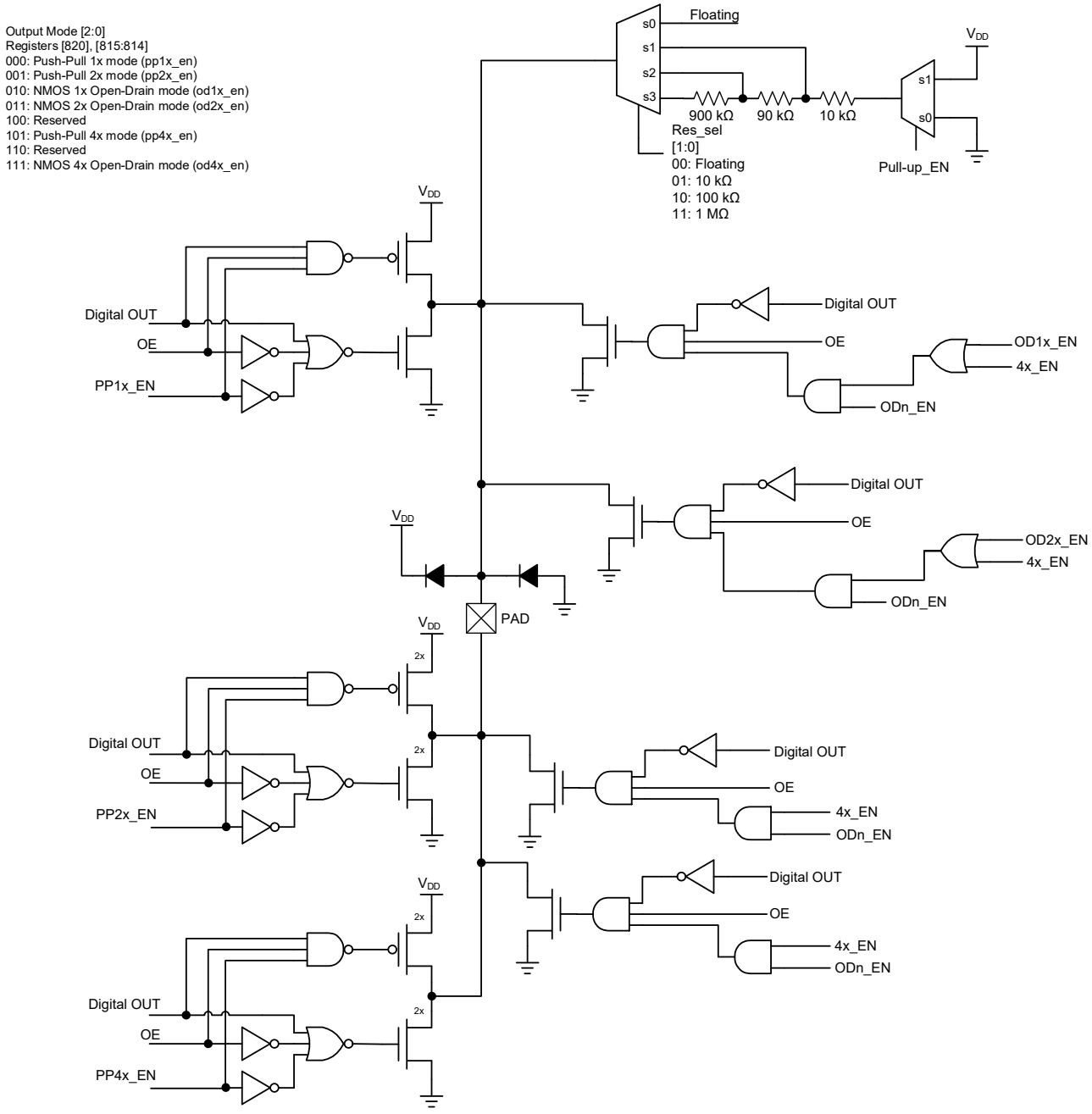

Figure 8. GPO Register OE 4x Drive Structure Diagram

5.10 IO Typical Performance

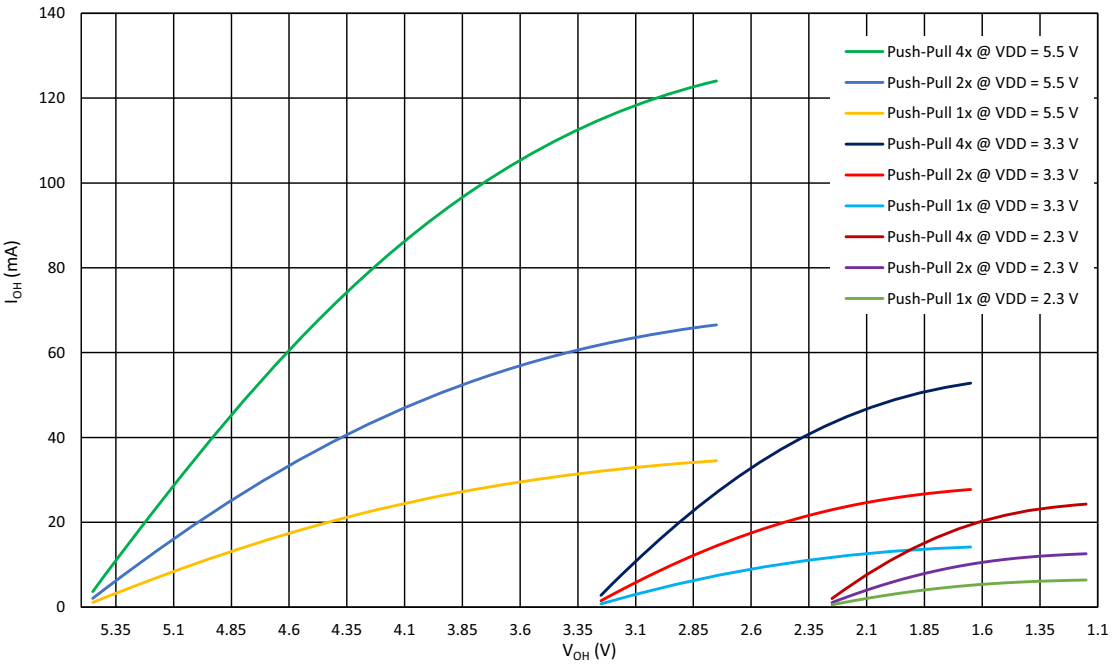

Figure 9. Typical High Level Output Current vs. High Level Output Voltage at T_A = 25 °C

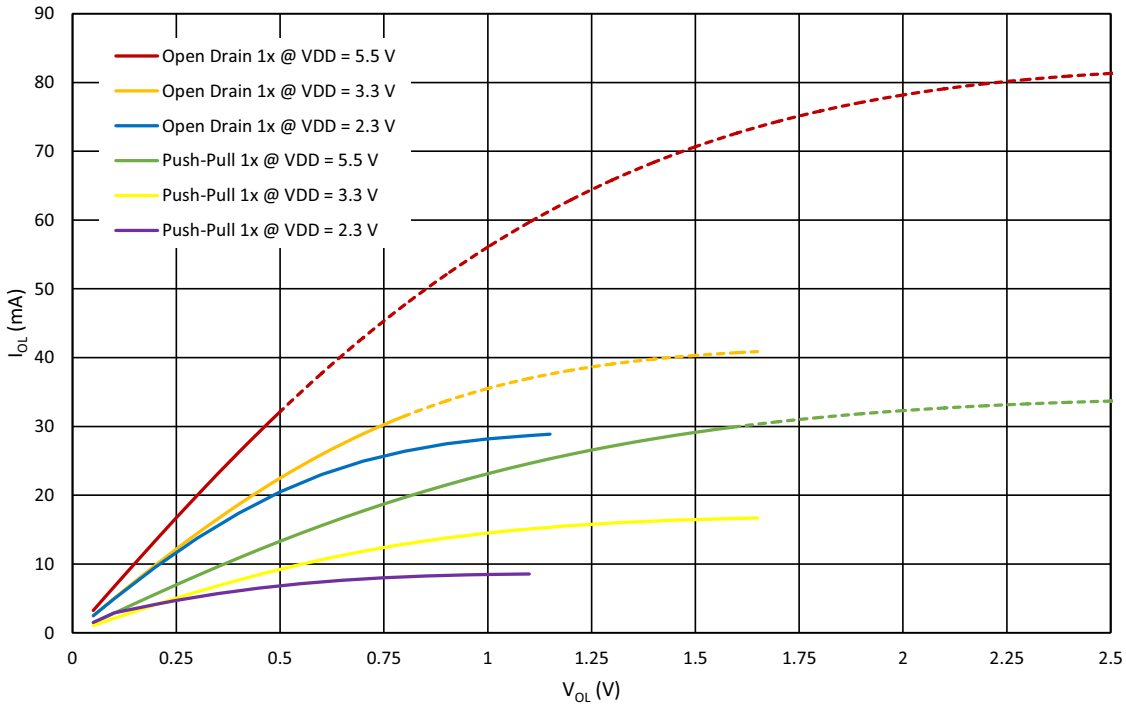

Figure 10. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C, Full Range

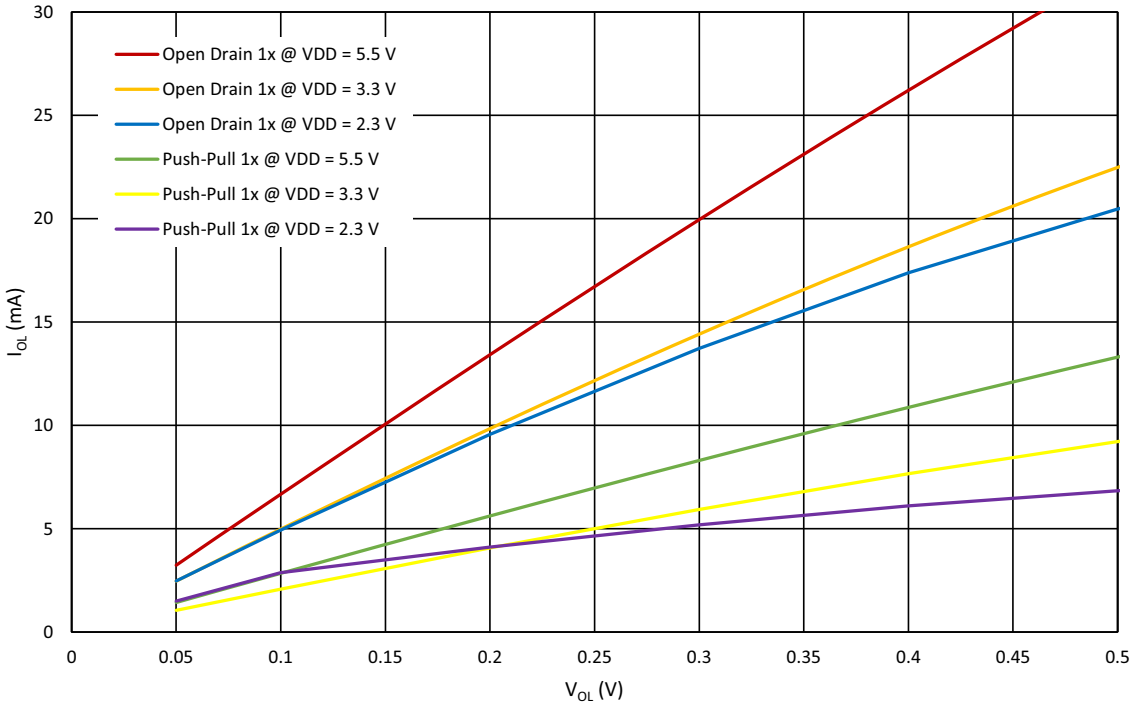

Figure 11. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C

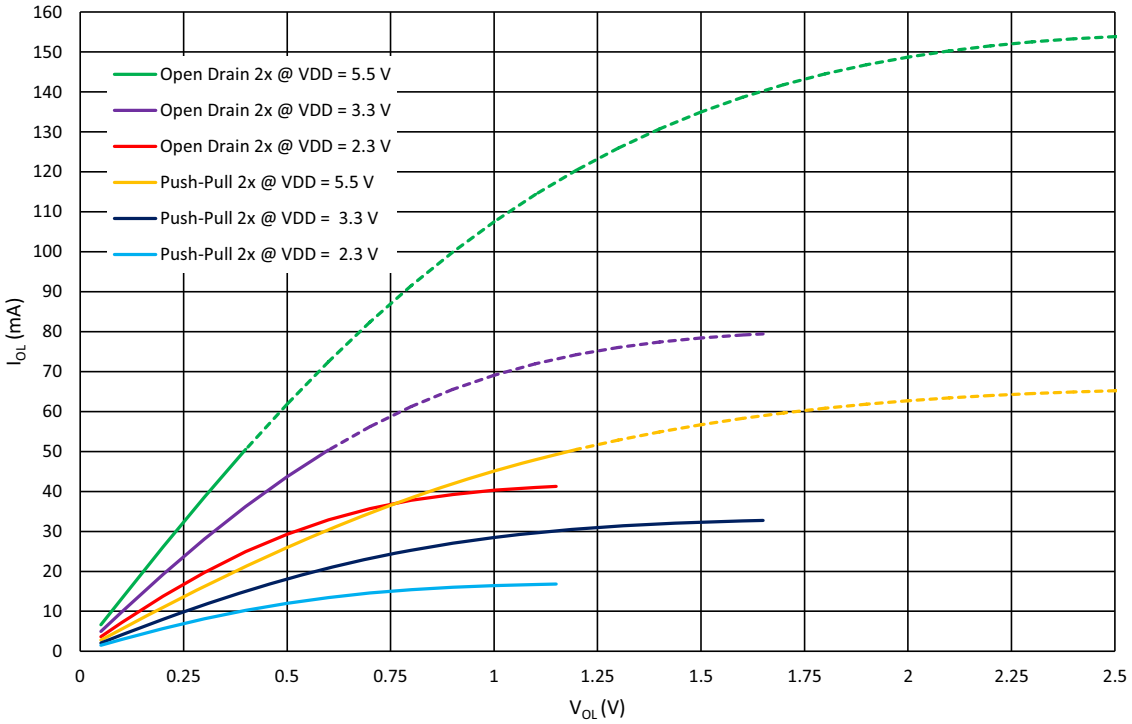

Figure 12. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C, Full Range

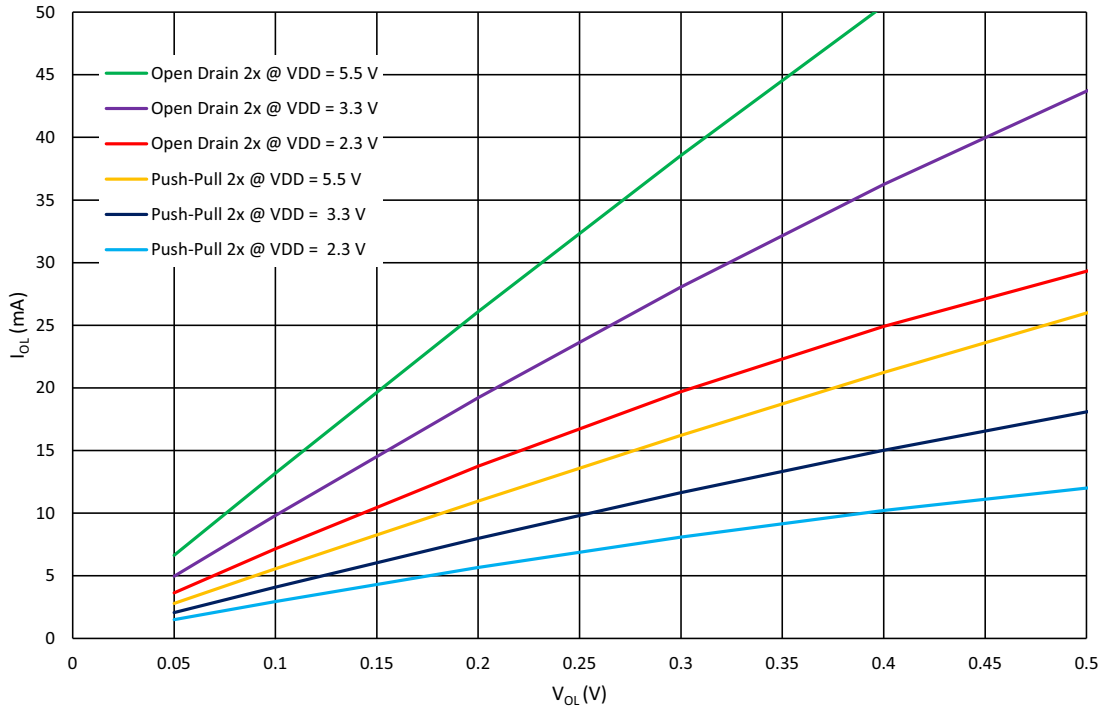

Figure 13. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C

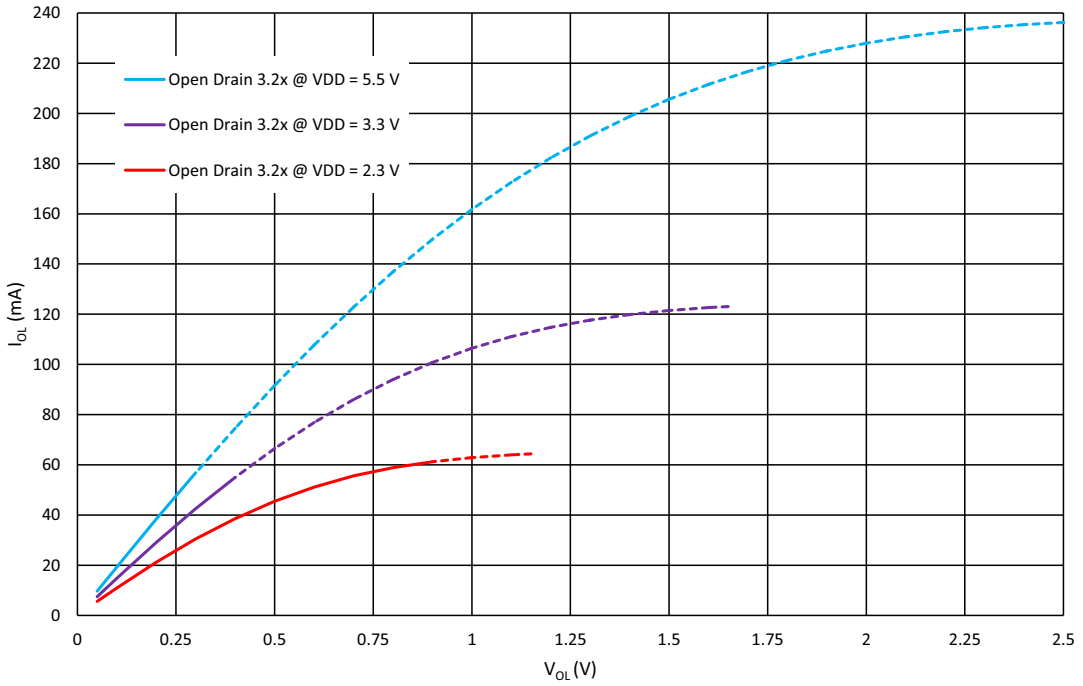

Figure 14. Typical Low Level Output Current vs. Low Level Output Voltage, 3.2x Drive at T_A = 25 °C, Full Range

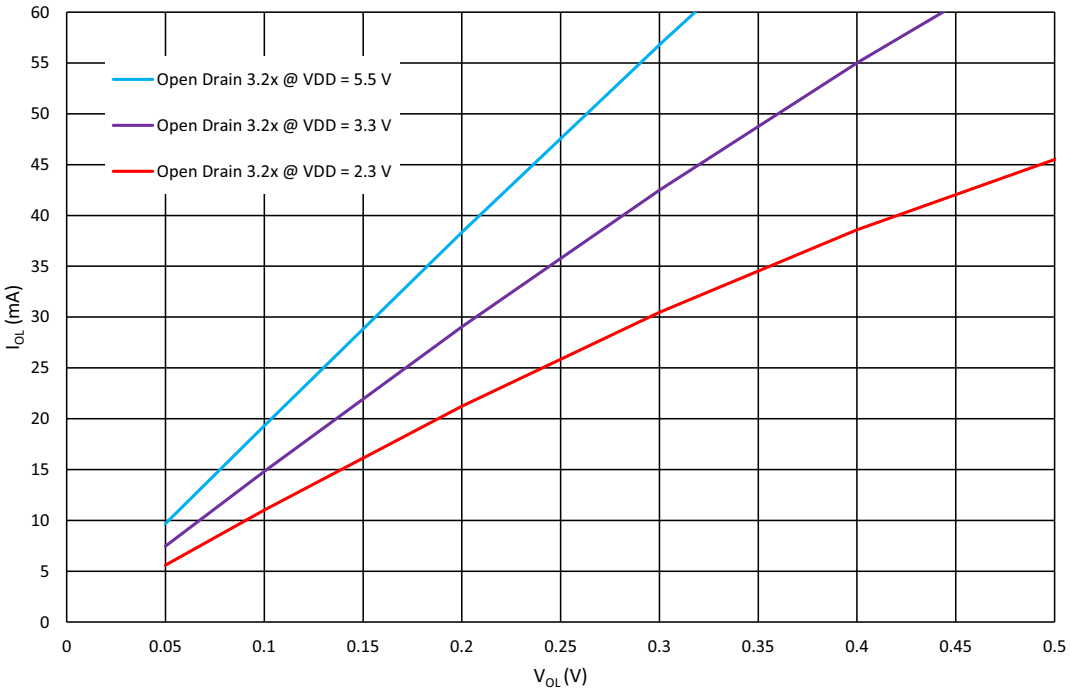

Figure 15. Typical Low Level Output Current vs. Low Level Output Voltage, 3.2x Drive at T_A = 25 °C

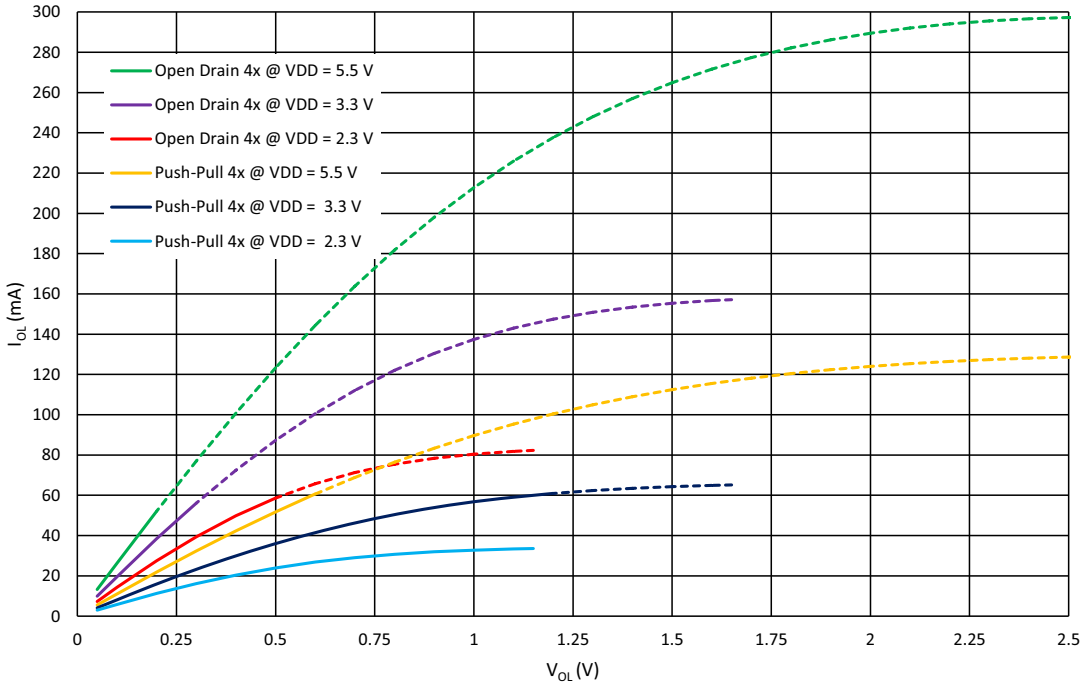

Figure 16. Typical Low Level Output Current vs. Low Level Output Voltage, 4x Drive at T_A = 25 °C, Full Range

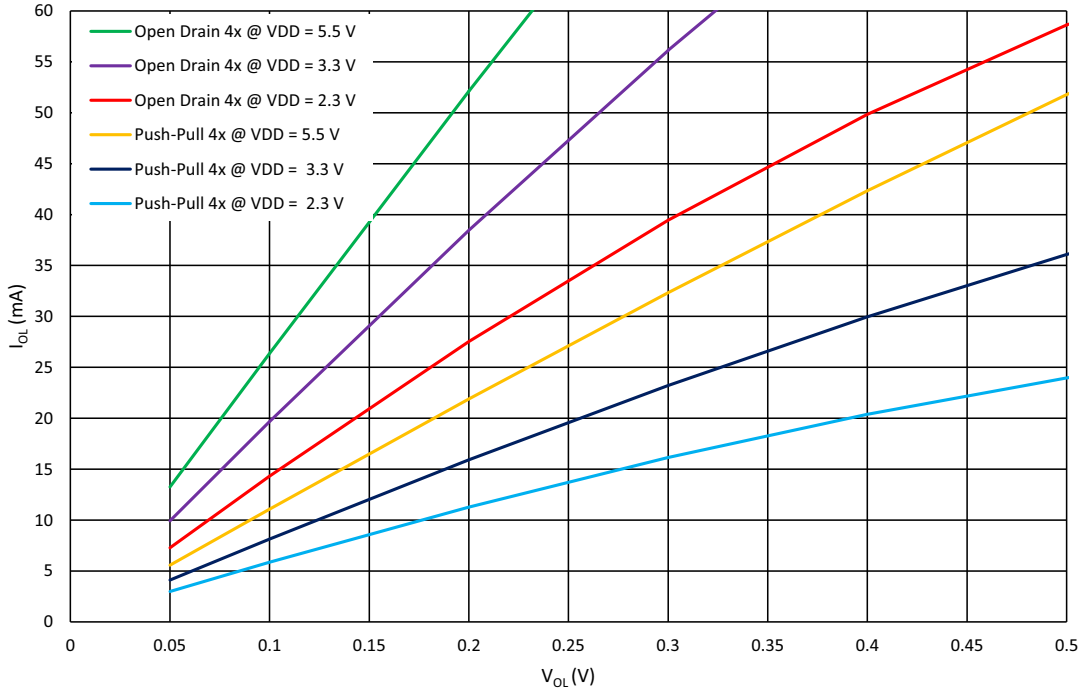

Figure 17. Typical Low Level Output Current vs. Low Level Output Voltage, 4x Drive at T_A = 25 °C

6. Connection Matrix

The Connection Matrix in the SLG46857-A is used to create the internal routing for internal functional macrocells of the device once it is programmed. The registers are programmed from the one-time programmable (OTP) NVM cell during Test Mode Operation. The output of each functional macrocell within the SLG46857-A has a specific digital bit code assigned to it, that is either set to active “HIGH”, or inactive “LOW”, based on the design that is created. Once the 2048 register bits within the SLG46857-A are programmed, a fully custom circuit will be created.

The Connection matrix has 64 inputs and 96 outputs. Each of the 64 inputs to the Connection matrix is hard-wired to the digital output of a particular source macrocell, including IO pins, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG46857-A’s register table, see Section 17. Register Definitions.

Matrix Input Signal	N
GND	0
GPIO1 Digital In	1
GPIO2 Digital In	2
GPIO3 Digital In	2
⋮	⋮
nRST_core	62
VDD	63

Matrix Input / Matrix Output	N	0	1	2	. . . .	95
	Register	[5:0]	[11:6]	[17:12]		[575:570]
	Function	IN0 of LUT2_0 or Clock Input of DFF0	IN1 of LUT2_0 or Data Input of DFF0	IN0 of LUT2_1 or Clock Input of PGen		Multi3_lut3_in2

Figure 18. Connection Matrix

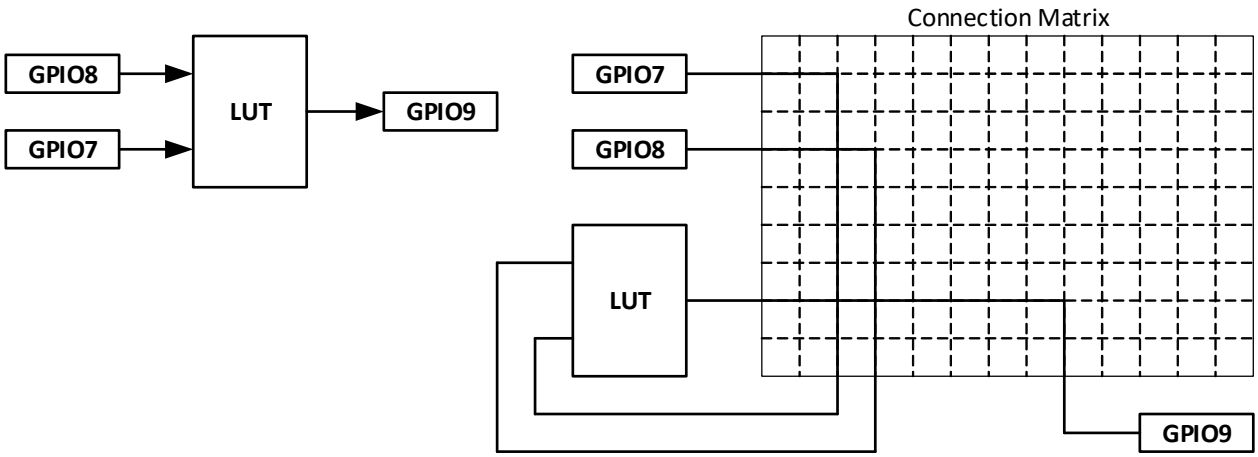

Figure 19. Connection Matrix Example

6.1 Matrix Input Table

Table 21. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output	0	0	0	0	1	0
3	LUT2_2/DFF2 output	0	0	0	0	1	1
4	LUT2_3/PGen output	0	0	0	1	0	0
5	LUT3_0/DFF3 output	0	0	0	1	0	1
6	LUT3_1/DFF4 output	0	0	0	1	1	0
7	LUT3_2/DFF5 output	0	0	0	1	1	1
8	LUT3_3/DFF6 output	0	0	1	0	0	0
9	LUT3_4/DFF7 output	0	0	1	0	0	1
10	LUT3_5/DFF8 output	0	0	1	0	1	0
11	LUT3_6/DFF9 output	0	0	1	0	1	1
12	LUT3_7/DFF10 output	0	0	1	1	0	0
13	LUT3_8/DFF11 output	0	0	1	1	0	1
14	CNT0 output	0	0	1	1	1	0
15	MF0_LUT4/DFF_OUT	0	0	1	1	1	1
16	CNT1 output	0	1	0	0	0	0
17	MF1_LUT3/DFF_OUT	0	1	0	0	0	1
18	CNT2 output	0	1	0	0	1	0
19	MF2_LUT3/DFF_OUT	0	1	0	0	1	1
20	CNT3 output	0	1	0	1	0	0
21	MF3_LUT3/DFF_OUT	0	1	0	1	0	1
22	CNT4 output	0	1	0	1	1	0
23	MF4_LUT3/DFF_OUT	0	1	0	1	1	1
24	CNT5 output	0	1	1	0	0	0
25	MF5_LUT3/DFF_OUT	0	1	1	0	0	1
26	CNT6 output	0	1	1	0	1	0
27	MF6_LUT3/DFF_OUT	0	1	1	0	1	1
28	CNT7 output	0	1	1	1	0	0
29	MF7_LUT3/DFF_OUT	0	1	1	1	0	1
30	LUT3_16/Ripple CNT/Pipe Delay_out0	0	1	1	1	1	0
31	Ripple CNT/Pipe Delay_out1	0	1	1	1	1	1
32	GPIO0 digital input or I^2C_virtual_0 Input	1	0	0	0	0	0
33	GPIO1 digital input or I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0

Table 21. Matrix Input Table (Cont.)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	Ripple CNT_out2	1	0	1	0	0	0
41	LUT4_0/DFF12 output	1	0	1	0	0	1
42	Programmable Delay Edge Detect Output	1	0	1	0	1	0
43	Edge Detect Filter Output	1	0	1	0	1	1
44	GPI0 Digital Input	1	0	1	1	0	0
45	GPIO2 Digital Input	1	0	1	1	0	1
46	GPIO3,Digital Input	1	0	1	1	1	0
47	GPIO4 Digital Input	1	0	1	1	1	1
48	GPIO5 Digital Input	1	1	0	0	0	0
49	GPIO6 Digital Input	1	1	0	0	0	1
50	GPIO7 Digital Input	1	1	0	0	1	0
51	GPIO8 Digital Input	1	1	0	0	1	1
52	GPIO9, Digital Input	1	1	0	1	0	0
53	Oscillator0 output 0	1	1	0	1	0	1
54	Oscillator1 output 0	1	1	0	1	1	0
55	Oscillator2 output	1	1	0	1	1	1
56	ACMP0 Output (normal speed)	1	1	1	0	0	0
57	ACMP1 Output (normal speed)	1	1	1	0	0	1
58	ACMP2 Output (low speed)	1	1	1	0	1	0
59	ACMP3 output (low speed)	1	1	1	0	1	1
60	Oscillator0 output 1	1	1	1	1	0	0
61	Oscillator1 output 1	1	1	1	1	0	1
62	POR OUT	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.2 Matrix Output Table

Table 22. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of LUT2_0 or Clock Input of DFF0	0
[11:6]	IN1 of LUT2_0 or Data Input of DFF0	1
[17:12]	IN0 of LUT2_1 or Clock Input of DFF1	2
[23:18]	IN1 of LUT2_1 or Data Input of DFF1	3
[29:24]	IN0 of LUT2_2 or Clock Input of DFF2	4
[35:30]	IN1 of LUT2_2 or Data Input of DFF2	5
[41:36]	IN0 of LUT2_3 or Clock Input of PGen	6
[47:42]	IN1 of LUT2_3 or nRST of PGen	7
[53:48]	IN0 of LUT3_0 or CLK Input of DFF3	8
[59:54]	IN1 of LUT3_0 or Data of DFF3	9
[65:60]	IN2 of LUT3_0 or nRST (nSET) of DFF3	10
[71:66]	IN0 of LUT3_1 or CLK Input of DFF4	11
[77:72]	IN1 of LUT3_1 or Data of DFF4	12
[83:78]	IN2 of LUT3_1 or nRST (nSET) of DFF4	13
[89:84]	IN0 of LUT3_2 or CLK Input of DFF5	14
[95:90]	IN1 of LUT3_2 or Data of DFF5	15
[101:96]	IN2 of LUT3_2 or nRST (nSET) of DFF5	16
[107:102]	IN0 of LUT3_3 or CLK Input of DFF6	17
[113:108]	IN1 of LUT3_3 or Data of DFF6	18
[119:114]	IN2 of LUT3_3 or nRST (nSET) of DFF6	19
[125:120]	IN0 of LUT3_4 or CLK Input of DFF7	20
[131:126]	IN1 of LUT3_4 or Data of DFF7	21
[137:132]	IN2 of LUT3_4 or Data of DFF7	22
[143:138]	IN0 of LUT3_5 or CLK Input of DFF8	23
[149:144]	IN1 of LUT3_5 or Data of DFF8	24
[155:150]	IN2 of LUT3_5 or nRST (nSET) of DFF8	25
[161:156]	IN0 of LUT3_6 or CLK Input of DFF9	26
[167:162]	IN1 of LUT3_6 or Data of DFF9	27
[173:168]	IN2 of LUT3_6 or nRST (nSET) of DFF9	28
[179:174]	IN0 of LUT3_7 or CLK Input of DFF10	29
[185:180]	IN1 of LUT3_7 or Data of DFF10	30
[191:186]	IN2 of LUT3_7 or nRST (nSET) of DFF10	31
[197:192]	IN0 of LUT3_8 or CLK Input of DFF11	32
[203:198]	IN1 of LUT3_8 or CLK Input of DFF11	33
[209:204]	IN2 of LUT3_8 or nRST (nSET) of DFF11	34

Table 22. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[215:210]	IN0 of LUT3_12 or CLK Input of DFF16 Delay4 Input (or Counter4 nRST Input)	35
[221:216]	IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay4 Input (or Counter4 nRST Input)	36
[227:222]	IN2 of LUT3_12 or Data of DFF16 Delay4 Input (or Counter4 nRST Input)	37
[233:228]	IN0 of LUT3_13 or CLK Input of DFF17 Delay5 Input (or Counter5 nRST Input)	38
[239:234]	IN1 of LUT3_13 or nRST (nSET) of DFF17 Delay5 Input (or Counter5 nRST Input)	39
[245:240]	IN2 of LUT3_13 or Data of DFF17 Delay5 Input (or Counter5 nRST Input)	40
[251:246]	IN0 of LUT3_14 or CLK Input of DFF18 Delay6 Input (or Counter6 nRST Input)	41
[257:252]	IN1 of LUT3_14 or nRST (nSET) of DFF18 Delay6 Input (or Counter6 nRST Input)	42
[263:258]	IN2 of LUT3_14 or Data of DFF18 Delay6 Input (or Counter6 nRST Input)	43
[269:264]	IN0 of LUT3_15 or CLK Input of DFF19 Delay7 Input (or Counter7 nRST Input)	44
[275:270]	IN1 of LUT3_15 or nRST (nSET) of DFF19 Delay7 Input (or Counter7 nRST Input)	45
[281:276]	IN2 of LUT3_15 or Data of DFF19 Delay7 Input (or Counter7 nRST Input)	46
[287:282]	IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT	47
[293:288]	IN1 of LUT3_16 or nRST of Pipe Delay or nSET of RIPP CNT	48
[299:294]	IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT	49
[305:300]	IN0 of LUT4_0 or CLK Input of DFF12	50
[311:306]	IN1 of LUT4_0 or Data of DFF12	51
[317:312]	IN2 of LUT4_0 or nRST (nSET) of DFF12	52
[323:318]	IN3 of LUT4_0	53
[329:324]	Programmable delay/edge detect input	54
[335:330]	Filter/Edge detect input	55
[341:336]	GPIO0 Digital Output	56
[347:342]	GPIO1 Digital Output	57
[353:348]	GPIO2 Digital Output	58
[359:354]	GPIO2 Digital Output OE	59
[365:360]	GPIO3, Digital Output	60
[371:366]	GPIO3, Digital Output OE	61

Table 22. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[377:372]	GPO0 Digital Output	62
[383:378]	GPIO4 Digital Output	63
[389:384]	GPIO4 Digital Output OE	64
[395:390]	GPIO5 Digital Output	65
[401:396]	GPIO5 Digital Output OE	66
[407:402]	GPIO6 Digital Output	67
[413:408]	GPIO6 Digital Output OE	68
[419:414]	GPIO7 Digital Output	69
[425:420]	GPIO7 Digital Output OE	70
[431:426]	GPIO8 Digital Output	71
[437:432]	GPIO8 Digital Output OE	72
[443:438]	GPIO9, Digital Output	73
[449:444]	GPIO9 Digital Output OE	74
[455:450]	PWR UP of ACMP0_H	75
[461:456]	PWR UP of ACMP1_H	76
[467:462]	PWR UP of ACMP2_L	77
[473:468]	PWR UP of ACMP3_L	78
[479:474]	Temp sensor, Vref Out_0, Vref Out_1 Power Up	79
[485:480]	Oscillator0 ENABLE	80
[491:486]	Oscillator1 ENABLE	81
[497:492]	Oscillator2 ENABLE	82
[503:498]	IN0 of LUT4_1 or CLK Input of DFF20 Delay0 Input (or Counter0 nRST Input)	83
[509:504]	IN1 of LUT4_1 or nRST of DFF20 Delay0 Input (or Counter0 nRST Input)	84
[515:510]	IN2 of LUT4_1 or nSET of DFF20 Delay0 Input (or Counter0 nRST Input)	85
[521:516]	IN3 of LUT4_1 or Data of DFF20 Delay0 Input (or Counter0 nRST Input)	86
[527:522]	IN0 of LUT3_9 or CLK Input of DFF13 Delay1 Input (or Counter1 nRST Input)	87
[533:528]	IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay1 Input (or Counter1 nRST Input)	88
[539:523]	IN2 of LUT3_9 or Data of DFF13 Delay1 Input (or Counter1 nRST Input)	89
[545:540]	IN0 of LUT3_10 or CLK Input of DFF14 Delay2 Input (or Counter2 nRST Input)	90
[551:546]	IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay2 Input (or Counter2 nRST Input)	91

Table 22. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[557:552]	IN2 of LUT3_10 or Data of DFF14 Delay2 Input (or Counter2 nRST Input)	92
[563:558]	IN0 of LUT3_11 or CLK Input of DFF15 Delay3 Input (or Counter3 nRST Input)	93
[569:564]	IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay3 Input (or Counter3 nRST Input)	94
[575:570]	IN2 of LUT3_11 or Data of DFF15 Delay3 Input (or Counter3 nRST Input)	95
[1] For each Address, the two most significant bits are unused.		

6.3 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at byte 0x4C (076).

Six of the eight Connection Matrix Virtual Inputs are dedicated to this virtual input function. An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

Two of the eight Connection Matrix Virtual Inputs are shared with Pin digital inputs (GPIO0 Digital or I^2C_virtual_0 Input), and (GPIO1 Digital or I^2C_virtual_1 Input). If the virtual input mode is selected, an I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened). The I^2C disable/enable register bit [2032] selects whether the Connection Matrix input comes from the Pin input or from the virtual register:

- Select SCL & Virtual Input 0 or GPIO0
- Select SDA & Virtual Input 1 or GPIO1

See Table 23 for Connection Matrix Virtual Inputs..

Table 23. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[608]
33	I^2C_virtual_1 Input	[609]
34	I^2C_virtual_2 Input	[610]
35	I^2C_virtual_3 Input	[611]

Table 23. Connection Matrix Virtual Inputs (Cont.)

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
36	I2C_virtual_4 Input	[612]
37	I2C_virtual_5 Input	[613]
38	I2C_virtual_6 Input	[614]
39	I2C_virtual_7 Input	[615]

6.4 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I2C addresses for reading these register values are bytes 0x48 (072) to 0x4F (079). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x4C (076)).

7. Combination Function Macrocells

The SLG46857-A has 15 combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells.

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input

Inputs/Outputs for the 15 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-Bit LUT or D Flip-Flop Macrocells

There are three macrocells that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

LATCH: when CLK is LOW, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is HIGH).

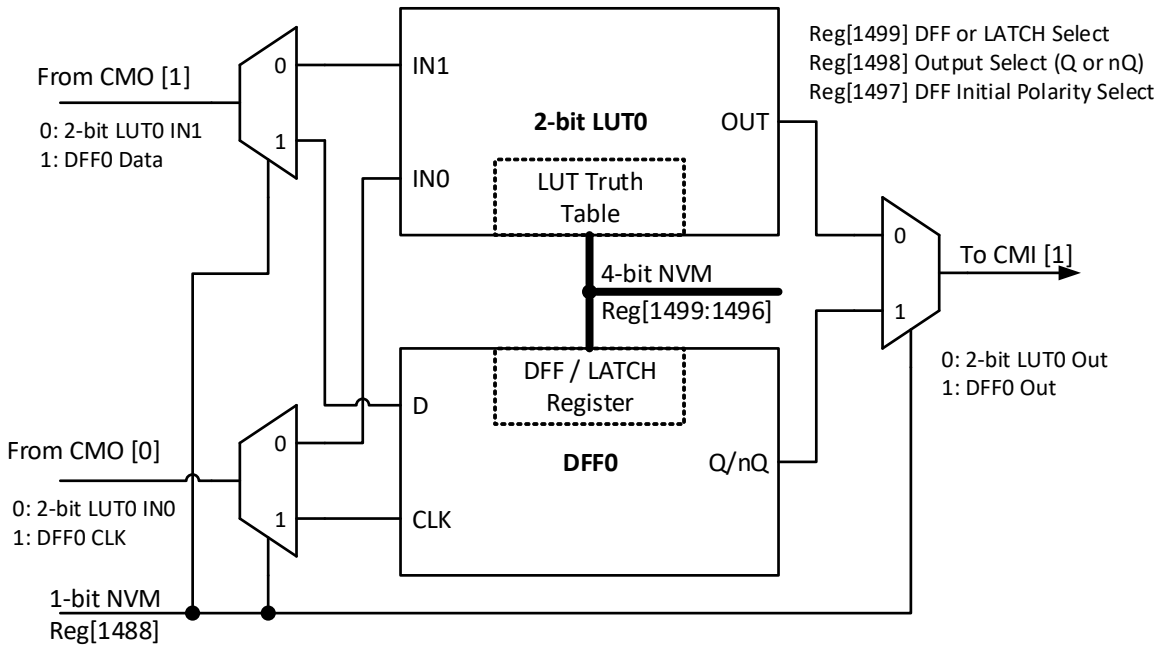

Figure 20. 2-bit LUT0 or DFF0

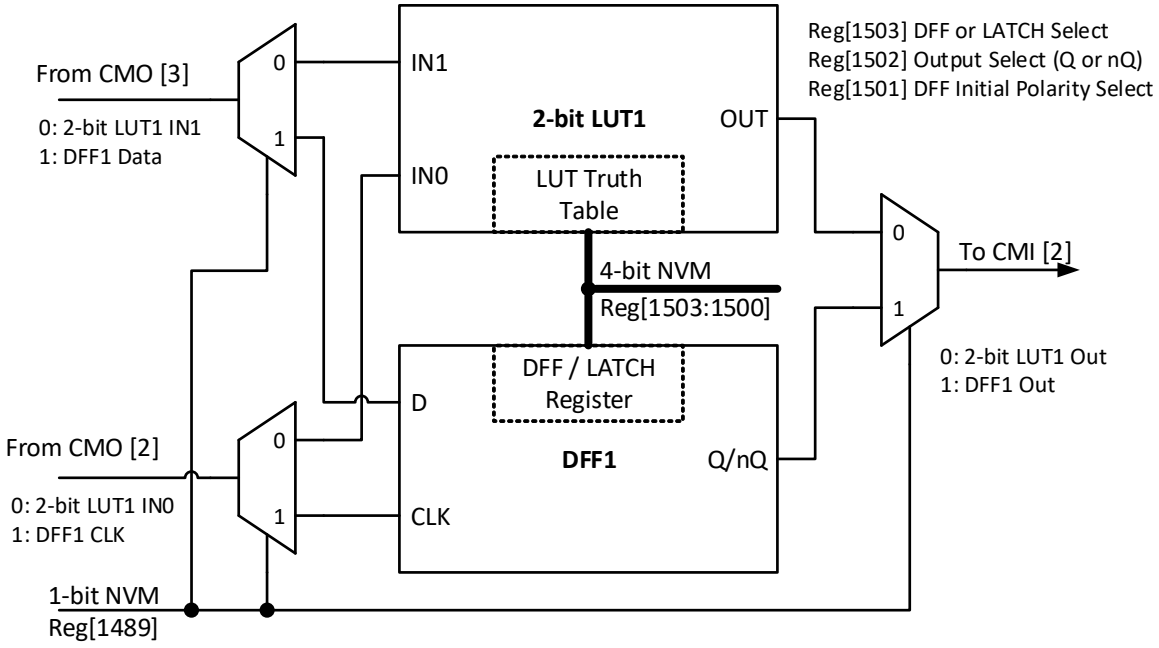

Figure 21. 2-bit LUT1 or DFF1

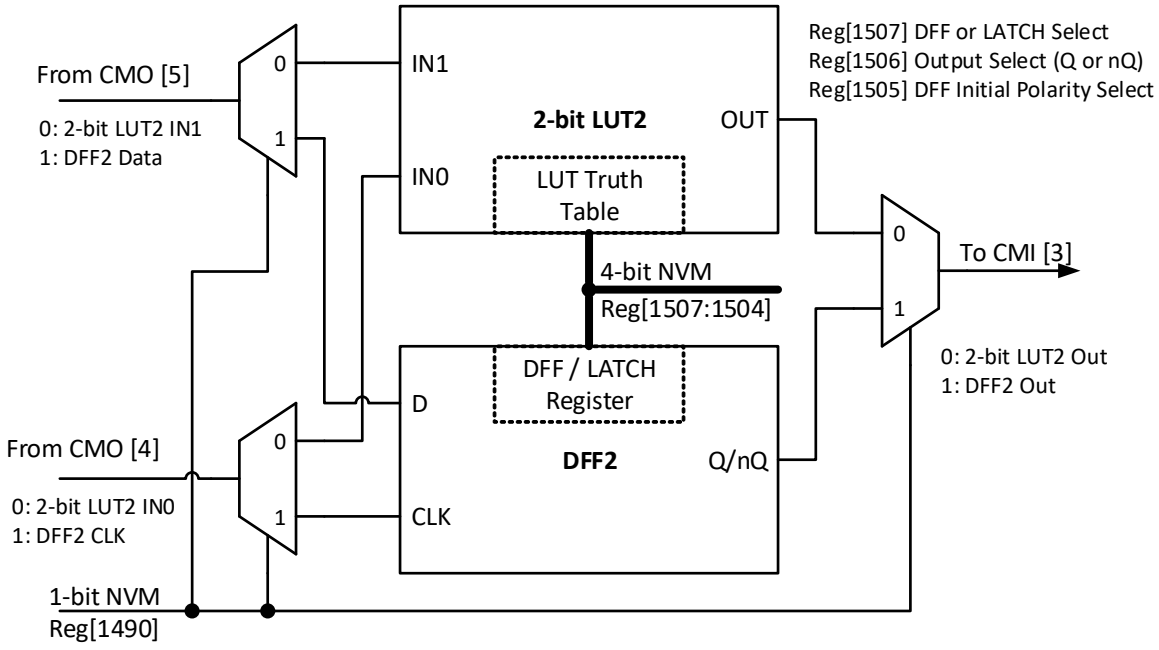

Figure 22. 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 24. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1496]	LSB
0	1	register [1497]	
1	0	register [1498]	
1	1	register [1499]	MSB

Table 25. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1500]	LSB
0	1	register [1501]	
1	0	register [1502]	
1	1	register [1503]	MSB

Table 26. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1504]	LSB
0	1	register [1505]	
1	0	register [1506]	
1	1	register [1507]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT0 is defined by registers [1499:1496]

2-bit LUT1 is defined by registers [1503:1500]

2-bit LUT2 is defined by registers [1507:1504]

Table 27 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 27. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

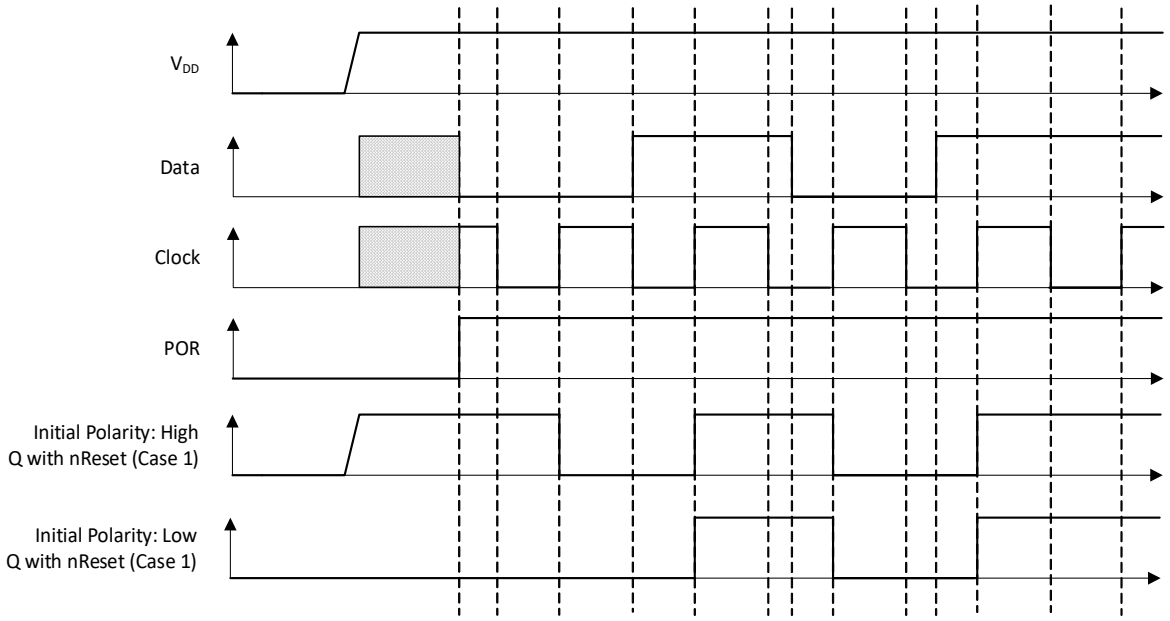

Figure 23. DFF Polarity Operations

7.2 2-bit LUT or Programmable Pattern Generator

The SLG46857-A has one combination function macrocell that can serve as a logic or timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by register [1409]. When operating as a Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

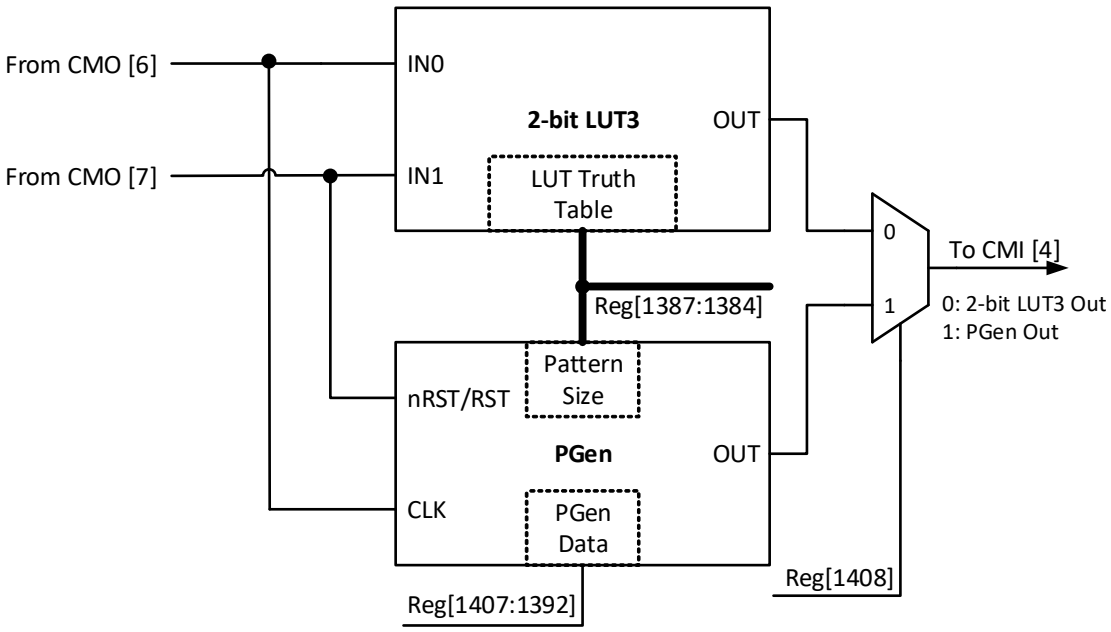

Figure 24. 2-bit LUT3 or PGen

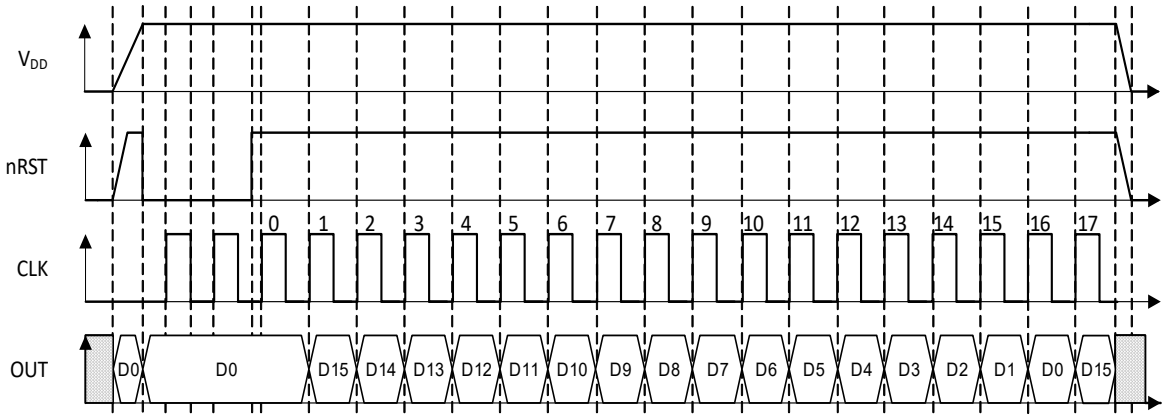

Figure 25. PGen Timing Diagram

7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 28. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1384]	LSB
0	1	register [1385]	
1	0	register [1386]	
1	1	register [1387]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT3 is defined by registers [1387:1384]

Table 29 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 29. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are nine macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1442].

DFF3 operation will flow the functional description below:

- If register [1444] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1444] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

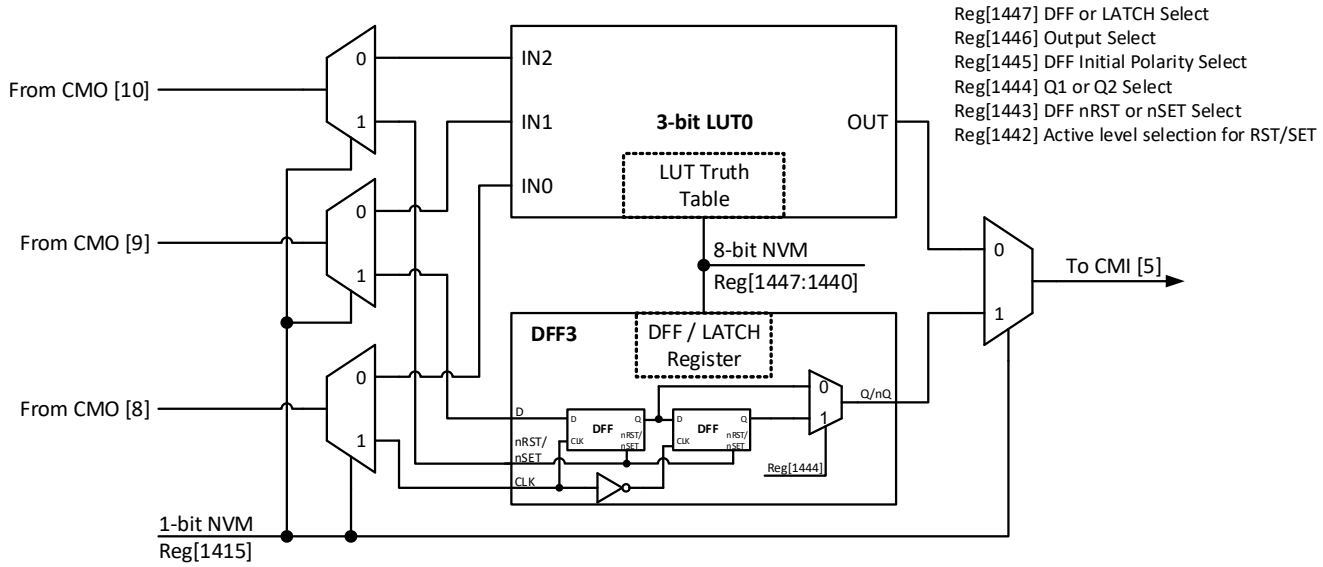

Figure 26. 3-bit LUT0 or DFF3

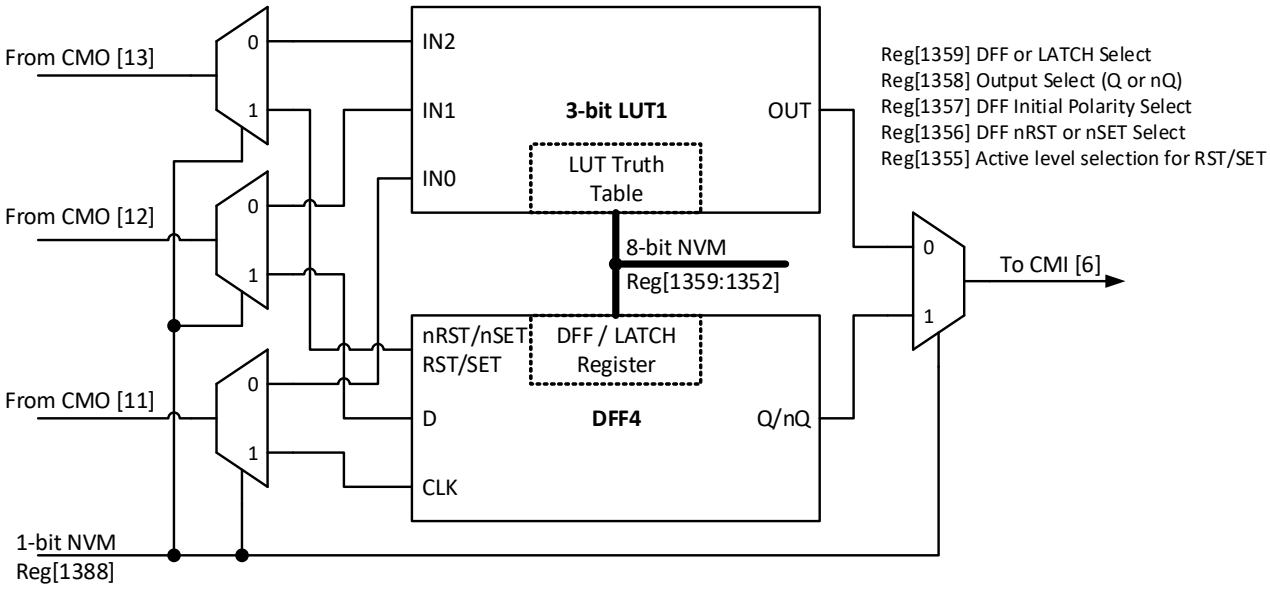

Figure 27. 3-bit LUT1 or DFF4

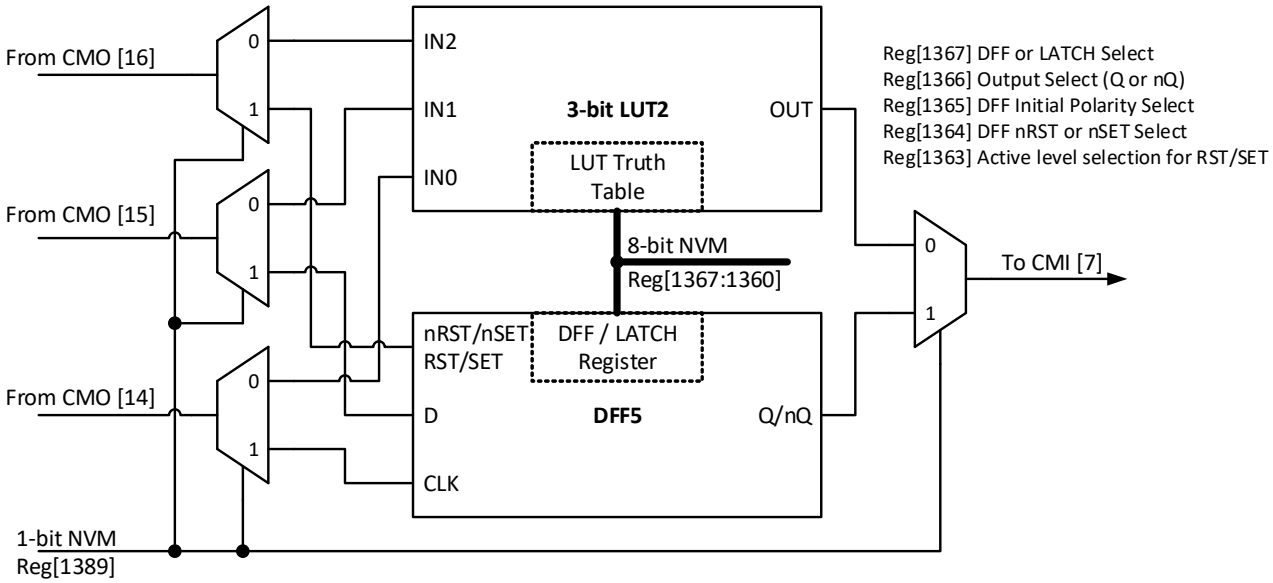

Figure 28. 3-bit LUT2 or DFF5

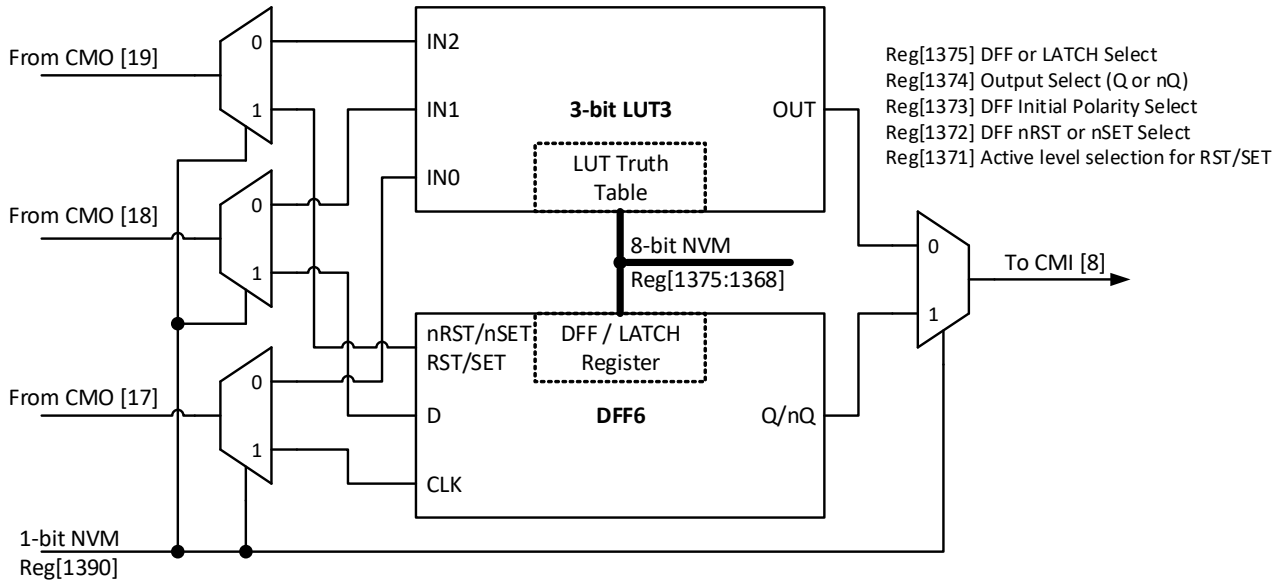

Figure 29. 3-bit LUT3 or DFF6

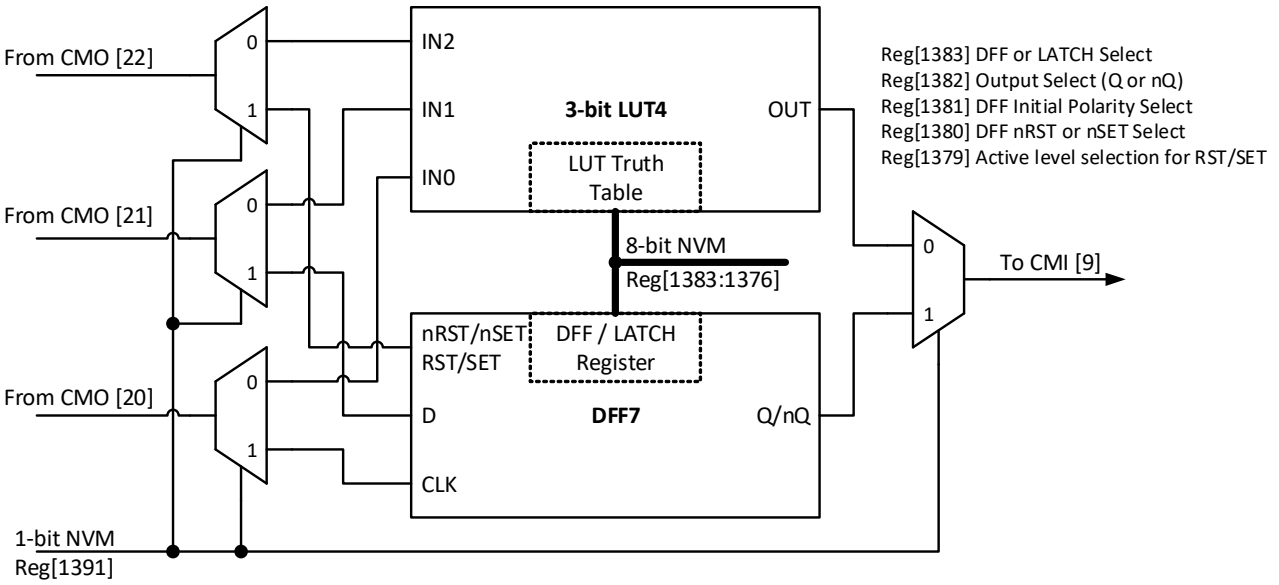

Figure 30. 3-bit LUT4 or DFF7

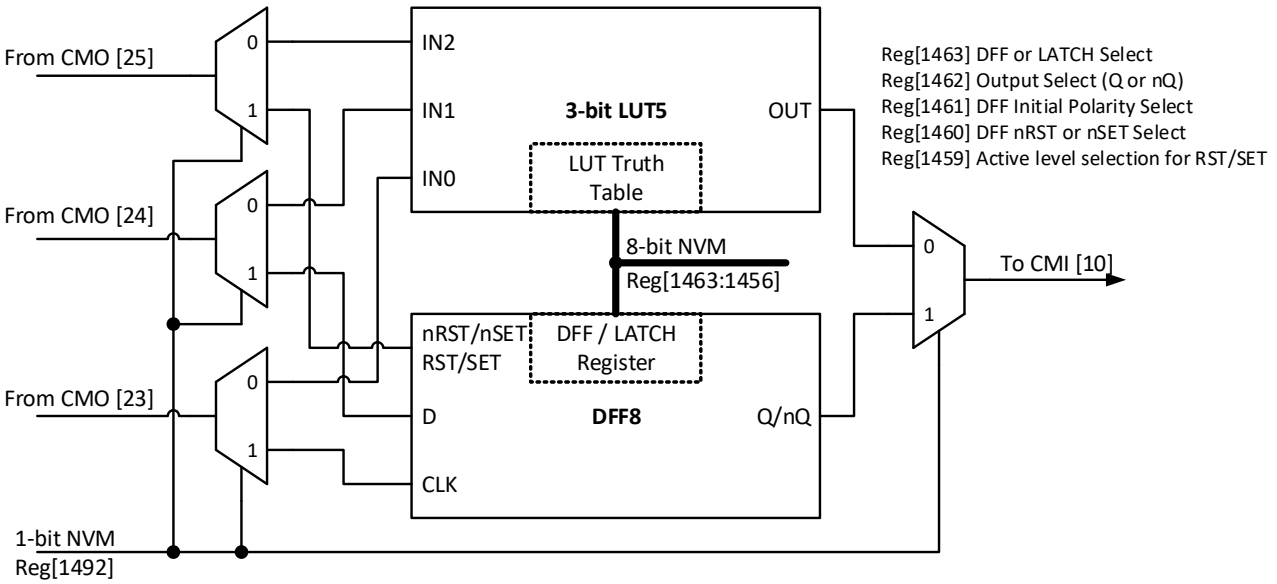

Figure 31. 3-bit LUT5 or DFF8

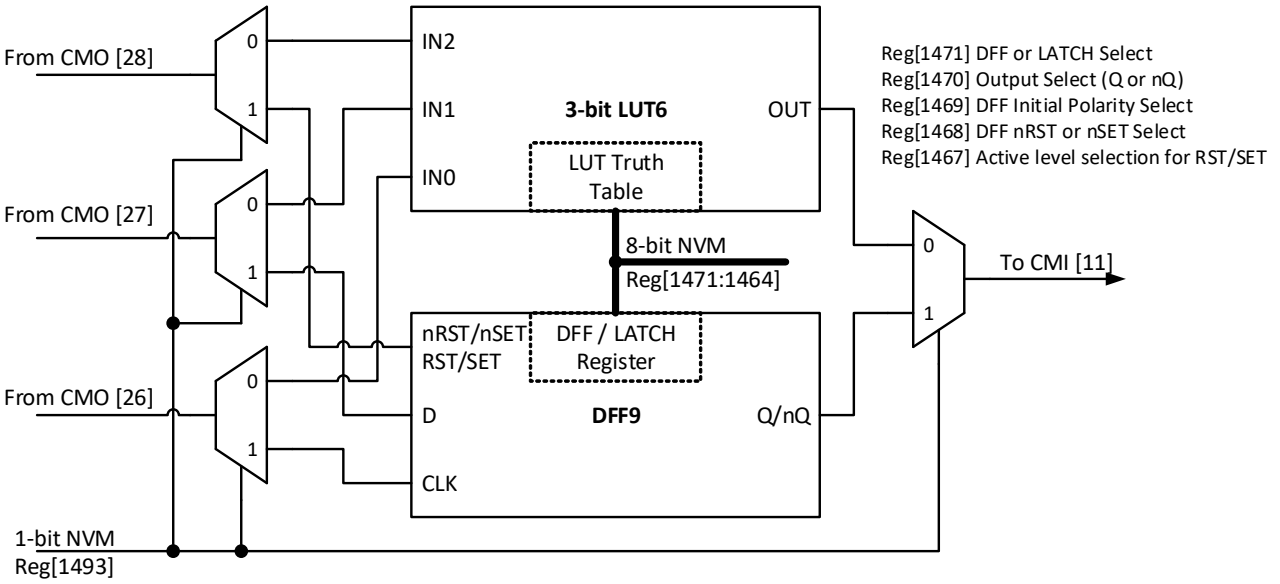

Figure 32. 3-bit LUT6 or DFF9

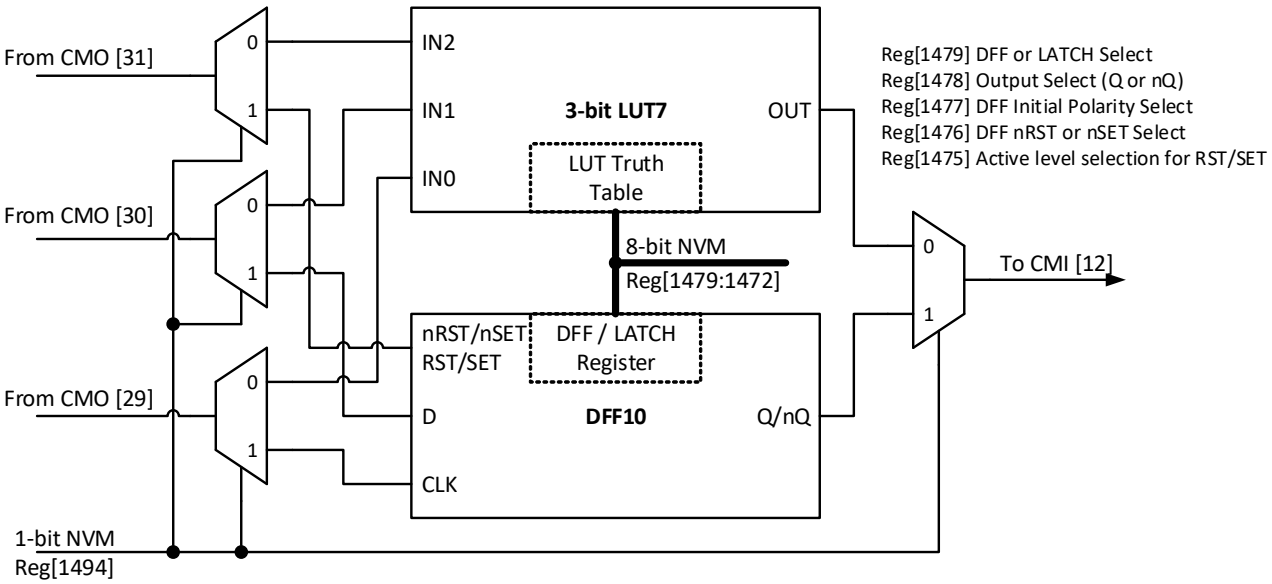

Figure 33. 3-bit LUT7 or DFF10

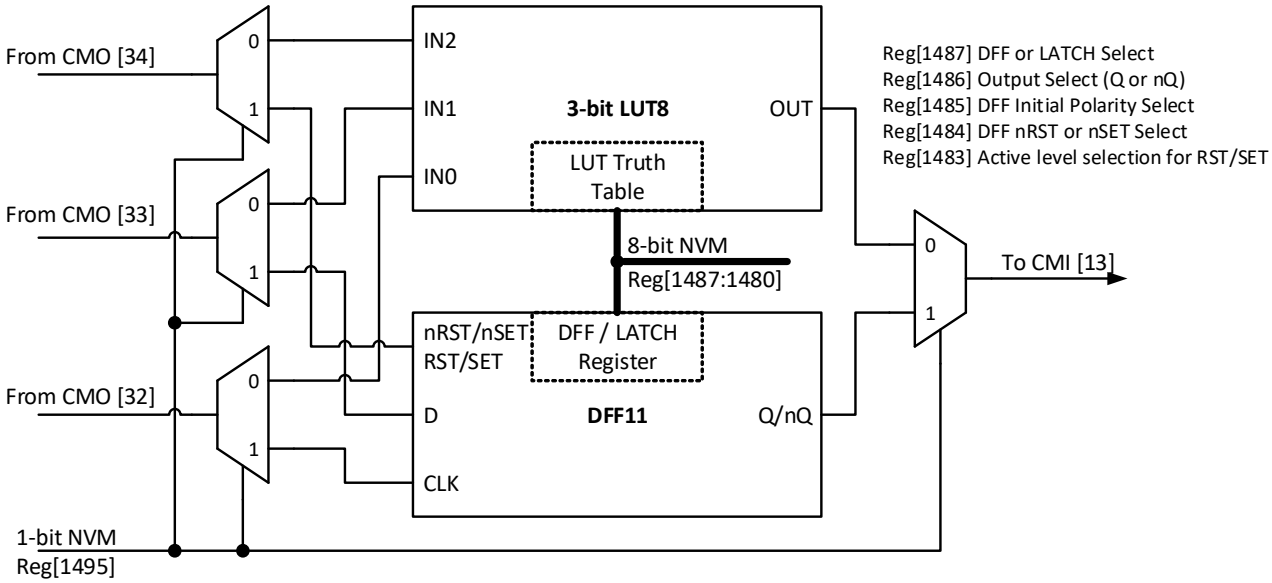

Figure 34. 3-bit LUT8 or DFF11

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 30. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1440]	LSB
0	0	1	register [1441]	
0	1	0	register [1442]	
0	1	1	register [1443]	
1	0	0	register [1444]	
1	0	1	register [1445]	
1	1	0	register [1446]	
1	1	1	register [1447]	MSB

Table 31. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1352]	LSB
0	0	1	register [1353]	
0	1	0	register [1354]	
0	1	1	register [1355]	
1	0	0	register [1356]	
1	0	1	register [1357]	
1	1	0	register [1358]	
1	1	1	register [1359]	MSB

Table 32. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1360]	LSB
0	0	1	register [1361]	
0	1	0	register [1362]	
0	1	1	register [1363]	
1	0	0	register [1364]	
1	0	1	register [1365]	
1	1	0	register [1366]	
1	1	1	register [1367]	MSB

Table 33. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1368]	LSB
0	0	1	register [1369]	
0	1	0	register [1370]	
0	1	1	register [1371]	
1	0	0	register [1372]	
1	0	1	register [1373]	
1	1	0	register [1374]	
1	1	1	register [1375]	MSB

Table 34. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1376]	LSB
0	0	1	register [1377]	
0	1	0	register [1378]	
0	1	1	register [1379]	
1	0	0	register [1380]	
1	0	1	register [1381]	
1	1	0	register [1382]	
1	1	1	register [1383]	MSB

Table 35. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1356]	LSB
0	0	1	register [1357]	
0	1	0	register [1358]	
0	1	1	register [1359]	
1	0	0	register [1360]	
1	0	1	register [1361]	
1	1	0	register [1362]	
1	1	1	register [1363]	MSB

Table 36. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1364]	LSB
0	0	1	register [1365]	
0	1	0	register [1366]	
0	1	1	register [1367]	
1	0	0	register [1368]	
1	0	1	register [1369]	
1	1	0	register [1370]	
1	1	1	register [1371]	MSB

Table 37. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1472]	LSB
0	0	1	register [1473]	
0	1	0	register [1474]	
0	1	1	register [1475]	
1	0	0	register [1476]	
1	0	1	register [1477]	
1	1	0	register [1478]	
1	1	1	register [1479]	MSB

Table 38. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1480]	LSB
0	0	1	register [1481]	
0	1	0	register [1482]	
0	1	1	register [1483]	
1	0	0	register [1484]	
1	0	1	register [1485]	
1	1	0	register [1486]	
1	1	1	register [1487]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT0 is defined by registers [1447:1440]

3-bit LUT1 is defined by registers [1359:1352]

3-bit LUT2 is defined by registers [1367:1360]

3-bit LUT3 is defined by registers [1375:1368]

3-bit LUT4 is defined by registers [1383:1376]

3-bit LUT5 is defined by registers [1463:1456]

3-bit LUT6 is defined by registers [1471:1464]

3-bit LUT7 is defined by registers [1479:1472]

3-bit LUT8 is defined by registers [1487:1480]

Table 39 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 39. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

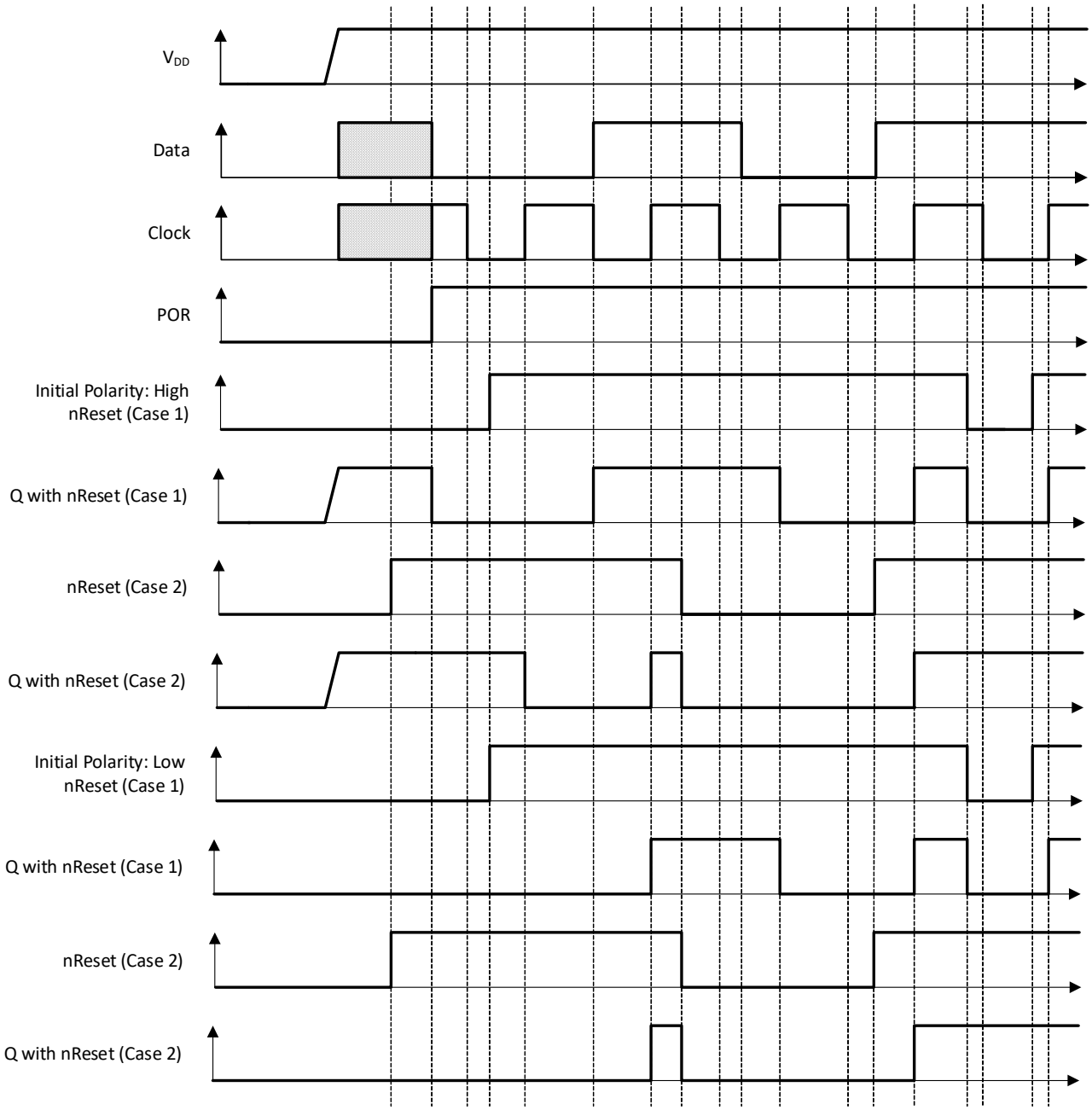

Figure 35. DFF Polarity Operations with nReset

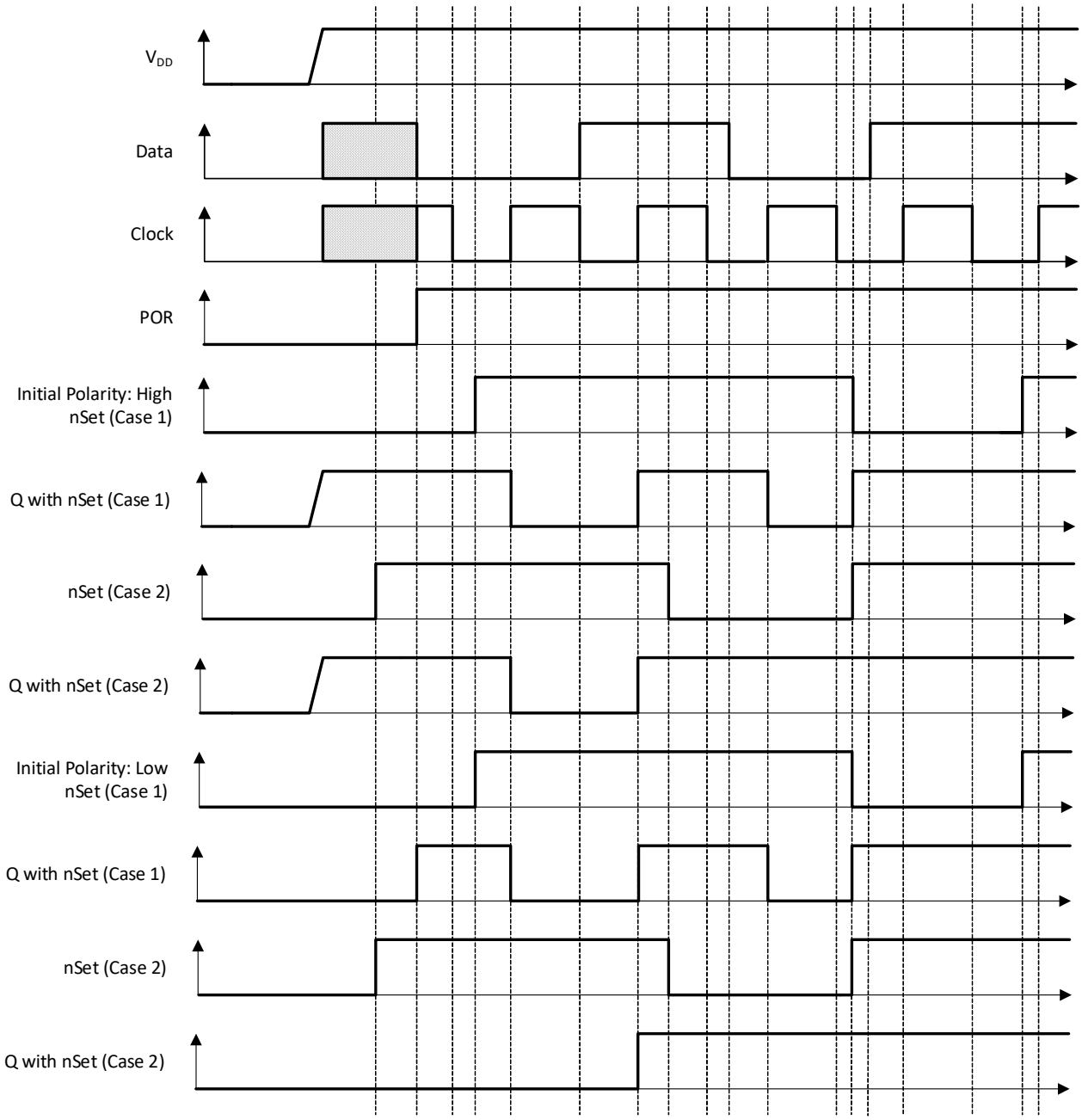

Figure 36. DFF Polarity Operations with nSet

7.4 4-Bit LUT or D Flip-Flop with Set/Reset Macrocell

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

- If register [1436] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.

- If register [1436] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available which are selected by register [1434].

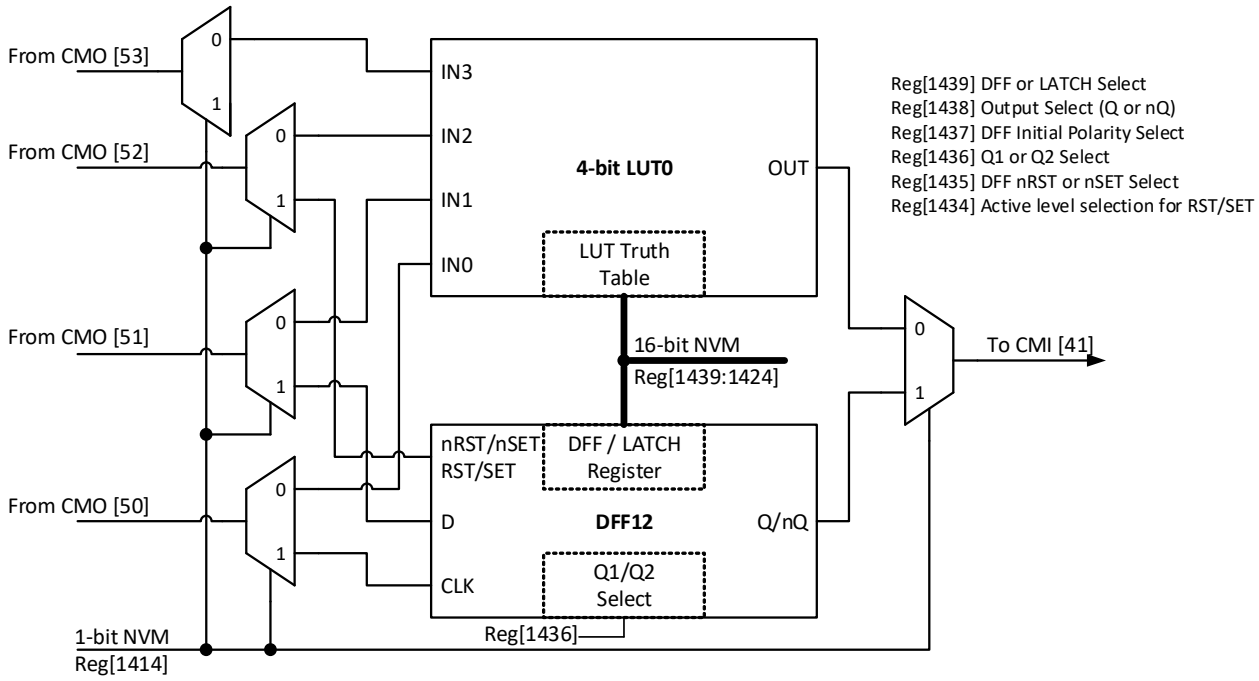

Figure 37. 4-bit LUT0 or DFF12

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 40. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1424]	LSB
0	0	0	1	register [1425]	
0	0	1	0	register [1426]	
0	0	1	1	register [1427]	
0	1	0	0	register [1428]	
0	1	0	1	register [1429]	
0	1	1	0	register [1430]	
0	1	1	1	register [1431]	
1	0	0	0	register [1432]	
1	0	0	1	register [1433]	
1	0	1	0	register [1434]	
1	0	1	1	register [1435]	
1	1	0	0	register [1436]	
1	1	0	1	register [1437]	
1	1	1	0	register [1438]	
1	1	1	1	register [1439]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT0 is defined by registers [1439:1424]

Table 41. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.5 3-bit LUT or Pipe Delay/Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled

by registers [1419:1416] for OUT0 and registers [1423:1420] for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46857-A design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG46857-A). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [1413]).

In the Ripple Counter mode there are 3 options for setting which use 7 bits. There are 3 bits to set **nSET value (SV)** in range from 0 to 7. This value will be set into the Ripple Counter outputs when nSET input goes LOW. **End value (EV)** will use 3 bits for setting output code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The **Functionality mode** option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 39.

Every step is executed by the rising edge on CLK input.

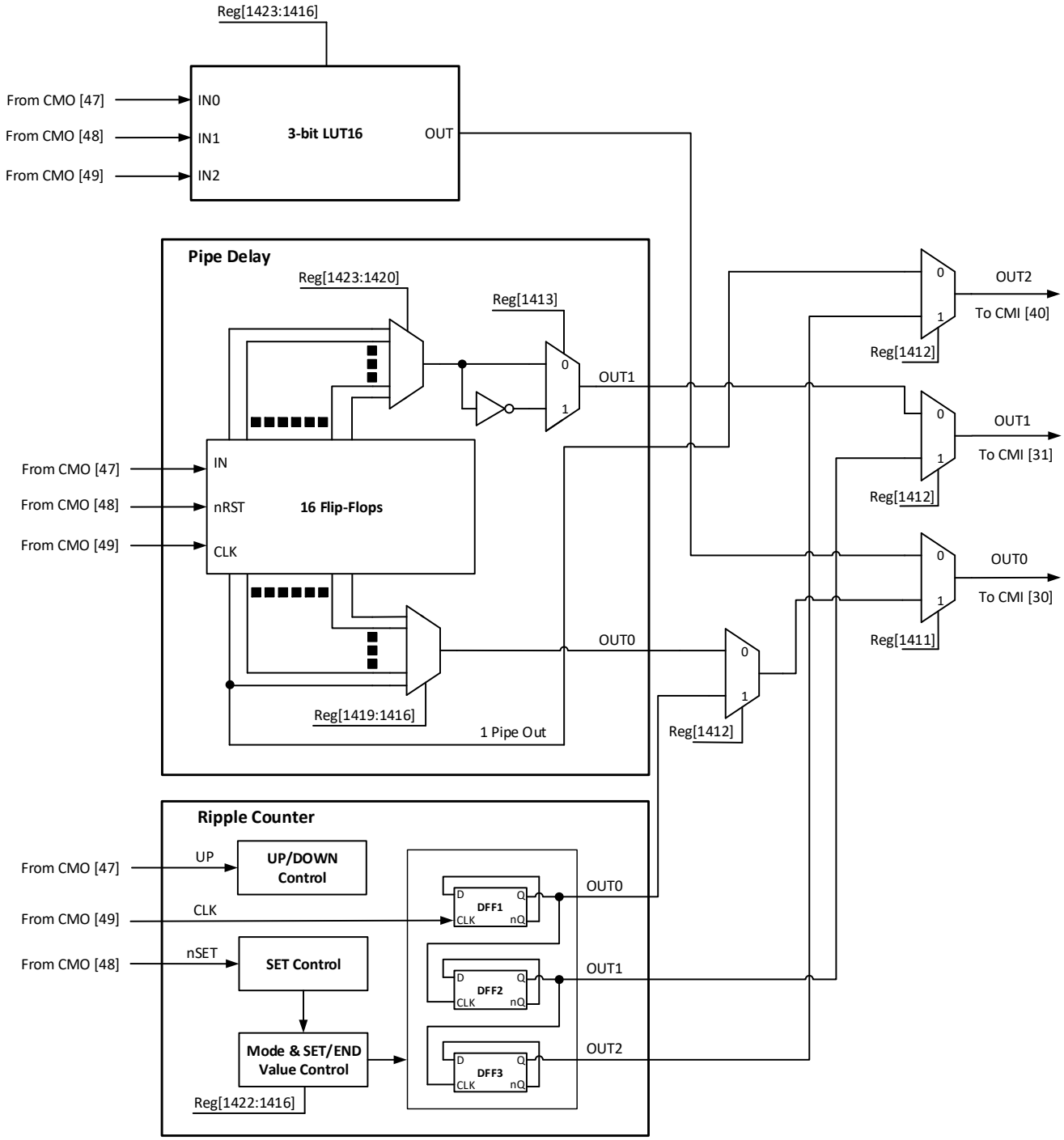

Figure 38. 3-bit LUT16/Pipe Delay/Ripple Counter

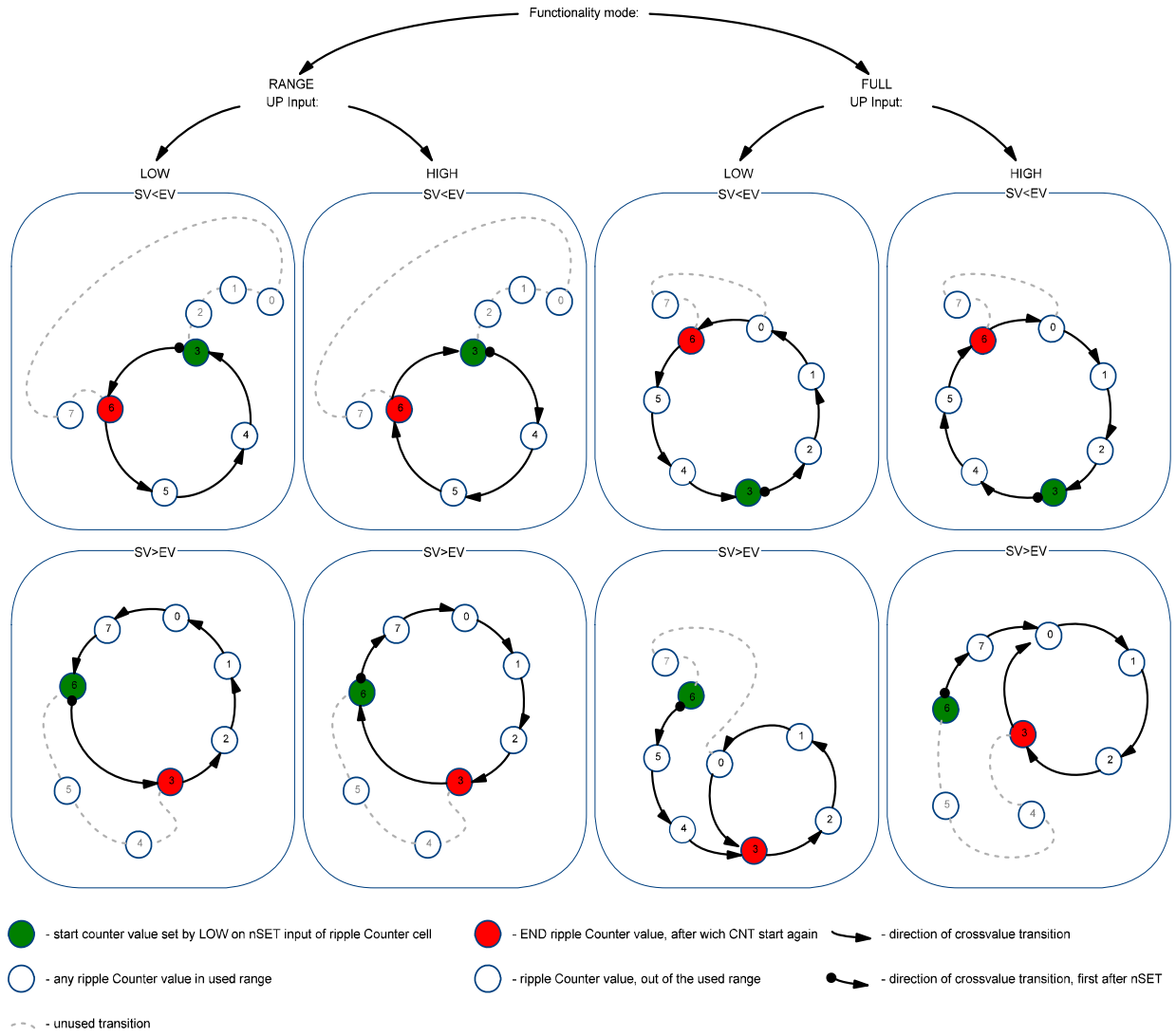

Figure 39. Example: Ripple Counter Functionality

7.5.1 3-bit LUT or Pipe Delay Macrocells Used as 3-bit LUT

Table 42. 3-bit LUT16 Truth Table

IN2	IN1	IN0	OUT
0	0	0	register [1416]
0	0	1	register [1417]
0	1	0	register [1418]
0	1	1	register [1419]
1	0	0	register [1420]
1	0	1	register [1421]
1	1	0	register [1422]
1	1	1	register [1423]

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT16 is defined by registers [1423:1416]

8. Multi-Function Macrocells

The SLG46857-A has 8 Multi-Function macrocells that can serve more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes, such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 40.

See the list below for the functions that can be implemented in these macrocells:

- Seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-bit Counter/Delay/FSM

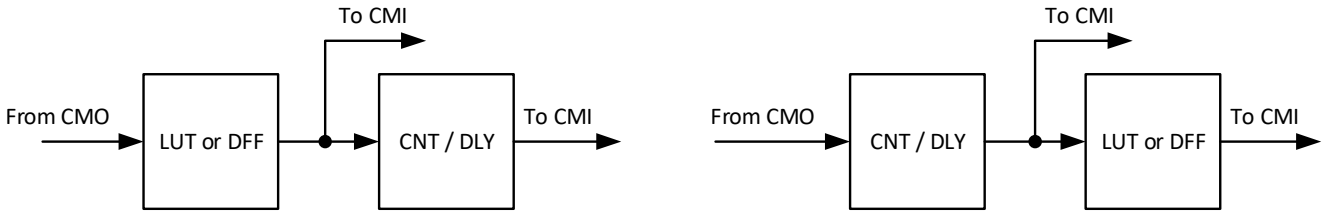

Figure 40. Possible Connections inside Multi-Function Macrocell

Inputs/Outputs for the 8 Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells

There are seven macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which define its initial value after GPAK is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 7.1 2-Bit LUT or D Flip-Flop Macrocells and 8.3 CNT/DLY/FSM Timing Diagrams.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

CNT6 and CNT7 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 15.6.1 Reading Counter Data via I2C for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

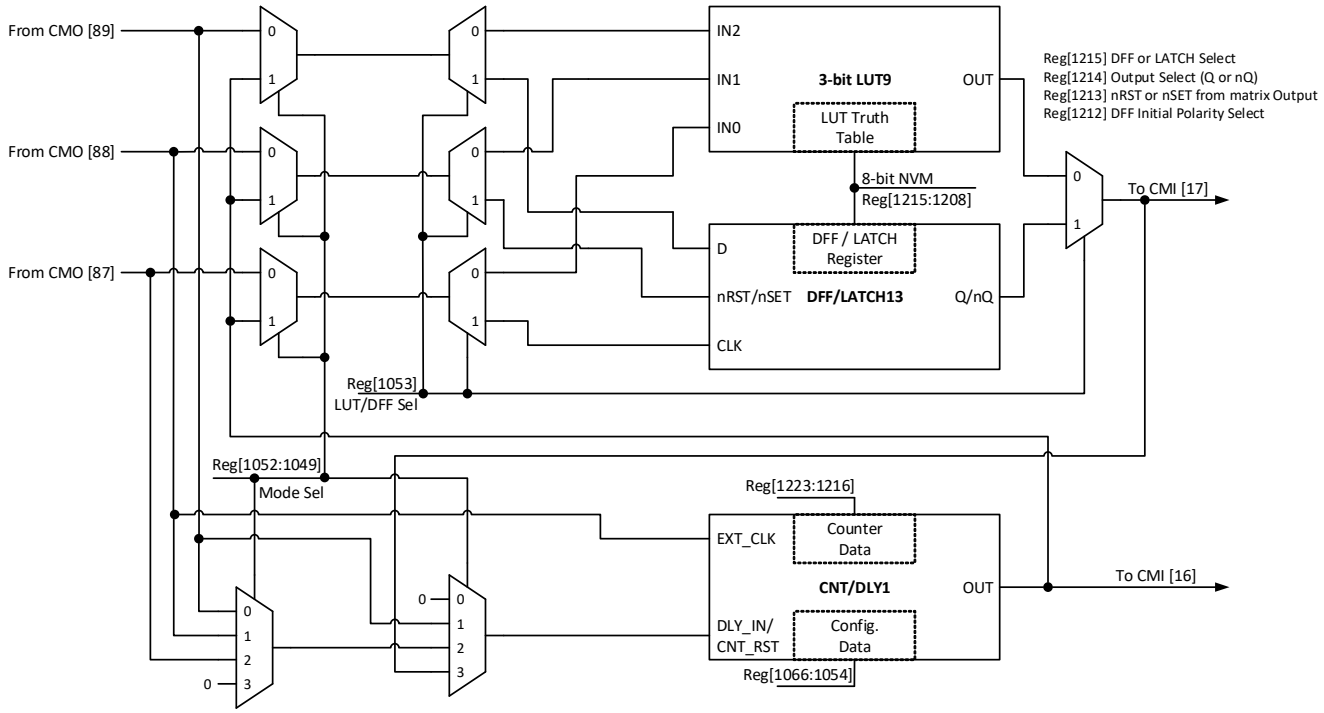

Figure 41. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY1)

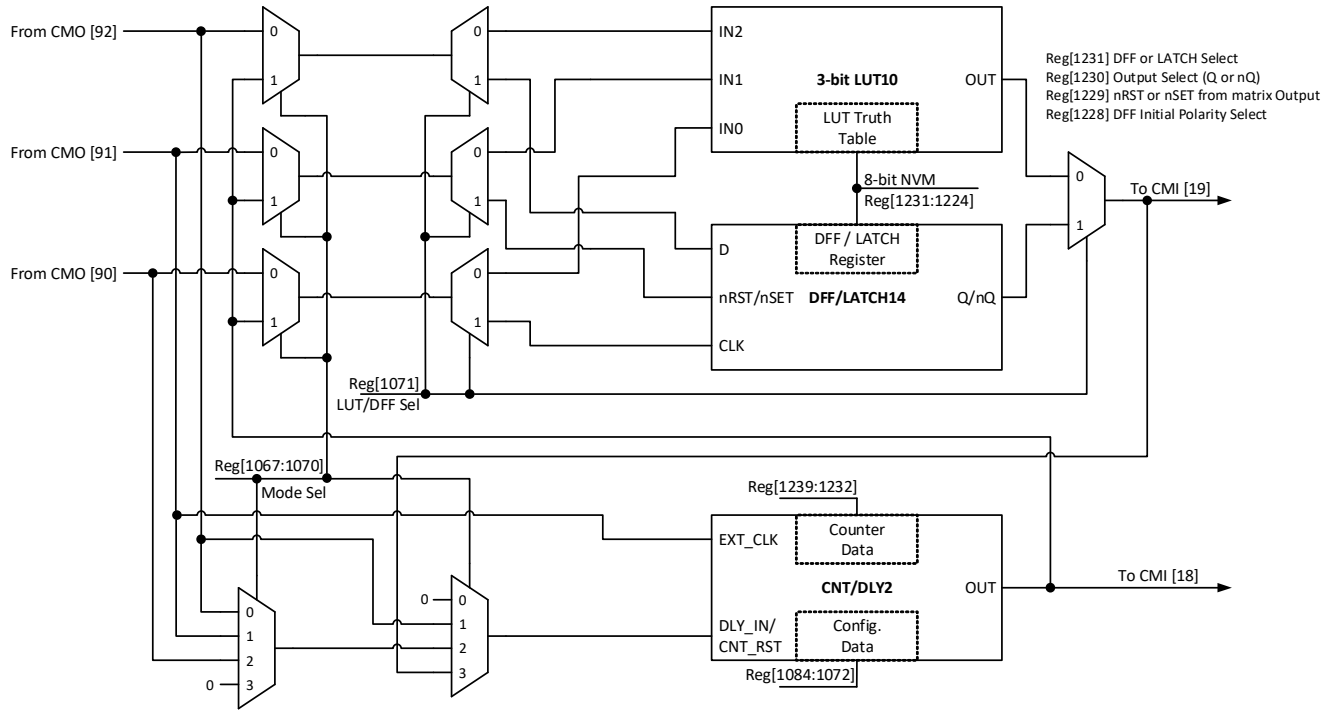

Figure 42. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY2)

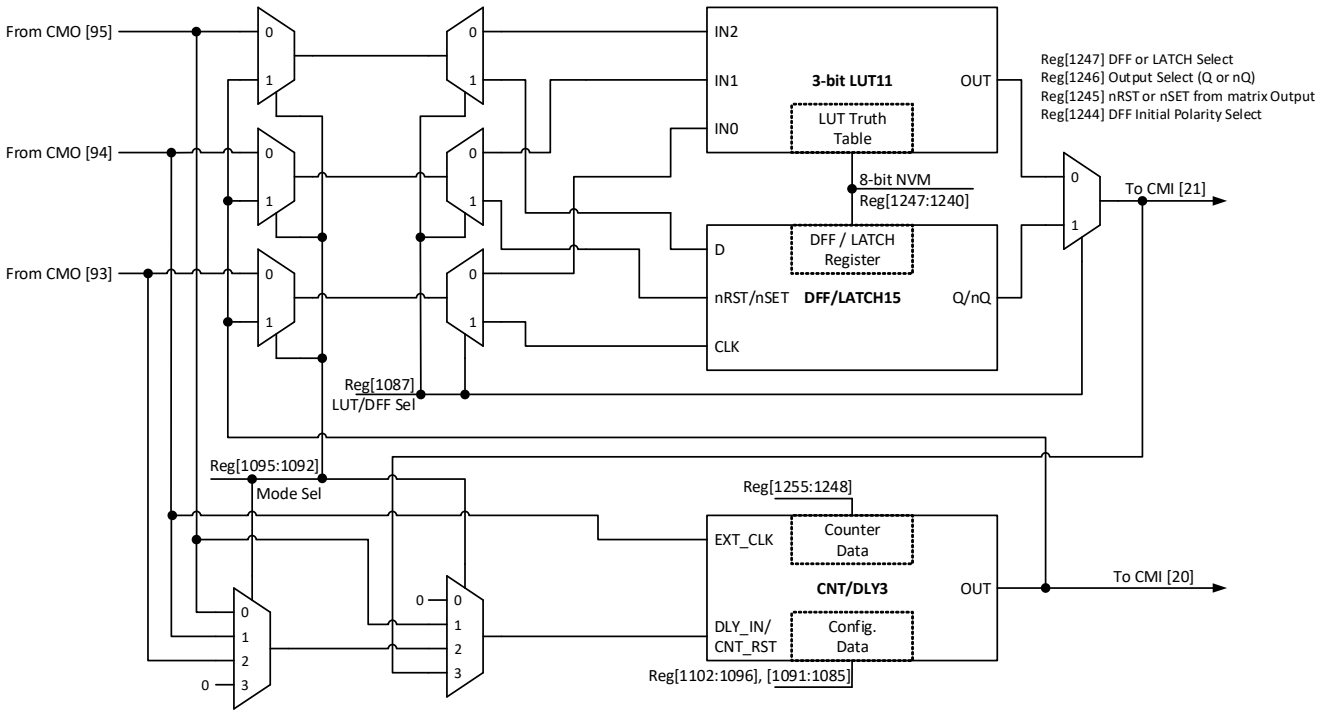

Figure 43. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY3)

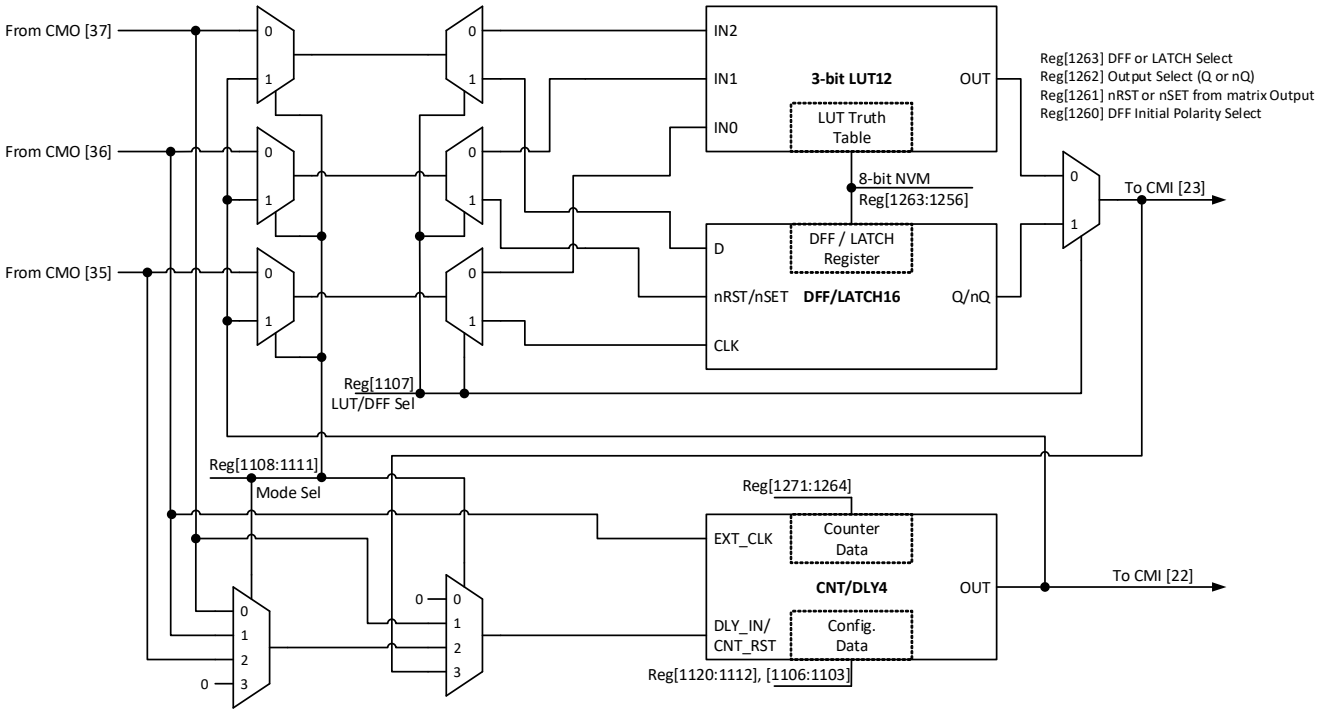

Figure 44. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY4)

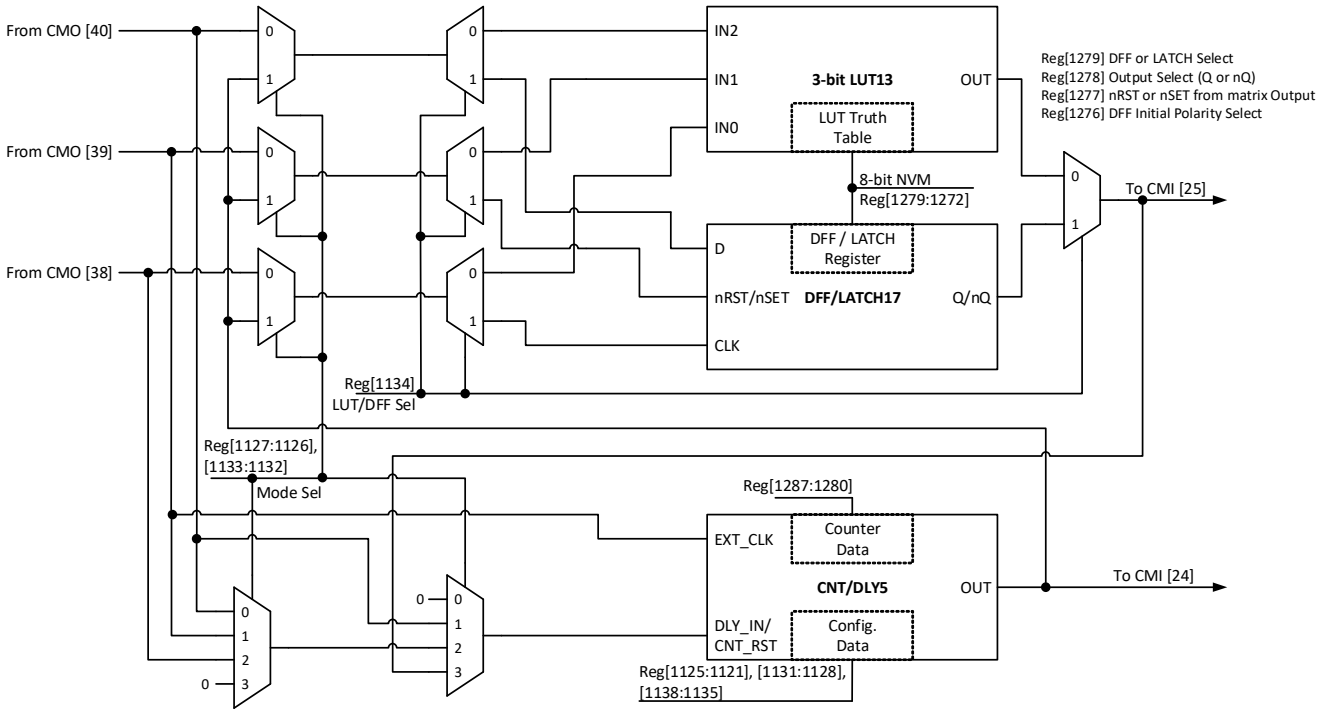

Figure 45. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT13/DFF17, CNT/DLY5)

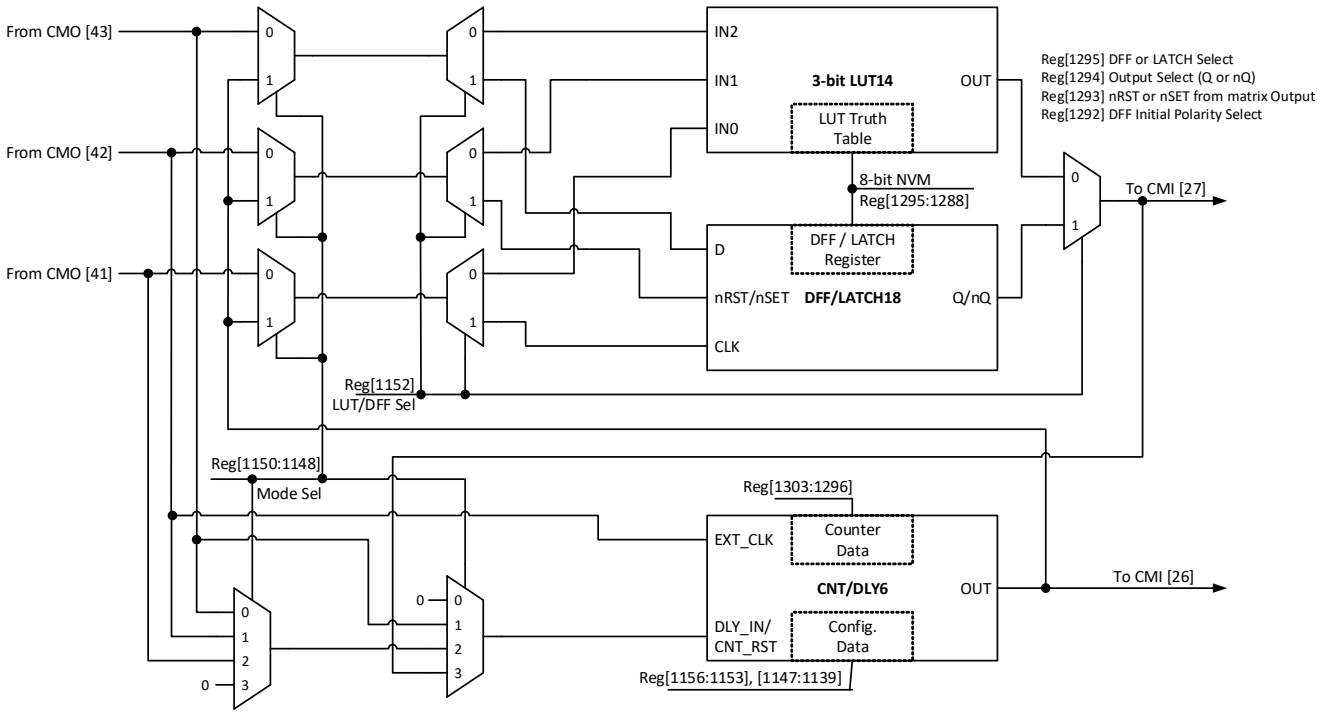

Figure 46. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT14/DFF18, CNT/DLY6)

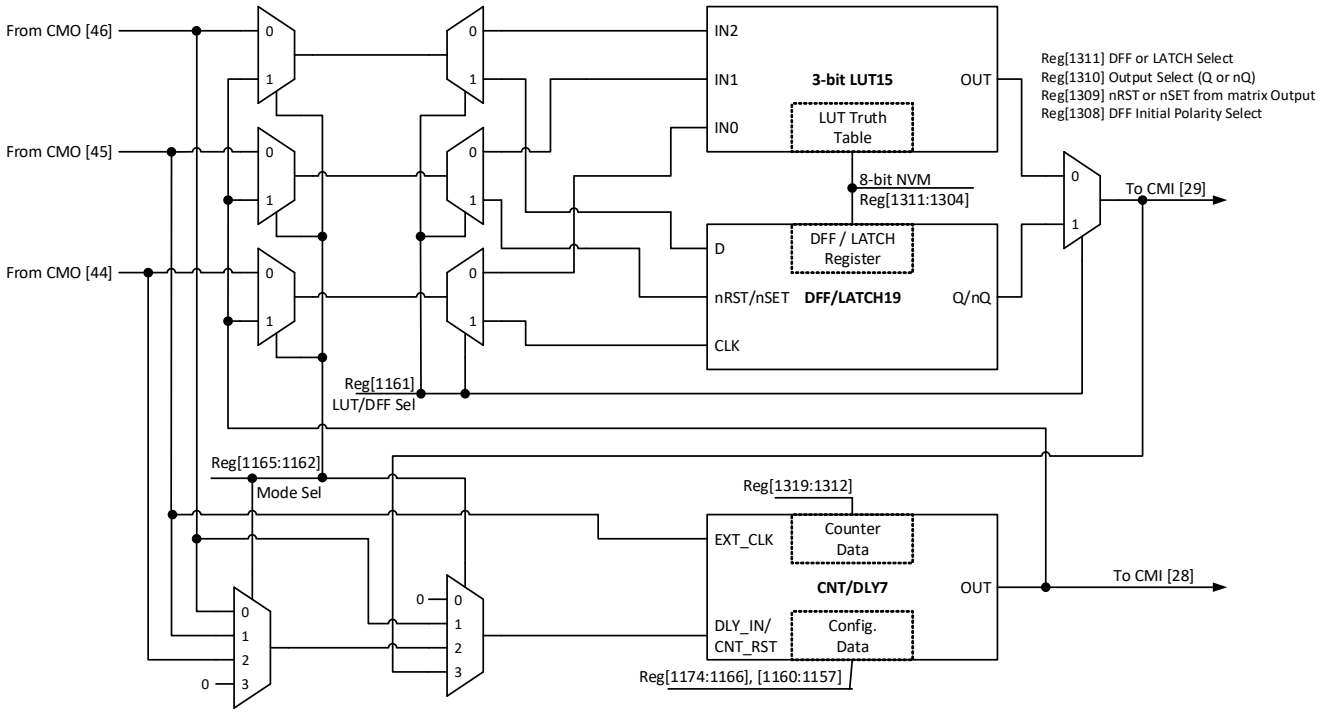

Figure 47. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT15/DFF19, CNT/DLY7)

As shown in Figures 41-47 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-bit LUT or CNT/DLYs Used as 3-bit LUTs

Table 43. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1208]	LSB
0	0	1	register [1209]	
0	1	0	register [1210]	
0	1	1	register [1211]	
1	0	0	register [1212]	
1	0	1	register [1213]	
1	1	0	register [1214]	
1	1	1	register [1215]	MSB

Table 44. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1224]	LSB
0	0	1	register [1225]	
0	1	0	register [1226]	
0	1	1	register [1227]	
1	0	0	register [1228]	
1	0	1	register [1229]	
1	1	0	register [1230]	
1	1	1	register [1231]	MSB

Table 45. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1240]	LSB
0	0	1	register [1241]	
0	1	0	register [1242]	
0	1	1	register [1243]	
1	0	0	register [1244]	
1	0	1	register [1245]	
1	1	0	register [1246]	
1	1	1	register [1247]	MSB

Table 46. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1256]	LSB
0	0	1	register [1257]	
0	1	0	register [1258]	
0	1	1	register [1259]	
1	0	0	register [1260]	
1	0	1	register [1261]	
1	1	0	register [1262]	
1	1	1	register [1263]	MSB

Table 47. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1272]	LSB
0	0	1	register [1273]	
0	1	0	register [1274]	
0	1	1	register [1275]	
1	0	0	register [1276]	
1	0	1	register [1277]	
1	1	0	register [1278]	
1	1	1	register [1279]	MSB

Table 48. 3-bit LUT14 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1288]	LSB
0	0	1	register [1289]	
0	1	0	register [1290]	
0	1	1	register [1291]	
1	0	0	register [1292]	
1	0	1	register [1293]	
1	1	0	register [1294]	
1	1	1	register [1295]	MSB

Table 49. 3-bit LUT15 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1304]	LSB
0	0	1	register [1305]	
0	1	0	register [1306]	
0	1	1	register [1307]	
1	0	0	register [1308]	
1	0	1	register [1309]	
1	1	0	register [1310]	
1	1	1	register [1311]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT9 is defined by registers [1215:1208]

3-bit LUT10 is defined by registers [1231:1224]

3-bit LUT11 is defined by registers [1247:1240]

3-bit LUT12 is defined by registers [1263:1256]

3-bit LUT13 is defined by registers [1279:1272]

3-bit LUT14 is defined by registers [1295:1288]

3-bit LUT15 is defined by registers [1311:1304]

8.2 4-bit LUT or DFF/LATCH with 16-bit Counter/Delay Macrocell

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flops or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.

This macrocell can also operate in a frequency detection or edge detection mode.

This macrocell can have its active count value read via I^2C. See Section 15.6.1 Reading Counter Data via I2C for further details.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.
Initial state = 0 And After two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-bit LUT or DFF/LATCH with 16-bit CNT/DLY Block Diagram

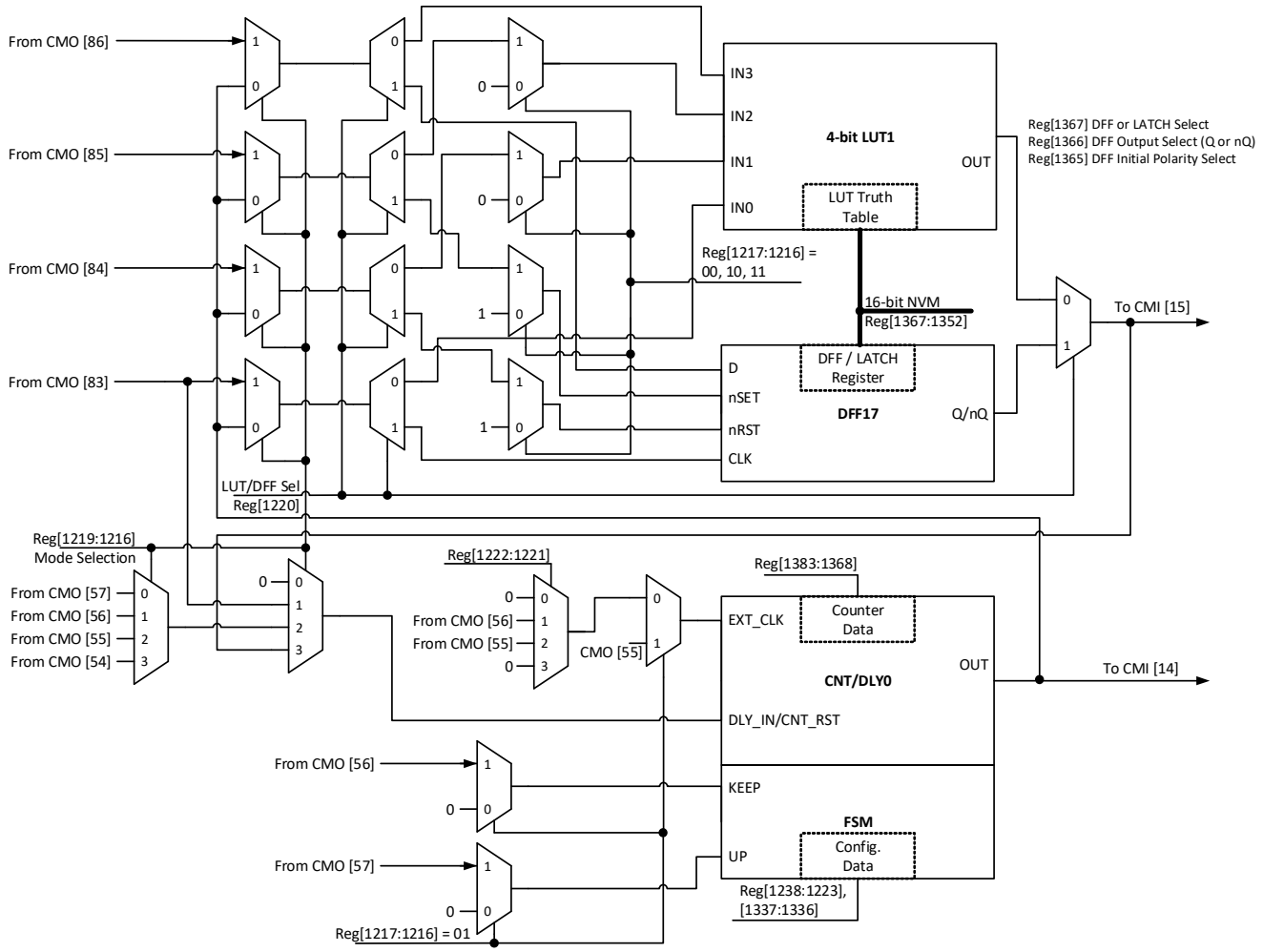

Figure 48. 4-bit LUT1 or CNT/DLY0

8.2.2 4-bit LUT or 16-bit Counter/Delay Macrocells Used as 4-bit LUTs

Table 50. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1176]	LSB
0	0	0	1	register [1177]	
0	0	1	0	register [1178]	
0	0	1	1	register [1179]	
0	1	0	0	register [1180]	
0	1	0	1	register [1181]	
0	1	1	0	register [1182]	
0	1	1	1	register [1183]	
1	0	0	0	register [1184]	
1	0	0	1	register [1185]	
1	0	1	0	register [1186]	
1	0	1	1	register [1187]	
1	1	0	0	register [1188]	
1	1	0	1	register [1189]	
1	1	1	0	register [1190]	
1	1	1	1	register [1191]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT1 is defined by registers [1191:1176]

Table 51. 4-bit LUT Standard Digital Functions

Function	MSB																LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	0	1

8.3 CNT/DLY/FSM Timing Diagrams

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY7

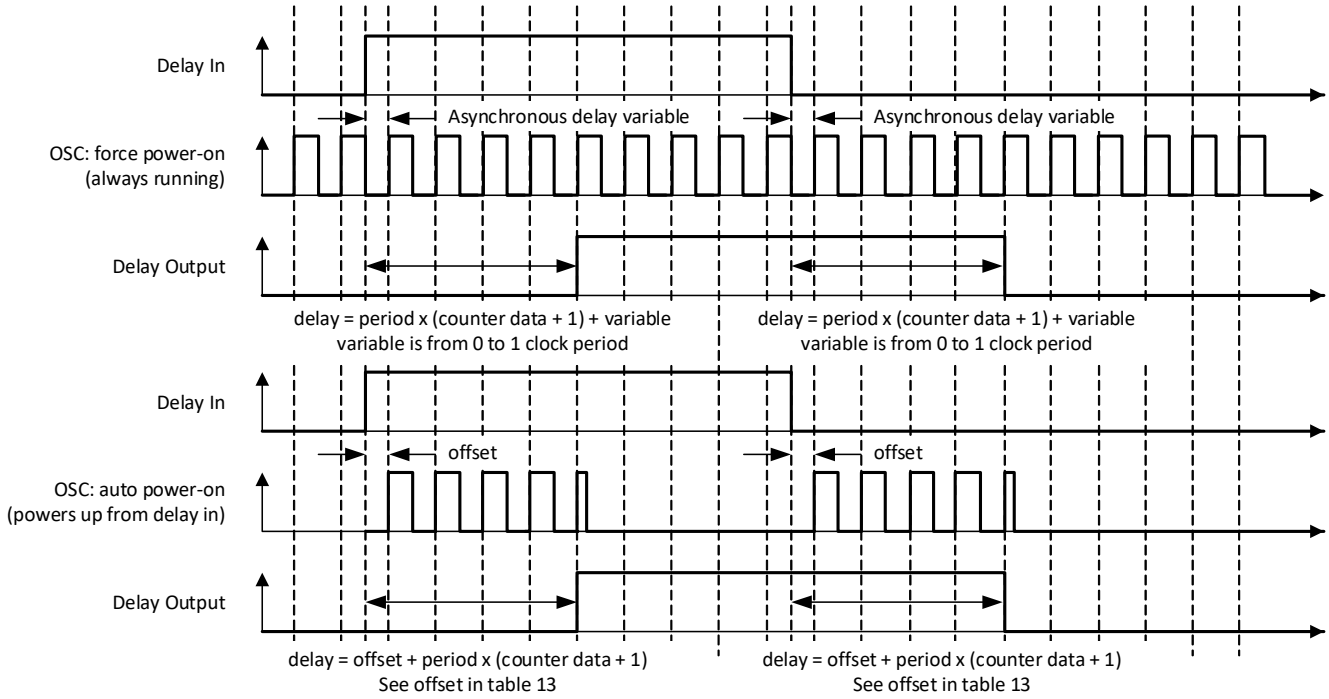

Figure 49. Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

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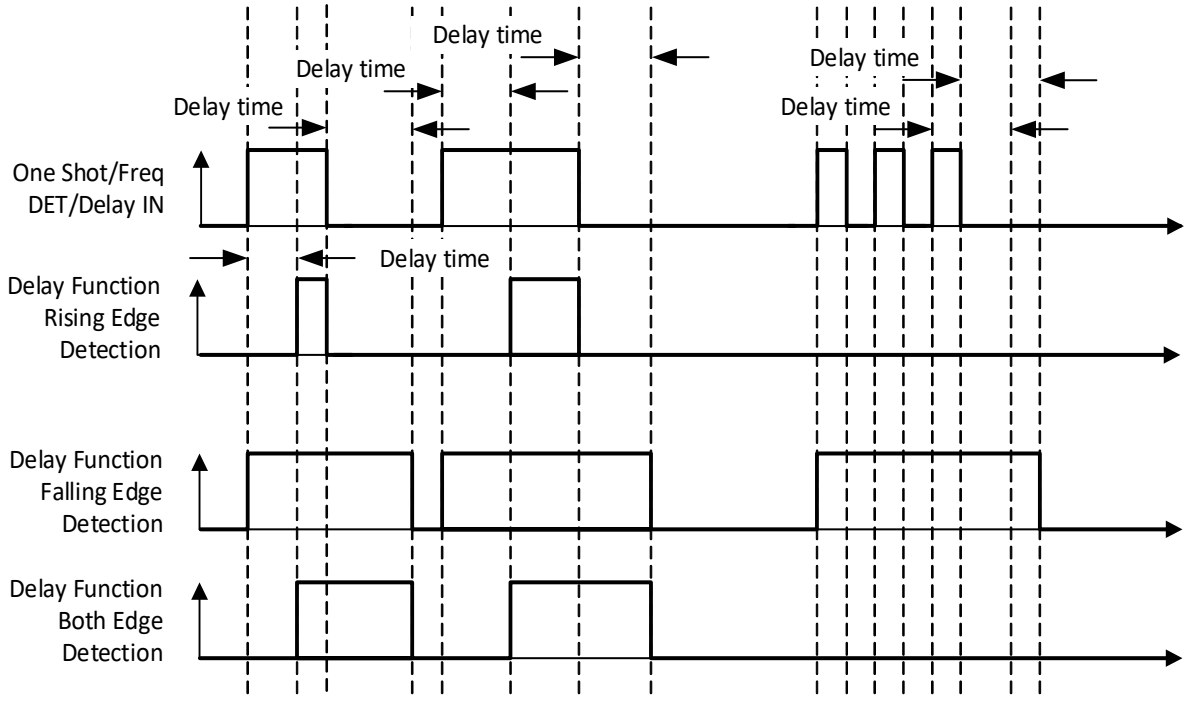

Figure 50. Delay Mode Timing Diagram for Different Edge Select Mode

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY7

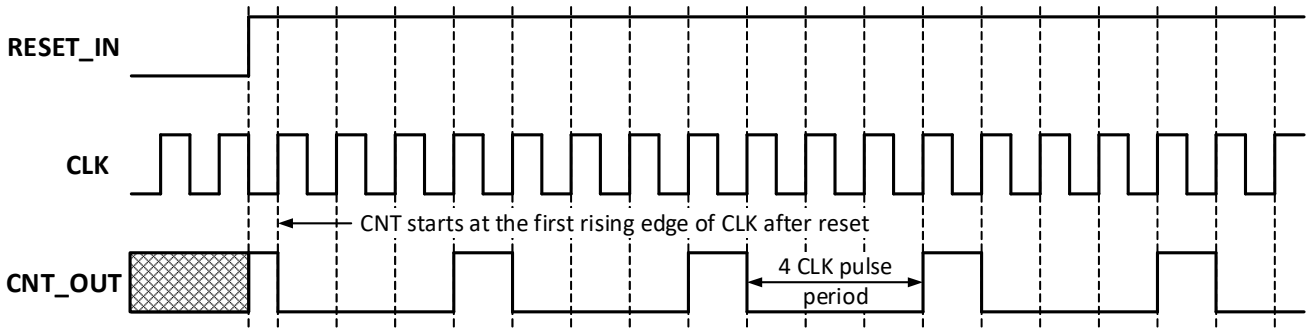

Figure 51. Counter Mode Timing Diagram without Two DFFs Synced Up

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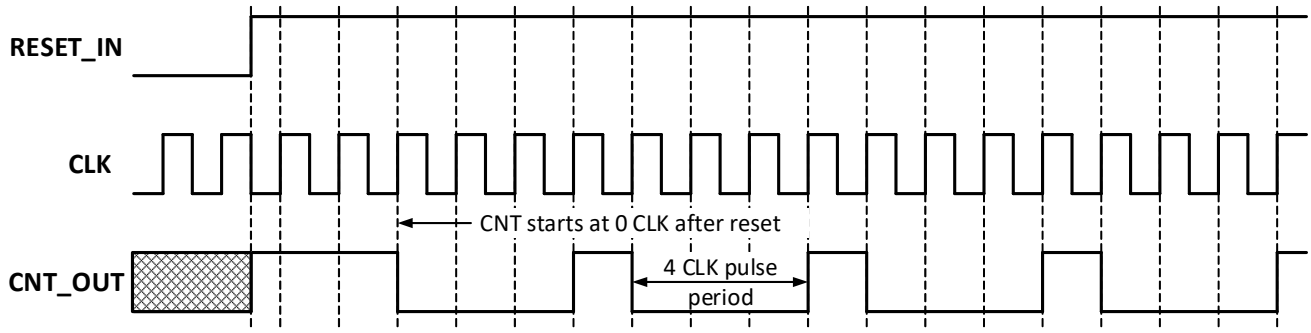


Figure 52. Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY7

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width determines by counter data and clock selection properties. The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

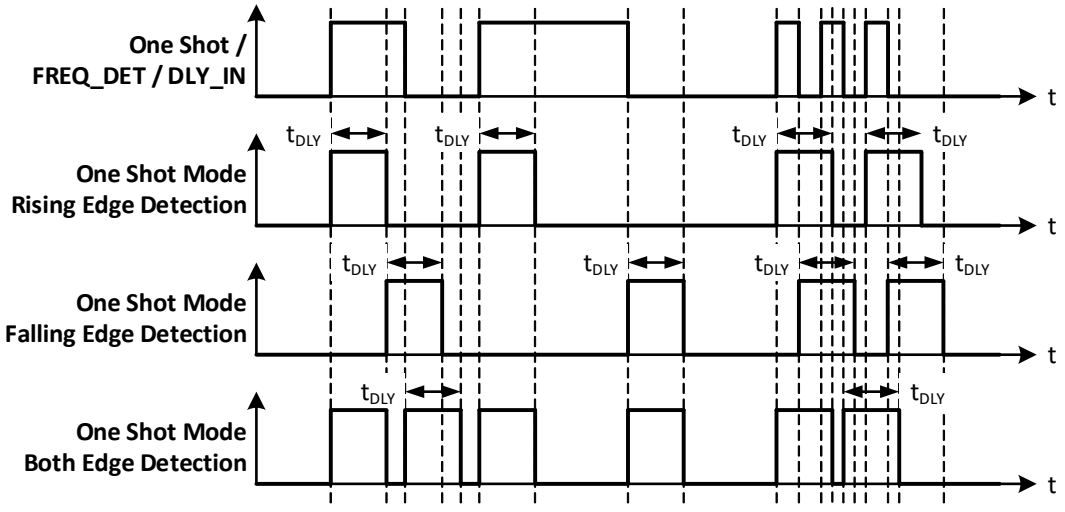


Figure 53. One-Shot Function Timing Diagram

This macrocell generates a high-level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is HIGH.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY7

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

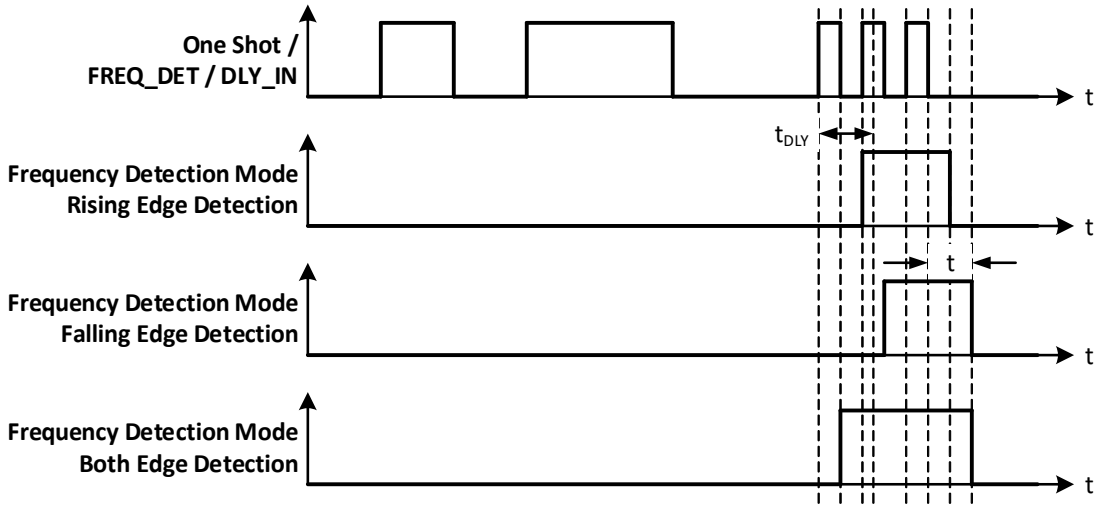


Figure 54. Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY7

The macrocell generates high-level short pulse when detecting the respective edge. See Table 13.

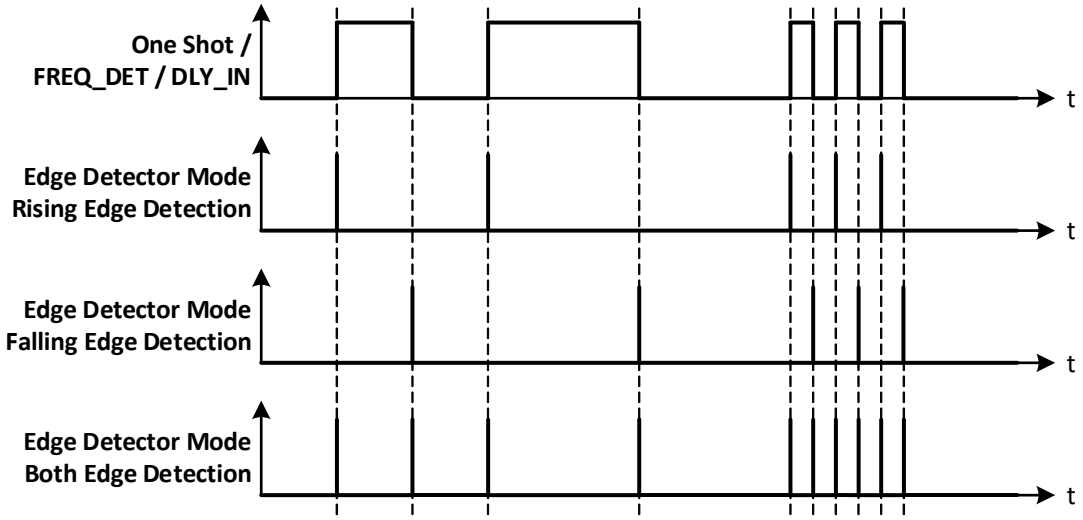


Figure 55. Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY7

In Delayed Edge Detection Mode, High level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated. See Figure 56.

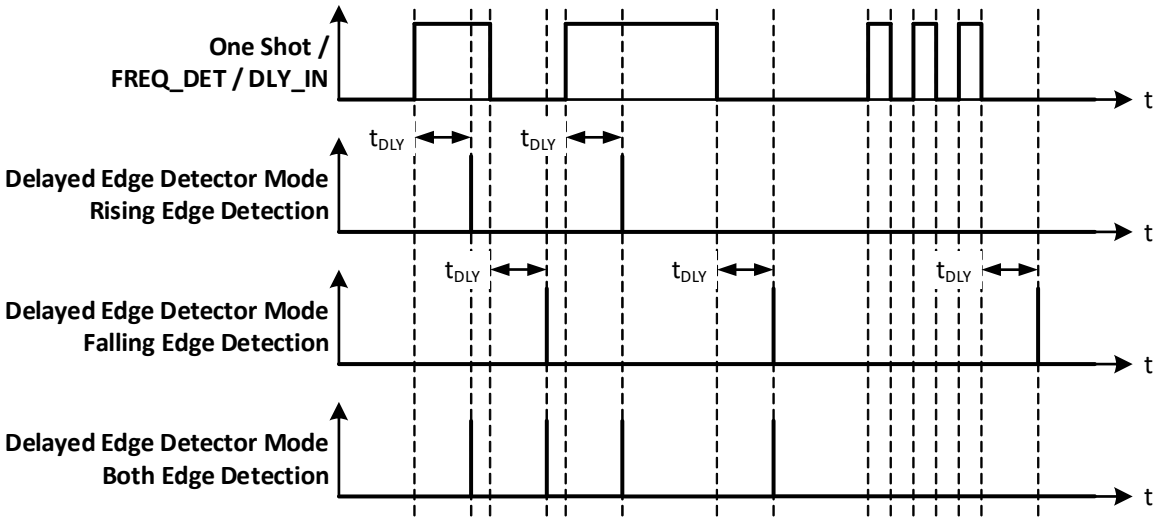
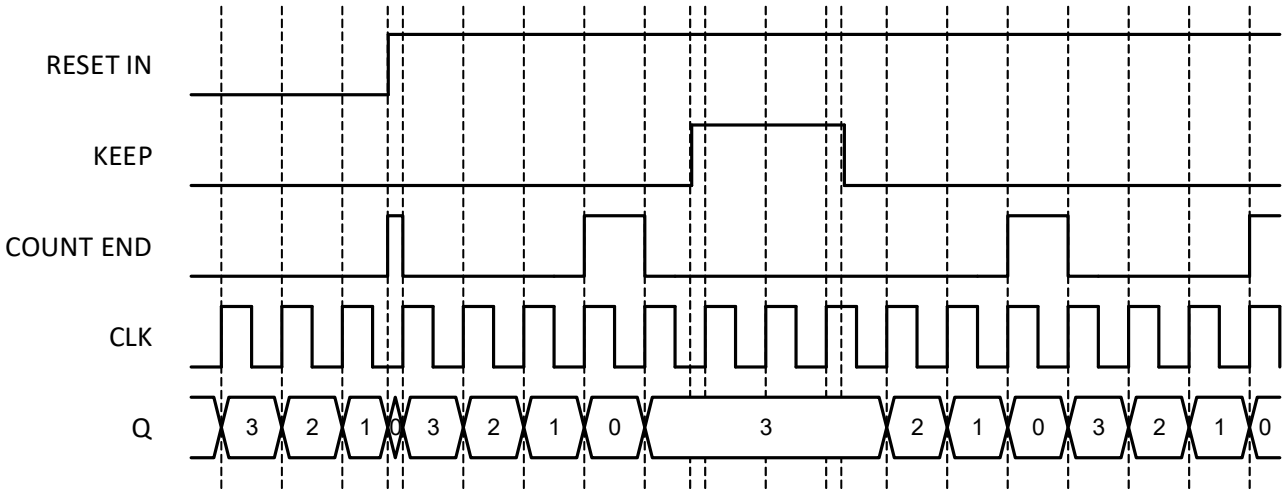


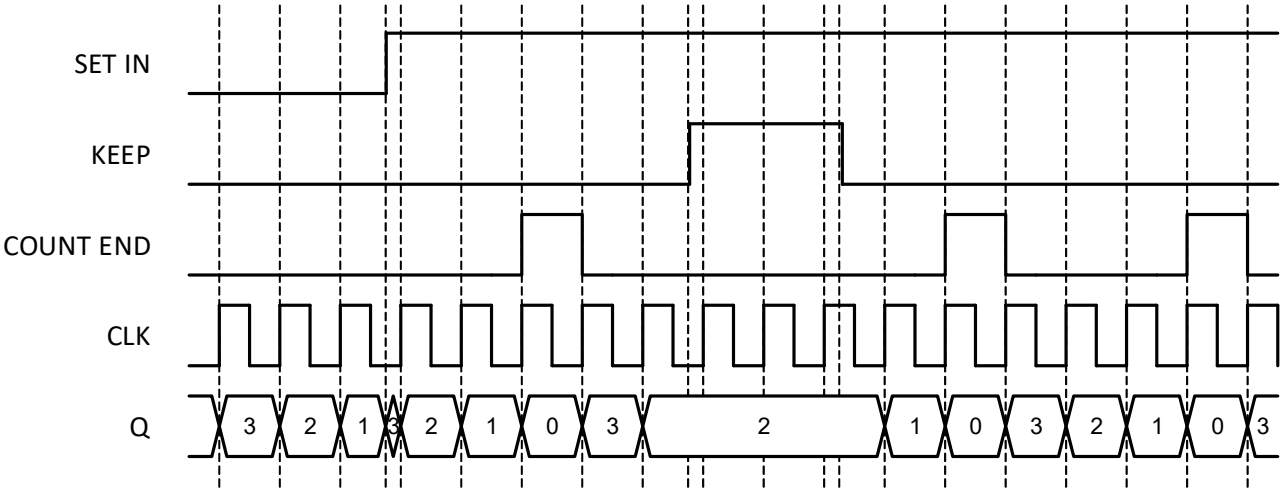
Figure 56. Delayed Edge Detection Mode Timing Diagram

8.3.7 CNT/FSM Mode CNT/DLY0



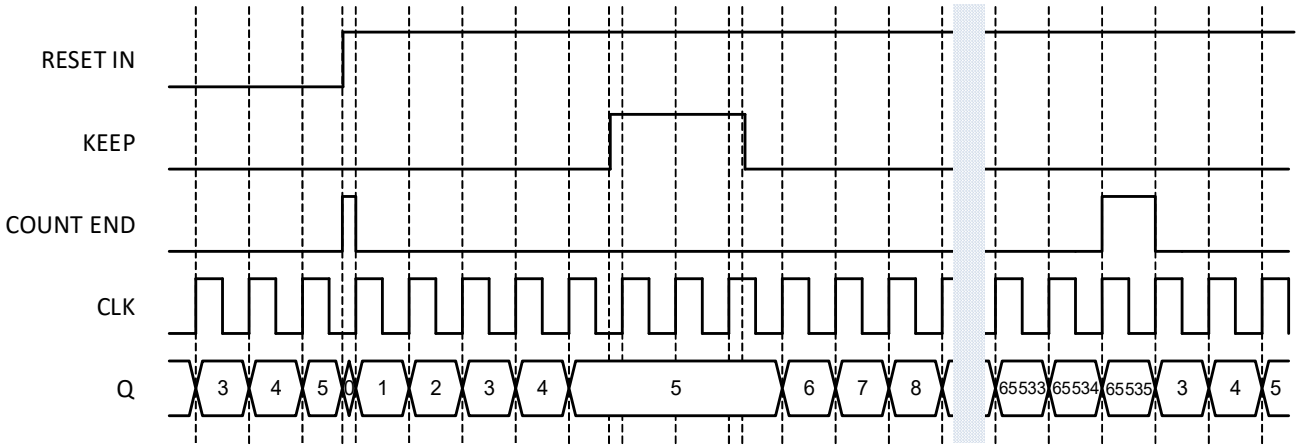
Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 57. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0)



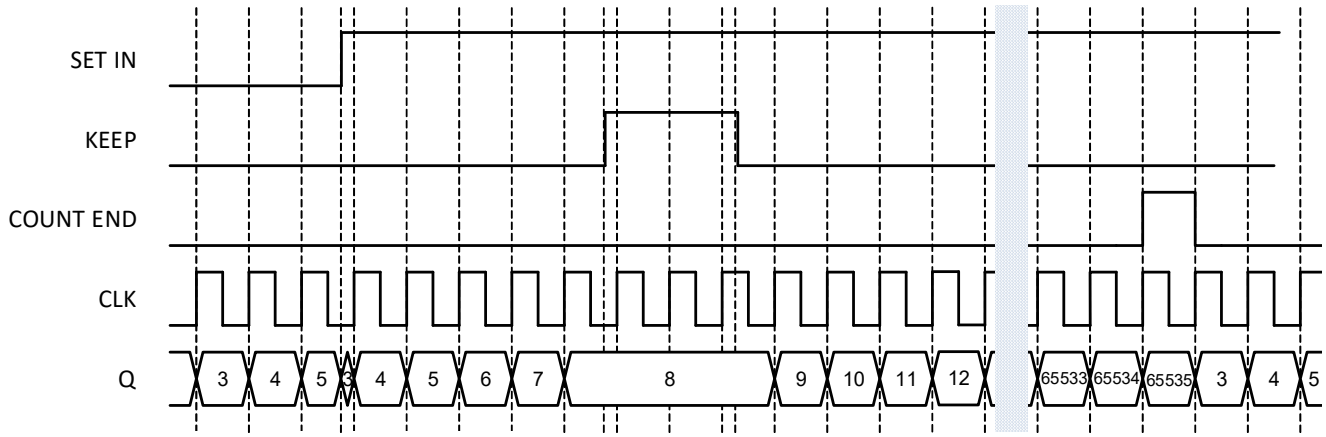
Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 58. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 59. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 60. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator Is Forced On, UP = 1)

8.3.8 Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. The counter value is shifted for two rising edges of the clock signal in Delay/One-Shot/Frequency Detect modes compared to Counter mode. See Figure 61.

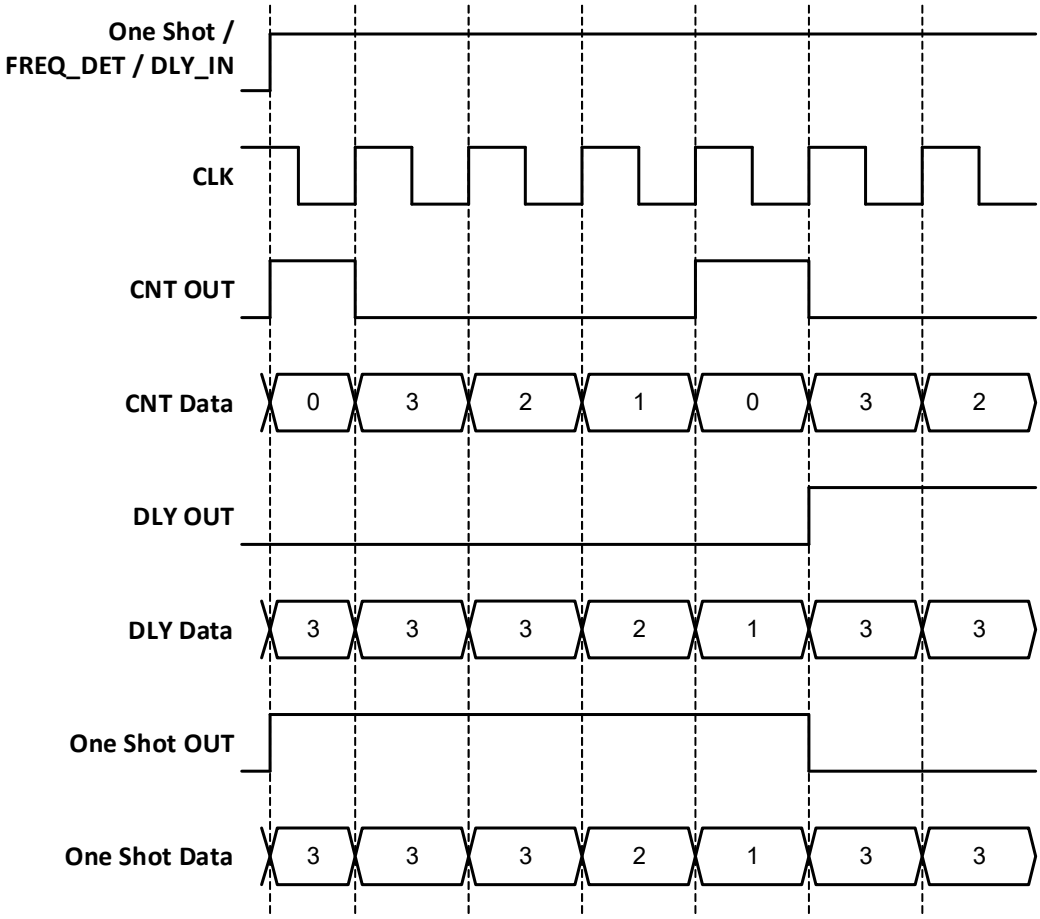


Figure 61. Counter Value, Counter Data = 3

8.4 Wake and Sleep Controller

The SLG46857-A has a Wake and Sleep function for all ACMPs. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1032:1031] = 11 and register [1046] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in wake and sleep timing in case it dynamically powers on/off.

Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.

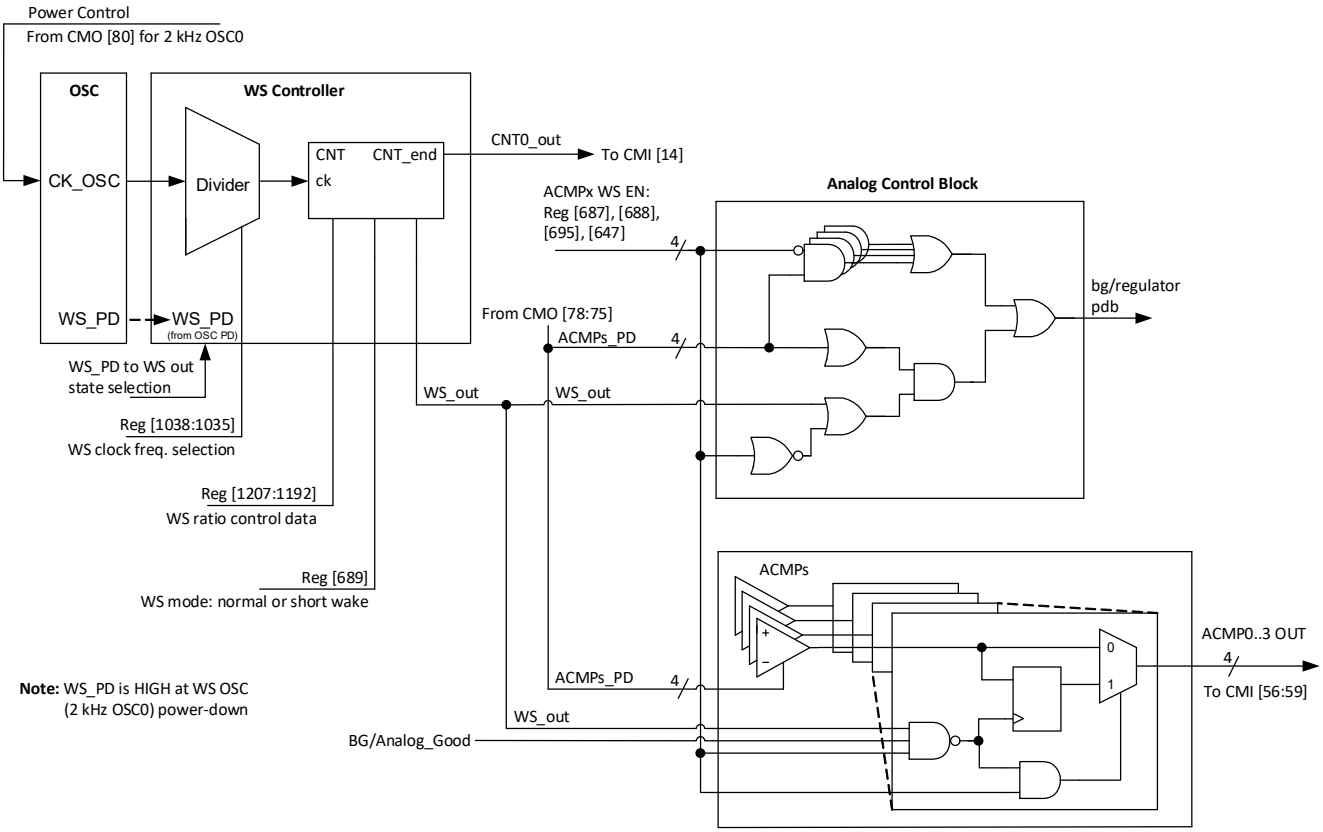
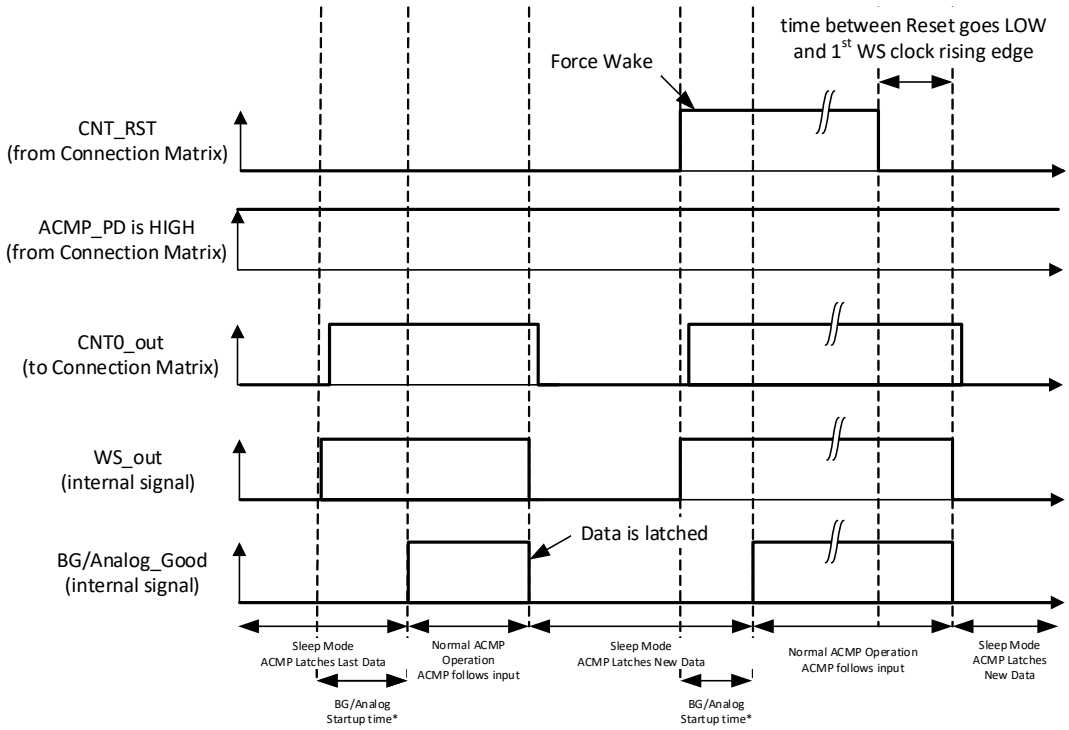
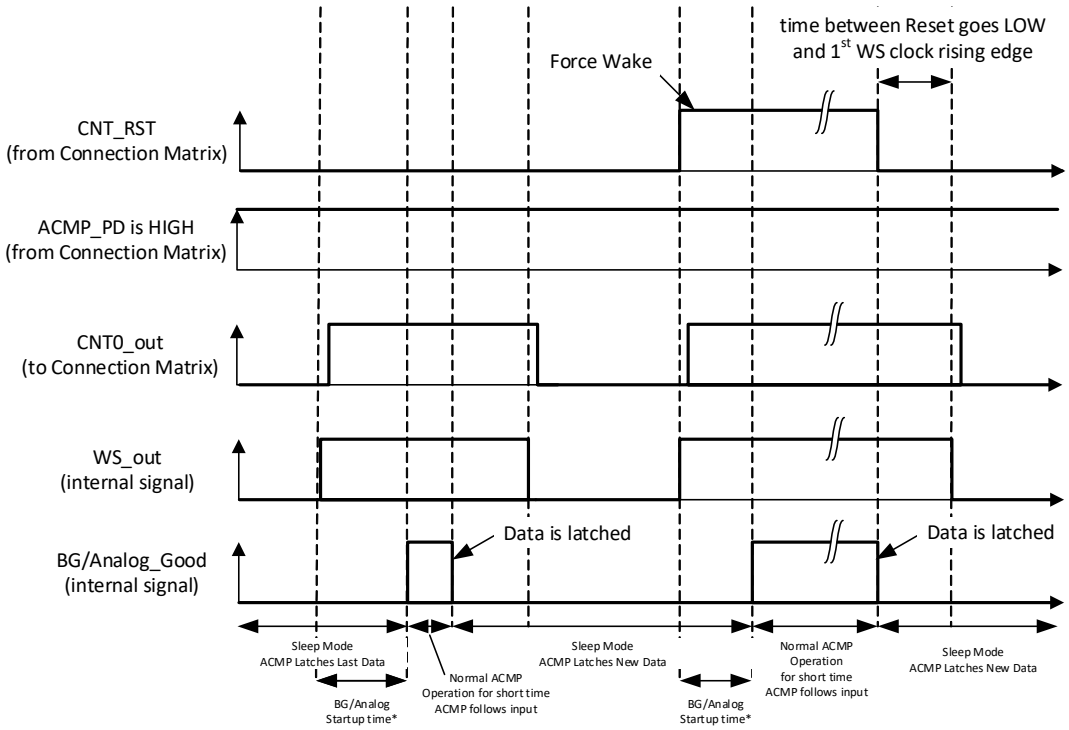


Figure 62. Wake/Sleep Controller



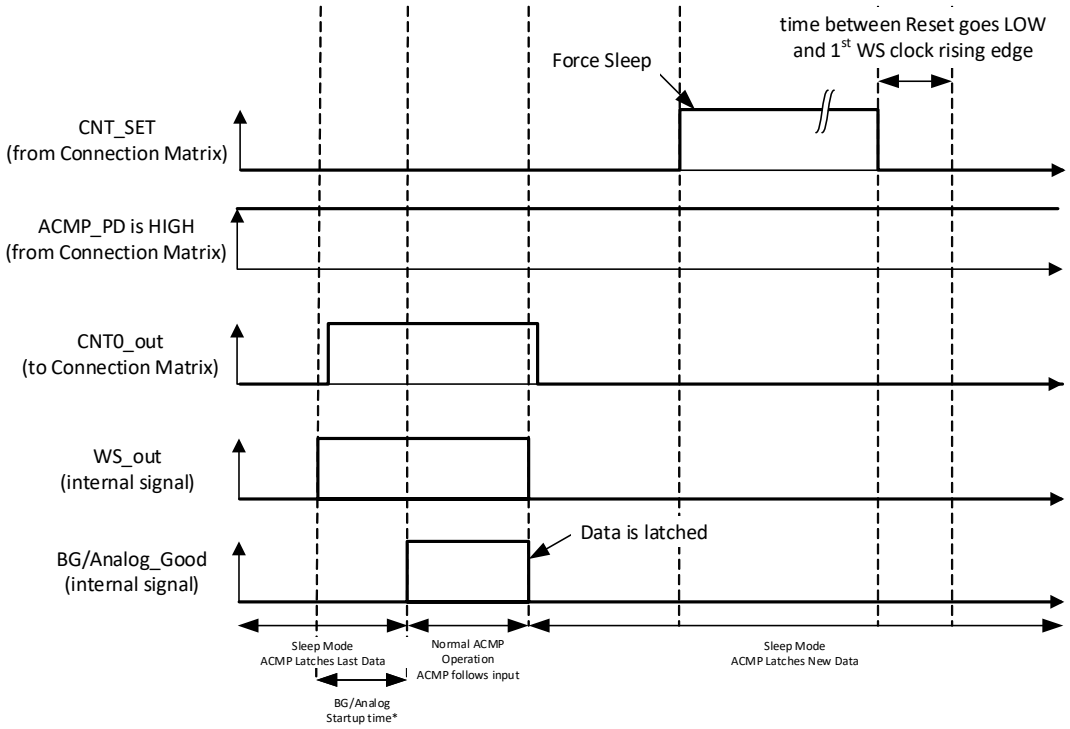
Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 63. Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used



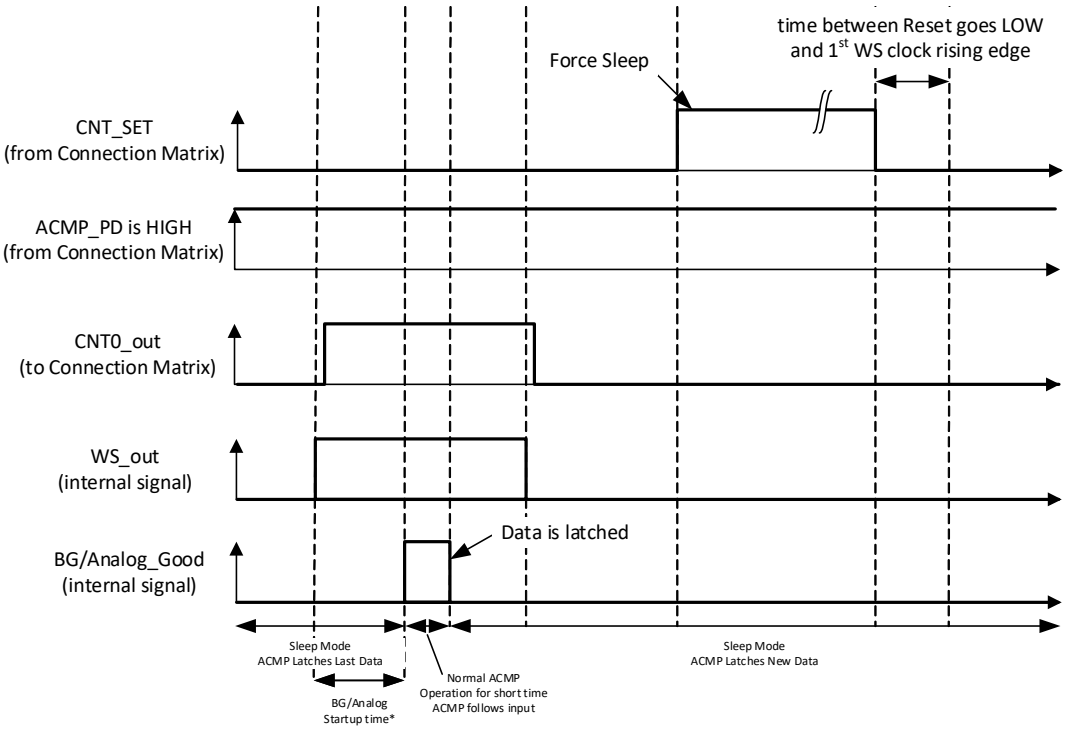
Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 64. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 65. Wake/Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 66. Wake/Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. Therefore, 8 periods of the Oscillator0 is recommended for the wake time, when BG is configured to Auto Power mode. If low power BG is always on, Oscillator0 period is longer than required wake time. The BG/analog start up time will take maximal 450 us for ACMP0/1 and a shorter time for ACMP2/3. The short wake mode can be used to reduce the current consumption.

To use any ACMP under WS controller, the following settings must be done:

- ACMP Power Up Input from matrix = 1 (for each ACMP separately);
- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMP);
- Register WS → enable (for each ACMP separately);
- CNT/DLY0 set/reset input = 0 (for all ACMP).

The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535)

  User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMP until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMP. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMP while counter is counting up to the end.

Note: The OSC0 matrix power-down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode

  High level Set/Reset - switches mode Set/Reset when level is High

Note: Q mode operates only in case of "High Level Set/Reset".

- Wake time selection - time required for wake signal to turn the ACMPxH on

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.

- Keep - pauses counting while Keep = 1
- Up - reverses counting

  If Up = 1, CNT is counting up from user selected value to 65535.

  If Up = 0, CNT is counting down from user selected value to 0.

9. Analog Comparators

There are two High Speed and two Low Power Rail-to-Rail General Purpose Analog Comparators (ACMP) macrocells in the SLG46857-A. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0H PWR UP, ACMP1H PWR UP, ACMP2L PWR UP, and ACMP3L PWR UP) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

Two of the four General Purpose Analog Comparators are optimized for high speed operation (ACMP0H and ACMP1H), and two other are optimized for low power operation (ACMP2L and ACMP3L).

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The gain divider is unbuffered and has input resistance of 2 MΩ (typ) for 0.5x, 0.33x, 0.25x, and 10 GΩ for 1x. Each of the ACMP cells has a negative input signal that is either created from an internal Vref or provided by any external source (GPIO2 and GPO0). Note that the external Vref signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see Figure 67 to Figure 70.

Input bias current < 1 nA (typ).

PWR UP = 1 => ACMP is powered up.

PWR UP = 0 => ACMP is powered down.

During power-up, the ACMP output will remain LOW, and then becomes valid in 52 µs (max) after power up signal goes high for ACMP0H and ACMP1H, and becomes valid 325 µs (max) after power up signal goes high for ACMP2L and ACMP3L.

Each High Speed ACMP (ACMP0H and ACMP1H) has an optional Rail-to-Rail Input Buffer, which can be used along with the Gain divider to increase ACMP input resistance. However, Input buffer will increase an input offset voltage.

Each cell also has a hysteresis selection, to offer hysteresis of (0, 32, 64, 192) mV. The hysteresis option is available when using an internal Vref only.

The ACMP0H has an additional option of connecting an internal 100 µA current source to its positive input, register [690]. It is also possible to connect the 100 µA current source to each next ACMP via an internal analog MUX.

ACMP0H IN+ options are GPIO4, buffered GPIO4, V_{DD}, 100 µA Current Source

ACMP1H IN+ options are GPIO5, buffered GPIO5, ACMP0H IN+ MUX output

ACMP2L IN+ options are GPIO6, ACMP0H IN+ MUX output, ACMP1H IN+ MUX output

ACMP3L IN+ options are GPIO7, ACMP2L IN+ MUX output, Temp Sensor OUT

9.1 ACMP0H Block Diagram

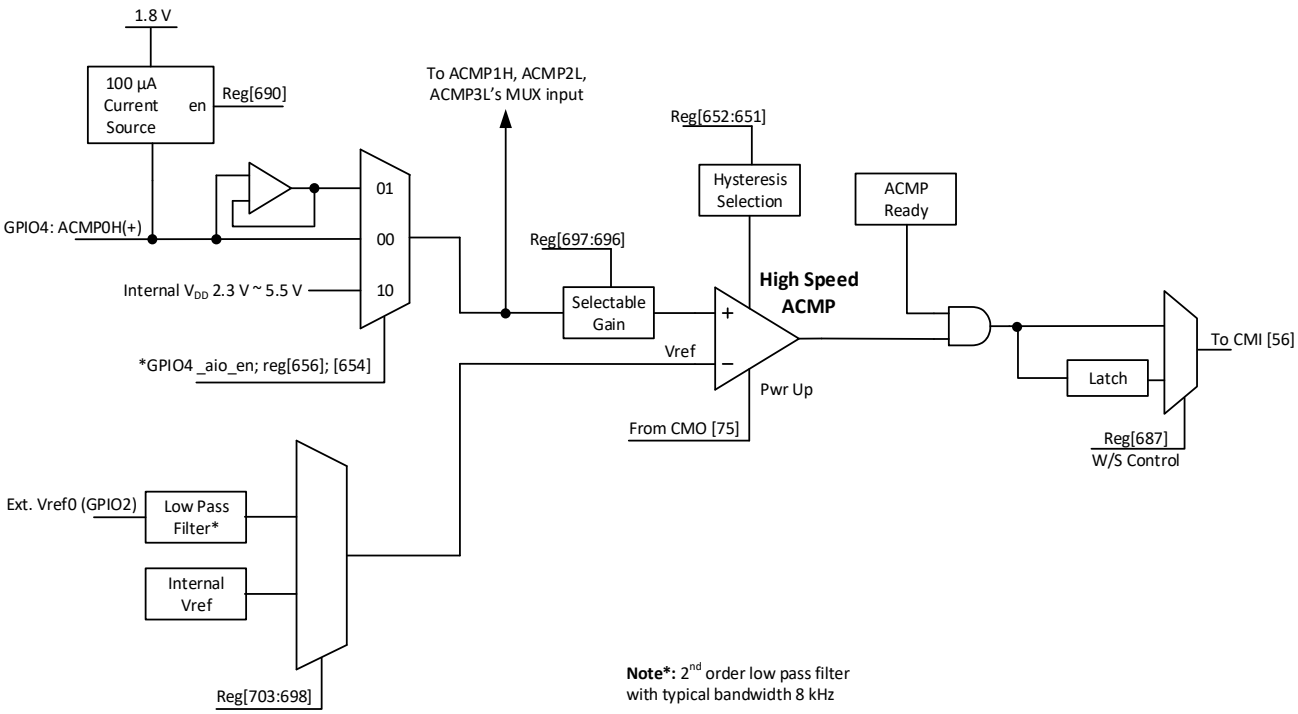


Figure 67. ACMP0H Block Diagram

9.2 ACMP1H Block Diagram

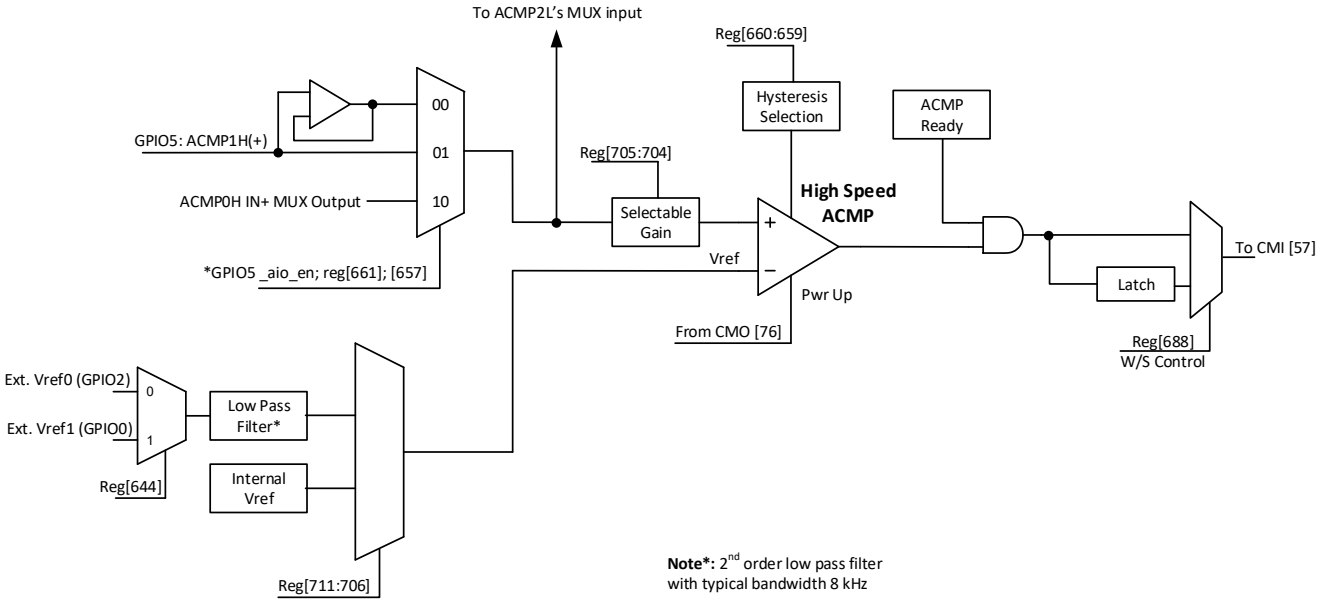


Figure 68. ACMP1H Block Diagram

9.3 ACMP2L Block Diagram

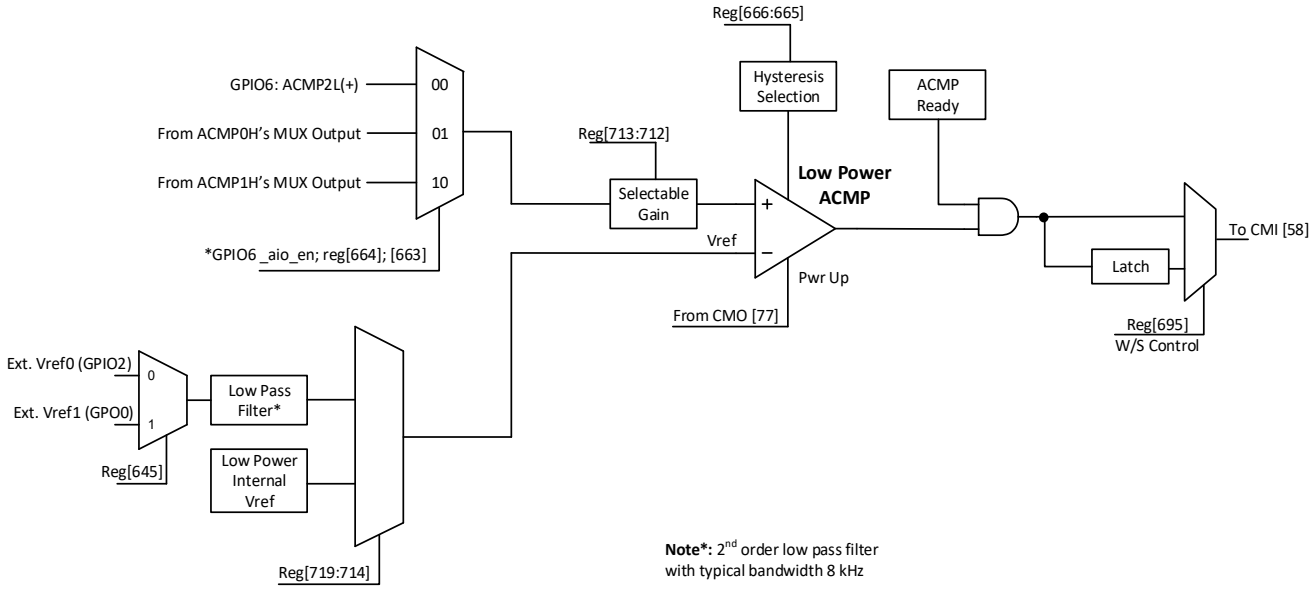


Figure 69. ACMP2L Block Diagram

9.4 ACMP3L Block Diagram

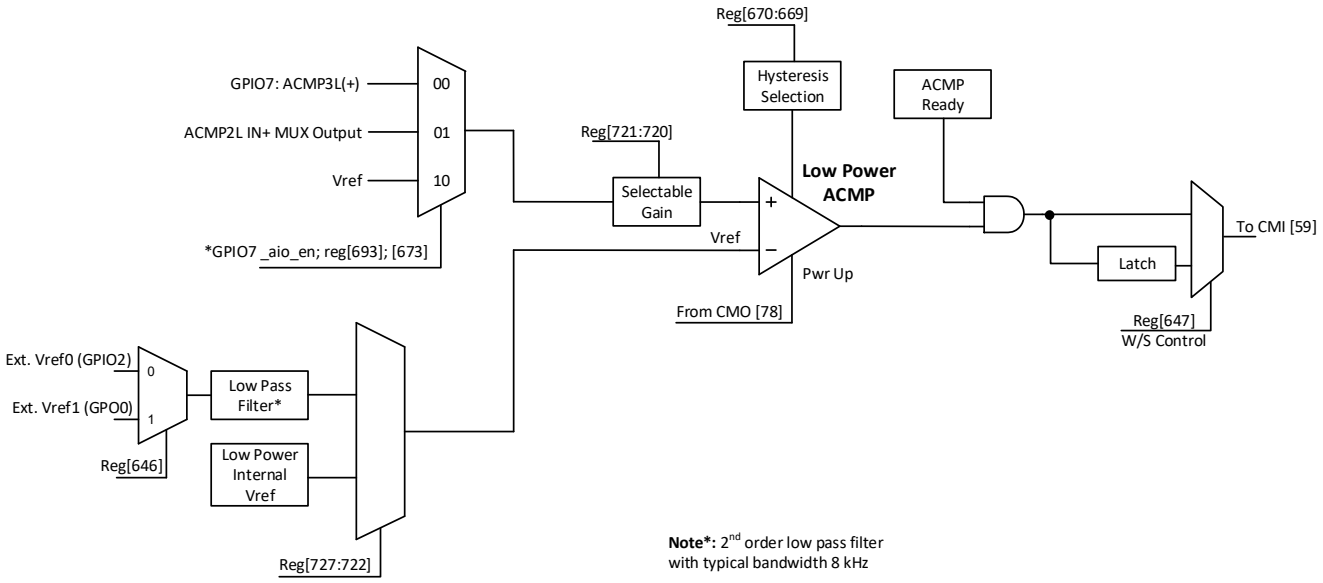


Figure 70. ACMP3L Block Diagram

9.5 ACMP Typical Performance

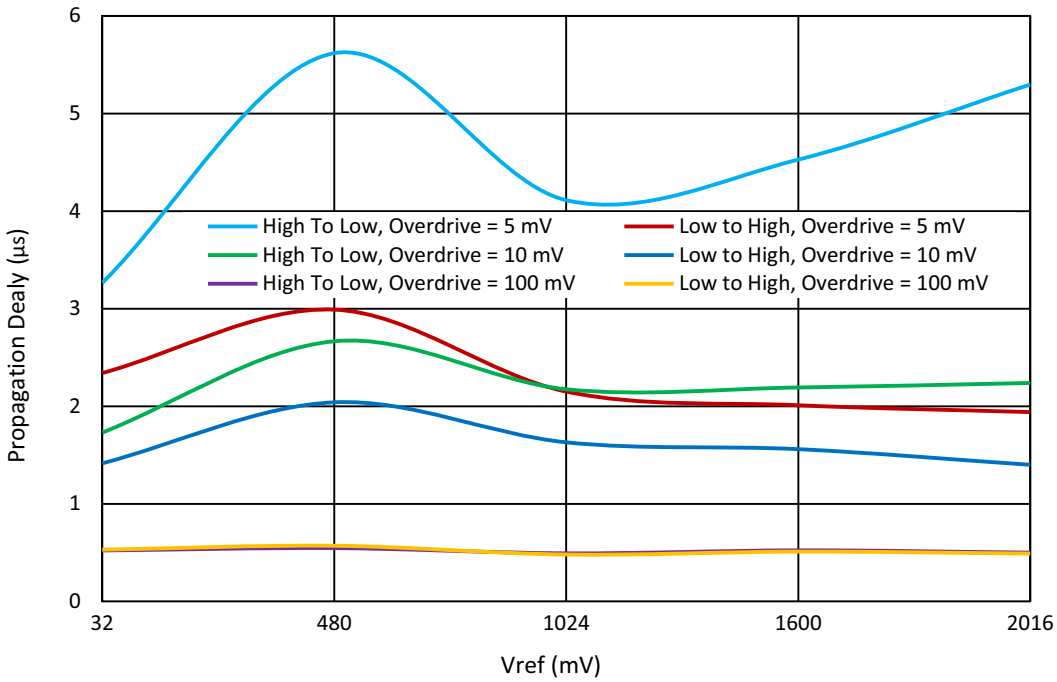


Figure 71. Typical Propagation Delay vs. Vref for ACMPxH at T_A = 25 °C, Gain = 1, Hysteresis = 0

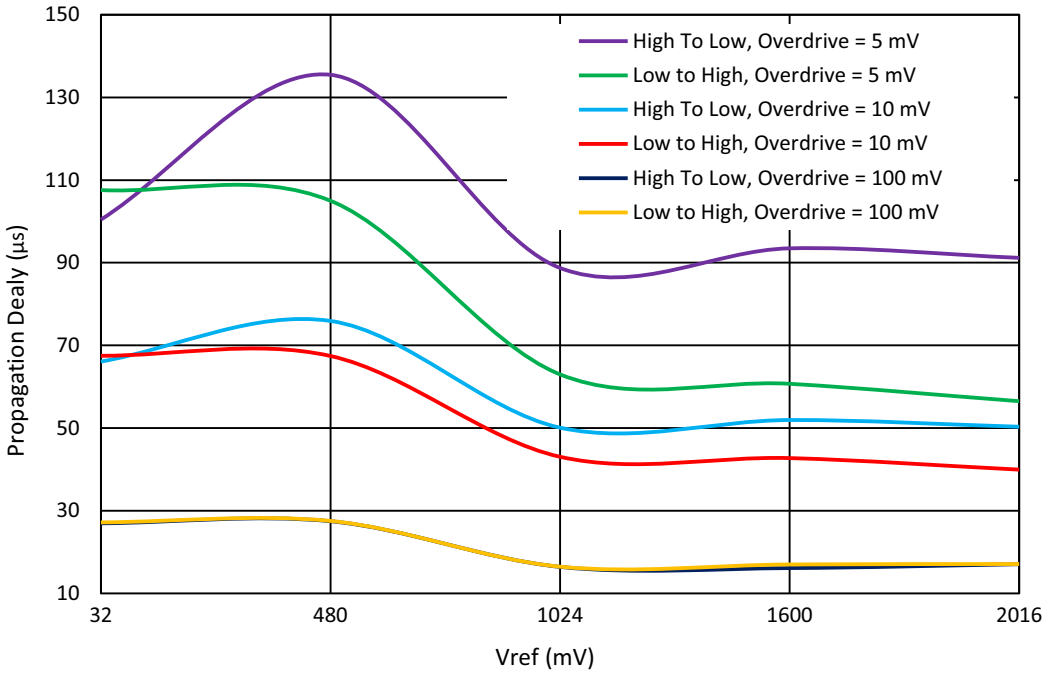


Figure 72. Typical Propagation Delay vs. Vref for ACMPxL at T_A = 25 °C, Gain = 1, Hysteresis = 0

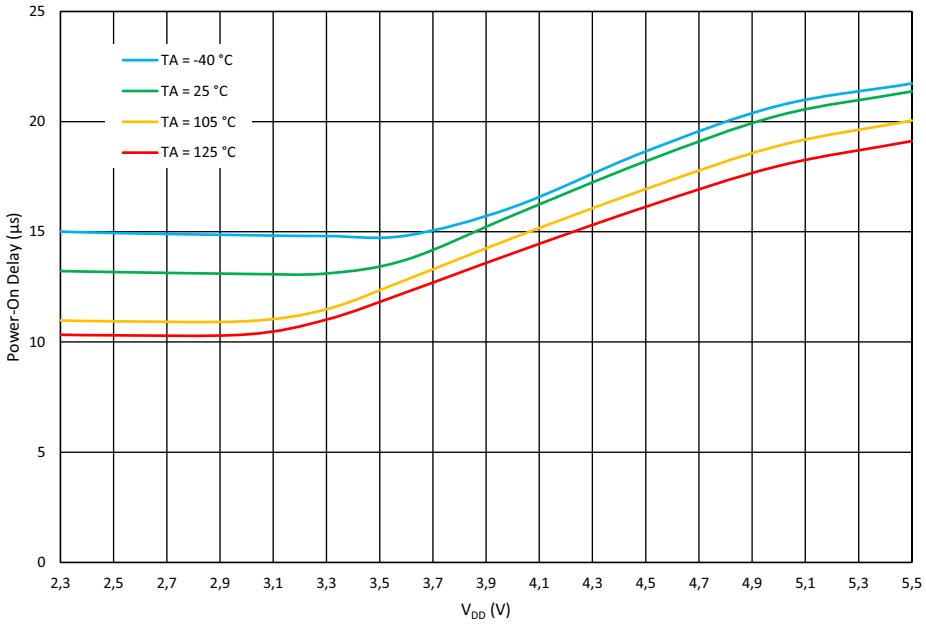


Figure 73. ACMPxH Power-On Delay vs. V_{DD}

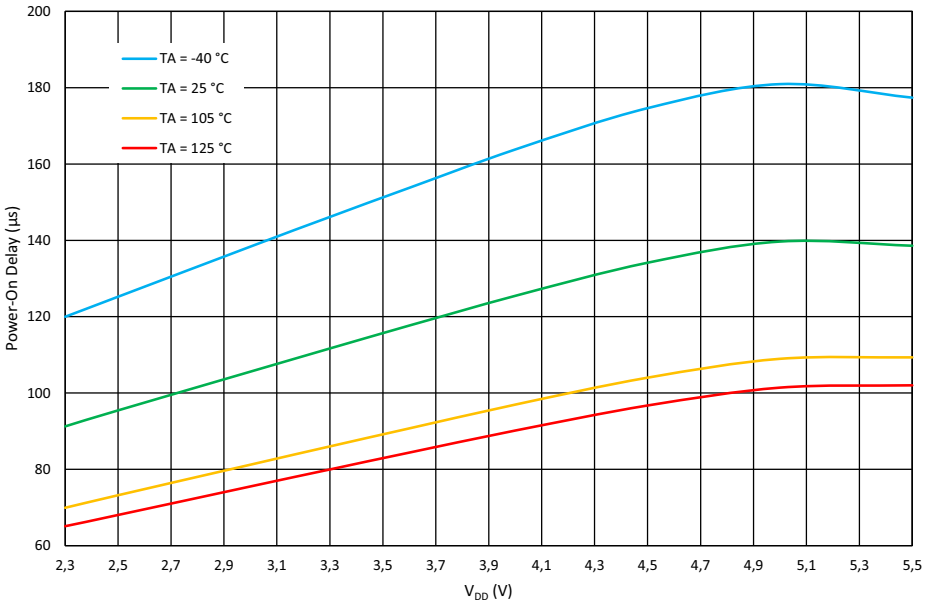


Figure 74. ACMPxL Power-On Delay vs. V_{DD}

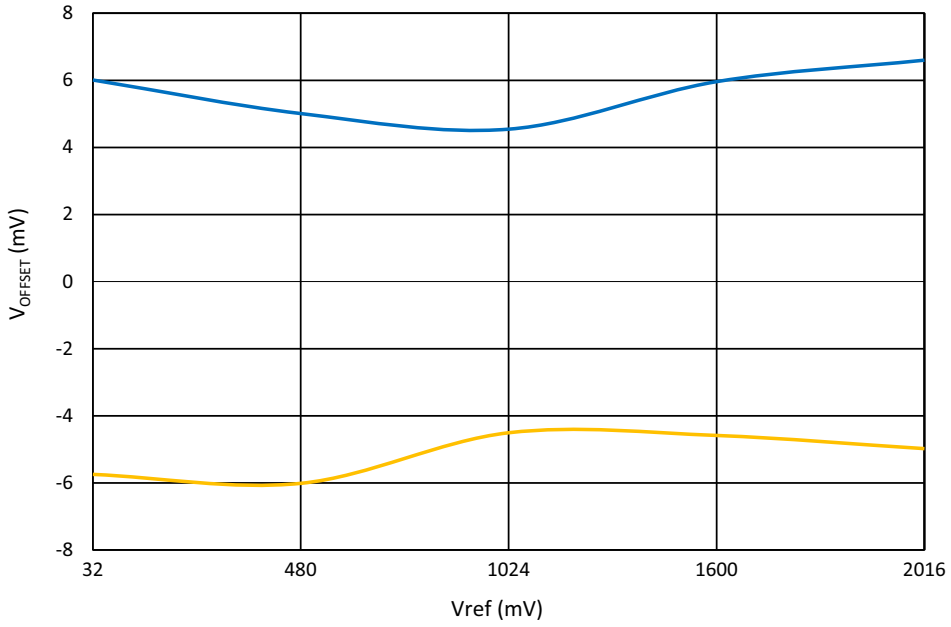


Figure 75. ACMPxH Input Offset Voltage vs. Vref at T_A = -40 °C to 125 °C

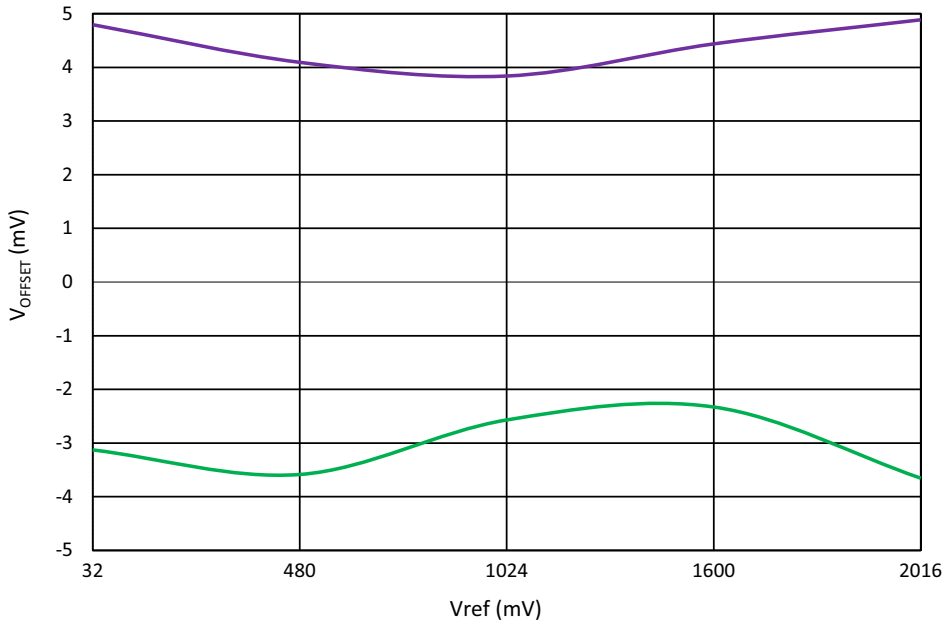


Figure 76. ACMPxH Input Offset Voltage vs. Vref at T_A = -40 °C to 125 °C, Input Buffer Enabled

10. Programmable Delay/Edge Detector

The SLG46857-A has a programmable time delay logic cell that can generate a delay that is selectable from one of four timings (time2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 77 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out. t

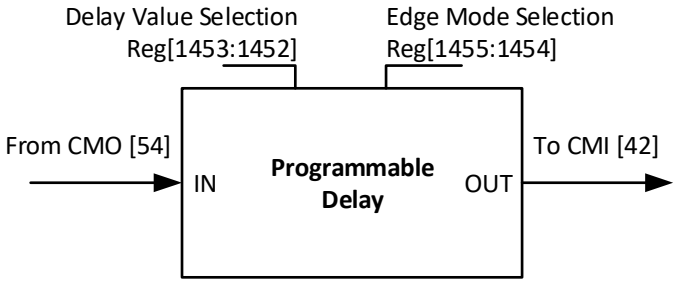


Figure 77. Programmable Delay

10.1 Programmable Delay Timing Diagram - Edge Detector Output

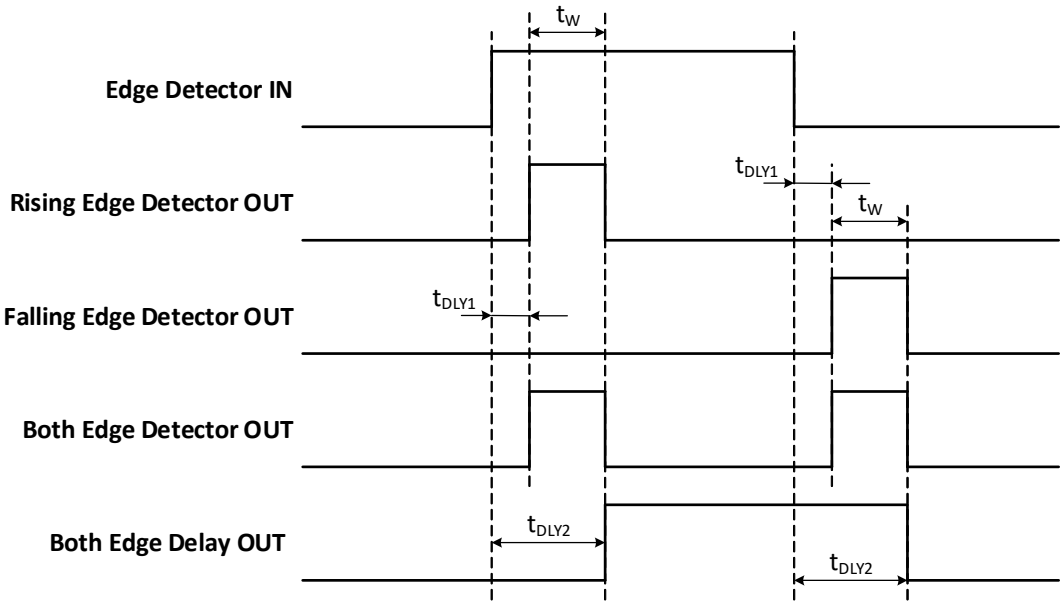


Figure 78. Edge Detector Output

Please refer to Table 13.

11. Additional Logic Function. Deglitch Filter

The SLG46857-A has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay

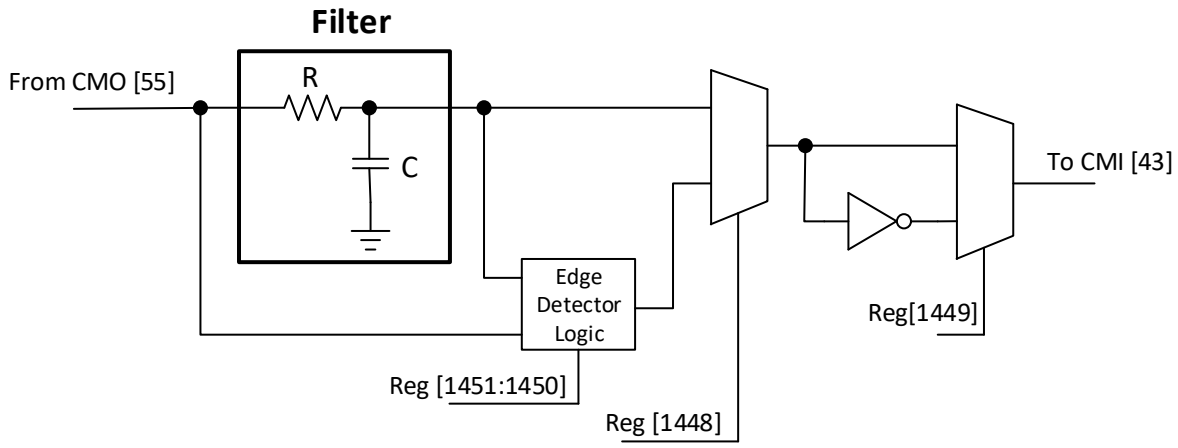


Figure 79. Deglitch Filter/Edge Detector

12. Voltage Reference

12.1 Voltage Reference Overview

The SLG46857-A has a Voltage Reference (Vref) macrocell to provide references to the four analog comparators. This macrocell can supply a user selection of fixed voltage references, or temperature sensor output. The macrocell also has the option to output reference voltages on GPIO8 and GPIO9. See Table 52 for the available selections for each analog comparator.

Also, see Figure 80, which shows the reference output structure.

12.2 Vref Selection Table

Table 52. Vref Selection Table

SEL	Vref	SEL	Vref
0	0.032	32	1.056
1	0.064	33	1.088
2	0.096	34	1.12
3	0.128	35	1.152
4	0.16	36	1.184
5	0.192	37	1.216
6	0.224	38	1.248
7	0.256	39	1.28
8	0.288	40	1.312
9	0.32	41	1.344
10	0.352	42	1.376
11	0.384	43	1.408
12	0.416	44	1.44
13	0.448	45	1.472
14	0.48	46	1.504
15	0.512	47	1.536
16	0.544	48	1.568
17	0.576	49	1.6
18	0.608	50	1.632
19	0.64	51	1.664
20	0.672	52	1.696
21	0.704	53	1.728
22	0.736	54	1.76
23	0.768	55	1.792
24	0.8	56	1.824
25	0.832	57	1.856
26	0.864	58	1.888
27	0.896	59	1.92

Table 52. Vref Selection Table (Cont.)

SEL	Vref	SEL	Vref
28	0.928	60	1.952
29	0.96	61	1.984
30	0.992	62	2.016
31	1.024	63	External

12.3 Vref Block Diagram

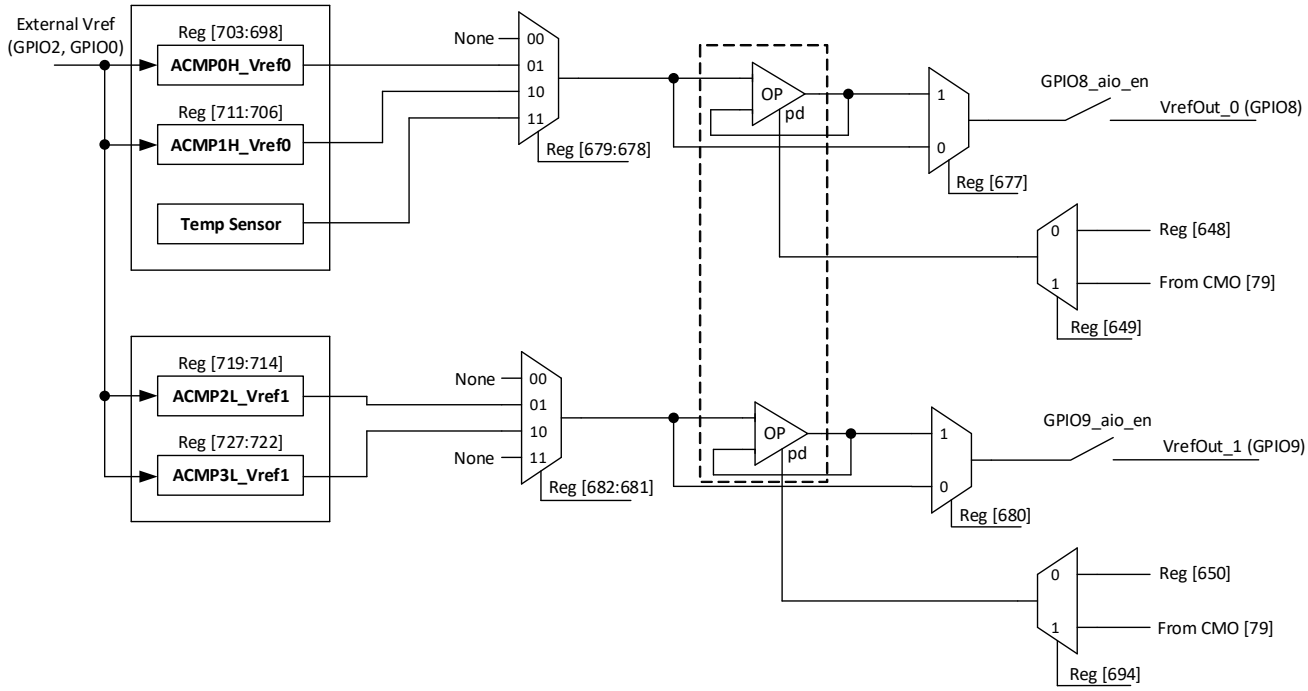


Figure 80. Voltage Reference Block Diagram

12.4 Vref Load Regulation

Note 1: It is not recommended to use Vref connected to external pin without buffer.

Note 2: Vref buffer performance is not guaranteed at V_{DD} < 2.7 V.

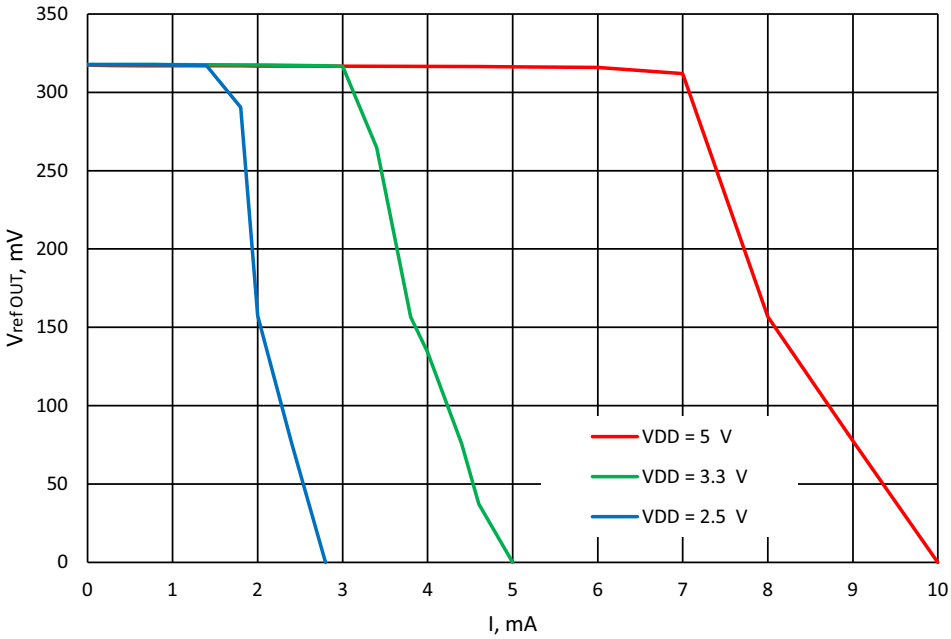


Figure 81. Typical Load Regulation, Vref = 320 mV, T_A = -40 °C to +125 °C, Buffer - Enabled

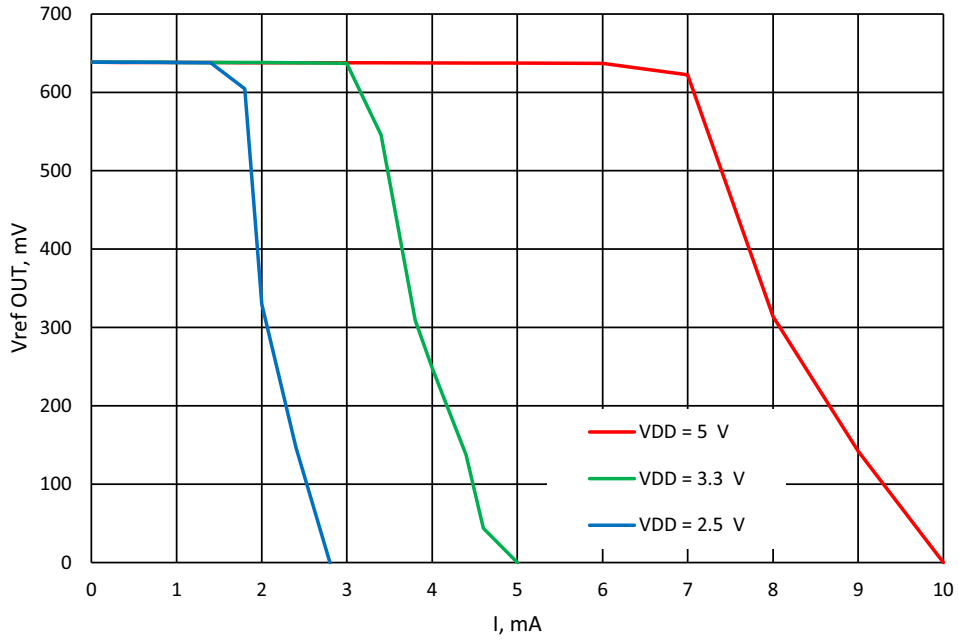


Figure 82. Typical Load Regulation, Vref = 640 mV, T_A = -40 °C to +125 °C, Buffer - Enabled

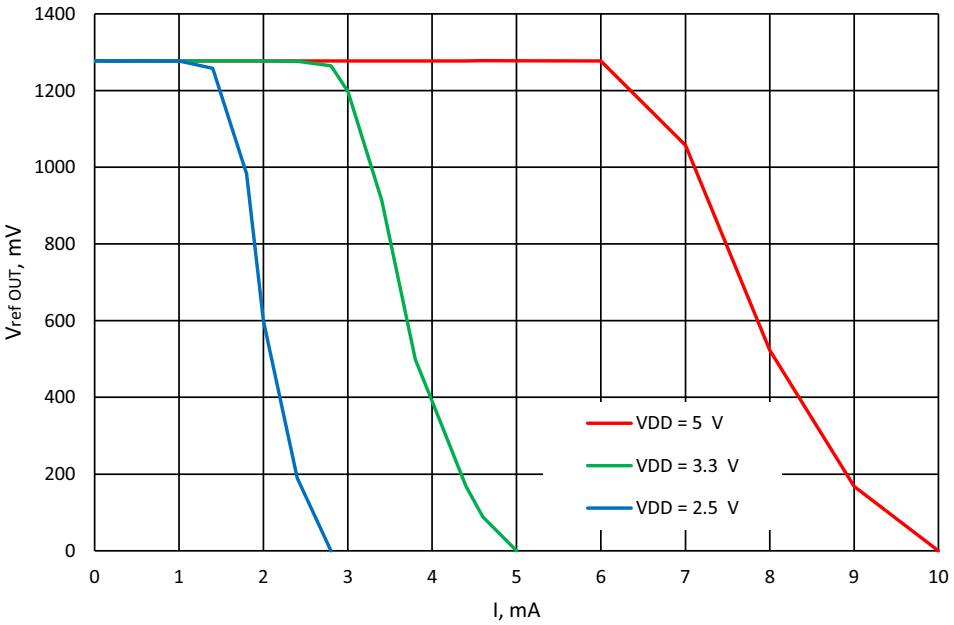


Figure 83. Typical Load Regulation, Vref = 1280 mV, T_A = -40 °C to +125 °C, Buffer - Enabled

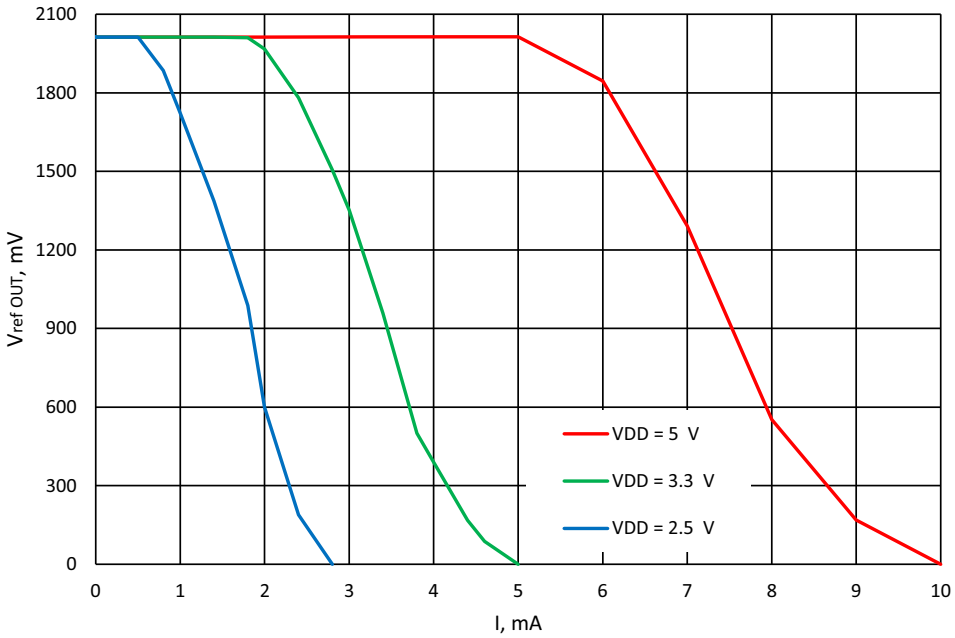


Figure 84. Typical Load Regulation, Vref = 2016 mV, T_A = -40 °C to +125 °C, Buffer - Enabled

13. Clocking

13.1 OSC General Description

The SLG46857-A has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that gives the user flexibility for introducing clock signals to connection matrix, as well as various other macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4 or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24 or /64 on Connection Matrix Input lines [53], [54], and [55]. Please see Figure 88 for more details on the SLG46857-A clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [749]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-Down/Force-On function allows switching off or force on the oscillator using an external pin. The Matrix Power-Down/Force-On (Connection Matrix Output [80], [81], [82]) signal has the highest priority. The OSC operates according to the following table:

Table 53. Oscillator Operation Mode Configuration Settings

POR	External Clock selection	Signal from Connection matrix	Register: Power-Down or Force On by matrix input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY macrocells	OSC operation mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

[1] The OSC will run only when any macrocell that uses OSC is powered on.

13.2 Oscillator0 (2.048 kHz)

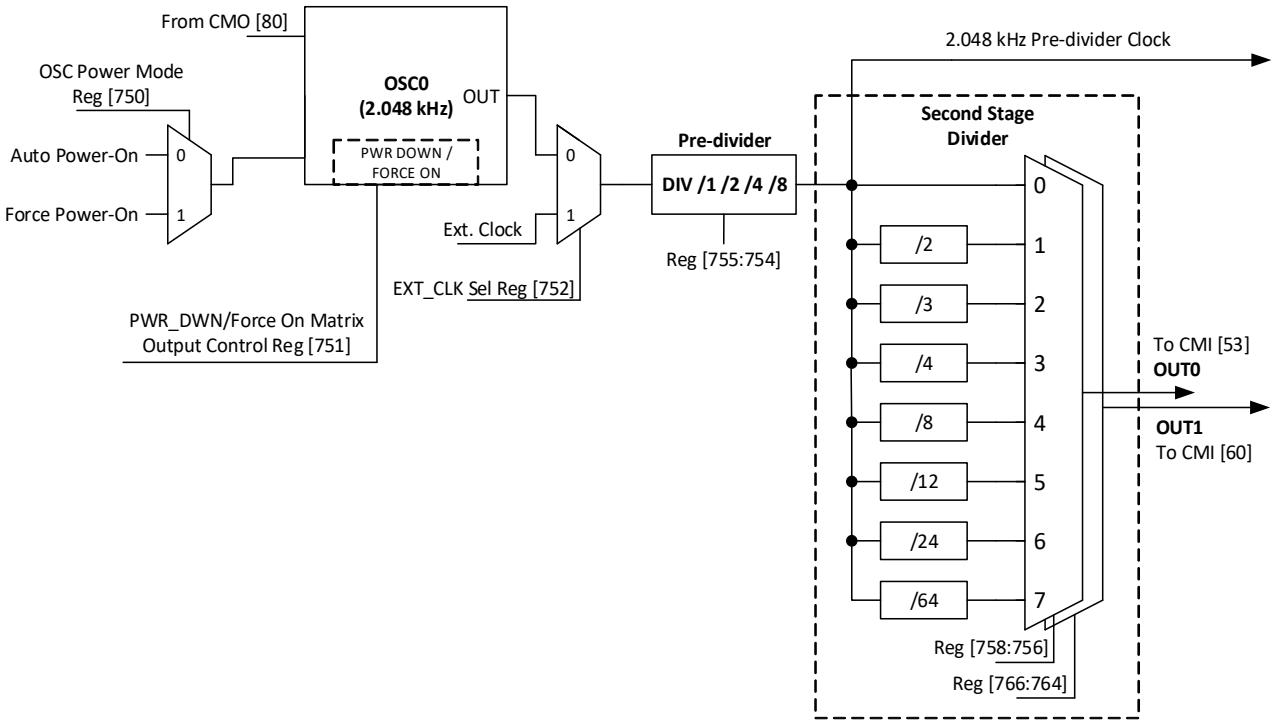


Figure 85. Oscillator0 Block Diagram

13.3 Oscillator1 (2.048 MHz)

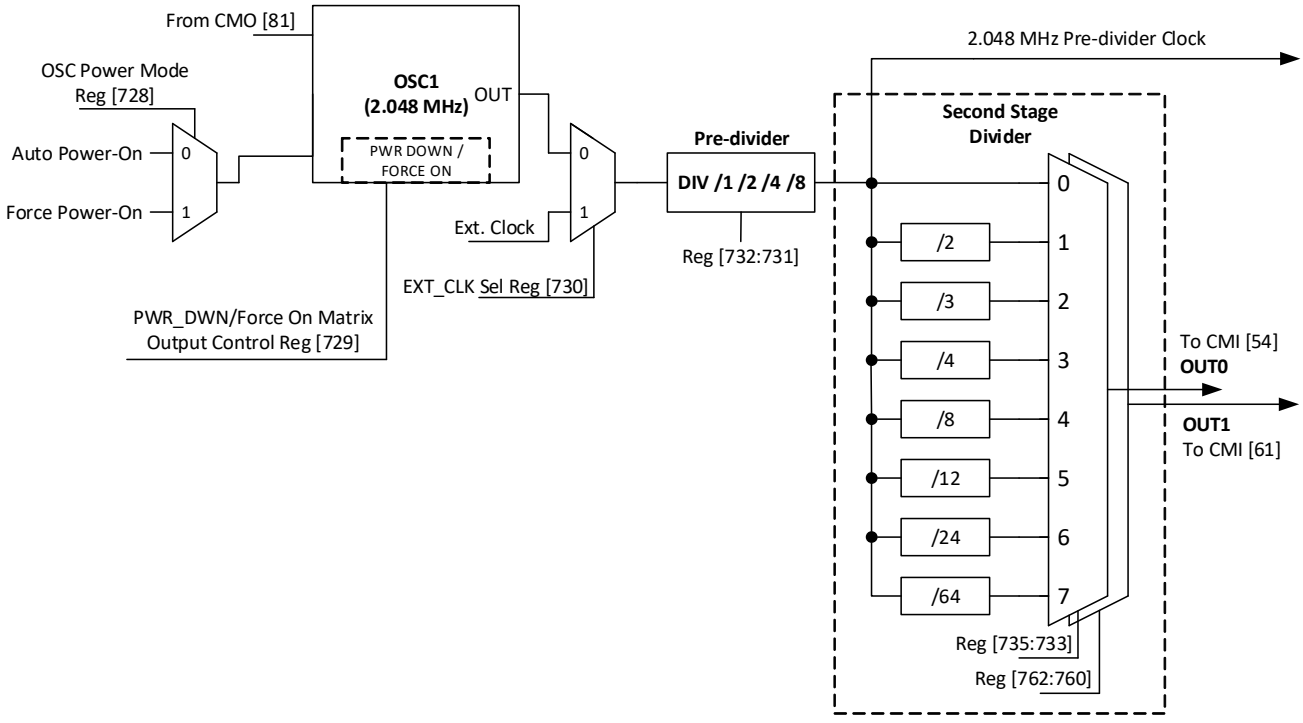


Figure 86. Oscillator1 Block Diagram

13.4 Oscillator2 (25 MHz)

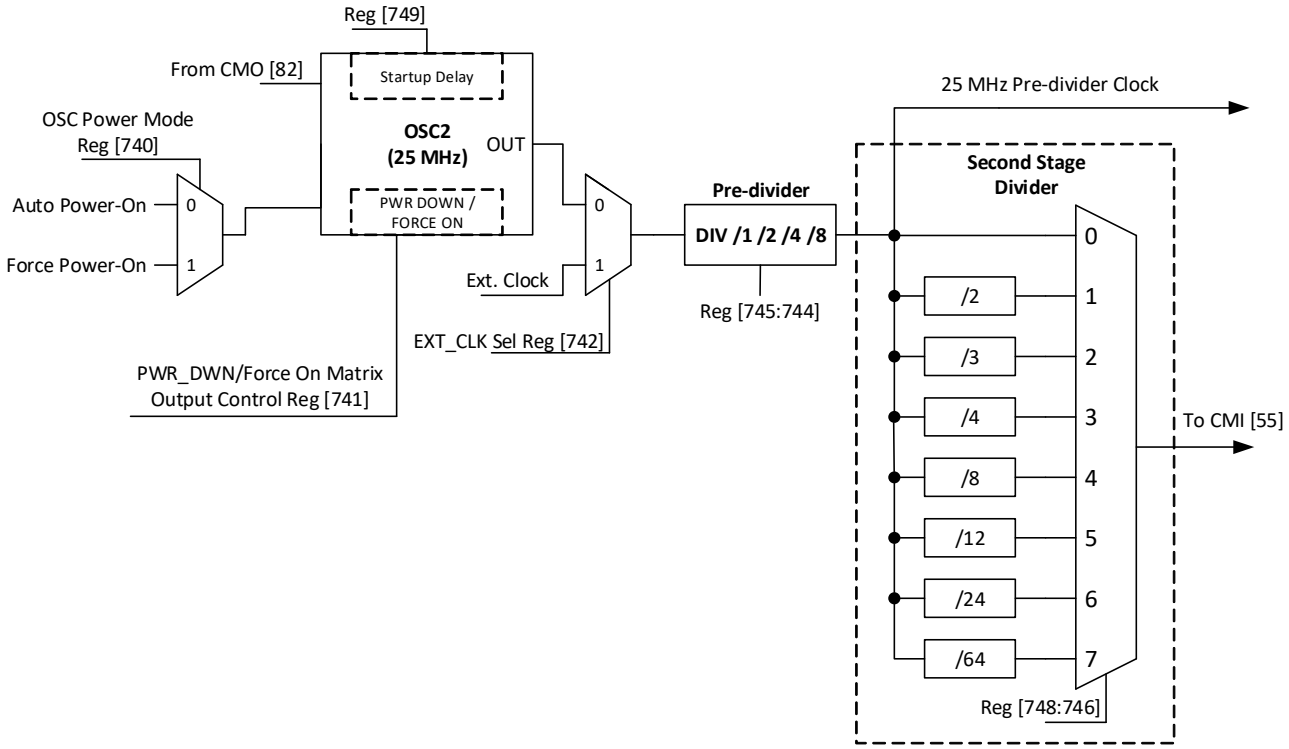


Figure 87. Oscillator2 Block Diagram

13.5 CNT/DLY Clock Scheme

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

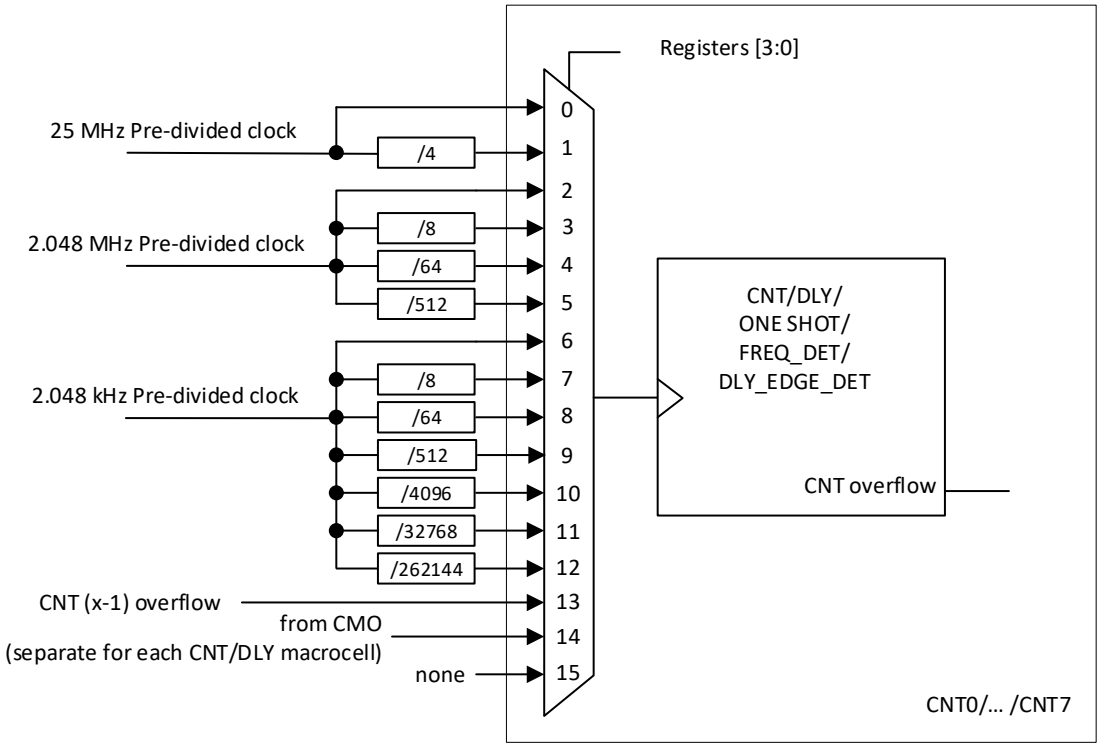


Figure 88. Clock Scheme

13.6 External Clocking

The SLG46857-A supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

13.6.1 GPI0 Source for Oscillator0 (2.048 kHz)

When register [752] is set to 1, an external clocking signal on GPI0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 85. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.6.2 GPIO2 Source for Oscillator1 (2.048 MHz)

When register [730] is set to 1, an external clocking signal on GPIO2 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 86. The low and high limits for external frequency that can be selected are 0 MHz and 10 MHz.

13.6.3 GPIO8 Source for Oscillator2 (25 MHz)

When register [742] is set to 1, an external clocking signal on GPIO8 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 87. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.3 V, 30 MHz at V_{DD} = 3.3 V, 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the GPIO8 input signal.

13.7 Oscillators Power-On Delay

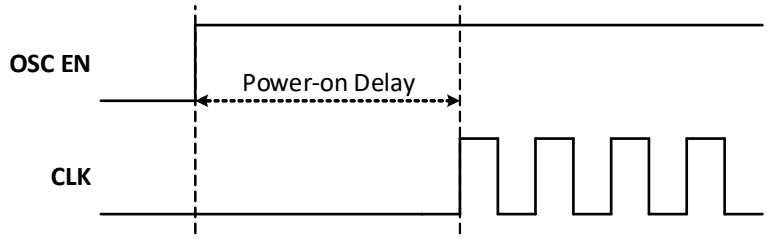


Figure 89. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.

Note 2: OSC enable” signal appears when any macrocell that uses OSC is powered on.

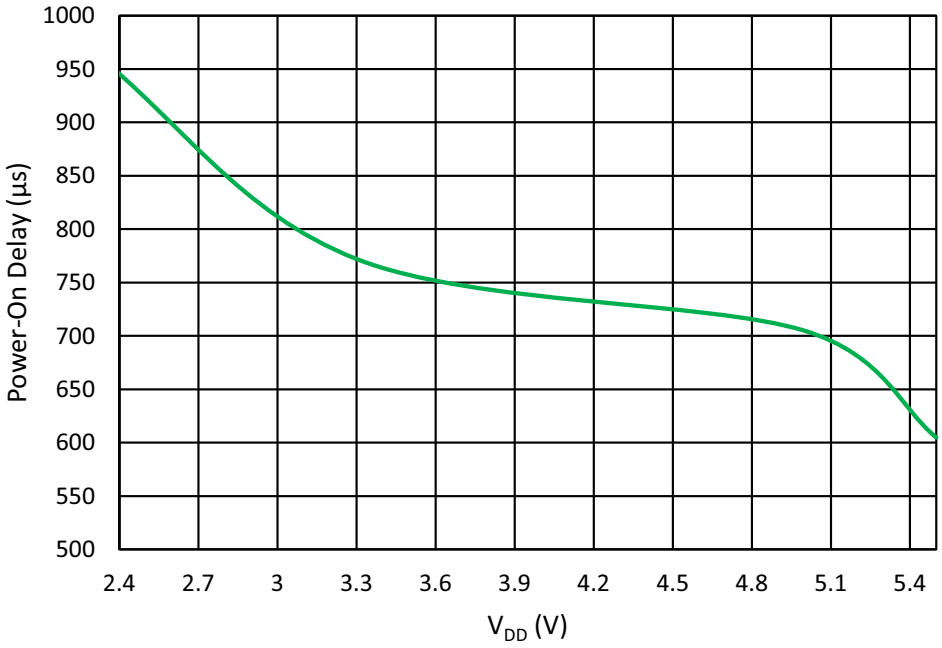


Figure 90. Oscillator0 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC0 = 2.048 kHz

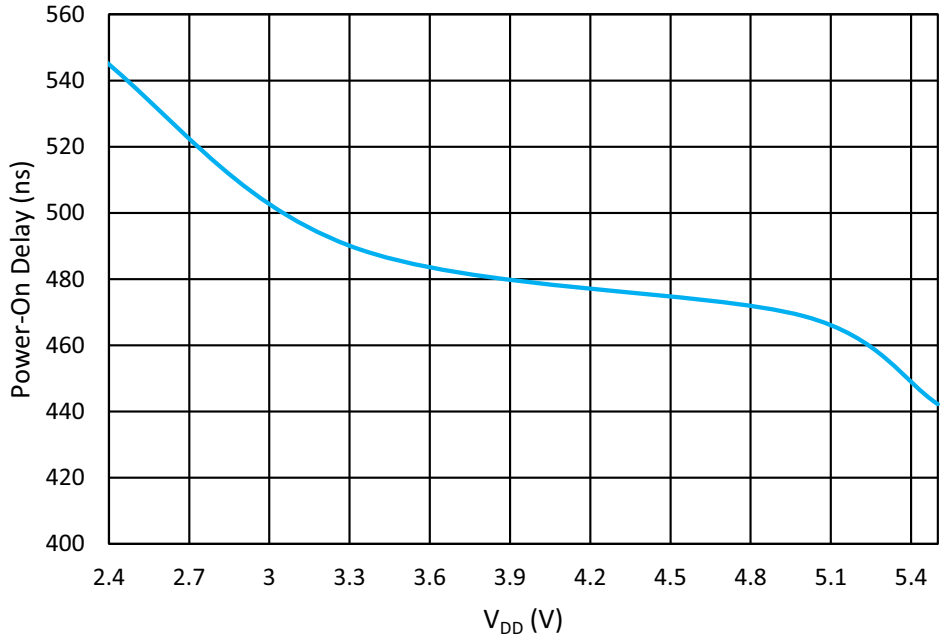


Figure 91. Oscillator1 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC1 = 2.048 MHz

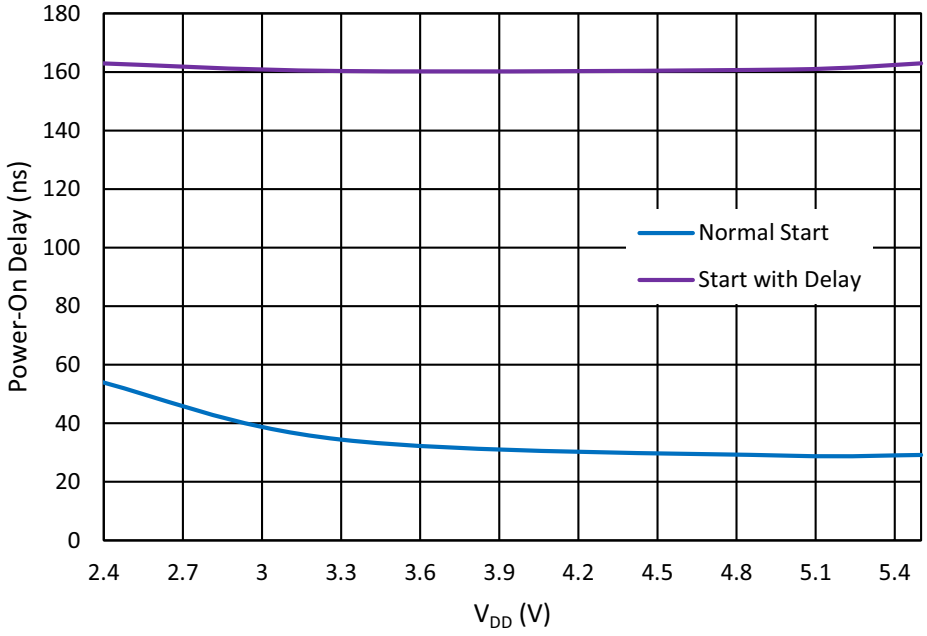


Figure 92. Oscillator1 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC1 = 2.048 MHz

13.8 Oscillators Accuracy

Note 1: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

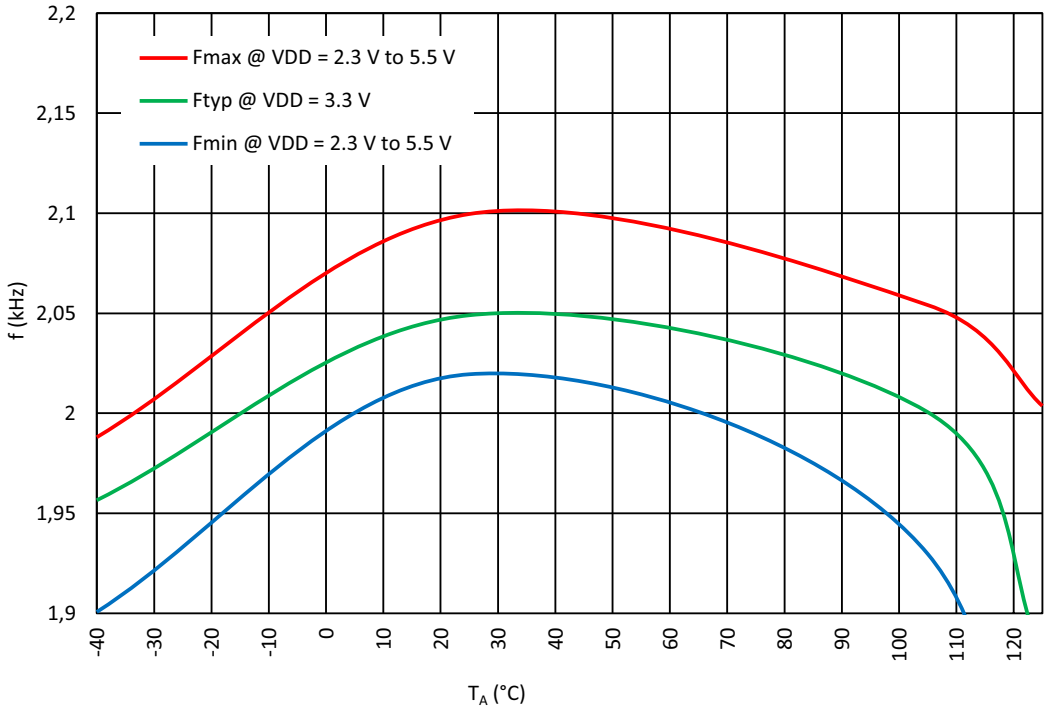


Figure 93. Oscillator0 Frequency vs. Temperature, OSC0 = 2.048 kHz

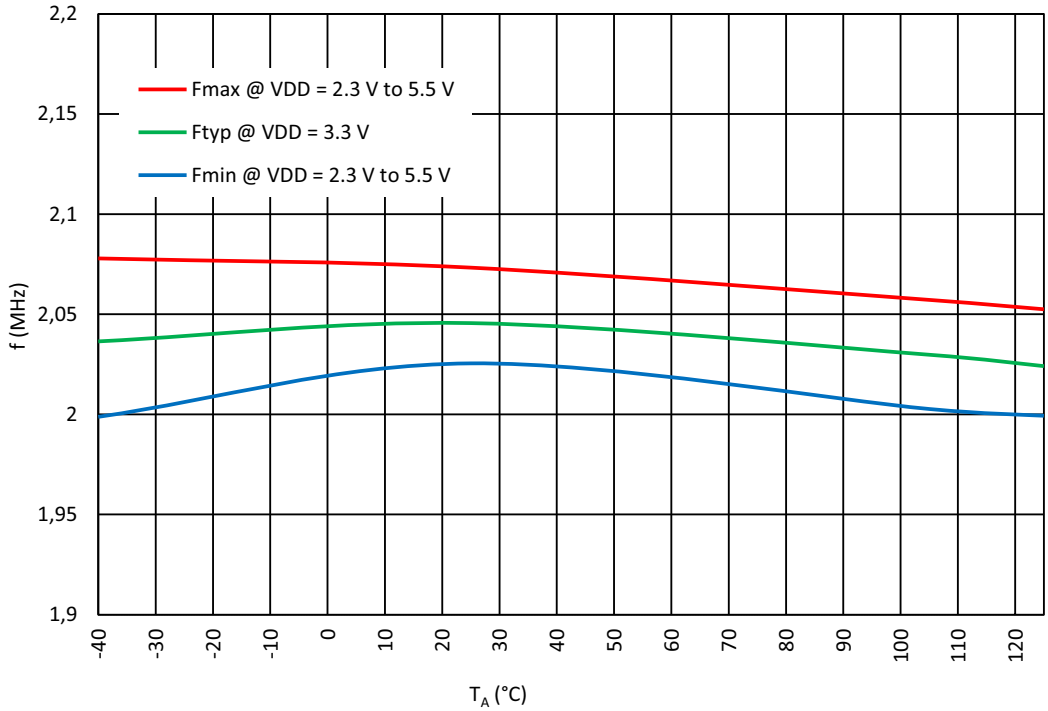


Figure 94. Oscillator1 Frequency vs. Temperature, OSC1 = 2.048 MHz

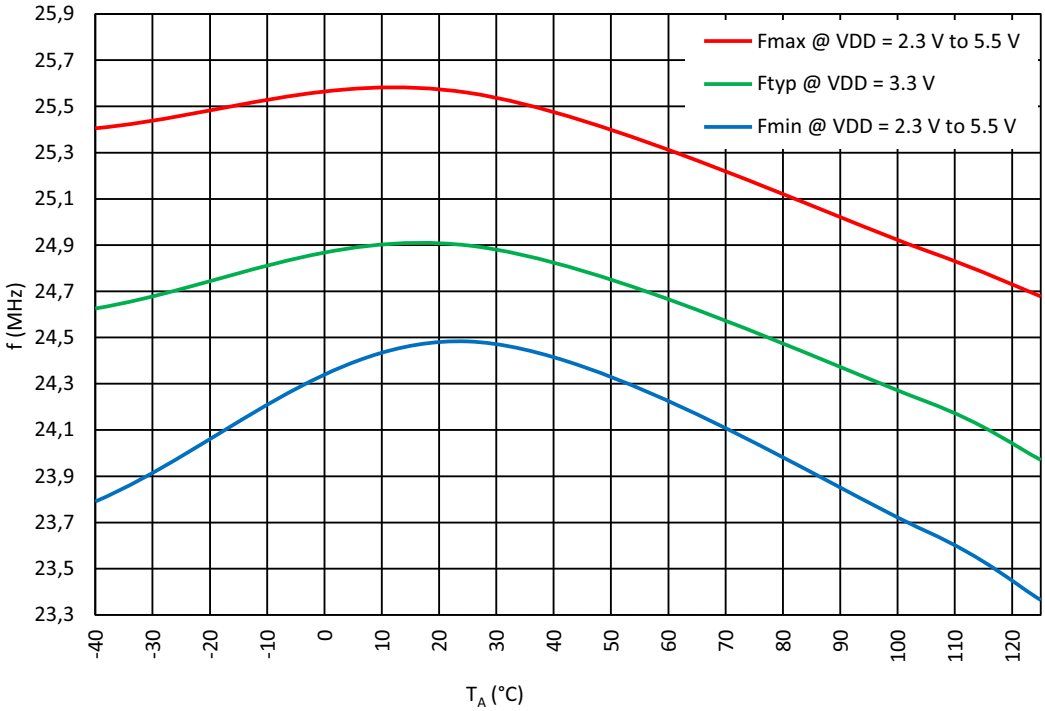


Figure 95. Oscillator2 Frequency vs. Temperature, OSC1 = 25 MHz

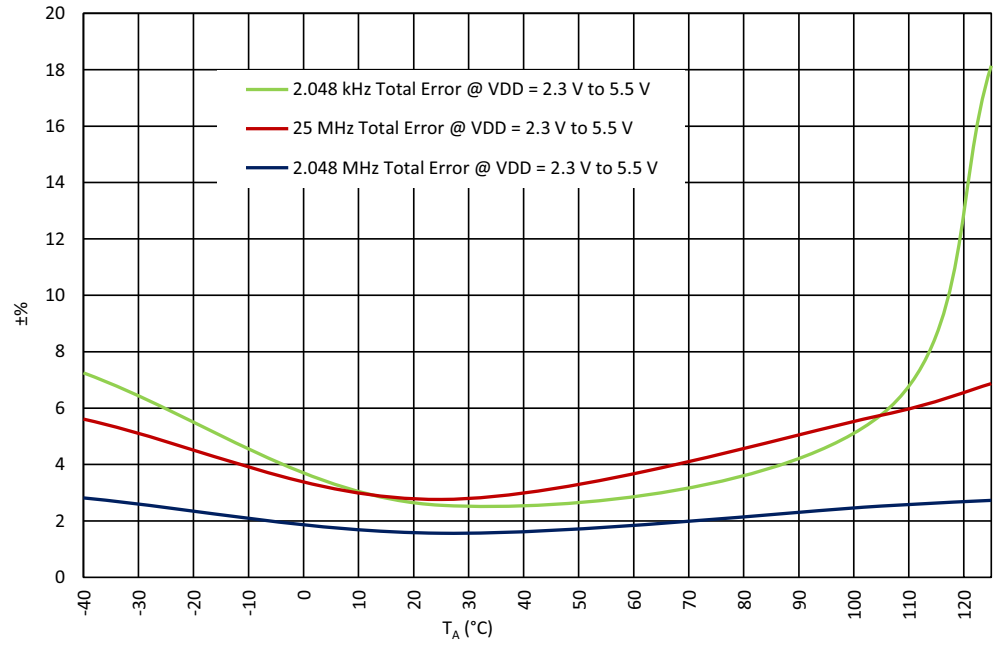


Figure 96. Oscillators Total error vs. Temperature

Note 2: For more information see section 3.9 Oscillator Specifications.

13.9 Oscillators Settling Time

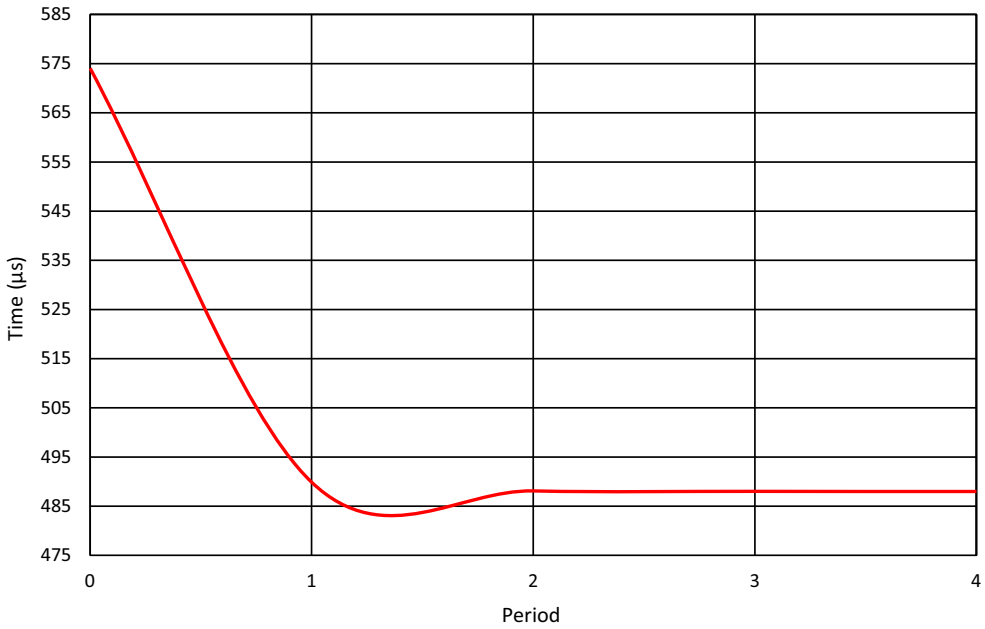


Figure 97. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC0 = 2.048 kHz

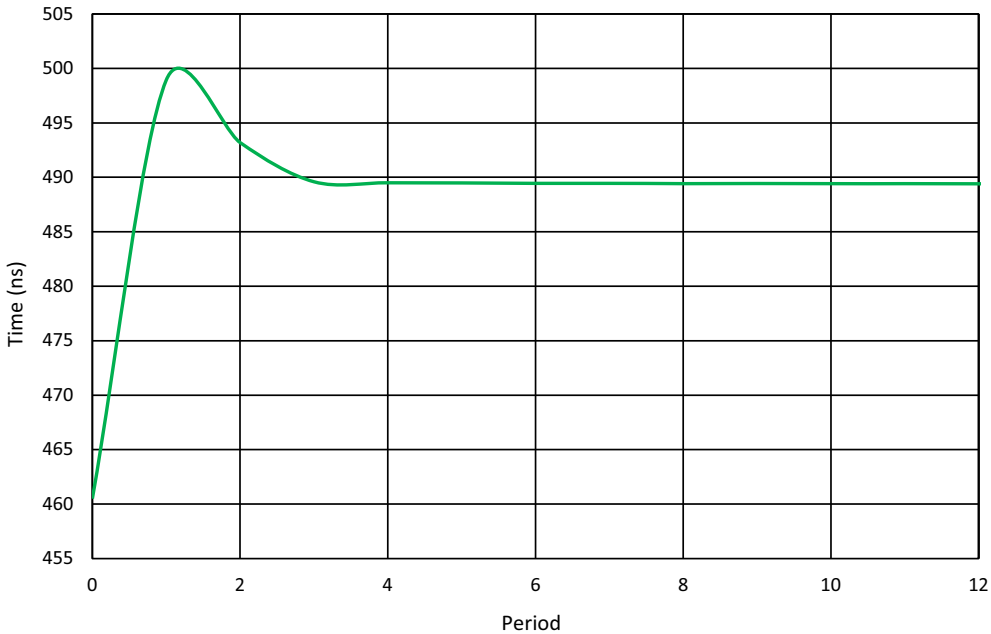


Figure 98. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC1 = 2.048 MHz

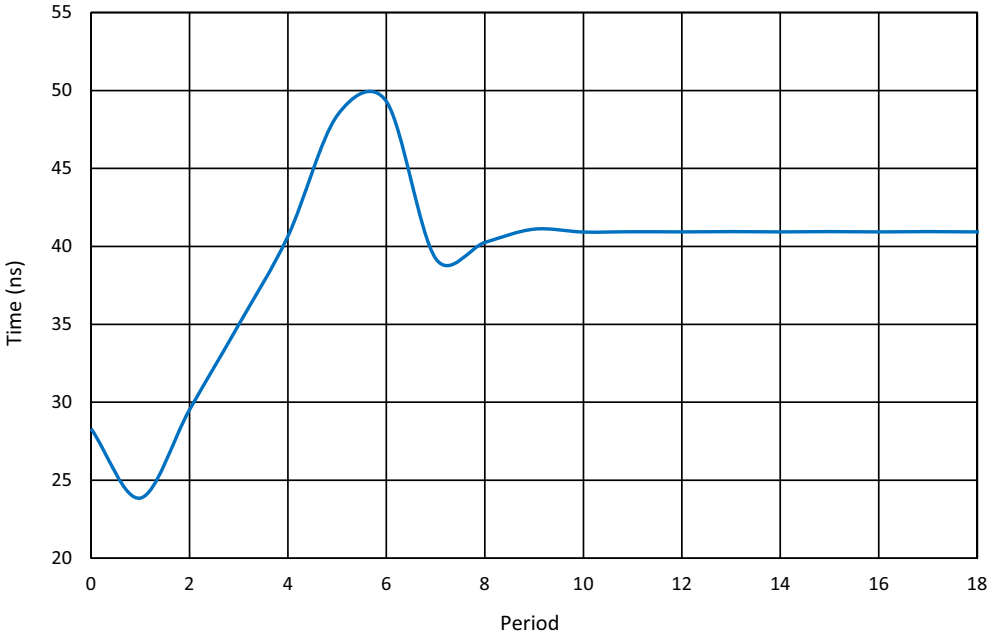


Figure 99. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Normal Start)

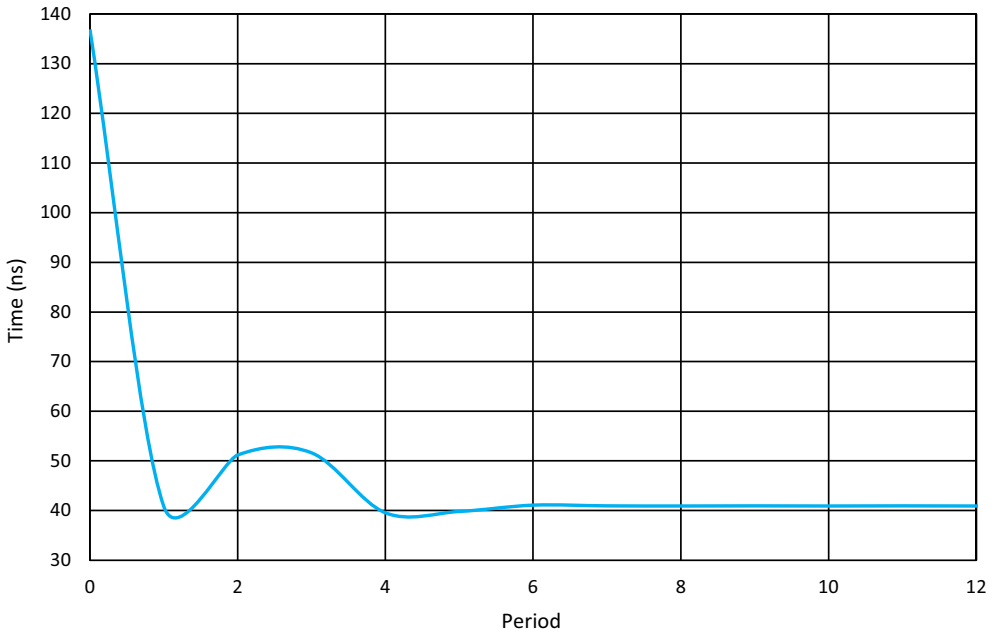


Figure 100. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Start with Delay)

14. Power-On Reset

The SLG46857-A has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

14.1 General Operation

The SLG46857-A is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on Pin 1) is less than Power-Off Threshold (see in Table 7), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher **(Note 1)** than the V_{DD} voltage is applied to any other Pin. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other pin is incorrect, and can lead to incorrect or unexpected device behavior.

Note 1: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG46857-A, the voltage applied on the V_{DD} should be higher than the Power-On Threshold **(Note 2)**. The full operational V_{DD} range for the SLG46857-A is 2.3 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On threshold. After the POR sequence is started, the SLG46857-A will have a typical period of time to go through all the steps in the sequence (noted in the datasheet for that device) and will be ready and completely operational after the POR sequence is complete.

Note 2: The Power-On Threshold is defined in Table 7.

To power down the chip the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down it should be less than Power-Off threshold.

All Pins are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before the voltage on Pins can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

14.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 101.

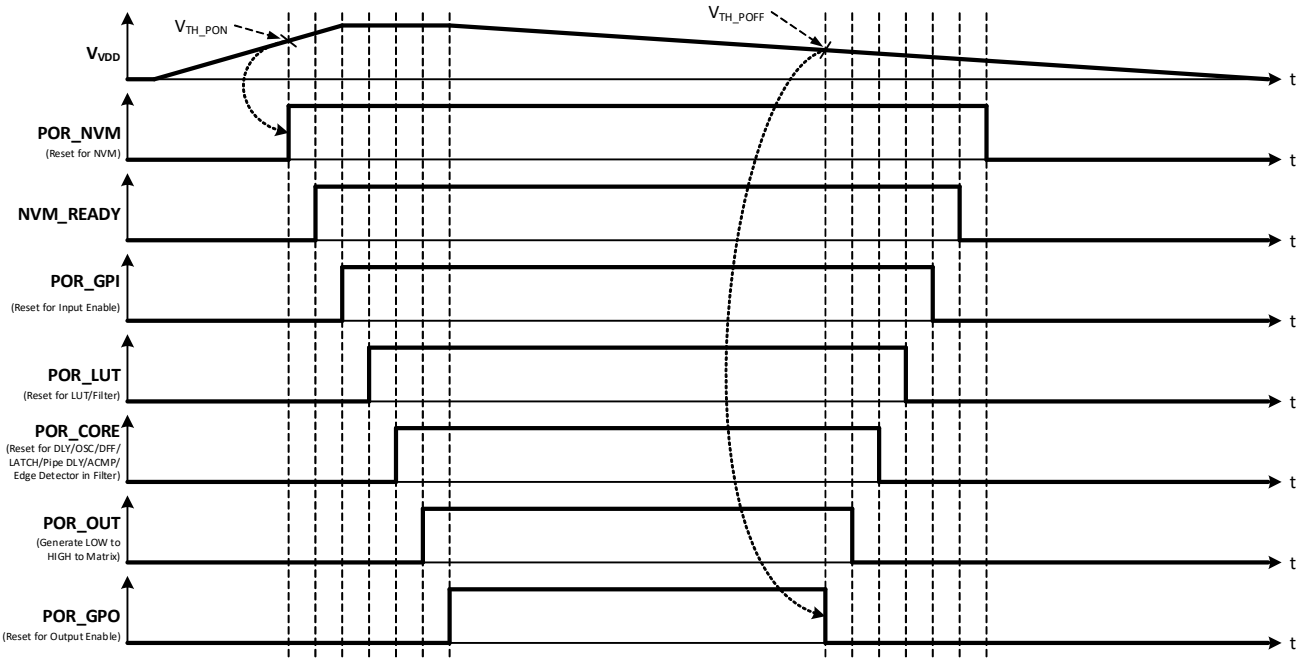


Figure 101. POR Sequence

As can be seen from Figure 101 after the V_{DD} has start ramping up and crosses the Power-On threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM, and transfers this information to a CMOS LATCH that serves to configure each macrocell, and the Connection Matrix which routes signals between macrocells. The third stage causes the reset of the input pins, and then to enable them. After that, the LUTs are reset and become active. After LUTs the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized internal POR signal (POR macrocell output) goes from LOW to HIGH. The last portion of the device to be initialized are the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

14.3 Macrocells Output States during POR Sequence

To have a full picture of SLG46857-A operation during powering and POR sequence, review the overview the macrocell output states during the POR sequence (Figure 102 describes the output signals states).

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; LUTs also output LOW. Only P_DLY macrocell configured as edge detector becomes active at this time. After that input pins are enabled.

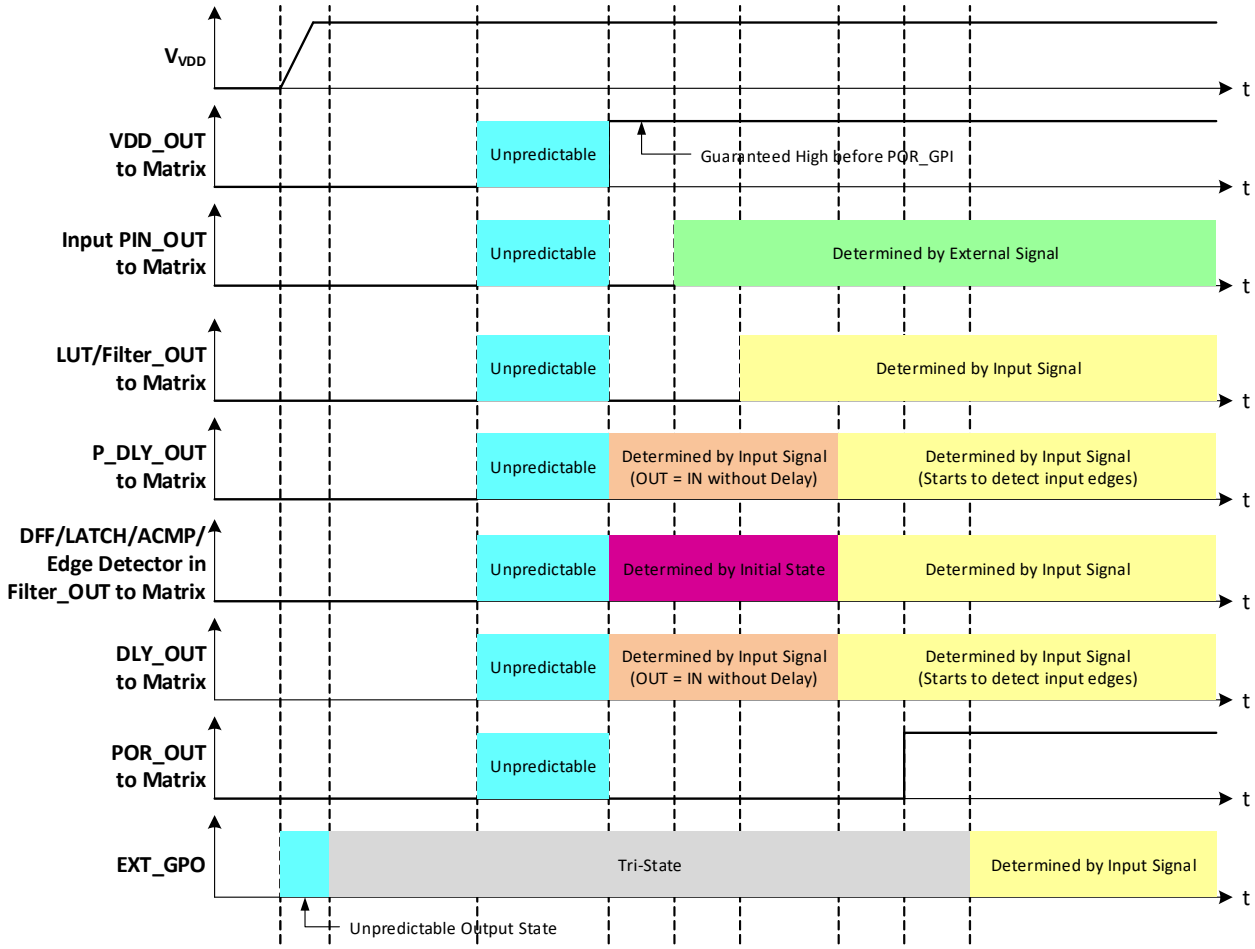


Figure 102. Internal Macrocell States during POR Sequence

14.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.56 V to 2.03 V, macrocells in SLG46857-A are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, ACMP, Pull-up/down.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 ms to 5 ms. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. So, if the input signal applied to pin is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will

be pulled up, following the voltage on the input pin.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

14.3.2 Power-Down

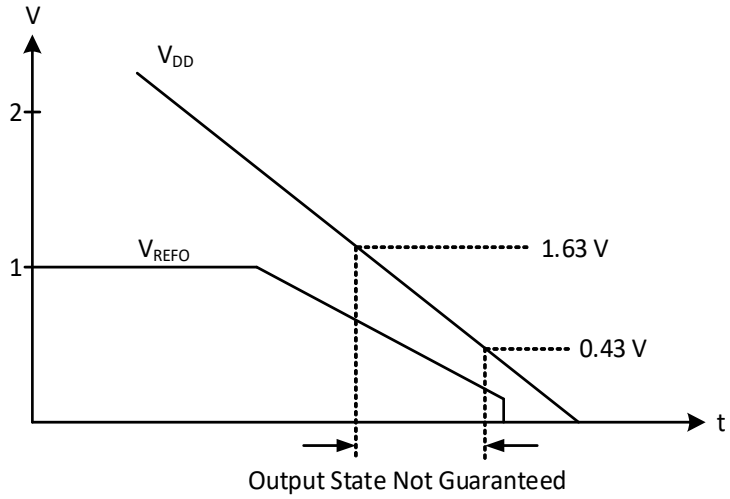


Figure 103. Power-Down

During Power-down, macrocells in SLG46857-A are powered off after V_{DD} falling down below Power-Off Threshold. Please note that during a slow rampdown, outputs can possibly switch state during this time.

15. I²C Serial Communications Macrocell

15.1 I²C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I²C Serial Communications Macrocell in this device allows an I²C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

An I²C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving an I²C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1967:1965]. See Section 15.5 I2C Serial Command Register Map for more details on I²C read/write memory protection.

15.2 I²C Serial Communications Device Addressing

Each command to the I²C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 104. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by GPI0, GPIO2, GPIO4, and GPIO5. The LSB of the control code is defined by the value of GPI0, while the MSB is defined by the value of GPIO5. The address source (either register bit or PIN) for each bit in the control code is defined by registers [2027:2024]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I²C bus. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I²C-bus specification and user manual, there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I²C-bus specification and user manual to understand the addressing and implementation of these special functions, to insure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. Of this 2K byte address space, the valid addresses accessible to the I²C Macrocell on the SLG46857-A are in the range from 0 (0x00) to 255 (0xFF). The MSB address bits (A10, A9, and A8) will be "0" for all commands to the SLG46857-A.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. Figure 104 shows this basic command structure.

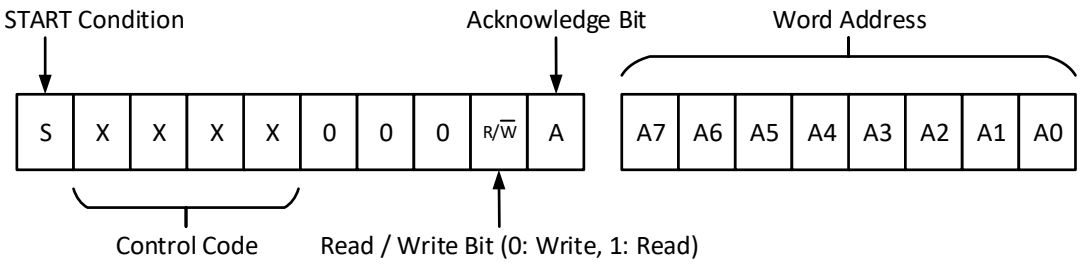


Figure 104. Basic Command Structure

15.3 I²C Serial Communications General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 105. Timing specifications can be found in the AC Characteristics section.

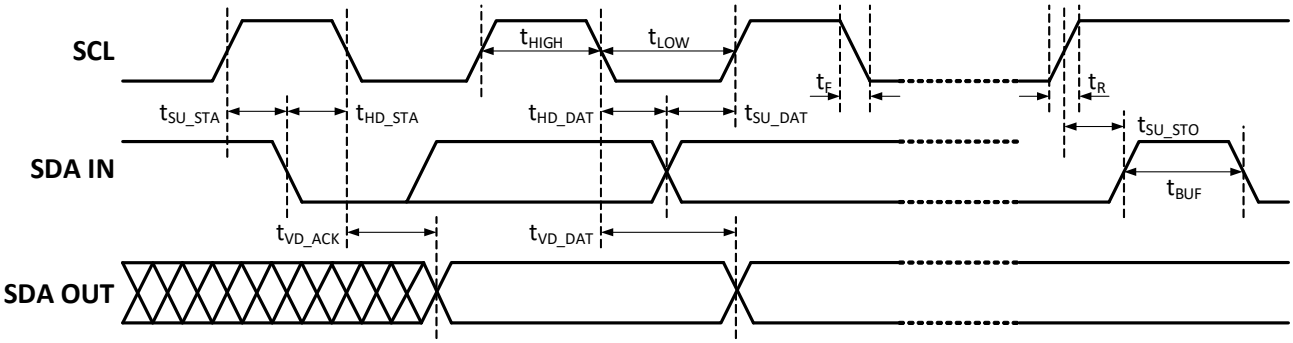


Figure 105. I²C General Timing Characteristics

15.4 I²C Serial Communications Commands

15.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to “0”) are placed onto the I²C bus by the Master. After the SLG46857-A sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG46857-A, where the data byte is to be written. After the SLG46857-A sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG46857-A again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46857-A generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command, register [1961] = 1 - Enable. It means that IOs will remain their state until the write command is done.

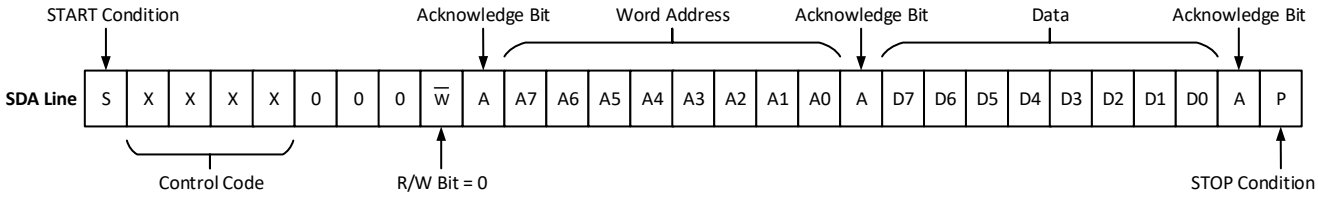


Figure 106. Byte Write Command, R/W = 0

15.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG46857-A in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG46857-A. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG46857-A generates the Acknowledge bit.

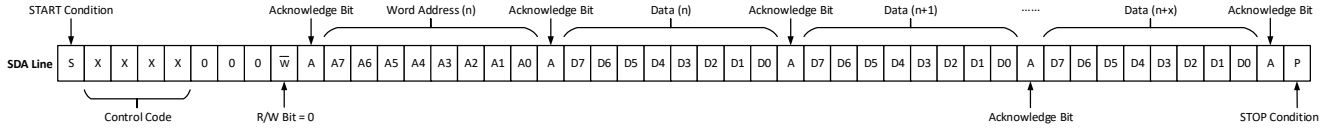


Figure 107. Sequential Write Command

15.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read Command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W bit = “1”. The SLG46857-A will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

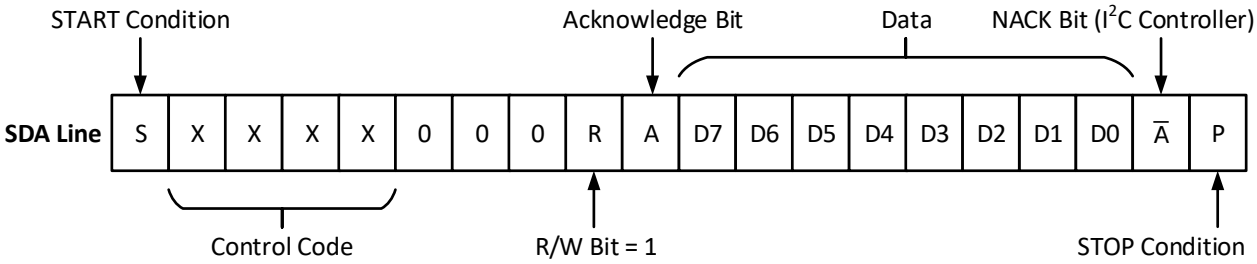


Figure 108. Current Address Read Command, R/W = 1

15.4.4 Random Read Command

The Random Read Command starts with a Control Byte (with R/W bit set to “0”, indicating a Write Command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command.

After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46857-A issues an Acknowledge bit, followed by the requested eight data bits.

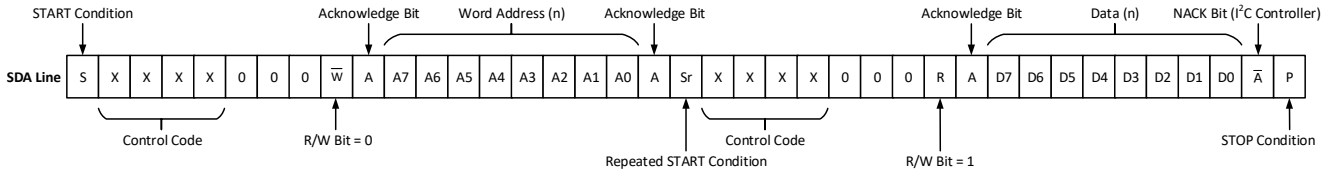


Figure 109. Random Read Command

15.4.5 Sequential Read Command

The Sequential Read Command is initiated in the same way as a Random Read Command, except that, once the SLG46857-A transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

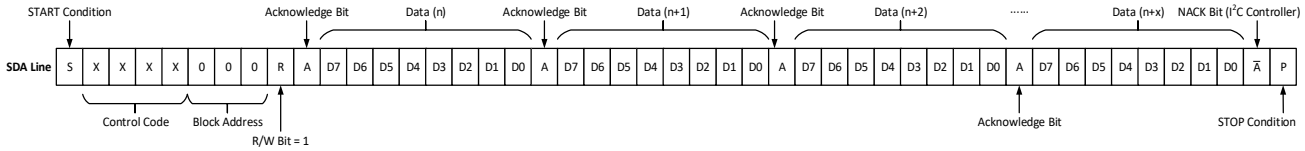


Figure 110. Sequential Read Command

15.4.6 I2C Serial Reset Command

If I2C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells, and all connections provided by the Connection Matrix. This is implemented by setting register [1960] I2C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [1960] will be set to “0” automatically. The Figure 111 illustrates the sequence of events for this reset function.

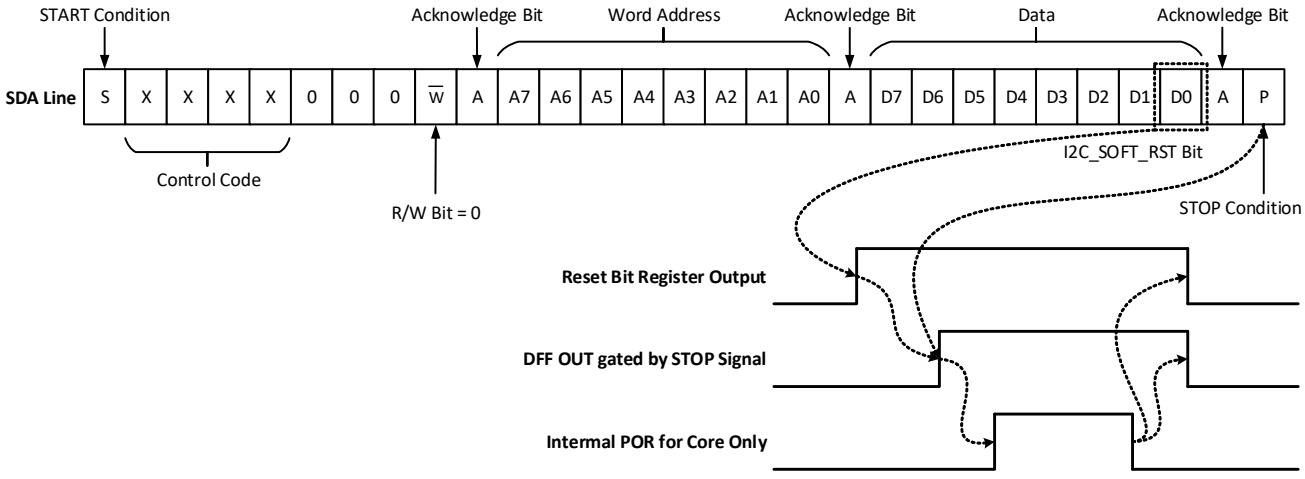


Figure 111. Reset Command Timing

15.5 I²C Serial Command Register Map

There are seven read/write protect modes for the design sequence from being corrupted or copied. See Table 54 for details.

Table 54. Read/Write Protection Options

Configurations	Protection modes configuration							Data output from	Register address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
I²C Byte Write Bit Masking (section 15.6.3 I2C Byte Write Bit Masking)	R/W	R/W	R/W	R/W	W	R	-	Memory	0xF6
I²C Serial Reset Command (section 15.6 I2C Additional Options)	R/W	R/W	R/W	R/W	W	R	-	Memory	0xF5,b'0
Outputs LATCHing during I²C Write	R/W	R/W	R/W	R/W	W	R	-	Memory	0xF5,b'1
Connection Matrix Virtual Inputs (section 6.3 Connection Matrix Virtual Inputs)	R/W	R/W	R/W	R/W	W	R	-	Macrocell	0x4C
Configuration Bits for All Macrocells (IO Pins, ACMPs, Combination Function Macrocells, and others)	R/W	R/W	W	-	W	R	-	Memory	
Macrocells Inputs Configuration (Connection Matrix Outputs, section 6.2 Matrix Output Table)	R/W	W	W	-	W	R	-	Memory	0x00~ 0x47
Protection Mode Enable	R/W	R	R	R	R	R	R	Memory	0xF5,b'3
Protection Mode Selection	R/W	R	R	R	R	R	R	Memory	0xF5,b'7~ 5
Macrocells Output Values (Connection Matrix Inputs, section 6.1 Matrix Input Table)	R	R	R	R	-	R	-	Macrocell	0x48~ 0x4B; 0x4D~ 0x4F
Counter Current Value (for 16-bit CNT)	R	R	R	R	-	R	-	Macrocell	0xA5, 0xA6

Table 54. Read/Write Protection Options (Cont.)

Configurations	Protection modes configuration							Data output from	Register address
	Unlocked	Partly Lock Read1	Partly Lock Read2	Partly Lock Read2/ Write	Lock Read	Lock Write	Lock Read/ Write		
	(Mode 0)	(Mode 1)	(Mode 2)	(Mode 3)	(Mode 4)	(Mode 5)	(Mode 6)		
Counter Current Value (for 8-bit CNT)	R	R	R	R	-	R	-	Macrocell	0xA7, 0xA8
Silicon Identification Service Bits	R	R	R	R	R	R	R	Memory	0xFC
Pattern ID0/1	R	R	R	R	R	R	R	Memory	0xFA, 0xF8
I2C Control Code (section 15.2 I2C Serial Communications Device Addressing)	R	R	R	R	R	R	R	Memory	0xFD,b'3 ~0
Pin Slave Address Select	R	R	R	R	R	R	R	Memory	0xFD,b'7 ~4
I2C Disable/Enable	R	R	R	R	R	R	R	Memory	0xFE,b'0

R/W	Allow Read and Write Data
W	Allow Write Data Only
R	Allow Read Data Only
-	The Data is protected for Read and Write

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I2C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allows identifying silicon family, its revision, and others. See Section 17. Register Definitions for detailed information on all registers.

15.6 I2C Additional Options

When output latching during I2C write, register [1961] = 1 allows all PINs output value to be latched until I2C write is done. It will protect the output change due to configuration process during I2C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I2C write **(Note)**.

If the user sets GPIO0 and GPIO1 function to a selection other than SDA and SCL, all access via I2C will be disabled.

Note: Any write commands that come to the device via I2C that are not blocked, based on the protection bits, will change the contents of the RAM register bits that mirror the NVM bits. These write commands will not change the NVM bits themselves, and a POR event will restore the register bits to original programmed contents of the NVM. See Section 17. Register Definitions for detailed information on all registers.

15.6.1 Reading Counter Data via I²C

The current counter value in three counters in the device can be read via I²C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT6 and CNT7.

15.6.2 I²C Expander

In addition to the eight Connection Matrix Virtual Inputs, the SLG46857-A chip has four pins which can be used as an I²C Expander. These four pins are GPO0, GPIO6, GPIO7, and GPIO8.

Each of these pins can be used as an I²C Expander output or used as a normal pin. Also, each of these four expander outputs have initial state settings which are specified in registers [1959:1952].

15.6.3 I²C Byte Write Bit Masking

The I²C macrocell inside SLG46857-A supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 15.4.1 Byte Write Command for details) on the I²C Byte Write Mask Register (address 0F6H) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I²C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I²C Byte Write Mask Register are reset (set to 00h) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I²C Byte Write Mask Register will be reset with no effect. Figure 112 shows an example of this function.

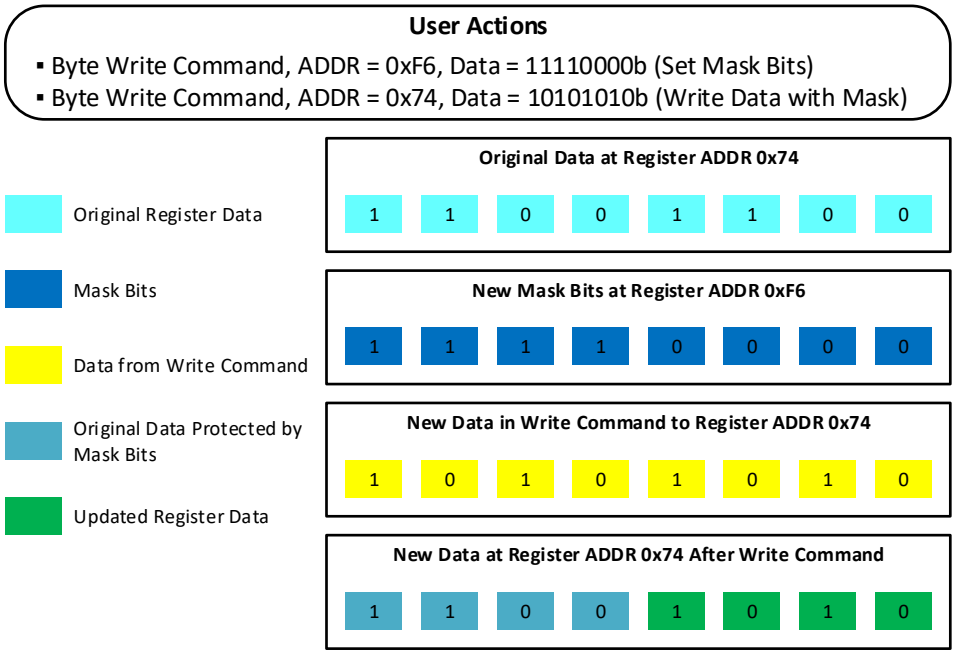


Figure 112. Example of I²C Byte Write Bit Masking

16. Analog Temperature Sensor

The SLG46857-A has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade temperature. The TS cell shares buffer with Vref0, so it is impossible to use both cells simultaneously, its output can be connected directly to the GPIO8 or to the ACMP3_L positive input. Using buffer causes low-output impedance, linear output, and makes interfacing to readout or control circuitry especially easy. The TS is rated to operate over a -40 °C to 125 °C temperature range. The error in the whole temperature range does not exceed ±3.36 %. For more details refer to Section 3.11 Analog Temperature Sensor Specifications.

The equations below calculates the typical analog voltage passed from the TS to the ACMPs' IN+ source input and the temperature at this voltage accordingly. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1} = -0.000676 \times T_{TS1}^2 - 2.3 \times T_{TS1} + 906.4$$

$$T_{TS1} = \frac{100}{169} \times (\sqrt{5} \times \sqrt{2419033 - 845 \times V_{TS1}} - 2875)$$

$$V_{TS2} = -0.000840 \times T_{TS2}^2 - 2.8 \times T_{TS2} + 1094.8$$

$$T_{TS2} = \frac{50}{21} \times (\sqrt{719908 - 210 \times V_{TS2}} - 700)$$

where:

V_{TS1} (mV) - TS Output Voltage, range 1

V_{TS2} (mV) - TS Output Voltage, range 2

T (°C) - Temperature

Temperature hysteresis can be setup by enabling the GreenPAK's internal ACMP hysteresis.

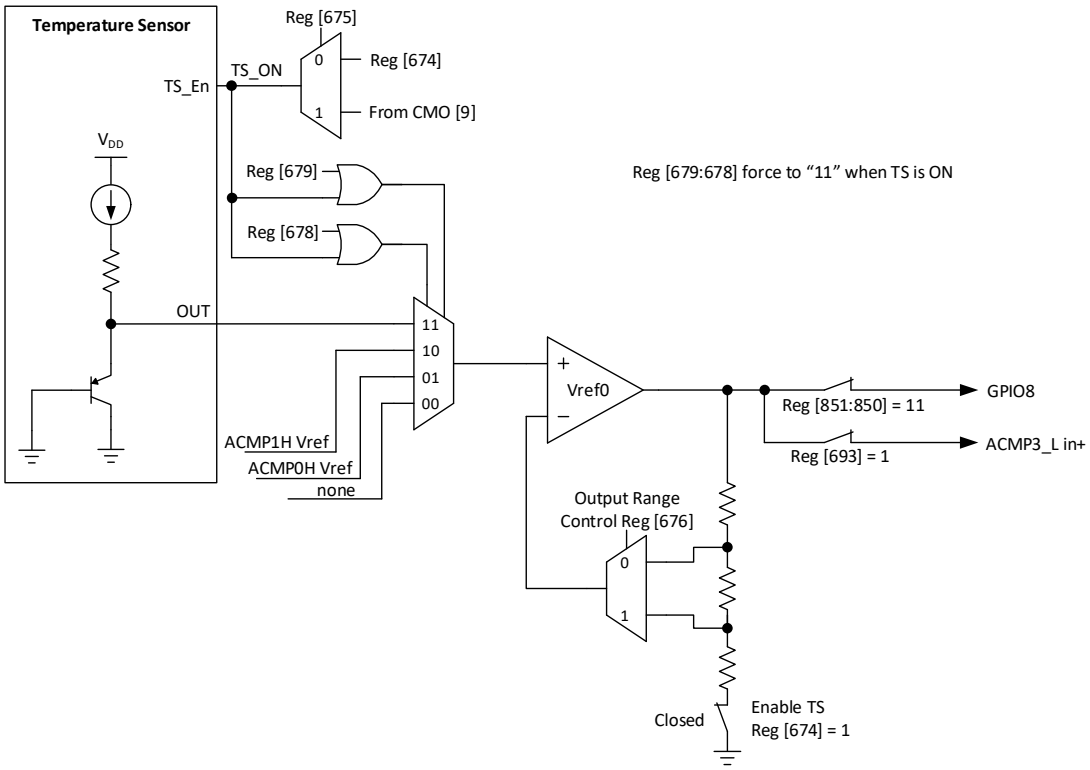


Figure 113. Analog Temperature Sensor Structure Diagram

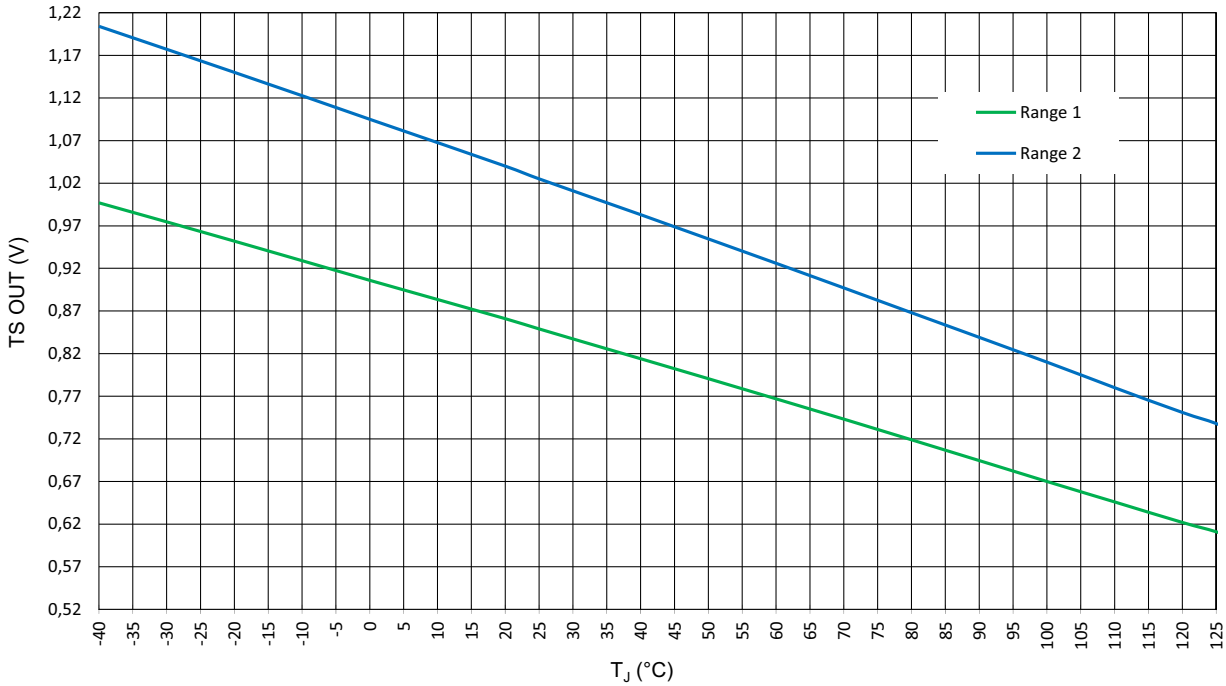


Figure 114. TS Output vs. Temperature, V_{DD} = 2.3 V to 5.5 V

17. Register Definitions

17.1 Register Map

Table 55. Register Map

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
Matrix Output				
0x00	0	LUT2_0 & DFF0	R/W	OUT0: IN0 of LUT2_0 or Clock Input of DFF0
	1			
	2			
	3			
	4			
	5			
	6		R/W	OUT1 IN1 of LUT2_0 or Data Input of DFF0
	7			
0x01	8			
	9			
	10			
	11			
	12	LUT2_1 & DFF1	R/W	OUT2: IN0 of LUT2_1 or Clock Input of DFF1
	13			
	14			
	15			
0x02	16			
	17			
	18		R/W	OUT3: IN1 of LUT2_1 or Data Input of DFF1
	19			
	20			
	21			
	22			
	23			
0x03	24	LUT2_2 & DFF2	R/W	OUT4: IN0 of LUT2_2 or Clock Input of DFF2
	25			
	26			
	27			
	28			
	29			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x03	30	LUT2_2 & DFF2	R/W	OUT5: IN1 of LUT2_2 or Data Input of DFF2
	31			
0x04	32			
	33			
	34			
	35			
	36	LUT2_3 & PGen	R/W	OUT6: IN0 of LUT2_3 or Clock Input of PGen
	37			
	38			
	39			
0x05	40		R/W	OUT7: IN1 of LUT2_3 or nRST of PGen
	41			
	42			
	43			
	44			
	45			
	46			
	47			
0x06	48	LUT3_0 & DFF3	R/W	OUT8: IN0 of LUT3_0 or CLK Input of DFF3
	49			
	50			
	51			
	52			
	53			
	54		R/W	OUT9: IN1 of LUT3_0 or Data of DFF3
	55			
0x07	56			
	57			
	58			
	59			
	60		R/W	OUT10: IN2 of LUT3_0 or nRST (nSET) of DFF3
	61			
	62			
	63			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x08	64	LUT3_0 & DFF3	R/W	OUT10: IN2 of LUT3_0 or nRST (nSET) of DFF3
	65			
	66	LUT3_1 & DFF4	R/W	OUT11: IN0 of LUT3_1 or CLK Input of DFF4
	67			
	68			
	69			
	70			
	71			
0x09	72	LUT3_1 & DFF4	R/W	OUT12: IN1 of LUT3_1 or Data of DFF4
	73			
	74			
	75			
	76			
	77			
	78		R/W	OUT13: IN2 of LUT3_1 or nRST (nSET) of DFF4
	79			
0x0A	80			
	81			
	82			
	83			
	84	LUT3_2 & DFF5	R/W	OUT14: IN0 of LUT3_2 or CLK Input of DFF5
	85			
	86			
	87			
0x0B	88			
	89			
	90		R/W	OUT15: IN1 of LUT3_2 or Data of DFF5
	91			
	92			
	93			
	94			
	95			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x0C	96	LUT3_2 & DFF5	R/W	OUT16: IN2 of LUT3_2 or nRST (nSET) of DFF5
	97			
	98			
	99			
	100			
	101			
	102	LUT3_3 & DFF6	R/W	OUT17: IN0 of LUT3_3 or CLK Input of DFF6
	103			
0x0D	104			
	105			
	106			
	107			
	108		R/W	OUT18: IN1 of LUT3_3 or Data of DFF6
	109			
	110			
	111			
0x0E	112			
	113			
	114		R/W	OUT19: IN2 of LUT3_3 or nRST (nSET) of DFF6
	115			
	116			
	117			
	118			
	119			
0x0F	120	LUT3_4 & DFF7	R/W	OUT20: IN0 of LUT3_4 or CLK Input of DFF7
	121			
	122			
	123			
	124			
	125			
	126		R/W	OUT21: IN1 of LUT3_4 or Data of DFF7
	127			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x10	128	LUT3_4 & DFF7	R/W	OUT21: IN1 of LUT3_4 or Data of DFF7
	129			
	130			
	131			
	132		R/W	OUT22: IN2 of LUT3_4 or nRST (nSET) of DFF7
	133			
	134			
	135			
0x11	136			
	137			
	138	LUT3_5 & DFF8	R/W	OUT23: IN0 of LUT3_5 or CLK Input of DFF8
	139			
	140			
	141			
	142			
	143			
0x12	144		R/W	OUT24: IN1 of LUT3_5 or Data of DFF8
	145			
	146			
	147			
	148			
	149			
	150		R/W	OUT25: IN2 of LUT3_5 or nRST (nSET) of DFF8
	151			
0x13	152			
	153			
	154			
	155			
	156	LUT3_6 & DFF9	R/W	OUT26: IN0 of LUT3_6 or CLK Input of DFF9
	157			
	158			
	159			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x14	160	LUT3_6 & DFF9	R/W	OUT26: IN0 of LUT3_6 or CLK Input of DFF9
	161			
	162		R/W	OUT27: IN1 of LUT3_6 or Data of DFF9
	163			
	164			
	165			
	166			
	167			
0x15	168		R/W	OUT28: IN2 of LUT3_6 or nRST (nSET) of DFF9
	169			
	170			
	171			
	172			
	173			
	174	LUT3_7 & DFF10	R/W	OUT29: IN0 of LUT3_7 or CLK Input of DFF10
	175			
0x16	176			
	177			
	178			
	179			
	180		R/W	OUT30: IN1 of LUT3_7 or Data of DFF10
	181			
	182			
	183			
0x17	184			
	185			
	186		R/W	OUT31: IN2 of LUT3_7 or nRST (nSET) of DFF10
	187			
	188			
	189			
	190			
	191			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x18	192	LUT3_8 & DFF11	R/W	OUT32: IN0 of LUT3_8 or CLK Input of DFF11
	193			
	194			
	195			
	196			
	197			
	198		R/W	OUT33: IN1 of LUT3_8 or Data of DFF11
	199			
0x19	200			
	201			
	202			
	203			
	204		R/W	OUT34: IN2 of LUT3_8 or nRST (nSET) of DFF11
	205			
	206			
	207			
0x1A	208			
	209			
	210	Multi_function4	R/W	OUT35: IN0 of LUT3_12 or CLK Input of DFF16 Delay4 Input (or Counter4 nRST Input)
	211			
	212			
	213			
	214			
	215			
0x1B	216		R/W	OUT36: IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay4 Input (or Counter4 nRST Input)
	217			
	218			
	219			
	220			
	221			
	222		R/W	OUT37: IN2 of LUT3_12 or Data of DFF16 Delay4 Input (or Counter4 nRST Input)
	223			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x1C	224	Multi_function4	R/W	OUT37: IN2 of LUT3_12 or Data of DFF16 Delay4 Input (or Counter4 nRST Input)
	225			
	226			
	227			
	228	Multi_function5	R/W	OUT38: IN0 of LUT3_13 or CLK Input of DFF17 Delay5 Input (or Counter5 nRST Input)
	229			
	230			
	231			
0x1D	232		R/W	OUT39: IN1 of LUT3_13 or nRST (nSET) of DFF17 Delay5 Input (or Counter5 nRST Input)
	233			
	234			
	235			
	236			
	237			
	238			
	239			
0x1E	240		R/W	OUT40: IN2 of LUT3_13 or Data of DFF17 Delay5 Input (or Counter5 nRST Input)
	241			
	242			
	243			
	244			
	245			
	246	Multi_function6	R/W	OUT41: IN0 of LUT3_14 or CLK Input of DFF18 Delay6 Input (or Counter6 nRST Input)
	247			
0x1F	248			
	249			
	250			
	251			
	252		R/W	OUT42: IN1 of LUT3_14 or nRST (nSET) of DFF18 Delay6 Input (or Counter6 nRST Input)
	253			
	254			
	255			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x20	256	Multi_function6	R/W	OUT42: IN1 of LUT3_14 or nRST (nSET) of DFF18 Delay6 Input (or Counter6 nRST Input)
	257			
	258		R/W	OUT43: IN2 of LUT3_14 or Data of DFF18 Delay6 Input (or Counter6 nRST Input)
	259			
	260			
	261			
	262			
	263			
0x21	264	Multi_function7	R/W	OUT44: IN0 of LUT3_15 or CLK Input of DFF19 Delay7 Input (or Counter7 nRST Input)
	265			
	266			
	267			
	268			
	269			
	270		R/W	OUT45: IN1 of LUT3_15 or nRST (nSET) of DFF19 Delay7 Input (or Counter7 nRST Input)
	271			
0x22	272			
	273			
	274			
	275			
	276		R/W	OUT46: IN2 of LUT3_15 or Data of DFF19 Delay7 Input (or Counter7 nRST Input)
	277			
	278			
	279			
0x23	280			
	281			
	282	LUT3_16 & Pipe Delay (RIPP CNT)	R/W	OUT47: IN0 of LUT3_16 or Input of Pipe Delay or UP signal of RIPP CNT
	283			
	284			
	285			
	286			
	287			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x24	288	LUT3_16 & Pipe Delay (RIPP CNT)	R/W	OUT48: IN1 of LUT3_16 or nRST of Pipe Delay or nSET of RIPP CNT
	289			
	290			
	291			
	292			
	293			
	294		R/W	OUT49: IN2 of LUT3_16 or Clock of Pipe Delay_RIPP CNT
	295			
0x25	296			
	297			
	298			
	299			
	300	LUT4_DFF12	R/W	OUT50: IN0 of LUT4_0 or CLK Input of DFF12
	301			
	302			
	303			
0x26	304			
	305			
	306		R/W	OUT51: IN1 of LUT4_0 or Data of DFF12
	307			
	308			
	309			
	310			
	311			
0x27	312	LUT4_DFF12	R/W	OUT52: IN2 of LUT4_0 or nRST (nSET) of DFF12
	313			
	314			
	315			
	316			
	317			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x27	318	LUT4_DFF12	R/W	OUT53: IN3 of LUT4_0
	319			
0x28	320			
	321			
	322			
	323			
	324	Programmable delay	R/W	OUT54: Programmable delay/edge detect input
	325			
	326			
	327			
0x29	328			
	329			
	330	Filter/Edge Detect	R/W	OUT55: Filter/Edge detect input
	331			
	332			
	333			
	334			
	335			
0x2A	336	GPIO0	R/W	OUT56: GPIO0 DOUT
	337			
	338			
	339			
	340			
	341			
	342	GPIO1	R/W	OUT57: GPIO1 DOUT
	343			
0x2B	344			
	345			
	346			
	347			
	348	GPIO2	R/W	OUT58: GPIO2 DOUT
	349			
	350			
	351			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x2C	352	GPIO2	R/W	OUT58: GPIO2 DOUT
	353			
	354		R/W	OUT59: GPIO2 DOUT OE
	355			
	356			
	357			
	358			
	359			
0x2D	360	GPIO3 DOUT and Input of Power Switch ON0	R/W	OUT60: GPIO3 DOUT and Input of Power Switch ON0
	361			
	362			
	363			
	364			
	365			
	366		R/W	OUT61: GPIO3 DOUT OE
	367			
0x2E	368			
	369			
	370			
	371			
	372	GPO0 and Input of Power Switch ON1	R/W	OUT62: GPO0 DOUT and Input of Power Switch ON1
	373			
	374			
	375			
0x2F	376			
	377			
	378	GPIO4	R/W	OUT63: GPIO4 DOUT
	379			
	380			
	381			
	382			
	383			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x30	384	GPIO4	R/W	OUT64: GPIO4 DOUT OE
	385			
	386			
	387			
	388			
	389			
	390	GPIO5	R/W	OUT65: GPIO5 DOUT
	391			
0x31	392			
	393			
	394			
	395			
	396		R/W	OUT66: GPIO5 DOUT OE
	397			
	398			
	399			
0x32	400			
	401			
	402	GPIO6	R/W	OUT67: GPIO6 DOUT
	403			
	404			
	405			
	406			
	407			
0x33	408		R/W	OUT68: GPIO6 DOUT OE
	409			
	410			
	411			
	412			
	413			
	414	GPIO7	R/W	OUT69: GPIO7 DOUT
	415			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x34	416	GPIO7	R/W	OUT69: GPIO7 DOUT
	417			
	418			
	419			
	420		R/W	OUT70: GPIO7 DOUT OE
	421			
	422			
	423			
0x35	424			
	425			
	426	GPIO8	R/W	OUT71: GPIO8 DOUT
	427			
	428			
	429			
	430			
	431			
0x36	432		R/W	OUT72: GPIO8 DOUT OE
	433			
	434			
	435			
	436			
	437			
	438	GPIO9	R/W	OUT73: GPIO9 DOUT
	439			
0x37	440			
	441			
	442			
	443			
	444		R/W	OUT74: GPIO9 DOUT OE
	445			
	446			
	447			
0x38	448			
	449			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x38	450	ACMP0H	R/W	OUT75: PWR UP of ACMP0H
	451			
	452			
	453			
	454			
	455			
0x39	456	ACMP1H	R/W	OUT76: PWR UP of ACMP1H
	457			
	458			
	459			
	460			
	461			
	462	ACMP2L	R/W	OUT77: PWR UP of ACMP2L
	463			
0x3A	464			
	465			
	466			
	467			
	468	ACMP3L	R/W	OUT78: PWR UP of ACMP3L
	469			
	470			
	471			
0x3B	472			
	473			
	474	Temp Sensor	R/W	OUT79: Temp sensor, Vref Out_0, Vref Out_1 Power Up
	475			
	476			
	477			
	478			
	479			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x3C	480	OSC0	R/W	OUT80: OSC0 ENABLE
	481			
	482			
	483			
	484			
	485			
	486	OSC1	R/W	OUT81: OSC1 ENABLE
	487			
0x3D	488			
	489			
	490			
	491			
	492	OSC2	R/W	OUT82: OSC2 ENABLE
	493			
	494			
	495			
0x3E	496			
	497			
	498	Multi_function0	R/W	OUT83: IN0 of LUT4_1 or CLK Input of DFF20 Delay0 Input (or Counter0 nRST Input)
	499			
	500			
	501			
	502			
	503			
0x3F	504	Multi_function0	R/W	OUT84: IN1 of LUT4_1 or nRST of DFF20 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source
	505			
	506			
	507			
	508			
	509			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x3F	510	Multi_function0	R/W	OUT85: IN2 of LUT4_1 or nSET of DFF20 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0
	511			
0x40	512			
	513			
	514			
	515			
	516		R/W	OUT86: IN3 of LUT4_1 or Data of DFF20 Delay0 Input (or Counter0 nRST Input) UP Input of FSM0
	517			
	518			
	519			
0x41	520			
	521			
	522	Multi_function1	R/W	OUT87: IN0 of LUT3_9 or CLK Input of DFF13 Delay1 Input (or Counter1 nRST Input)
	523			
	524			
	525			
	526			
	527			
0x42	528		R/W	OUT88: IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay1 Input (or Counter1 nRST Input)
	529			
	530			
	531			
	532			
	533			
	534		R/W	OUT89: IN2 of LUT3_9 or Data of DFF13 Delay1 Input (or Counter1 nRST Input)
	535			
0x43	536			
	537			
	538			
	539			
	540	Multi_function2	R/W	OUT90: IN0 of LUT3_10 or CLK Input of DFF14 Delay2 Input (or Counter2 nRST Input)
	541			
	542			
	543			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x44	544	Multi_function2	R/W	OUT90: IN0 of LUT3_10 or CLK Input of DFF14 Delay2 Input (or Counter2 nRST Input)
	545			
	546		R/W	OUT91: IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay2 Input (or Counter2 nRST Input)
	547			
	548			
	549			
	550			
	551			
0x45	552		R/W	OUT92: IN2 of LUT3_10 or Data of DFF14 Delay2 Input (or Counter2 nRST Input)
	553			
	554			
	555			
	556			
	557			
	558	Multi_function3	R/W	OUT93: IN0 of LUT3_11 or CLK Input of DFF15 Delay3 Input (or Counter3 nRST Input)
	559			
0x46	560			
	561			
	562			
	563			
	564		R/W	OUT94: IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay3 Input (or Counter3 nRST Input)
	565			
	566			
	567			
0x47	568			
	569			
	570		R/W	OUT95: IN2 of LUT3_11 or Data of DFF15 Delay3 Input (or Counter3 nRST Input)
	571			
	572			
	573			
	574			
	575			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x48	576	Matrix Input 0	R	GND
	577	Matrix Input 1	R	LUT2_0/DFF0 output
	578	Matrix Input 2	R	LUT2_1/DFF1 output
	579	Matrix Input 3	R	LUT2_2/DFF2 output
	580	Matrix Input 4	R	LUT2_3/PGen output
	581	Matrix Input 5	R	LUT3_0/DFF3 output
	582	Matrix Input 6	R	LUT3_1/DFF4 output
	583	Matrix Input 7	R	LUT3_2/DFF5 output
0x49	584	Matrix Input 8	R	LUT3_3/DFF6 output
	585	Matrix Input 9	R	LUT3_4/DFF7 output
	586	Matrix Input 10	R	LUT3_5/DFF8 output
	587	Matrix Input 11	R	LUT3_6/DFF9 output
	588	Matrix Input 12	R	LUT3_7/DFF10 output
	589	Matrix Input 13	R	LUT3_8/DFF11 output
	590	Matrix Input 14	R	CNT0 output
	591	Matrix Input 15	R	MF0_LUT4/DFF_OUT
0x4A	592	Matrix Input 16	R	CNT1 output
	593	Matrix Input 17	R	MF1_LUT3/DFF_OUT
	594	Matrix Input 18	R	CNT2 output
	595	Matrix Input 19	R	MF2_LUT3/DFF_OUT
	596	Matrix Input 20	R	CNT3 output
	597	Matrix Input 21	R	MF3_LUT3/DFF_OUT
	598	Matrix Input 22	R	CNT4 output
	599	Matrix Input 23	R	MF4_LUT3/DFF_OUT
0x4B	600	Matrix Input 24	R	CNT5 output
	601	Matrix Input 25	R	MF5_LUT3/DFF_OUT
	602	Matrix Input 26	R	CNT6 output
	603	Matrix Input 27	R	MF6_LUT3/DFF_OUT
	604	Matrix Input 28	R	CNT7 output
	605	Matrix Input 29	R	MF7_LUT3/DFF_OUT
	606	Matrix Input 30	R	LUT3_16/Ripple CNT/Pipe Delay_out0
	607	Matrix Input 31	R	Ripple CNT/Pipe Delay_out1

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x4C	608	Matrix Input 32	R/W	GPIO0 digital input or I2C_virtual_0 Input
	609	Matrix Input 33	R/W	GPIO1 digital input or I2C_virtual_1 Input
	610	Matrix Input 34	R/W	I2C_virtual_2 Input
	611	Matrix Input 35	R/W	I2C_virtual_3 Input
	612	Matrix Input 36	R/W	I2C_virtual_4 Input
	613	Matrix Input 37	R/W	I2C_virtual_5 Input
	614	Matrix Input 38	R/W	I2C_virtual_6 Input
	615	Matrix Input 39	R/W	I2C_virtual_7 Input
0x4D	616	Matrix Input 40	R	Ripple CNT_out2
	617	Matrix Input 41	R	LUT4_0/DFF12 output
	618	Matrix Input 42	R	Programmable Delay Edge Detect Output
	619	Matrix Input 43	R	Edge Detect Filter Output
	620	Matrix Input 44	R	GPI0 Digital Input
	621	Matrix Input 45	R	GPIO2 Digital Input
	622	Matrix Input 46	R	Power Switch ON0, GPIO3 Digital Input
	623	Matrix Input 47	R	GPIO4 Digital Input
0x4E	624	Matrix Input 48	R	GPIO5 Digital Input
	625	Matrix Input 49	R	GPIO6 Digital Input
	626	Matrix Input 50	R	GPIO7 Digital Input
	627	Matrix Input 51	R	GPIO8 Digital Input
	628	Matrix Input 52	R	GPIO9 Digital Input
	629	Matrix Input 53	R	OSC0 output 0
	630	Matrix Input 54	R	OSC1 output 0
	631	Matrix Input 55	R	OSC2 output
0x4F	632	Matrix Input 56	R	ACMP0H Output (normal speed)
	633	Matrix Input 57	R	ACMP1H Output (normal speed)
	634	Matrix Input 58	R	ACMP2L Output (low speed)
	635	Matrix Input 59	R	ACMP3L output (low speed)
	636	Matrix Input 60	R	OSC0 output 1
	637	Matrix Input 61	R	OSC1 output 1
	638	Matrix Input 62	R	Matrix nRST
	639	Matrix Input 63	R	V_{DD}

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x50	640	BG CHOP OFF	R/W	0: CHOP enable 1: chopper off
	641	BG Chopper clock test enable	R/W	1: enable
	642	Bandgap internal voltage output to IO enable	R/W	1: enable
	643	Bandgap power-down control	R/W	0: always on 1: power-down if no function enable it (ACMP, Vref, TS)
	644	ACMP1H external Vref0 source selection	R/W	0: from GPIO2 1: from GPO0
	645	ACMP2L external Vref1 source selection	R/W	0: from GPIO2 1: from GPO0
	646	ACMP3L external Vref1 source selection	R/W	0: from GPIO2 1: from GPO0
	647	ACMP3L wake sleep enable	R/W	1: enable 0: disable
0x51	648	VrefO0 register Power-On/Off	R/W	1: on 0: off
	649	VrefO0 power-down selection	R/W	0: come from register [648] 1: come from matrix out92
	650	VrefO1 register Power-On/Off	R/W	1: on 0: off
	651	ACMP0H hysteresis	R/W	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	652		R/W	
	653	Reserved	R/W	
	654	ACMP0_H input buffer enable	R/W	1: enable
	655	Reserved	R/W	
0x52	656	ACMP0H input tie to V_{DD} enable	R/W	1: enable
	657	ACMP1_H positive input come from ACMP0_H's input mux output enable; 1:enable	R/W	
	658	Reserved	R/W	
	659	ACMP1H hysteresis	R/W	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	660		R/W	
	661	ACMP1H input buffer enable	R/W	1: enable
	662	Reserved	R/W	
	663	ACMP2L positive input come from ACMP0H's input mux output enable	R/W	1: enable

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x53	664	ACMP2L positive input come from ACMP1H's input mux output enable	R/W	1: enable
	665	ACMP2L hysteresis	R/W	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	666		R/W	
	667	Reserved	R/W	
	668	Reserved	R/W	
	669	ACMP3_L hysteresis	R/W	00: 0 mV 01: 32 mV 10: 64 mV 11: 192 mV
	670		R/W	
	671	Reserved	R/W	
0x54	672	Reserved	R/W	
	673	ACMP3_L positive input come from ACMP2L's input mux output enable	R/W	1: enable
	674	Temp sensor register pdb control	R/W	0: Power-down 1: Power-On
	675	Temp sensor register pdb select	R/W	0: come from register 1: come from Matrix
	676	Temp sensor range select	R/W	0: range 1 (0.62V ~ 0.99V (TYP)) 1: range 2 (0.75V ~ 1.2V (TYP))
	677	Vref0 output OP	R/W	0: disable 1: enable
	678	Vref0 input selection	R/W	00: None 01: ACMP0H Vref 10: ACMP1H Vref 11: temp sensor
	679		R/W	
0x55	680	Vref1 output OP	R/W	0: disable 1: enable
	681	Vref1 input selection	R/W	00: None 01: ACMP2L Vref 10: ACMP3L Vref
	682		R/W	
	683	VBG fine tune selection	R/W	0000: 1.194, 0001:1.195, 0011:1.196, 0100:1.197, 0101:1.198, 0110:1.199 0111:1.2, 1000:1.201, 1001:1.202, 1010:1.203, 1011:1.204, 1100:1.205, 1101:1.206, 1110:1.207, 1111:1.208
	684		R/W	
	685		R/W	
	686		R/W	
	687	ACMP0H Wake/Sleep enable	R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x56	688	ACMP1H Wake/Sleep enable	R/W	
	689	ACMP Wake/Sleep time selection	R/W	0: short time 1: normal w/s
	690	ACMP0H 100 uA current source enable	R/W	
	691	Reserve for ACMP	R/W	
	692	Reserved	R/W	
	693	ACMP3L input come from Temp sensor output enable	R/W	
	694	VrefO1 power-down selection	R/W	0: come from register [650] 1: come from matrix OUT92
	695	ACMP2L wake sleep enable	R/W	0: disable 1: enable
0x57	696	ACMP0H Gain divider	R/W	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	697		R/W	
	698	ACMP0H Vref0	R/W	ACMP Vref select: 000000: 32mV ~ 111110: 2.016V/step = 32 mV 111111: External Vref
	699		R/W	
	700		R/W	
	701		R/W	
	702		R/W	
	703		R/W	
0x58	704	ACMP1H Gain divider	R/W	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	705		R/W	
	706	ACMP1H Vref0	R/W	ACMP Vref select: 000000: 32 mV ~ 1 11110: 2.016V/step = 32mV 111111: External Vref
	707		R/W	
	708		R/W	
	709		R/W	
	710		R/W	
	711		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x59	712	ACMP2L Gain divider	R/W	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	713		R/W	
	714	ACMP2L Vref1	R/W	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016V/step = 32mV 111111: External Vref
	715		R/W	
	716		R/W	
	717		R/W	
	718		R/W	
	719		R/W	
0x5A	720	ACMP3L Gain divider	R/W	ACMP gain divider select: 00: 1x 01:0.5x 10:0.33x 11:0.25x
	721		R/W	
	722	ACMP3L Vref1	R/W	ACMP Vref select: 000000: 32 mV ~ 111110: 2.016V/step = 32mV 111112: External Vref
	723		R/W	
	724		R/W	
	725		R/W	
	726		R/W	
	727		R/W	
OSC1				
0x5B	728	OSC1 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	729	matrix power-down or on select	R/W	0: matrix down 1: matrix on
	730	external clock source enable	R/W	0: internal OSC1 1: external clock from GPIO2
	731	post divider ratio control OSC1	R/W	00: div 1 01: div 2 10: div 4 11: div 8
	732		R/W	
	733	matrix divider ratio control OSC1, OUT0	R/W	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	734		R/W	
	735		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x5C	736	matrix out enable OSC1, OUT0	R/W	0: disable 1: enable
	737	Reserved	R/W	
	738	Reserved	R/W	
	739	Reserved	R/W	
OSC2				
0x5C	740	OSC2 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	741	matrix power-down or on select	R/W	0: matrix down 1: matrix on
	742	external clock source enable	R/W	0: internal OSC2 1: external clock from GPIO8
	743	matrix out enable	R/W	0: disable 1: enable
0x5D	744	post divider ratio control OSC2	R/W	00: div 1 01: div 2 10: div 4 11: div 8
	745		R/W	
	746	matrix divider ratio control OSC2	R/W	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	747		R/W	
	748		R/W	
	749	startup delay with 100 ns	R/W	0: enable 1: disable
OSC0				
0x5D	750	OSC0 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	751	matrix power-down or on select	R/W	0: matrix down 1: matrix on

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x5E	752	external clock source enable	R/W	0: internal OSC0 1: external clock from GPIO
	753	matrix out enable OSC0, OUT0	R/W	0: disable 1: enable
	754	post divider ratio control OSC0	R/W	00: div 1 01: div 2 10: div 4 11: div 8
	755		R/W	
	756	matrix divider ratio control OSC0, OUT0	R/W	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	757		R/W	
	758		R/W	
	759	enable OSC0 output gating by wake_sleep signal (note: the wake_sleep clock is separated path, so it is not gated)	R/W	0: no gating 1: enable
0x5F	760	matrix divider ratio control OSC1, OUT1	R/W	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	761		R/W	
	762		R/W	
	763	2nd output to matrix enable OSC1	R/W	0: disable 1: enable
	764	matrix divider ratio control OSC0, OUT1	R/W	000: /1, 001:/2 , 010:/4, 011: /3, 100: /8, 101: /12, 110: /24, 111: /64
	765		R/W	
	766		R/W	
	767	2nd output to matrix enable OSC0, OUT1	R/W	0: disable 1: enable
0x60	768	Reserved	R/W	
	769		R/W	
	770	Reserved	R/W	
	771	Reserved	R/W	
	772	Reserved	R/W	
	773	Reserved	R/W	
	774	Reserved	R/W	
	775	Reserved	R/W	
0x61	776	Reserved	R/W	
	777	Reserved	R/W	
	778	IO fast Pull-up/down enable	R/W	0: disable 1: enable
GPI0				

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x61	779	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	780		R/W	
	781	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	782		R/W	
	783	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPIO0				
0x62	784	input mode configuration	R/W	00: digital in without Schmitt Trigger 01: digital in with Schmitt Trigger (when register [2032] = 1) 10: low voltage digital in 11: Reserved
	785		R/W	
	786	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	787		R/W	
	788	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
	789	I^2C mode selection	R/W	0: I^2C fast mode+ (3.2x drivability) 1: I^2C standard/fast mode
	790	I/O selection	R/W	0: digital input 1: digital output (1x Open-Drain NMOS)
GPIO1				
0x62	791	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital in with Schmitt Trigger (when register [2032] = 1) 10: low voltage digital in 11: Reserved
0x63	792		R/W	
	793	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	794		R/W	
	795	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
	796	I/O selection	R/W	0: digital input 1: digital output (1x Open-Drain NMOS)
	797	Reserved	R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
GPIO2				
0x63	798	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	799		R/W	
0x64	800	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	801		R/W	
	802	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	803		R/W	
	804	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPIO3				
0x64	805	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	806		R/W	
	807	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x65	808		R/W	
0x65	809	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	810		R/W	
	811	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPO0				
0x65	812	Reserved	R/W	
	813		R/W	
	814	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	815		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x66	816	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	817		R/W	
	818	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
	819	output enable	R/W	0: output disable (input mode) 1: output enable
	820	4x drive	R/W	0: disable 1: enable
GPIO4				
0x66	821	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	822		R/W	
	823	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x67	824		R/W	
	825	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	826		R/W	
	827	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
	828	4x drive	R/W	0: disable 1: enable
GPIO5				
0x67	829	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	830		R/W	
	831	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x68	832		R/W	
	833	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	834		R/W	
	835	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
GPIO6				
0x68	836	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	837		R/W	
	838	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	839		R/W	
0x69	840	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	841		R/W	
	842	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPIO7				
0x69	843	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	844		R/W	
	845	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	846		R/W	
	847	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
0x6A	848		R/W	
	849	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPIO8				
0x6A	850	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	851		R/W	
	852	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	853		R/W	
	854	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	855		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x6B	856	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
GPIO9				
0x6B	857	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	858		R/W	
	859	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	860		R/W	
	861	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	862		R/W	
	863	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
0x6C	864	Reserved	R	
	865	Reserved	R	
	866	Reserved	R	
	867	Reserved	R	
	868	Reserved	R	
	869	Reserved	R	
	870	Reserved	R	
	871	Reserved	R	
0x6D	872	Reserved	R	
	873	Reserved	R	
	874	Reserved	R	
	875	Reserved	R	
	876	Reserved	R	
	877	Reserved	R	
	878	Reserved	R	
	879	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x6E	880	Reserved	R	
	881	Reserved	R	
	882	Reserved	R	
	883	Reserved	R	
	884	Reserved	R	
	885	Reserved	R	
	886	Reserved	R	
	887	Reserved	R	
0x6F	888	Reserved	R	
	889	Reserved	R	
	890	Reserved	R	
	891	Reserved	R	
	892	Reserved	R	
	893	Reserved	R	
	894	Reserved	R	
	895	Reserved	R	
0x70	896	Reserved	R	
	897	Reserved	R	
	898	Reserved	R	
	899	Reserved	R	
	900	Reserved	R	
	901	Reserved	R	
	902	Reserved	R	
	903	Reserved	R	
0x71	904	Reserved	R	
	905	Reserved	R	
	906	Reserved	R	
	907	Reserved	R	
	908	Reserved	R	
	909	Reserved	R	
	910	Reserved	R	
	911	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x72	912	Reserved	R	
	913	Reserved	R	
	914	Reserved	R	
	915	Reserved	R	
	916	Reserved	R	
	917	Reserved	R	
	918	Reserved	R	
	919	Reserved	R	
0x73	920	Reserved	R	
	921	Reserved	R	
	922	Reserved	R	
	923	Reserved	R	
	924	Reserved	R	
	925	Reserved	R	
	926	Reserved	R	
	927	Reserved	R	
0x74	928	Reserved	R	
	929	Reserved	R	
	930	Reserved	R	
	931	Reserved	R	
	932	Reserved	R	
	933	Reserved	R	
	934	Reserved	R	
	935	Reserved	R	
0x75	936	Reserved	R	
	937	Reserved	R	
	938	Reserved	R	
	939	Reserved	R	
	940	Reserved	R	
	941	Reserved	R	
	942	Reserved	R	
	943	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x76	944	Reserved	R	
	945	Reserved	R	
	946	Reserved	R	
	947	Reserved	R	
	948	Reserved	R	
	949	Reserved	R	
	950	Reserved	R	
	951	Reserved	R	
0x77	952	Reserved	R	
	953	Reserved	R	
	954	Reserved	R	
	955	Reserved	R	
	956	Reserved	R	
	957	Reserved	R	
	958	Reserved	R	
	959	Reserved	R	
0x78	960	Reserved	R	
	961	Reserved	R	
	962	Reserved	R	
	963	Reserved	R	
	964	Reserved	R	
	965	Reserved	R	
	966	Reserved	R	
	967	Reserved	R	
0x79	968	Reserved	R	
	969	Reserved	R	
	970	Reserved	R	
	971	Reserved	R	
	972	Reserved	R	
	973	Reserved	R	
	974	Reserved	R	
	975	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x7A	976	Reserved	R	
	977	Reserved	R	
	978	Reserved	R	
	979	Reserved	R	
	980	Reserved	R	
	981	Reserved	R	
	982	Reserved	R	
	983	Reserved	R	
0x7B	984	Reserved	R	
	985	Reserved	R	
	986	Reserved	R	
	987	Reserved	R	
	988	Reserved	R	
	989	Reserved	R	
	990	Reserved	R	
	991	Reserved	R	
0x7C	992	Reserved	R	
	993	Reserved	R	
	994	Reserved	R	
	995	Reserved	R	
	996	Reserved	R	
	997	Reserved	R	
	998	Reserved	R	
	999	Reserved	R	
0x7D	1000	Reserved	R	
	1001	Reserved	R	
	1002	Reserved	R	
	1003	Reserved	R	
	1004	Reserved	R	
	1005	Reserved	R	
	1006	Reserved	R	
	1007	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x7E	1008	Reserved	R	
	1009	Reserved	R	
	1010	Reserved	R	
	1011	Reserved	R	
	1012	Reserved	R	
	1013	Reserved	R	
	1014	Reserved	R	
	1015	Reserved	R	
0x7F	1016	Reserved	R	
	1017	Reserved	R	
	1018	Reserved	R	
	1019	Reserved	R	
	1020	Reserved	R	
	1021	Reserved	R	
	1022	Reserved	R	
	1023	Reserved	R	
0x80	1030:1024	Single 4-bit LUT	R/W	0000000: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	0010000: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	0000001: Matrix A - UP (CNT); Matrix B - KEEP (CNT); Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (CNT) (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	0000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3)
		CNT/DLY → DFF	R/W	0010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	0100010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In3; In2 - LOW)
		CNT/DLY → DFF	R/W	0110010: Matrix A - DLY_IN; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to D; nSET - HIGH)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x80	1030:1024	CNT/DLY → LUT	R/W	1000010: Matrix A - DLY_IN; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In3; In1 - LOW)
		CNT/DLY → DFF	R/W	1010010: Matrix A - DLY_IN; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to D; nRST - HIGH)
		CNT/DLY → LUT	R/W	0000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - In1; Matrix D - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	0010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - nRST; Matrix D - CLK (DLY_OUT connected to nSET)
		CNT/DLY → LUT	R/W	1000110: Matrix A - In3; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - In0 (DLY_OUT connected to In2; In1 - LOW)
		CNT/DLY → DFF	R/W	1010110: Matrix A - D; Matrix B - DLY_IN; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DLY_OUT connected to nSET; nRST - HIGH)
		CNT/DLY → LUT	R/W	0001010: Matrix A - In3; Matrix B - In2; Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	0011010: Matrix A - D; Matrix B - nSET; Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST)
		CNT/DLY → LUT	R/W	0101010: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - In0 (DLY_OUT connected to In1; In2 - LOW)
		CNT/DLY → DFF	R/W	0111010: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - DLY_IN; Matrix D - CLK (DLY_OUT connected to nRST; nSET - HIGH)
		CNT/DLY → LUT	R/W	0001110: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	0011110: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x80	1030:1024	CNT/DLY → LUT	R/W	0101110: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - DLY_IN (DLY_OUT connected to In0; In2 - LOW)
		CNT/DLY → DFF	R/W	0111110: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - DLY_IN (DLY_OUT connected to CLK; nSET - HIGH)
		CNT/DLY → LUT	R/W	1001110: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to In0; In1 - LOW)
		CNT/DLY → DFF	R/W	1011110: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - DLY_IN (DLY_OUT connected to CLK; nRST - HIGH)
		LUT → CNT/DLY	R/W	0000011: Matrix A - In3; Matrix B - In2; Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	0010011: Matrix A - D; Matrix B - nSET; Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN)
		LUT → CNT/DLY	R/W	0100011: Matrix A - In3; Matrix B - EXT_CLK (CNT); Matrix C - In1; Matrix D - In0 (LUT_OUT connected to DLY_IN; In2 - LOW)
		DFF → CNT/DLY	R/W	0110011: Matrix A - D; Matrix B - EXT_CLK (CNT); Matrix C - nRST; Matrix D - CLK (DFF_OUT connected to DLY_IN; nSET - HIGH)
		LUT → CNT/DLY	R/W	1000011: Matrix A - In3; Matrix B - In2; Matrix C - EXT_CLK (CNT); Matrix D - In0 (LUT_OUT connected to DLY_IN; In1 - LOW)
		DFF → CNT/DLY	R/W	1010011: Matrix A - D; Matrix B - nSET; Matrix C - EXT_CLK (CNT); Matrix D - CLK (DFF_OUT connected to DLY_IN; nRST - HIGH)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x80	1031	DLY/CNT0 Mode Selection	R/W	00: DLY 01: one shot 10: frequency det 11: CNT register [1040] = 0
0x81	1032		R/W	
	1033	DLY/CNT0 edge Mode Selection	R/W	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	1034		R/W	
	1035	DLY/CNT0 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011: 2M/8; 0100: 2M/64; 0101: 2M/512; 0110: 2K(OSC0); 0111: 2K/8; 1000: 2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2 K/262144; 1101: CNT7_END; 1110: External; 1111: Not used
	1036		R/W	
	1037		R/W	
	1038		R/W	
	1039	FSM0 SET/RST Selection	R/W	0: Reset to 0 1: Set to data
0x82	1040	CNT0 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1032:1031] = 00)
	1041	UP signal SYNC selection	R/W	0: bypass 1: after two DFF
	1042	Keep signal SYNC selection	R/W	0: bypass 1: after two DFF
	1043	CNT0 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1044		R/W	
	1045	Wake sleep power-down state selection	R/W	0: low 1: high
	1046	wake sleep mode selection	R/W	0: Default Mode 1: Wake Sleep Mode (registers [1032:1031] = 11)
0x82	1047	CNT0 output pol selection	R/W	0: Default Output 1: Inverted Output

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x83	1048	CNT0 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1053:1049	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x83	1054	CNT1 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1055		R/W	
0x84	1056		R/W	
	1057		R/W	
	1058	CNT1 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1059		R/W	
0x84	1060	DLY/CNT1 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT0_END; 1110: External; 1111: Not used
	1061		R/W	
	1062		R/W	
	1063		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x85	1064	CNT1 output pol selection	R/W	0: Default Output 1: Inverted Output
	1065	CNT1 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1066	CNT1 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers[1057:1054]=0000/0001/0010)
	1071:1067	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x86	1072	CNT2 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1073		R/W	
	1074	CNT2 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1075		R/W	
	1076		R/W	
	1077		R/W	
	1078	DLY/CNT2 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT1_END; 1110: External; 1111: Not used
	1079		R/W	
0x87	1080		R/W	
	1081		R/W	
	1082	CNT2 output pol selection	R/W	0: Default Output, 1: Inverted Output
	1083	CNT2 CNT mode SYNC selection	R/W	0: bypass; 1: after two DFF
	1084	CNT2 DLY EDET FUNCTION Selection	R/W	0: normal; 1: DLY function edge detection(registers[1077:1074] = 0000/0001/0010)
	1085	CNT3 initial value selection	R/W	00:bypass the initial; 01: initial 0; 10: initial 1; 11: initial 1
	1086		R/W	
	1087	Multi3 register configure	R/W	refer to byte 0x88

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x88	1088	CNT3 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1089		R/W	
	1090		R/W	
	1091		R/W	
	1087, 1093:1092, 1095:1094	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x88	1087, 1093:1092, 1095:1094	LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
0x89	1096	DLY/CNT3 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT2_END; 1110: External; 1111: Not used
	1097		R/W	
	1098		R/W	
	1099		R/W	
	1100	CNT3 output pol selection	R/W	0: Default Output 1: Inverted Output
	1101	CNT3 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1102	CNT3 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers[1091:1088]=0000/0001/0010)
	1103	CNT4 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
0x8A	1104	CNT4 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1105		R/W	
	1106	CNT4 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers[1119:1116]=0000/0001/0010)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8A	1111:1107	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8B	1112	DLY/CNT4 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT3_END; 1110: External; 1111: Not used
	1113		R/W	
	1114		R/W	
	1115		R/W	
0x8B	1116	CNT4 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1117		R/W	
	1118		R/W	
	1119		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8C	1120	CNT4 output pol selection	R/W	0: Default Output 1: Inverted Output
	1121	CNT5 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1122		R/W	
	1123		R/W	
	1124		R/W	
	1125	CNT5 output pol selection	R/W	0: Default Output 1: Inverted Output
	1134, 1127:1126, 1133:1132	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8C	1134, 1127:1126, 1133:1132	CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
0x8D	1128	DLY/CNT5 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT4_END; 1110: External; 1111: Not used
	1129		R/W	
	1130		R/W	
	1131		R/W	
	1135	CNT5 DLY EDET FUNCTION Selection	R/W	0: normal; 1: DLY function edge detection (registers[1124:1121]=0000/0001/0010)
0x8E	1136	CNT5 CNT mode SYNC selection	R/W	0: bypass; 1: after two DFF
	1137	CNT5 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1138		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8E	1139	CNT6 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1140		R/W	
	1141		R/W	
	1142		R/W	
	1143	CNT6 output pol selection	R/W	0: Default Output 1: Inverted Output
0x8F	1144	DLY/CNT6 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011:2K/32768; 1100: 2K/262144; 1101: CNT5_END; 1110: External; 1111: Not used
	1145		R/W	
	1146		R/W	
	1147		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8F	1152, 1149:1148, 1151:1150	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)
		CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x90	1152, 1149:1148, 1151:1150	DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1153	CNT6 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers[1142:1139]=0000/0001/0010)
	1154	CNT6 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1155	CNT6 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1156		R/W	
	1157	CNT7 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1158		R/W	
	1159	CNT7 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
0x91	1160	CNT7 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1174:1171]=0000/0001/0010)
	1161, 1165:1162	Single 3-bit LUT	R/W	00000: Matrix A - In2; Matrix B - In1; Matrix C - In0 (DLY_IN - LOW)
		Single DFF w RST and SET	R/W	10000: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DLY_IN - LOW)
		Single CNT/DLY	R/W	00001: Matrix A - DLY_IN (CNT); Matrix B - EXT_CLK (CNT); Matrix C - NC (DLY_OUT connected to LUT/DFF)
		CNT/DLY → LUT	R/W	00010: Matrix A - DLY_IN; Matrix B - In1; Matrix C - In0 (DLY_OUT connected to In2)
		CNT/DLY → DFF	R/W	10010: Matrix A - DLY_IN; Matrix B - nSET/nRST; Matrix C - CLK (DLY_OUT connected to D)
		CNT/DLY → LUT	R/W	00110: Matrix A - In2; Matrix B - DLY_IN; Matrix C - In0 (DLY_OUT connected to In1)
		CNT/DLY → DFF	R/W	10110: Matrix A - D; Matrix B - DLY_IN; Matrix C - CLK (DLY_OUT connected to nSET/nRST)

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x91	1161, 1165:1162	CNT/DLY → LUT	R/W	01010: Matrix A - In2; Matrix B - In1; Matrix C - DLY_IN (DLY_OUT connected to In0)
		CNT/DLY → DFF	R/W	11010: Matrix A - D; Matrix B - nSET/nRST; Matrix C - DLY_IN (DLY_OUT connected to CLK)
		LUT → CNT/DLY	R/W	00011: Matrix A - In2; Matrix B - In1; Matrix C - In0 (LUT_OUT connected to DLY_IN)
		DFF → CNT/DLY	R/W	10011: Matrix A - D; Matrix B - nSET/nRST; Matrix C - CLK (DFF_OUT connected to DLY_IN)
	1166	DLY/CNT7 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2); 0001: 25M/4; 0010: 2M(OSC1); 0011:2M/8; 0100: 2M/64; 0101: 2M/512; 0110:2K(OSC0); 0111: 2K/8; 1000:2K/64; 1001: 2K/512; 1010: 2K/4096; 1011: 2K/32768; 1100: 2K/262144; 1101: CNT6_END; 1110: External; 1111: Not used
	1167		R/W	
0x92	1168		R/W	
	1169		R/W	
	1170	CNT7 output pol selection	R/W	0: Default Output 1: Inverted Output
	1171	CNT7 function and edge mode selection	R/W	0000: both edge Delay; 0001: falling edge delay; 0010: rising edge delay: 0011: both edge One Shot; 0100: falling edge One Shot; 0101: rising edge One Shot; 0110: both edge freq detect; 0111: falling edge freq detect; 1000: rising edge freq detect; 1001: both edge detect; 1010: falling edge detect; 1011: rising edge detect; 1100: both edge reset CNT; 1101: falling edge reset CNT; 1110: rising edge reset CNT; 1111: high level reset CNT
	1172		R/W	
	1173		R/W	
	1174		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x92	1175	Reserved	R/W	
0x93	1176	Multi0_LUT4_DFF setting	R/W	[15]:LUT4_1 [15]/DFF20 or LATCH Select 0: DFF function, 1: LATCH function [14]:LUT4_1 [14]/DFF20 Output Select 0: Q output, 1: QB output [13]:LUT4_1 [13]/DFF20 Initial Polarity Select 0: Low, 1: High [12:0]:LUT4_1 [12:0]
	1177			
	1178			
	1179			
	1180			
	1181			
	1182			
	1183			
0x94	1184			
	1185			
	1186			
	1187			
	1188			
	1189			
	1190			
	1191			
0x95	1192	REG_CNT0_D[15:0]	R/W	Data[15:0]
	1193			
	1194			
	1195			
	1196			
	1197			
	1198			
	1199			
0x96	1200			
	1201			
	1202			
	1203			
	1204			
	1205			
	1206			
	1207			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x97	1208	Multi1_LUT3_DFF setting	R/W	[7]:LUT3_9 [7]/DFF13 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_9 [6]/DFF13 Output Select 0: Q output, 1: QB output [5]:LUT3_9 [5]/DFF13 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_9 [4]/DFF13 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_9 [3:0]
	1209			
	1210			
	1211			
	1212			
	1213			
	1214			
	1215			
0x98	1216	REG_CNT1_D[7:0]	R/W	Data[7:0]
	1217			
	1218			
	1219			
	1220			
	1221			
	1222			
	1223			
0x99	1224	Multi2_LUT3_DFF setting	R/W	[7]:LUT3_10 [7]/DFF14 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_10[6]/DFF14 Output Select 0: Q output, 1: QB output [5]:LUT3_10 [5]/DFF14 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_10 [4]/DFF14 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_10 [3:0]
	1225			
	1226			
	1227			
	1228			
	1229			
	1230			
	1231			
0x9A	1232	REG_CNT2_D[7:0]	R/W	Data[7:0]
	1233			
	1234			
	1235			
	1236			
	1237			
	1238			
	1239			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x9B	1240	Multi3_LUT3_DFF setting	R/W	[7]:LUT3_11 [7]/DFF15 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_11[6]/DFF15 Output Select 0: Q output, 1: QB output [5]:LUT3_11 [5]/DFF15 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_11 [4]/DFF15 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_11 [3:0]
	1241			
	1242			
	1243			
	1244			
	1245			
	1246			
	1247			
0x9C	1248	REG_CNT3_D[7:0]	R/W	Data[7:0]
	1249			
	1250			
	1251			
	1252			
	1253			
	1254			
	1255			
0x9D	1256	Multi4_LUT3_DFF setting	R/W	[7]:LUT3_12 [7]/DFF16 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_12[6]/DFF16 Output Select 0: Q output, 1: QB output [5]:LUT3_12 [5]/DFF16 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_12 [4]/DFF16 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_12 [3:0]
	1257			
	1258			
	1259			
	1260			
	1261			
	1262			
	1263			
0x9E	1264	REG_CNT4_D[7:0]	R/W	Data[7:0]
	1265			
	1266			
	1267			
	1268			
	1269			
	1270			
	1271			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x9F	1272	Multi5_LUT3_DFF setting	R/W	[7]:LUT3_13 [7]/DFF17 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_13[6]/DFF17 Output Select 0: Q output, 1: QB output [5]:LUT3_13 [5]/DFF17 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_13 [4]/DFF17 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_13 [3:0]
	1273			
	1274			
	1275			
	1276			
	1277			
	1278			
	1279			
0xA0	1280	REG_CNT5_D[7:0]	R/W	Data[7:0]
	1281			
	1282			
	1283			
	1284			
	1285			
	1286			
	1287			
0xA1	1288	Multi6_LUT3_DFF setting	R/W	[7]:LUT3_14 [7]/DFF18 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_14[6]/DFF18 Output Select 0: Q output, 1: QB output [5]:LUT3_14 [5]/DFF18 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_14 [4]/DFF18 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_14 [3:0]
	1289			
	1290			
	1291			
	1292			
	1293			
	1294			
	1295			
0xA2	1296	REG_CNT6_D[7:0]	R/W	Data[7:0]
	1297			
	1298			
	1299			
	1300			
	1301			
	1302			
	1303			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA3	1304 1305 1306 1307 1308 1309 1310 1311	Multi7_LUT3_DFF setting	R/W	[7]:LUT3_15 [7]/DFF19 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_15[6]/DFF19 Output Select 0: Q output, 1: QB output [5]:LUT3_15 [5]/DFF19 0: nRST from Matrix Output, 1: nSET from Matrix Output [4]:LUT3_15 [4]/DFF19 Initial Polarity Select 0: Low, 1: High [3:0]:LUT3_15 [3:0]
0xA4	1312 1313 1314 1315 1316 1317 1318 1319	REG_CNT7_D[7:0]	R/W	Data[7:0]
0xA5	1320 1321 1322 1323 1324 1325 1326 1327	CNT0 (16bits) Counted Value	R	Virtual Input
0xA6	1328 1329 1330 1331 1332 1333 1334 1335		R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA7	1336	CNT6 (8bits) Counted Value	R	Virtual Input
	1337			
	1338			
	1339			
	1340			
	1341			
	1342			
	1343			
0xA8	1344	CNT7 (8bits) Counted Value	R	Virtual Input
	1345			
	1346			
	1347			
	1348			
	1349			
	1350			
	1351			
0xA9	1352	LUT3_1_DFF4 setting	R/W	[7]:LUT3_1 [7]/DFF4 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_1 [6]/DFF4 Output Select 0: Q output, 1: QB output [5]:LUT3_1 [5]/DFF4 Initial Polarity Select 0: Low, 1: High [4]:LUT3_1 [4]/DFF4 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_1 [3]/DFF4 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_1 [2:0]
	1353			
	1354			
	1355			
	1356			
	1357			
	1358			
	1359			
0xAA	1360	LUT3_2_DFF5 setting	R/W	[7]:LUT3_2 [7]/DFF5 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_2 [6]/DFF5 Output Select 0: Q output, 1: QB output [5]:LUT3_2 [5]/DFF5 Initial Polarity Select 0: Low, 1: High [4]:LUT3_2 [4]/DFF5 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_2 [3]/DFF5 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_2 [2:0]
	1361			
	1362			
	1363			
	1364			
	1365			
	1366			
	1367			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xAB	1368	LUT3_3_DFF6 setting	R/W	[7]:LUT3_3 [7]/DFF6 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_3 [6]/DFF6 Output Select 0: Q output, 1: QB output [5]:LUT3_3 [5]/DFF6 Initial Polarity Select 0: Low, 1: High [4]:LUT3_3 [4]/DFF6 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_3 [3]/DFF6 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_3 [2:0]
	1369			
	1370			
	1371			
	1372			
	1373			
	1374			
	1375			
0xAC	1376	LUT3_4_DFF7 setting	R/W	[7]:LUT3_4 [7]/DFF7 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_4 [6]/DFF7 Output Select 0: Q output, 1: QB output [5]:LUT3_4 [5]/DFF7 Initial Polarity Select 0: Low, 1: High [4]:LUT3_4 [4]/DFF7 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_4 [3]/DFF7 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_4 [2:0]
	1377			
	1378			
	1379			
	1380			
	1381			
	1382			
	1383			
0xAD	1384	LUT2_3_VAL or PGen_data	R/W	LUT2_3[3:0] or PGen 4bit counter data[3:0]
	1385		R/W	
	1386		R/W	
	1387		R/W	
	1388	LUT3_1 or DFF4 Select	R/W	0: LUT3_1 1: DFF4
	1389	LUT3_2 or DFF5 Select	R/W	0: LUT3_2 1: DFF5
	1390	LUT3_3 or DFF6 Select	R/W	0: LUT3_3 1: DFF6
	1391	LUT3_4 or DFF7 Select	R/W	0: LUT3_4 1: DFF7

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xAE	1392	PGen data	R/W	PGen Data[15:0]
	1393		R/W	
	1394		R/W	
	1395		R/W	
	1396		R/W	
	1397		R/W	
	1398		R/W	
	1399		R/W	
0xAF	1400		R/W	
	1401		R/W	
	1402		R/W	
	1403		R/W	
	1404		R/W	
	1405		R/W	
	1406		R/W	
	1407		R/W	
0xB0	1408	LUT2_3 or PGen Select	R/W	0: LUT2_3 1: PGen
	1409	Active level selection for RST/SET for LUT2_3 or PGen	R/W	0: Active low level reset/set 1: Active high level reset/set
	1410	Active level selection for RST/SET for LUT3_16 or Pipe Delay/RIPP CNT	R/W	0: Active low level reset/set 1: Active high level reset/set
	1411	Out of LUT3_16 or Out0 of Pipe Delay/RIPP CNT Select	R/W	0: LUT3_16 1: OUT0 of Pipe Delay or RIPP CNT
	1412	PIPE_RIPP_CNT_S	R/W	0: Pipe delay mode selection 1: Ripple Counter mode selection
	1413	Pipe Delay OUT1 Polarity Select	R/W	0: Non-inverted 1: Inverted
	1414	LUT4_0 or DFF12 Select	R/W	0: LUT4_0 1: DFF12
	1415	LUT3_0 or DFF3 Select	R/W	0: LUT3_0 1: DFF3

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB1	1416	LUT value or pipe delay out sel or nSET/END value	R/W	[7:4]: LUT3_8 [7:4]/REG_S1[3:0] pipe delay out1 sel [3:0]: LUT3_8 [3:0]/REG_S0[3:0] pipe delay out0 sel at RIPP CNT mode: bit[1418:1416] is the nSET value bit[1421:1419] is the END value bit[1422] is the range control: 0 full cycle, 1 range cycle bit[1423] Not used
	1417		R/W	
	1418		R/W	
	1419		R/W	
	1420		R/W	
	1421		R/W	
	1422		R/W	
	1423		R/W	
0xB2	1424	LUT4_0_DFF12 setting	R/W	[15]:LUT4_0 [15]/DFF12 or LATCH Select 0: DFF function, 1: LATCH function [14]:LUT4_0 [14]/DFF12 Output Select 0: Q output, 1: QB output [13]:LUT4_0 [13]/DFF12 Initial Polarity Select 0: Low, 1: High [12]:LUT4_0 [12]/DFF12 stage selection 0: Q of first DFF; 1 Q of second DFF [11]:LUT4_0 [11]/DFF12 0: nRST from Matrix Output, 1: nSET from Matrix Output [10]:LUT4_0 [10]/DFF12 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [9:0]: LUT4_0 [9:0]
	1425		R/W	
	1426		R/W	
	1427		R/W	
	1428		R/W	
	1429		R/W	
	1430		R/W	
	1431		R/W	
0xB3	1432		R/W	
	1433		R/W	
	1434		R/W	
	1435		R/W	
	1436		R/W	
	1437		R/W	
	1438		R/W	
	1439		R/W	
0xB4	1440	LUT3_0_DFF3 setting	R/W	[7]:LUT3_0 [7]/DFF3 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_0 [6]/DFF3 Output Select 0: Q output, 1: QB output [5]:LUT3_0 [5]/DFF3 Initial Polarity Select 0: Low, 1: High [4]:LUT3_0 [4]/DFF3stage selection 0: Q of first DFF; 1 Q of second DFF [3]:LUT3_0 [3]/DFF3 0: nRST from Matrix Output, 1: nSET from Matrix Output [2]:LUT3_0 [2]/DFF3 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [1:0]: LUT3_0 [1:0]
	1441		R/W	
	1442		R/W	
	1443		R/W	
	1444		R/W	
	1445		R/W	
	1446		R/W	
	1447		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB5	1448	Filter or Edge Detector selection	R/W	0, filter 1, edge det
	1449	Output Polarity Select	R/W	0: output non-invert 1: output invert
	1450	Select the edge mode	R/W	00: Rising Edge Det 01: Falling Edge Det 10: Both Edge Det 11: Both Edge DLY
	1451		R/W	
	1452	Delay Value Select for Programmable Delay & Edge Detector	R/W	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
	1453		R/W	
	1454	Select the Edge Mode of Programmable Delay & Edge Detector	R/W	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
	1455		R/W	
0xB6	1456	LUT3_5_DFF8 setting	R/W	[7]:LUT3_5 [7]/DFF8 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_5 [6]/DFF8 Output Select 0: Q output, 1: QB output [5]:LUT3_5 [5]/DFF8 Initial Polarity Select 0: Low, 1: High [4]:LUT3_5 [4]/DFF8 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_5 [3]/DFF8 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_5 [2:0]
	1457		R/W	
	1458		R/W	
	1459		R/W	
	1460		R/W	
	1461		R/W	
	1462		R/W	
	1463		R/W	
0xB7	1464	LUT3_6_DFF9 setting	R/W	[7]:LUT3_6 [7]/DFF9 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_6 [6]/DFF9 Output Select 0: Q output, 1: QB output [5]:LUT3_6 [5]/DFF9 Initial Polarity Select 0: Low, 1: High [4]:LUT3_6 [4]/DFF9 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_6 [3]/DFF9 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_6 [2:0]
	1465		R/W	
	1466		R/W	
	1467		R/W	
	1468		R/W	
	1469		R/W	
	1470		R/W	
	1471		R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB8	1472	LUT3_7_DFF10 setting	R/W	[7]:LUT3_7 [7]/DFF10 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_7 [6]/DFF10 Output Select 0: Q output, 1: QB output [5]:LUT3_7 [5]/DFF10 Initial Polarity Select 0: Low, 1: High [4]:LUT3_7 [4]/DFF10 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_7 [3]/DFF10 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_7 [2:0]
	1473		R/W	
	1474		R/W	
	1475		R/W	
	1476		R/W	
	1477		R/W	
	1478		R/W	
	1479		R/W	
0xB9	1480	LUT3_8_DFF11 setting	R/W	[7]:LUT3_8 [7]/DFF11 or LATCH Select 0: DFF function, 1: LATCH function [6]:LUT3_8 [6]/DFF11 Output Select 0: Q output, 1: QB output [5]:LUT3_8 [5]/DFF11 Initial Polarity Select 0: Low, 1: High [4]:LUT3_8 [4]/DFF11 0: nRST from Matrix Output, 1: nSET from Matrix Output [3]:LUT3_8 [3]/DFF11 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set [2:0]: LUT3_8 [2:0]
	1481		R/W	
	1482		R/W	
	1483		R/W	
	1484		R/W	
	1485		R/W	
	1486		R/W	
	1487		R/W	
0xBA	1488	LUT2_0 or DFF0 Select	R/W	0: LUT2_0 1: DFF0
	1489	LUT2_1 or DFF1 Select	R/W	0: LUT2_1 1: DFF1
	1490	LUT2_2 or DFF2 Select	R/W	0: LUT2_2 1: DFF2
	1491	Reserved	R/W	
	1492	LUT3_5 or DFF8 Select	R/W	0: LUT3_5 1: DFF8
	1493	LUT3_6 or DFF9 Select	R/W	0: LUT3_6 1: DFF9
	1494	LUT3_7 or DFF10 Select	R/W	0: LUT3_7 1: DFF10
	1495	LUT3_8 or DFF11 Select	R/W	0: LUT3_8 1: DFF11

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xBB	1496	LUT2_0/DFF0 setting	R/W	[3]:LUT2_0 [3]/DFF0 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_0 [2]/DFF0 Output Select 0: Q output, 1: QB output [1]:LUT2_0 [1]/DFF0 Initial Polarity Select 0: Low, 1: High [0]:LUT2_0 [0]
	1497		R/W	
	1498		R/W	
	1499		R/W	
	1500	LUT2_1/DFF1 setting	R/W	[3]:LUT2_1 [3]/DFF1 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_1 [2]/DFF1 Output Select 0: Q output, 1: QB output [1]:LUT2_1 [1]/DFF1 Initial Polarity Select 0: Low, 1: High [0]:LUT2_1 [0]
	1501		R/W	
	1502		R/W	
	1503		R/W	
0xBC	1504	LUT2_2/DFF2 setting	R/W	[3]:LUT2_2 [3]/DFF2 or LATCH Select 0: DFF function, 1: LATCH function [2]:LUT2_2 [2]/DFF2 Output Select 0: Q output, 1: QB output [1]:LUT2_2 [1]/DFF2 Initial Polarity Select 0: Low, 1: High [0]:LUT2_2 [0]
	1505		R/W	
	1506		R/W	
	1507		R/W	
	1508	Reserved	R/W	
	1509		R/W	
	1510		R/W	
	1511		R/W	
0xBD	1512		R/W	
	1513		R/W	
	1514		R/W	
	1515		R/W	
	1516		R/W	
	1517		R/W	
	1518		R/W	
	1519		R/W	
0xBE	1520	Reserved	R/W	
	1521	Reserved	R/W	
	1522	Reserved	R/W	
	1523	Reserved	R/W	
	1524	Reserved	R/W	
	1525			
	1526			
	1527			

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xBF	1528	Reserved	R/W	
	1529	Reserved	R/W	
	1530	Reserved	R/W	
	1531	Reserved	R/W	
	1532	Reserved	R/W	
	1533	Reserved	R/W	
	1534	Reserved	R/W	
	1535	Reserved	R/W	
0xC0	1536	Reserved	R/W	
	1537	Reserved	R/W	
	1538	Reserved	R/W	
	1539	Reserved	R/W	
	1540	Reserved	R/W	
	1541	Reserved	R/W	
	1542	Reserved	R/W	
	1543	Reserved	R/W	
0xC1	1544	Reserved	R/W	
	1545	Reserved	R/W	
	1546	Reserved	R/W	
	1547	Reserved	R/W	
	1548	Reserved	R/W	
	1549	Reserved	R/W	
	1550	Reserved	R/W	
	1551	Reserved	R/W	
0xC2	1552	Reserved	R	
	1553	Reserved	R	
	1554	Reserved	R	
	1555	Reserved	R	
	1556	Reserved	R	
	1557	Reserved	R	
	1558	Reserved	R	
	1559	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xC3	1560	Reserved	R	
	1561	Reserved	R	
	1562	Reserved	R	
	1563	Reserved	R	
	1564	Reserved	R	
	1565	Reserved	R	
	1566	Reserved	R	
	1567	Reserved	R	
0xC4	1568	Reserved	R	
	1569	Reserved	R	
	1570	Reserved	R	
	1571	Reserved	R	
	1572	Reserved	R	
	1573	Reserved	R	
	1574	Reserved	R	
	1575	Reserved	R	
0xC5	1576	Reserved	R	
	1577	Reserved	R	
	1578	Reserved	R	
	1579	Reserved	R	
	1580	Reserved	R	
	1581	Reserved	R	
	1582	Reserved	R	
	1583	Reserved	R	
0xC6	1584	Reserved	R	
	1585	Reserved	R	
	1586	Reserved	R	
	1587	Reserved	R	
	1588	Reserved	R	
	1589	Reserved	R	
	1590	Reserved	R	
	1591	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xC7	1592	Reserved	R	
	1593	Reserved	R	
	1594	Reserved	R	
	1595	Reserved	R	
	1596	Reserved	R	
	1597	Reserved	R	
	1598	Reserved	R	
	1599	Reserved	R	
0xC8	1600	Reserved	R	
	1601	Reserved	R	
	1602	Reserved	R	
	1603	Reserved	R	
	1604	Reserved	R	
	1605	Reserved	R	
	1606	Reserved	R	
	1607	Reserved	R	
0xC9	1608	Reserved	R	
	1609	Reserved	R	
	1610	Reserved	R	
	1611	Reserved	R	
	1612	Reserved	R	
	1613	Reserved	R	
	1614	Reserved	R	
	1615	Reserved	R	
0xCA	1616	Reserved	R	
	1617	Reserved	R	
	1618	Reserved	R	
	1619	Reserved	R	
	1620	Reserved	R	
	1621	Reserved	R	
	1622	Reserved	R	
	1623	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xCB	1624	Reserved	R	
	1625	Reserved	R	
	1626	Reserved	R	
	1627	Reserved	R	
	1628	Reserved	R	
	1629	Reserved	R	
	1630	Reserved	R	
	1631	Reserved	R	
0xCC	1632	Reserved	R	
	1633	Reserved	R	
	1634	Reserved	R	
	1635	Reserved	R	
	1636	Reserved	R	
	1637	Reserved	R	
	1638	Reserved	R	
	1639	Reserved	R	
0xCD	1640	Reserved	R	
	1641	Reserved	R	
	1642	Reserved	R	
	1643	Reserved	R	
	1644	Reserved	R	
	1645	Reserved	R	
	1646	Reserved	R	
	1647	Reserved	R	
0xCE	1648	Reserved	R	
	1649	Reserved	R	
	1650	Reserved	R	
	1651	Reserved	R	
	1652	Reserved	R	
	1653	Reserved	R	
	1654	Reserved	R	
	1655	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xCF	1656	Reserved	R	
	1657	Reserved	R	
	1658	Reserved	R	
	1659	Reserved	R	
	1660	Reserved	R	
	1661	Reserved	R	
	1662	Reserved	R	
	1663	Reserved	R	
0xD0	1664	Reserved	R	
	1665	Reserved	R	
	1666	Reserved	R	
	1667	Reserved	R	
	1668	Reserved	R	
	1669	Reserved	R	
	1670	Reserved	R	
	1671	Reserved	R	
0xD1	1672	Reserved	R	
	1673	Reserved	R	
	1674	Reserved	R	
	1675	Reserved	R	
	1676	Reserved	R	
	1677	Reserved	R	
	1678	Reserved	R	
	1679	Reserved	R	
0xD2	1680	Reserved	R	
	1681	Reserved	R	
	1682	Reserved	R	
	1683	Reserved	R	
	1684	Reserved	R	
	1685	Reserved	R	
	1686	Reserved	R	
	1687	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xD3	1688	Reserved	R	
	1689	Reserved	R	
	1690	Reserved	R	
	1691	Reserved	R	
	1692	Reserved	R	
	1693	Reserved	R	
	1694	Reserved	R	
	1695	Reserved	R	
0xD4	1696	Reserved	R	
	1697	Reserved	R	
	1698	Reserved	R	
	1699	Reserved	R	
	1700	Reserved	R	
	1701	Reserved	R	
	1702	Reserved	R	
	1703	Reserved	R	
0xD5	1704	Reserved	R	
	1705	Reserved	R	
	1706	Reserved	R	
	1707	Reserved	R	
	1708	Reserved	R	
	1709	Reserved	R	
	1710	Reserved	R	
	1711	Reserved	R	
0xD6	1712	Reserved	R	
	1713	Reserved	R	
	1714	Reserved	R	
	1715	Reserved	R	
	1716	Reserved	R	
	1717	Reserved	R	
	1718	Reserved	R	
	1719	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xD7	1720	Reserved	R	
	1721	Reserved	R	
	1722	Reserved	R	
	1723	Reserved	R	
	1724	Reserved	R	
	1725	Reserved	R	
	1726	Reserved	R	
	1727	Reserved	R	
0xD8	1728	Reserved	R	
	1729	Reserved	R	
	1730	Reserved	R	
	1731	Reserved	R	
	1732	Reserved	R	
	1733	Reserved	R	
	1734	Reserved	R	
	1735	Reserved	R	
0xD9	1736	Reserved	R	
	1737	Reserved	R	
	1738	Reserved	R	
	1739	Reserved	R	
	1740	Reserved	R	
	1741	Reserved	R	
	1742	Reserved	R	
	1743	Reserved	R	
0xDA	1744	Reserved	R	
	1745	Reserved	R	
	1746	Reserved	R	
	1747	Reserved	R	
	1748	Reserved	R	
	1749	Reserved	R	
	1750	Reserved	R	
	1751	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xDB	1752	Reserved	R	
	1753	Reserved	R	
	1754	Reserved	R	
	1755	Reserved	R	
	1756	Reserved	R	
	1757	Reserved	R	
	1758	Reserved	R	
	1759	Reserved	R	
0xDC	1760	Reserved	R	
	1761	Reserved	R	
	1762	Reserved	R	
	1763	Reserved	R	
	1764	Reserved	R	
	1765	Reserved	R	
	1766	Reserved	R	
	1767	Reserved	R	
0xDD	1768	Reserved	R	
	1769	Reserved	R	
	1770	Reserved	R	
	1771	Reserved	R	
	1772	Reserved	R	
	1773	Reserved	R	
	1774	Reserved	R	
	1775	Reserved	R	
0xDE	1776	Reserved	R	
	1777	Reserved	R	
	1778	Reserved	R	
	1779	Reserved	R	
	1780	Reserved	R	
	1781	Reserved	R	
	1782	Reserved	R	
	1783	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xDF	1784	Reserved	R	
	1785	Reserved	R	
	1786	Reserved	R	
	1787	Reserved	R	
	1788	Reserved	R	
	1789	Reserved	R	
	1790	Reserved	R	
	1791	Reserved	R	
0xE0	1792	Reserved	R	
	1793	Reserved	R	
	1794	Reserved	R	
	1795	Reserved	R	
	1796	Reserved	R	
	1797	Reserved	R	
	1798	Reserved	R	
	1799	Reserved	R	
0xE1	1800	Reserved	R	
	1801	Reserved	R	
	1802	Reserved	R	
	1803	Reserved	R	
	1804	Reserved	R	
	1805	Reserved	R	
	1806	Reserved	R	
	1807	Reserved	R	
0xE2	1808	Reserved	R	
	1809	Reserved	R	
	1810	Reserved	R	
	1811	Reserved	R	
	1812	Reserved	R	
	1813	Reserved	R	
	1814	Reserved	R	
	1815	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xE3	1816	Reserved	R	
	1817	Reserved	R	
	1818	Reserved	R	
	1819	Reserved	R	
	1820	Reserved	R	
	1821	Reserved	R	
	1822	Reserved	R	
	1823	Reserved	R	
0xE4	1824	Reserved	R	
	1825	Reserved	R	
	1826	Reserved	R	
	1827	Reserved	R	
	1828	Reserved	R	
	1829	Reserved	R	
	1830	Reserved	R	
	1831	Reserved	R	
0xE5	1832	Reserved	R	
	1833	Reserved	R	
	1834	Reserved	R	
	1835	Reserved	R	
	1836	Reserved	R	
	1837	Reserved	R	
	1838	Reserved	R	
	1839	Reserved	R	
0xE6	1840	Reserved	R	
	1841	Reserved	R	
	1842	Reserved	R	
	1843	Reserved	R	
	1844	Reserved	R	
	1845	Reserved	R	
	1846	Reserved	R	
	1847	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xE7	1848	Reserved	R	
	1849	Reserved	R	
	1850	Reserved	R	
	1851	Reserved	R	
	1852	Reserved	R	
	1853	Reserved	R	
	1854	Reserved	R	
	1855	Reserved	R	
0xE8	1856	Reserved	R	
	1857	Reserved	R	
	1858	Reserved	R	
	1859	Reserved	R	
	1860	Reserved	R	
	1861	Reserved	R	
	1862	Reserved	R	
	1863	Reserved	R	
0xE9	1864	Reserved	R	
	1865	Reserved	R	
	1866	Reserved	R	
	1867	Reserved	R	
	1868	Reserved	R	
	1869	Reserved	R	
	1870	Reserved	R	
	1871	Reserved	R	
0xEA	1872	Reserved	R	
	1873	Reserved	R	
	1874	Reserved	R	
	1875	Reserved	R	
	1876	Reserved	R	
	1877	Reserved	R	
	1878	Reserved	R	
	1879	Reserved	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xEB	1880	Reserved	R	
	1881	Reserved	R	
	1882	Reserved	R	
	1883	Reserved	R	
	1884	Reserved	R	
	1885	Reserved	R	
	1886	Reserved	R	
	1887	Reserved	R	
0xEC	1888	Reserved	R/W	
	1889	Reserved	R/W	
	1890	Reserved	R/W	
	1891	Reserved	R/W	
	1892	Reserved	R/W	
	1893	Reserved	R/W	
	1894	Reserved	R/W	
	1895	Reserved	R/W	
0xED	1896	Reserved	R/W	
	1897	Reserved	R/W	
	1898	Reserved	R/W	
	1899	Reserved	R/W	
	1900	Reserved	R/W	
	1901	Reserved	R/W	
	1902	Reserved	R/W	
	1903	Reserved	R/W	
0xEE	1904	Reserved	R/W	
	1905	Reserved	R/W	
	1906	Reserved	R/W	
	1907	Reserved	R/W	
	1908	Reserved	R/W	
	1909	Reserved	R/W	
	1910	Reserved	R/W	
	1911	Reserved	R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xEF	1912	Reserved	R/W	
	1913	Reserved	R/W	
	1914	Reserved	R/W	
	1915	Reserved	R/W	
	1916	Reserved	R/W	
	1917	Reserved	R/W	
	1918	Reserved	R/W	
	1919	Reserved	R/W	
0xF0	1920	Reserved	R/W	
	1921	Reserved	R/W	
	1922	Reserved	R/W	
	1923	Reserved	R/W	
	1924	Reserved	R/W	
	1925	Reserved	R/W	
	1926	Reserved	R/W	
	1927	Reserved	R/W	
0xF1	1928	Reserved	R/W	
	1929	Reserved	R/W	
	1930	Reserved	R/W	
	1931	Reserved	R/W	
	1932	Reserved	R/W	
	1933	Reserved	R/W	
	1934	Reserved	R/W	
	1935	Reserved	R/W	
0xF2	1936	Reserved	R/W	
	1937	Reserved	R/W	
	1938	Reserved	R/W	
	1939	Reserved	R/W	
	1940	Reserved	R/W	
	1941	Reserved	R/W	
	1942	Reserved	R/W	
	1943	Reserved	R/W	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xF3	1944	Reserved	R/W	
	1945	Reserved	R/W	
	1946	Reserved	R/W	
	1947	Reserved	R/W	
	1948	Reserved	R/W	
	1949	Reserved	R/W	
	1950	Reserved	R/W	
	1951	Reserved	R/W	
0xF4	1952	GPO0 I^2C output expander data	R/W	
	1953	GPO0 I^2C output expander select	R/W	0: GPO0 output come from matrix 1: GPO0 output is register
	1954	GPIO6 I^2C output expander data	R/W	
	1955	GPIO6 I^2C output expander select	R/W	0: GPIO6 output come from matrix 1: GPIO6 output is register
	1956	GPIO7 I^2C output expander data	R/W	
	1957	GPIO7 I^2C output expander select	R/W	0: GPIO7 output come from matrix 1: GPIO7 output is register
	1958	GPIO8 I^2C output expander data	R/W	
	1959	GPIO8 I^2C output expander select	R/W	0: GPIO8 output come from matrix 1: GPIO8 output is register
0xF5	1960	I^2C reset bit with reloading NVM into Data register (soft reset)	R	0: Keep existing condition 1: Reset execution
	1961	IO Latching Enable During I^2C Write Interface	R	0: Disable 1: Enable
	1962	Reserved	R	
	1963	Protect mode enable	R	0: Disable 1: Enable
	1964	Reserved	R	
	1965	Register protection mode bit 0	R	000: all open read/write (mode 0); 001: partly lock read (mode 1); 010: partly lock read2 (mode 2); 011: partly lock read2/write (mode 3); 100: all lock read (mode 4); 101: all lock write (mode 5); 110: all lock read/write (mode 6).
	1966	Register protection mode bit 1	R	
	1967	Register protection mode bit 2	R	

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xF6	1968	Reserved I^2C write mask bits	R/W	0: overwrite 1: mask
	1969		R/W	
	1970		R/W	
	1971		R/W	
	1972		R/W	
	1973		R/W	
	1974		R/W	
	1975		R/W	
0xF7	1976	Reserved	R	
	1977		R	
	1978		R	
	1979		R	
	1980		R	
	1981		R	
	1982		R	
	1983		R	
0xF8	1984	Reserved	R	
	1985		R	
	1986		R	
	1987		R	
	1988		R	
	1989		R	
	1990		R	
	1991		R	
0xF9	1992	Reserved	R	
	1993	Reserved	R	
	1994	Reserved	R	
	1995		R	
	1996	Reserved	R	
	1997		R	
	1998		R	
	1999		R	

Table 55. Register Map (Cont.)

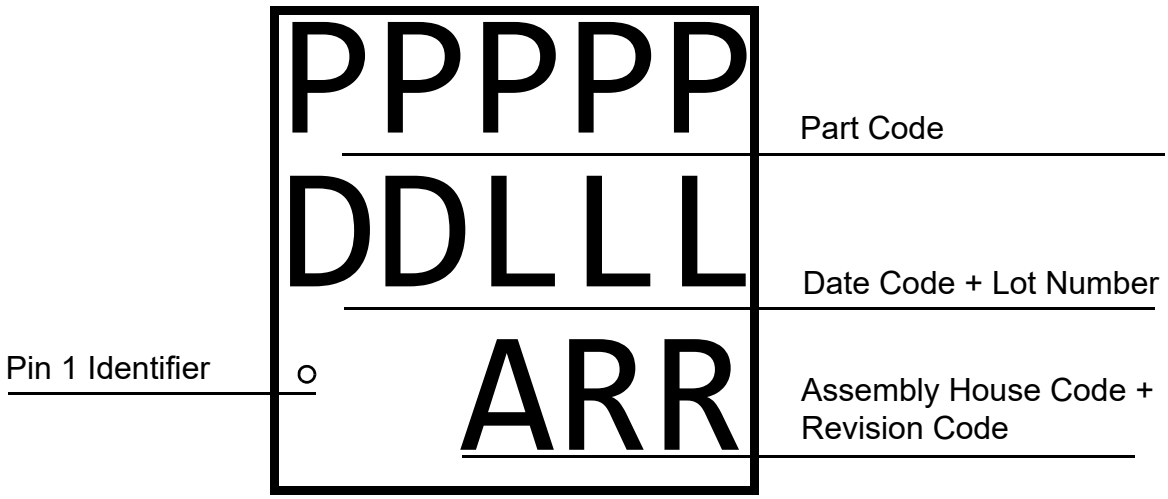
Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xFA	2000	8-bit Pattern ID Byte 0 (from NVM): ID[23:16]	R	
	2001		R	
	2002		R	
	2003		R	
	2004		R	
	2005		R	
	2006		R	
	2007		R	
0xFB	2008	Reserved	R	
	2009		R	
	2010		R	
	2011		R	
	2012		R	
	2013		R	
	2014		R	
	2015		R	
0xFC	2016	Reserved	R	
	2017		R	
	2018		R	
	2019		R	
	2020		R	
	2021		R	
	2022		R	
	2023		R	
0xFD	2024	I^2C slave address	R	
	2025		R	
	2026		R	
	2027		R	
	2028	Slave address selection bit0	R	0: from register [2024] 1: from GPI0
	2029	Slave address selection bit1	R	0: from register [2025] 1: from GPIO2
	2030	Slave address selection bit2	R	0: from register [2026] 1: from GPIO4
	2031	Slave address selection bit3	R	0: from register [2027] 1: from GPIO5

Table 55. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xFE	2032	I²C operation disable bit	R	0: I²C operation enable; matrix in 32(33) select I2C_virtual_0(1) Input 1: I²C operation disable; matrix in 32(33) select GPIO0(GPIO1) digital input
	2033	Reserved	R	
	2034	Reserved	R	
	2035	Reserved	R	
	2036	Reserved	R	
	2037	Reserved	R	
	2038	Reserved	R	
	2039	Reserved	R	
0xFF	2040	Reserved	R	
	2041		R	
	2042		R	
	2043		R	
	2044		R	
	2045		R	
	2046		R	
	2047		R	

18. Package Top Marking Definitions

18.1 STQFN 14L 3.0 mm x 3.1 mm 0.65P FCD

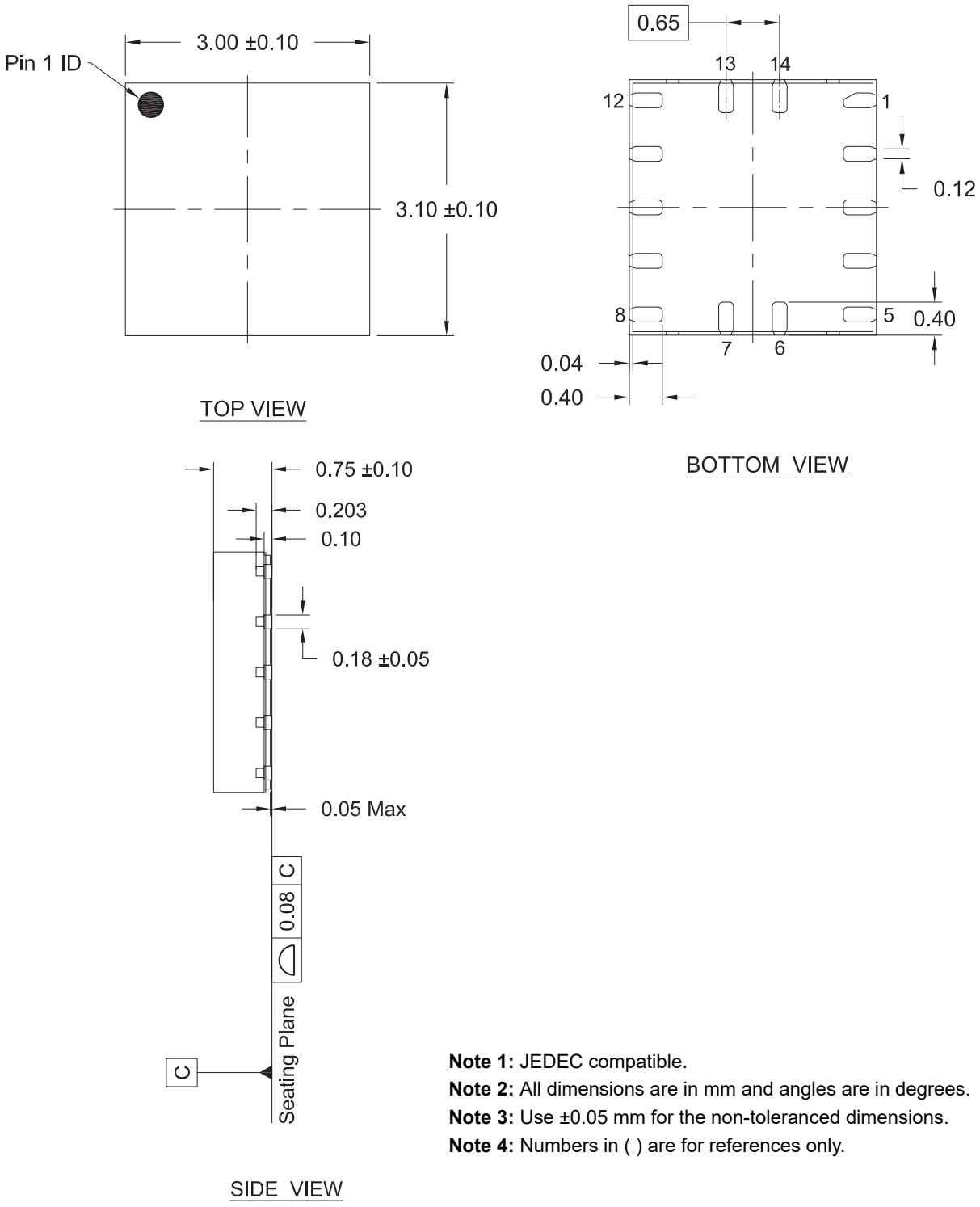


19. Package Information

19.1 Package Outlines for STQFN 14L 3.0 mm x 3.1 mm x 0.75 mm 0.65P FC Package

JEDEC MO-220

IC Net Weight: 0.016 g



Note 1: JEDEC compatible.
Note 2: All dimensions are in mm and angles are in degrees.
Note 3: Use ±0.05 mm for the non-toleranced dimensions.
Note 4: Numbers in ( ) are for references only.

Figure 115. STQFN 14L 3.0x3.1mm 0.65P FC Package

19.2 STQFN Handling

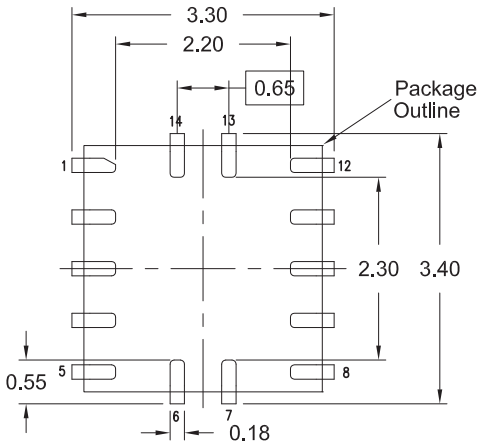
Be sure to handle STQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle STQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

19.3 Soldering Information

Please see IPC/JEDEC J-STD-020: latest revision for re-flow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at http://www.jedec.org.

20. Layout Guidelines

20.1 STQFN 14L 3.0 mm x 3.1 mm x 0.75 mm 0.65P FC Green Package



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

Unit: mm

21. Ordering Information

Part number	Type
SLG46857-AP	14-pin STQFN

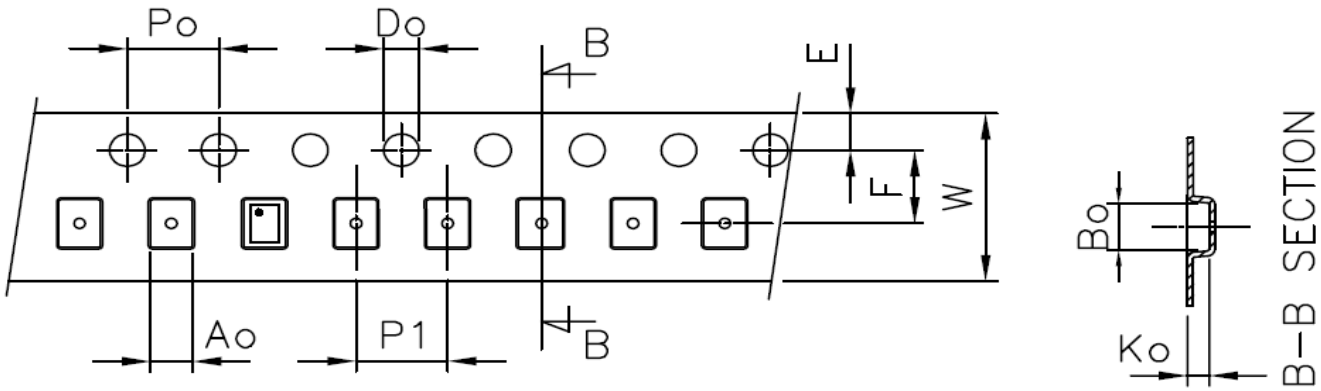
Note: Use SLG46857-AP to order. Shipments are automatically in Tape and Reel.

21.1 Tape and Reel Specifications

Package type	# of pins	Nominal Package size (mm)	Max units		Reel & Hub size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
STQFN 14L 3.0 mm x 3.1 mm 0.65P FC Green	14	3.0x3.1x0.75	5000	5000	330/102	42	336	42	336	12	8

21.2 Carrier Tape Drawing and Dimensions

Package type	Pocket BTM length (mm)	Pocket BTM width (mm)	Pocket depth (mm)	Index hole pitch (mm)	Pocket pitch (mm)	Index hole diameter (mm)	Index hole to tape edge (mm)	Index hole to pocket center (mm)	Tape width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 3.0 mm x 3.1 mm 0.65P FC Green	3.25	3.35	1.00	4.00	8.00	1.50	1.75	5.50	12.15



Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High Speed
ACMPL	Analog Comparator Low Power
ADAS	Advanced Driver Assistance Systems

B

BG	Bandgap

C

CLK	Clock
CMO	Connection matrix output
CMP	Comparator
CNT	Counter

D

DFF	D Flip-Flop
DLY	Delay

E

ESD	Electrostatic discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
IO	Input/Output

L

LPF	Low-pass Filter
LSB	Least Significant Bit

LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OD	Open-drain
OE	Output Enable
OSC	Oscillator
OTP	One Time Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-pull
PWR	Power
P DLY	Programmable Delay

R

R/W	Read/Write

S

SCL	I^2C Clock Input
SDA	I^2C Data Input/Output
SLA	Slave Address
SMT	With Schmitt trigger
SV	nSET Value

T

TS	Temperature Sensor

V

Vref	Voltage Reference

W

WOSMT	Without Schmitt trigger
WS	Wake and Sleep Controller

Revision History

Revision	Date	Description
1.00	Aug 6, 2024	Initial release

RoHS Compliance

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(Disclaimer Rev.5.0-1 October 2020)

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