Datasheet

SLG47004-A

Auto AEC-Q100 Qualified GreenPAK Programmable Mixed-Signal Matrix with In-System Debug and Advanced Analog Features

The SLG47004-A provides a small, low power component for commonly used analog signal processing and mixed-signal functions. Individual, tunable, analog components used in conjunction with configurable logic provide a way to solve a wide variety of tasks with minimal costs. The user creates their circuit design by programming the Non-Volatile Memory (NVM) to configure the interconnect logic, the analog and digital macrocell, and the IO Pins of the SLG47004-A.

Features

- Two Programmable Bandwidth Op Amps
  - 3-Op Amp Instrumentation Amplifier Function (including Additional Internal Op Amp)
  - Rail to Rail Input
  - Low Quiescent Current
  - Low Offset Voltage
  - Analog Comparator Mode
  - Optional Vref Voltage Connection for In put Pins
- Two 1024 Position Digital Rheostats
  - User Defined Auto-Trim Option
  - Manual Control Option
  - I^2C Control Option
  - Potentiometer Mode
- Two Single-Pole/Single-Throw Analog Switches
  - Voltage or Current Source/Sink Mode
- One Low Offset Chopper Comparator
- Two Low Power General Purpose ACMPs
  - ACMP Sampling Mode
  - Hysteresis with Independently-Selectable Thresholds
- Three Voltage References
  - Two ACMP Vref Output Buffers
  - One High Drive Buffer
- Thirteen Combination Function Macrocells
  - Three Selectable DFF/LATCH or 2-bit LUTs
  - One Selectable Programmable Pattern Generator or 2-bit LUT
  - Seven Selectable DFF/LATCH or 3-bit LUTs
  - One Selectable Pipe Delay or Ripple Counter or 3-bit LUT
  - One Selectable DFF/LATCH or 4-bit LUT
- Seven Multi-Function Macrocells
  - Six Selectable DFF/LATCH or 3-bit LUTs + 8-bit Delay/Counters
  - One Selectable DFF/LATCH or 4-bit LUT + 16-bit Delay/Counter
- Serial Communications
  - I^2C Protocol Interface
- Programmable Delay with Edge Detector Output
- Deglitch Filter or Edge Detector
- Three Oscillators
  - 2.048 kHz Oscillator
  - 2.048 MHz Oscillator
  - 25 MHz Oscillator
- Analog Temperature Sensor
- Power-On-Reset
- In-System Debug
- Multiple Time Programmable Memory in Development
- Wide Range Power Supply
  - 2.5 V (±4 %) to 5 V (±10 %) V_{DD}
- Ambient Operation Temperature Range: -40 °C to 125 °C
- RoHS Compliant/Halogen-Free
- Package Available
  - 24-pin TQFN: 4 mm x 4 mm x 0.75 mm, 0.5 mm pitch
- AEC-Q100 (T_A = -40 °C to 125 °C) Qualified

Applications

- Infotainment
- Navigation
- Automotive Display Clusters
- Chassis and Body Electronics
- Sensor Interface
- Electronic/Electrical Architecture

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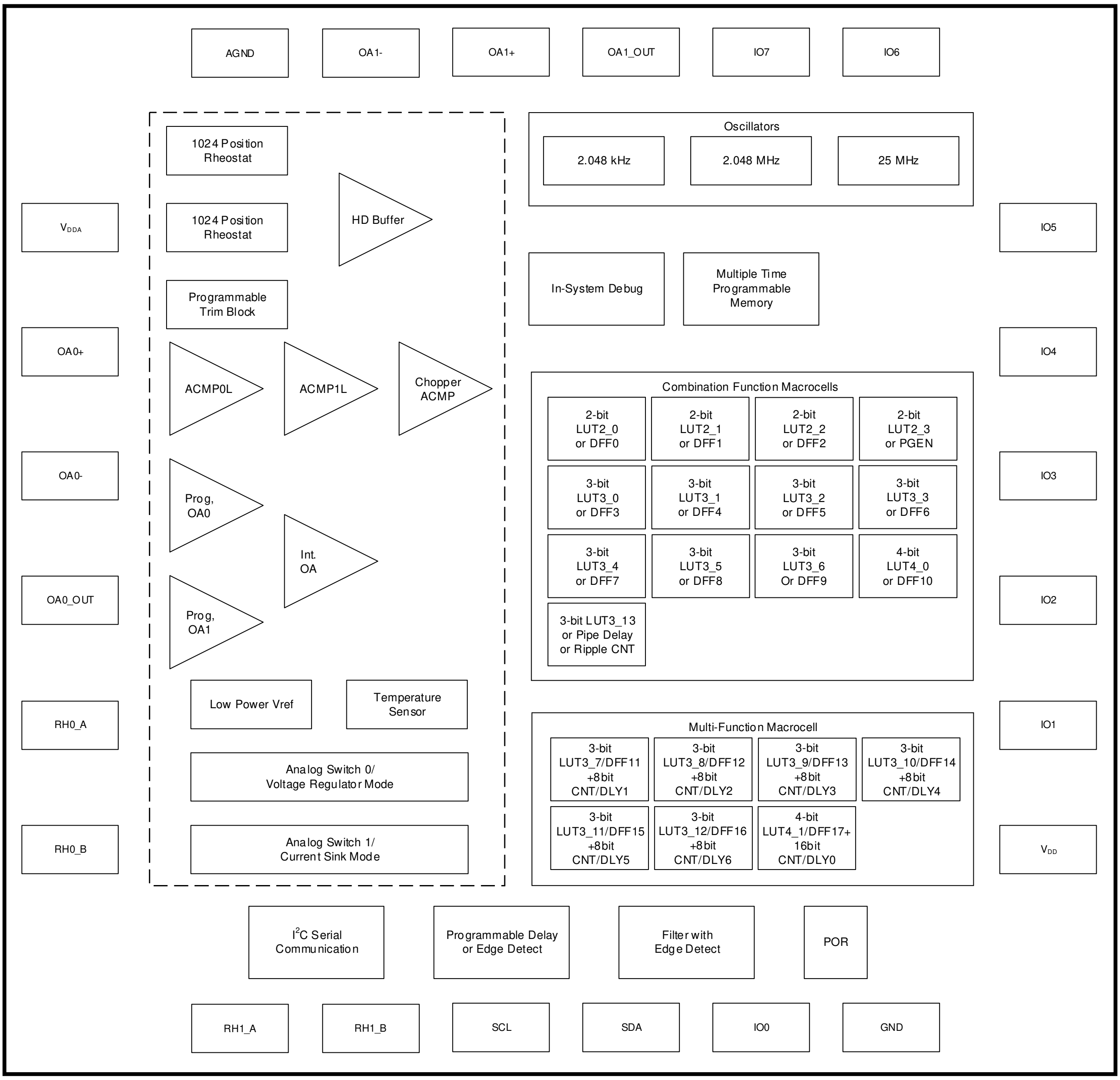


Figure 1. Block Diagram

2. Pin Information

2.1 Pin Assignments

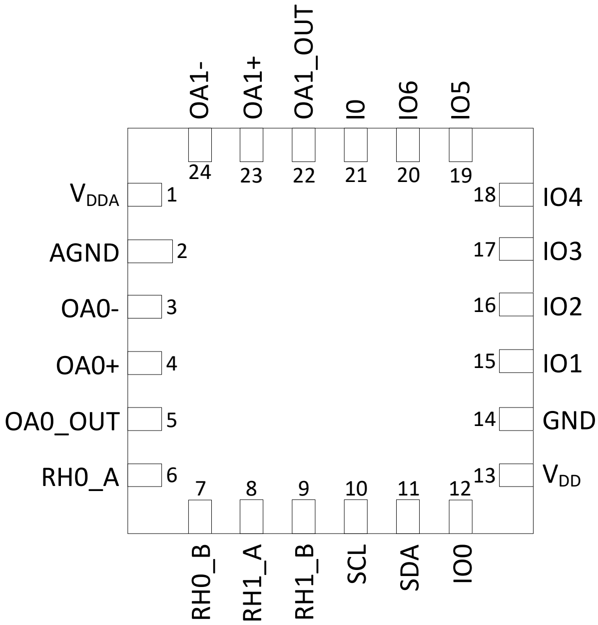


Figure 2. Pin Assignments - TQFN-24 (Top View)

2.2 Pin Descriptions

Table 1. Pin Description

Pin Number	Pin Name	Description
1	V_{DDA}	Analog Power Supply
2	AGND	Analog Ground
3	OA0-	Op Amp0 Inverting Input
4	OA0+	Op Amp0 Non-Inverting Input
5	OA0_OUT	Op Amp0_OUT/ACMP0L+
6	RH0_A	Digital Rheostat 0 Terminal A
7	RH0_B	Digital Rheostat 0 Terminal B
8	RH1_A	Digital Rheostat 1 Terminal A
9	RH1_B	Digital Rheostat 1 Terminal B
10	SCL	I^2C_SCL
11	SDA	I^2C_SDA
12	IO0	GPIO, ACMP0L-, ACMP1L-, EXT_OSC0_IN, Vref0_Out or Temp_Sens_Out
13	V_{DD}	Digital Power Supply
14	GND	Digital Ground
15	IO1	GPIO, Chop_ACMP+, Vref1_OUT or Temp_Sens_Out, EXT_OSC1_IN or SLA_0

Table 1. Pin Description (Cont.)

Pin Number	Pin Name	Description
16	IO2	GPIO, ACMP0L+, EXT_OSC2_IN, SLA_1
17	IO3	GPIO, AS_1_A, ACMP1L+ or SLA_2
18	IO4	GPIO, AS_1_B, Chop_ACMP-or SLA_3
19	IO5	GPIO, AS_0_B
20	IO6	GPIO, AS_0_A, HD_Buff_Out, In Amp_Vref
21	I0	GPI, In Amp_OUT
22	OA1_OUT	Op Amp1_OUT, ACMP1L+
23	OA1+	Op Amp1 Non-inverting Input
24	OA1-	Op Amp1 Inverting Input

Table 2. Functional Pin Description

Pin Number TQFN 24	Pin Name	Signal Name	Function	Input Options	Output Options
1	V_{DDA}	V_{DDA}	Analog Power Supply	--	--
2	AGND	AGND	Analog Ground	--	--
3	OA0-	OA0-	Op Amp0 Inverting Input	Analog	--
4	OA0+	OA0+	Op Amp0 Non-Inverting Input	Analog	--
5	OA0_OUT	OA0_OUT	Op Amp0 Output	--	Analog
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	--
6	RH0_A	RH0_A	Digital Rheostat 0 Terminal A	--	--
7	RH0_B	RH0_B	Digital Rheostat 0 Terminal B	--	--
8	RH1_A	RH1_A	Digital Rheostat 1 Terminal A	--	--
9	RH1_B	RH1_B	Digital Rheostat 1 Terminal B	--	--
10	SCL	SCL	I^2C Serial Clock	--	--
11	SDA	SDA	I^2C Serial Data	--	--
12	IO0	IO0	General Purpose IO	--	--
		ACMP0L-	Analog Comparator 0 Negative Input	Analog	--
		ACMP1L-	Analog Comparator 1 Negative Input	Analog	--
		EXT_OSC0_IN	External Clock Connection	--	--
		Vref0_Out	Voltage Reference 0 Output	--	Analog
		Temp_Sens_Out	Temperature Sensor Output	--	Analog

Table 2. Functional Pin Description (Cont.)

Pin Number TQFN 24	Pin Name	Signal Name	Function	Input Options	Output Options
13	V_{DD}	V_{DD}	Digital Power Supply	--	--
14	GND	GND	Digital Ground	--	--
15	IO1	IO1	General Purpose IO	--	--
		CHOP_ACMP+	Chopper ACMP Positive Input	Analog	--
		Temp_Sens_Out	Temperature Sensor Output	--	Analog
		EXT_OSC1_IN	External Clock Connection	--	--
		SLA_0	Slave Address 0	--	--
16	IO2	IO2	General Purpose IO	--	--
		ACMP0L+	Analog Comparator 0 Positive Input	Analog	--
		EXT_OSC2_IN	External Clock Connection	--	--
		SLA_1	Slave Address 1	--	--
17	IO3	IO3	General Purpose IO	--	--
		AS_1_A	Analog Switch 1 Input A	Analog	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	--	--
		SLA_2	Slave Address 2	--	--
18	IO4	IO4	General Purpose IO	--	--
		AS_1_B	Analog Switch 1 Input B	Analog	Analog
		CHOP_ACMP-	Chopper ACMP Negative Input	Analog	--
		SLA_3	Slave Address 3	--	--
19	IO5	IO5	General Purpose IO	--	--
		AS_0_B	Analog Switch 0 Input B	Analog	Analog
20	IO6	IO6	General Purpose IO	--	--
		AS_0_A	Analog Switch 0 Input A	Analog	Analog
		HD_Buffer_Out	High Drive Buffer Out put	--	Analog
		In Amp_Vref	Instrumentation Amplifier Voltage Reference	Analog	--
21	I0	I0	General Purpose Input	--	--
		In Amp Out	Instrumentation Amplifier Output	Analog	--

Table 2. Functional Pin Description (Cont.)

Pin Number TQFN 24	Pin Name	Signal Name	Function	Input Options	Output Options
22	OA1_OUT	OA1_OUT	Op Amp1 Output	--	Analog
		ACMP1L+	Analog Comparator 1 Positive Input	Analog	--
23	OA1+	OA1+	Op Amp1 Non-inverting Input	Analog	--
24	OA1-	OA1-	Op Amp1 Inverting Input	Analog	--

Table 3. Pin Type Definitions

Pin type	Definition
V_{DDA}	Analog Power Supply
AGND	Analog Ground
OA-	Op Amp Inverting Input
OA+	Op Amp Non-Inverting Input
OA_OUT	Op Amp Output
RH_A	Digital Rheostat Terminal A
RH_B	Digital Rheostat Terminal B
SCL	I^2C Serial Clock
SDA	I^2C Serial Data
IO	General Purpose Input/Output
V_{DD}	Digital Power Supply
GND	Digital Ground
I	General Purpose Input

3. Specifications

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Analog and digital grounds must be connected together on the PCB board. The place of connection depends on users schematic. For application cases with low digital current of SLG47004-A, both AGND and GND should be connected to analog ground plane.

Table 4. Absolute Maximum Ratings

Parameter		Min	Max	Unit
V_{DD} to GND, V_{DDA} to AGND[1]		-0.3	7	V
Maximum Slew Rate of V_{DDA}		--	2	V/µs
Voltage at Input Pin		GND-0.3	V_{DD}+0.3	V
Current at Input Pin		-1.0	1.0	mA
Maximum Average Current through V_{DD} and V_{DDA}	T_J = 85 °C	--	110	mA
	T_J = 110 °C	--	50	
	T_J = 85 °C	--	100	
	T_J = 110 °C	--	50	
Input Leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
Thermal Resistance[2]		--	45.2	°C/W
Moisture Sensitivity Level [3]		1		

[1] V_{DDA} must be equal to V_{DD}.
[2] Measurements based on Analog Switches.
[3] Device is mounted on a 4-layer JEDEC board with 70 µm thick top copper, in a natural convection chamber.

3.2 Electrostatic Discharge Ratings

Table 5. Electrostatic Discharge Ratings

Parameter	Min	Max	Unit
ESD protection (human body model)	2000	--	V
ESD protection (charged device model)	1300	--	V

3.3 Recommended Operating Conditions

Table 6. Recommended Operating Conditions

Parameter	Condition	Min	Max	Unit
Supply Voltage (V_{DDA})	--	2.4	5.5	V
	During NVM Write and Erase Commands	2.5	5.5	V
Voltage Difference Between OpAmp Inputs	$\|V_{OAx+} - V_{OAx-}\|$	--	1.0	V
Operating Ambient Temperature	--	-40	125	°C
Capacitor Value at V_{DD}	--	0.1	--	µF
Analog Input Common Mode Range	Allowable Input Voltage at Analog Pins	-0.2	V_{DDA}+0.2	V

3.4 Electrical Specifications

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{IH}	High-level input voltage	Logic input[1]	0.7x V_{DD}	--	V_{DD}+ 0.3	V
		Logic input with Schmitt trigger	0.8x V_{DD}	--	V_{DD}+ 0.3	V
		Low-level logic input[1]	1.25	--	V_{DD}+ 0.3	V
V_{IL}	Low-level input voltage	Logic input[1]	GND- 0.3	--	0.3x V_{DD}	V
		Logic Input with Schmitt trigger	GND- 0.3	--	0.2x V_{DD}	V
		Low-level logic input[1]	GND- 0.3	--	0.5	V
V_{HYS}	Schmitt Trigger Hysteresis Voltage	V_{DD} = 2.5 V + 8 %/- 4 %	0.28	0.43	0.58	V
		V_{DD} = 3.3 V +/- 10 %	0.31	0.46	0.60	V
		V_{DD} = 5 V +/- 10 %	0.42	0.58	0.77	V
V_O	Maximal Voltage Applied to any PIN in High Impedance State		--	--	V_{DD}+ 0.3	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OH}	High-level output voltage	Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V	2.270	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V	2.376	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V	2.587	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V	2.678	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.011	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.335	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V	4.127	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V	4.656	--	--	V
		Push-Pull, 1x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V	5.186	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.4 V	2.337	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.5 V	2.440	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 1 mA, V_{DD} = 2.7 V	2.644	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.0 V	2.845	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.3 V	3.159	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 3 mA, V_{DD} = 3.6 V	3.469	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 4.5 V	4.317	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.0 V	4.831	--	--	V
		Push-Pull, 2x Drive, I_{OH} = 5 mA, V_{DD} = 5.5 V	5.342	--	--	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage	Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	--	--	0.095	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.5 V	--	--	0.092	V
		Push-Pull, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.7 V	--	--	0.086	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	--	--	0.245	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	--	0.227	V
		Push-Pull, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	--	0.212	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 4.5 V	--	--	0.311	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.0 V	--	--	0.291	V
		Push-Pull, 1x Drive, I_{OL}= 5 mA, V_{DD} = 5.5 V	--	--	0.274	V
		Push-Pull, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	--	--	0.048	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	--	--	0.047	V
		Push-Pull, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	--	--	0.044	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.0 V	--	--	0.123	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.3 V	--	--	0.114	V
		Push-Pull, 2x Drive, I_{OL}= 3 mA, V_{DD} = 3.6 V	--	--	0.108	V

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
V_{OL}	Low-level output voltage	Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	--	--	0.159	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	--	0.150	V
		Push-Pull, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	--	--	0.141	V
		NMOS OD, 1x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	--	--	0.039	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	--	--	0.038	V
		NMOS OD, 1x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	--	--	0.035	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	--	--	0.099	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	--	0.092	V
		NMOS OD, 1x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	--	0.087	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	--	--	0.128	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	--	0.121	V
		NMOS OD, 1x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	--	--	0.115	V
		NMOS OD, 2x Drive, I_{OL}= 1 mA, V_{DD} = 2.4 V	--	--	0.021	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.5 V	--	--	0.021	V
		NMOS OD, 2x Drive, I_{OL} = 1 mA, V_{DD} = 2.7 V	--	--	0.020	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.0 V	--	--	0.053	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.3 V	--	--	0.050	V
		NMOS OD, 2x Drive, I_{OL} = 3 mA, V_{DD} = 3.6 V	--	--	0.047	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 4.5 V	--	--	0.070	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.0 V	--	--	0.067	V
		NMOS OD, 2x Drive, I_{OL} = 5 mA, V_{DD} = 5.5 V	--	--	0.064	V
I_{OH}	High-level output current[2]	Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V	1.46	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V	1.55	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V	1.68	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V	4.98	--	--	mA

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OH}	High-level output current[2]	Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	7.57	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	10.21	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V	18.21	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V	22.33	--	--	mA
		Push-Pull, 1x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V	27.42	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.4 V	2.95	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.5 V	3.09	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = V_{DD} - 0.2 V_{DD} = 2.7 V	3.37	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.0 V	9.85	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.3 V	14.94	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 3.6 V	20.10	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 4.5 V	35.73	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.0 V	44.01	--	--	mA
		Push-Pull, 2x Drive, V_{OH} = 2.4 V, V_{DD} = 5.5 V	53.10	--	--	mA
I_{OL}	Low-level output current[2]	Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	1.46	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	1.51	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	1.62	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	4.43	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	4.79	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	5.11	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	5.93	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	6.33	--	--	mA
		Push-Pull, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	6.75	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	2.87	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	2.96	--	--	mA

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
I_{OL}	Low-level output current[2]	Push-Pull, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	3.15	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	8.65	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	9.32	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	9.90	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	11.47	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	12.16	--	--	mA
		Push-Pull, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	12.97	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	3.56	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	3.68	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	3.93	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	10.74	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	11.56	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	12.27	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	14.19	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	15.09	--	--	mA
		NMOS OD, 1x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	15.99	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.4 V	6.78	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.5 V	7.01	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.15 V, V_{DD} = 2.7 V	7.41	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.0 V	20.19	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.3 V	21.62	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 3.6 V	22.89	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 4.5 V	26.15	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.0 V	27.66	--	--	mA
		NMOS OD, 2x Drive, V_{OL} = 0.4 V, V_{DD} = 5.5 V	29.23	--	--	mA

Table 7. ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Min	Typ	Max	Unit
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR} Slew Rate 1 V/µs	--	1.9	2.8	ms
T_{WR}	NVM Page Write Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
T_{ER}	NVM Page Erase Time	V_{DD} = 2.5 V to 5.5 V	--	--	20	ms
PON_{THR}	Power-on threshold	V_{DD} level required to start up the chip	1.63	1.84	2.05	V
$POFF_{THR}$	Power-off threshold	V_{DD} level required to switch off the chip	0.83	1.27	1.54	V
R_{PULL}	Pull-up or pull-down resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	1.06	--	MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	106.6	--	kΩ
		10 k For Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = V_{DD}	--	9.3	--	kΩ
C_{IN}	Input capacitance	PINs 10, 11	--	2.9	--	pF
		PIN 12	--	3.6	--	pF
		PINs 15, 16	--	3.8	--	pF
		PINs 17, 18, 19	--	10.2	--	pF
		PIN 20	--	27.8	--	pF
		PIN 21	--	5.7	--	pF

[1] No hysteresis.
[2] DC or average current through any pin should not exceed value given in Absolute maximum conditions.

3.5 I²C Pins Specifications

Table 8. ES of the I²C Pins for DI Mode at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
V_{IL}	Low-level input voltage	--	-0.5	$0.3xV_{DD}$	-0.5	$0.3xV_{DD}$	V
V_{IH}	High-level input voltage	--	$0.7xV_{DD}$	5.5	$0.7xV_{DD}$	5.5	V
V_{HYS}	Hysteresis of Schmitt trigger inputs	--	$0.05xV_{DD}$	--	$0.05xV_{DD}$	--	V
V_{OL1}	Low-level output voltage 1	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	0	0.4	V
V_{OL2}	Low-level output voltage 2	(Open-Drain) at 2 mA sink current $V_{DD} \le 2$ V	0	$0.2xV_{DD}$	0	$0.2xV_{DD}$	V
I_{OL}	Low-level output current[1]	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	--	16.75	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	20	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	20	--	
		V_{OL}= 0.6 V	6	--	--	--	
t_{of}	Output fall time from V_{IHmin} to V_{ILmax} [1]	--	14x (V_{DD}/5.5 V)	250	10x (V_{DD}/5.5 V)	120	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter	--	0	50	0	50	ns
I_i	Input current (each IO pin)	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	-10	+10	µA
C_i	Capacitance (each IO pin)	--	--	10	--	10	pF

[1] Does not meet standard I²C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min); for Fast-mode Plus I_{OL} = 20 mA (min) at V_{OL} = 0.4 V.
[2] For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [1155] in Section 21. Register Definitions.

Table 9. ES of the I²C Pins for DILV Mode at T_A = -40°C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
V_{IL}	Low-level input voltage	--	-0.5	0.619	V
V_{IH}	High-level input voltage	--	1.154	5.5	V
V_{OL1}	Low-level output voltage 1	(Open-Drain) at 3 mA sink current V_{DD} > 2 V	0	0.4	V
V_{OL2}	Low-level output voltage 2	(Open-Drain) at 2 mA sink current $V_{DD} \le 2$ V	0	$0.2xV_{DD}$	V

Table 9. ES of the I2C Pins for DILV Mode at T_A = -40°C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
I_{OL}	Low-level output current[1]	V_{OL} = 0.4 V, V_{DD} = 2.4 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 3.0 V	3	--	mA
		V_{OL} = 0.4 V, V_{DD} = 4.5 V	3	--	mA
		V_{OL}= 0.6 V	6	--	mA
t_{of}	Output fall time from V_{IHmin} to V_{ILmax}[1]		14x (V_{DD}/5.5 V)	250	ns
t_{SP}	Pulse width of spikes that must be suppressed by the input filter		0	50	ns
I_i	Input current (each IO pin)	$0.1xV_{DD} < V_I < 0.9xV_{DDmax}$	-10	+10	µA
C_i	Capacitance (each IO pin)		--	10	pF

[1] Does not meet standard I2C specifications: t_{of} = 20x(V_{DD}/5.5 V) (min).
[2] For Fast-mode Plus SDA pin must be configured as NMOS 2x Open-Drain, see register [1155] in Section 21. Register Definitions.

Table 10. I2C Pins Timing Specifications, DI Mode, T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Fast-Mode Plus		Unit
			Min	Max	Min	Max	
F_{SCL}	Clock frequency, SCL	--	--	400	--	1000	kHz
t_{LOW}	Clock pulse width Low	--	1300	--	500	--	ns
t_{HIGH}	Clock pulse width High	--	600	--	260	--	ns
t_I	Input filter spike suppression (SCL, SDA)	--	--	50	--	50	ns
t_{AA}	Clock Low to Data OUT Valid	--	--	900	--	450	ns
t_{BUF}	Bus free time between stop and start	--	1300	--	500	--	ns
t_{HD_STA}	Start hold time	--	600	--	260	--	ns
t_{SU_STA}	Start set-up time	--	600	--	260	--	ns
t_{HD_DAT}	Data hold time	--	0	--	0	--	ns
t_{SU_DAT}	Data set-up time	--	100	--	50	--	ns
t_R	Inputs rise time	--	--	300	--	120	ns
t_F	Inputs fall time	--	--	300	--	120	ns
t_{SU_STO}	Stop set-up time	--	600	--	260	--	ns
t_{DH}	Data OUT hold time	--	50	--	50	--	ns

[1] Timing diagram can be found in Figure 238.

Table 11. I²C Pins Timing Specifications, DILV Mode, T_A = -40°C to +125°C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Condition	Fast-Mode		Unit
			Min	Max	
F_{SCL}	Clock frequency, SCL	--	--	400	kHz
t_{LOW}	Clock pulse width Low	--	1300	--	ns
t_{HIGH}	Clock pulse width High	--	600	--	ns
t_I	Input filter spike suppression (SCL, SDA)	--	--	50	ns
t_{AA}	Clock Low to Data OUT Valid	--	--	900	ns
t_{BUF}	Bus free time between stop and start	--	1300	--	ns
t_{HD_STA}	Start hold time	--	600	--	ns
t_{SU_STA}	Start set-up time	--	600	--	ns
t_{HD_DAT}	Data hold time[1]	--	185	--	ns
t_{SU_DAT}	Data set-up time[1]	--	335	--	ns
t_R	Inputs rise time	--	--	300	ns
t_F	Inputs fall time	--	--	300	ns
t_{SU_STO}	Stop set-up time	--	600	--	ns
t_{DH}	Data OUT hold time	--	50	--	ns

[1] Does not meet standard I²C specifications: t_{HD_DAT} = 0 ns (min), t_{SU_DAT} = 100 ns (min) for Fast-mode.
[2] Timing diagram can be found in Figure 238.

3.6 Macrocells Current Consumption

Table 12. Typical Current Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I_{DD}	Current	Chip Quiescent, BG disabled	0.06	0.08	0.13	µA
		Chip Quiescent, BG enabled	0.36	0.39	0.47	µA
		OSC2 25 MHz, pre-divider = 1	40.78	49.64	70.54	µA
		OSC2 25 MHz, pre-divider = 4	31.75	37.46	51.41	µA
		OSC2 25 MHz, pre-divider = 8	29.96	35.06	47.62	µA
		OSC1 2.048 MHz, pre-divider = 1	19.19	19.98	21.73	µA
		OSC1 2.048 MHz, pre-divider = 4	18.50	19.05	20.26	µA
		OSC1 2.048 MHz, pre-divider = 8	18.36	18.87	19.97	µA
		OS00 2.048 kHz, pre-divider = 1	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, pre-divider = 4	0.33	0.36	0.44	µA
		OSC0 2.048 kHz, pre-divider = 8	0.33	0.36	0.44	µA
		Push-Pull 1x + 4 pF @ 2.048 kHz	0.38	0.44	0.55	µA
		Push-Pull 1x + 4 pF @ 2.048 MHz	66.8	82.6	116.0	µA
		Temperature Sensor, range 1	10.9	10.9	11.2	µA
		Temperature Sensor, range 2	11.0	11.1	11.4	µA
		One ACMPx_L (includes internal Vref)	6.1	6.2	6.4	µA
		Two ACMPx_L (includes internal Vref)	8.4	8.5	8.8	µA
		Op AmpX Quiescent Current (128 kHz bandwidth)	32.2	32.8	33.8	µA
		Op AmpX Quiescent Current (8.192 MHz bandwidth)	607	611	613	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Disabled)	98	101	104	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 128 kHz bandwidth, Charge Pump - Enabled)	75.2	77.5	80.8	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Disabled)	1819	1834	1844	µA
		In Amp Quiescent Current (three Op Amps are ON, Rf1 = Rf2 = 50 kΩ, Rg =1 kΩ, 8.192 MHz bandwidth, Charge Pump - Enabled)	1225	1235	1245	µA
		Chopper ACMP (with 2.048 kHz clock)	31.4	33.6	38.4	µA

3.7 Timing Specifications

Table 13. Typical Delay Estimated for Each Macrocell at T_A = 25 °C

Parameter	Description	Conditions	V_{DD} = 2.5 V		V_{DD} = 3.3 V		V_{DD} = 5 V		Unit
			Rising	Falling	Rising	Falling	Rising	Falling	
tpd	Delay	Digital Input to PP 1x	26	27	18	20	13	15	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1x	27	28	19	21	15	15	ns
tpd	Delay	Digital Input to PP 2x	24	25	17	18	12	14	ns
tpd	Delay	Low Voltage Digital input to PP 1x	28	246	20	163	15	95	ns
tpd	Delay	Digital input to NMOS output	--	24	--	18	--	13	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 1	26	--	19	--	13	--	ns
tpd	Delay	Output enable from Pin, OE Hi-Z to 0	--	26	--	19	--	14	ns
tpd	Delay	Digital input to 1x3-State (Z to 1)	26	--	19	--	13	--	ns
tpd	Delay	Digital input to x3-State (Z to 0)	--	26	--	17	--	14	ns
tpd	Delay	Digital input to 2x3-State (Z to 1)	24	--	17	--	13	--	ns
tpd	Delay	Digital input to 2x3-State (Z to 0)	--	24	--	19	--	12	ns
tpd	Delay	LUT2bt	17	17	12	12	8	8	ns
tpd	Delay	LUT3bit	19	20	13	14	9	10	ns
tpd	Delay	LUT4bit	20	21	15	14	9	10	ns
tpd	Delay	LATCH	25	25	17	18	12	12	ns
tpd	Delay	DFF	24	25	16	18	11	12	ns
tpd	Delay	CNT/DLY	107	107	77	74	48	70	ns
tw	Width	Edge detect	206	205	161	160	116	116	ns
tpd	Delay	Edge detect	19	20	13	13	8	8	ns
tpd	Delay	Edge detect Delayed	241	241	175	175	125	125	ns
tpd	Delay	Ripple Counter	45	60	32	44	22	31	ns
tpd	Delay	PGen	20	20	14	14	9	10	ns
tpd	Delay	Filter	177	177	121	121	77	78	ns
tpd	Delay	Inverter Filter	115	115	83	83	57	57	ns
tpd	Delay	Pipe Delay	36	37	25	26	17	18	ns

Table 14. Programmable Delay Expected Typical Delays and Widths at T_A = 25 °C

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
tw	Pulse width, 1 cell	mode: (any) edge detect, edge detect output	223	163	118	ns
tw	Pulse width, 2 cell	mode: (any) edge detect, edge detect output	444	324	233	ns
tw	Pulse width, 3 cell	mode: (any) edge detect, edge detect output	663	484	347	ns
tw	Pulse width, 4 cell	mode: (any) edge detect, edge detect output	882	643	461	ns
time1	Delay, 1 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 2 cell	mode: (any) edge detect, edge detect output	18	12	8	ns

Table 14. Programmable Delay Expected Typical Delays and Widths at T_A = 25 °C (Cont.)

Parameter	Description	Note	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time1	Delay, 3 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time1	Delay, 4 cell	mode: (any) edge detect, edge detect output	18	12	8	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	243	176	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	464	337	241	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	683	497	356	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	902	655	470	ns

Table 15. Typical Filter Rejection Pulse Width at T_A = 25 °C

Parameter	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered pulse width	< 131	< 89	< 59	ns

3.8 Counter/Delay Specifications

Table 16. Typical Counter/Delay Offset Measurements at T_A = 25 C

Parameter	OSC Freq	OSC Power	V_{DD} = 2.5 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Power-on time	25 MHz	auto	0.046	0.032	0.022	µs
Power-on time	2.048 MHz	auto	0.511	0.458	0.414	µs
Power-on time	2.048 kHz	auto	657	563	477	µs
Frequency settling time	25 MHz	auto	0.314	0.378	0.455	µs
Frequency settling time	2.048 MHz	auto	1.344	1.597	2.063	µs
Frequency settling time	2.048 kHz	auto	657	1066.295	476.500	µs
Variable (CLK period)	25 MHz	forced	0.039 - 0.042	0.040 - 0.041	0.038 - 0.042	µs
Variable (CLK period)	2.048 MHz	forced	0.480 - 0.500	0.490 - 0.491	0.480 - 0.495	µs
Variable (CLK period)	2.048 kHz	forced	477 - 500	478 - 499	478 - 498	µs
Typical Propagation Delay (non-delayed edge)	25 MHz/ 2.048 kHz	either	35	14	10	ns

3.9 Oscillator Specifications

Table 17. Oscillators Frequency Limits, V_{DD} = 2.4 V to 5.5 V

OSC	Ambient Temperature Range					
	+25 °C		-40 °C to +85 °C		-40 °C to +125 °C	
	Minimum value, kHz	Maximum value, kHz	Minimum value, kHz	Maximum value, kHz	Minimum value, kHz	Maximum value, kHz
2.048 kHz OSC0	2.024	2.072	1.935	2.075	1.600	2.098
2.048 MHz OSC1	2024	2072	--	--	1967	2103
25 MHz OSC2	24500	25500	--	--	22920	25780

Table 18. Oscillators Frequency Error, V_{DD} = 2.4 V to 5.5 V, (Error Calculated Relative to Nominal Value)

OSC	Ambient Temperature Range					
	+25 °C		-40 °C to +85 °C		-40 °C to +125 °C	
	Error (%, at Min)	Error (%, at Max)	Error (%, at Min)	Error (%, at Max)	Error (%, at Min)	Error (%, at Max)
2.048 kHz OSC0	-1.17	+1.17	-5.52	+1.32	-21.88	+2.44
2.048 MHz OSC1	-1.17	+1.17	--	--	-3.96	+2.69
25 MHz OSC2	-2.00	+2.00	--	--	-8.32	+3.12

3.9.1 OSC Power-On Delay

Table 19. Oscillators Power-On Delay at T_A = 25 °C, OSC Power Setting: "Auto Power-On"

Power Supply Range (V_{DD}) V	OSC0 2.048 kHz		OSC1 2.048 MHz		OSC2 25 MHz		OSC2 25 MHz Start with Delay	
	Typical value, µs	Maximum value, µs	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns	Typical value, ns	Maximum value, ns
2.50	673.07	931.67	516.58	535.21	44.68	53.91	146.42	158.60
3.30	575.79	765.49	467.35	525.05	31.47	55.70	141.64	153.68
4.00	529.44	686.46	444.62	554.38	25.95	61.94	140.48	152.69
5.00	486.06	612.94	423.41	664.22	21.63	82.23	139.95	152.70
5.50	462.68	576.56	415.84	642.99	20.25	82.51	139.77	152.91

3.10 ACMP Specifications

Table 20. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input		0	--	V_{DD}	V
		Negative Input		0	--	V_{DD}	V
V_{offset}	ACMP input offset	ACMPxL, Vhys = 0 mV, Gain = 1, Vref = 32 mV to 2048 mV	T_A = -40 °C to +125 °C	-6.35	--	3.67	mV
			T_A = 25 °C	-5.76	-0.98	3.39	mV
	Chopper ACMP Input Offset		T_A = -40 °C to +125 °C	-0.26	--	0.49	mV
			T_A = 25 °C	-0.12	0.11	0.39	mV
t_{start}	ACMP Startup Time when BG ON	ACMP Power-On delay, Minimal required wake time for the "Wake and Sleep function", for ACMPxL	T_A = -40 °C to +125 °C	--	51.0	99.6	µs
	ACMP Startup Time when BG OFF			--	1729	3110	µs
	Chopper ACMP Startup Time when BG ON	OSC0		--	1074	1719	µs
		OSC1/64		--	71	74	µs
R_{sin}	Series input resistance	Gain = 1x	--	--	10	--	GΩ
		Gain = 0.5x		--	1.6	--	MΩ
		Gain = 0.33x		--	1.6	--	MΩ
		Gain = 0.25x		--	1.6	--	MΩ
PROP	Propagation Delay, Response time	ACMPxL, Vref =1.024 V, Gain = 1, Overdrive = 100 mV	Low to High	--	2.59	3.66	µs
			High to Low	--	2.80	5.21	µs
		ACMPxL, Vref = 32 mV to 2048 mV, Gain = 1, Overdrive = 100 mV	Low to High	--	2.83	5.16	µs
			High to Low	--	2.96	7.63	µs
		ACMPxL, Vref =1.024 V, Gain = 1, Overdrive = 10 mV	Low to High	--	8.18	12.57	µs
			High to Low	--	9.14	18.54	µs
		ACMPxL, Vref = 32 mV to 2048 mV, Gain = 1, Overdrive = 10 mV	Low to High	--	9.16	31.42	µs
			High to Low	--	10.01	36.39	µs

Table 20. ACMP Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted (Cont.)

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
G	Gain error	G = 1		1	1	1	
		G = 0.5		0.496	0.500	0.504	
		G = 0.33		0.331	0.330	0.336	
		G = 0.25		0.248	0.250	0.253	

3.11 Internal Vref Specifications

Table 21. Internal Vref Specifications at V_{DD} = 2.4 V to 5.5 V

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
$Vref_{ACCURACY}$	Internal Vref Accuracy at Vref > 1216 mV	No loading	T_A = +25 °C	-0.60	--	0.56	%
			T_A = -40 °C to +125 °C	-1.17	--	0.83	%
$Div_{ACCURACY}$	Vref Divider Accuracy	Vref from (16/64) to (64/64)	T_A = -40 °C to +125 °C	-0.46	0.04	0.37	%
		Vref from (1/64) to (64/64)	T_A = -40 °C to +125 °C	-2.24	0.02	1.31	%
Div_{OFFSET}	Vref Divider Offset	Vref from (16/64) to (64/64)	T_A = -40 °C to +125 °C	-6.16	0.83	8.69	mV
		Vref from (1/64) to (64/64)	T_A = -40 °C to +125 °C	-6.16	0.62	8.69	mV

3.12 Output Buffers Specifications

Table 22. HD Buffer Electrical Specifications at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
Offset						
V_{OFFSET}	Input Offset Voltage	V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V, T_A = 25 °C	--	0.25	8.0	mV
		V_{DDA} = 5 V, V_{OUT} = 0.5 V to 4 V	--	--	9.0	mV
dV_{OFFSET}/dt	Offset Drift with Ambient Temperature	V_{OUT} = $V_{DDA}/2$	--	--	16.8	µV/C
Output						
$\Delta V_{OUT}(I)$	Load Regulation	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T_A = 25 °C	--	0.2	1.2	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T_A = 25 °C		0.4	1.9	mV
$\Delta V_{OUT}(U)$	Line Regulation	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T_A = 25 °C	--	0.9	5.0	mV
I_{SC}	Short Circuit Current	V_{DDA} = 2.4 V to 5.5 V	--	67.8	--	mA
Shutdown Characteristics						
t_{on}	Buffer Turn-On Time	R_{LOAD} = 5 kΩ, BG is ON, T_A = 25 °C	--	--	50	µs
t_{off}	Buffer Turn-Off Time	R_{LOAD} = 5 kΩ, T_A = 25 °C	--	0.071	--	µs

Table 23. Vref Output Buffer at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Note	Min	Typ	Max	Unit
$\Delta V_{OUT}(I)$	Load Regulation	V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 2 mA, T_A = 25 °C	--	-0.99	--	1.21	mV
		V_{DDA} = 5 V, V_{OUT} = 2.048 V, I_{LOAD} = 0.5 mA to 5 mA, T_A = 25 °C	--	-0.99	--	1.39	mV
$\Delta V_{OUT}(U)$	Line Regulation	V_{DDA} = 2.5 V to 5 V, V_{OUT} = 2.048 V, T_A = 25 °C	--	-2.97	--	5.13	mV
Vref Buffer Accuracy and Loading	Vref Output Buffer Offset	Vref < 1024 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-26.2	--	10.0	mV
				-28.2	--	10.8	mV
		Vref =1024 mV to 1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-14.8	--	6.2	mV
				-15.5	--	7.2	mV
		Vref >1600 mV, V_{DDA} = 2.4 V to 5.5V, No Loading	T_A = 25 °C	-19.1	--	11.6	mV
				-20.0	--	13.0	mV
		Vref =1024 mV to 2048 mV, V_{DDA} = 3.3 V, No Loading	T_A = 25 °C	-14.8	--	5.8	mV
				-15.8	--	6.6	mV
	Vref0 Buffer Output Capacitance Loading		Load Resistance = 1 MΩ	--	--	5	pF
			Load Resistance = 560 kΩ	--	--	10	pF
			Load Resistance = 100 kΩ	--	--	40	pF
			Load Resistance = 10 kΩ	--	--	80	pF
			Load Resistance = 2 kΩ	--	--	120	pF
			Load Resistance = 1 kΩ, Vref = 32 mV to 1024 mV	--	--	150	pF

3.13 Analog Temperature Sensor Specifications

Typical deviation from Temperature Sensor equations (section 20. Analog Temperature Sensor) is ± 0.09 % for both ranges at V_{DD} = 3.3 V.

Table 24. TS Output vs. Junction Temperature (Output Range 1) , V_{DD} = 2.4 V to 5.5 V

Parameter	T_J, °C	Target V_{TS_OUT}, V	V_{TS_OUT}, V		Calculated T_J, °C		V_{TS_OUT} Accuracy, %		T_J Accuracy, °C	
			Min	Max	Min	Max	Min	Max	Min	Max
TS Output vs. T_J Buffer Enabled	-40	0.9893	0.9791	1.0020	-45.7	-35.5	-1.03	1.28	-5.7	4.5
	-30	0.9668	0.9571	0.9788	-35.3	-25.7	-1.00	1.24	-5.3	4.3
	-20	0.9441	0.9349	0.9553	-24.9	-16.0	-0.98	1.18	-4.9	4.0
	-10	0.9213	0.9129	0.9318	-14.6	-6.3	-0.92	1.14	-4.6	3.7
	0	0.8983	0.8900	0.9082	-4.3	3.6	-0.92	1.11	-4.3	3.6
	10	0.8751	0.8681	0.8842	6.1	13.0	-0.79	1.04	-3.9	3.0
	20	0.8517	0.8450	0.8603	16.3	22.8	0.78	1.02	-3.7	2.8
	25	0.8399	0.8338	0.8480	21.6	27.6	-0.73	0.96	-3.4	2.6
	30	0.8281	0.8220	0.8366	26.4	32.6	-0.74	1.02	-3.6	2.6
	40	0.8043	0.7978	0.8133	36.2	42.7	-0.81	1.11	-3.8	2.7
	50	0.7804	0.7737	0.7900	46.0	52.8	-0.86	1.22	-4.0	2.8
	60	0.7563	0.7493	0.7663	55.9	62.9	-0.92	1.33	-4.1	2.9
	70	0.7320	0.7246	0.7424	65.7	73.0	-1.01	1.42	-4.3	3.0
	80	0.7075	0.6997	0.7182	75.7	83.2	-1.10	1.50	-4.3	3.2
	85	0.6952	0.6872	0.7060	80.6	88.3	-1.16	1.55	-4.4	3.3
	90	0.6829	0.6743	0.6937	85.6	93.5	-1.26	1.59	-4.4	3.5
	100	0.6581	0.6493	0.6691	95.5	103.5	-1.33	1.68	-4.5	3.5
	110	0.6331	0.6238	0.6444	105.5	113.7	1.46	1.79	-4.5	3.7
	120	0.6079	0.5990	0.6188	115.7	123.5	-1.46	1.81	-4.3	3.5
	125	0.5952	0.5850	0.6079	120.0	129.0	-1.71	2.13	-5.0	4.0

.

Table 25. TS Output vs. Junction Temperature (Output Range 2) , V_{DD} = 2.4 V to 5.5 V

Parameter	T_J, °C	Target V_{TS_OUT}, V	V_{TS_OUT}, V		Calculated T_J, °C		V_{TS_OUT} Accuracy, %		T_J Accuracy, °C	
			Min	Max	Min	Max	Min	Max	Min	Max
TS Output vs. T_J Buffer Enabled	-40	1.1936	1.1812	1.2087	-45.6	-35.4	-1.04	1.27	-5.6	4.6
	-30	1.1664	1.1547	1.1807	-35.2	-25.7	-1.01	1.22	-5.2	4.3
	-20	1.1391	1.1279	1.1524	-24.9	-15.9	-0.99	1.17	-4.9	4.1
	-10	1.1116	1.1011	1.1240	-14.5	-6.2	-0.94	1.12	-4.5	3.8
	0	1.0838	1.0736	1.0956	-4.3	3.6	-0.94	1.09	-4.3	3.6
	10	1.0558	1.0472	1.0667	6.1	13.0	-0.81	1.03	-3.9	3.0
	20	1.0276	1.0194	1.0380	16.3	22.9	-0.80	1.01	-3.7	2.9
	25	1.0134	1.0059	1.0229	21.6	27.6	-0.74	0.94	-3.4	2.6
	30	0.9992	0.9916	1.0092	26.5	32.6	-0.76	1.00	-3.5	2.6
	40	0.9705	0.9624	0.9811	36.3	42.8	-0.83	1.09	-3.7	2.8
	50	0.9417	0.9334	0.9530	46.1	52.8	-0.87	1.21	-3.9	2.8
	60	0.9126	0.9040	0.9244	55.9	62.9	-0.93	1.30	-4.1	2.9
	70	0.8833	0.8742	0.8956	65.8	73.1	-1.03	1.40	-4.2	3.1
	80	0.8537	0.8442	0.8664	75.7	83.2	-1.12	1.48	-4.3	3.2
	85	0.8389	0.8291	0.8518	80.7	88.3	-1.17	1.54	-4.3	3.3
	90	0.8240	0.8135	0.8371	85.6	93.5	-1.27	1.59	-4.4	3.5
	100	0.7940	0.7833	0.8073	95.6	103.6	-1.35	1.68	-4.4	3.6
	110	0.7638	0.7526	0.7774	105.5	113.7	-1.47	1.78	-4.5	3.7
	120	0.7334	0.7226	0.7467	115.6	123.5	-1.47	1.81	-4.4	3.5
	125	0.7181	0.7057	0.7334	120.0	129.0	-1.73	2.12	-5.0	4.0

3.14 Programmable Operational Amplifier Specifications

Table 26. ES of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM}= V_{DDA}/2, V_{OUT}≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T_A = 25 °C

Parameter	Description	Conditions[1]	Min	Typ	Max	Unit
Input Voltage Offset (without Customers Trimming, Included Factory Block Offset Trim)						
V_{OFFSET}	Input Offset Voltage	BW = 128 kHz	--	69	500	μV
		BW = 128 kHz, T_A = -40 °C to +125 °C	--	69	2300	μV
		BW = 512 kHz	--	56	500	μV
		BW = 512 kHz, T_A = -40 °C to +125 °C	--	56	2710	μV
		BW = 2 MHz	--	47	500	μV
		BW = 2 MHz, T_A = -40 °C to +125 °C	--	47	2300	μV
		BW = 8 MHz	--	35	243	μV
		BW = 8 MHz, T_A = -40 °C to +125 °C	--	35	1000	μV
dV_{OFFSET}/dt	Offset Drift with Ambient Temperature	V_{CM} = V_{DD}/2 T_A = -40 °C to +125 °C	--	0.6	13.0	μV/°C
		V_{CM} = GND, T_A = -40 °C to +125 °C	--	0.3	13.1	μV/°C
dV_{OFFSET}/ Time	Long-Term Offset Voltage Drift	V_{CM} = V_{DD}/2	--	0	550	μV
Trimmed Input Offset (Customer Perspective after Using Digital Rheostats with Gain = 200x)[2]						
V_{OFFSET}	Input Offset Voltage		--	--	5	μV
Input Voltage Range						
V_{CMR}	Input Common-Mode Voltage Range	T_A = -40 °C to +125 °C	-0.2	--	V_{DD} + 0.2	V
CMRR	Common-Mode Rejection Ratio	All Op Amps, BW = 128 kHz GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 °C to +125 °C	74.9	103.7	--	dB
		All Op Amps, BW = 128 kHz GND < V_{CM}< GND + 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD} T_A = -40 °C to +125 °C	51.3	101.6	--	dB
		All Op Amps, BW = 512 kHz/2MHz/8MHz GND + 0.8 V < V_{CM} < V_{DD} - 0.8 V, T_A = -40 °C to +125 °C	73.5	102.3	--	dB
		All Op Amps, BW = 512 kHz/2MHz/8MHz GND < V_{CM}< GND + 0.8 V or V_{DD} - 0.8 V < V_{CM} < V_{DD} T_A = -40 °C to +125 °C	69.5	101.1	--	dB
PSRR	Power Supply Rejection Ratio	T_A = -40 °C to +125 °C	80	101	--	dB
		V_{CM} = GND, T_A = -40 °C to +125 °C	83	102	--	dB
CS	Channel Separation	V_{DD} = 5 V, f = 10 Hz	--	119	--	dB
		V_{DD} = 5 V, f = 1 kHz	--	112	--	dB
Input Current and Impedance						
I_B	Input Bias Current		--	1.9	±9	pA
		T_A = -40 °C to +125 °C	--	1.9	±12021	pA

Table 26. ES of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM}= V_{DDA}/2, V_{OUT}≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T_A = 25 °C

Parameter	Description	Conditions[1]	Min	Typ	Max	Unit
I_{OFFSET}	Input Offset Current		--	--	3.2	pA
		T_A = +125 °C	--	--	3839	pA
R_{CM}	Common-Mode Input Resistance		--	$3*10^{12}$	--	Ω
R_{DIFF}	Differential Input Resistance		--	10^{13}	--	Ω
C_{CM}	Input Capacitance Common-Mode		--	5	7	pF
C_{DIFF}	Input Capacitance Differential		--	1.98	2.27	pF
Open-Loop Gain						
A_{OL}	DC Open Loop Gain	R_{LOAD} = 1 MΩ, GND + 0.1 V < V_{OUT} < V_{DD} - 0.1 V, T_A = -40 °C to +125 °C	95.7	125	--	dB
		R_{LOAD} = 50 kΩ, GND + 0.5 V < V_{OUT} < V_{DD} - 0.5 V T_A = -40 °C to +125 °C	81.0	123	--	dB
Output						
V_{OH}	Maximum Voltage Swing	R_{LOAD} = 50 kΩ, T_A = -40 °C to +125 °C	V_{DD} - 6.3	--	--	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T_A = -40 °C to +125 °C	V_{DD} - 142	--	--	mV
V_{OL}		R_{LOAD} = 50 kΩ, T_A = -40 °C to +125 °C	--	--	GND + 3.53	mV
		BW = 8.192 MHz, R_{LOAD} = 600 Ω, T_A = -40 °C to +125 °C	--	--	GND + 106	mV
V_{OSR}	Linear Output Swing Range	V_{OVR} from Rail R_{LOAD} = 1 MΩ	GND + 100	--	V_{DD} - 100	mV
I_{SC}	Short Circuit Current	I_{SC} to GND: BW = 128 kHz, T_A = -40 °C to +125 °C	--	10.8	--	mA
		I_{SC} to GND: BW = 512 kHz, T_A = -40 °C to +125 °C	--	14.4	--	mA
		I_{SC} to GND: BW = 2.048 MHz, T_A = -40 °C to +125 °C	--	22.5	--	mA
		I_{SC} to GND: BW = 8.192 MHz, T_A = -40 °C to +125 °C	--	52.0	--	mA
		I_{SC} to V_{DD}: BW = 128 kHz, T_A = -40 °C to +125 °C		20.6	--	mA
		I_{SC} to V_{DD}: BW = 512 kHz, T_A = -40 °C to +125 °C		27.0	--	mA
		I_{SC} to V_{DD}: BW = 2.048 MHz, T_A = -40 °C to +125 °C		41.1	--	mA
		I_{SC} to V_{DD}: BW = 8.192 MHz, T_A = -40 °C to +125 °C		92.1	--	mA
C_{LOAD}	Capacitive Load Drive		See Section 10.3 Op Amps Typical Performance (Small Signal Overshoot vs. Capacitive Load plots)			

Table 26. ES of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM}= V_{DDA}/2, V_{OUT}≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T_A = 25 °C

Parameter	Description	Conditions[1]		Min	Typ	Max	Unit
Power Supply							
V_{DD}	Supply Voltage	Guaranteed by PSRR Test		2.4	--	5.5	V
I_Q (including charge pump current consumption)	Quiescent Current per Amplifier, BW = 128 kHz	V_{DDA} = 2.5 V to 5.5 V		--	33.3	47	µA
		T_A = -40 °C to +125 °C, V_{DDA} = 2.5 V to 5.5 V		--	36.6	63	µA
	Quiescent Current per Amplifier, BW = 512 kHz	V_{DDA} = 2.5 V to 5.5 V		--	89.8	101	µA
		T_A = -40 °C to +125 °C, V_{DDA} = 2.5 V to 5.5 V		--	93.2	124	µA
	Quiescent Current per Amplifier, BW = 2.048 MHz	V_{DDA} = 2.5 V to 5.5 V		--	238.7	255	µA
		T_A = -40 °C to +125 °C, V_{DDA} = 2.5 V to 5.5 V		--	241.2	281	µA
	Quiescent Current per Amplifier, BW = 8.192 MHz	T_A = 25 °C, V_{DDA} = 2.5 V to 5.5 V		--	611.5	652	µA
		T_A = -40 °C to +125 °C, V_{DDA} = 2.5 V to 5.5 V		--	622.8	748	µA
I_Q (including charge pump current consumption)	Full Shutdown			--	105.8	--	nA
	Partial Shutdown[3], All Supporting Blocks are ON, BW = 128 kHz			--	7.3	--	µA
	Partial Shutdown[3], All Supporting Blocks are ON, BW = 8.192 MHz			--	21.3	--	µA
Frequency Response							
GBW	Gain Bandwidth Product	R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, G = +1 V/V, T_A = -40 °C to +125 °C	BW = 128 kHz	--	124	--	kHz
			BW = 512 kHz	--	542	--	kHz
			BW = 2.048 MHz	--	2569	--	kHz
			BW = 8.192 MHz	--	9594	--	kHz
PM	Phase Margin	G = +1 V/V, BW = 128 kHz → 8.192 MHz; R_{LOAD} = 10 kΩ, C_{LOAD} = 20 pF, T_A = -40 °C to +125 °C		39	71	--	degree
SR	Slew Rate	R_{LOAD} = 50 kΩ, C_{LOAD} = 85 pF	BW = 128 kHz, T_A = -40 °C to +125 °C	--	0.09	--	V/µs
			BW = 512 kHz, T_A = -40 °C to +125 °C	--	0.38	--	V/µs
			BW = 2.048 MHz, T_A = -40 °C to +125 °C	--	1.85	--	V/µs
			BW = 8.192 MHz, T_A = -40 °C to +125 °C	--	6.48	--	V/µs
t_{OR}	Overload Recovery Time	T_A = -40 °C to +125 °C R_{LOAD} = 50 kΩ C_{LOAD} = 85 pF		--	12.68	--	µs

Table 26. ES of OA, V_{DDA} = 2.4 V to 5.5 V, V_{CM}= V_{DDA}/2, V_{OUT}≈ V_{DDA}/2, R_L = 100 kΩ to V_{DDA}/2, C_L = 50 pF, T_A = 25 °C

Parameter	Description	Conditions[1]		Min	Typ	Max	Unit
Noise							
THD	Total Harmonic Distortion	AV = 1, R_{LOAD} = 50 kΩ, $V_{OUT(PP)}$ = V_{DD}/2	f = 1 kHz, BW = 128 kHz	--	0.171	--	%
			f = 1 kHz, BW = 512 kHz	--	0.073	--	%
			f = 1 kHz, BW = 2.048 MHz	--	0.033	--	%
			f = 1 kHz, BW = 8.192 MHz	--	0.02	--	%
e_n	Input Voltage Noise	f = 0.1 to 10 Hz		--	24.78	--	µVpp
Vn	Input Voltage Noise Density	f = 1 kHz	BW = 128 kHz	--	92.198	--	nV/√Hz
			BW = 512 kHz	--	85.72	--	
			BW = 2.048 MHz	--	74.303	--	
			BW = 8.192 MHz	--	50.659	--	
In	Input Current Noise Density	f = 1 kHz		--	1	--	fA/√Hz
Shutdown Characteristics							
t_{on}	Amplifier Turn-On Time	BW = 8.192 MHz, T_A = -40 °C to +125 °C	V_{CM} = V_{DDA}/2, R_L = 50 kΩ	--	2.143	6.095	µs
			V_{DDA} > V_{CM} > (V_{DDA} - 1.3) R_L = 50 kΩ	--	2.166	6.070	µs
		BW = 128 kHz, T_A = -40 °C to +125 °C	V_{CM} = V_{DDA}/2, R_L = 50 kΩ	--	25.177	43.158	µs
			V_{DDA} > V_{CM} > (V_{DDA} - 1.3) R_L = 50 kΩ	--	34.769	70.602	µs
t_{off}	Amplifier Turn-Off Time	T_A = -40 °C to +125 °C R_L = 50 kΩ		--	0.653	1.083	µs
Comparator Mode							
t_{PHL}	Propagation Delay Output High to Low	Vref = 2.048 mV, Overdrive = 100 mV, Charge Pump is always On	BW = 128 kHz	--	23.6	41.3	µs
			BW = 512 kHz	--	10.8	19.1	µs
			BW = 2.048 MHz	--	6.8	12.6	µs
			BW = 8.192 MHz	--	5.6	11.0	µs
t_{PLH}	Propagation Delay Output Low to High		BW = 128 kHz	--	24.6	42.2	µs
			BW = 512 kHz	--	10.6	18.4	µs
			BW = 2.048 MHz	--	6.5	11.7	µs
			BW = 8.192 MHz	--	5.4	9.8	µs

[1] AGND = GND, unless otherwise noted.
[2] Equivalent offset voltage of the amplifier after user's trim using digital rheostat. Gain of the amplifier is G = 200 and the zero output voltage level V_{zero} = V_{DD}/2 (See Section 10.2.1 Operational Amplifier Mode)
[3] Op amps analog supporting blocks are always turned on.

3.15 100K Digital Rheostat Specifications

Table 27. 100K Digital Rheostat ES at V_A=V_{DD}, V_B=GND, T_A=-40°C to +125°C, V_{DD}=2.4V to 5.5V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{DR}	Rheostat Pin Voltage Range	Voltage between any (A or B) pins and AGND	AGND	--	V_{DDA}	V
R_{DR}	Digital Rheostat Resistance	Full resistance with all switches open[1]	94.426	101.582	113.741	kΩ
R_{DR_MIN}	Minimal Rheostat Resistance	Code = 0x00	43.679	--	94.863	Ω
R_{MATCH}	Mismatch between rheostats	Code = 0x3FF, T_A = 25 °C	--	0.084	--	%
Number of taps			--	--	1024	
$BWDT_{DR}$	Digital Rheostat Bandwidth	Frequency applied on one side of resistor chain and -3 dB frequency measured at the other side with full 100 kΩ, assume no additional load	--	50	--	kHz
R_S	Step Resistance	V_{DD} = (2.4 V; 3.3 V; 5.5 V) V_{AB} = (1 V; -1 V) T_A = 25 °C	--	99.236	--	Ω
I_{DR_MAX}	Max current through Rheostat	T_A = 25 °C	--	--	2	mA
E_{SW_N}	Resistor Noise Voltage	R_{AB} = 25 kΩ, f = 1 kHz	--	30	--	nV/√Hz
f_{ChACMP}	Chopper Comparator Switching Frequency		--	--	30	kHz
V_{Ch_offset}	Chopper comparator offset when Auto-Trim process is active		--	100	300	μV
f_{DR_CLK}	Counter Frequency independent from the Rheostat	The counter frequency is determined by user selection	0	--	25	MHz
f_{DR_SWCH}	Rheostat Switch Speed[2]	V_A = 5 V, V_B = 0 V, ±1 LSB error band, Auto-Trim or Fast mode	--	--	100	kHz
		V_A = 5 V, V_B = 0 V, ±1 LSB error band, regular mode	--	--	1	kHz
T_{settle}	Settling Time	Fast mode, I^2C code change from 0 to 1023	--	--	50	μs
		Fast mode, Rheostat 1 bit code change	--	--	10	μs
C_{DR}	Maximum Capacitance of A, B pins Measured to AGND	All switches are ON, f = 200 kHz	--	33.152	--	pF
I_{LKG}	Leakage Current	Including active charge pump current consumption	--	--	1000	nA
Error ZScale	Zero-Scale Error	Code = 0x00	--	--	0.867	LSB
INL	Integral Non-linearity		--	--	±2	LSB
DNL	Differential Non-linearity		--	--	±1	LSB

Table 27. 100K Digital Rheostat ES at V_A=V_{DD}, V_B=GND, T_A=-40°C to +125°C, V_{DD}=2.4V to 5.5V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
$BWDT_{CAP}$	Bandwidth -3 dB (Load = 30 pF)	$R_{RHEOSTAT}$ < 12.5 kΩ	--	240	--	kHz
		$R_{RHEOSTAT}$ = 12.5 kΩ to 25 kΩ	--	120	--	kHz
		$R_{RHEOSTAT}$ = 25 kΩ to 50 kΩ	--	60	--	kHz
		$R_{RHEOSTAT}$ = 50 kΩ to 100 kΩ	--	30	--	kHz
αR(T)	Resistance Temperature Coefficient	V_{AB} = const,	-119.694	0	196.287	ppm/°C

[1] User can calculate actual Digital Rheostat value using calibration data from NVM (see Section 12.2 Calculating Actual Resistance).
[2] Includes internal timing. External circuit should be counted separately.

3.16 Analog Switches Specifications

Table 28. Analog Switch0/Voltage Regulator ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{AS}	Maximum Voltage at Pins	Voltage between any Analog Switch pin to AGND	0	--	V_{DD} + 0.3	V
f_{MAX}	Maximum Switching Frequency	Pull Up	1806	--	--	kHz
		Pull Up, V_{DD} = 2.4 V	3591	--	--	kHz
		Pull Down	363	--	--	kHz
		Pull Down, V_{DD} = 2.4 V	363	--	--	kHz
R_{ON}	ON Resistance	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T_A = 25 °C	--	30	53.4	Ω
		V_{DD} = 3.3 V, V_{IN} > V_{DD} - 1.2, P-ch FET, T_A = 25 °C	--	2	3.0	Ω
I_{PWROFF}	OFF Leakage Current	Switch OFF; from IN to OUT V_A = V_{DD} or V_B = V_{DD}	--	--	1000	nA
I_{SW_MAX}	Maximum ON-state Switch Current	V_A = V_{DD}, load connected to ground, V_{AB}= 0.4 V	--	--	300	mA
I_{SW_PULSE}	Maximum Pulse Current Through Switch	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

Table 29. Analog Switch1/Current Sink ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{AS}	Maximum Voltage at Pins	Voltage between any Analog Switch pin to AGND	0	--	V_{DD} + 0.3	V
f_{MAX}	Maximum Switching Frequency	Pull Up	1600	--	--	kHz
		Pull Up, V_{DD} = 2.4 V	1600	--	--	kHz
		Pull Down	3920	--	--	kHz
		Pull Down, V_{DD} = 2.4 V	3920	--	--	kHz

Table 29. Analog Switch1/Current Sink ES at T_A = -40 °C to +125 °C, V_{DD} = 2.4 V to 5.5 V Unless Otherwise Noted

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{ON}	ON Resistance	V_{DD} = 3.3 V, V_{IN} < 1.2 V, N-ch FET, T_A = 25 °C	--	1	1.6	Ω
		V_{DD} = 3.3 V, V_{IN} > V_{DD} - 1.2, P-ch FET, T_A = 25 °C	--	53	203.9	Ω
I_{PWROFF}	OFF Leakage Current	Switch OFF; from IN to OUT, V_A = V_{DD} or V_B = V_{DD}	--	--	1000	nA
I_{SW_MAX}	Maximum ON-state Switch Current	V_A = V_{DD}, load connected to ground, V_{AB}= 0.4 V	--	--	250	mA
I_{SW_PULSE}	Maximum Pulse Current Through Switch	Pulse duration = 1 ms, Duty cycle < 5 %	--	--	500	mA

4. User Programmability

The SLG47004-A is a user programmable device with One-Time-Programmable (OTP) memory elements that are able to configure the connection matrix and macrocells. A programming development kit allows the user the ability to create initial devices. Once the design is finalized, the programming code (.aap file) is forwarded to Renesas Electronics Corporation to integrate into a production process.

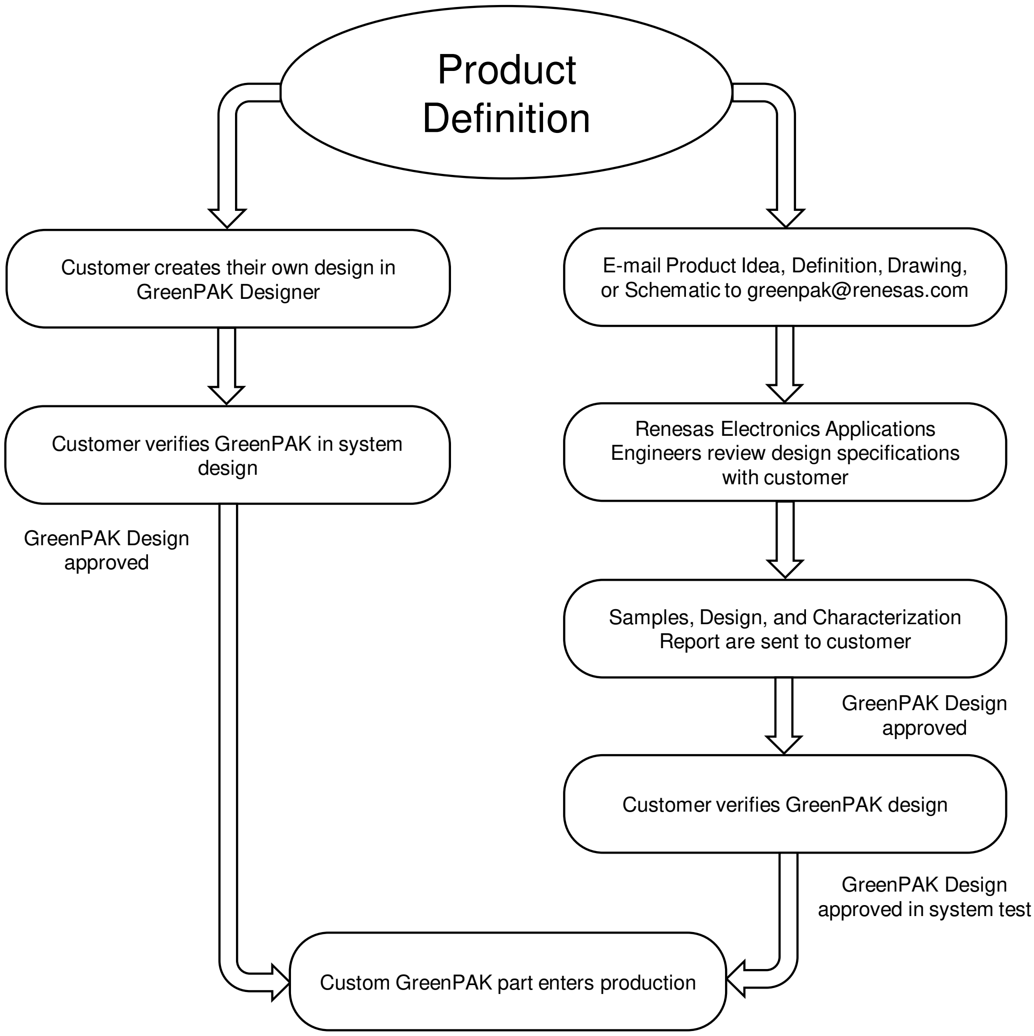


Figure 3. Steps to Create a Custom GreenPAK Device

5. I/O Pins

The SLG47004-A has a total of 7 GPIO Pins which can function as either a user-defined input or output, as well as serve as a special function (such as outputting the voltage reference) and 1 GPI Pin.

5.1 GPIO Pins

IO0, IO1, IO2, IO3, IO4, IO5, and IO6 serve as general purpose IO pins.

5.2 GPI Pin

I0 serves as general purpose input pin. It is strongly recommended to connect I0 (Pin21) to the ground if it is not used in the project.

5.3 Pull-Up/Down Resistors

All IO pins have the option of user-selectable resistors that can be connected to the pin structure. The selectable values on these resistors are 10 kΩ, 100 kΩ, and 1 MΩ. The internal resistors can be configured as either pull-up or pull-downs.

5.4 Fast Pull-Up/Down During Power-Up

During power-up, IO pull-up/down resistance will switch to 2.6 kΩ initially and then it will switch to normal setting value. This function is enabled by register [1207].

5.5 I²C Mode IO Structure

5.5.1 I²C Mode Structure (for SCL and SDA)

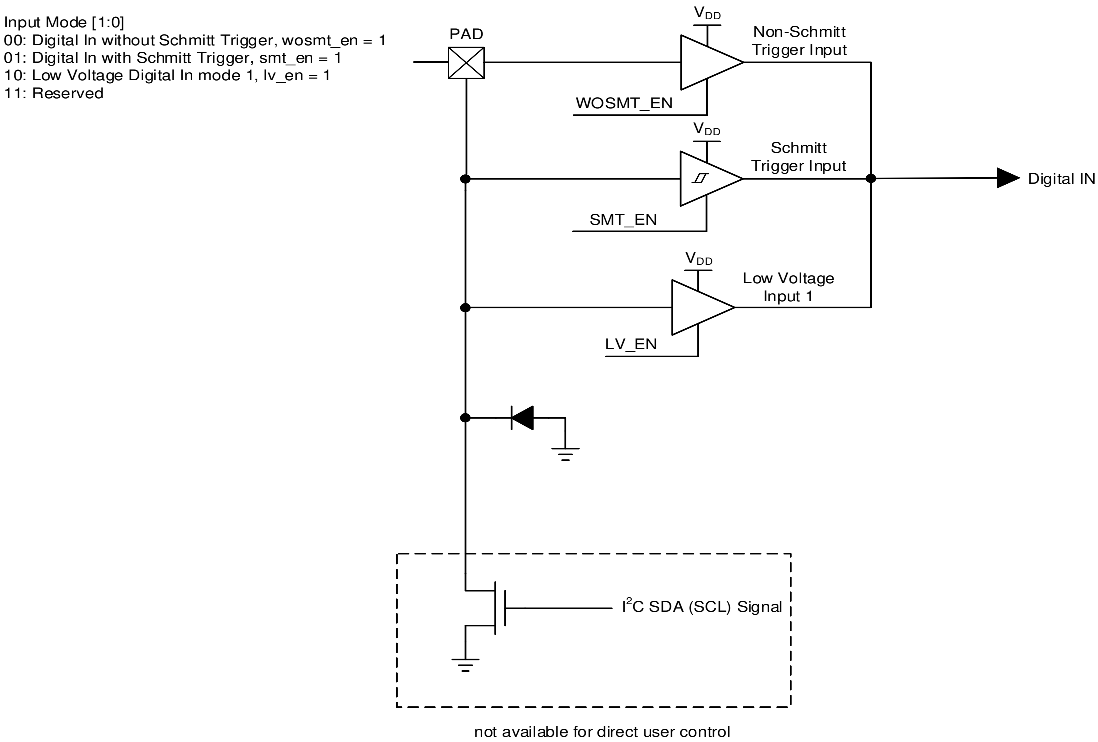


Figure 4. IO with I²C Mode IO Structure Diagram

5.6 Matrix OE IO Structure

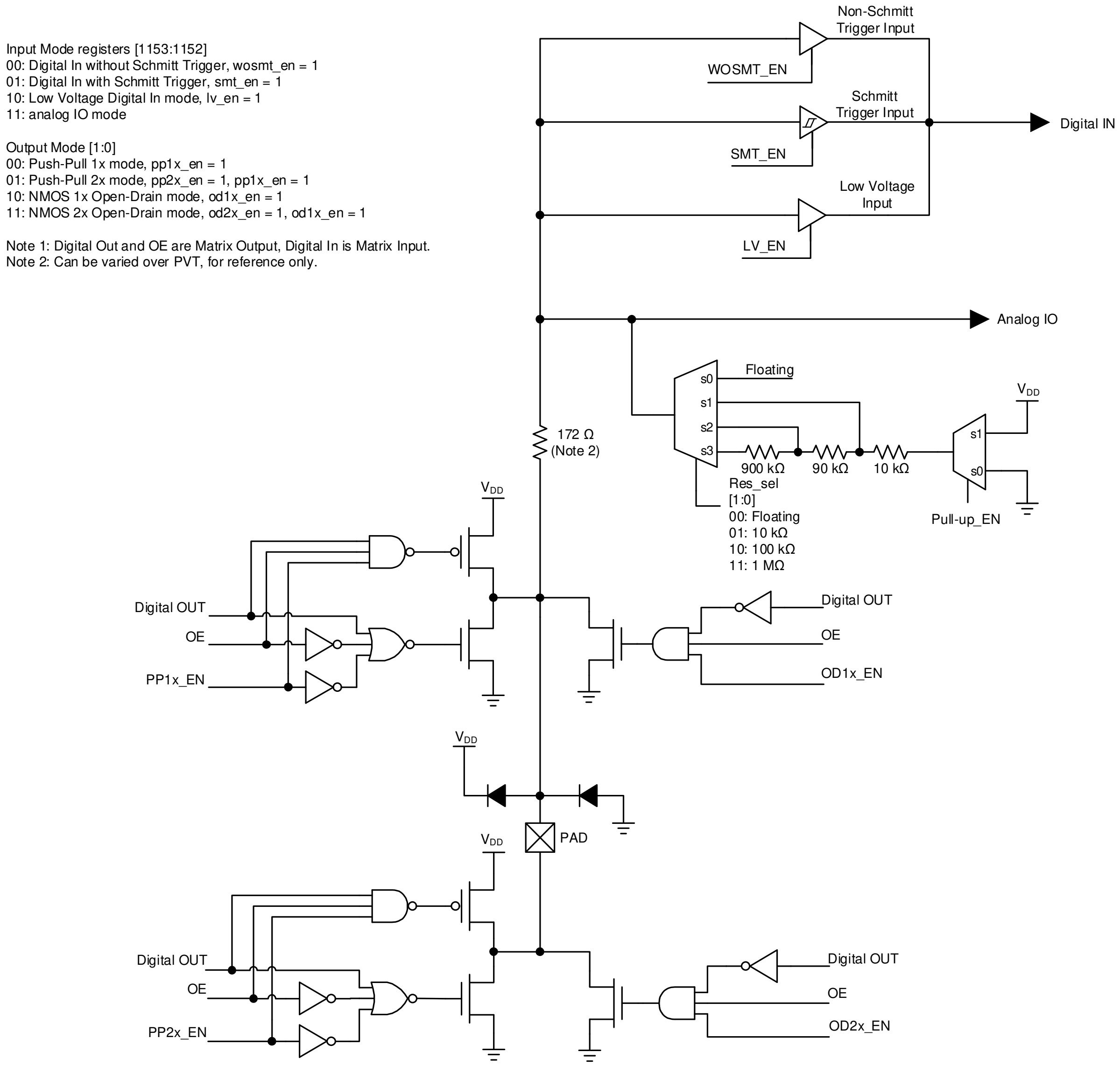


Figure 5. Matrix OE IO Structure Diagram

5.7 GPI Structure

5.7.1 GPI Structure (for I0)

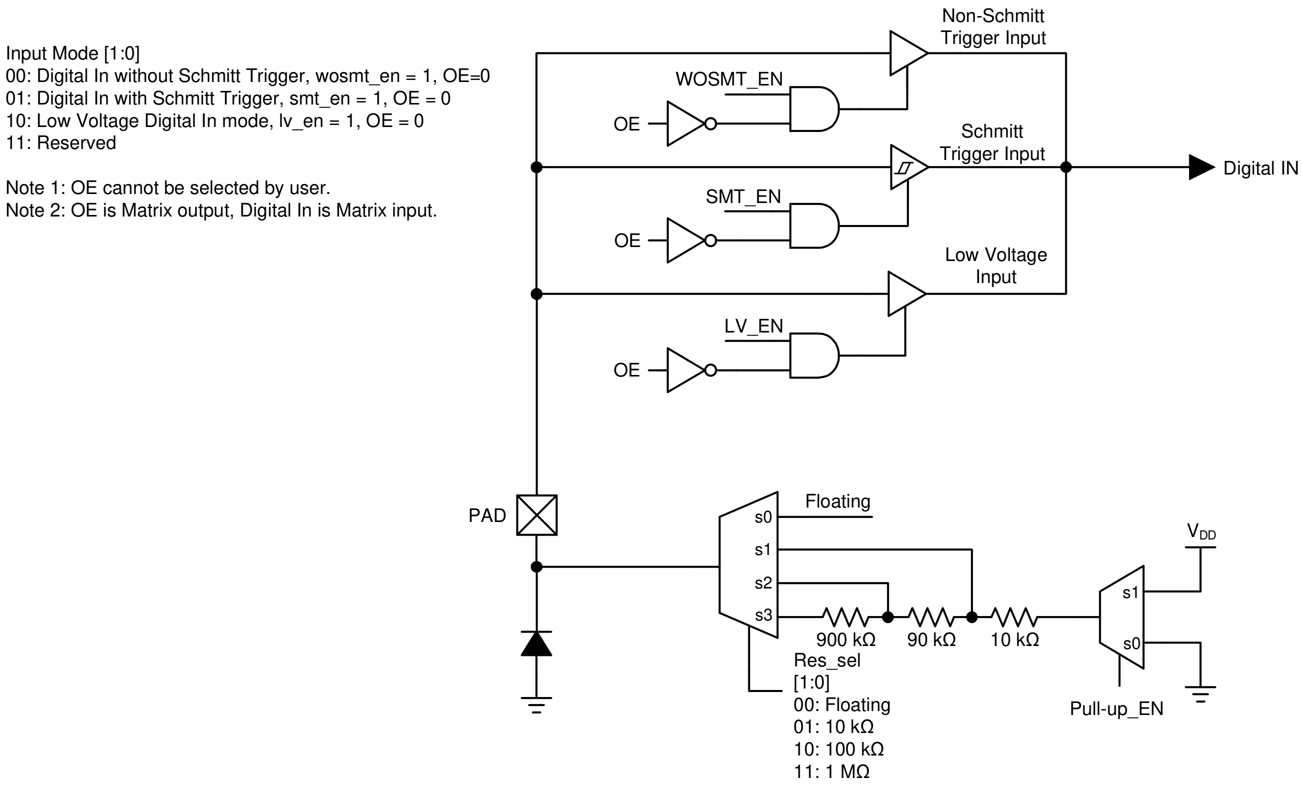


Figure 6. IO0 GPI Structure Diagram

5.8 IO Pins Typical Performance

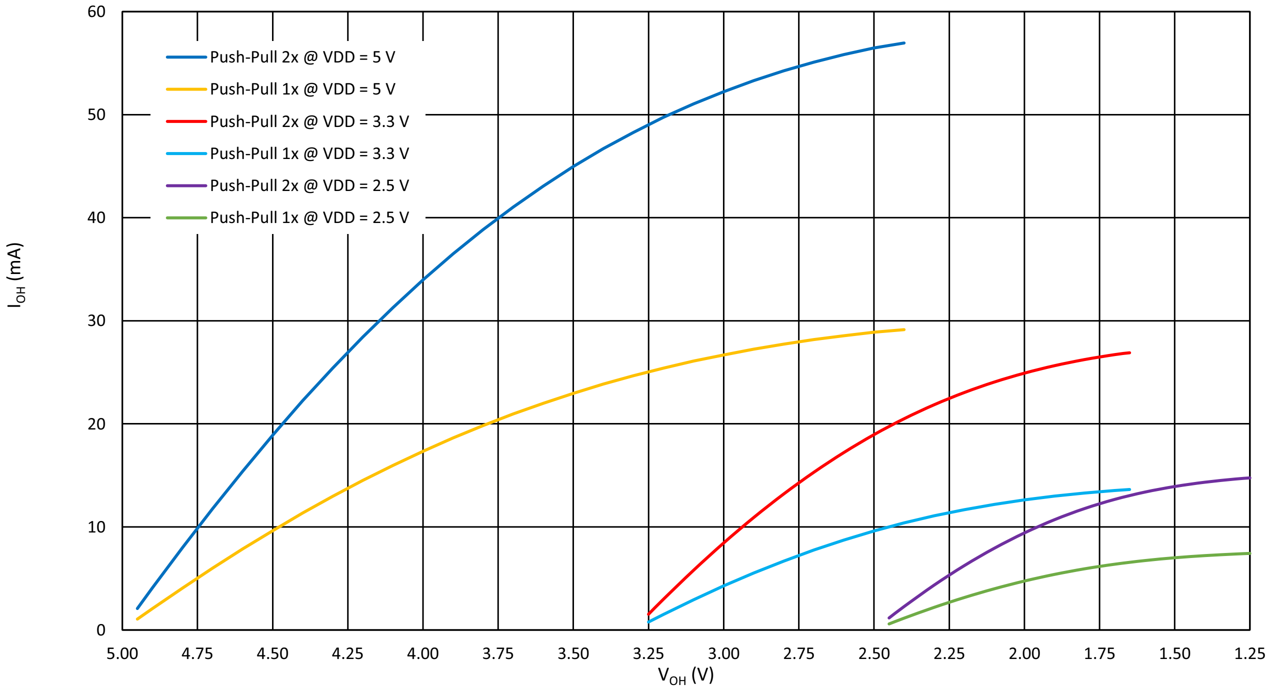


Figure 7. Typical High Level Output Current vs. High Level Output Voltage at T_A = 25 °C

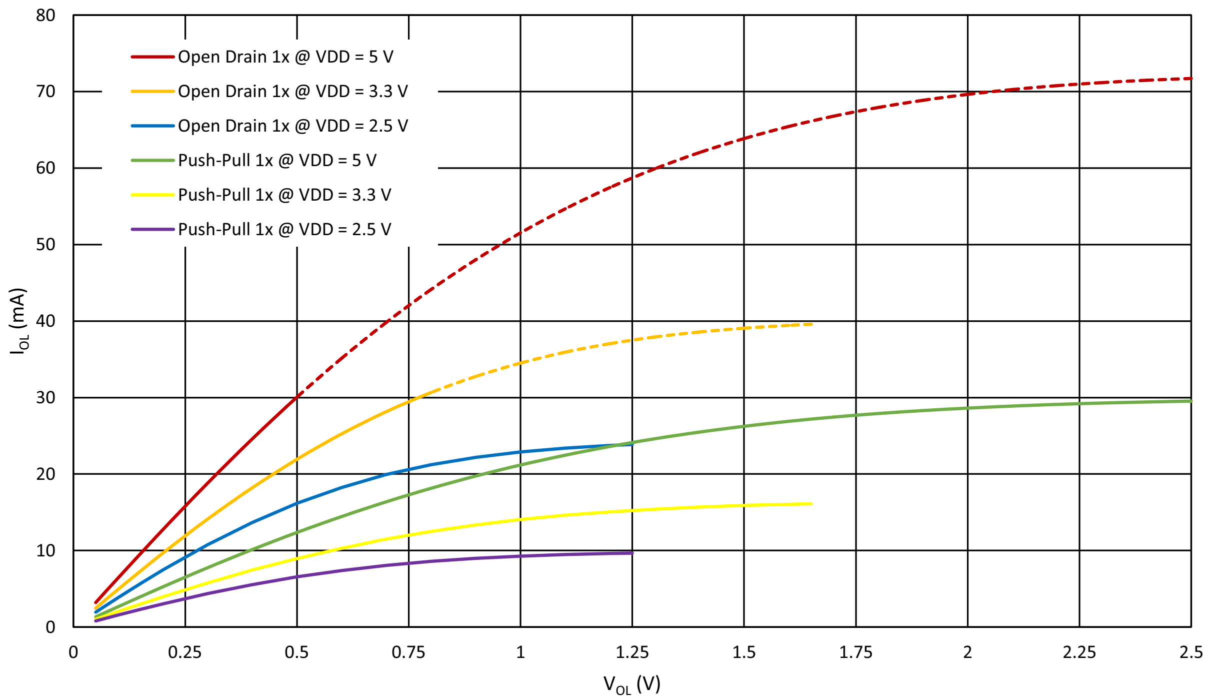


Figure 8. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C, Full Range

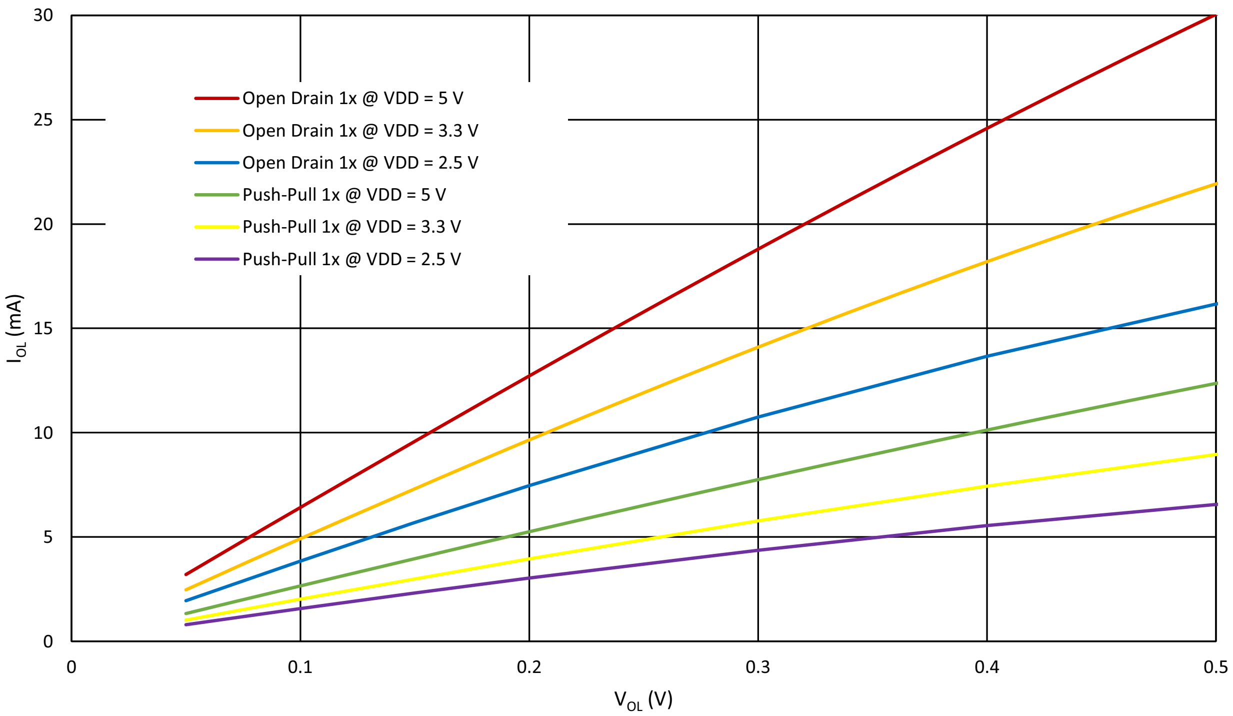


Figure 9. Typical Low Level Output Current vs. Low Level Output Voltage, 1x Drive at T_A = 25 °C

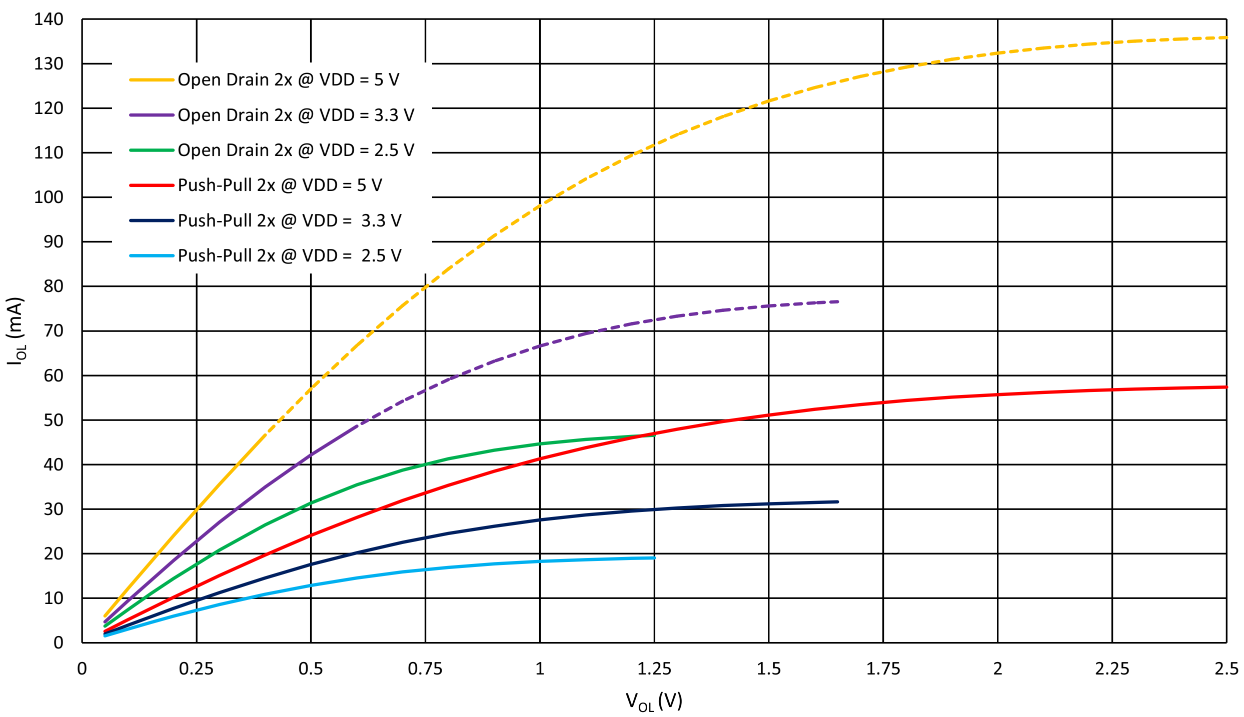


Figure 10. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C, Full Range

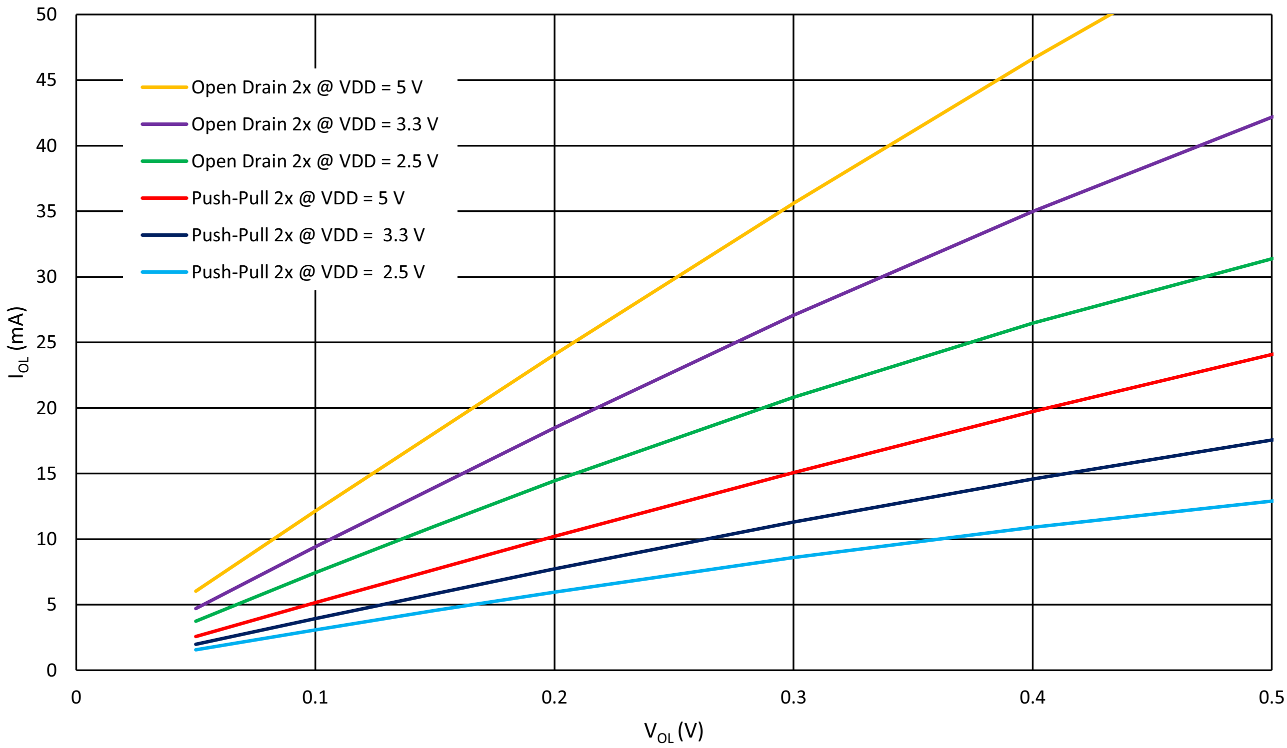


Figure 11. Typical Low Level Output Current vs. Low Level Output Voltage, 2x Drive at T_A = 25 °C

6. Connection Matrix

6.1 Connection Matrix Structure

The Connection Matrix in the SLG47004-A is used to create an internal routing for internal functional macrocells of the device once it is programmed. The output of each functional macrocell within the SLG47004-A has a specific digital bit code assigned to it, that is either set to active "High" or inactive "Low", based on the design that is created. Once the 2048 register bits within the SLG47004-A are programmed, a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 99 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to the digital output of a particular source macrocell, including IOs, LUTs, analog comparators, other digital resources, such as V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

For a complete list of the SLG47004-A's register table, see Section 21. Register Definitions.

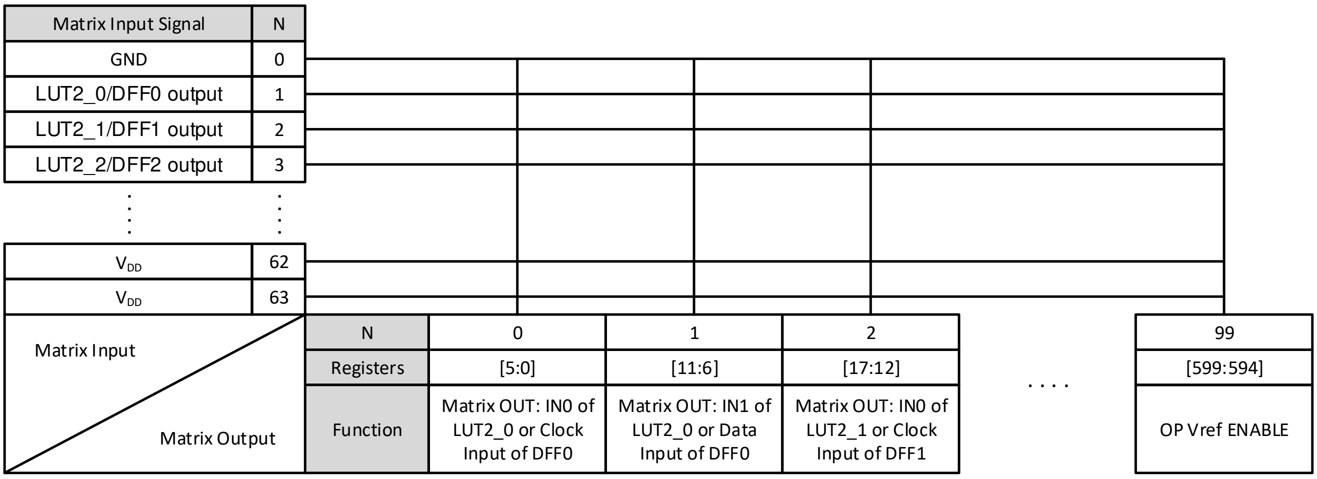


Figure 12. Connection Matrix

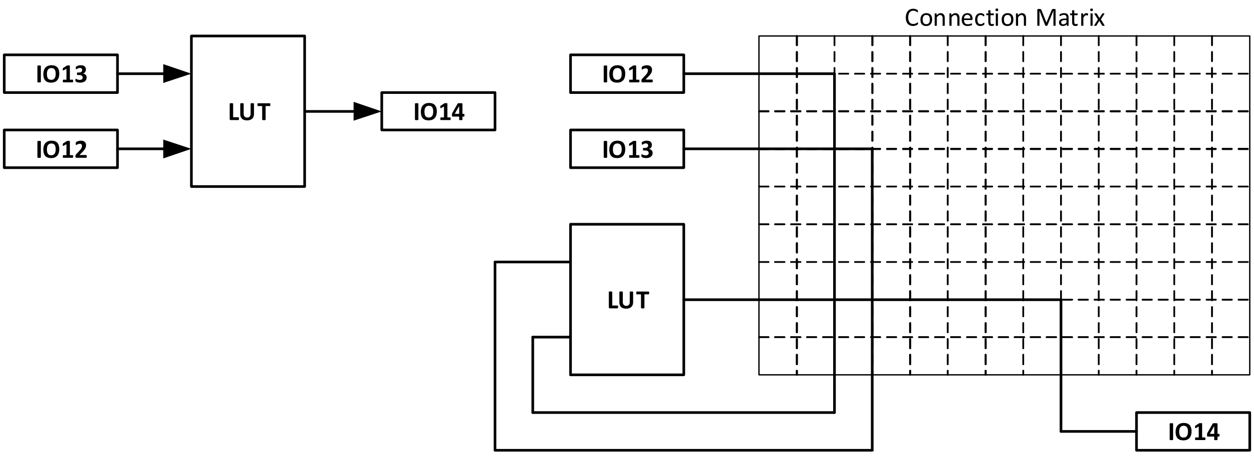


Figure 13. Connection Matrix Example

6.2 Matrix Input Table

Table 30. Matrix Input Table

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	LUT2_0/DFF0 output	0	0	0	0	0	1
2	LUT2_1/DFF1 output	0	0	0	0	1	0
3	LUT2_2/DFF2 output	0	0	0	0	1	1
4	LUT2_3/PGen output	0	0	0	1	0	0
5	LUT3_0/DFF3 output	0	0	0	1	0	1
6	LUT3_1/DFF4 output	0	0	0	1	1	0
7	LUT3_2/DFF5 output	0	0	0	1	1	1
8	LUT3_3/DFF6 output	0	0	1	0	0	0
9	LUT3_4/DFF7 output	0	0	1	0	0	1
10	LUT3_5/DFF8 output	0	0	1	0	1	0
11	LUT3_6/DFF9 output	0	0	1	0	1	1
12	CNT_DLY0 output	0	0	1	1	0	0
13	MLT0_LUT4_1/DFF17_OUT	0	0	1	1	0	1
14	CNT_DLY1 output	0	0	1	1	1	0
15	MLT1_LUT3_7/DFF11_OUT	0	0	1	1	1	1
16	CNT_DLY2 output	0	1	0	0	0	0
17	MLT2_LUT3_8/DFF12_OUT	0	1	0	0	0	1
18	CNT_DLY3 output	0	1	0	0	1	0
19	MLT3_LUT3_9/DFF13_OUT	0	1	0	0	1	1
20	CNT_DLY4 output	0	1	0	1	0	0
21	MLT4_LUT3_10/DFF14_OUT	0	1	0	1	0	1
22	CNT_DLY5 output	0	1	0	1	1	0
23	MLT5_LUT3_11/DFF15_OUT	0	1	0	1	1	1
24	CNT_DLY6 output	0	1	1	0	0	0
25	MLT6_LUT3_12/DFF16_OUT	0	1	1	0	0	1
26	LUT3_13/Pipe Delay/RippleCNT_out0	0	1	1	0	1	0
27	Pipe Delay/RippleCNT_out1	0	1	1	0	1	1
28	Pipe Delay/RippleCNT_out2	0	1	1	1	0	0
29	LUT4_0/DFF10 output	0	1	1	1	0	1
30	Programmable Delay Edge Detect Output	0	1	1	1	1	0
31	Edge Detect Filter Output	0	1	1	1	1	1
32	I^2C_virtual_0 Input	1	0	0	0	0	0
33	I^2C_virtual_1 Input	1	0	0	0	0	1
34	I^2C_virtual_2 Input	1	0	0	0	1	0

Table 30. Matrix Input Table (Cont.)

Matrix Input Number	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
35	I^2C_virtual_3 Input	1	0	0	0	1	1
36	I^2C_virtual_4 Input	1	0	0	1	0	0
37	I^2C_virtual_5 Input	1	0	0	1	0	1
38	I^2C_virtual_6 Input	1	0	0	1	1	0
39	I^2C_virtual_7 Input	1	0	0	1	1	1
40	RH0 Idle/Active	1	0	1	0	0	0
41	RH1 Idle/Active	1	0	1	0	0	1
42	Output of Op Amp0 in ACMP mode	1	0	1	0	1	0
43	Output of Op Amp1 in ACMP mode	1	0	1	0	1	1
44	IO0 Digital Input	1	0	1	1	0	0
45	IO1 Digital Input	1	0	1	1	0	1
46	IO2 Digital Input	1	0	1	1	1	0
47	IO3 Digital Input	1	0	1	1	1	1
48	IO4 Digital Input	1	1	0	0	0	0
49	IO5 Digital Input	1	1	0	0	0	1
50	IO6 Digital Input	1	1	0	0	1	0
51	I0 Digital Input	1	1	0	0	1	1
52	Oscillator0 output 0	1	1	0	1	0	0
53	Oscillator1 output 0	1	1	0	1	0	1
54	Oscillator2 output	1	1	0	1	1	0
55	Chopper ACMP Out	1	1	0	1	1	1
56	ACMP0 Output (low speed)	1	1	1	0	0	0
57	ACMP1 Output (low speed)	1	1	1	0	0	1
58	Oscillator0 output 1	1	1	1	0	1	0
59	Oscillator1 output 1	1	1	1	0	1	1
60	POR OUT	1	1	1	1	0	0
61	V_{DD}	1	1	1	1	0	1
62	V_{DD}	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

6.3 Matrix Output Table

Table 31. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[5:0]	IN0 of LUT2_0 or Clock Input of DFF0	0
[11:6]	IN1 of LUT2_0 or Data Input of DFF0	1
[17:12]	IN0 of LUT2_1 or Clock Input of DFF1	2
[23:18]	IN1 of LUT2_1 or Data Input of DFF1	3
[29:24]	IN0 of LUT2_2 or Clock Input of DFF2	4
[35:30]	IN1 of LUT2_2 or Data Input of DFF2	5
[41:36]	IN0 of LUT2_3 or Clock Input of PGen	6
[47:42]	IN1 of LUT2_3 or nRST of PGen	7
[53:48]	IN0 of LUT3_0 or CLK Input of DFF3	8
[59:54]	IN1 of LUT3_0 or Data of DFF3	9
[65:60]	IN2 of LUT3_0 or nRST (nSET) of DFF3	10
[71:66]	IN0 of LUT3_1 or CLK Input of DFF4	11
[77:72]	IN1 of LUT3_1 or Data of DFF4	12
[83:78]	IN2 of LUT3_1 or nRST (nSET) of DFF4	13
[89:84]	IN0 of LUT3_2 or CLK Input of DFF5	14
[95:90]	IN1 of LUT3_2 or Data of DFF5	15
[101:96]	IN2 of LUT3_2 or nRST(nSET) of DFF5	16
[107:102]	IN0 of LUT3_3 or CLK Input of DFF6	17
[113:108]	IN1 of LUT3_3 or Data of DFF6	18
[119:114]	IN2 of LUT3_3 or nRST (nSET) of DFF6	19
[125:120]	IN0 of LUT3_4 or CLK Input of DFF7	20
[131:126]	IN1 of LUT3_4 or Data of DFF7	21
[137:132]	IN2 of LUT3_4 or nRST (nSET) of DFF7	22
[143:138]	IN0 of LUT3_5 or CLK Input of DFF8	23
[149:144]	IN1 of LUT3_5 or Data of DFF8	24
[155:150]	IN2 of LUT3_5 or nRST (nSET) of DFF8	25
[161:156]	IN0 of LUT3_6 or CLK Input of DFF9	26
[167:162]	IN1 of LUT3_6 or CLK Input of DFF9	27
[173:168]	IN2 of LUT3_6 or nRST (nSET) of DFF9	28
[179:174]	IN0 of LUT3_7 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)	29
[185:180]	IN1 of LUT3_7 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)	30
[191:186]	IN2 of LUT3_7 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)	31
[197:192]	IN0 of LUT3_8 or CLK Input of DFF12 Delay2 Input (or Counter2 nRST Input)	32

Table 31. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[203:198]	IN1 of LUT3_8 or nRST (nSET) of DFF12 Delay2 Input (or Counter2 nRST Input)	33
[209:204]	IN2 of LUT3_8 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)	34
[215:210]	IN0 of LUT3_9 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)	35
[221:216]	IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)	36
[227:222]	IN2 of LUT3_9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)	37
[233:228]	IN0 of LUT3_10 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)	38
[239:234]	IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)	39
[245:240]	IN2 of LUT3_10 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)	40
[251:246]	IN0 of LUT3_11 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)	41
[257:252]	IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	42
[263:258]	IN2 of LUT3_11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)	43
[269:264]	IN0 of LUT3_12 or CLK Input of DFF16 Delay6 Input (or Counter6 nRST Input)	44
[275:270]	IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay6 Input (or Counter6 nRST Input)	45
[281:276]	IN2 of LUT3_12 or Data of DFF16 Delay6 Input (or Counter6 nRST Input)	46
[287:282]	IN0 of LUT3_13 or Input of Pipe Delay or UP signal of RIPP CNT	47
[293:288]	IN1 of LUT3_13 or nRST of Pipe Delay or nSet of RIPP CNT	48
[299:294]	IN2 of LUT3_13 or CLK of Pipe Delay_RIPP CNT	49
[305:300]	IN0 of LUT4_0 or CLK of DFF10	50
[311:306]	IN1 of LUT4_0 or Data of DFF10	51
[317:312]	IN2 of LUT4_0 or nRST (nSET) of DFF10	52
[323:318]	IN3 of LUT4_0	53
[329:324]	IN0 of LUT4_1 or CLK Input of DFF17 Delay0 Input (or Counter0 nRST Input)	54
[335:330]	IN1 of LUT4_1 or nRST of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source	55
[341:336]	IN2 of LUT4_1 or nSet of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0	56
[347:342]	IN3 of LUT4_1 or Data of DFF17 Delay0 Input (or Counter0 nRST Input) UP Input of FSM0	57
[353:348]	Programmable delay/edge detect input	58

Table 31. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[359:354]	Filter/Edge detect input	59
[365:360]	IO0 DOUT	60
[371:366]	IO0 DOUT OE	61
[377:372]	IO1 DOUT	62
[383:378]	IO1 DOUT OE	63
[389:384]	IO2 DOUT	64
[395:390]	IO2 DOUT OE	65
[401:396]	IO3 DOUT	66
[407:402]	IO3 DOUT OE	67
[413:408]	IO4 DOUT	68
[419:414]	IO4 DOUT OE	69
[425:420]	IO5 DOUT	70
[431:426]	IO5 DOUT OE	71
[437:432]	IO6 DOUT	72
[443:438]	IO6 DOUT OE	73
[449:444]	Set of PT0 block	74
[455:450]	Clock of PT0 block	75
[461:456]	Reload of PT0 block	76
[467:462]	Reserved	77
[473:468]	Up/Down of PT0 block	78
[479:474]	Set of PT1 block	79
[485:480]	Clock of PT1 block	80
[491:486]	Reload of PT1 block	81
[497:492]	Reserved	82
[503:498]	Up/Down of PT1 block	83
[509:504]	FIFO Reset of PT blocks	84
[515:510]	Power Up of Chopper ACMP	85
[521:516]	Rheostats Charge Pump Enable	86
[527:522]	ASW0 enable/Half bridge Enable	87
[533:528]	ASW1 enable/Half bridge data	88
[539:534]	ACMP0 Power Up	89
[545:540]	ACMP1 Power Up	90
[551:546]	Oscillator0 Enable	91
[557:552]	Oscillator1 Enable	92
[563:558]	Oscillator2 Enable	93
[569:564]	VrefO, Temp sensor, VrefO Power Up	94

Table 31. Matrix Output Table (Cont.)

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
[575:570]	HDBUF Enable	95
[581:576]	Op Amp0 Power Up	96
[587:582]	Op Amp1 Power Up	97
[593:588]	Op Amp2 Power Up	98
[599:594]	Op amps Vref Enable	99
[1] For each Address, the two most significant bits are unused.		

6.4 Connection Matrix Virtual Inputs

As mentioned previously, the Connection Matrix inputs come from the outputs of various digital macrocells on the device. Eight of the Connection Matrix inputs have the special characteristic that the state of these signal lines comes from a corresponding data bit written as a register value via I^2C. This gives the user the ability to write data via the serial channel, and have this information translated into signals that can be driven into the Connection Matrix and from the Connection Matrix to the digital inputs of other macrocells on the device. The I^2C address for reading and writing these register values is at 0x7C (124).

An I^2C write command to these register bits will set the signal values going into the Connection Matrix to the desired state. A read command to these register bits will read either the original data values coming from the NVM memory bits (that were loaded during the initial device startup), or the values from a previous write command (if that has happened).

See table Table 32.

Table 32. Connection Matrix Virtual Inputs

Matrix Input Number	Matrix Input Signal Function	Register Bit Addresses (d)
32	I^2C_virtual_0 Input	[992]
33	I^2C_virtual_1 Input	[993]
34	I^2C_virtual_2 Input	[994]
35	I^2C_virtual_3 Input	[995]
36	I^2C_virtual_4 Input	[996]
37	I^2C_virtual_5 Input	[997]
38	I^2C_virtual_6 Input	[998]
39	I^2C_virtual_7 Input	[999]

6.5 Connection Matrix Virtual Outputs

The digital outputs of the various macrocells are routed to the Connection Matrix to enable interconnections to the inputs of other macrocells in the device. At the same time, it is possible to read the state of each of the macrocell outputs as a register value via I^2C. This option, called Connection Matrix Virtual Outputs, allows the user to remotely read the values of each macrocell output. The I^2C addresses for reading these register values are bytes 0xC4 (196) to 0xCA (202). Write commands to these same register values will be ignored (with the exception of the Virtual Input register bits at byte 0x7C (124)).

7. Combination Function Macrocells

The SLG47004-A has 13 combination function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells:

- Three macrocells that can serve as either 2-bit LUT or as D Flip-Flop
- Seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset Input
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay/Ripple Counter
- One macrocell that can serve as either 2-bit LUT or as Programmable Pattern Generator (PGen)
- One macrocell that can serve as either 4-bit LUT or as D Flip-Flop with Set/Reset Input.

Inputs/Outputs for the 13 combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of configuration bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user-defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

7.1 2-Bit LUT or D Flip-Flop Macrocells

There is one macrocell that can serve as either 2-bit LUT or as D Flip-Flop. When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

The operation of the D Flip-Flop and LATCH will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change.

LATCH: when CLK is Low, then Q = D; otherwise Q remains its previous value (input D has no effect on the output, when CLK is High).

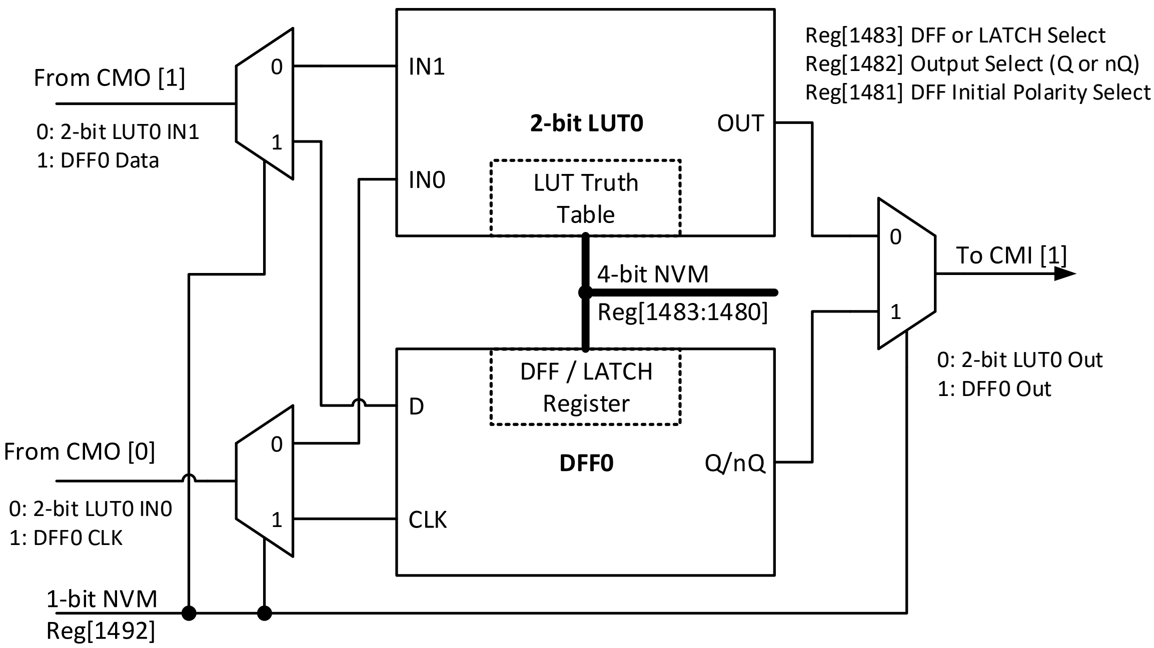


Figure 14. 2-bit LUT0 or DFF0

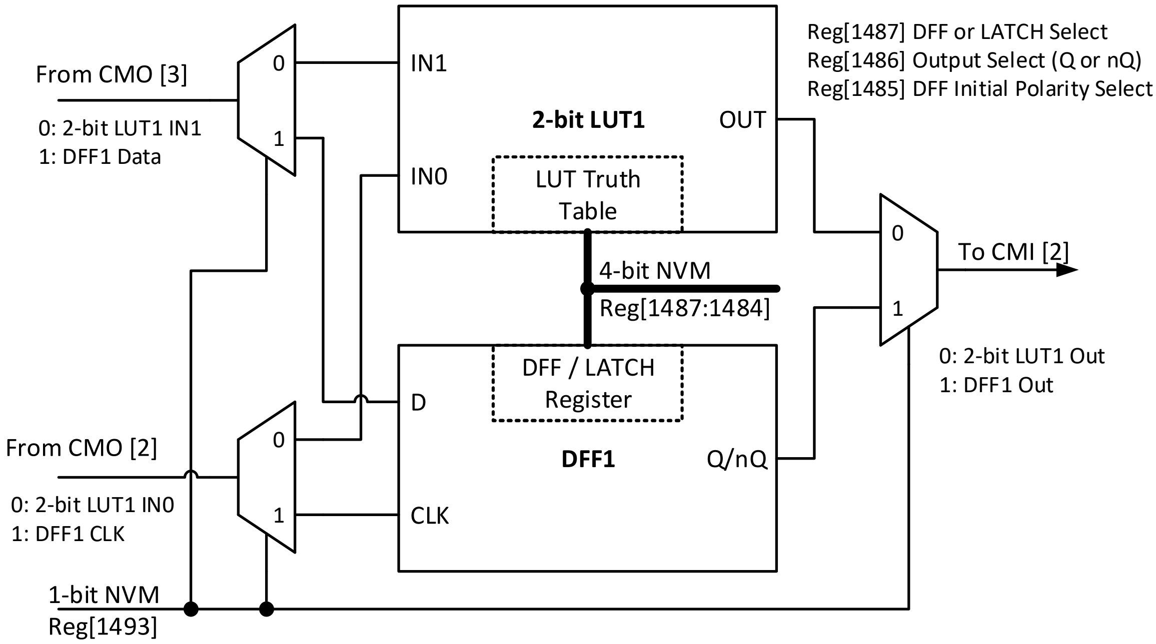


Figure 15. 2-bit LUT1 or DFF1

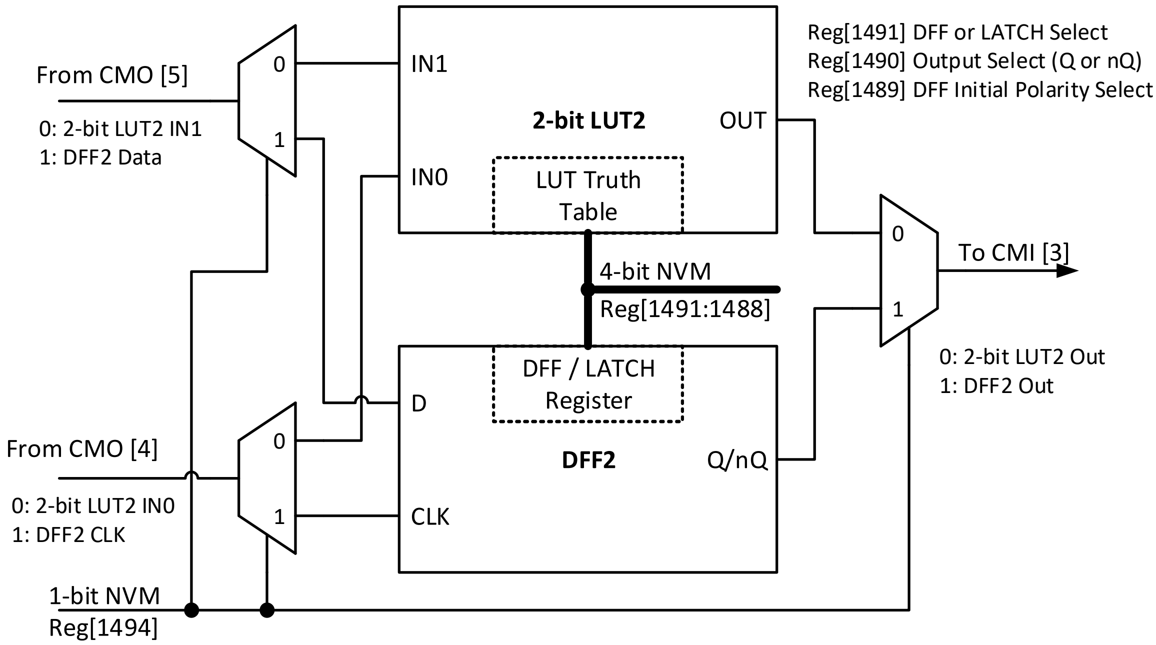


Figure 16. 2-bit LUT2 or DFF2

7.1.1 2-Bit LUT or D Flip-Flop Macrocell Used as 2-Bit LUT

Table 33. 2-bit LUT0 Truth Table

IN1	IN0	OUT	
0	0	register [1480]	LSB
0	1	register [1481]	
1	0	register [1482]	
1	1	register [1483]	MSB

Table 34. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1484]	LSB
0	1	register [1485]	
1	0	register [1486]	
1	1	register [1487]	MSB

Table 35. 2-bit LUT2 Truth Table

IN1	IN0	OUT	
0	0	register [1488]	LSB
0	1	register [1489]	
1	0	register [1490]	
1	1	register [1491]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT0 is defined by registers [1483:1480]

2-bit LUT1 is defined by registers [1487:1484]

2-bit LUT2 is defined by registers [1491:1488]

Table 36 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 36. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.1.2 Initial Polarity Operations

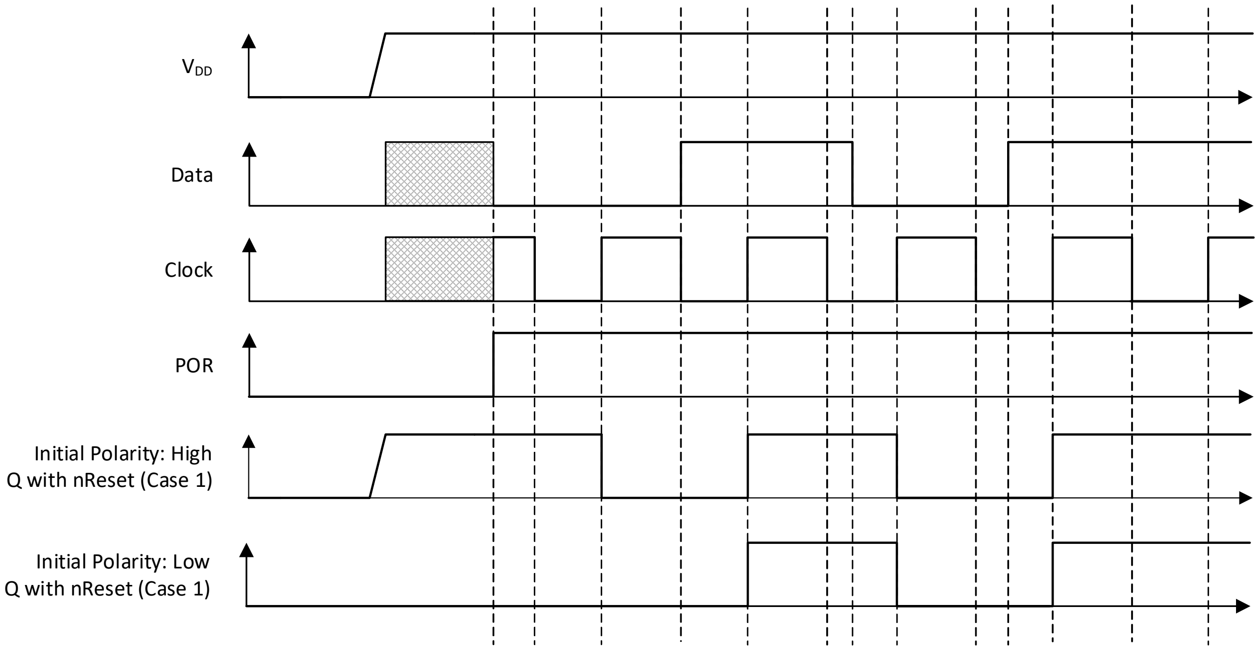


Figure 17. DFF Polarity Operations

7.2 2-bit LUT or Programmable Pattern Generator

The SLG47004-A has one combination function macrocell that can serve as a logic or a timing function. This macrocell can serve as a Look Up Table (LUT), or a Programmable Pattern Generator (PGen).

When used to implement LUT functions, the 2-bit LUT takes in two input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used as a LUT to implement combinatorial logic functions, the outputs of the LUT can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR). The user can also define the combinatorial relationship between inputs and outputs to be any selectable function.

It is possible to define the RST level for the PGen macrocell. There are both high level reset (RST) and a low level reset (nRST) options available, which are selected by register [1517]. When operating as the Programmable Pattern Generator, the output of the macrocell will clock out a sequence of two to sixteen bits that are user selectable in their bit values, and user selectable in the number of bits (up to sixteen) that are output before the pattern repeats.

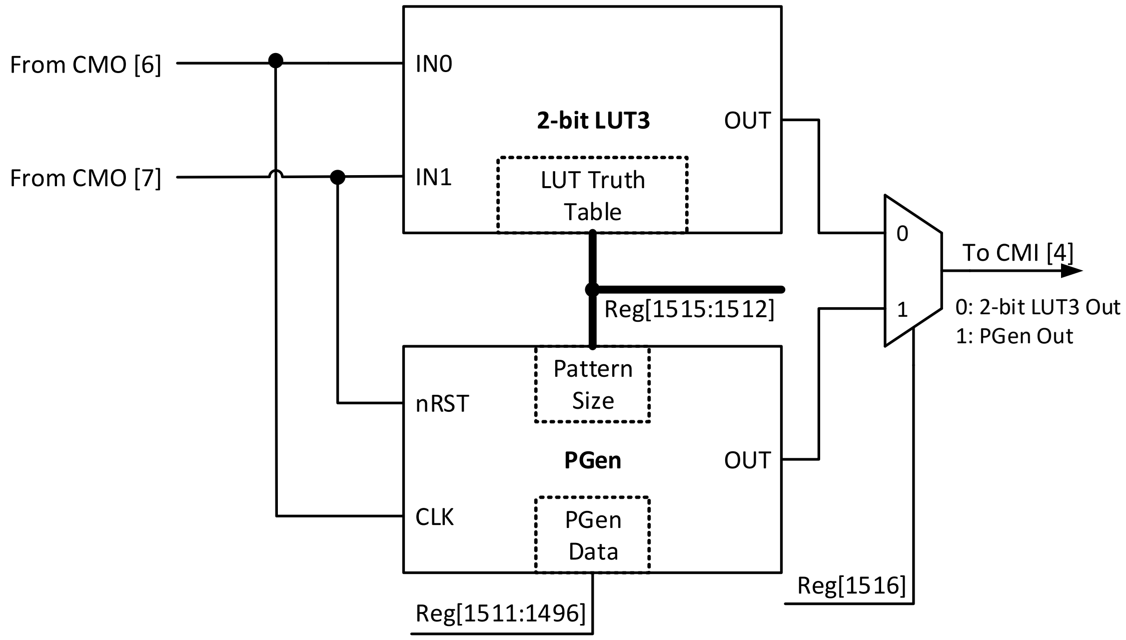


Figure 18. 2-bit LUT3 or PGen

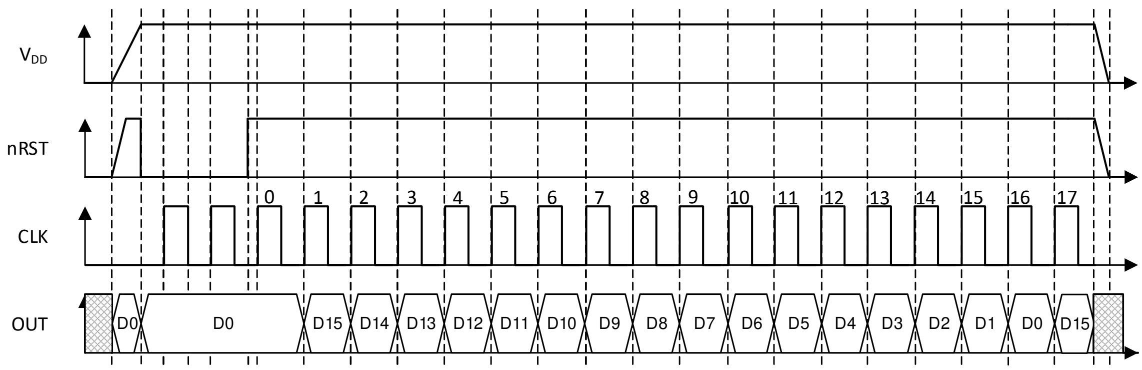


Figure 19. PGen Timing Diagram

7.2.1 2-Bit LUT or PGen Macrocell Used as 2-Bit LUT

Table 37. 2-bit LUT1 Truth Table

IN1	IN0	OUT	
0	0	register [1512]	LSB
0	1	register [1513]	
1	0	register [1514]	
1	1	register [1515]	MSB

This macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-bit LUT3 is defined by registers [1515:1512]

Table 38 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the 2-bit LUT logic cells.

Table 38. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

7.3 3-Bit LUT or D Flip-Flop with Set/Reset Macrocells

There are seven macrocells that can serve as either 3-bit LUTs or as D Flip-Flops with Set/Reset inputs. When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register [1523].

DFF3 operation will flow the functional description below:

- If register [1522] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.
- If register [1522] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK.

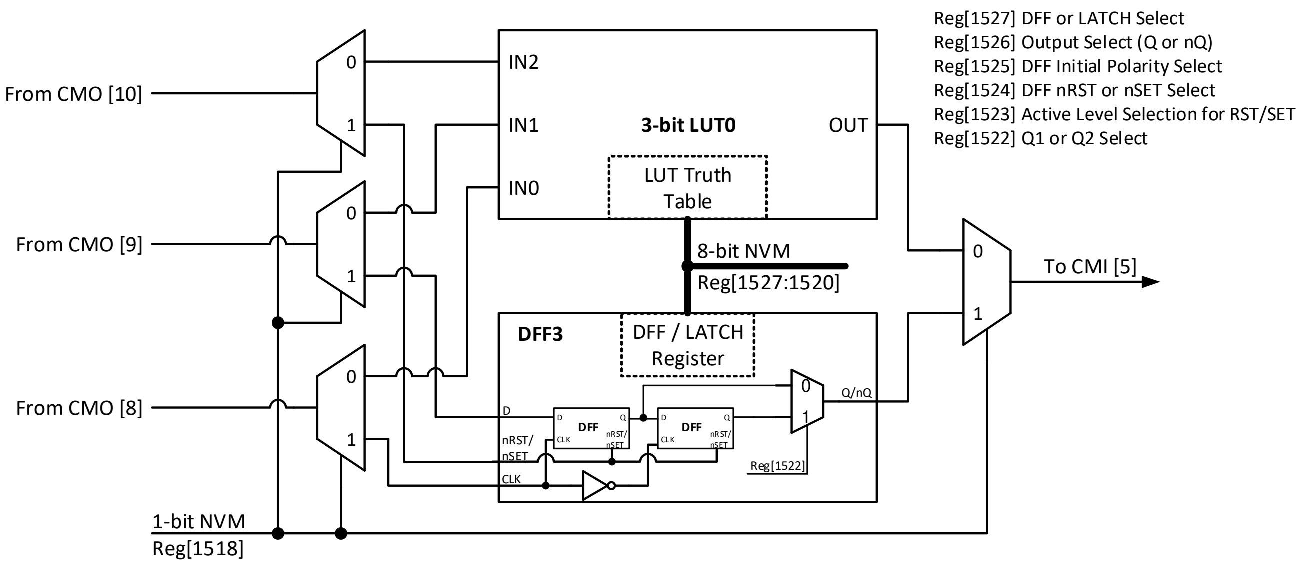


Figure 20. 3-bit LUT0 or DFF3

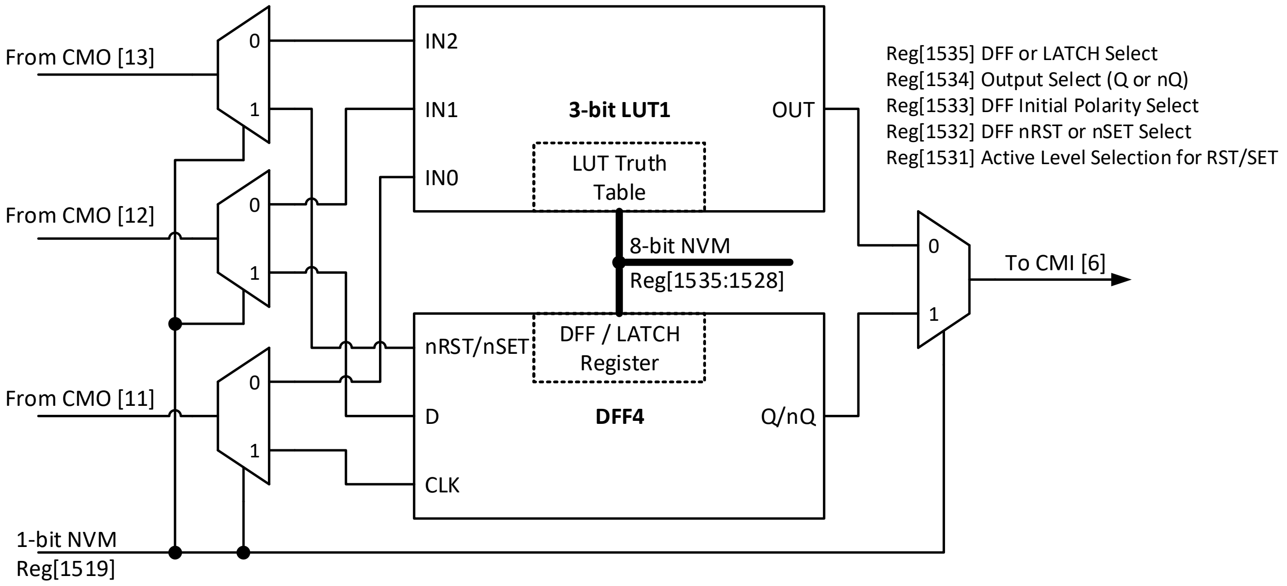


Figure 21. 3-bit LUT1 or DFF4

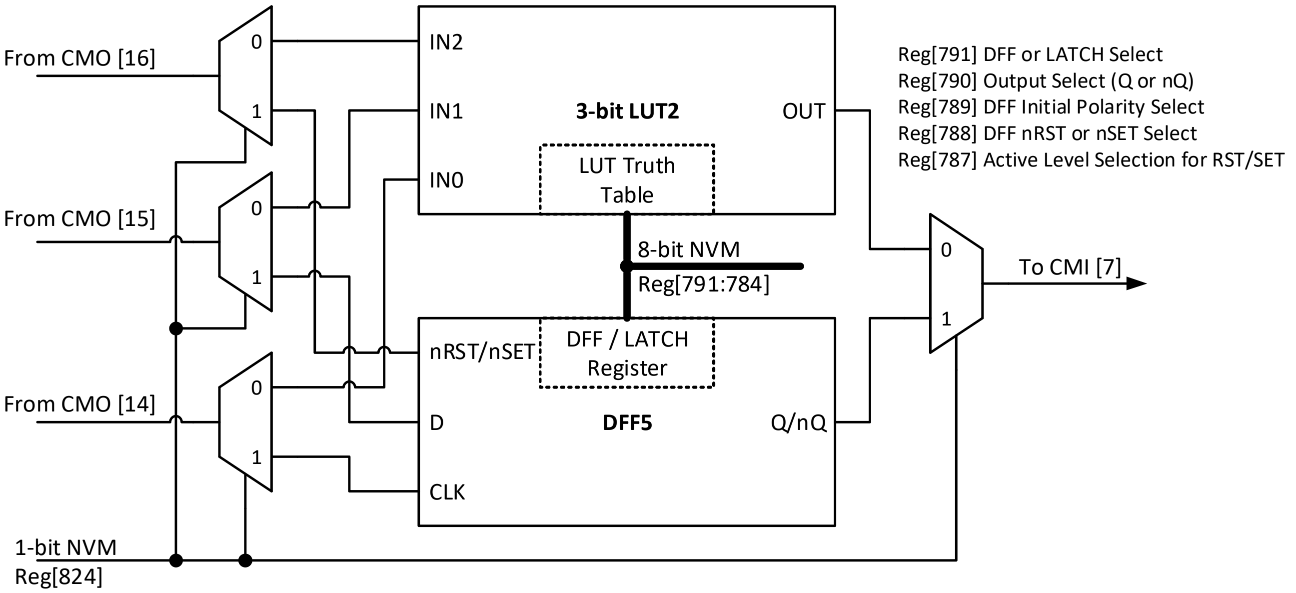


Figure 22. 3-bit LUT2 or DFF5

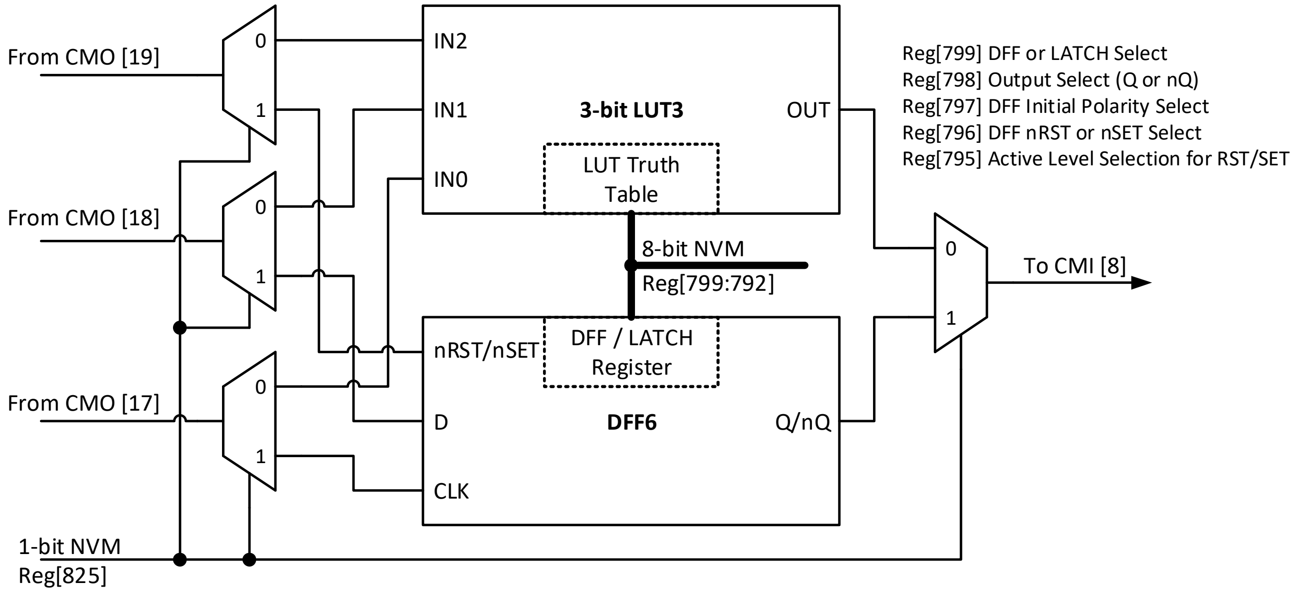


Figure 23. 3-bit LUT3 or DFF6

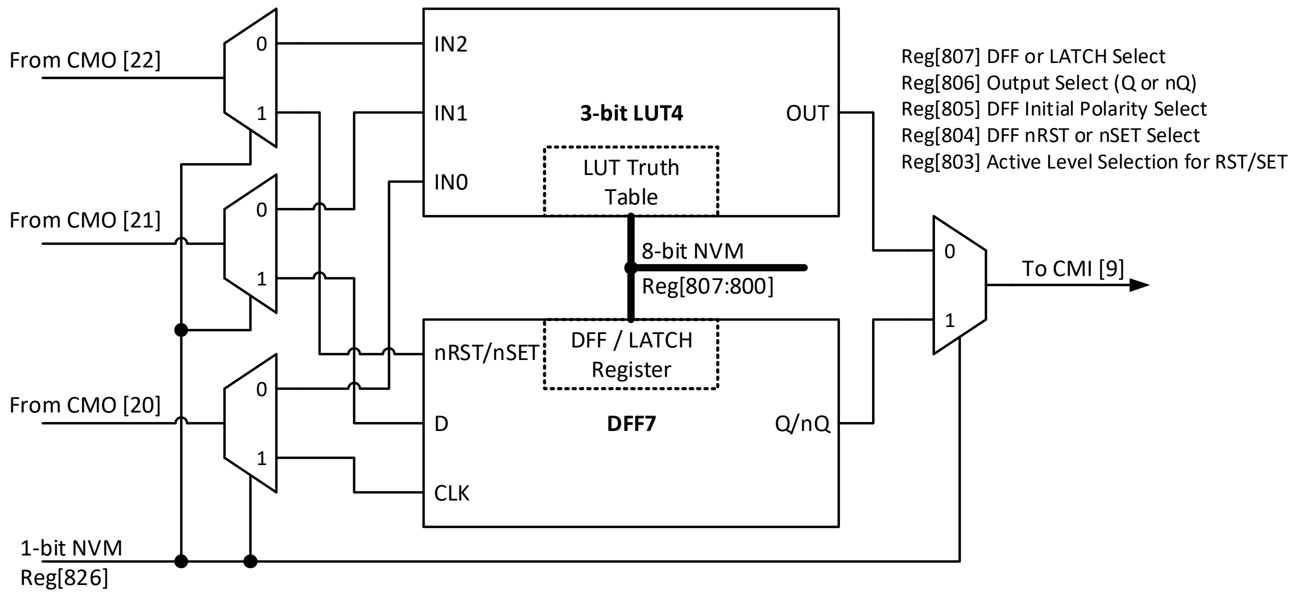


Figure 24. 3-bit LUT4 or DFF7

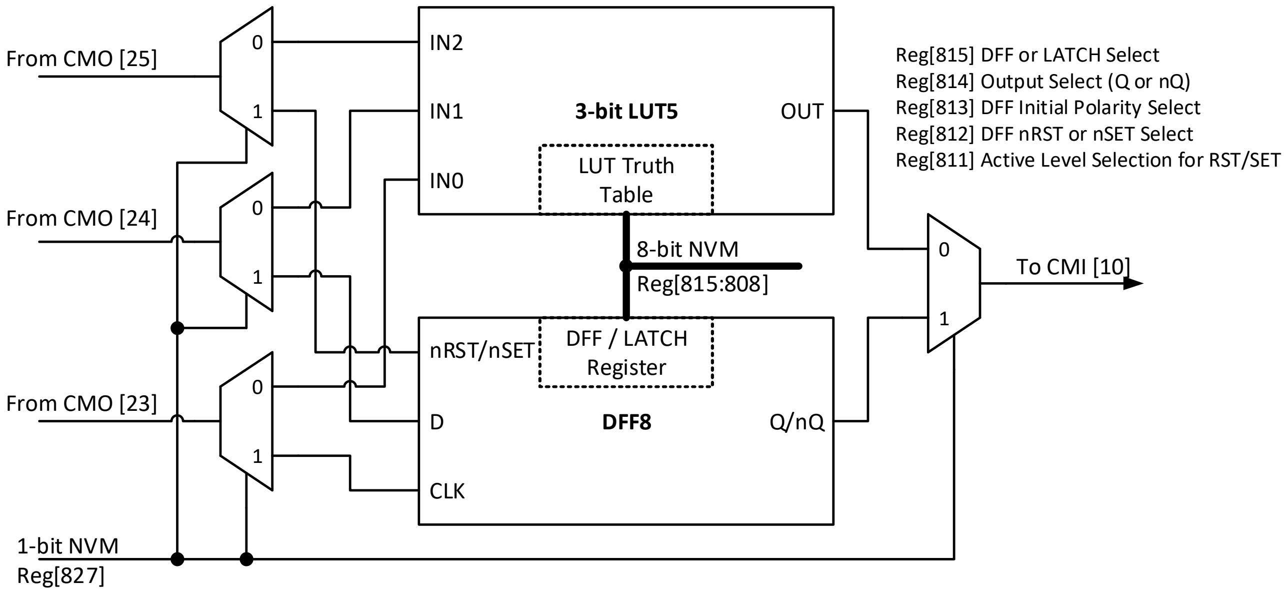


Figure 25. 3-bit LUT5 or DFF8

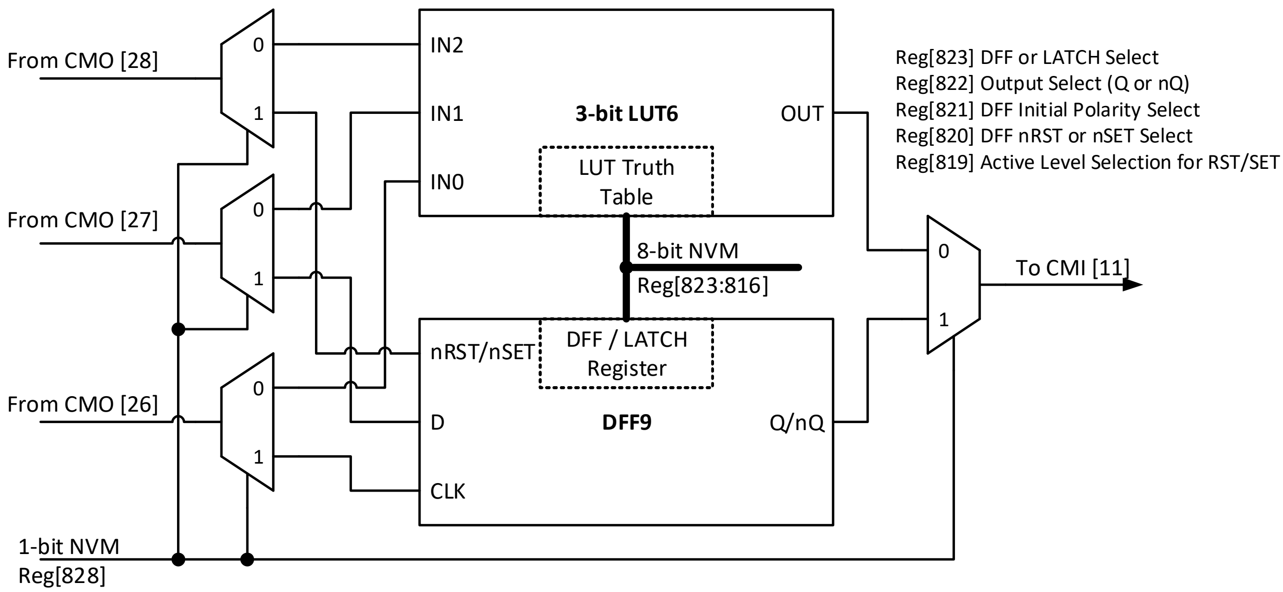


Figure 26. 3-bit LUT6 or DFF9

7.3.1 3-Bit LUT or D Flip-Flop Macrocells Used as 3-Bit LUTs

Table 39. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1520]	LSB
0	0	1	register [1521]	
0	1	0	register [1522]	
0	1	1	register [1523]	
1	0	0	register [1524]	
1	0	1	register [1525]	
1	1	0	register [1526]	
1	1	1	register [1527]	MSB

Table 40. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1528]	LSB
0	0	1	register [1529]	
0	1	0	register [1530]	
0	1	1	register [1531]	
1	0	0	register [1532]	
1	0	1	register [1533]	
1	1	0	register [1534]	
1	1	1	register [1535]	MSB

Table 41. 3-bit LUT2 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [784]	LSB
0	0	1	register [785]	
0	1	0	register [786]	
0	1	1	register [787]	
1	0	0	register [788]	
1	0	1	register [789]	
1	1	0	register [790]	
1	1	1	register [791]	MSB

Table 42. 3-bit LUT3 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [792]	LSB
0	0	1	register [793]	
0	1	0	register [794]	
0	1	1	register [795]	
1	0	0	register [796]	
1	0	1	register [797]	
1	1	0	register [798]	
1	1	1	register [799]	MSB

Table 43. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [800]	LSB
0	0	1	register [801]	
0	1	0	register [802]	
0	1	1	register [803]	
1	0	0	register [804]	
1	0	1	register [805]	
1	1	0	register [806]	
1	1	1	register [807]	MSB

Table 44. 3-bit LUT5 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [808]	LSB
0	0	1	register [809]	
0	1	0	register [810]	
0	1	1	register [811]	
1	0	0	register [812]	
1	0	1	register [813]	
1	1	0	register [814]	
1	1	1	register [815]	MSB

Table 45. 3-bit LUT6 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [816]	LSB
0	0	1	register [817]	
0	1	0	register [818]	
0	1	1	register [819]	
1	0	0	register [820]	
1	0	1	register [821]	
1	1	0	register [822]	
1	1	1	register [823]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT0 is defined by registers [1527:1520]

3-bit LUT1 is defined by registers [1535:1528]

3-bit LUT2 is defined by registers [791:784]

3-bit LUT3 is defined by registers [799:792]

3-bit LUT4 is defined by registers [807:800]

3-bit LUT5 is defined by registers [815:808]

3-bit LUT6 is defined by registers [823:816]

Table 46 shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the four 3-bit LUT logic cells.

Table 46. 3-bit LUT Standard Digital Functions

Function	MSB						LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0

Table 46. **3-bit LUT Standard Digital Functions (Cont.)**

Function	MSB						LSB
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

7.3.2 Initial Polarity Operations

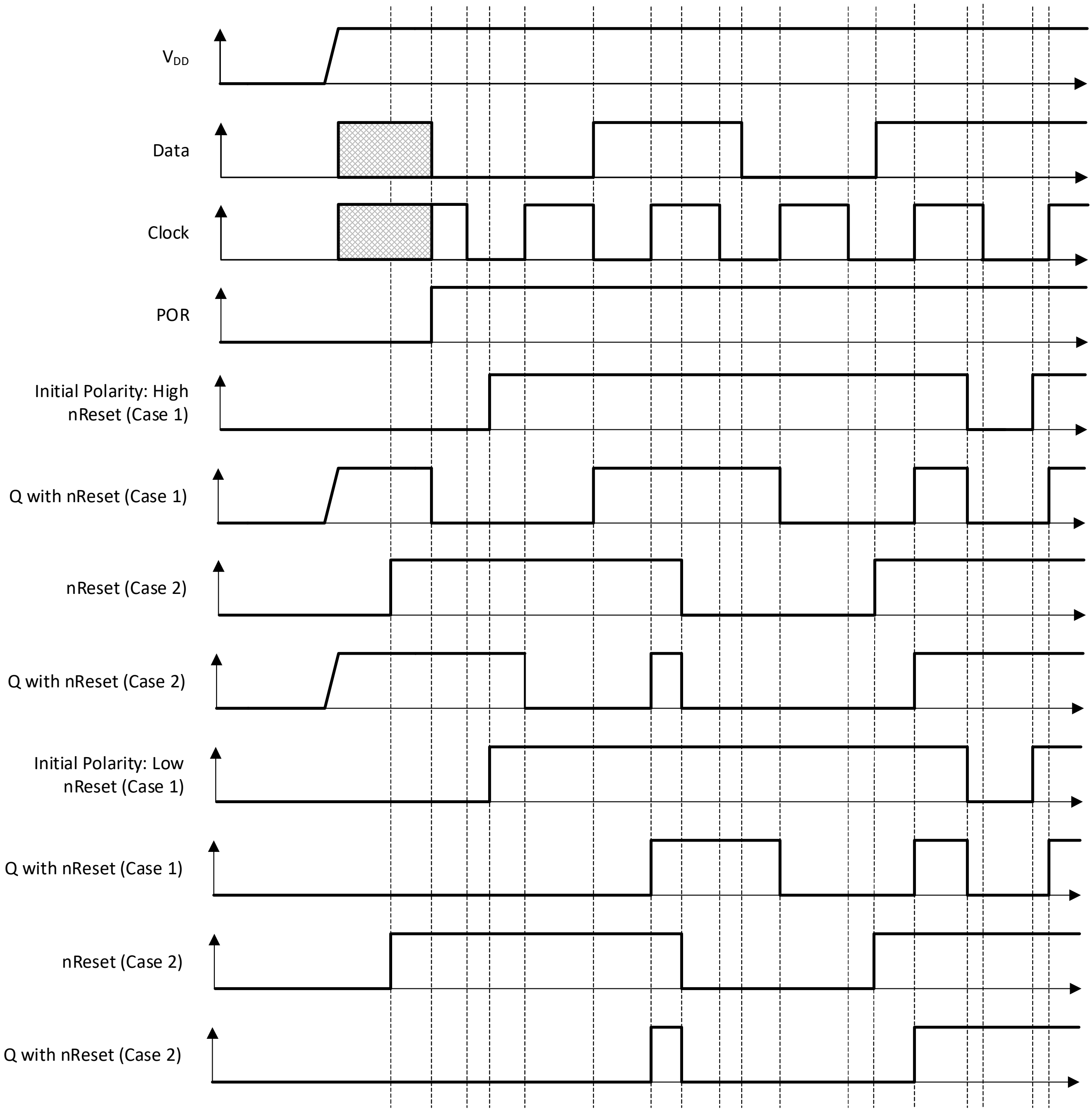


Figure 27. DFF Polarity Operations with nReset

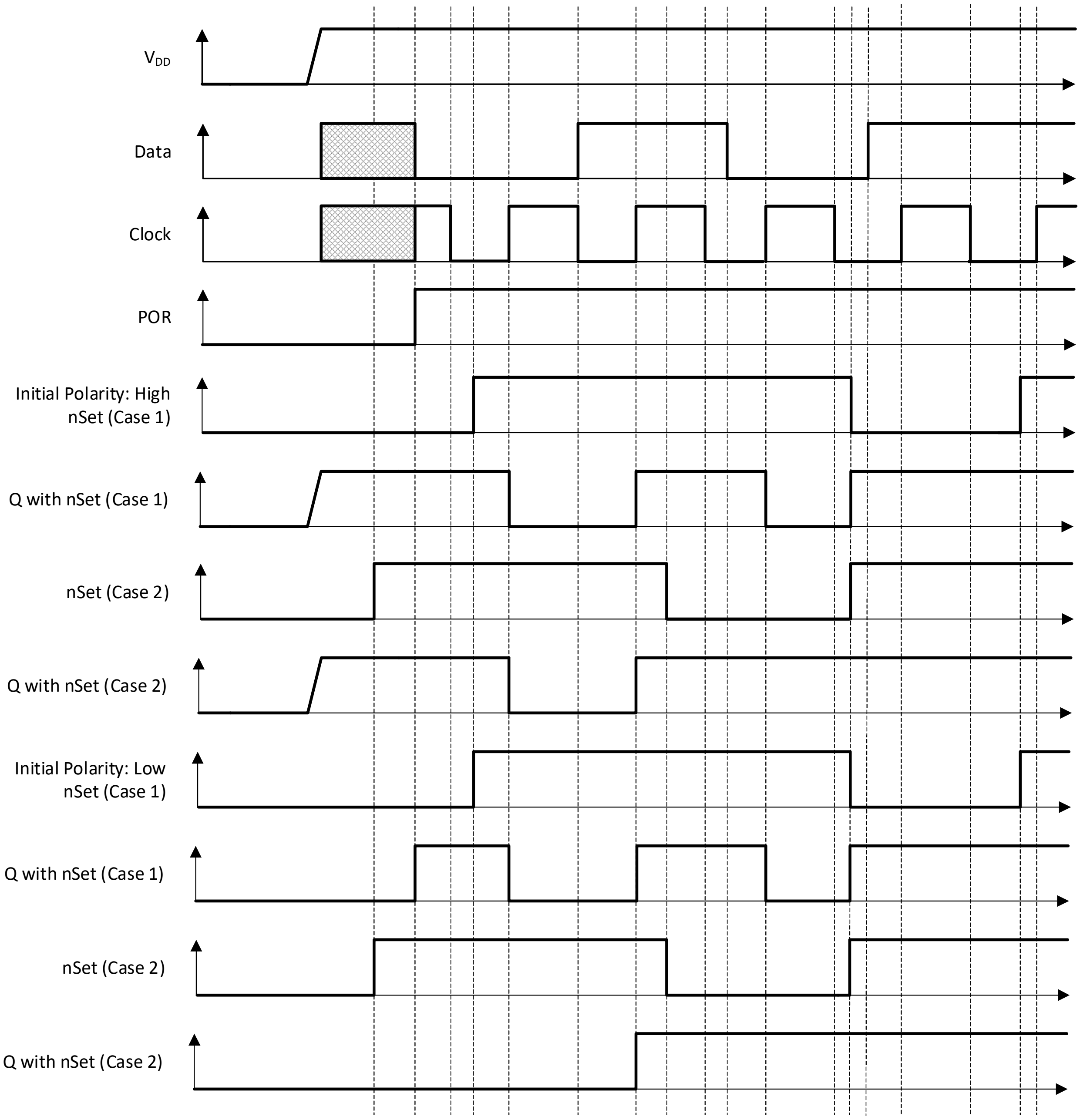


Figure 28. DFF Polarity Operations with nSet

7.4 4-Bit LUT or D Flip-Flop with Set/Reset Macrocell

There is one macrocell that can serve as either a 4-bit LUT or as a D Flip-Flop with Set/Reset inputs. When used to implement LUT functions, the 4-bit LUT takes in four input signals from the connection matrix and produces a single output, which goes back into the connection matrix. When used to implement D Flip-Flop function, the input signals from the connection matrix go to the data (D) and clock (CLK), and Reset/Set (nRST/nSET) inputs for the Flip-Flop, with the output going back to the connection matrix.

If register [842] = 0, and the CLK is rising edge triggered, then Q = D, otherwise Q will not change.

If register [842] = 1, then data from D is written into the DFF by the rising edge on CLK and output to Q by the falling edge on CLK. It is possible to define the active level for the reset/set input of DFF/LATCH macrocell. There are both active high level reset/set (RST/SET) and active low level reset/set (nRST/nSET) options available, which are selected by register [843].

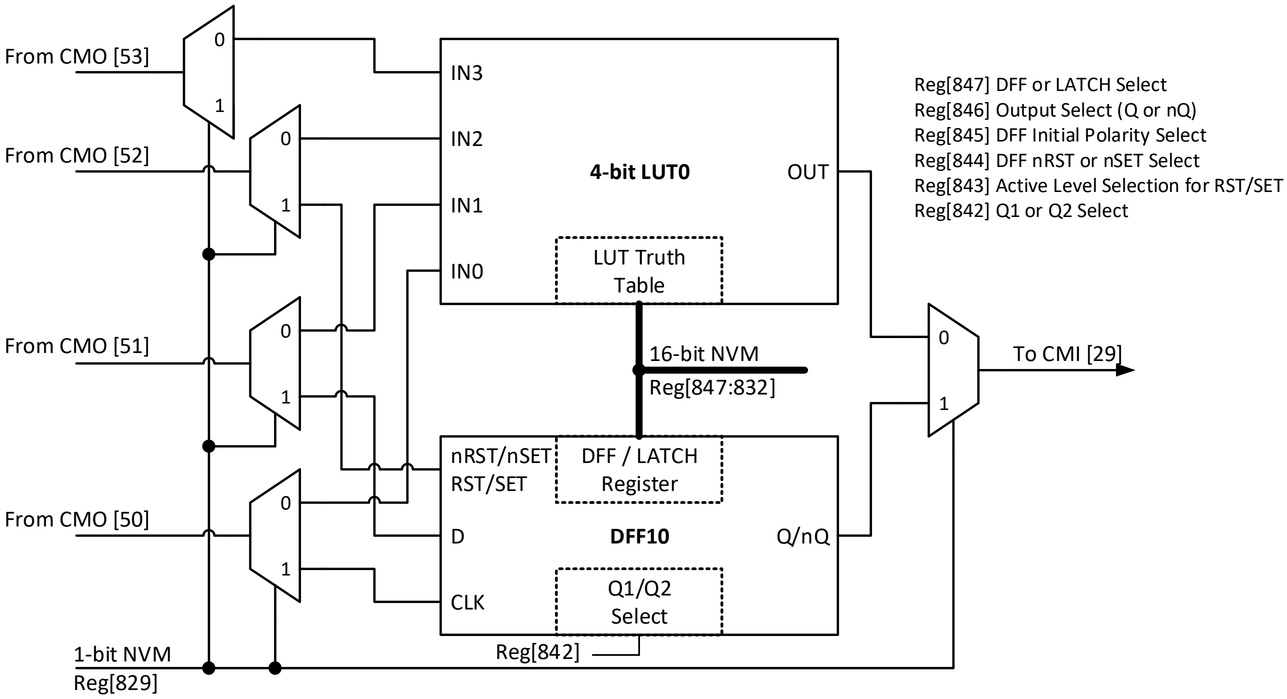


Figure 29. 4-bit LUT0 or DFF10

7.4.1 4-Bit LUT Macrocell Used as 4-Bit LUT

Table 47. 4-bit LUT0 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [832]	LSB
0	0	0	1	register [833]	
0	0	1	0	register [834]	
0	0	1	1	register [835]	
0	1	0	0	register [836]	
0	1	0	1	register [837]	
0	1	1	0	register [838]	
0	1	1	1	register [839]	
1	0	0	0	register [840]	
1	0	0	1	register [841]	
1	0	1	0	register [842]	
1	0	1	1	register [843]	
1	1	0	0	register [844]	
1	1	0	1	register [845]	
1	1	1	0	register [846]	
1	1	1	1	register [847]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT0 is defined by registers [847:832]

Table 48. 4-bit LUT Standard Digital Functions

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	0	0	1	0	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	1	1	0	1	0	0	1

7.5 3-Bit LUT or Pipe Delay/Ripple Counter Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay/Ripple Counter.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a Pipe Delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK), and Reset (nRST). The Pipe Delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell input (IN). Both of the two outputs (OUT0 and OUT1) provide user selectable options for 1 to 16 stages of delay. There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled

by registers [851:848] for OUT0 and registers [855:852] for OUT1.
The 4-input MUX is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG47004-A design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the internal Oscillator within the SLG47004-A). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell. OUT1 Output can be inverted (as selected by register [859]).

In the Ripple Counter mode, there are 3 options for setting, which use 7 bits. There are 3 bits to set nSET value (SV) in range from 0 to 7. It is a value, which will be set into the Ripple Counter outputs when nSET input goes LOW. End value (EV) will use 3 bits for setting outputs code, which will be last code in the cycle. After reaching the EV, the Ripple Counter goes to the first code by the rising edge on CLK input. The Functionality mode option uses 1 bit. This setting defines how exactly Ripple Counter will operate.

The user can select one of the functionality modes by register: RANGE or FULL. If the RANGE option is selected, the count starts from SV. If UP input is LOW the count goes down: SV→EV→EV-1 to SV+1→SV, and others (if SV is smaller than EV), or SV→SV-1 to EV+1→EV→SV (if SV is bigger than EV). If UP input is HIGH, count starts from SV up to EV, and others.

In the FULL range configuration the Ripple Counter functions as follows. If UP input is LOW, the count starts from SV and goes down to 0. Then current counter value jumps to EV and goes down to 0, and others.

If UP input is HIGH, count goes up starting from SV. Then current counter value jumps to 0 and counts up to EV, and others. See Ripple Counter functionality example in Figure 31.

Every step is executed by the rising edge on CLK input.

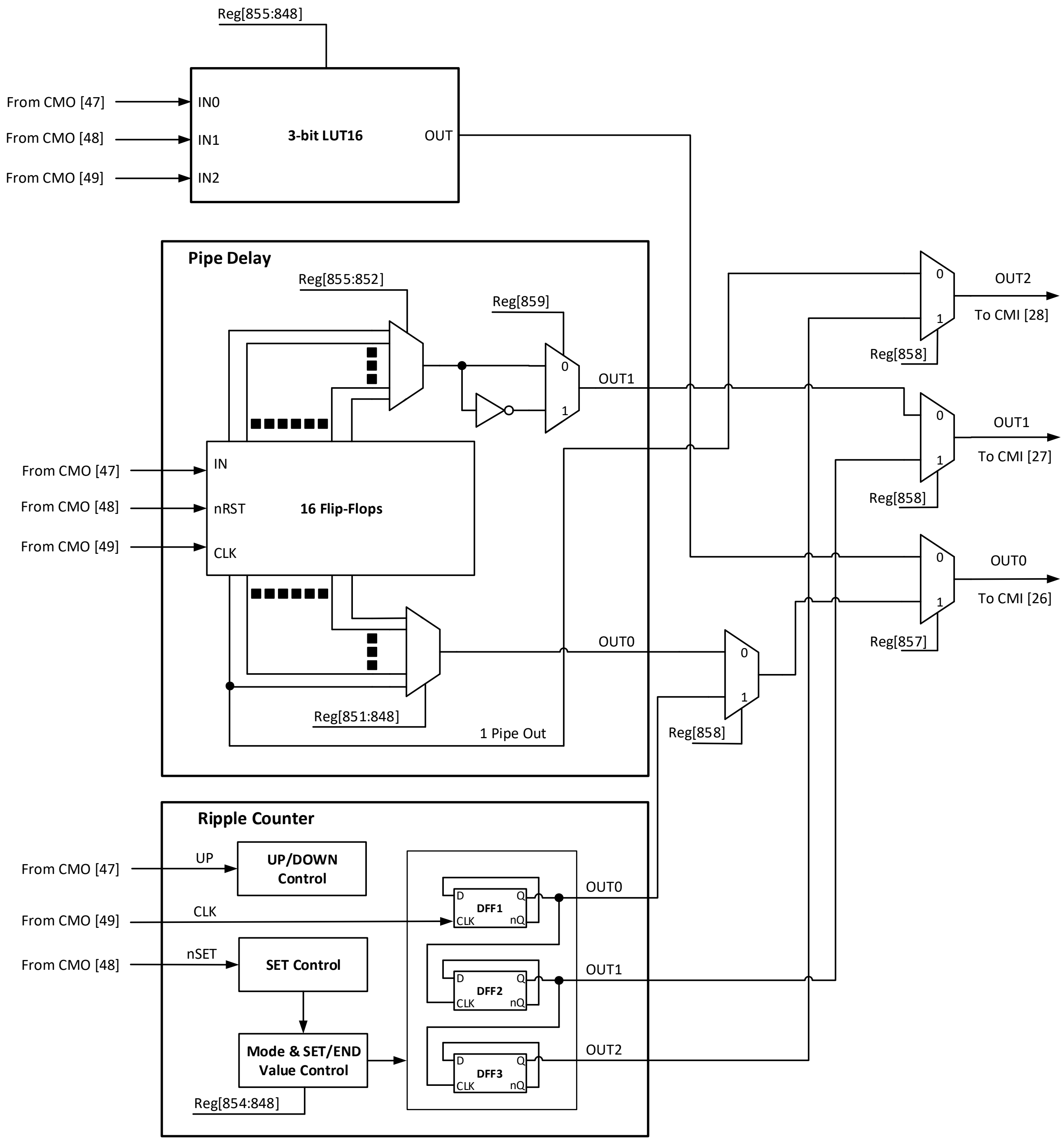


Figure 30. 3-bit LUT13/Pipe Delay/Ripple Counter

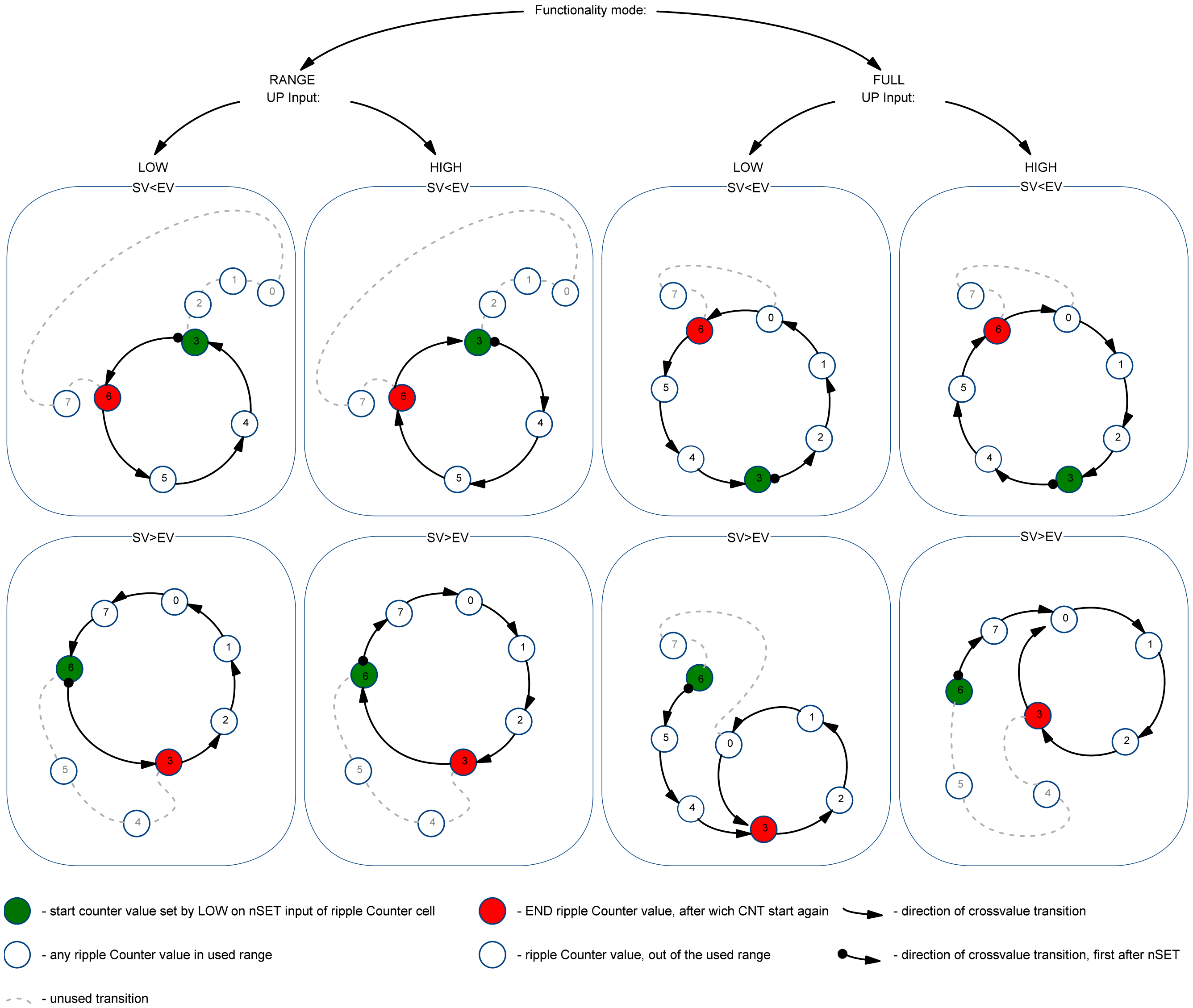


Figure 31. Example of Ripple Counter Functionality

7.5.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUT

Table 49. 3-bit LUT13 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [848]	LSB
0	0	1	register [849]	
0	1	0	register [850]	
0	1	1	register [851]	
1	0	0	register [852]	
1	0	1	register [853]	
1	1	0	register [854]	
1	1	1	register [855]	MSB

Each macrocell, when programmed for a LUT function, uses an 8-bit register to define their output function:

3-bit LUT13 is defined by registers [855:848]

8. Multi-Function Macrocells

The SLG47004-A has seven Multi-Function macrocells that can serve as more than one logic or timing function. In each case, they can serve as a LUT, DFF with flexible settings, or as CNT/DLY with multiple modes such as One Shot, Frequency Detect, Edge Detect, and others. Also, the macrocell is capable to combine those functions: LUT/DFF connected to CNT/DLY or CNT/DLY connected to LUT/DFF, see Figure 32.

See the list below for the functions that can be implemented in these macrocells:

- Six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays
- One macrocell that can serve as a 4-bit LUT/D Flip-Flop and as 16-Bit Counter/Delay/FSM

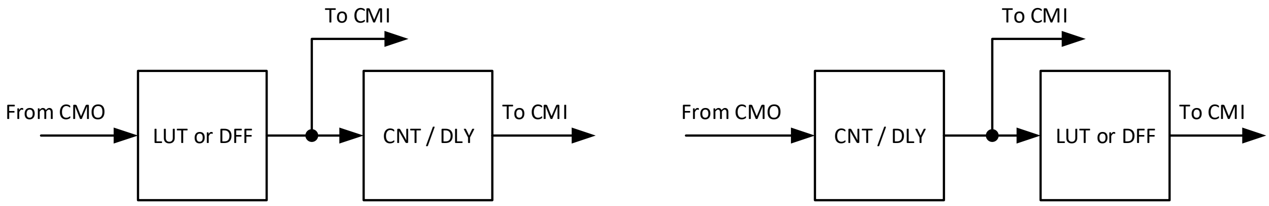


Figure 32. Possible Connections inside Multi-Function Macrocell

Inputs/Outputs for the seven Multi-Function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

8.1 3-Bit LUT or DFF/LATCH with 8-Bit Counter/Delay Macrocells

There are six macrocells that can serve as 3-bit LUTs/D Flip-Flops and as 8-Bit Counter/Delays.

When used to implement LUT functions, the 3-bit LUTs each takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix or can be connected to CNT/DLY's input.

When used to implement D Flip-Flop function, the three input signals from the connection matrix go to the data (D), clock (CLK), and Reset/Set (nRST/nSET) inputs of the Flip-Flop, with the output going back to the connection matrix or to the CNT/DLY's input.

When used to implement Counter/Delays, each macrocell has a dedicated matrix input connection. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count/delay circuits. These macrocells can also operate in a One-Shot mode, which will generate an output pulse of user-defined width. They can also operate in a Frequency Detection or Edge Detection mode.

Counter/Delay macrocell has an initial value, which defines its initial value after SLG47004-A is powered up. It is possible to select initial Low or initial High, as well as initial value defined by a Delay In signal.

For example, in case initial LOW option is used, the rising edge delay will start operation.

For timing diagrams refer to Section 8.3 CNT/DLY/FSM Timing Diagrams.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 and after two DFF is bypass – counters initialize with counter data after POR.

CNT5 and CNT6 current count value can be read via I^2C. However, it is possible to change the counter data (value counter starts operating from) for any macrocell using I^2C write commands. In this mode, it is possible to load count data immediately (after two DFF) or after counter ends counting. See Section 18.7.1 Reading Counter Data via I2C for further details.

8.1.1 3-Bit LUT or 8-Bit CNT/DLY Block Diagrams

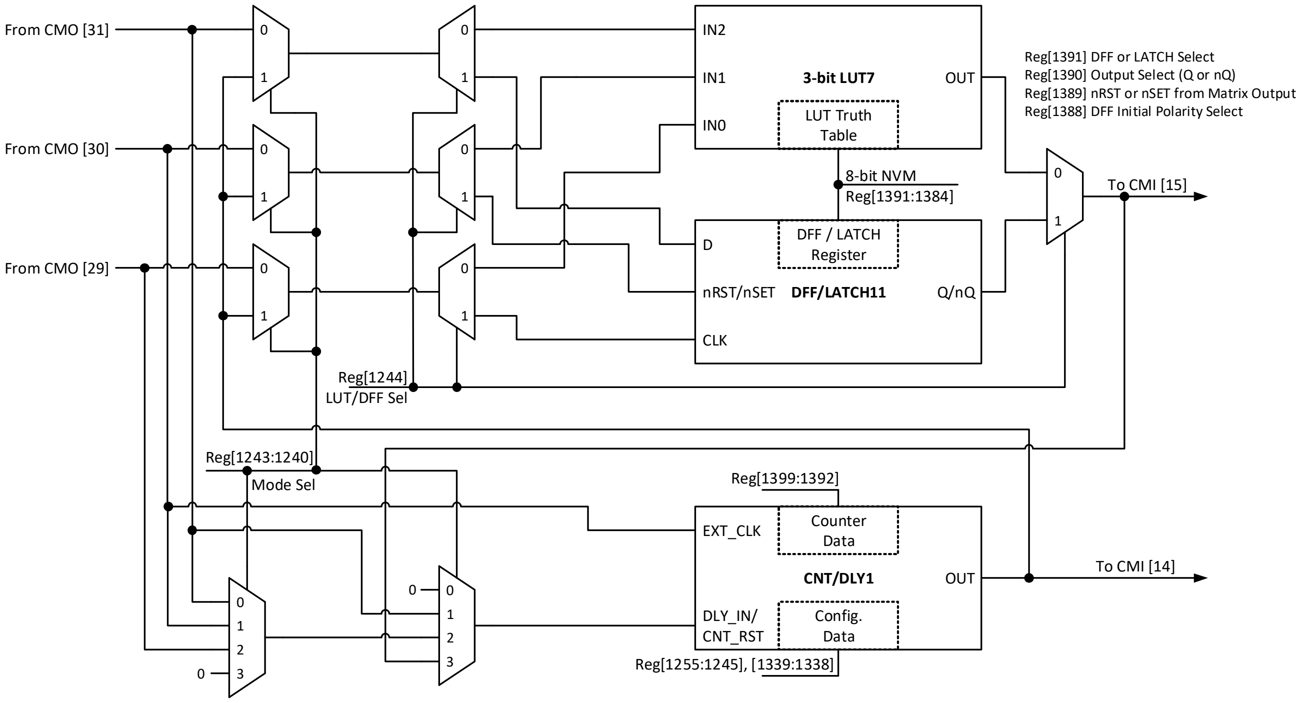


Figure 33. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT7/DFF11, CNT/DLY1)

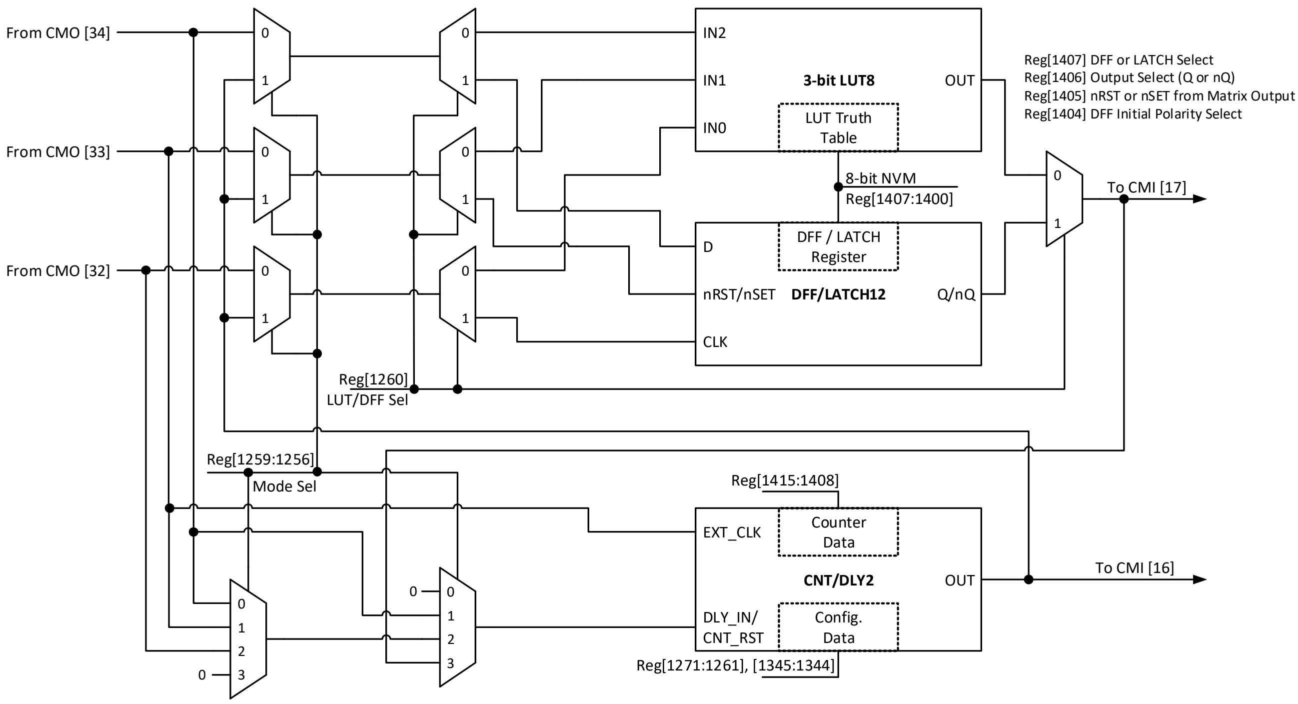


Figure 34. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT8/DFF12, CNT/DLY2)

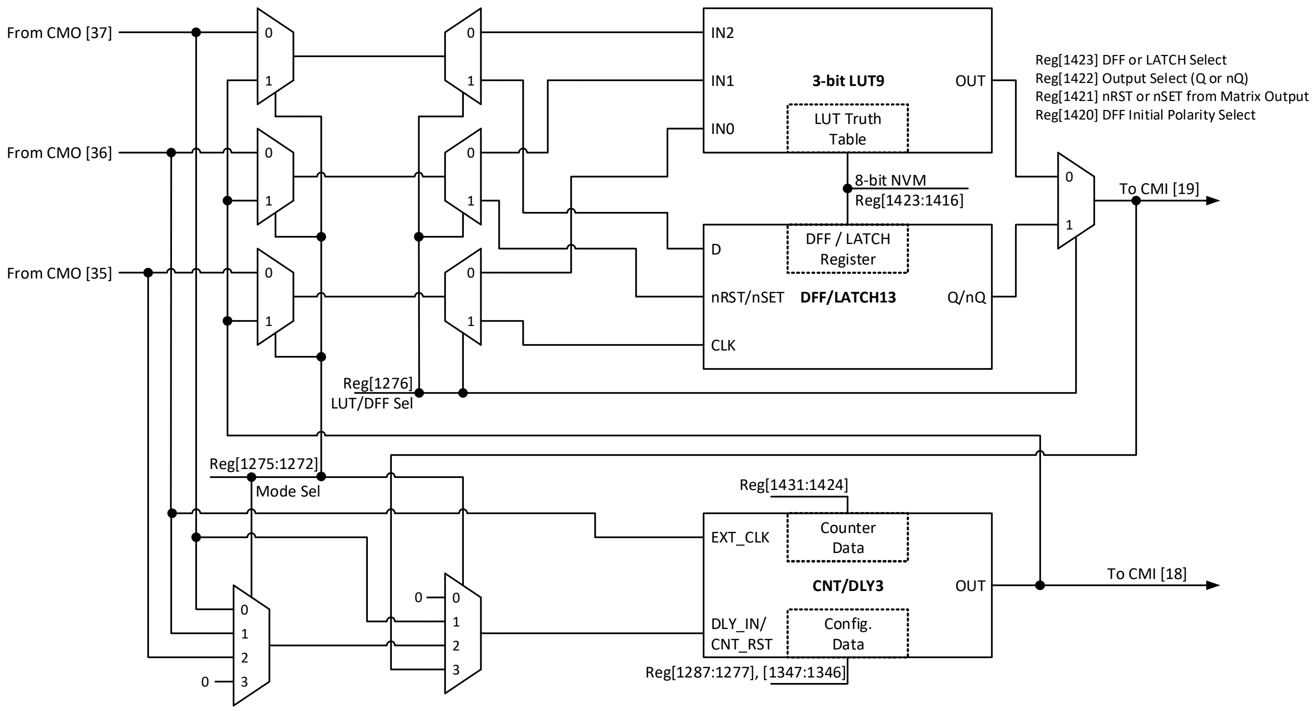


Figure 35. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT9/DFF13, CNT/DLY3)

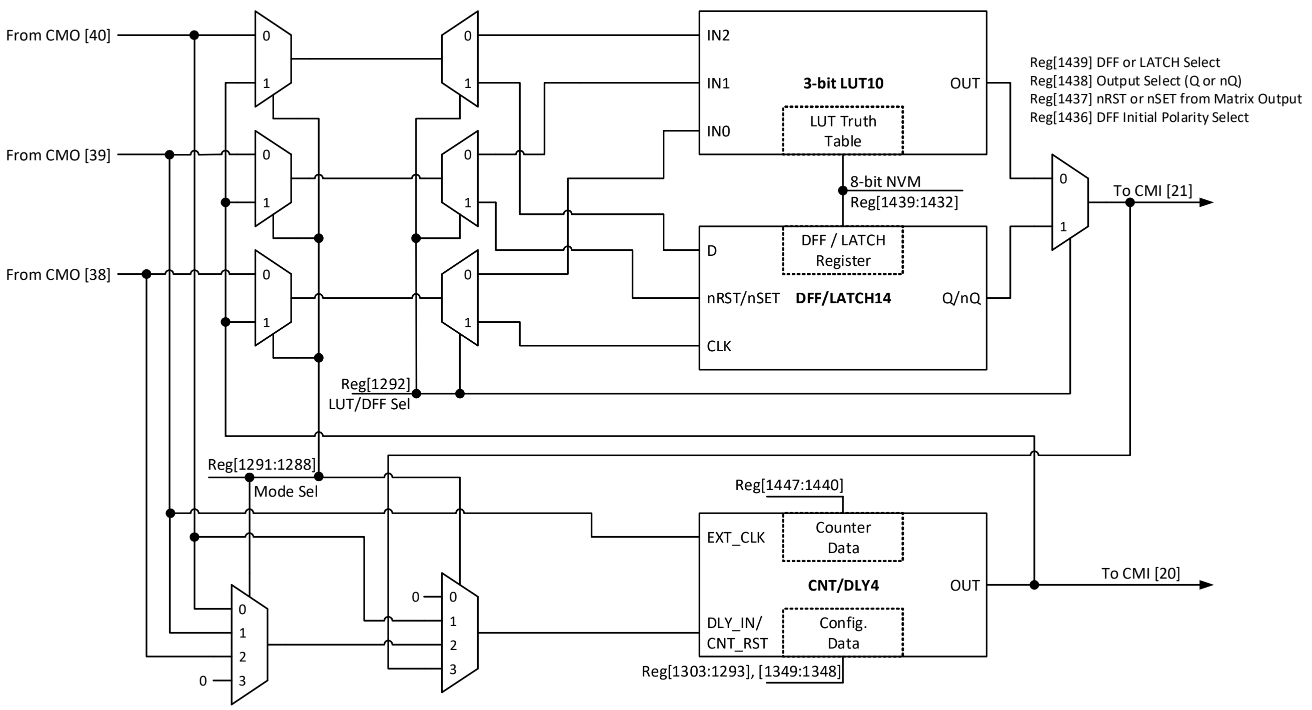


Figure 36. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT10/DFF14, CNT/DLY4)

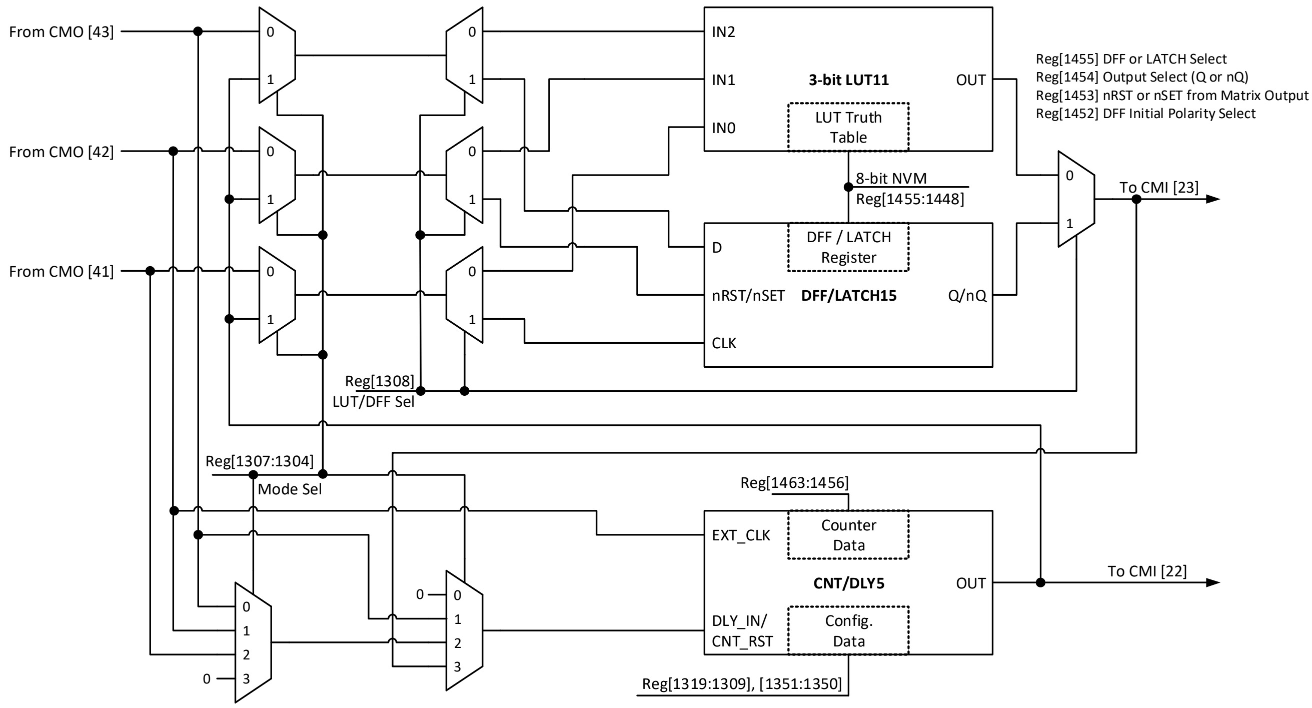


Figure 37. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT11/DFF15, CNT/DLY5)

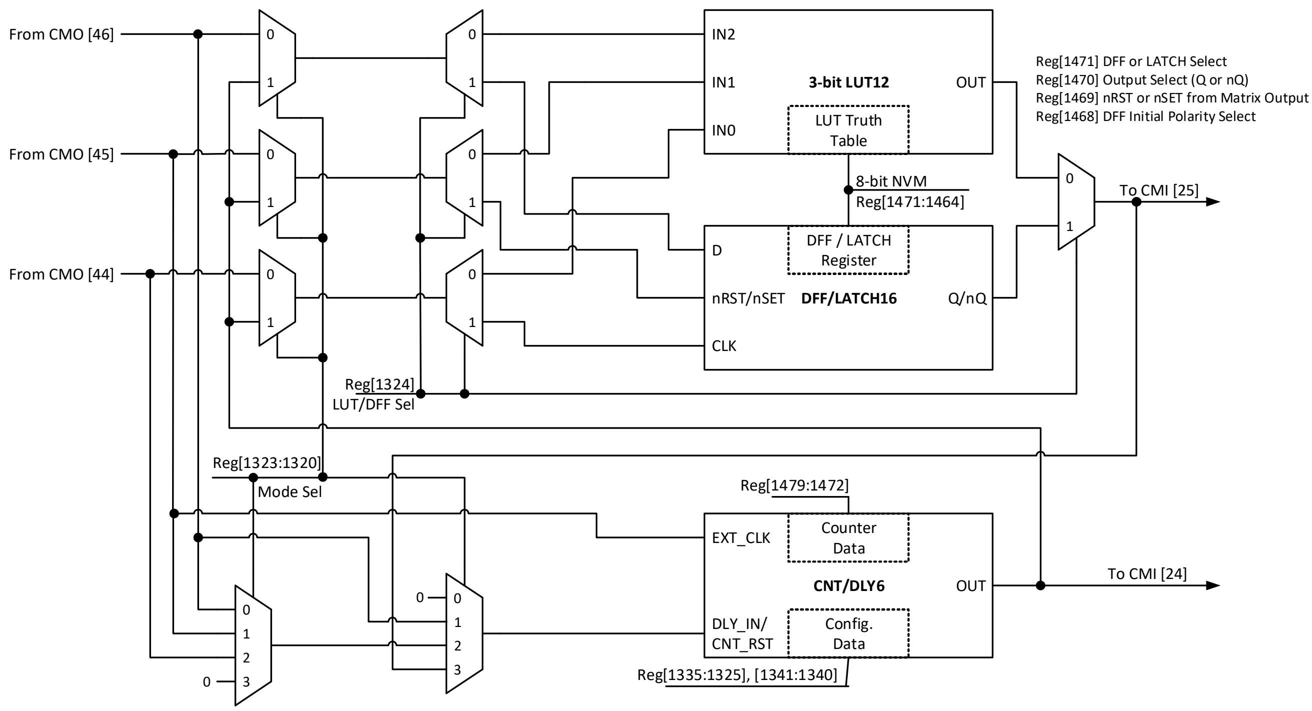


Figure 38. 8-bit Multi-Function Macrocells Block Diagram (3-bit LUT12/DFF16, CNT/DLY6)

As shown in Figure 33 to Figure 38 there is a possibility to use LUT/DFF and CNT/DLY simultaneously.

Note: It is not possible to use LUT and DFF at once, one of these macrocells must be selected.

- Case 1. LUT/DFF in front of CNT/DLY. Three input signals from the connection matrix go to previously selected LUT or DFF's inputs and produce a single output which goes to a CND/DLY input. In its turn Counter/Delay's output goes back to the matrix.
- Case 2. CNT/DLY in front of LUT/DFF. Two input signals from the connection matrix go to CND/DLY's inputs (IN and CLK). Its output signal can be connected to any input of previously selected LUT or DFF, after which the signal goes back to the matrix.
- Case 3. Single LUT/DFF or CNT/DLY. Also, it is possible to use a standalone LUT/DFF or CNT/DLY. In this case, all inputs and output of the macrocell are connected to the matrix.

8.1.2 3-Bit LUT or CNT/DLYs Used as 3-Bit LUTs

Table 50. 3-bit LUT7 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1384]	LSB
0	0	1	register [1385]	
0	1	0	register [1386]	
0	1	1	register [1387]	
1	0	0	register [1388]	
1	0	1	register [1389]	
1	1	0	register [1390]	
1	1	1	register [1391]	MSB

Table 51. 3-bit LUT8 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1400]	LSB
0	0	1	register [1401]	
0	1	0	register [1402]	
0	1	1	register [1403]	
1	0	0	register [1404]	
1	0	1	register [1405]	
1	1	0	register [1406]	
1	1	1	register [1407]	MSB

Table 52. 3-bit LUT9 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1416]	LSB
0	0	1	register [1417]	
0	1	0	register [1418]	
0	1	1	register [1419]	
1	0	0	register [1420]	
1	0	1	register [1421]	
1	1	0	register [1422]	
1	1	1	register [1423]	MSB

Table 53. 3-bit LUT10 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1432]	LSB
0	0	1	register [1433]	
0	1	0	register [1434]	
0	1	1	register [1435]	
1	0	0	register [1436]	
1	0	1	register [1437]	
1	1	0	register [1438]	
1	1	1	register [1439]	MSB

Table 54. 3-bit LUT11 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1448]	LSB
0	0	1	register [1449]	
0	1	0	register [1450]	
0	1	1	register [1451]	
1	0	0	register [1452]	
1	0	1	register [1453]	
1	1	0	register [1454]	
1	1	1	register [1455]	MSB

Table 55. 3-bit LUT12 Truth Table

IN2	IN1	IN0	OUT	
0	0	0	register [1464]	LSB
0	0	1	register [1465]	
0	1	0	register [1466]	
0	1	1	register [1467]	
1	0	0	register [1468]	
1	0	1	register [1469]	
1	1	0	register [1470]	
1	1	1	register [1471]	MSB

Each macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-bit LUT7 is defined by registers [1391:1384]

3-bit LUT8 is defined by registers [1407:1400]

3-bit LUT9 is defined by registers [1423:1416]

3-bit LUT10 is defined by registers [1439:1432]

3-bit LUT11 is defined by registers [1455:1448]

3-bit LUT12 is defined by registers [1471:1464]

8.2 4-Bit LUT or DFF/LATCH with 16-Bit Counter/Delay Macrocell

There is one macrocell that can serve as either 4-bit LUT/D Flip-Flops or as 16-bit Counter/Delay.

When used to implement LUT function, the 4-bit LUT takes in four input signals from the Connection Matrix and produces a single output, which goes back into the Connection Matrix.

When used to implement D Flip-Flop function, the two input signals from the connection matrix go to the data (D) and clock (CLK) inputs for the Flip-Flop, with the output going back to the connection matrix.

When used to implement 16-Bit Counter/Delay function, two of the four input signals from the connection matrix go to the external clock (EXT_CLK) and reset (DLY_IN/CNT Reset) for the Counter/Delay, with the output going back to the connection matrix.

This macrocell has an optional Finite State Machine (FSM) function. There are two additional matrix inputs for Up and Keep to support FSM functionality.

This macrocell can also operate in a one-shot mode, which will generate an output pulse of user-defined width.
This macrocell can also operate in a frequency detection or edge detection mode.
This macrocell can have its active count value read via I^2C. See Section 18.7.1 Reading Counter Data via I2C.

Note: After two DFF – counters initialize with counter data = 0 after POR.

Initial state = 1 – counters initialize with counter data = 0 after POR.

Initial state = 0 and after two DFF is bypass – counters initialize with counter data after POR.

8.2.1 4-Bit LUT or DFF/LATCH with 16-Bit CNT/DLY Block Diagram

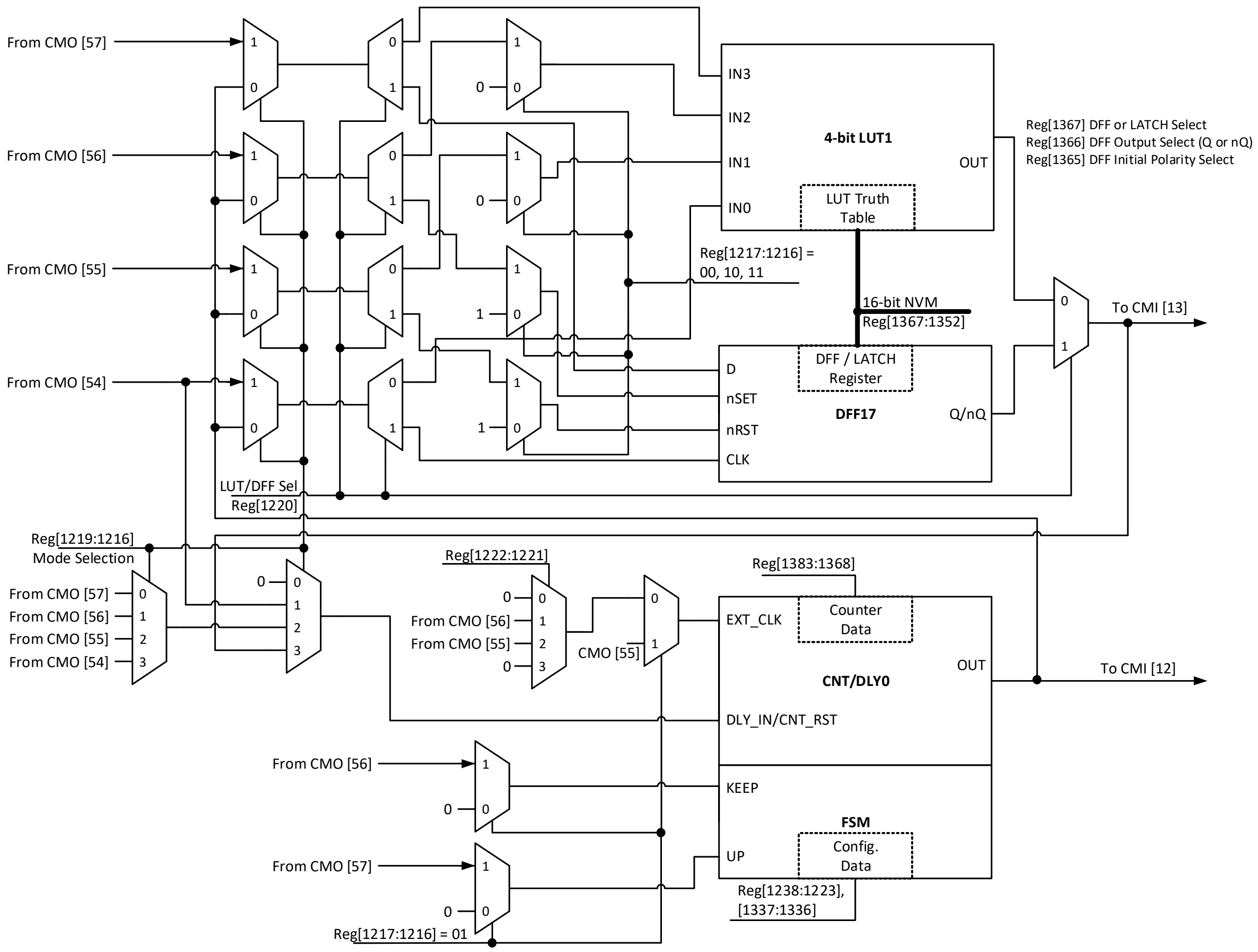


Figure 39. 4-bit LUT1 or CNT/DLY0

8.2.2 4-Bit LUT or 16-Bit Counter/Delay Macrocells Used as 4-Bit LUTs

Table 56. 4-bit LUT1 Truth Table

IN3	IN2	IN1	IN0	OUT	
0	0	0	0	register [1352]	LSB
0	0	0	1	register [1353]	
0	0	1	0	register [1354]	
0	0	1	1	register [1355]	
0	1	0	0	register [1356]	
0	1	0	1	register [1357]	
0	1	1	0	register [1358]	
0	1	1	1	register [1359]	
1	0	0	0	register [1360]	
1	0	0	1	register [1361]	
1	0	1	0	register [1362]	
1	0	1	1	register [1363]	
1	1	0	0	register [1364]	
1	1	0	1	register [1365]	
1	1	1	0	register [1366]	
1	1	1	1	register [1367]	MSB

This macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-bit LUT1 is defined by registers [1367:1352]

Table 57. 4-bit LUT Standard Digital Functions

Function	MSB														LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

8.3 CNT/DLY/FSM Timing Diagrams

8.3.1 Delay Mode CNT/DLY0 to CNT/DLY6

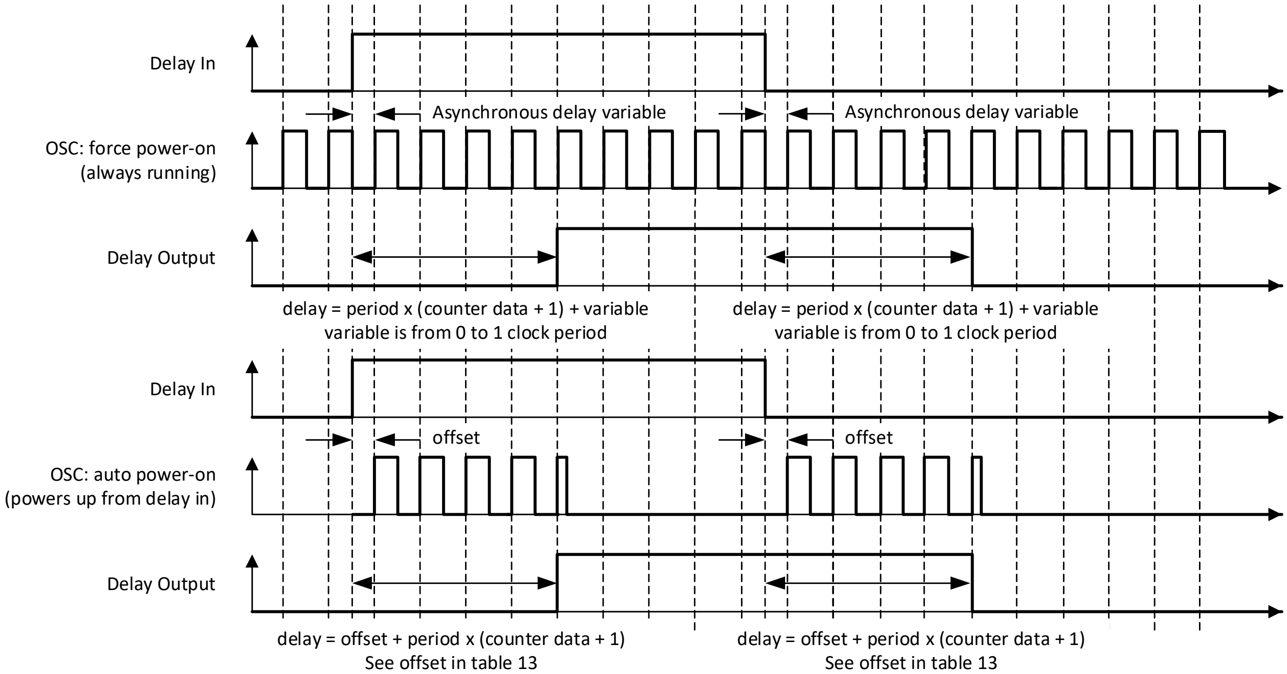


Figure 40. Delay Mode Timing Diagram, Edge Select: Both, Counter Data: 3

The macrocell shifts the respective edge to a set time and restarts by appropriate edge. It works as a filter if the input signal is shorter than the delay time.

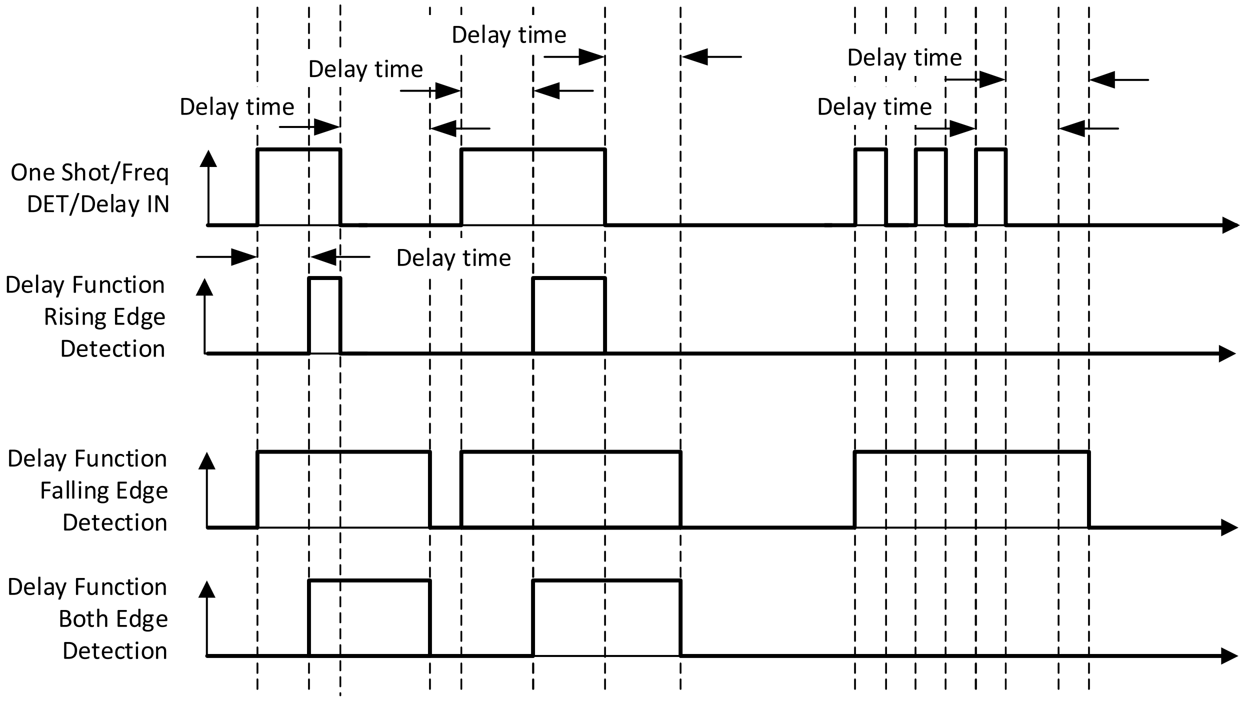


Figure 41. Delay Mode Timing Diagram for Different Edge Select Modes

8.3.2 Count Mode (Count Data: 3), Counter Reset (Rising Edge Detect) CNT/DLY0 to CNT/DLY6

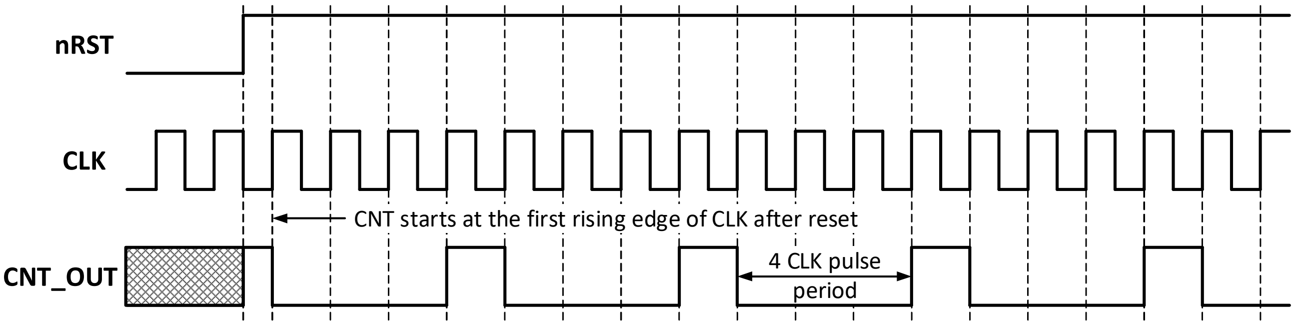


Figure 42. Counter Mode Timing Diagram without Two DFFs Synced Up

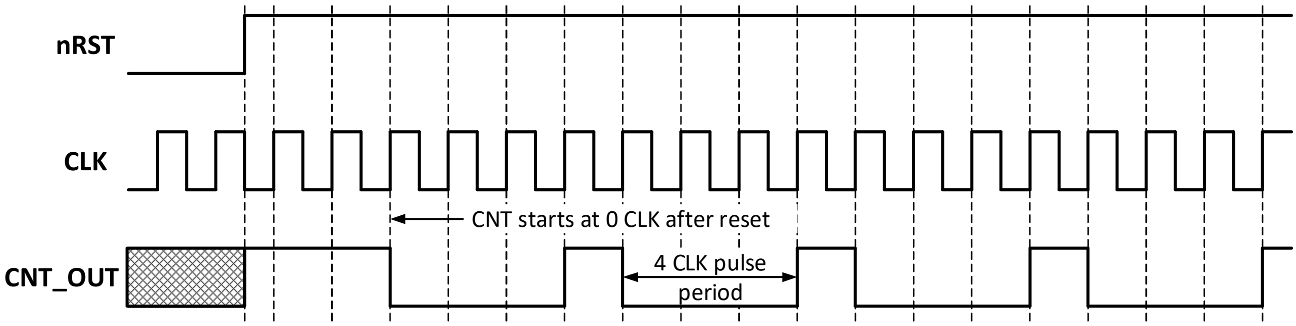


Figure 43. Counter Mode Timing Diagram with Two DFFs Synced Up

8.3.3 One-Shot Mode CNT/DLY0 to CNT/DLY6

This macrocell will generate a pulse whenever a selected edge is detected on its input. Register bits set the edge selection. The pulse width is determined by counter data and clock selection properties.

The output pulse polarity (non-inverted or inverted) is selected by register bit. Any incoming edges will be ignored during the pulse width generation. The following diagram shows one-shot function for non-inverted output.

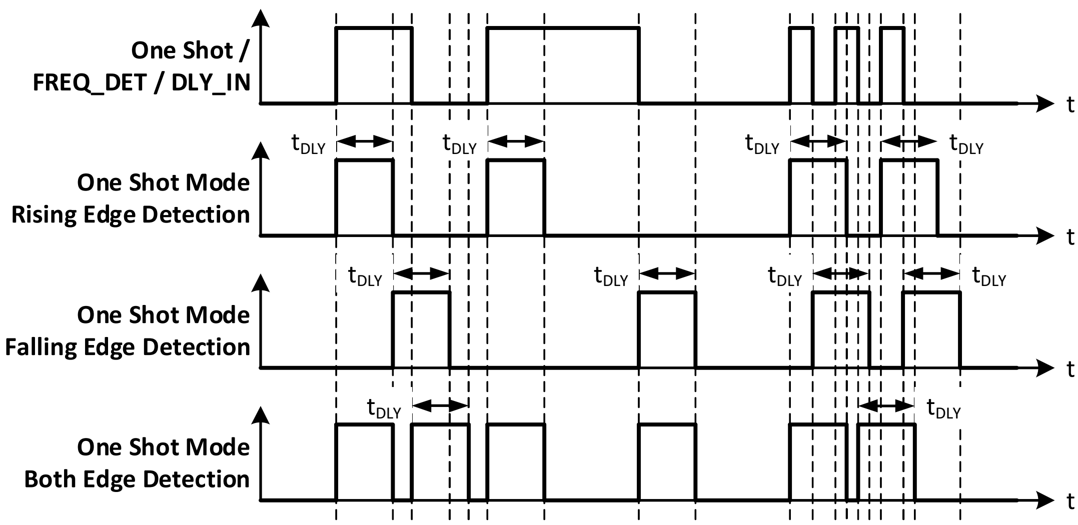


Figure 44. One-Shot Function Timing Diagram

This macrocell generates a high-level pulse with a set width (defined by counter data) when detecting the respective edge. It does not restart while pulse is HIGH.

8.3.4 Frequency Detection Mode CNT/DLY0 to CNT/DLY6

Rising Edge: The output goes high if the time between two successive edges is less than the delay. The output goes low if the second rising edge has not come after the last rising edge in specified time.

Falling Edge: The output goes high if the time between two falling edges is less than the set time. The output goes low if the second falling edge has not come after the last falling edge in specified time.

Both Edge: The output goes high if the time between the rising and falling edges is less than the set time, which is equivalent to the length of the pulse. The output goes low if after the last rising/falling edge and specified time, the second edge has not come.

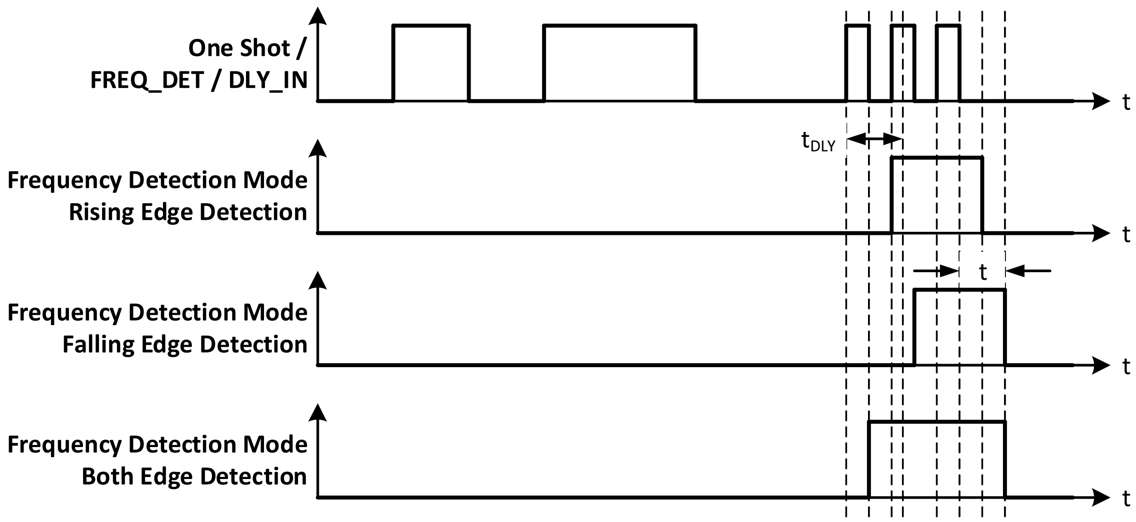


Figure 45. Frequency Detection Mode Timing Diagram

8.3.5 Edge Detection Mode CNT/DLY1 to CNT/DLY6

The macrocell generates high-level short pulse when detecting the respective edge. See Table 13.

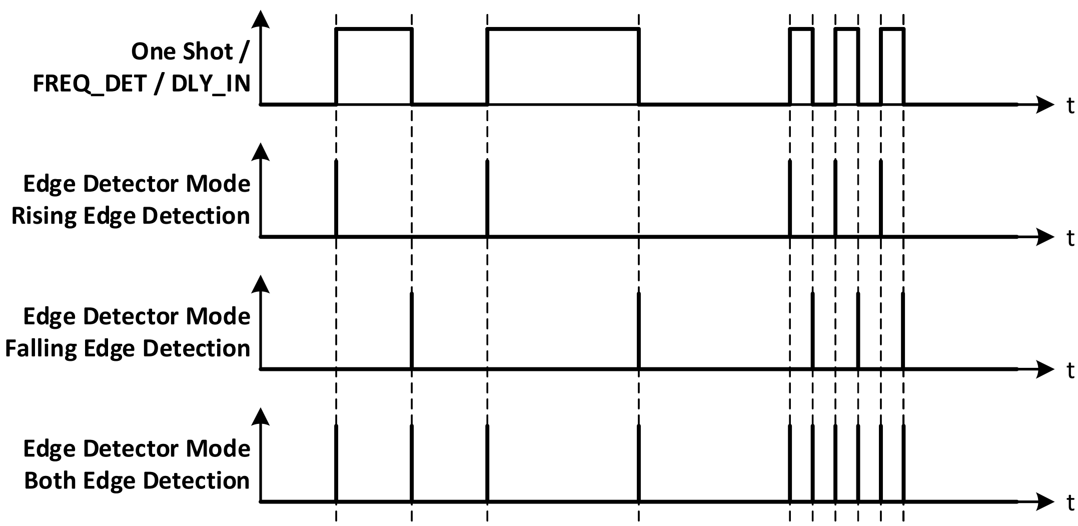


Figure 46. Edge Detection Mode Timing Diagram

8.3.6 Delayed Edge Detection Mode CNT/DLY0 to CNT/DLY6

In Delayed Edge Detection Mode, High-level short pulses are generated on the macrocell output after the configured delay time, if the corresponding edge was detected on the input.

If the input signal is changed during the set delay time, the pulse will not be generated.

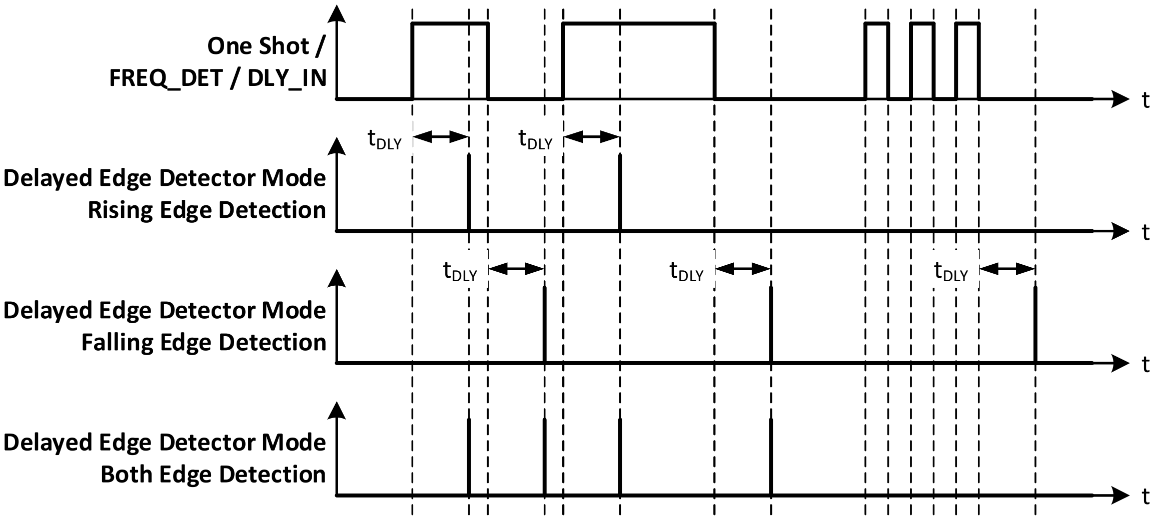
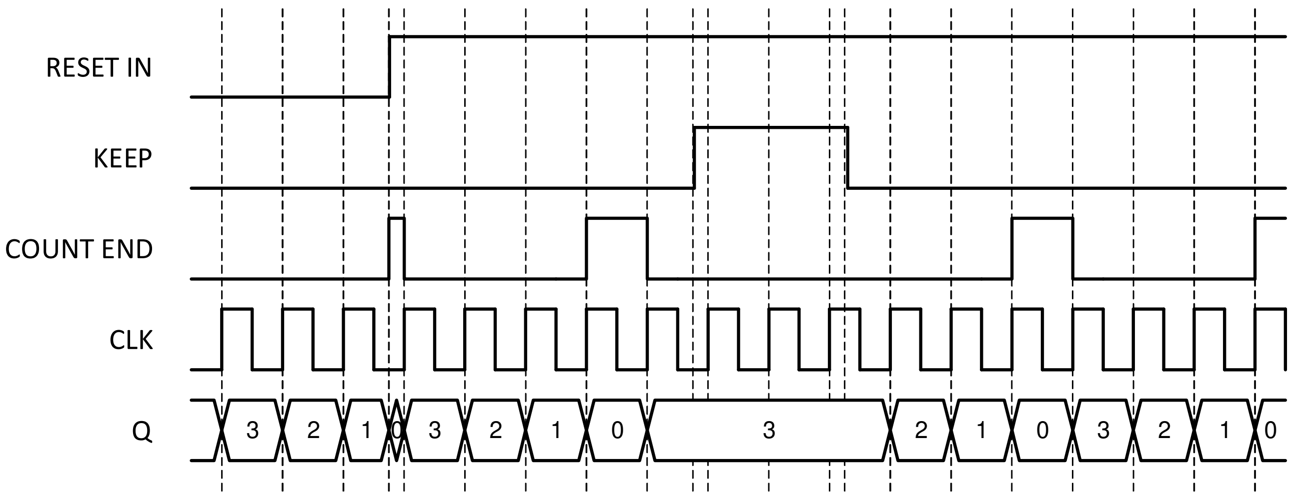


Figure 47. Delayed Edge Detection Mode Timing Diagram

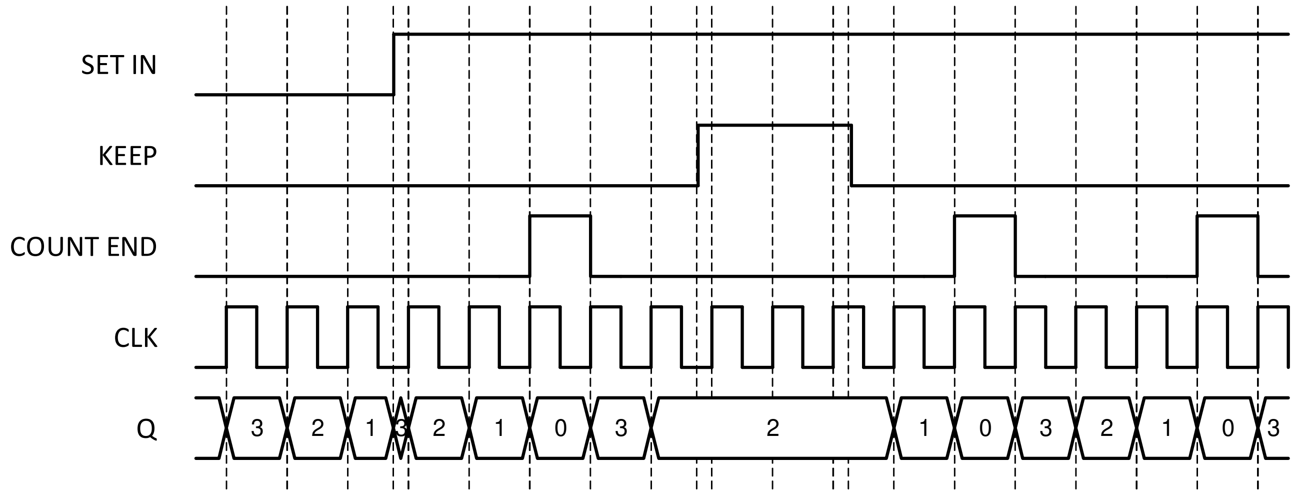
8.3.7 CNT/FSM Mode CNT/DLY0



Note 1: CNT Data = 3.

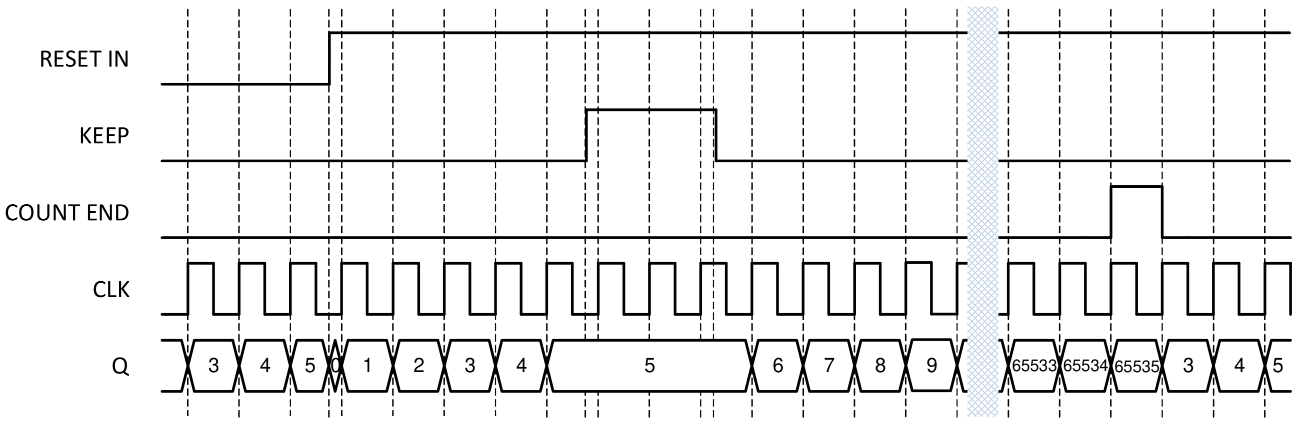
Note 2: Q = current counter value.

Figure 48. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 0)



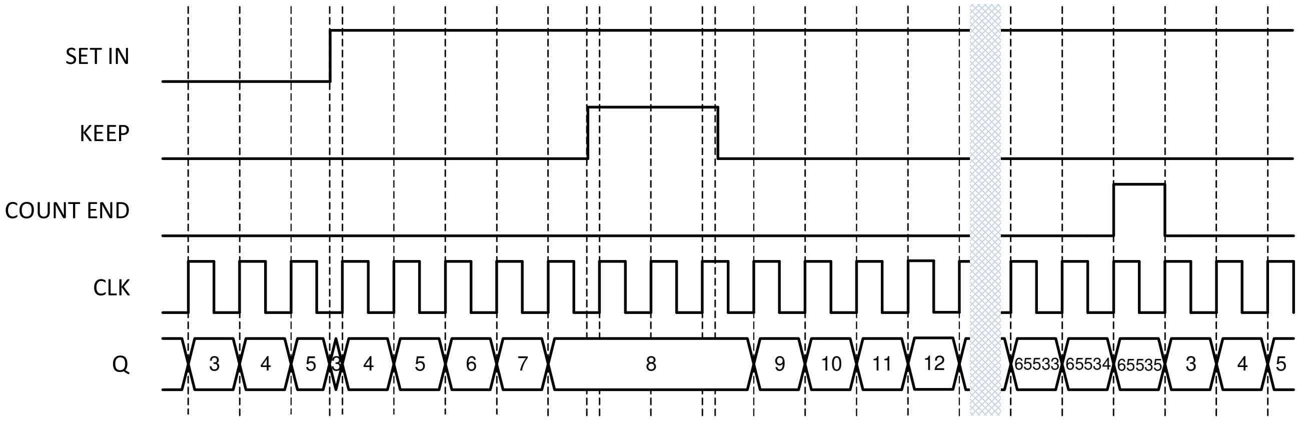
Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 49. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 0)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 50. CNT/FSM Timing Diagram (Reset Rising Edge Mode, Oscillator is Forced On, UP = 1)



Note 1: CNT Data = 3.
Note 2: Q = current counter value.

Figure 51. CNT/FSM Timing Diagram (Set Rising Edge Mode, Oscillator is Forced On, UP = 1)

8.3.8 The Difference in Counter Value for Counter, Delay, One-Shot, and Frequency Detect Modes

There is a difference in counter value for Counter and Delay/One-Shot/Frequency Detect modes. Compared to Counter mode, in Delay/One-Shot/Frequency Detect modes the counter value is shifted for two rising edges of the clock signal. See Figure 52.

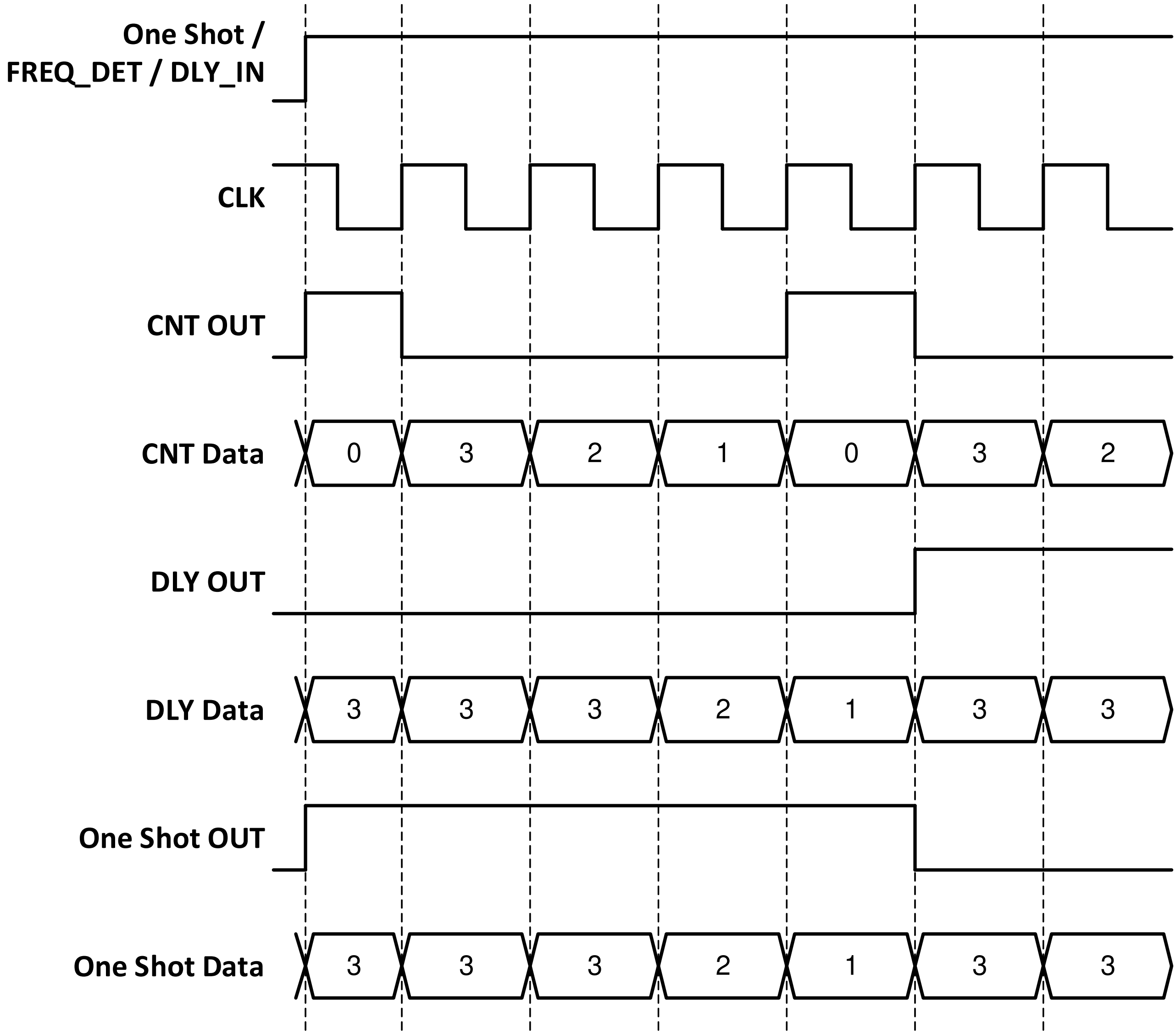


Figure 52. Counter Value, Counter Data = 3

8.4 Wake and Sleep Controller

The SLG47004-A has a Wake and Sleep (WS) function for ACMP. The macrocell CNT/DLY0 can be reconfigured for this purpose registers [1224:1223] = 11 and register [1232] = 1. The WS serves for power saving, it allows to switch on and off selected ACMPs on selected bit of 16-bit counter.

Note 1: BG/Analog_Good time is long and should be considered in the wake and sleep timing in case it dynamically powers on/off.
Note 2: Wake time should be long enough to make sure ACMP and Vref have enough time to get a sample before going to sleep.
Note 3: ACMPs power up must be connected to POR.

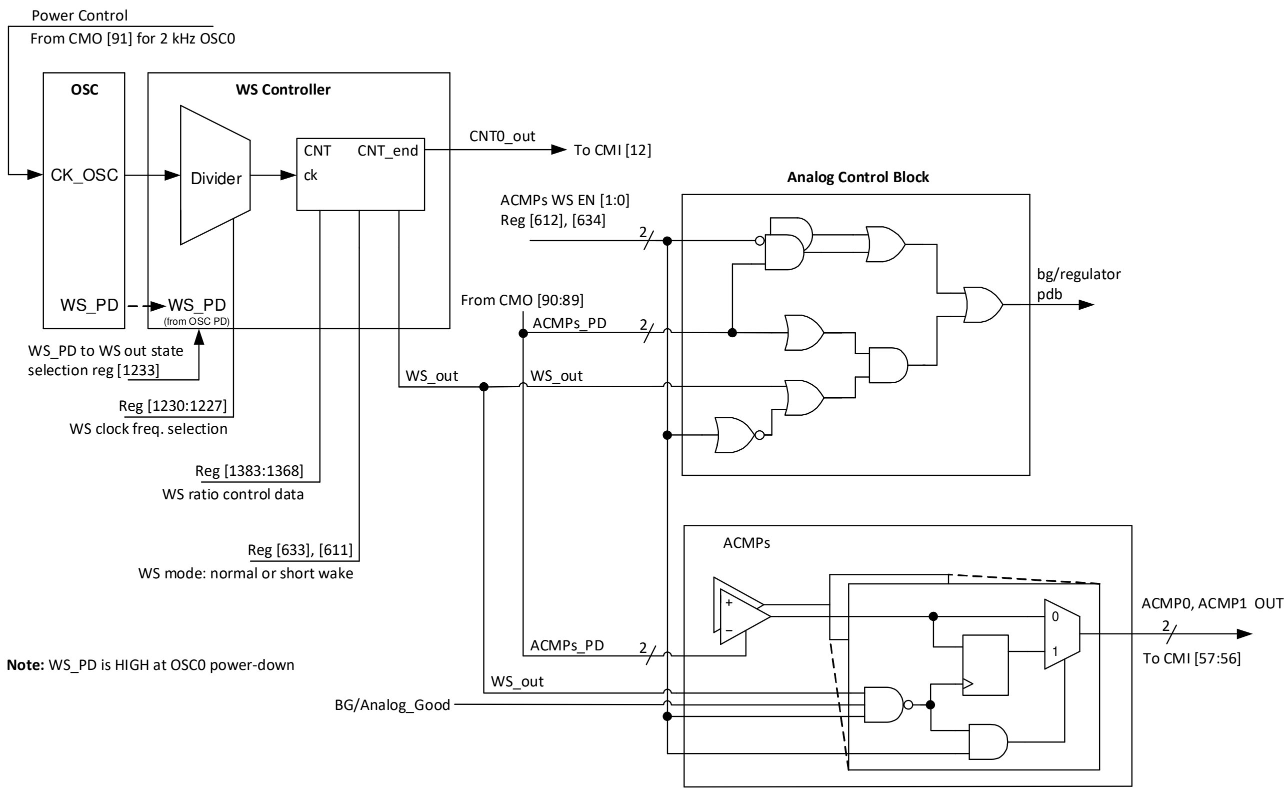


Figure 53. Wake and Sleep Controller

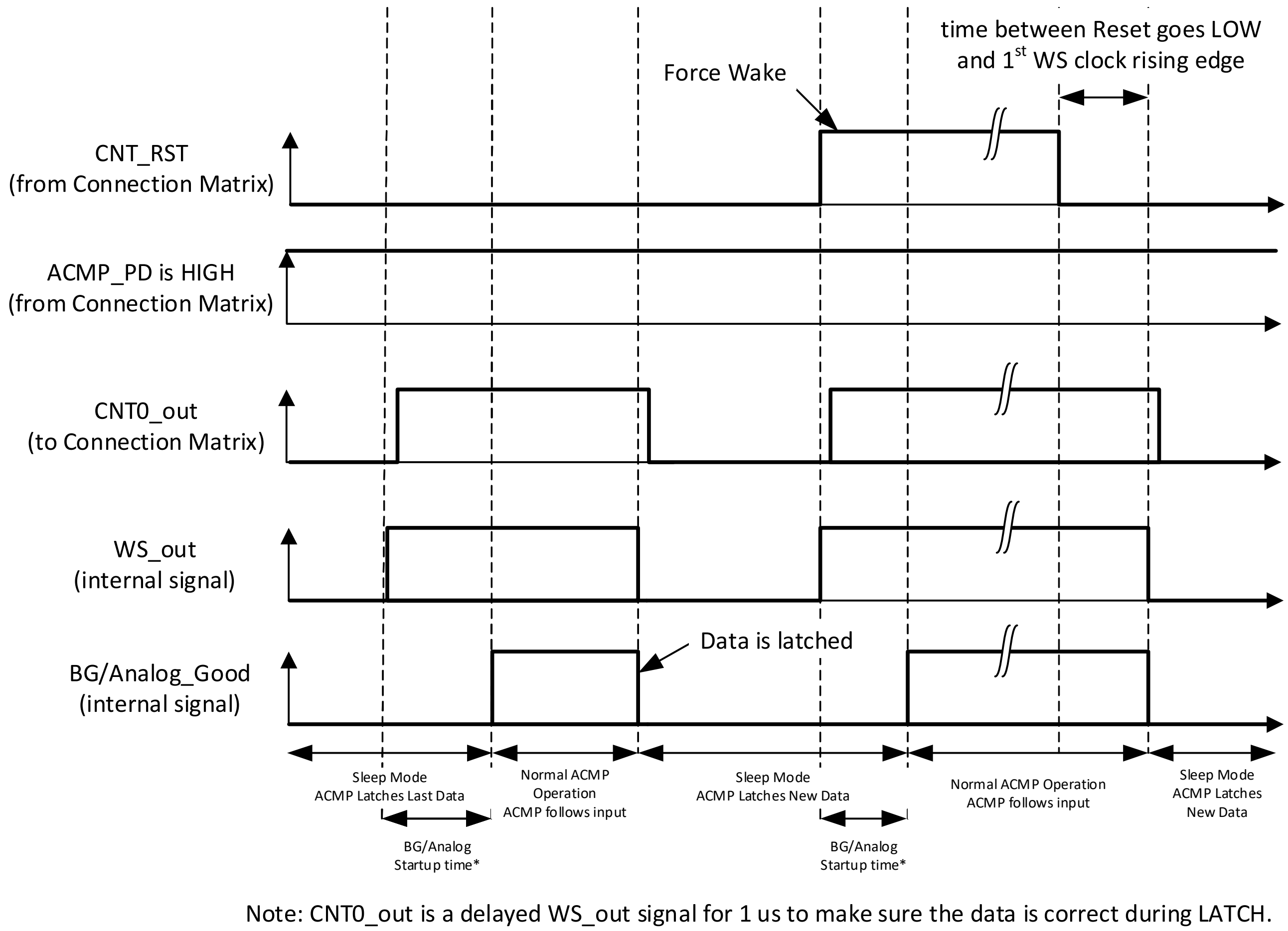


Figure 54. Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Reset is Used

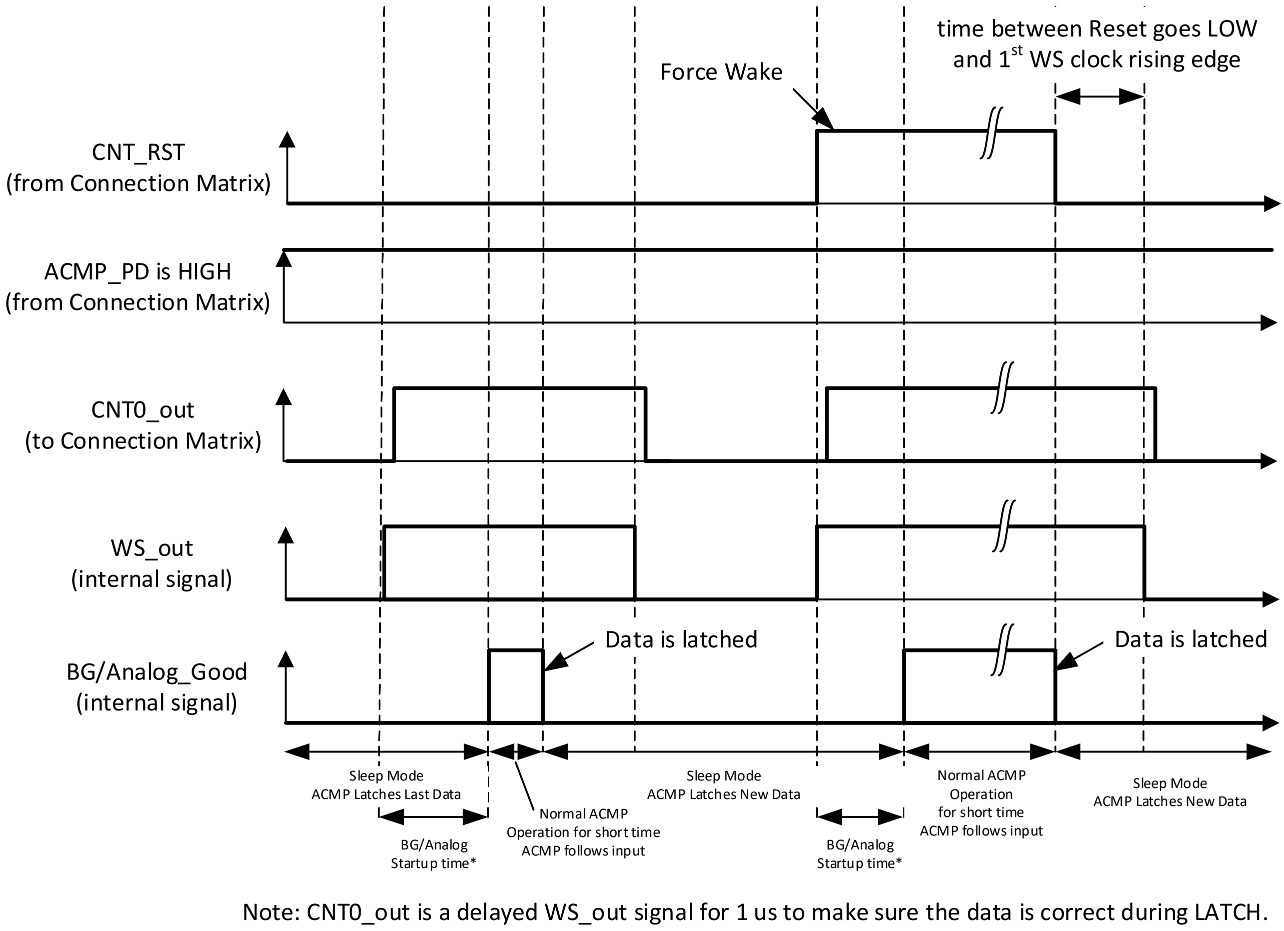
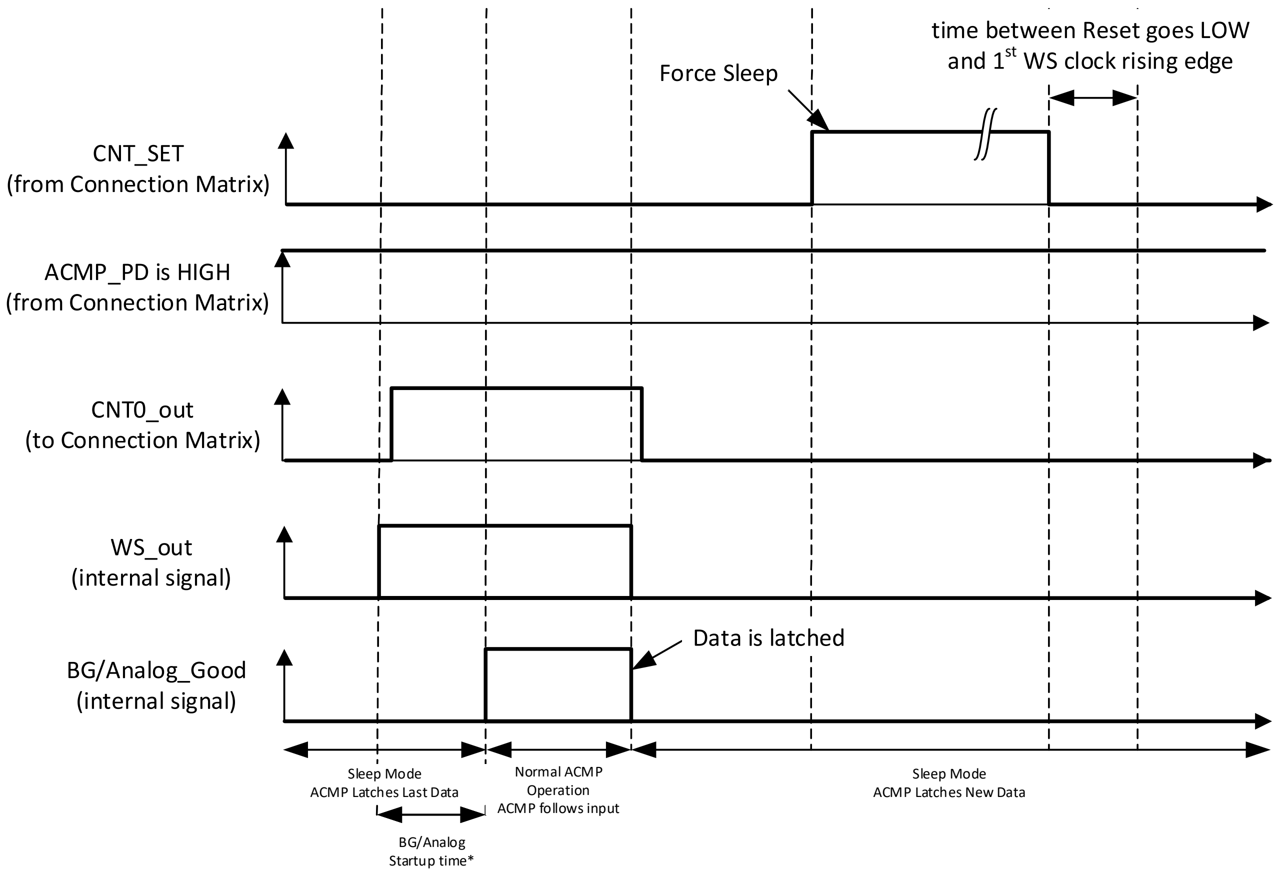


Figure 55. Wake and Sleep Timing Diagram, Short Wake Mode, Counter Reset is Used



Note: CNT0_out is a delayed WS_out signal for 1 us to make sure the data is correct during LATCH.

Figure 56. Wake and Sleep Timing Diagram, Normal Wake Mode, Counter Set is Used

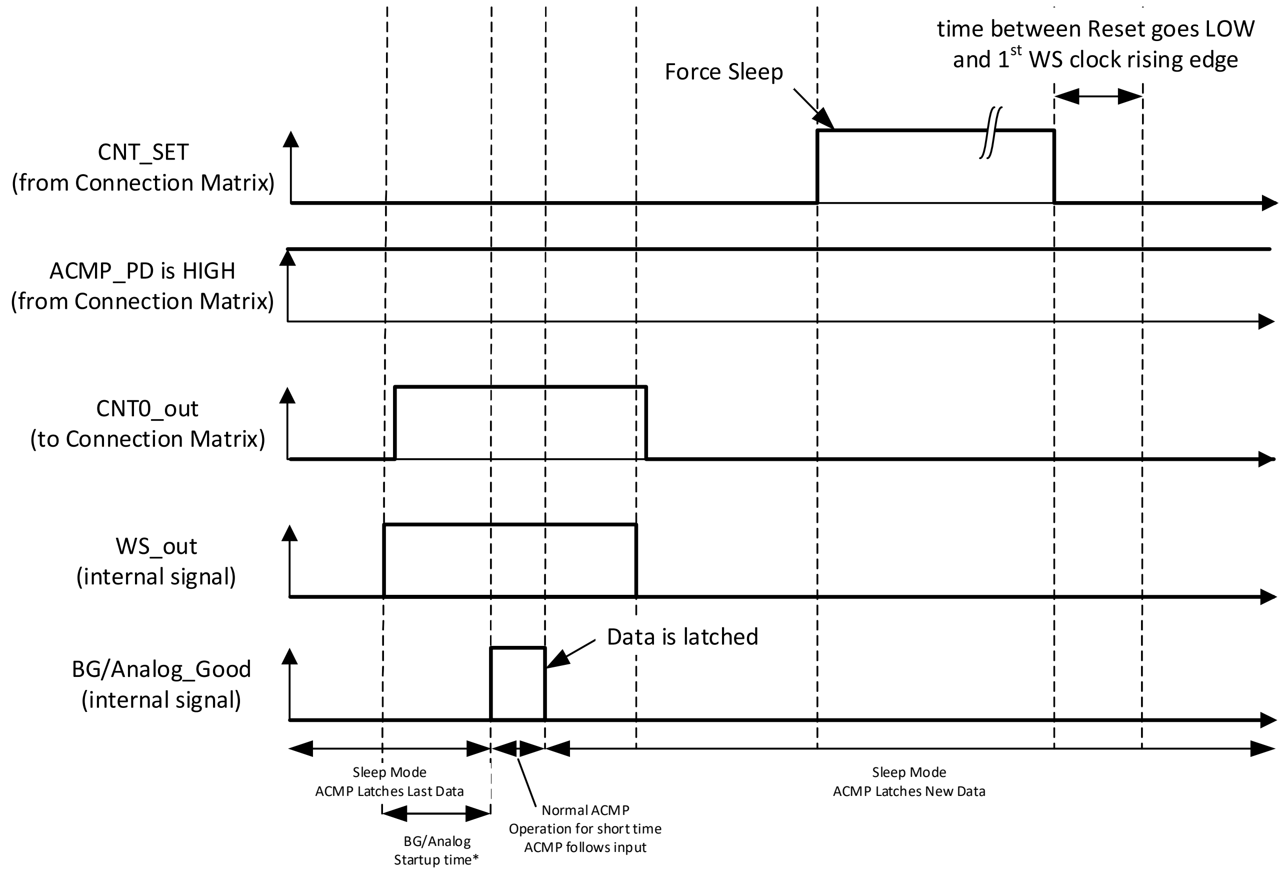


Figure 57. Wake and Sleep Timing Diagram, Short Wake Mode, Counter Set is Used

Note: If low power BG is powered on/off by WS, the wake time should be longer than 2.1 ms. The BG/analog start up time will take maximal 2 ms. If low power BG is always on, OSC0 period is longer than required wake time. The short wake mode can be used to reduce the current consumption. The short wake mode is edge triggered, when the wake signal is latched by rising edge and released the Power-On signal after the ACMP output data is latched. This allows to have a valid ACMP data for any type of wake signal and have the optimized current consumption.

To use any ACMP under WS controller, the following settings must be done:

- CNT/DLY0 must be set to Wake and Sleep Controller function (for all ACMPs)
- Register WS → enable (for each ACMP separately)
- CNT/DLY0 set/reset input = 0 (for all ACMPs).

As the OSC any oscillator with any pre-divider can be used. The user can select a period of time while the ACMP is sleeping in a range of 1 - 65535 clock cycles. Before they are sent to sleep their outputs are latched, so the ACMPs remain their state (High or Low) while sleeping.

WS controller has the following settings:

- Wake and Sleep Output State (High/Low)

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = High, the ACMP is continuously on.

  If OSC is powered off (Power-down option is selected; Power-down input = 1) and Wake and Sleep Output State = Low, the ACMP is continuously off.

  Both cases WS function is turned off.

- Counter Data (Range: 1 - 65535).

The User can select wake and sleep ratio of the ACMP; counter data = sleep time, one clock = wake time.

- Q mode - defines the state of WS counter data when Set/Reset signal appears Reset - when active signal appears, the WS counter will reset to zero and High level signal on its output will turn on the ACMPs. When Reset signal goes out, the WS counter will go Low and turn off the ACMPs until the counter counts up to the end. Set - when active signal appears, the WS counter will stop and Low level signal on its output will turn off the ACMPs. When Set signal goes out, the WS counter will go on counting and High level signal will turn on the ACMPs while counter is counting up to the end.

Note: The OSC0 matrix power down to control ACMP WS is not supported for short wait time option.

- Edge Select defines the edge for Q mode.
  High level Set/Reset - switches mode Set/Reset when level is High.

Note: Q mode operates only in case of “High Level Set/Reset”.

- Wake time selection - time required for wake signal to turn the ACMPxH on.

  Normal Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on until WS signal is Low again. Wake time is one clock period. It should be longer than BG turn on time and minimal required comparing time of the ACMP.

  Short Wake Time - when WS signal is High, it takes BG/analog start up time to turn the ACMPs on. They will stay on for 1 µs and turn off regardless of WS signal. The WS signal width does not matter.
- Keep - pauses counting while Keep = 1.
- Up - reverses counting.

  If Up = 1, CNT is counting up from user-selected value to 65535.

  If Up = 0, CNT is counting down from user-selected value to 1.

9. Analog Comparators

There are two Low Power Rail-to-Rail General Purpose Analog Comparator (ACMP) macrocells in the SLG47004-A. For the ACMP macrocells to be used in a GreenPAK design, the power-up signals (ACMP0_L_pdb and ACMP1_L_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be ON continuously, OFF continuously, or switched on periodically, based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low. Two General Purpose Analog Comparators are optimized for low power operation.

Each of the General Purpose ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage (1x, 0.5x, 0.33x, 0.25x) before connection to the analog comparator. The gain divider is unbuffered and has an input resistance of 2 MΩ (typ) for 0.5x, 0.33x, 0.25x, and 10 GΩ for 1x. Each of the General Purpose ACMP macrocells has a negative input signal that is either created from an internal Vref or provided by any external source (from external pins). Note that the external Vref signal is filtered with a 2nd order low pass filter with 8 kHz typical bandwidth, see in Figure 58 and Figure 59.

Input bias current < 1 nA (typ).

Power-Up = 1 => ACMP is powered up.

Power-Up = 0 => ACMP is powered down.

Both General Purpose Analog Comparators have "Low Energy Power Up" setting (register [608] - ACMP0, register [630] - ACMP1). When enabled, it allows reducing average power consumption during ACMP power up process. This setting changes power up sequence of analog macrocells:

Low Energy Power Up register [608], register [630] = 0 - all analog macrocells associated with ACMP turns on simultaneously.

Low Energy Power Up register [608], register [630] = 1 - the first macrocell that begins to turn on is Bandgap. Other analog macrocells begin to turn on only after BG_OK signal is valid. This option slightly increases general ACMP Power-On time, while reducing the average current consumption.

During power-up, the ACMP output will remain LOW, and then becomes valid after power up signal goes high for ACMP0_L and ACMP1_L (see parameter t_{start} in Table 20).

Each cell also has a flexible hysteresis selection, to offer hysteresis of 32 steps, but not more than Vref voltage. It means that there are 6-bits to select Vref and independent 6-bits to select the hysteresis (no need to have an adder logic).

It's possible to enable low pass filter at the Vref input. But it's highly recommended to enable this LPF only when hysteresis Vhys > 196 mV.

ACMP0_L IN+ options are OA0_out, GPIOx (PIN), V_{DD}.
ACMP1_L IN+ options are OA1, GPIOx (PIN), ACMP0L_IN+, Temp Sensor OUT.

9.1 ACMP0L Block Diagram

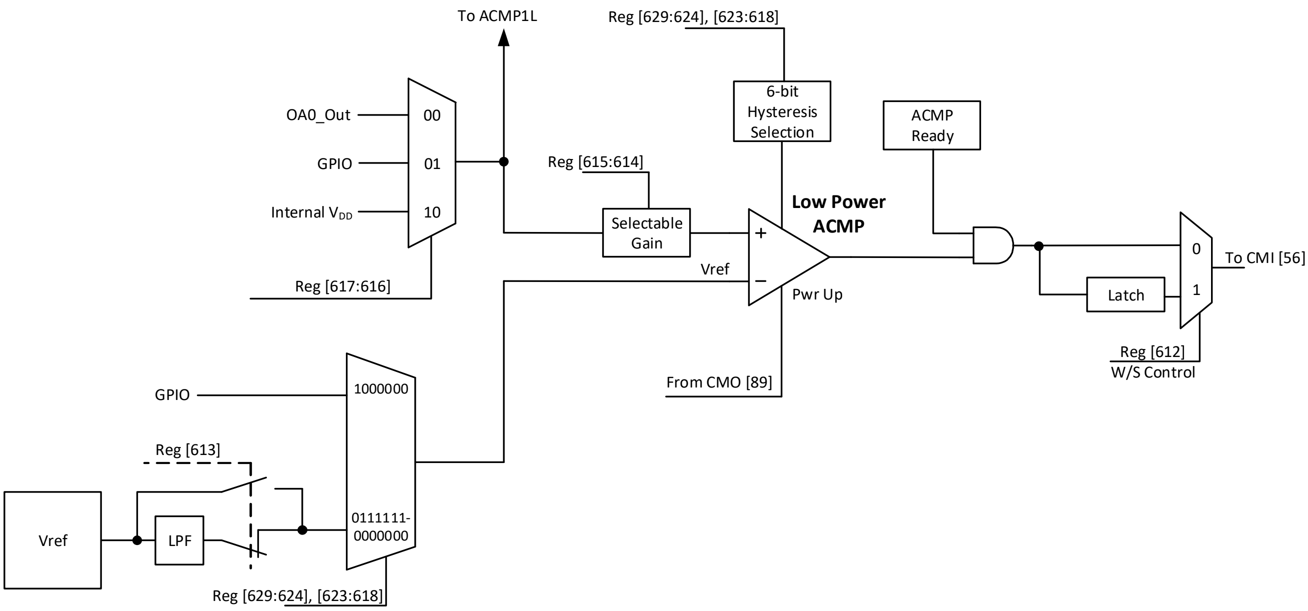


Figure 58. ACMP0L Block Diagram

9.2 ACMP1L Block Diagram

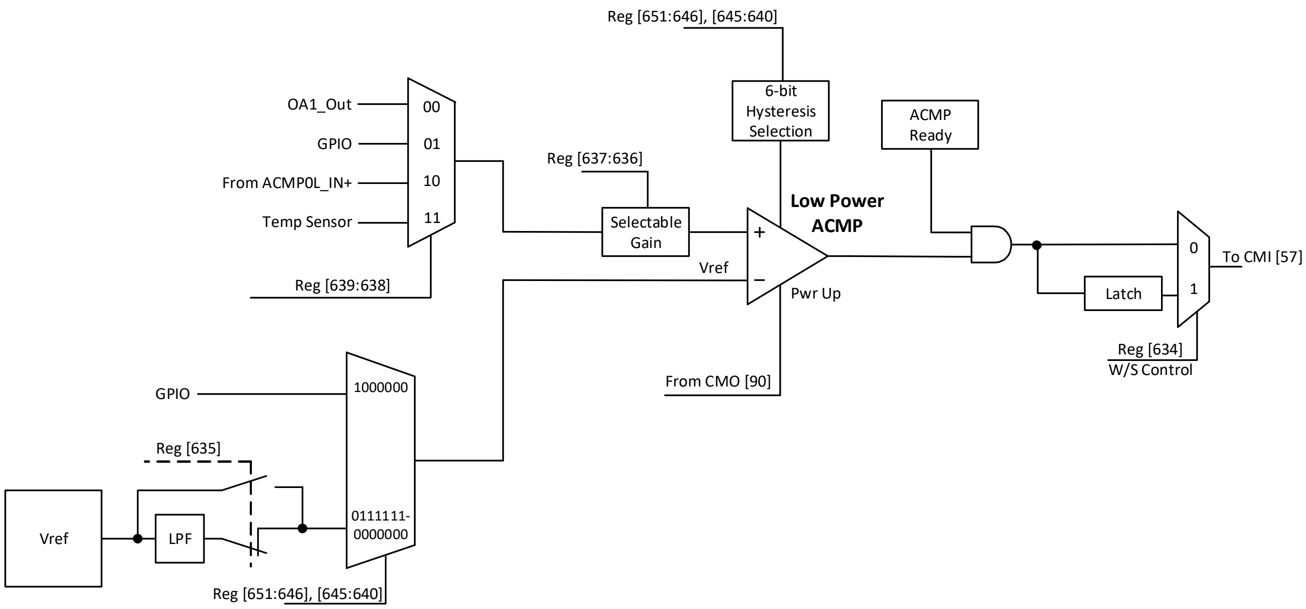


Figure 59. ACMP1L Block Diagram

9.3 Chopper Analog Comparator

There is one Chopper Rail-to-Rail Analog Comparator (ACMP) macrocells in the SLG47004-A. It is possible to use Chopper ACMP to do in system trim by changing the Rheostat resistance in Auto-Trim mode. It is also possible to use a Chopper ACMP as a general purpose analog comparator.

The chopper ACMP power up signal is controlled either by internal Auto-Trim logic (Set 0/1 of Digital Rheostat 0/1) or by matrix input.

The chopper ACMP is automatically powered on during the calibration time to control the up/down signal of the counter/rheostat, when the Auto-Trim is enabled (register [909]= 0).

In order to use Chopper ACMP as a standalone comparator (Auto-Trim mode is disabled, register [909] = 1) user should provide the clock signal to this macrocell. Clock source can be internal oscillators or any pulses from the connection matrix.

Note that clock frequency for the Chopper ACMP shouldn't be greater than f_{ChACMP}. Please refer to Table 27.

For proper Chopper ACMP operation it is recommended to force the bandgap on. It's highly recommended to force the bandgap on when OSC1 is used as a clock source for Chopper ACMP. Also, if Vref (bandgap) is used in the project, internal Vref should be stable before the 2nd rising edge of Chopper ACMP clock signal (see Figure 60). Please consider the bandgap turn on delay (approximately 1 ms).

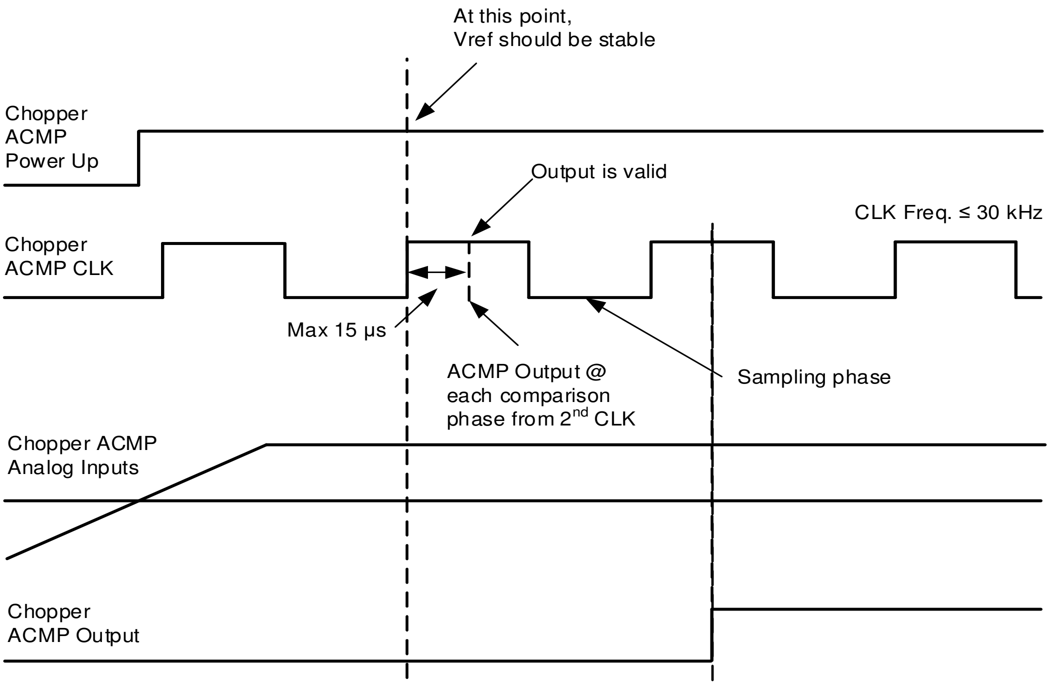


Figure 60. Chopper ACMP CLK Correct Operation. Bandgap Forced On

Output of Chopper ACMP can be optionally inverted by register [882].

The matrix output [85] is used to control chopper ACMP power up signal for the general purpose usage, see Figure 61. It is possible to use the chopper ACMP as a general purpose ACMP after Auto-Trim procedure is completed, since the power up signal is a logic OR of the latched Set (Digital Rheostat 0/1) signal and matrix signal. If Auto-Trim (Set 0/1 of Digital Rheostat 0/1) is disabled and chopper ACMP channel is set to Auto (Channel 0/1), then ACMP output defaults to Channel 0 while Channel 1 is ignored.

The power-up signals need to be active high in order to use the Chopper ACMP. By connecting to signals coming from the Connection Matrix, it is possible to have ACMP be ON continuously, OFF continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, its output is low.

There are no Gain and Hysteresis selection for chopper ACMP compared to the ACMP0L and ACMP1L.

It's possible to select different reference sources for Chopper ACMP. It can be:

- external voltage from pin
- divided internal voltage from internal reference source (from 32 mV to 2048 mV)
- divided internal reference voltage from HD Buffer (64 steps)
- divided V_{DDA} voltage (64 steps).

For more information see Section 15. Voltage Reference.

The positive input of the Chopper ACMP can be connected to the Op Amp0 out or Op Amp1 out or In Amp out, or to the external PIN.

The inputs of Chopper ACMP can be reconfigured while operating in AutoTrim mode. There is one configuration of inputs (Figure 61) for case when Set0 (Digital Rheostat 0) signal is latched, and another configuration of Chopper ACMP inputs when Set1 (Digital Rheostat 1) signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 (Digital Rheostat 0) is latched and Chopper_ACMP+ pin when Set1 (Digital Rheostat 1) is latched. The same way, "-" input of Chopper ACMP can be configured to work with any of possible inputs when Set0 (Digital Rheostat 0) or Set1 (Digital Rheostat 1) are latched.

Note that the default configuration is the configuration for Set0 (Digital Rheostat 0) signal. When Chopper ACMP operates as separate ACMP and AutoTrim function is disabled, inputs of Chopper ACMP are defined by registers [893:892].

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (register 946 = 0) and Chopper ACMP is powered up.

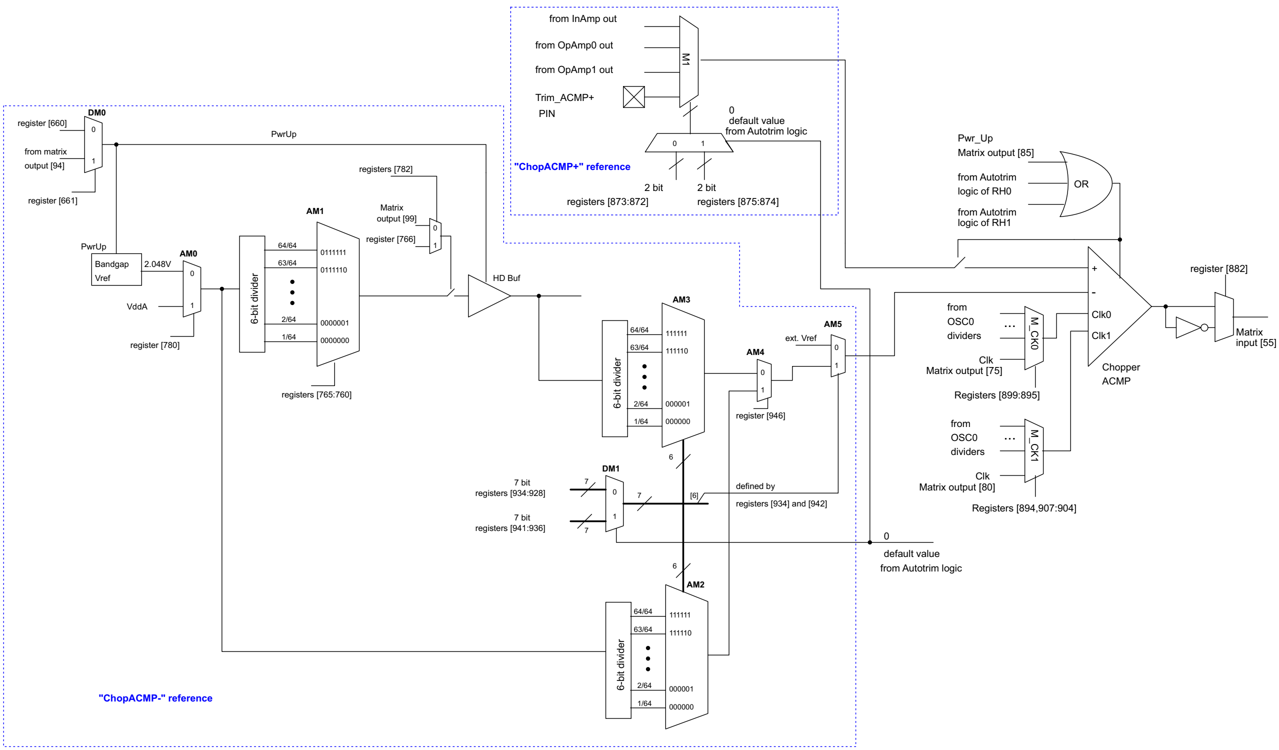


Figure 61. Chopper ACMP Block Diagram

9.4 ACMP Sampling Mode

Both General Purpose Analog Comparators (ACMPL0 and ACMPL1) have an optional sampling mode. In this mode, ACMP is enabled for the shortest amount of time after rising edge at Power Up input to get a valid data. Then ACMP latches its value and goes sleep again.

Registers [610], [632] enable sampling mode for two comparators.

9.5 ACMP Typical Performance

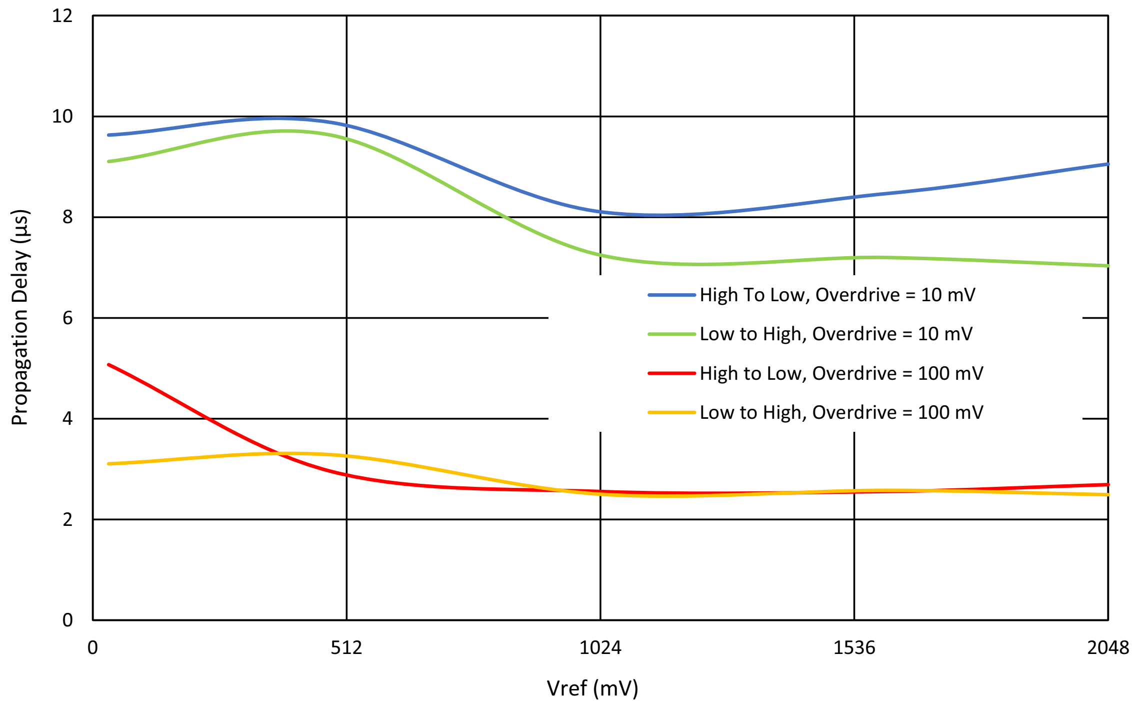


Figure 62. Propagation Delay vs. Vref for ACMPx at T_A = 25 °C, V_{DD} = 2.4 V to 5.5 V, Hysteresis = 0

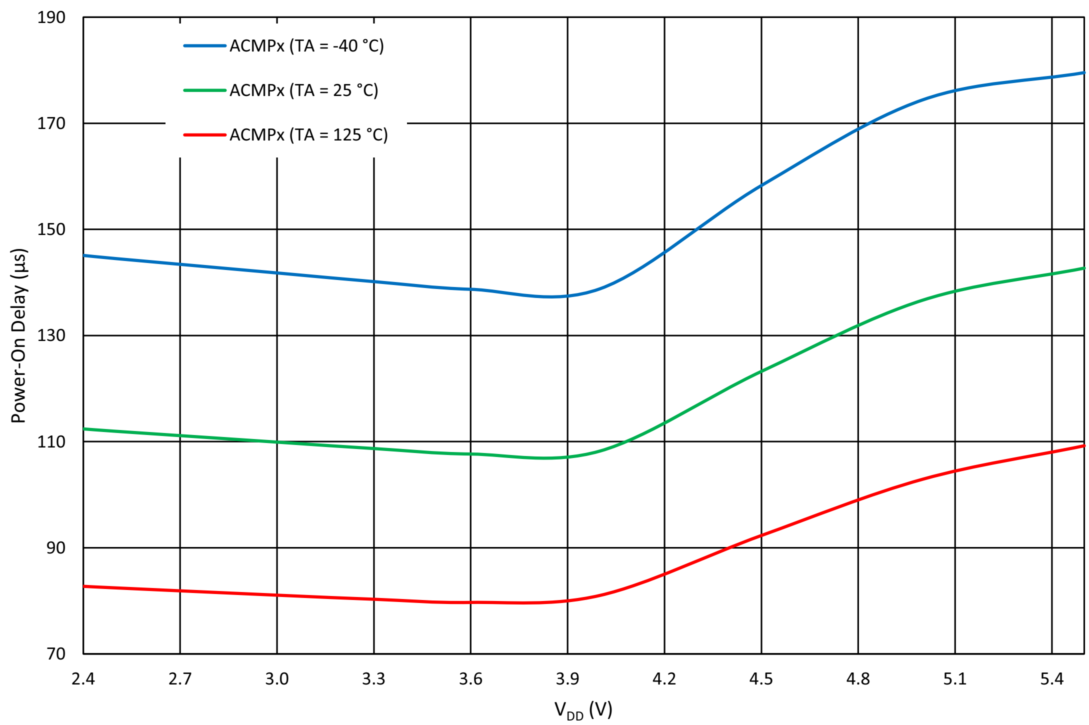


Figure 63. ACMPx Power-On Delay vs. V_{DD} at BG - Forced

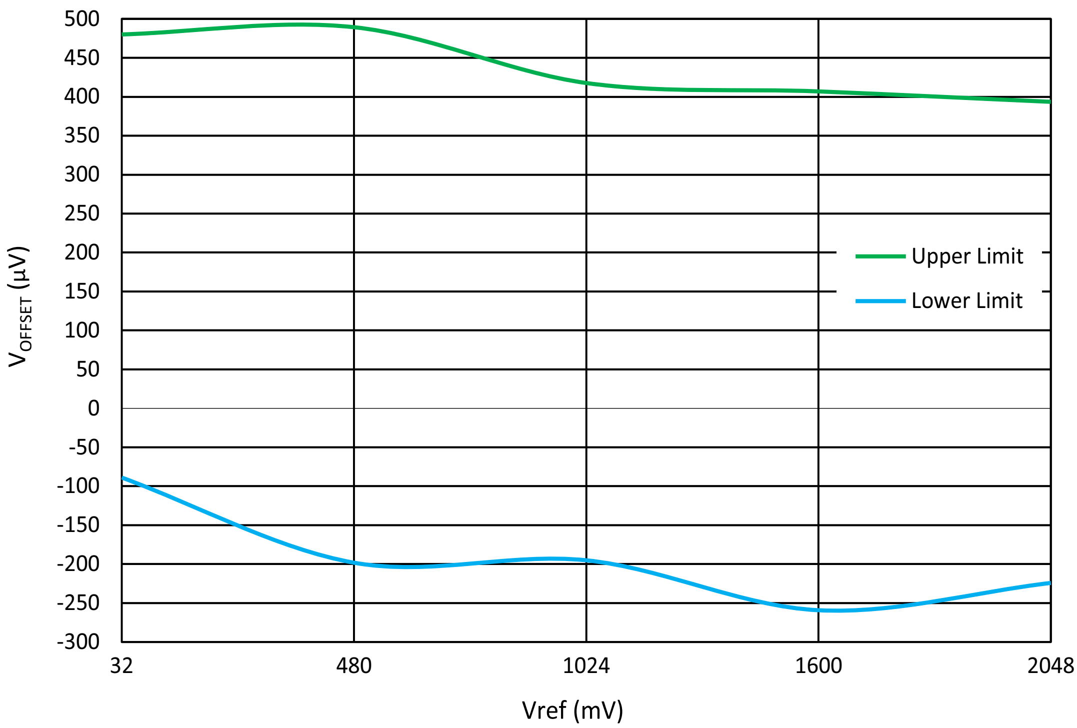


Figure 64. ACMPx Input Offset Voltage vs. Vref at T_A = -40 °C to 125 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

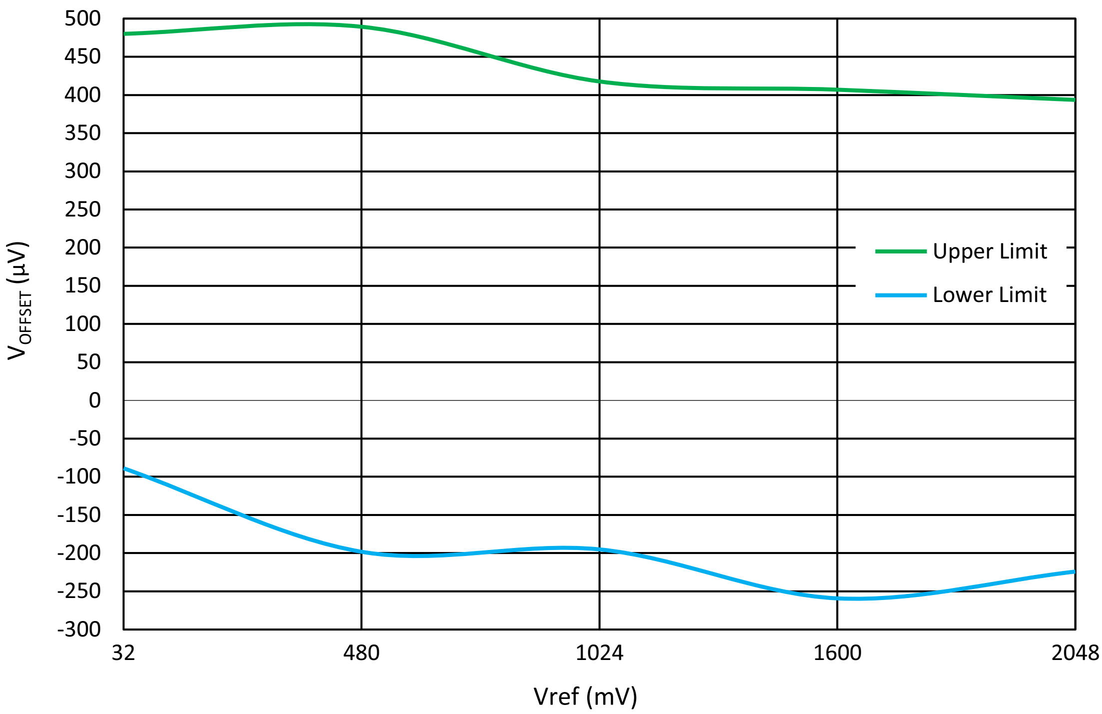


Figure 65. Chopper ACMP Input Offset Voltage vs. Vref at T_A = -40 °C to 125 °C, V_{DD} = 2.4 V to 5.5 V, Gain = 1

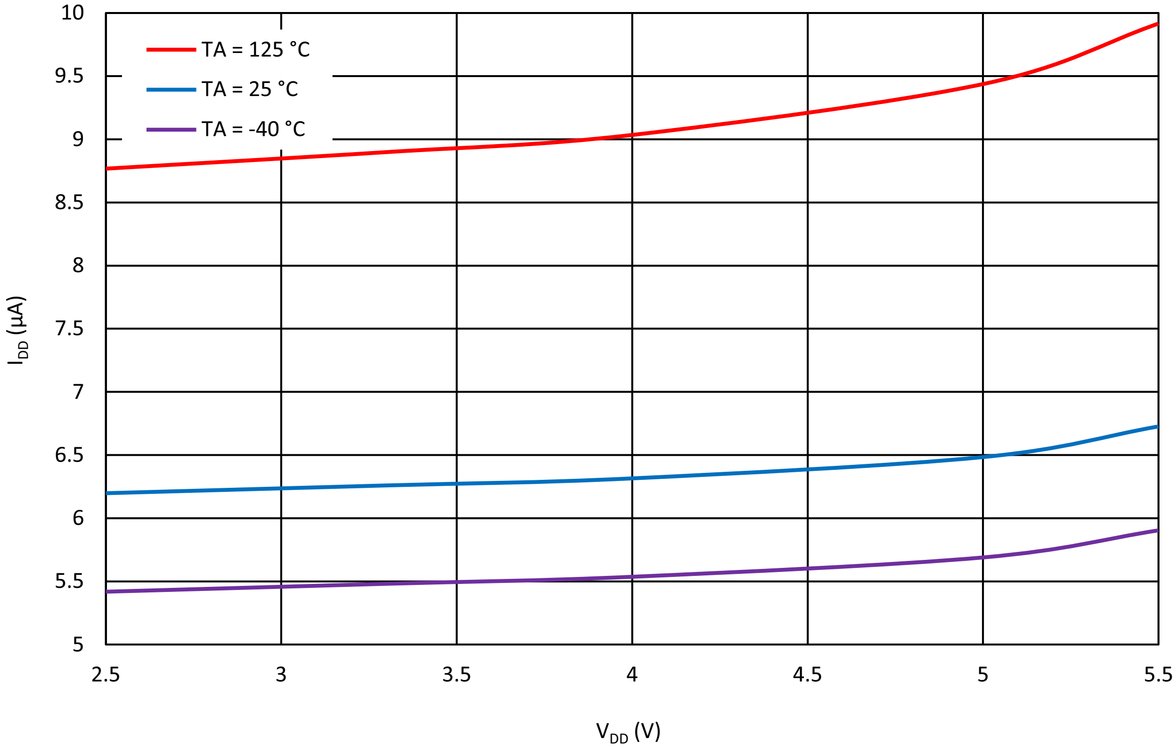


Figure 66. ACMPx Current Consumption vs. V_{DD}

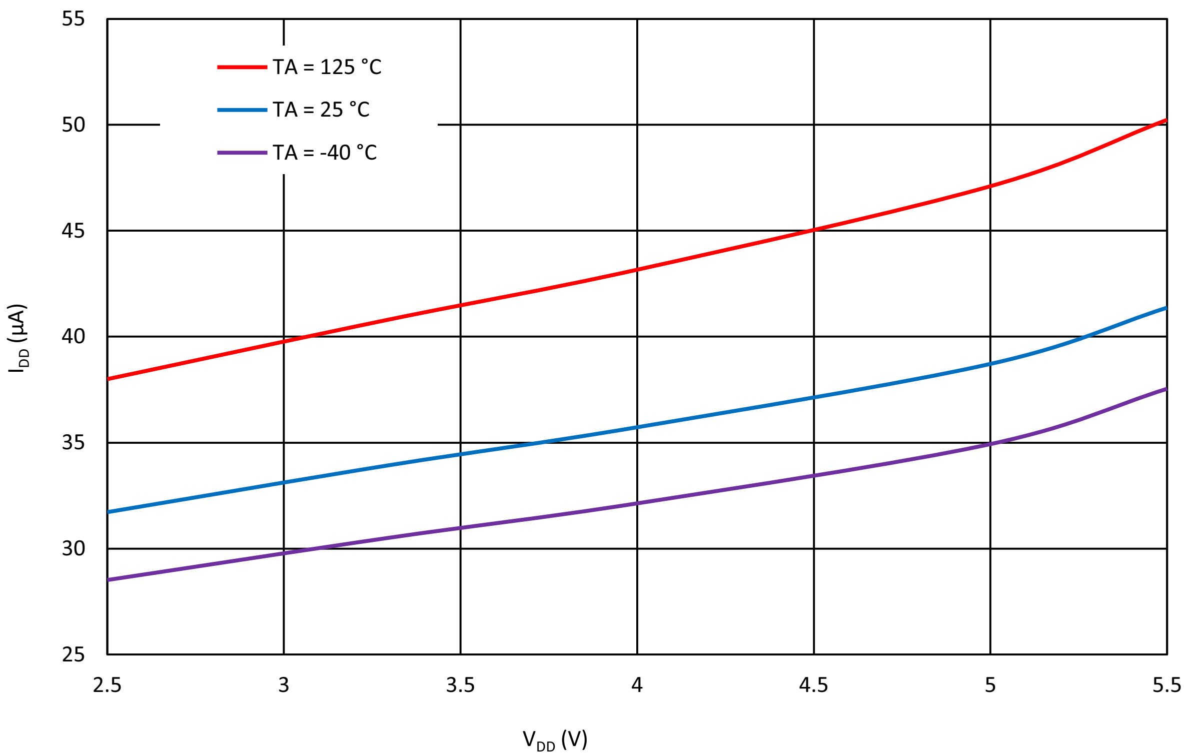


Figure 67. Chopper ACMP Current Consumption vs. V_{DD} (with 2.048 kHz Clock)

10. Programmable Operational Amplifiers

10.1 General Description

The SLG47004-A contains three operational amplifiers with rail-to-rail input and output. Two of them (Programmable Op Amps) have the additional functions of driving internal analog FETs (Voltage Regulator and Current Sink modes) and Comparator mode. The third Internal Op Amp is an amplifier with internal resistors, and can be configured as a difference amplifier with Gain = 1. All three op amps can function as instrumentation amplifiers. The structures of the op amps are shown in Figure 68 and Figure 69.

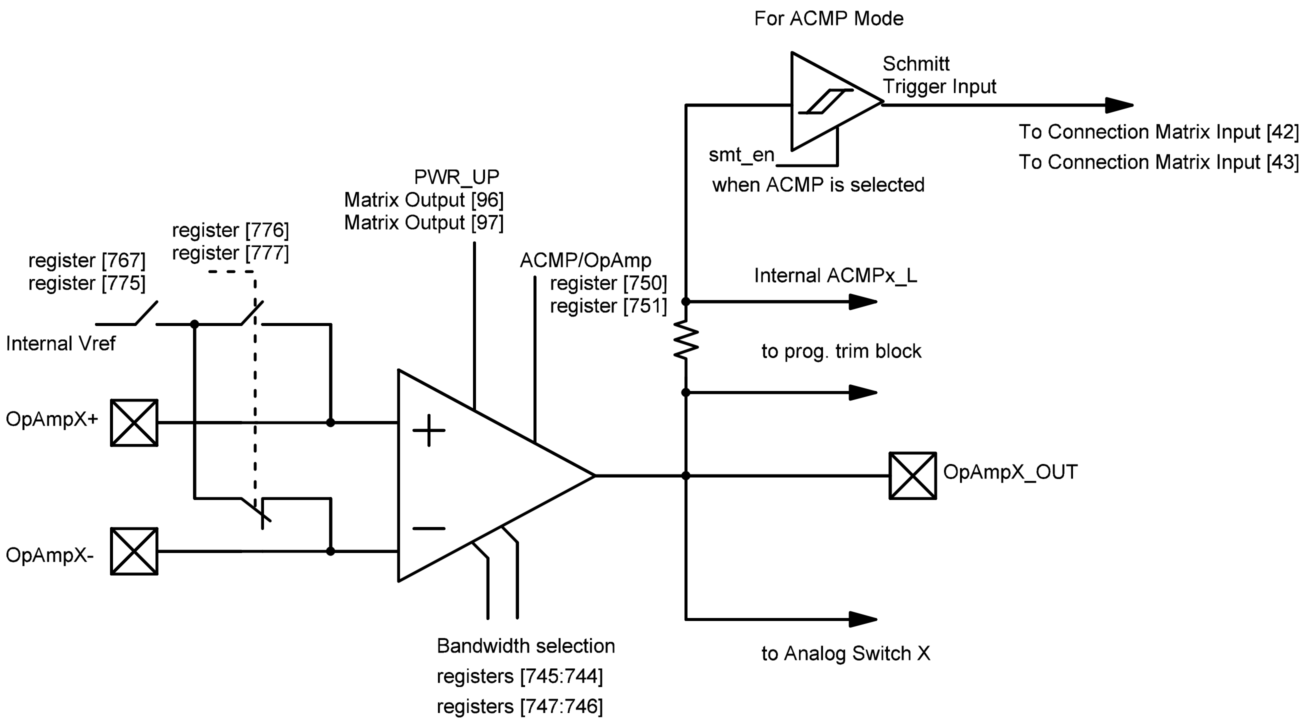


Figure 68. Programmable Operational Amplifier OA0, OA1 Internal Circuit

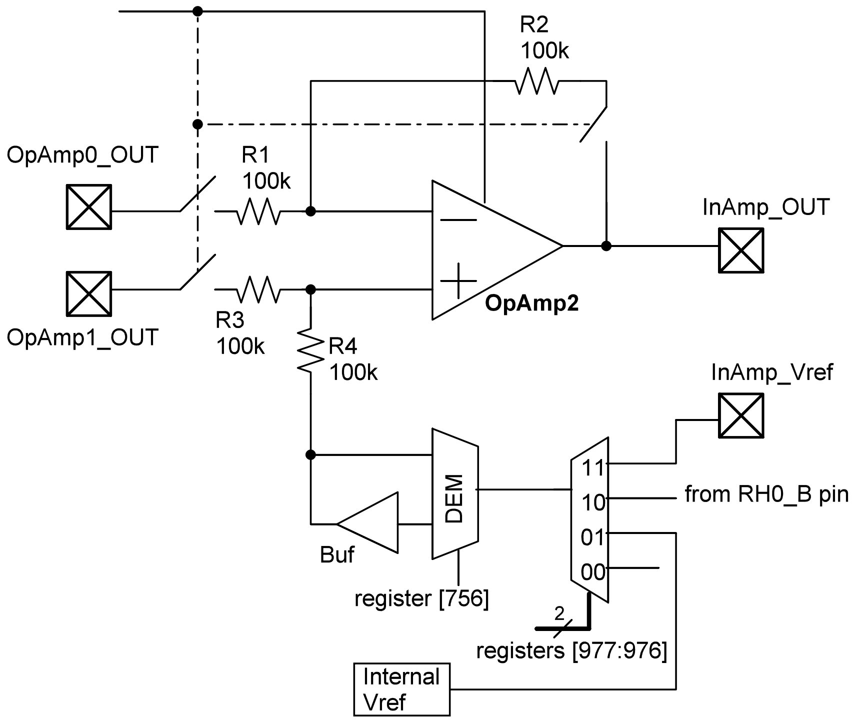


Figure 69. Internal Operational Amplifier Circuit

Each of the two Programmable Op Amp inputs has a hardware connection to the external pin and an optional connection to the internal voltage reference source, which makes it possible to create precise voltage or current source. For more detailed description of op amp Vref sources see Section 15. Voltage Reference. The output of the operational amplifier is hardwired to an external pin. This output can also be connected to the Programmable Trim block of rheostat macrocell, ACMP non-inverting input (ACMP0_L+ for OA0, ACMP1_L+ for OA1), or control the corresponding Analog Switch, depending on the mode of operation. Each Programmable Op Amp can also be configured as an analog comparator, in which case its output signal is connected to the Connection Matrix through a dedicated buffer.

Each Programmable Op Amp has a programmable bandwidth that can be set by two register bits. In addition, internal charge pump setting for each Op Amp must be changed according to bandwidth selection, see Table 58.

Internal charge pump can be disabled if input common-mode voltage $V_{CM} < (V_{DDA} - 1.5\ V)$. But it is strongly recommended to keep the default setting (enable charge pump).

The bandwidths may vary up to +/-30 % over PVT. Each operational amplifier is factory trimmed. This trimming is independent of the trimming associated with the onboard digital rheostat (system calibration).

The Internal operational amplifier shares its inputs with the Programmable Op Amps outputs. The voltage reference for the internal amplifier can be sourced from either the internal or external Vref. Note that if the internal Vref is used as a source for the instrumentation amplifier Vref, the user can optionally connect this Vref to the output pin, or disconnect the Vref from output pin and use this pin as GPIO.

Also, if the Internal Op Amp is inactive (In Amp Mode is disabled), the user can use the In Amp_Vref pin as GPIO. The In Amp_Out pin can be configured as GPI.

Table 58. Op Amps Bandwidth Settings

Op Amp Bandwidth Selection	Op Amp0				Op Amp1				Op Amp2 (Internal)			
	Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency		Bandwidth Selection		Charge Pump Frequency	
Register Bit →	745	744	955	954	747	746	963	962	749	748	971	970
128 kHz	0	0	0	0	0	0	0	0	0	0	0	0
512 kHz	0	1	0	1	0	1	0	1	0	1	0	1
2.048 MHz	1	0	1	0	1	0	1	0	1	0	1	0
8.192 MHz	1	1	1	1	1	1	1	1	1	1	1	1

10.1.1 Maximum Differential Input Voltage Protection Circuit

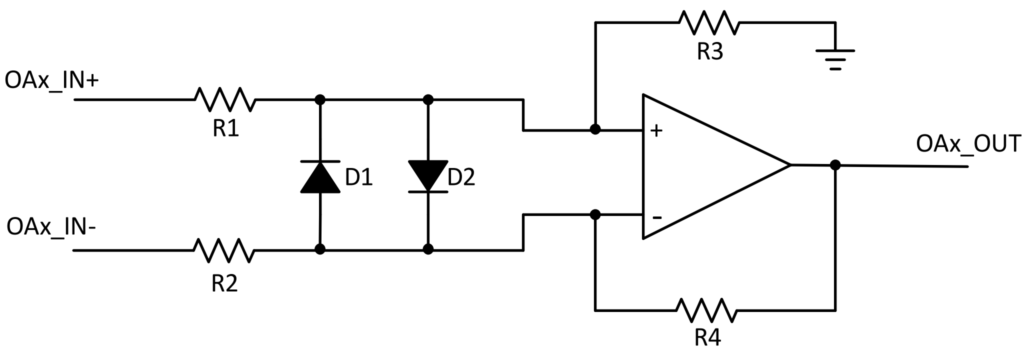


Figure 70. Differential Input Protection of OpAmp using Diode Clamping

To keep the SLG47004-A OpAmp inputs within their maximum differential voltage ratings, it is recommended to use external diodes to clamp the differential input voltage, as shown with diodes D1 and D2 in Figure 70. Such clamps prevent the differential voltage from exceeding the recommended operating differential voltage rating (see DV in Table 6), which can cause permanent shifts of such parameters as input offset voltage. The forward voltage drop of used diodes must not exceed the recommended maximum differential voltage rating at the maximum operating ambient temperature expected in the system design.

10.2 Modes of Operation

In order to use any of the op amp macrocells in the GreenPAK Designer, the power up signal (PWR_UP) must be set to logic High. By default, all op amp macrocells are turned off after SLG47004-A startup. During power-up, outputs of all op amps will remain in a Hi-Z state and then become valid (see parameter t_{on} in Table 26).

Operational amplifiers turn-on time can be decreased by setting register bits [759:757] to 1. In this case op amps analog supporting blocks are always turned on. Note that current consumption of op amp will be increased when op amp is powered down and bits [759:757] is 1 (see Section 3.14 Programmable Operational Amplifier Specifications).

See the list below for the op amp operation modes:

- Operational Amplifier mode
- Instrumentation Amplifier mode
- Analog Comparator mode
- Voltage Regulator mode
- Current Sink mode.

10.2.1 Operational Amplifier Mode

In this mode, the Programmable Op Amp operates as a conventional operational amplifier. Also, the Programmable Op Amp can source the corresponding non-inverting ACMP input (see ACMP macrocell settings). The output of the Programmable Op Amp macrocell is in a Hi-Z state while the macrocell is turned off.

Figure 71 shows the example of differential amplifier with input offset voltage compensation with help of digital rheostat and programmable trim block. Zero input voltage equal to output voltage $V_{OUT} = V_{DD}/2$.

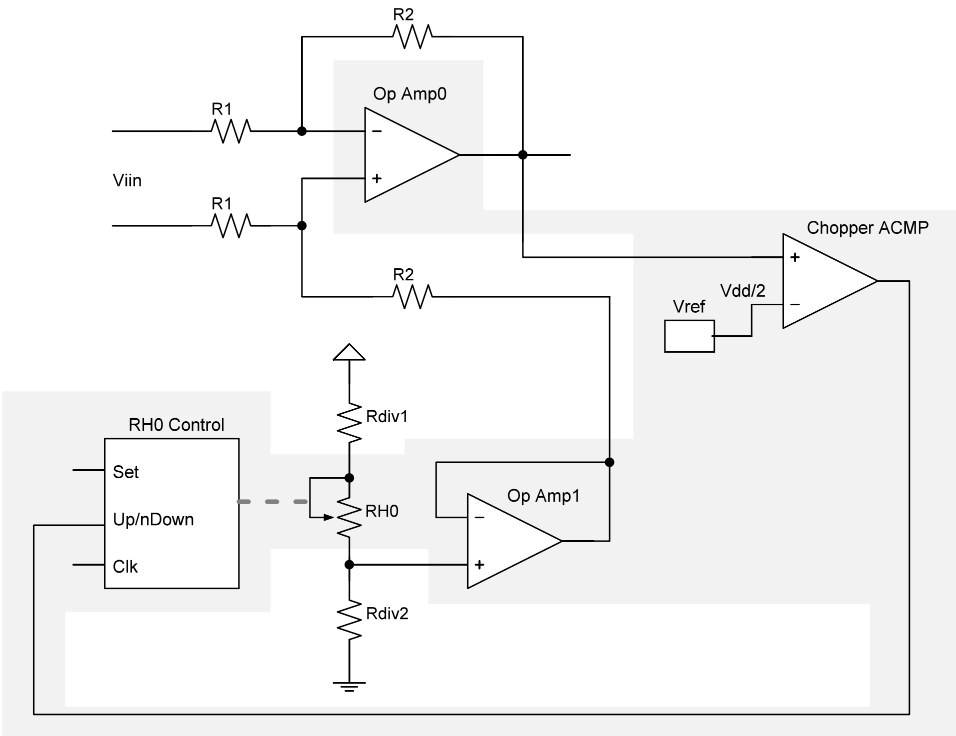


Figure 71. Example of Input Voltage Offset Compensation

10.2.2 Instrumentation Amplifier Mode

If this mode is active (Matrix Output [98] is High level), the two Programmable Op Amps and the single Internal Op Amp work together in Instrumentation Amplifier configuration, shown in Figure 72. When power up signal is logic LOW the output of In Amp is in Hi-Z state.

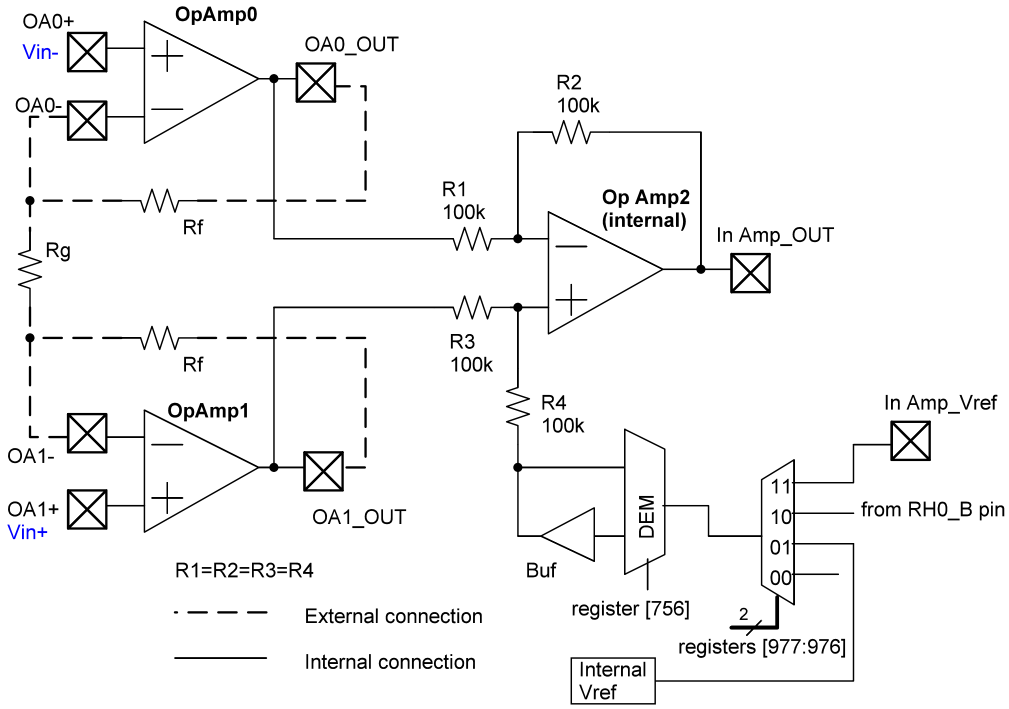


Figure 72. Instrumentation Amplifier Structure

The absolute value of internal resistors R_1, R_2, R_3, R_4 is 100 kΩ. The resistors R_f and R_g are user defined external resistors. The output voltage V_{OUT} of the instrumentation amplifier shown in Figure 72 is

$$V_{OUT} = (1 + 2R_f / R_g)(V_{IN+} - V_{IN-}) + V_{REF}$$

The user can trim both the gain and the offset error of the instrumentation amplifier using two of the Rheostats from the SLG47004-A. Figure 73 shows the configuration of the instrumentation amplifier in this scenario.

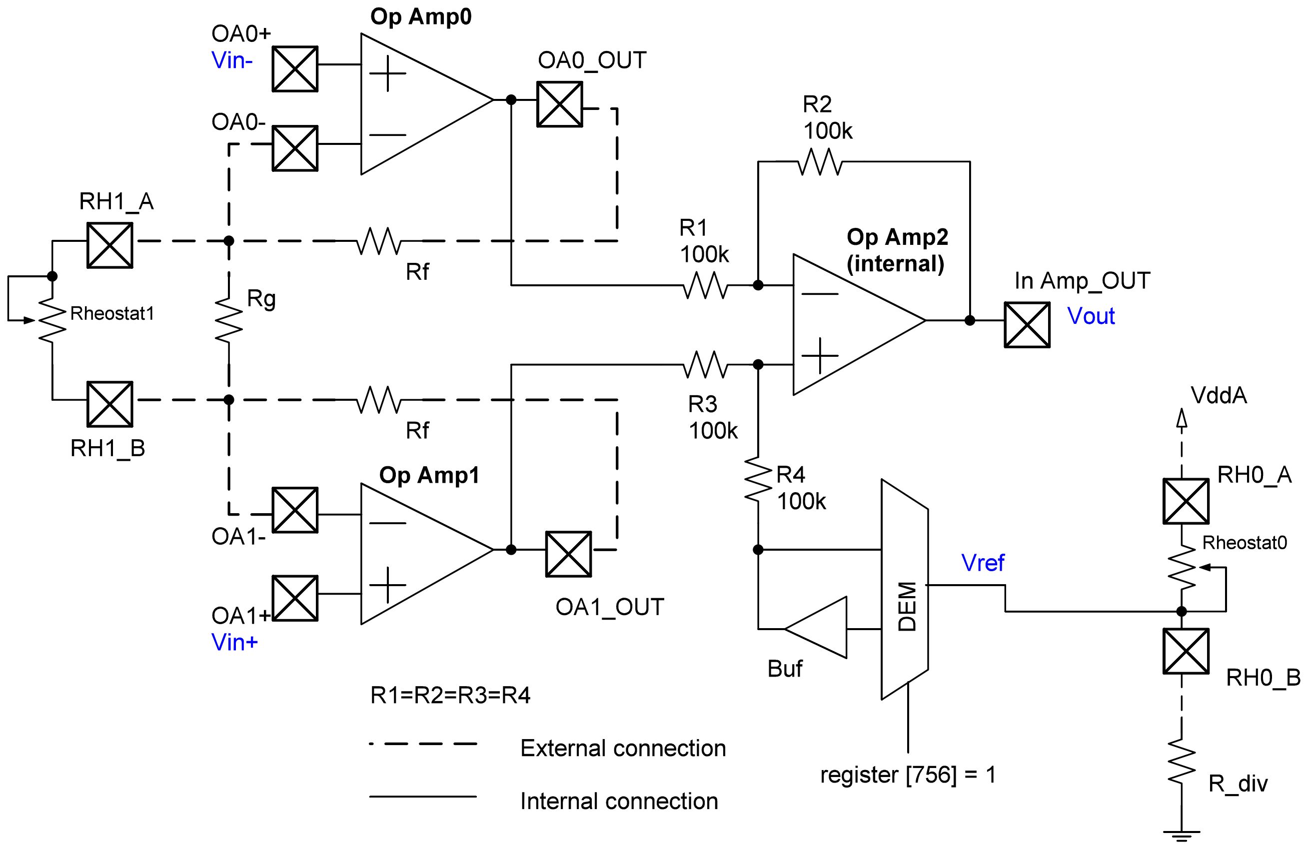


Figure 73. Instrumentation Operational Amplifier Configuration for Users Trim

Note that in Figure 73, the Demux connects to the Vref external input with an internal buffer (register [756] = 1). This allows us to eliminate the influence of resistor divider R_{div} and Rheostat0 on instrumentation amplifier.

It is possible to use a built-in Auto-Trim function for either setting the zero point of the Wheatstone bridge sensor using the In Amp or tuning a system output voltage to the desired level. However, the following limitations exist for using the built-in Auto-Trim function to trim both total system offset and system gain errors:

- The Auto-Trim procedures of total offset compensation and system gain error must be done iteratively starting and finishing with the total offset compensation: 1st iteration - offset compensation, 2nd iteration - gain trim, 3rd iteration - offset compensation. Extra iterations can be added to achieve a better accuracy. The last iteration should be an offset compensation.
- Total system offset (sensor offset + Op Amp1 offset + Op Amp2 offset) must not be greater than Vsensor_output_range/2.

It's possible to power external components like bridge or ADC from internal HD Buffer of SLG47004-A to improve accuracy of system.

10.2.3 Analog Comparator Mode

Both operational amplifiers have an Analog Comparator mode in which they work as conventional rail-to-rail comparators.

10.2.4 Voltage Regulator Mode

In this mode, the op amp output drives P-FET (part of Analog Switch). Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement voltage regulator mode using Analog Switch 0. In this mode the op amp output is High when the macrocell is turned off. Figure 74 (A) shows the typical implementation of the voltage source function. Optionally, the user can use this mode to implement a constant current source with load connected to ground (Figure 74, B, C). Note that op amp must operate in operational amplifier mode (register 750 = 0 for Op Amp0, register 751 = 0 for Op Amp1).

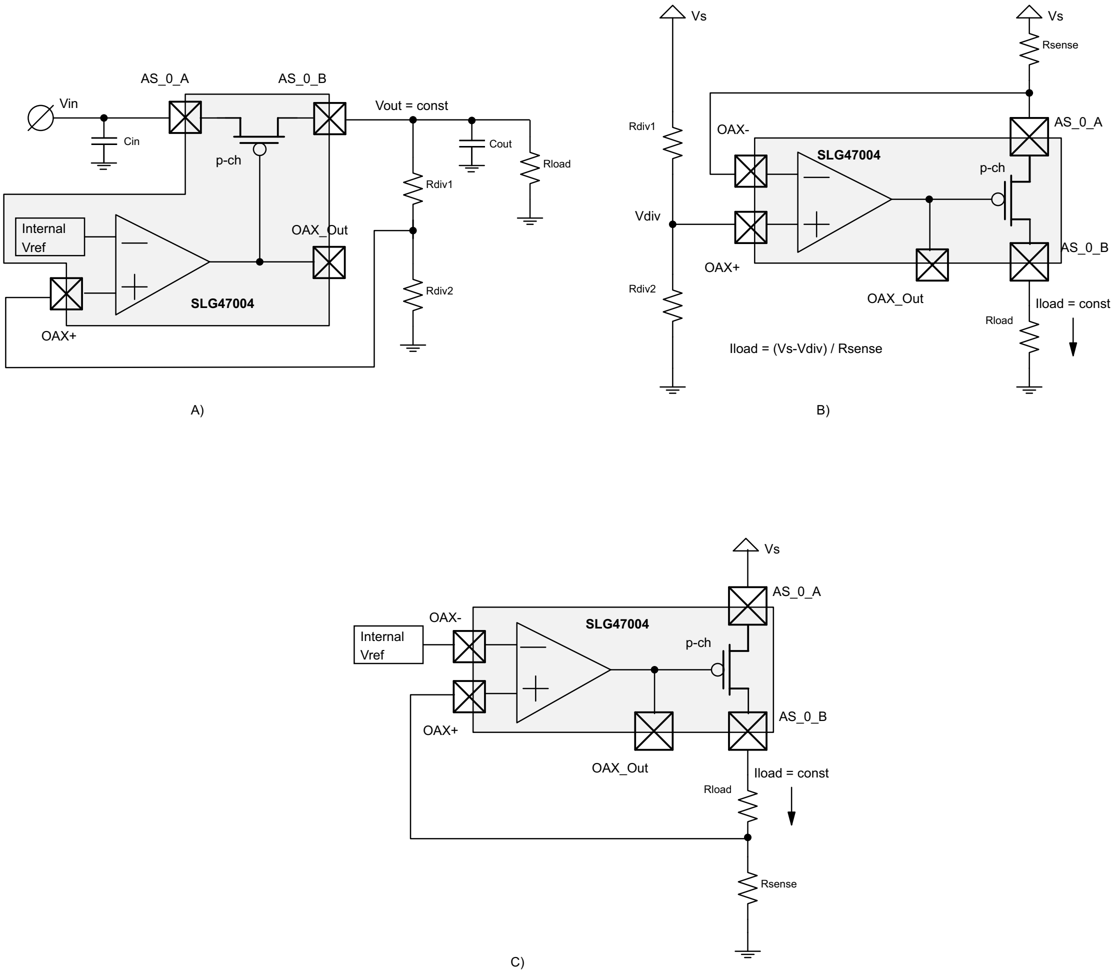


Figure 74. Typical Implementation of Voltage Regulator (A) and Current Sources (B, C)

Note that in this mode only an enhanced P channel FET of An_Sw_0 is used.

10.2.5 Current Sink Mode

Also, the op amp output can drive the N-FET (part of the Analog Switch) in order to implement a constant current sink. Note that FETs of Analog Switches have different resistances. Analog Switch 0 has Rds_PMOS << Rds_NMOS, while Analog Switch 1 has Rds_NMOS << Rds_PMOS. That's why it is recommended to implement current sink mode using Analog Switch 1. In this mode, the op amp output is LOW when the macrocell is turned off. Figure 75 shows a typical implementation of this Current Sink Function. Note that op amp must operate in operational amplifier mode (register 750 = 0 for Op Amp0, register 751 = 0 for Op Amp1).

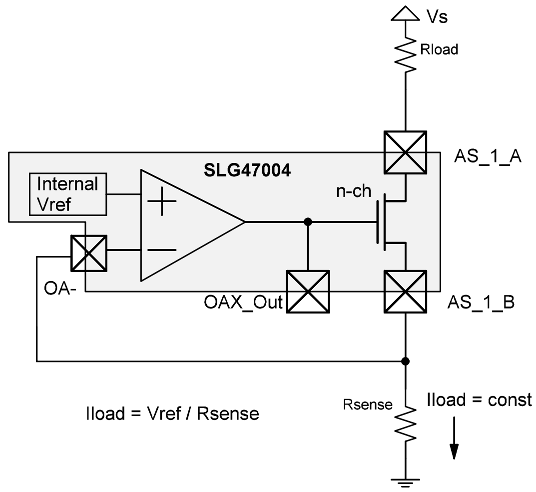


Figure 75. Constant Current Sink

Note that in this mode only an enhanced N channel FET of An_Sw_1 is used.

10.3 Op Amps Typical Performance

T_A = 25 °C, V_{DDA} = 5.0 V, V_{SS} = GND, V_{CM} = $V_{DD}/2$, V_{OUT} = $V_{DD}/2$, V_L = $V_{DD}/2$, R_L = 1 MΩ to V_L, C_L = 80 pF, unless otherwise stated.

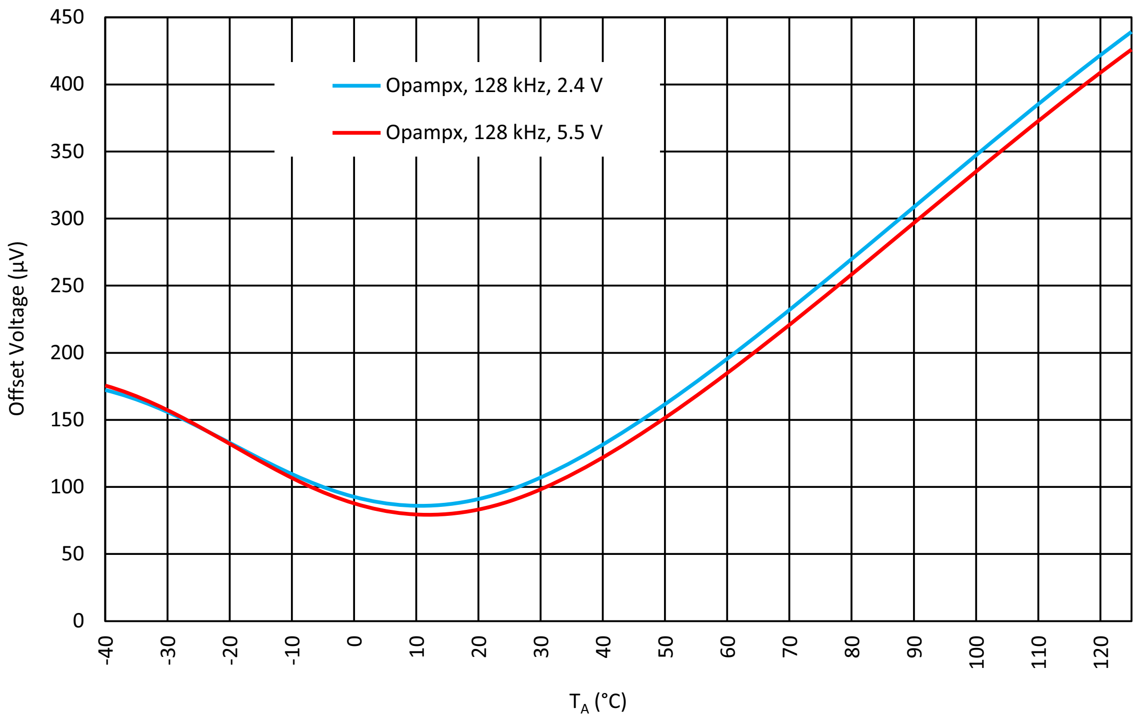


Figure 76. Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 128 kHz

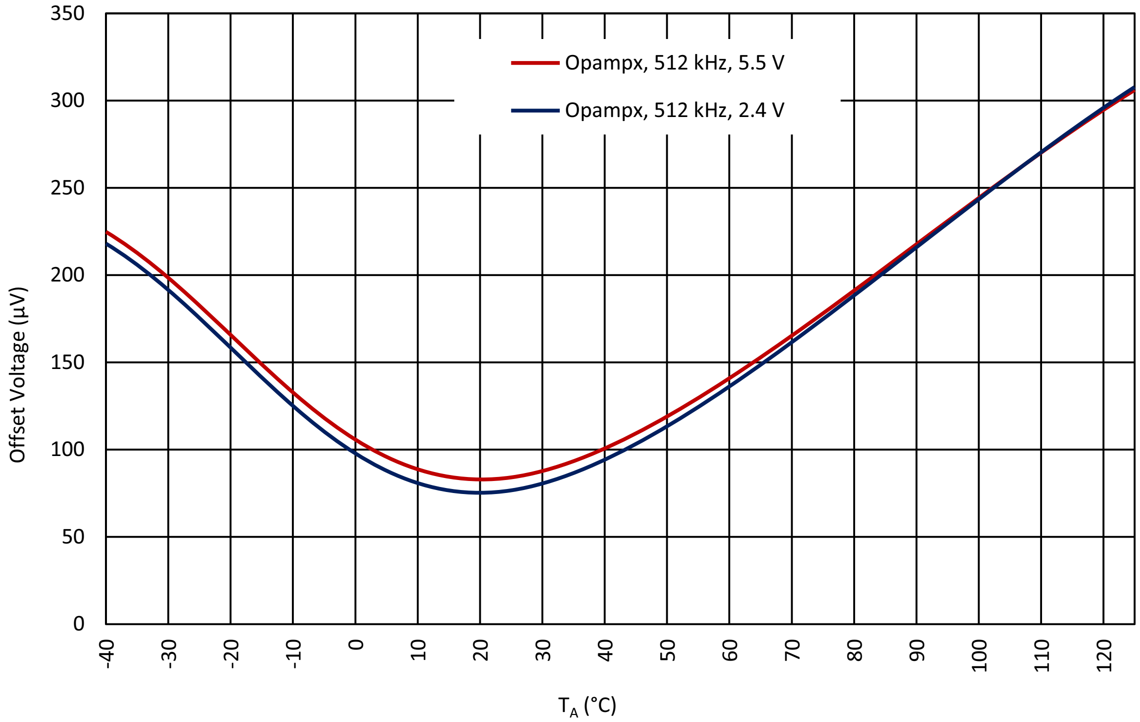


Figure 77. Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 512 kHz

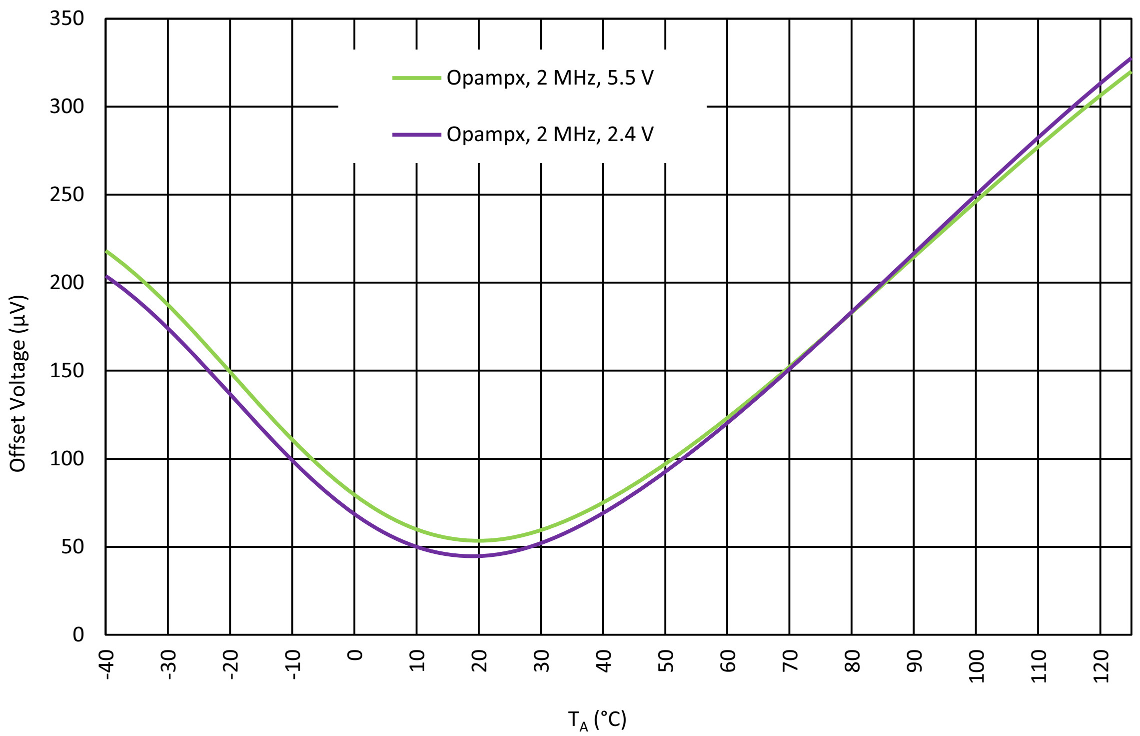


Figure 78. Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 2 MHz

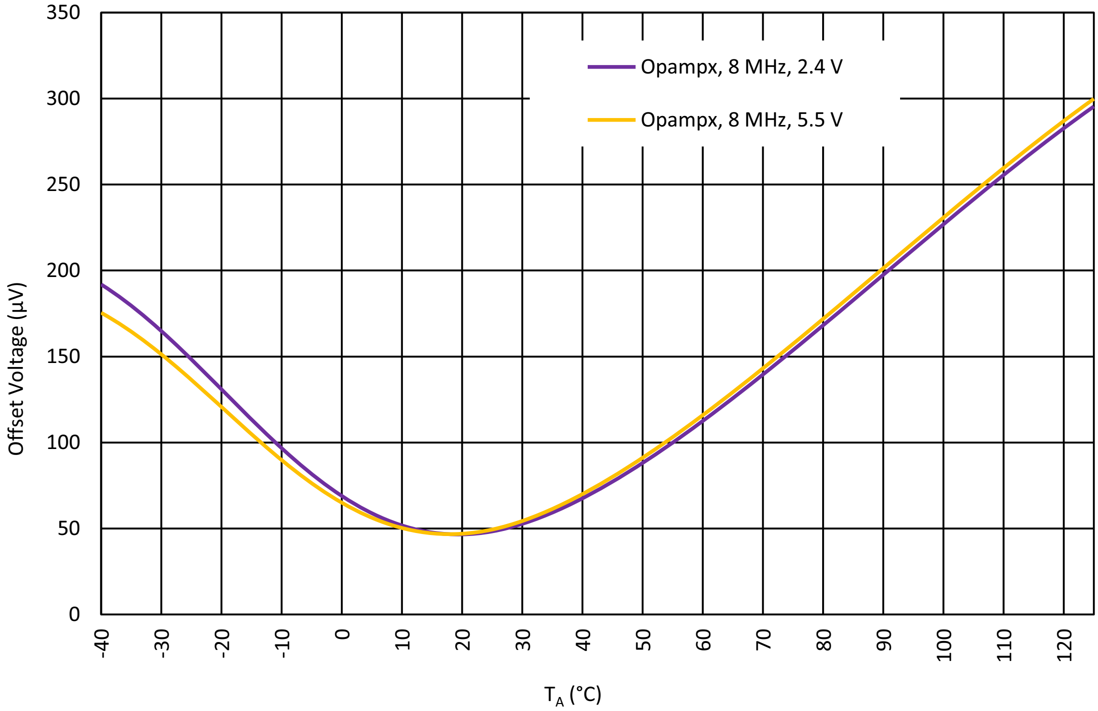


Figure 79. Op Ampx Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 8 MHz

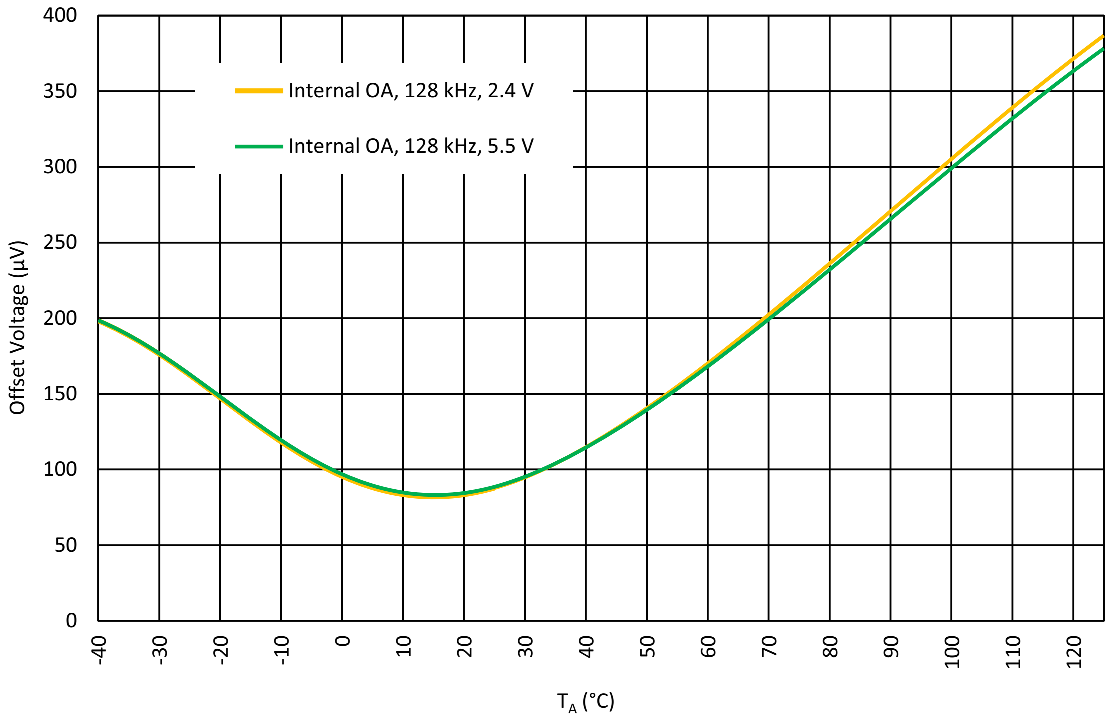


Figure 80. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = $V_{DD}/2$, BW = 128 kHz

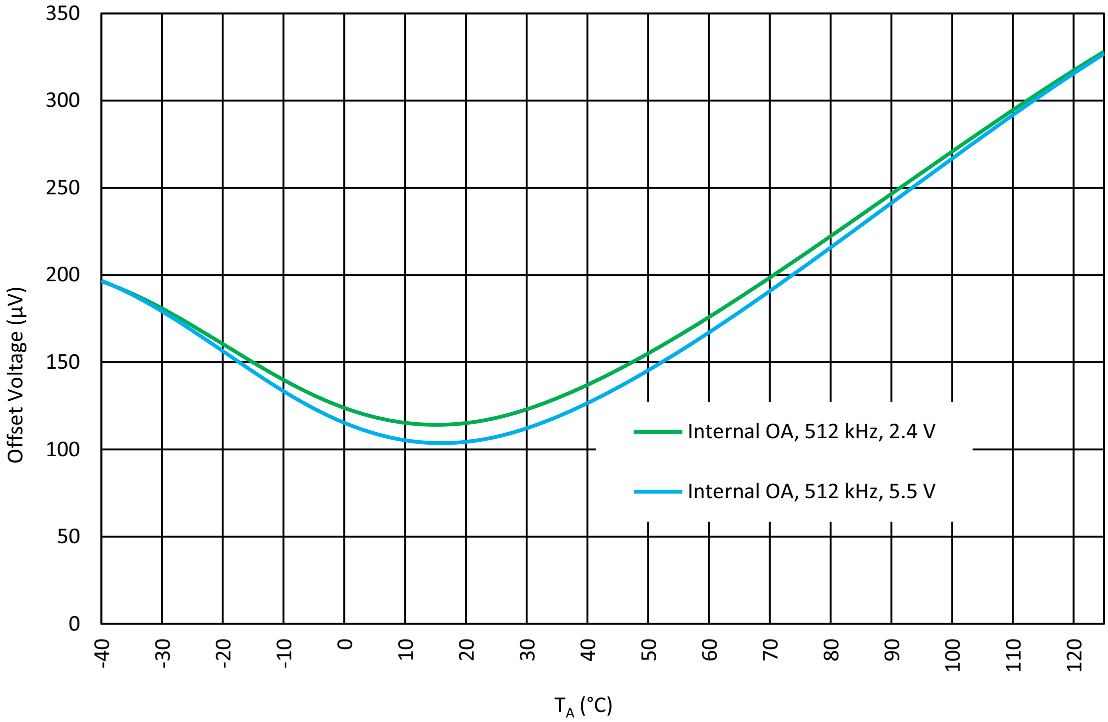


Figure 81. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 512 kHz

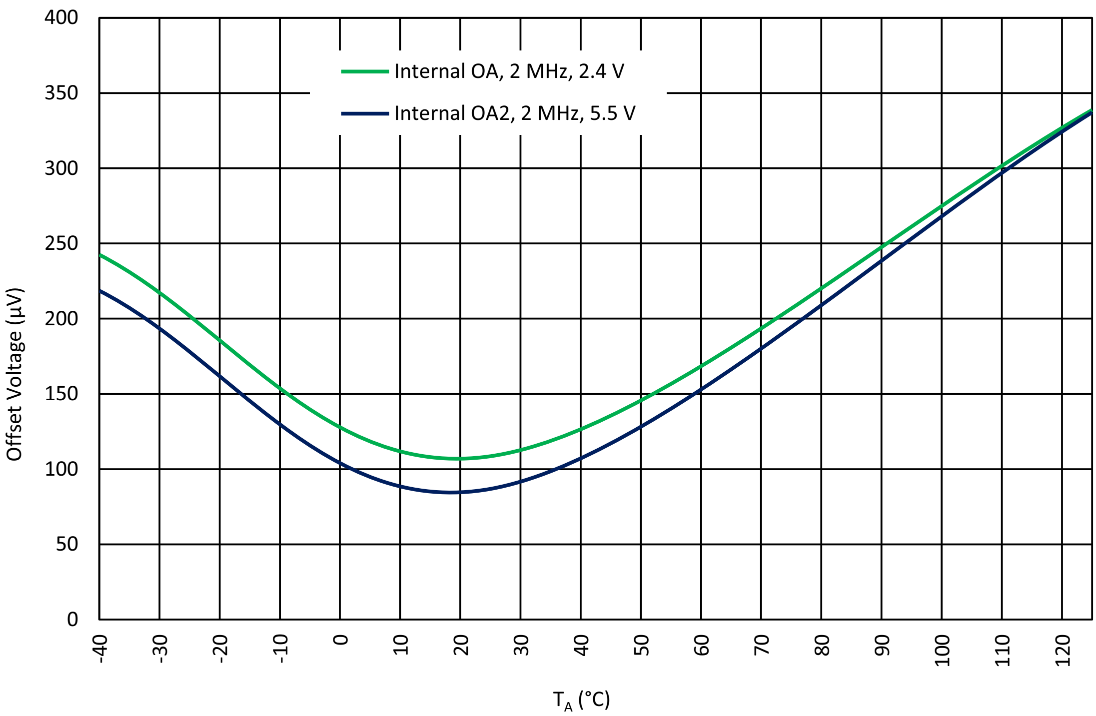


Figure 82. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 2 MHz

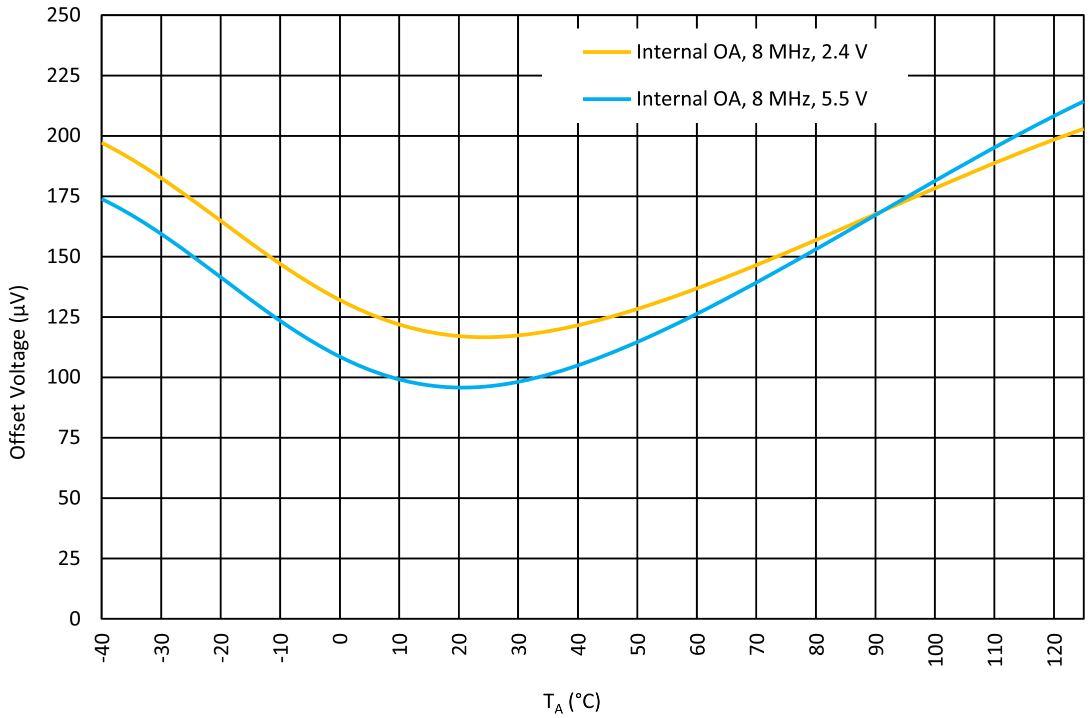


Figure 83. Internal Op Amp Input Offset Voltage vs. T_A at Input CM Voltage = V_{DD}/2, BW = 8 MHz

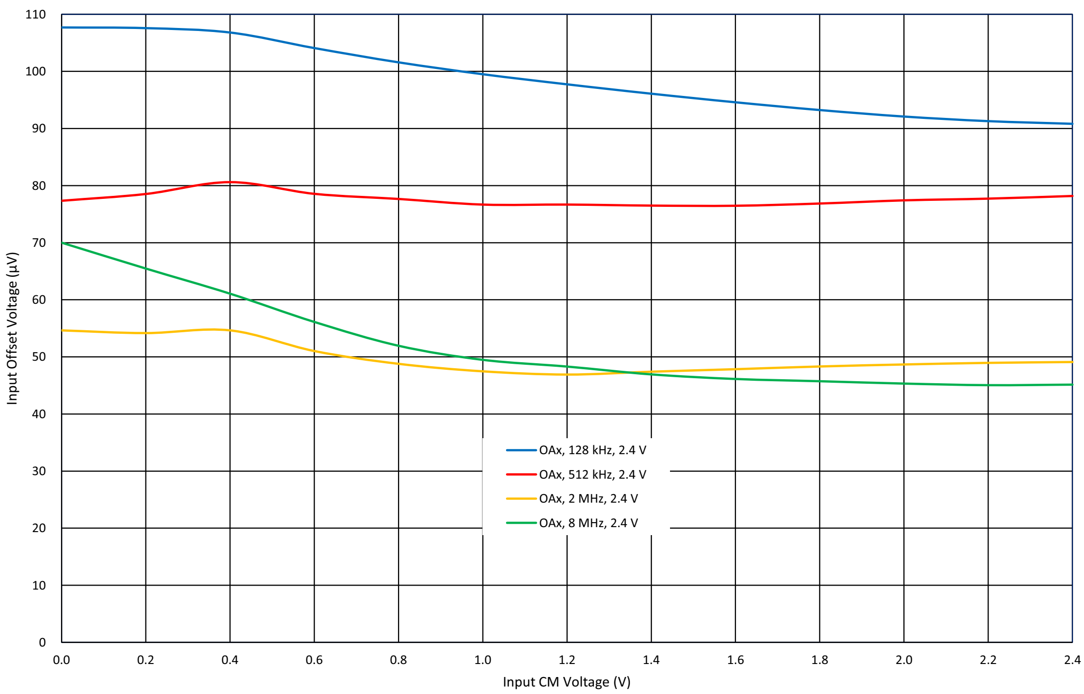


Figure 84. OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 2.4 V

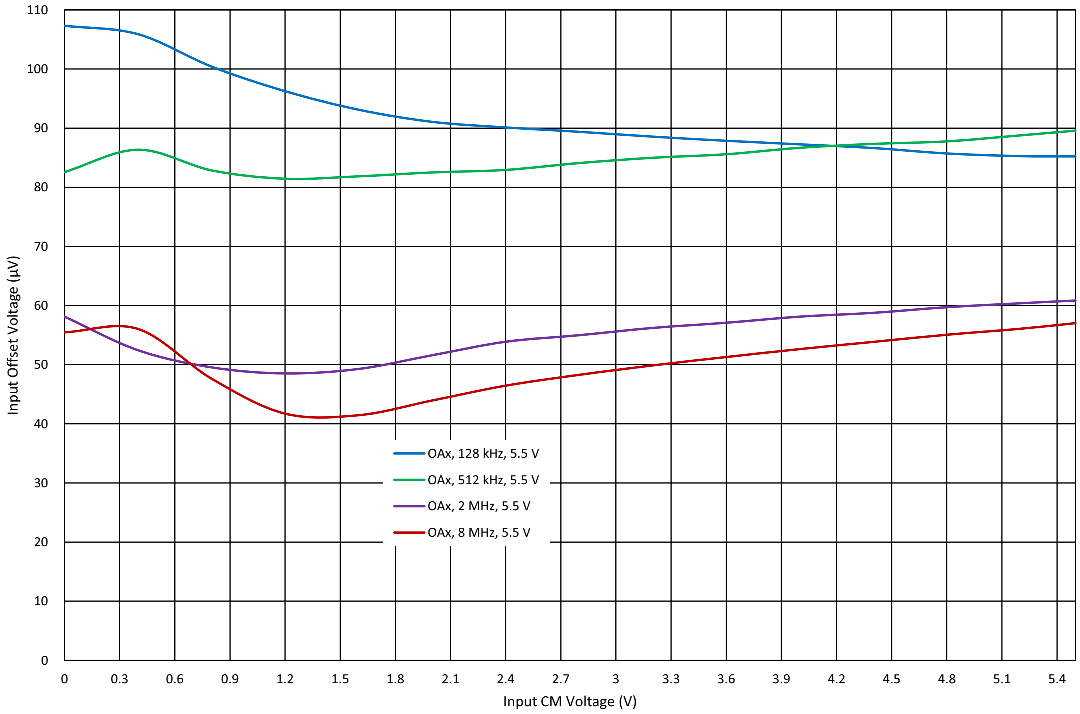


Figure 85. OpAmp0, 1 Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 5.5 V

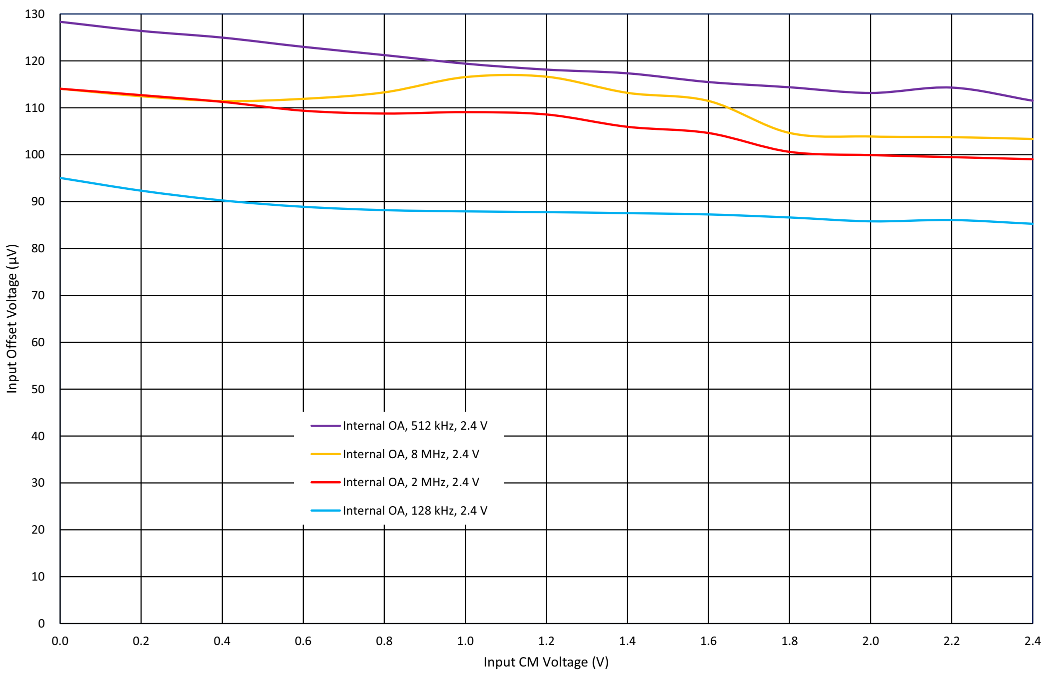


Figure 86. Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 2.4 V

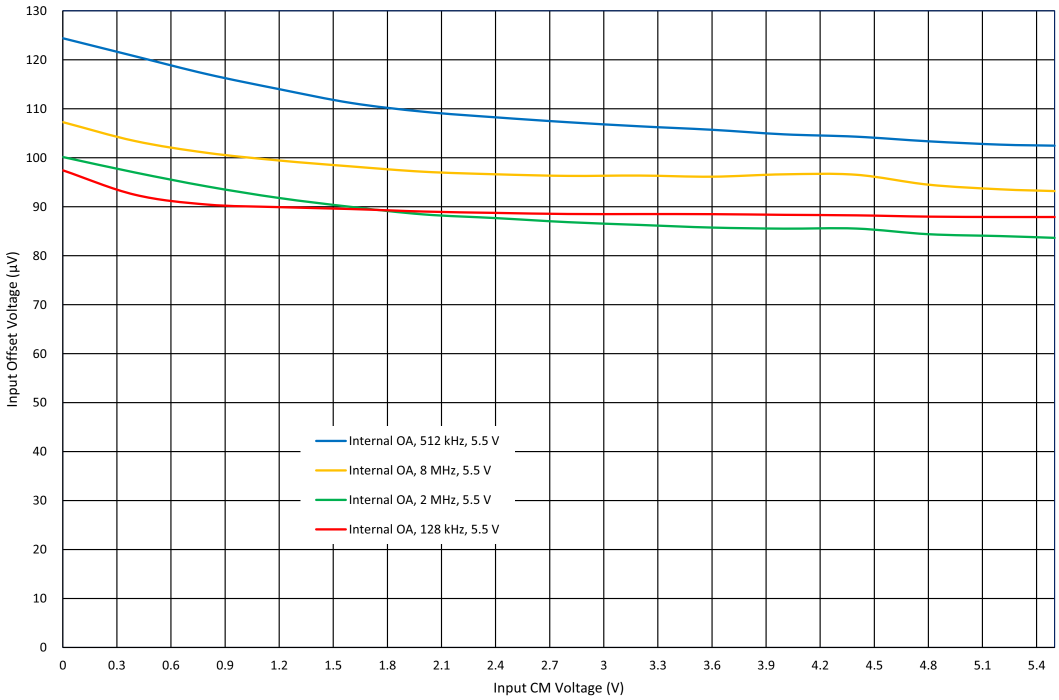


Figure 87. Internal OpAmp Input Offset Voltage vs. Input CM Voltage at T_A = 25 °C, V_{DDA} = 5.5 V

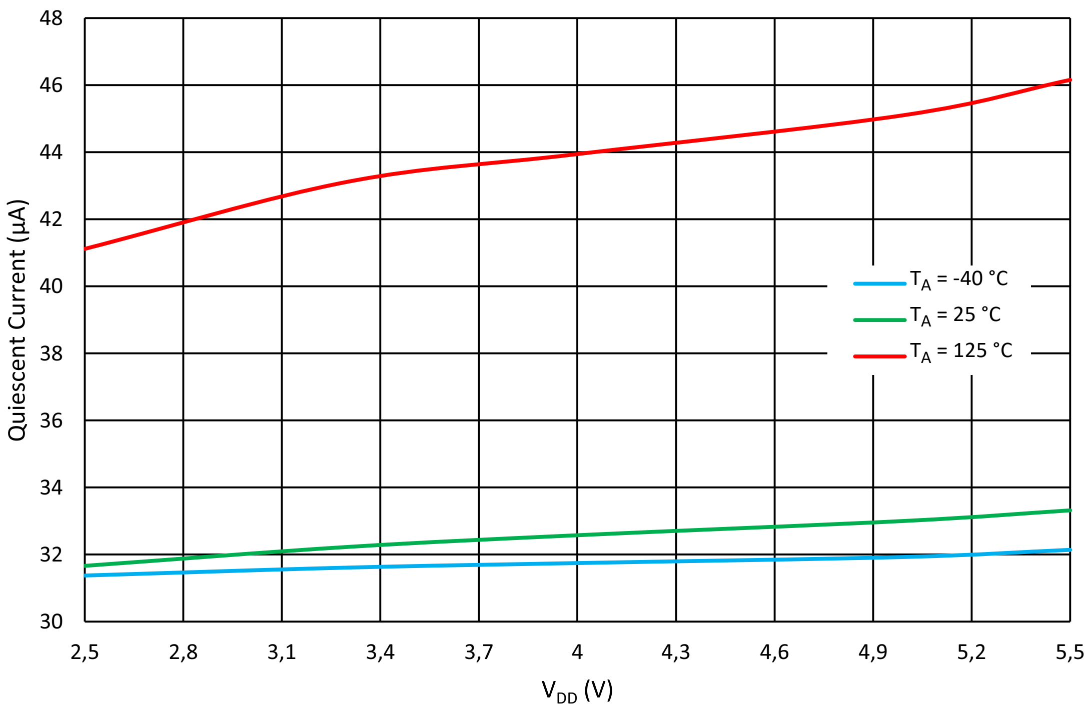


Figure 88. Quiescent Current vs. Power Supply Voltage for BW = 128 kHz

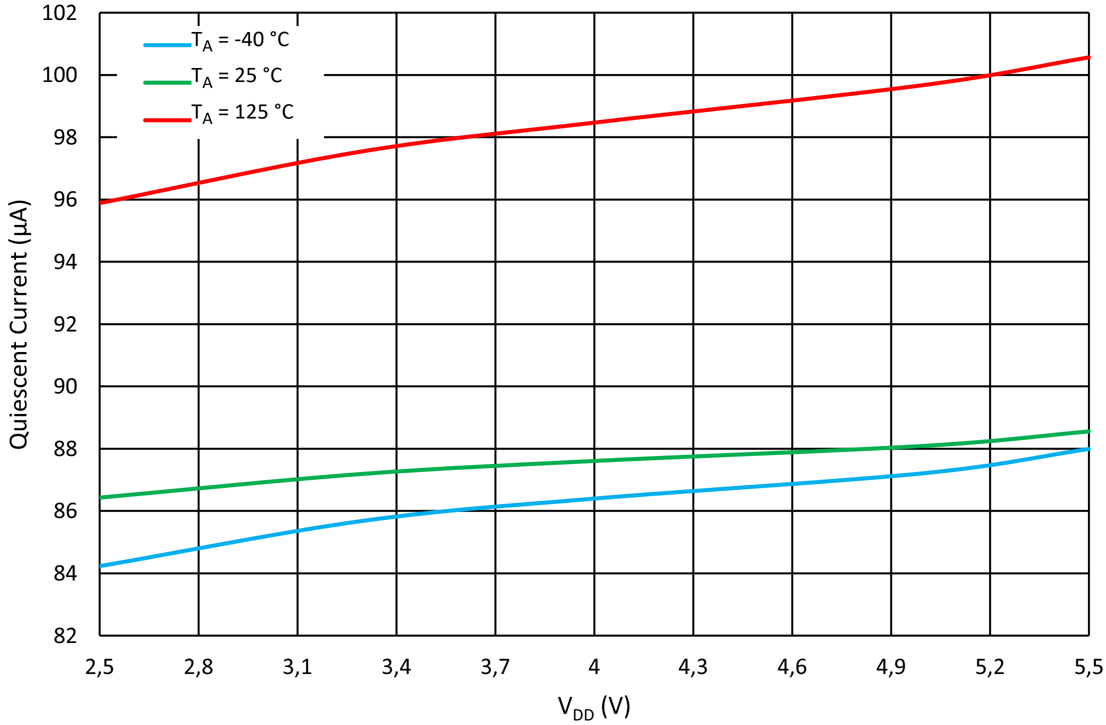


Figure 89. Quiescent Current vs. Power Supply Voltage for BW = 512 kHz

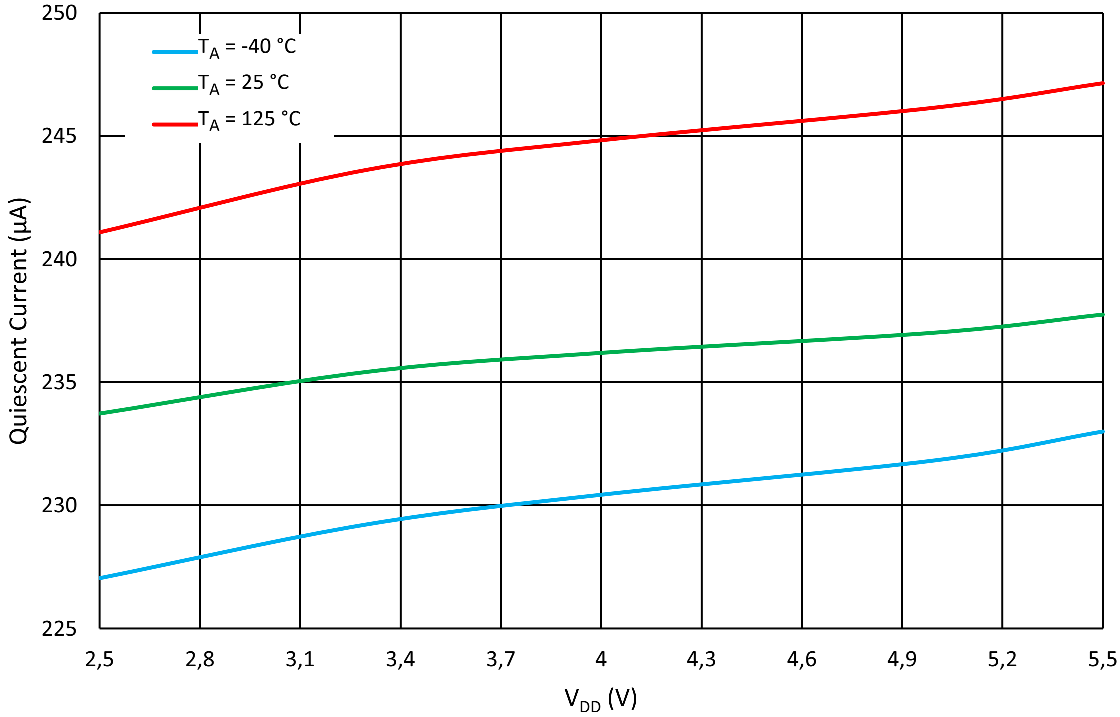


Figure 90. Quiescent Current vs. Power Supply Voltage for BW = 2 MHz

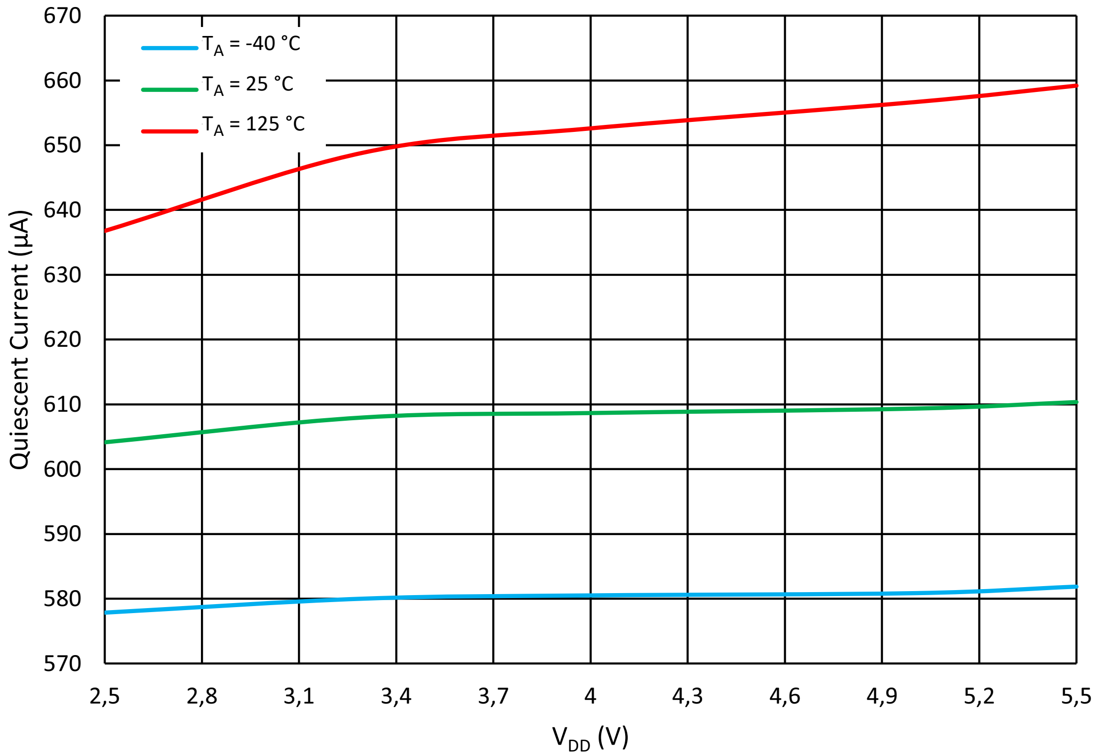


Figure 91. Quiescent Current vs. Power Supply Voltage for BW = 8 MHz

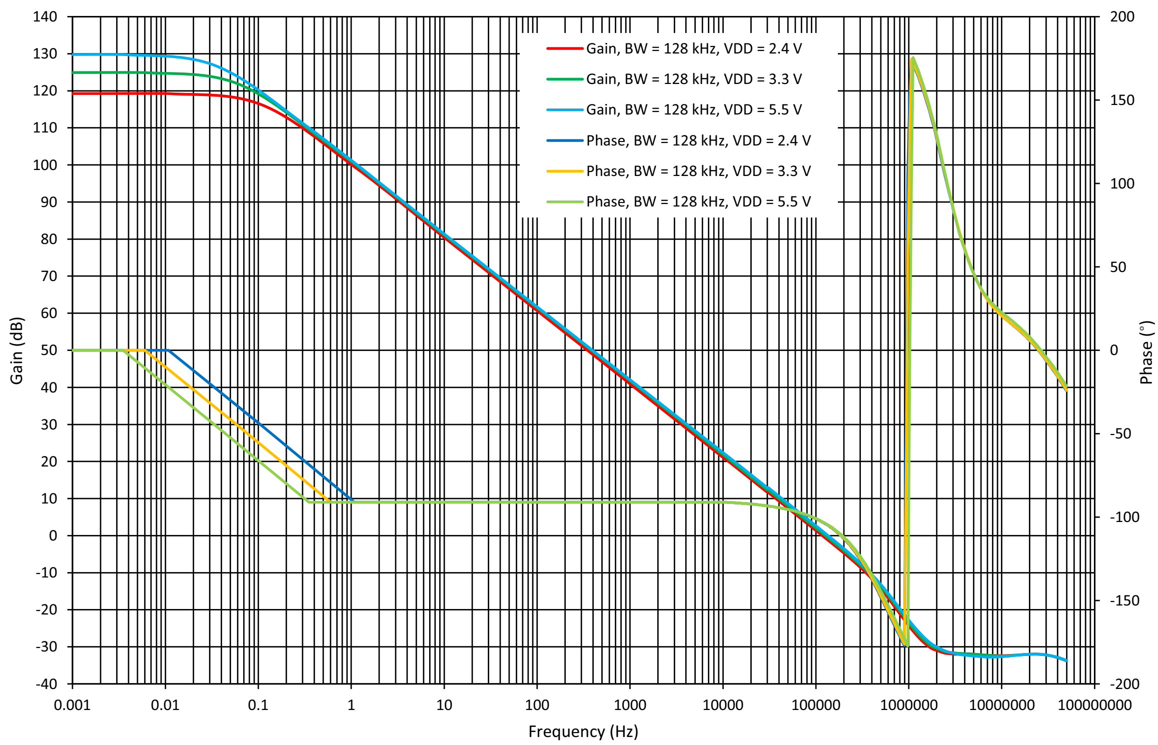


Figure 92. OA0 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

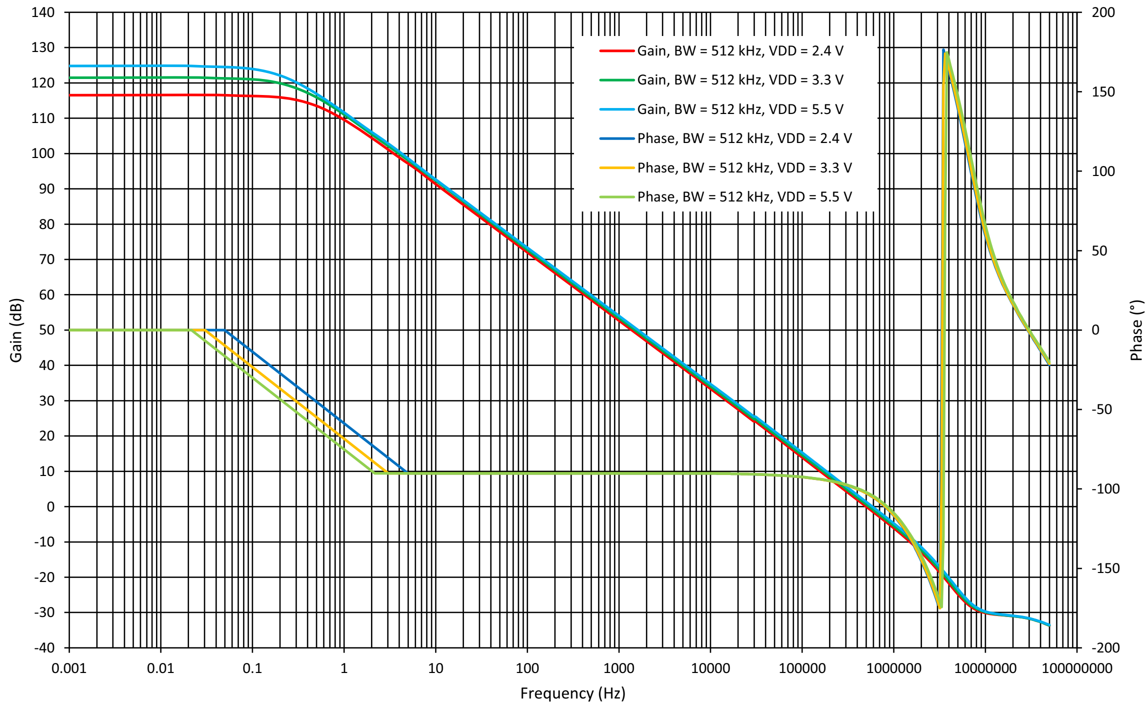


Figure 93. OA0 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

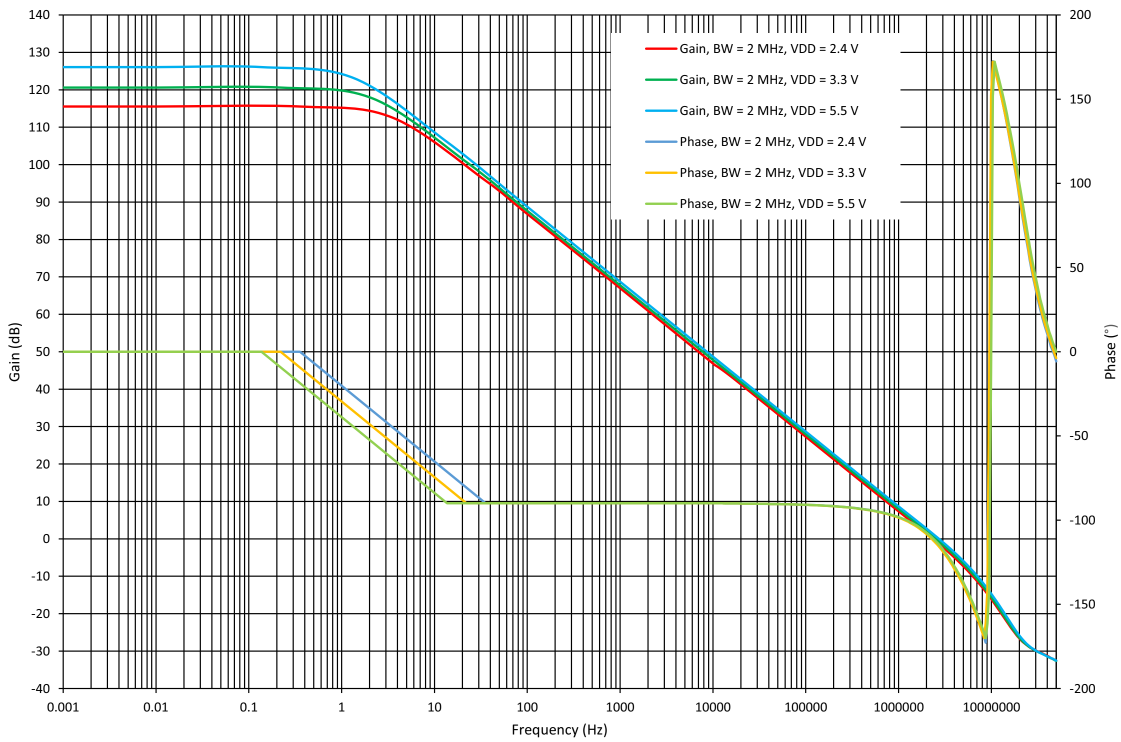


Figure 94. OA0 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

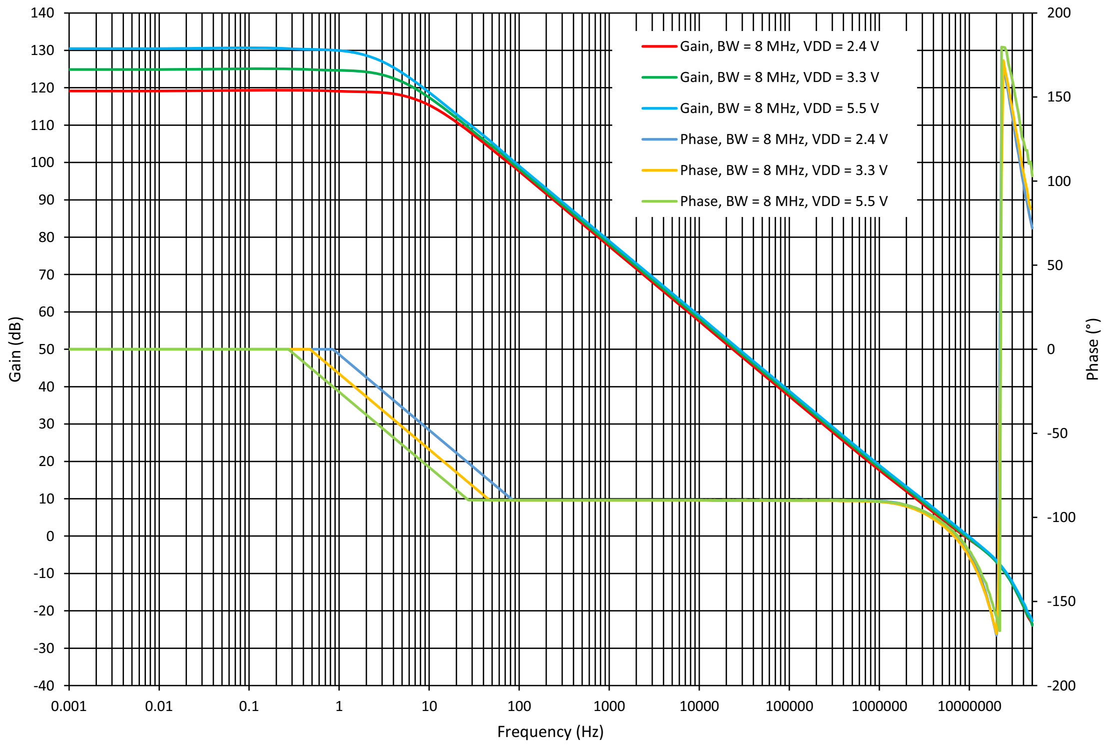


Figure 95. OA0 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

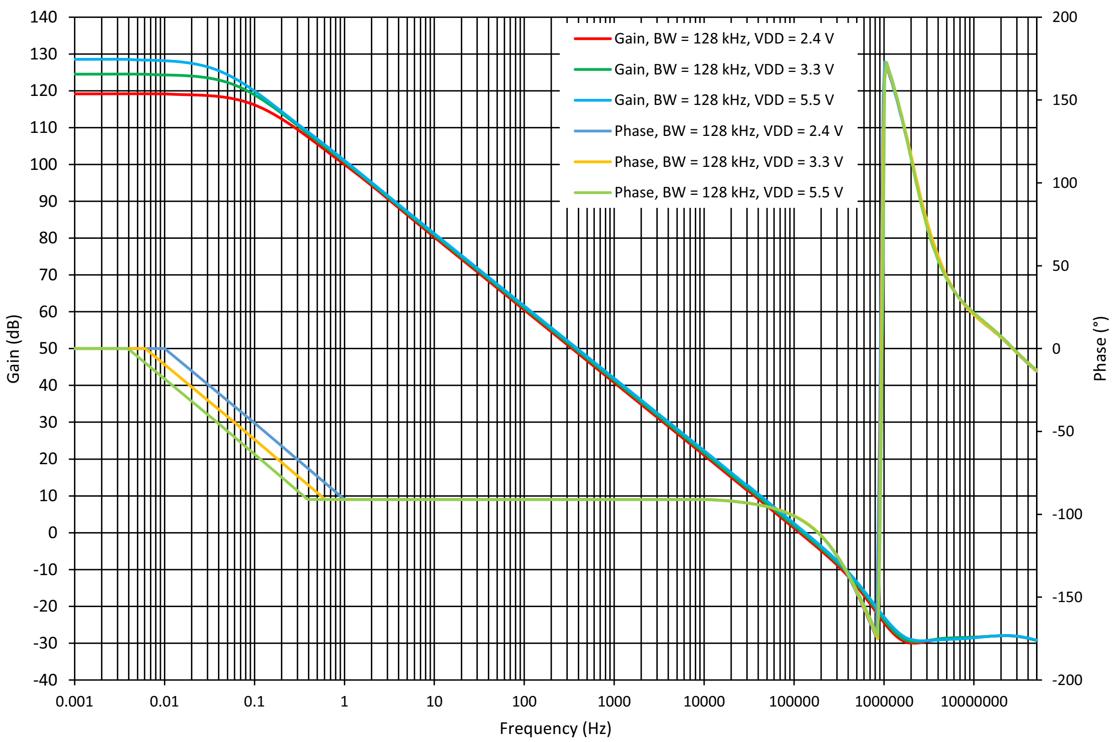


Figure 96. OA1 Open Loop Gain and Phase vs. Frequency for BW = 128 kHz

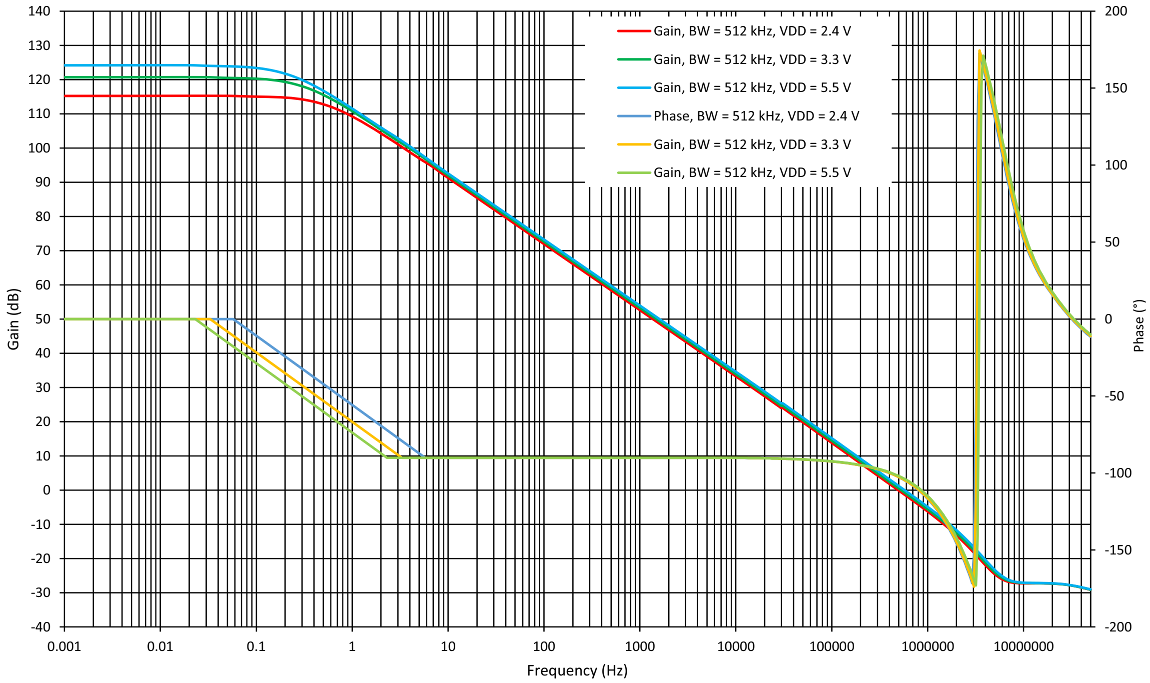


Figure 97. OA1 Open Loop Gain and Phase vs. Frequency for BW = 512 kHz

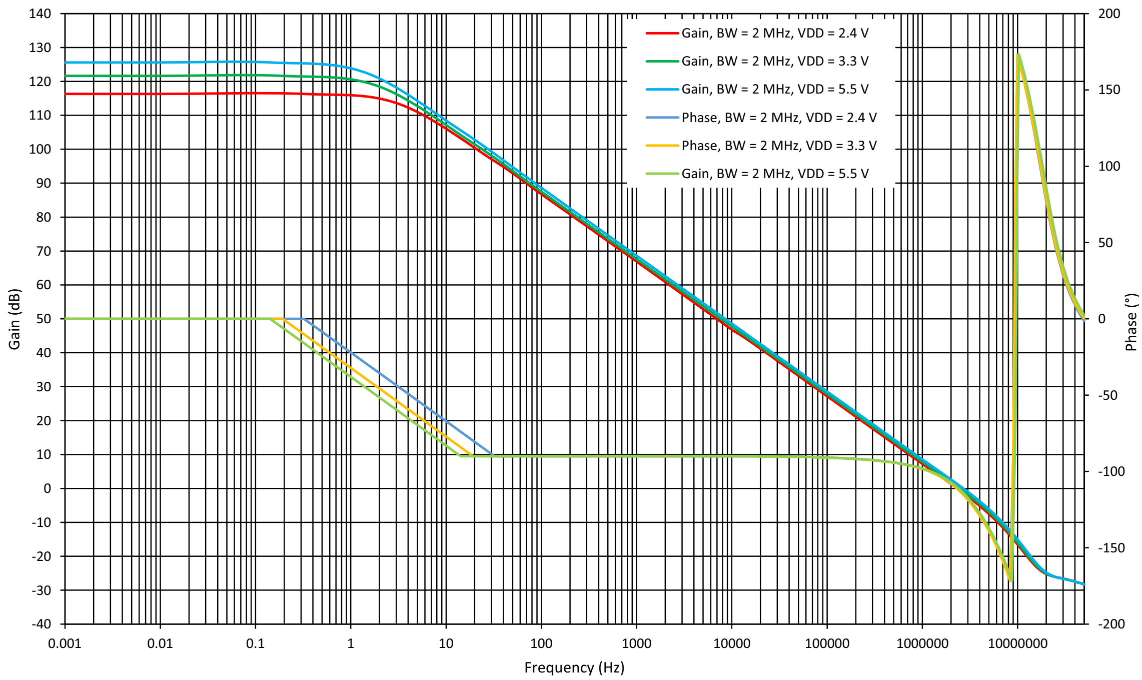


Figure 98. OA1 Open Loop Gain and Phase vs. Frequency for BW = 2 MHz

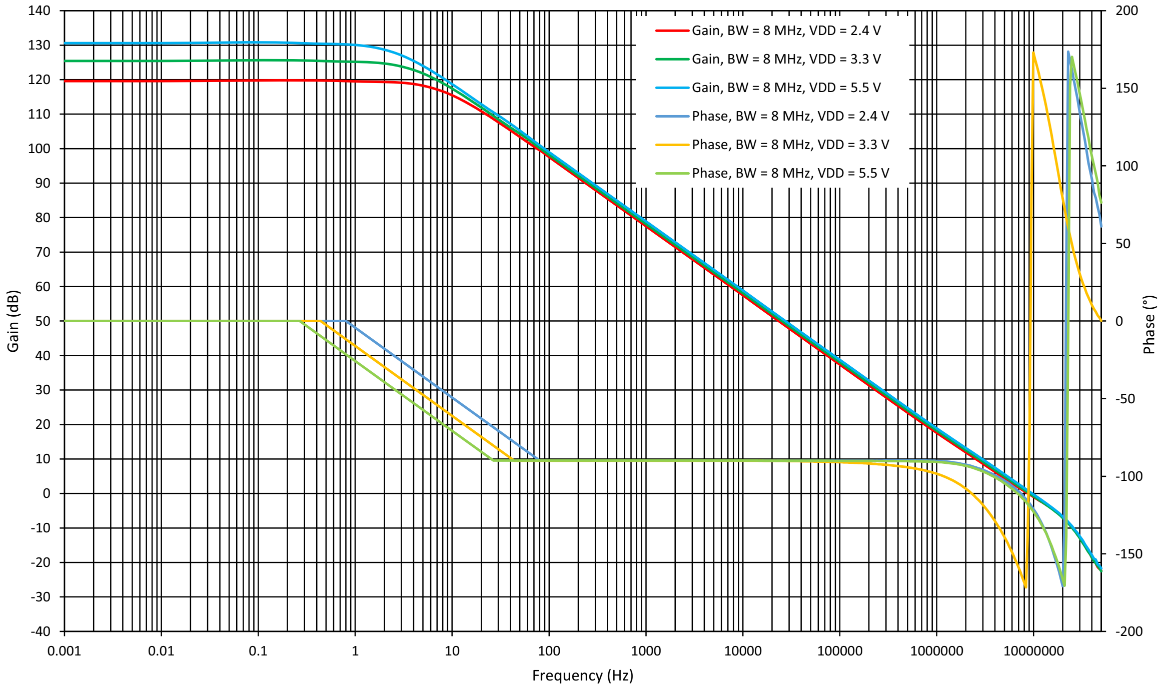


Figure 99. OA1 Open Loop Gain and Phase vs. Frequency for BW = 8 MHz

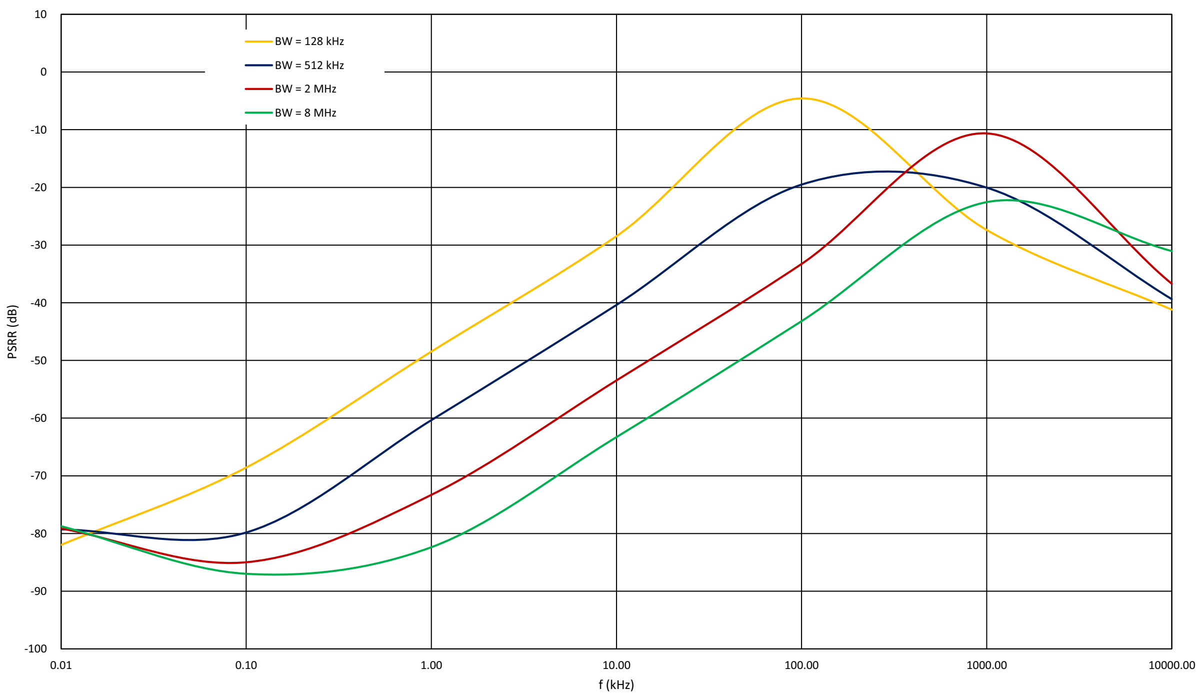


Figure 100. PSRR vs. Frequency V_{DD} = 2.4 V to 5.5 V

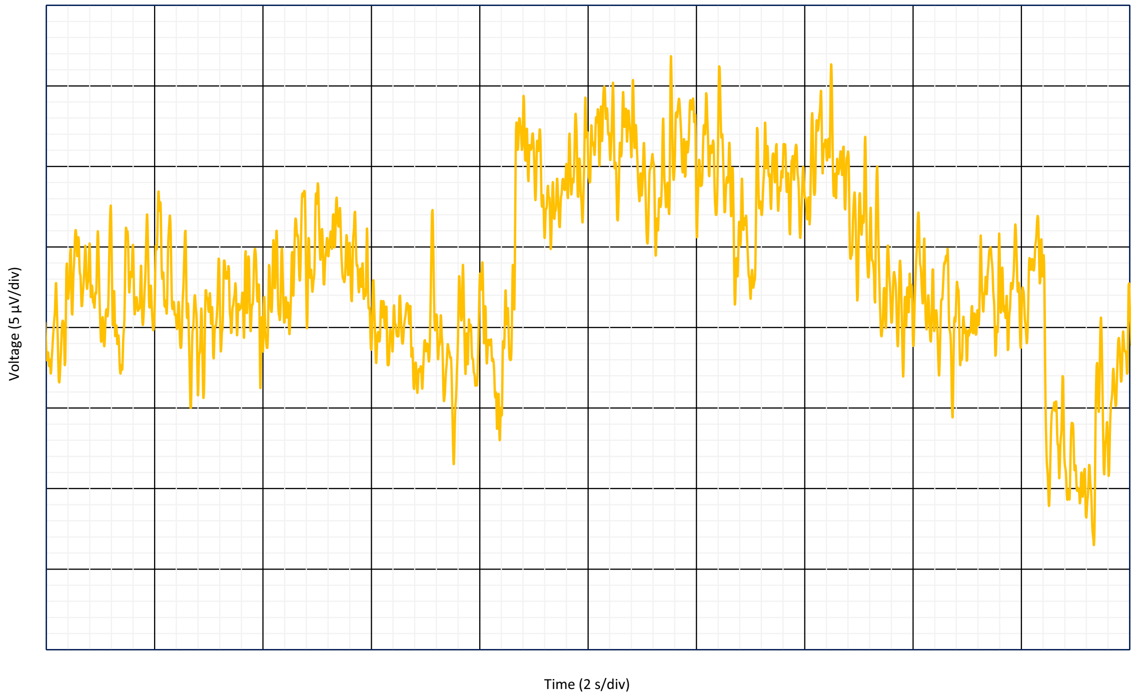


Figure 101. 0.1 Hz to 10 Hz Noise, BW = 128 kHz

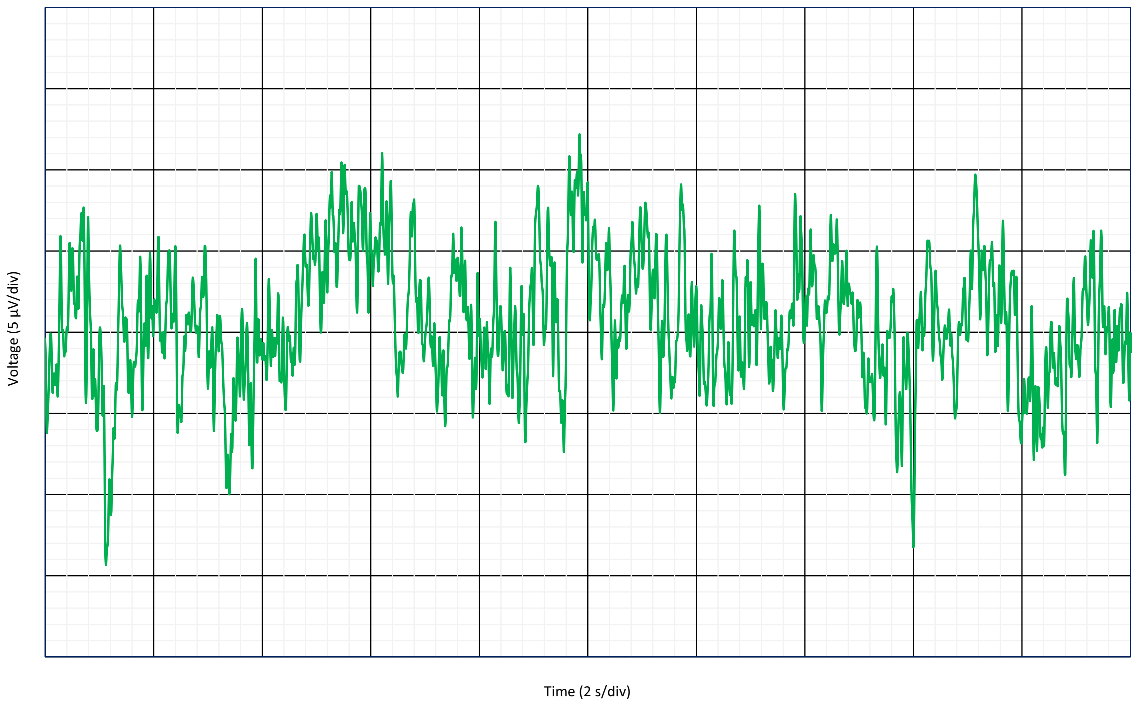


Figure 102. 0.1 Hz to 10 Hz Noise, BW = 512 kHz

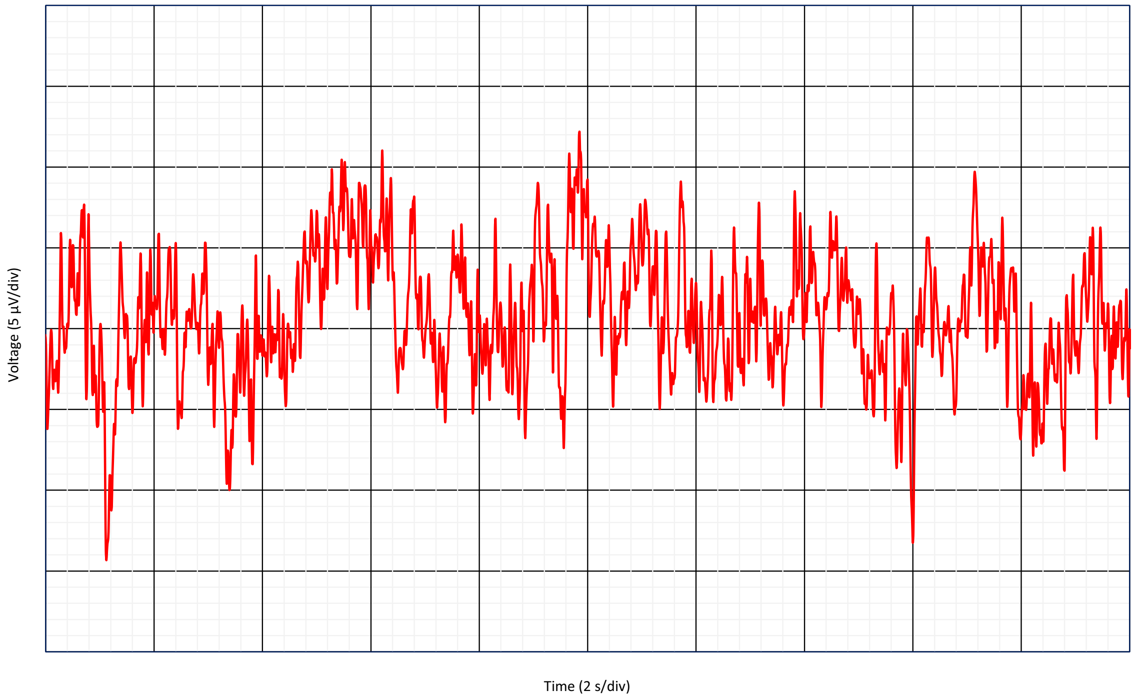


Figure 103. 0.1 Hz to 10 Hz Noise, BW = 2 MHz

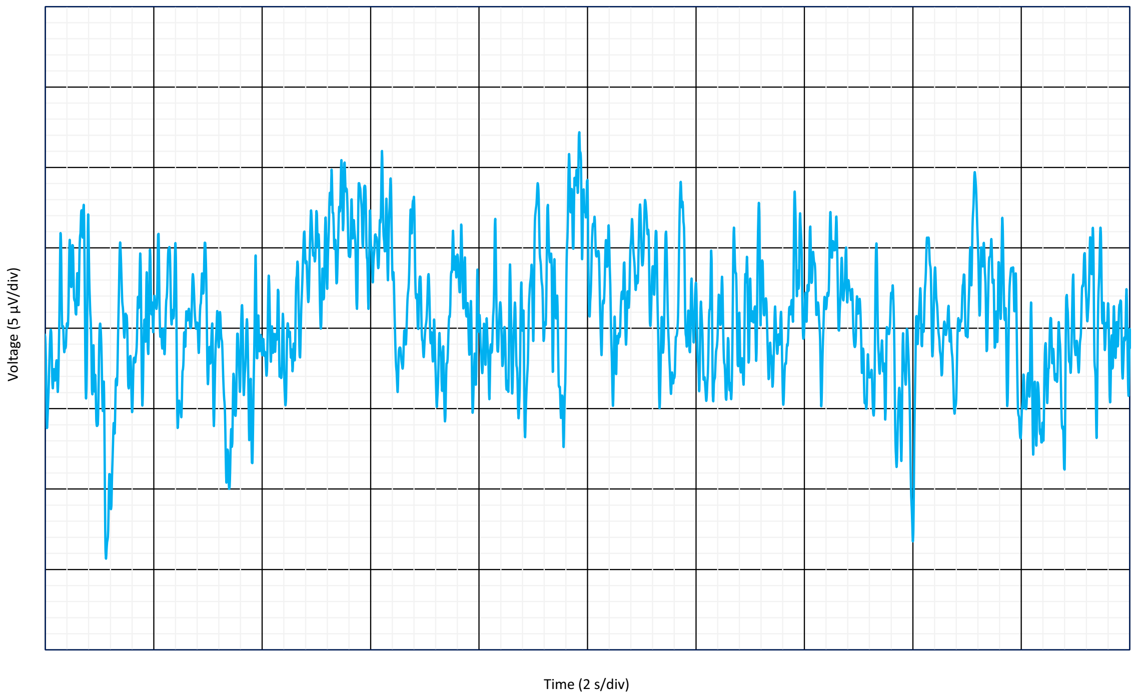


Figure 104. 0.1 Hz to 10 Hz Noise, BW = 8 MHz

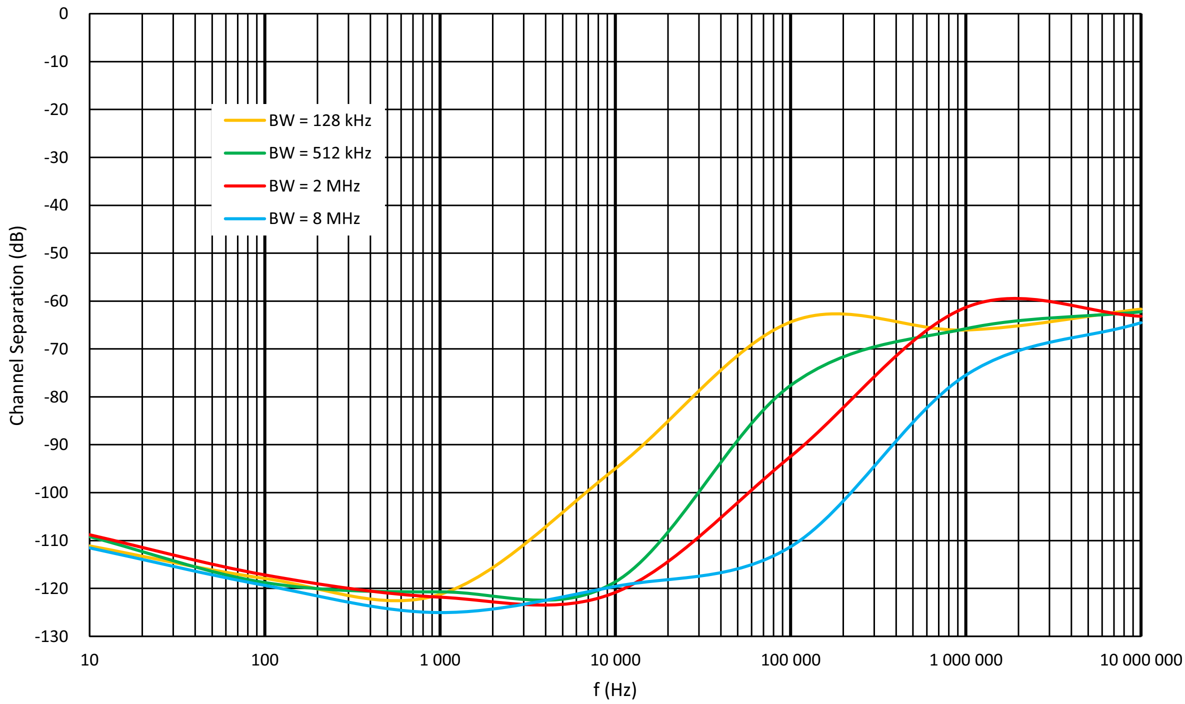


Figure 105. Channel Separation vs. Frequency

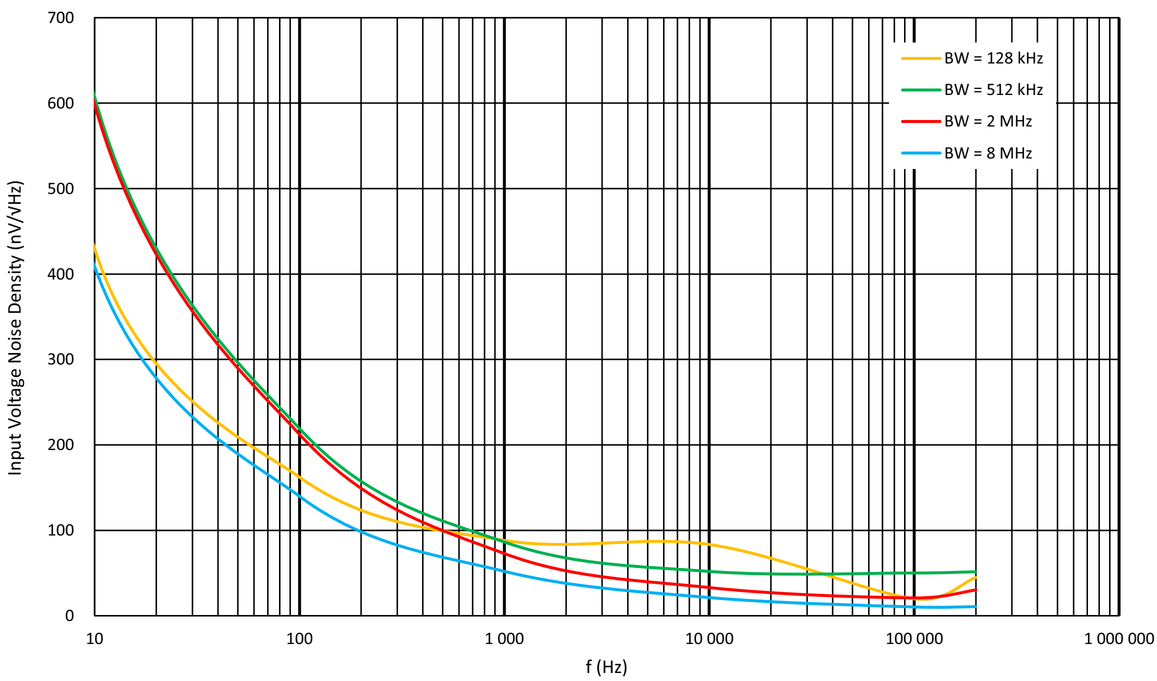


Figure 106. Op Ampx Noise Voltage Density vs. Frequency

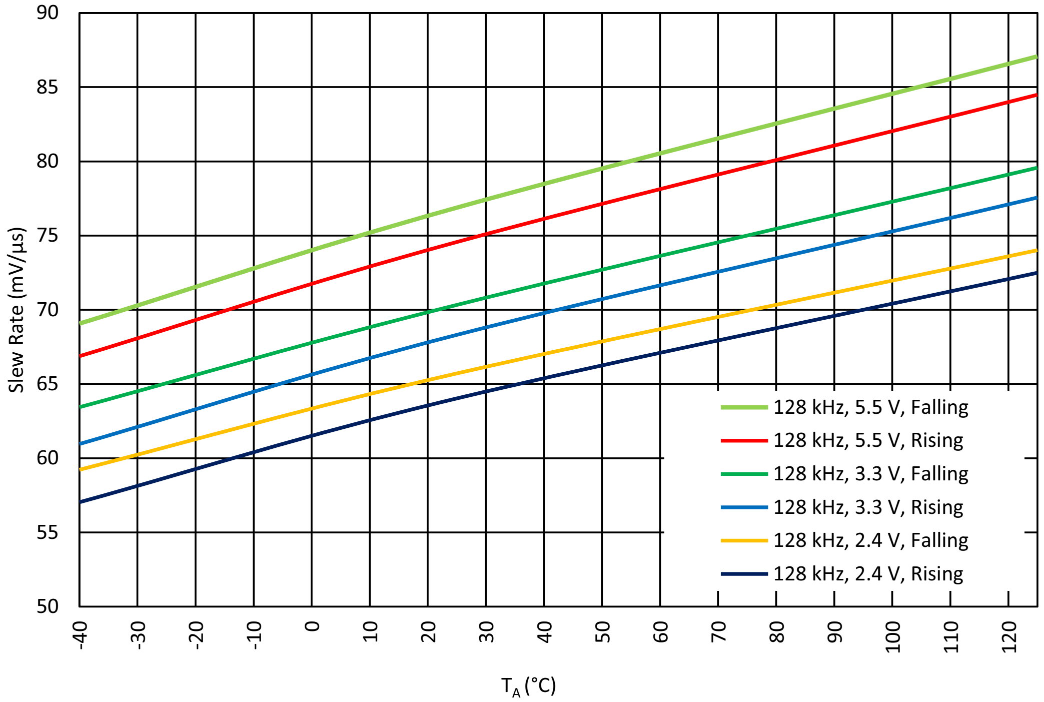


Figure 107. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 128 kHz

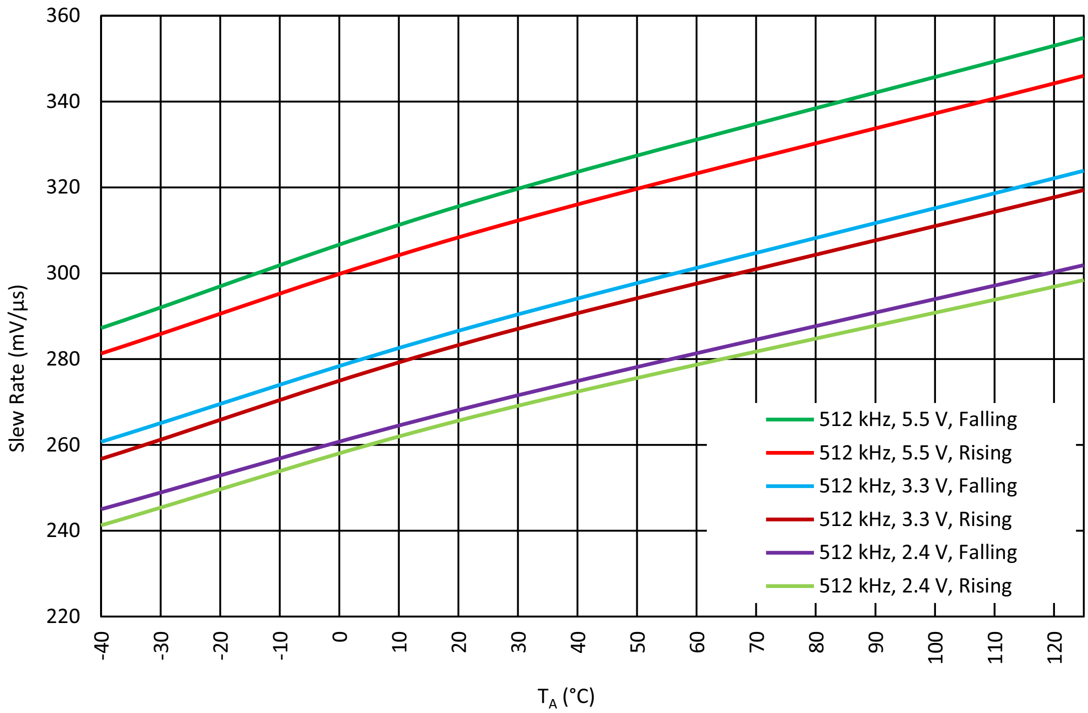


Figure 108. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 512 kHz

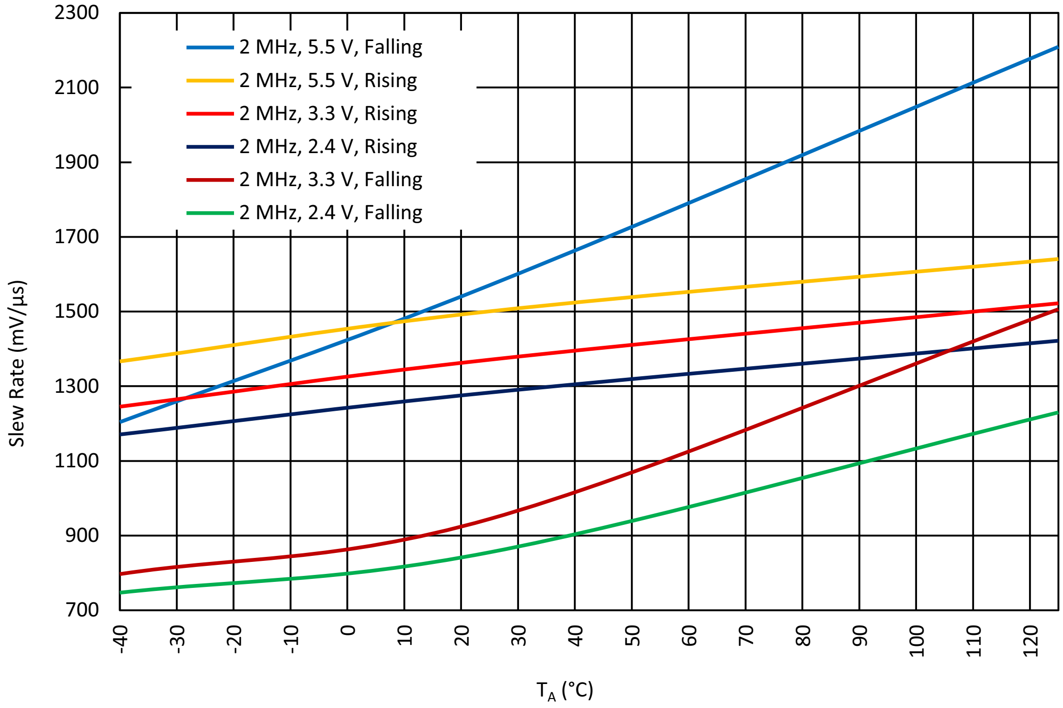


Figure 109. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 2 MHz

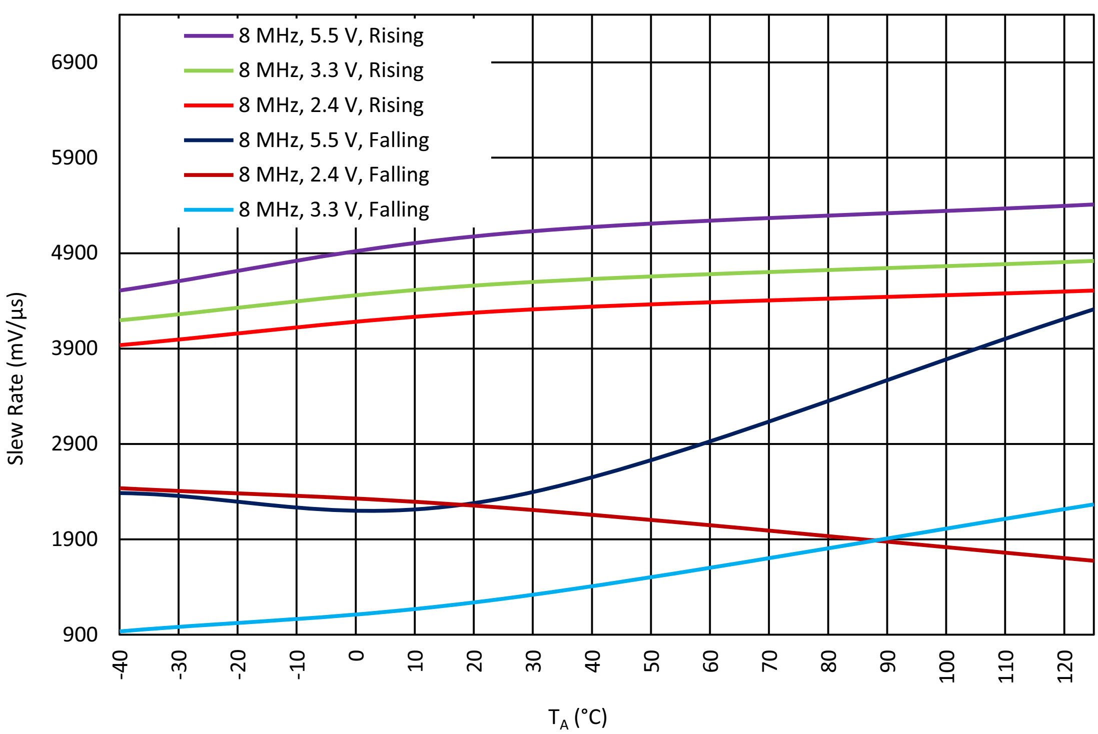


Figure 110. Slew Rate vs. Ambient Temperature G = 1 V/V; R_L = 50 kΩ for BW = 8 MHz

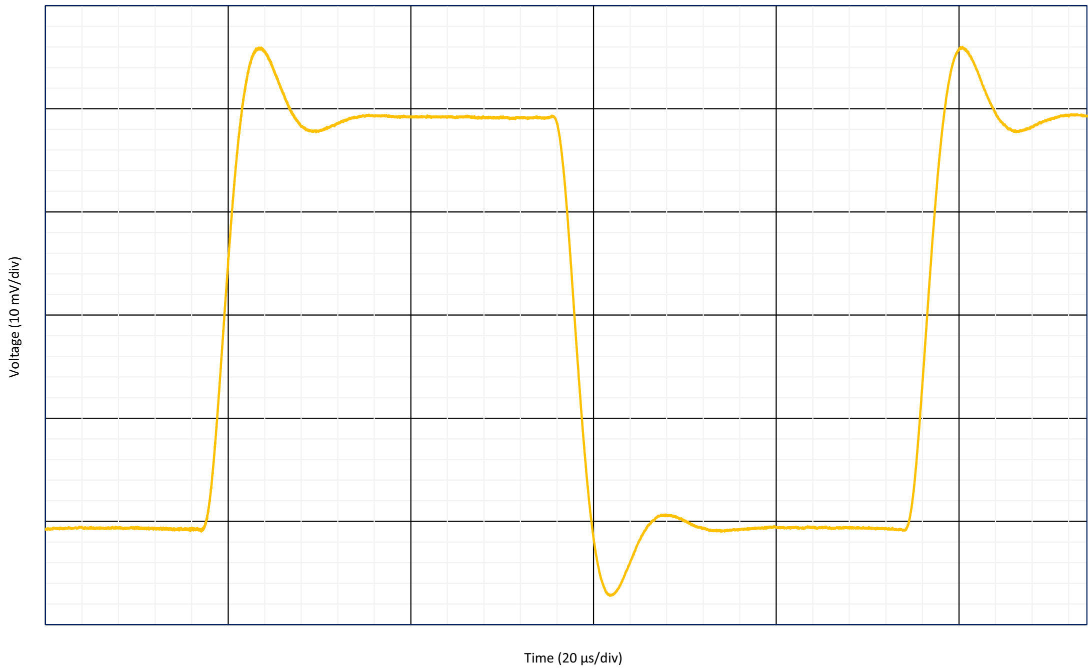


Figure 111. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

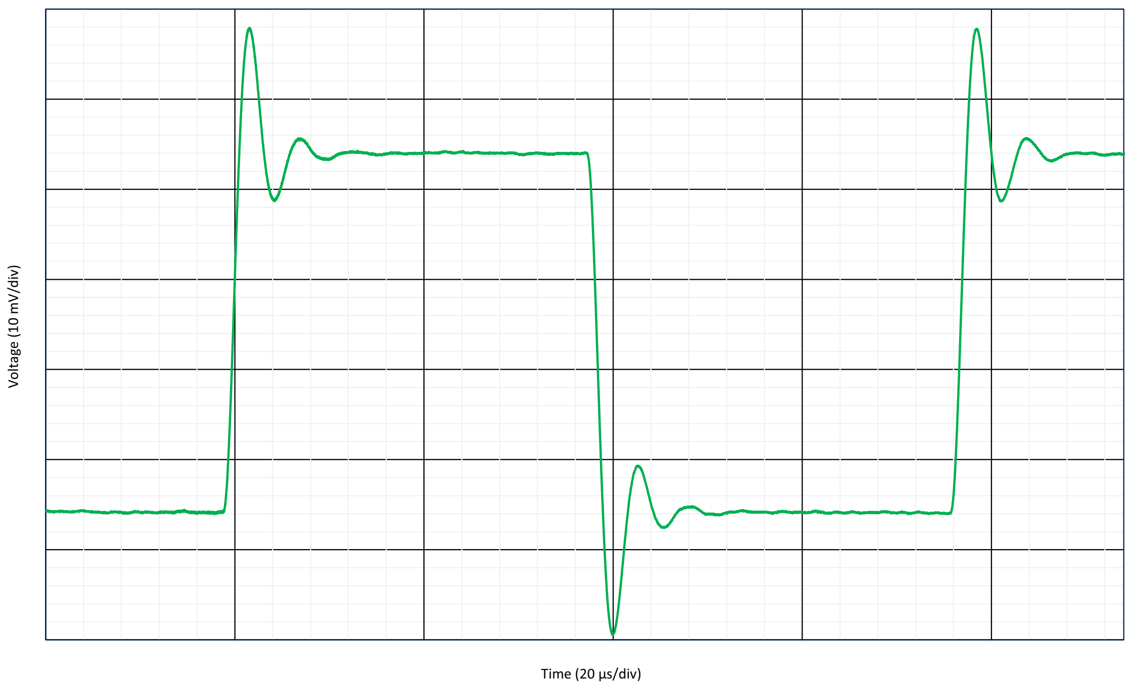


Figure 112. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

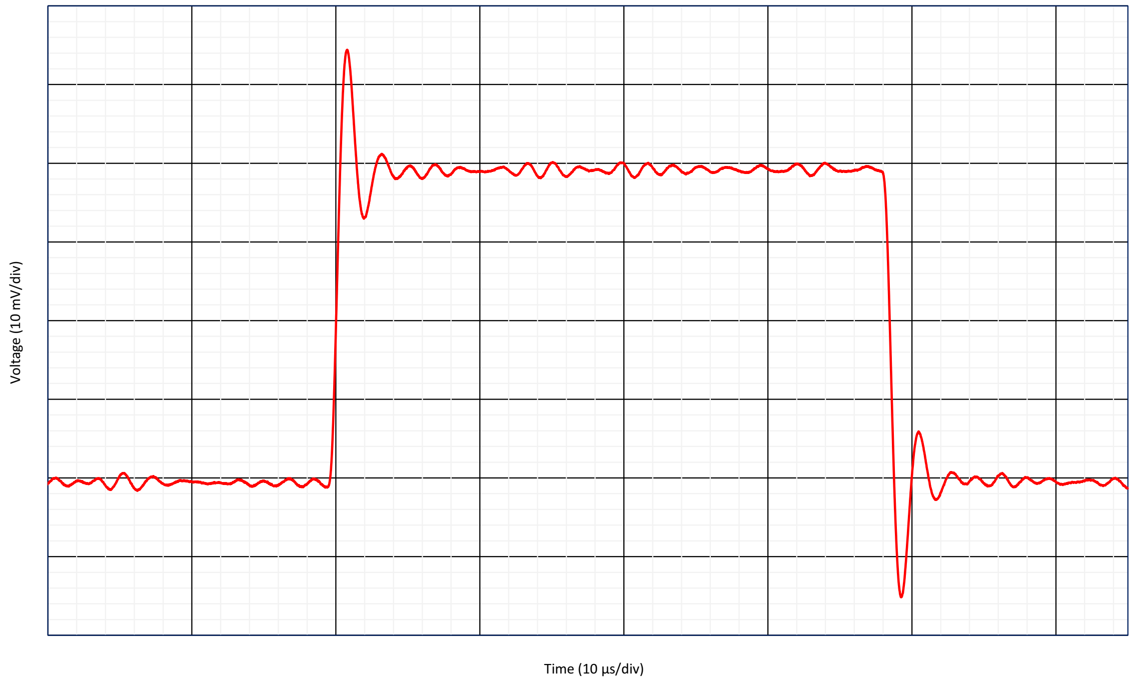


Figure 113. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

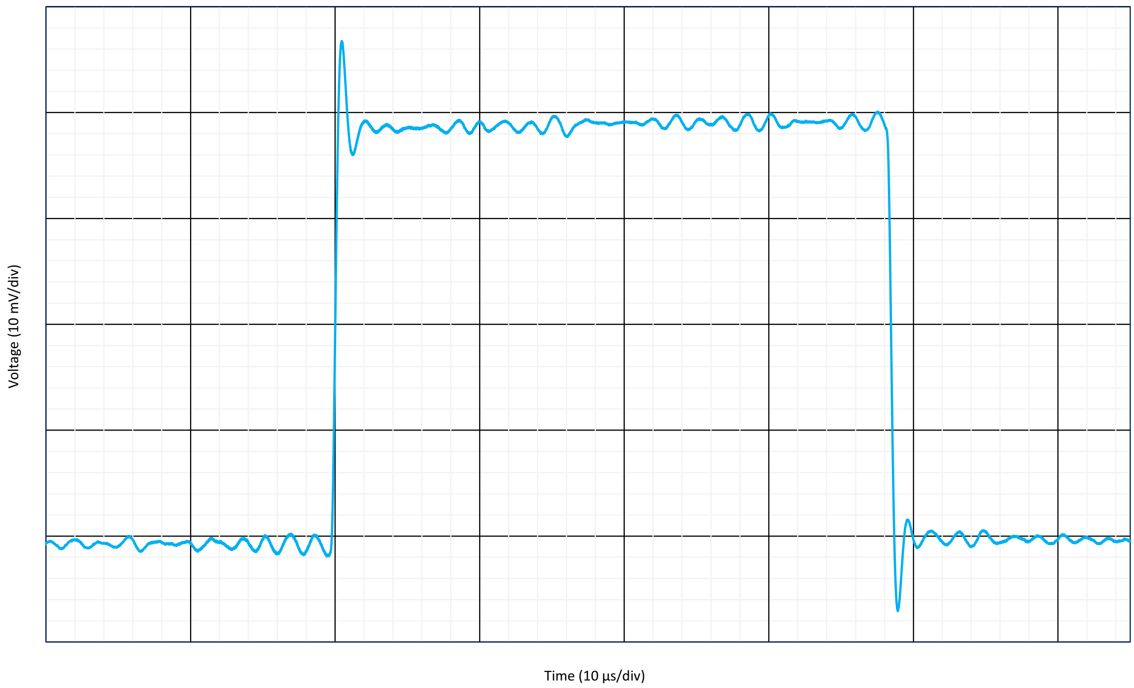


Figure 114. Small Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

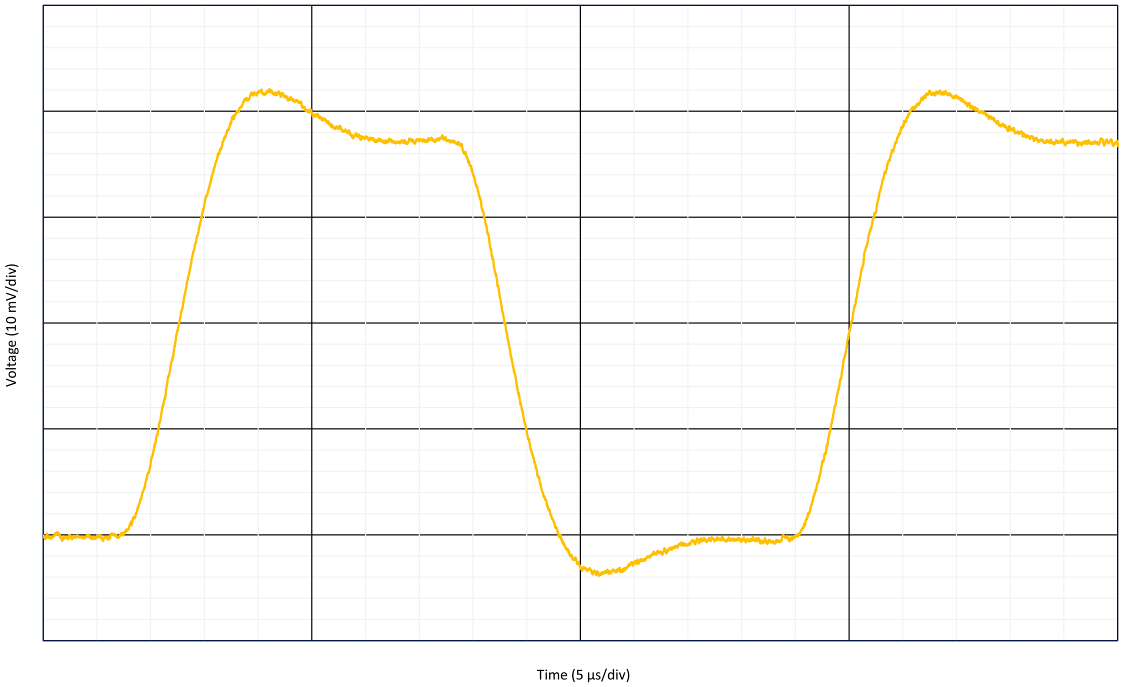


Figure 115. Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

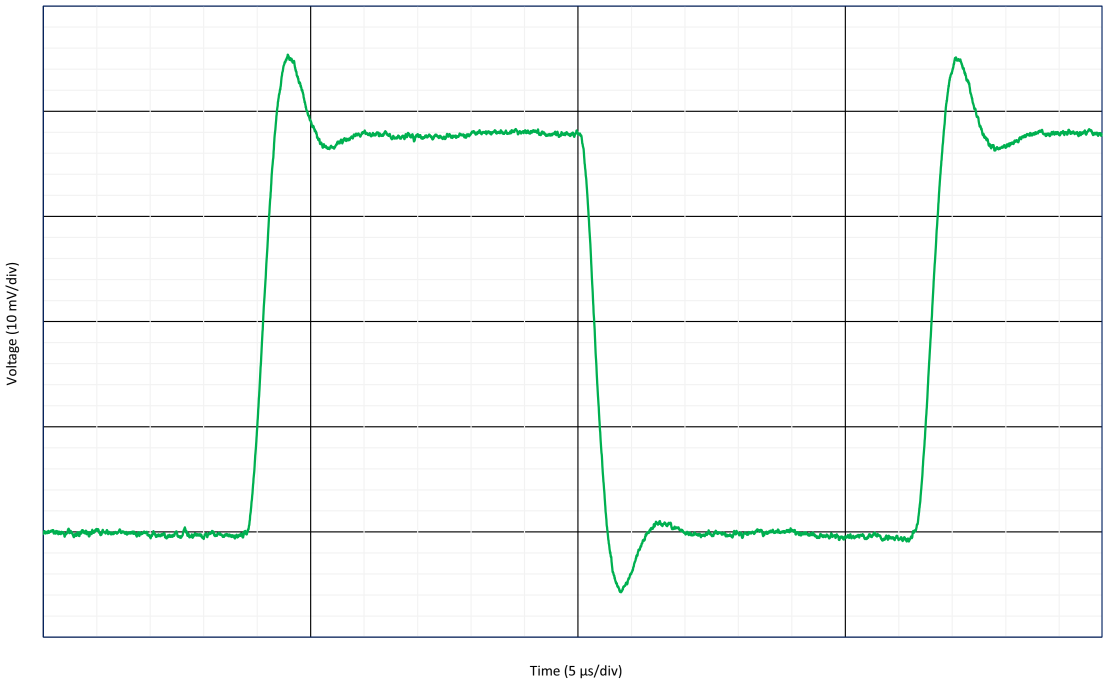


Figure 116. Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

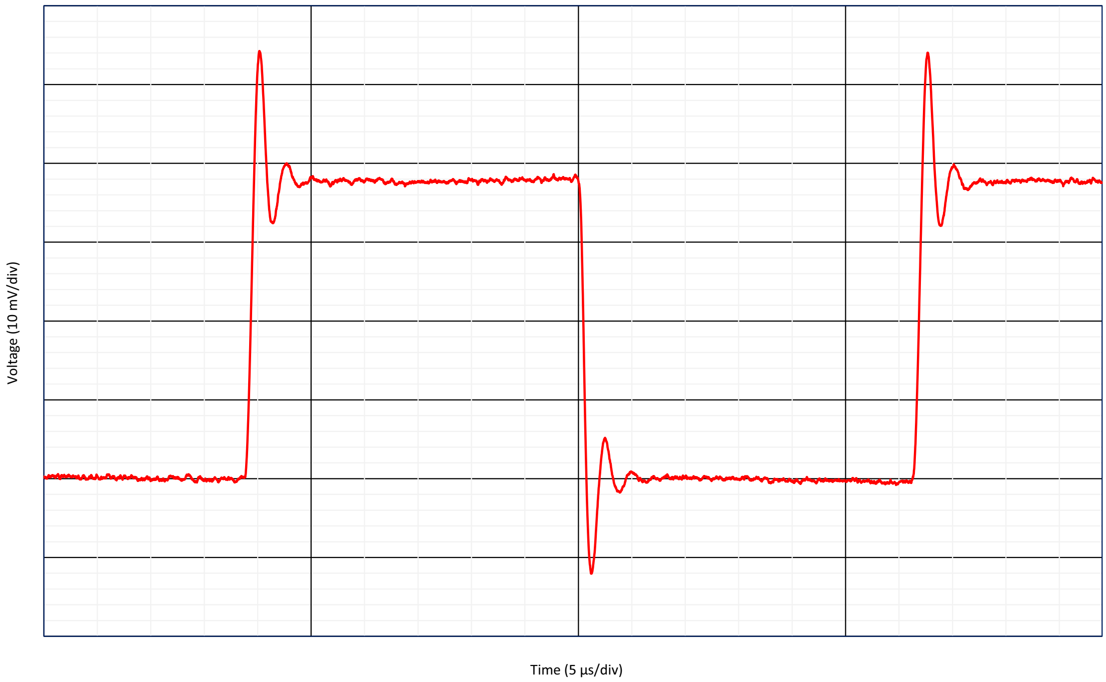


Figure 117. Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

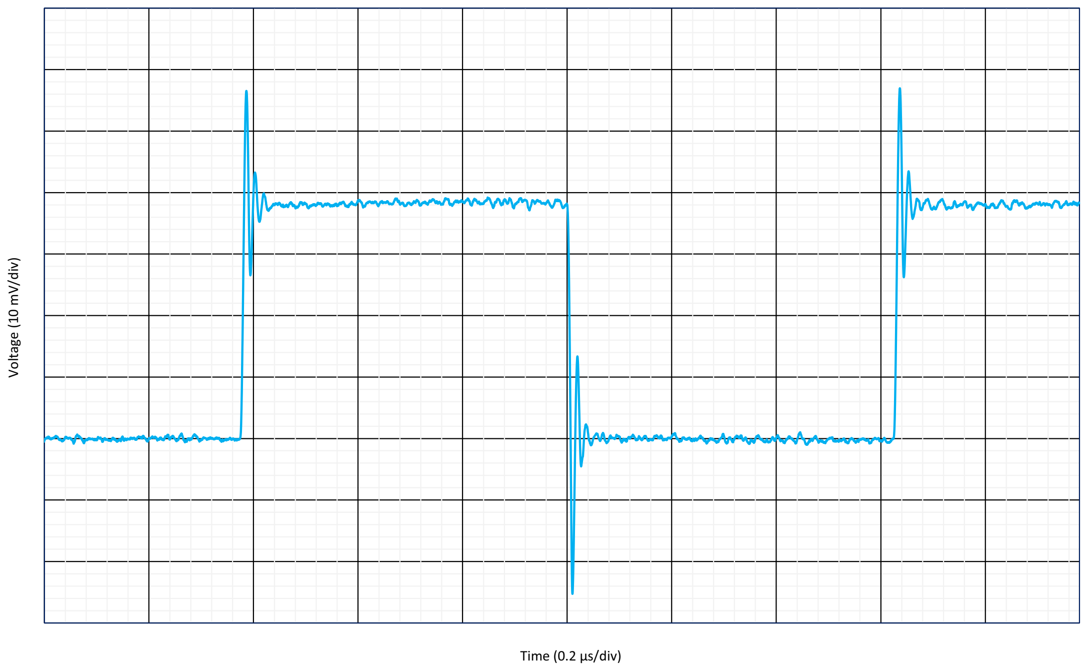


Figure 118. Small Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

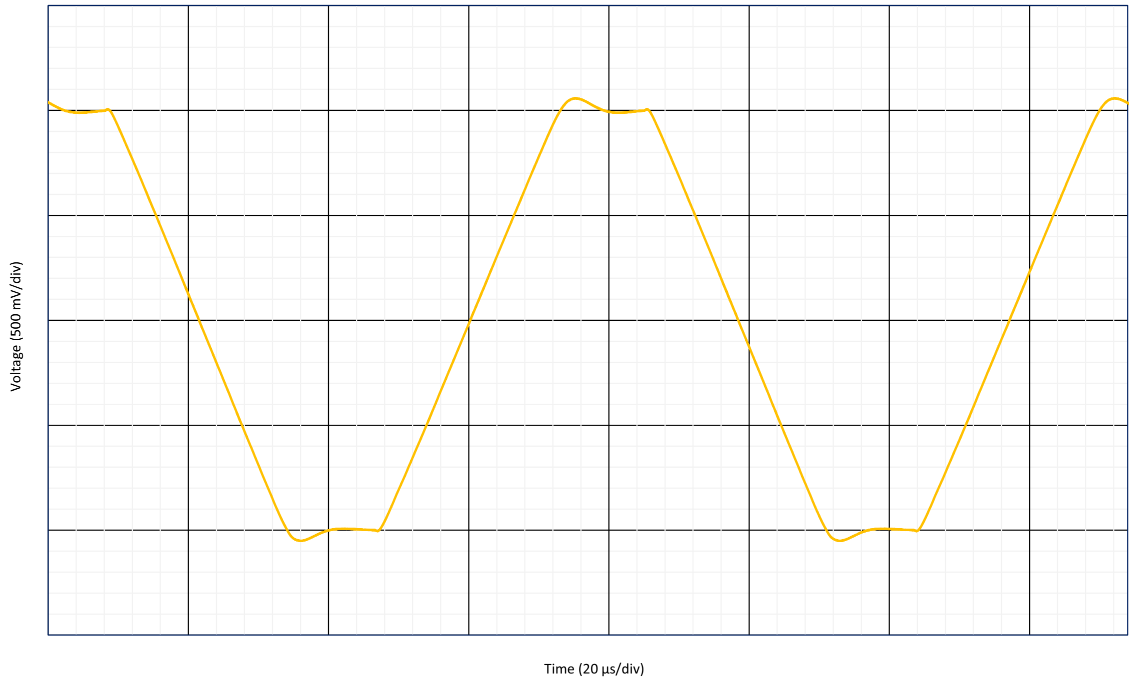


Figure 119. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 128 kHz

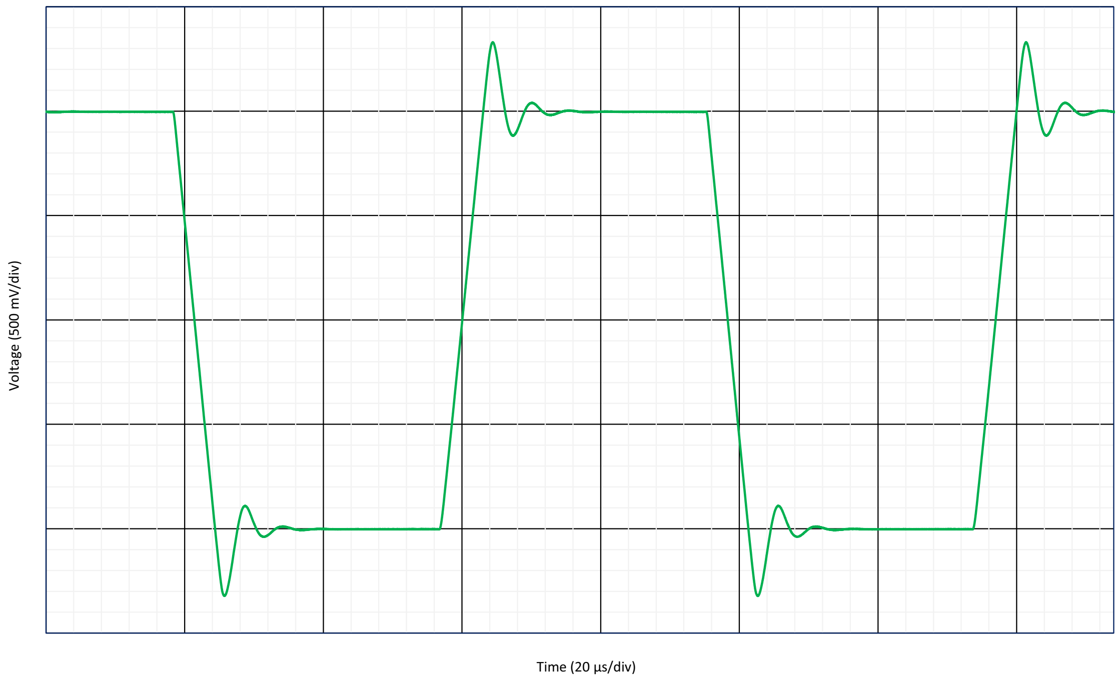


Figure 120. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 512 kHz

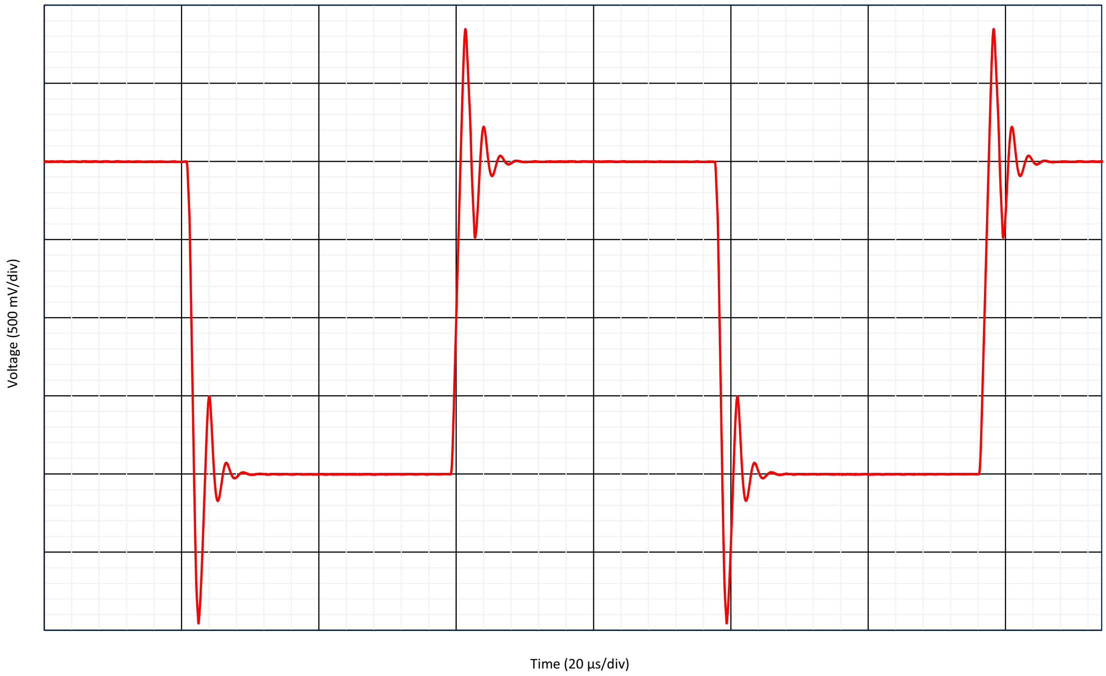


Figure 121. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 2 MHz

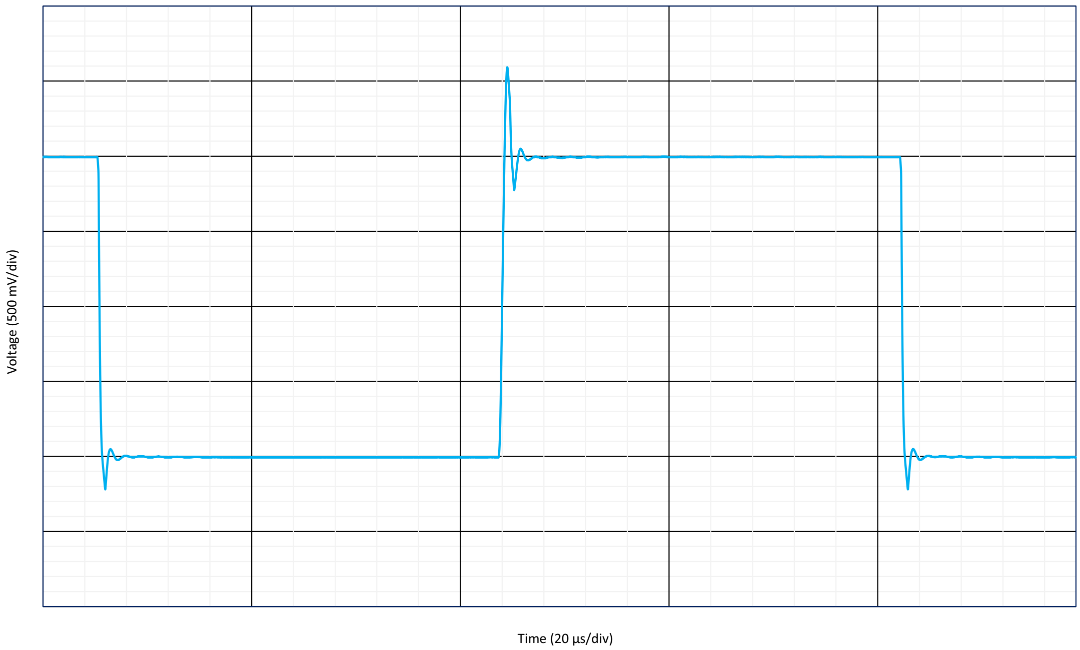


Figure 122. Large Signal Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 80 pF, BW = 8 MHz

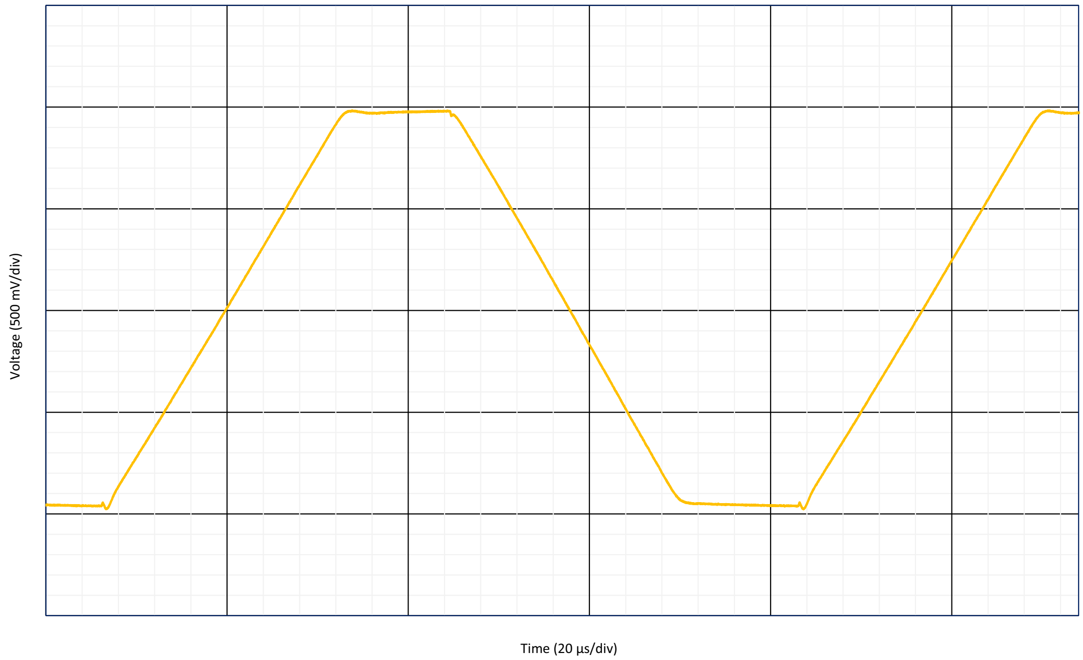


Figure 123. Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

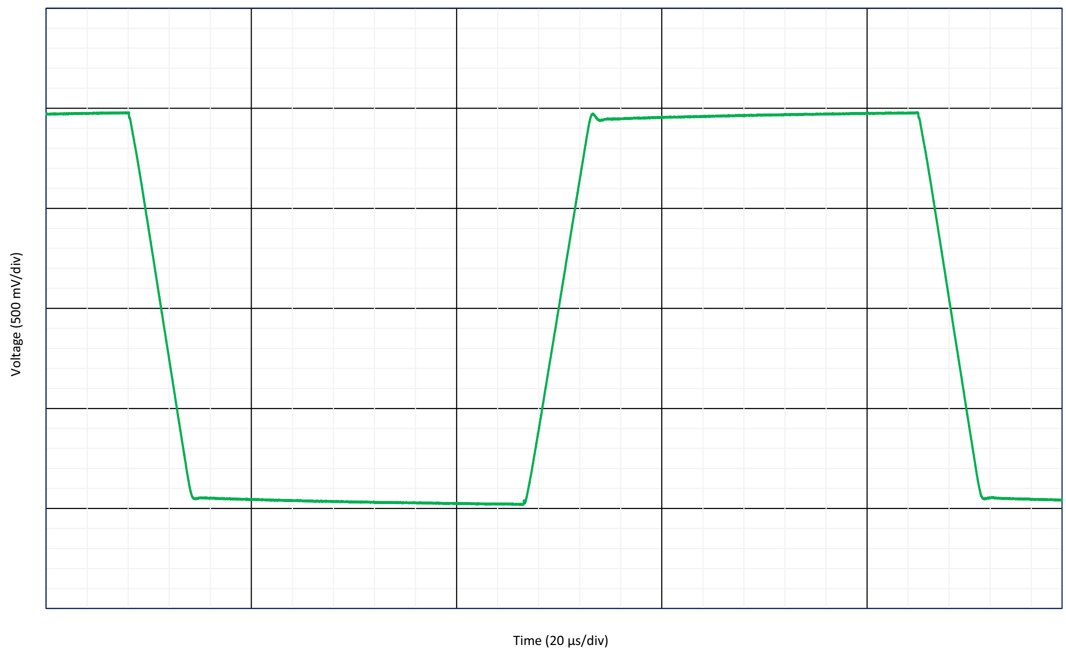


Figure 124. Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

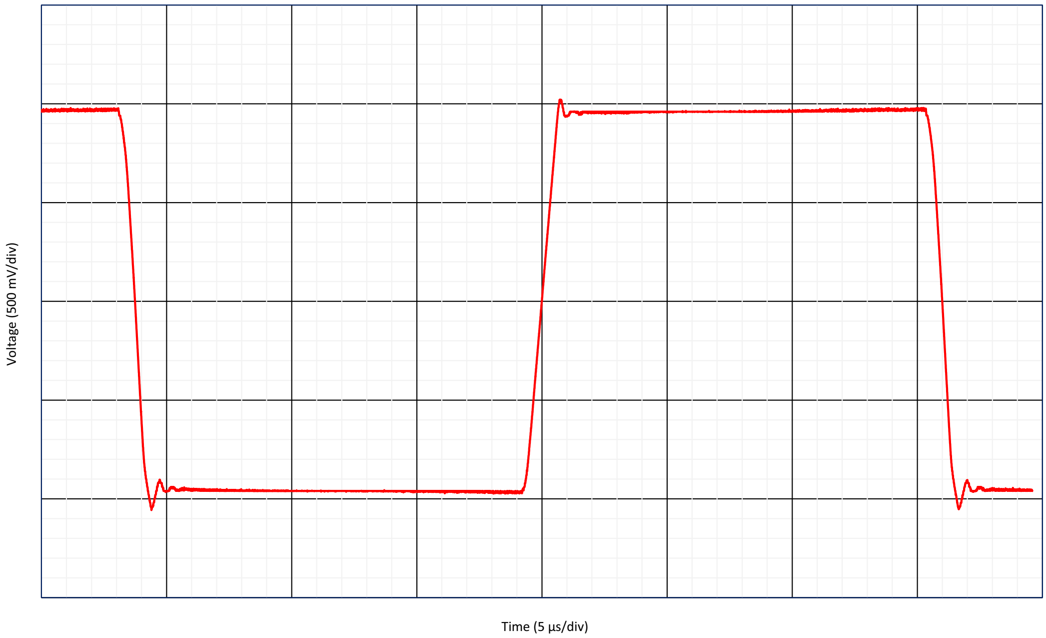


Figure 125. Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

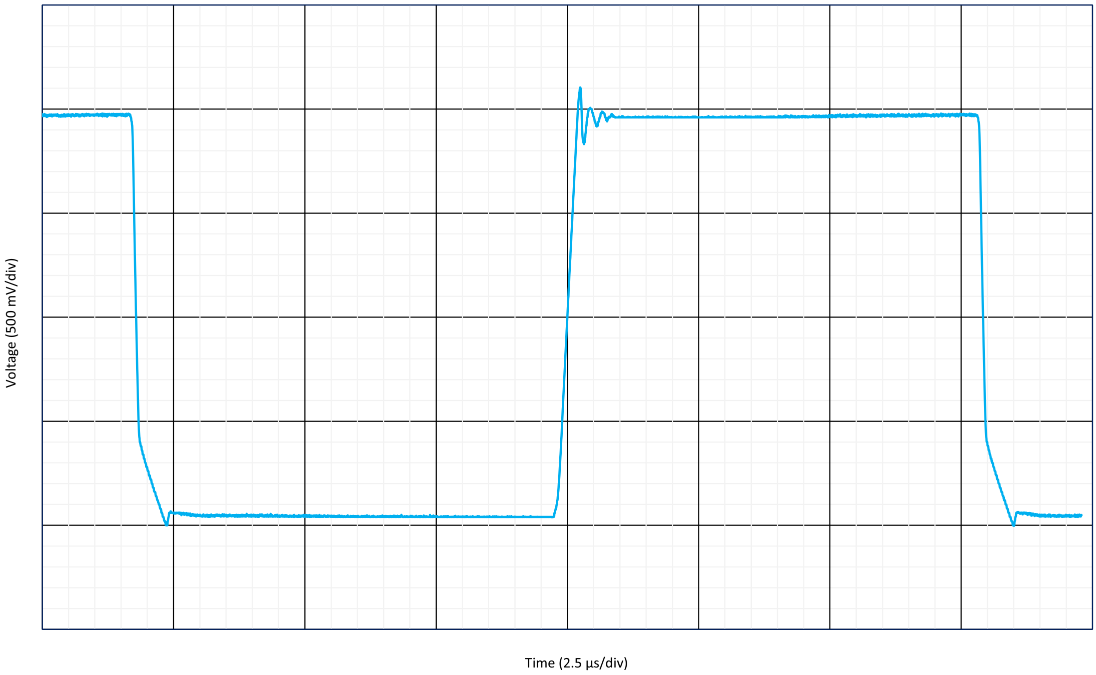


Figure 126. Large Signal Non-Inverting Step Response G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

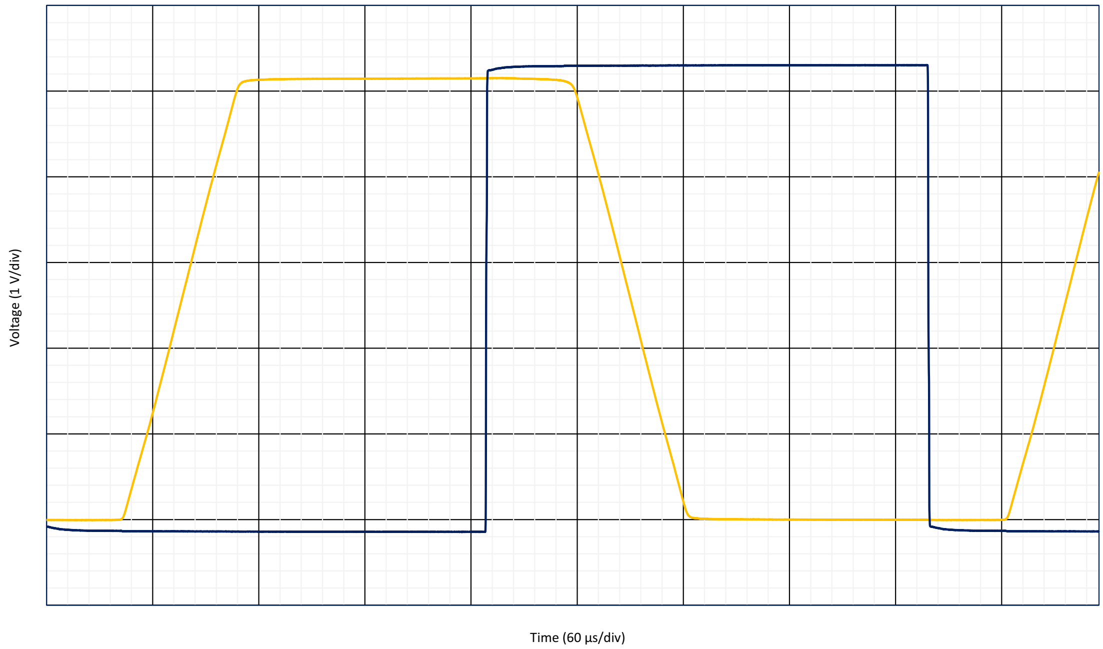


Figure 127. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

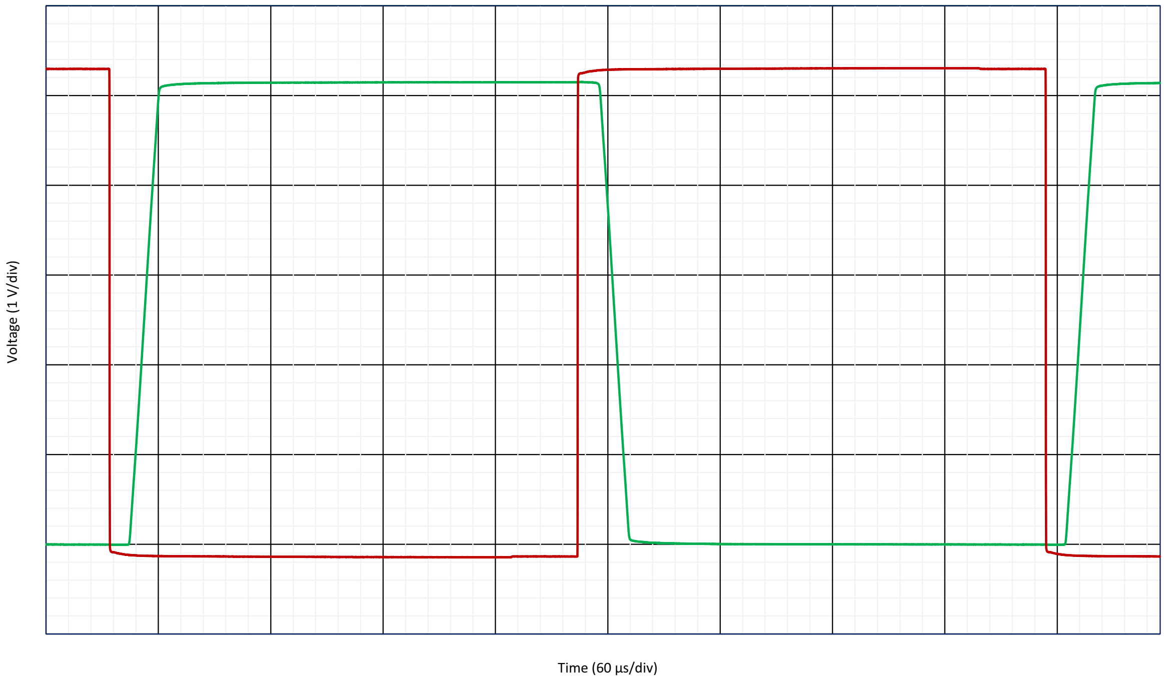


Figure 128. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

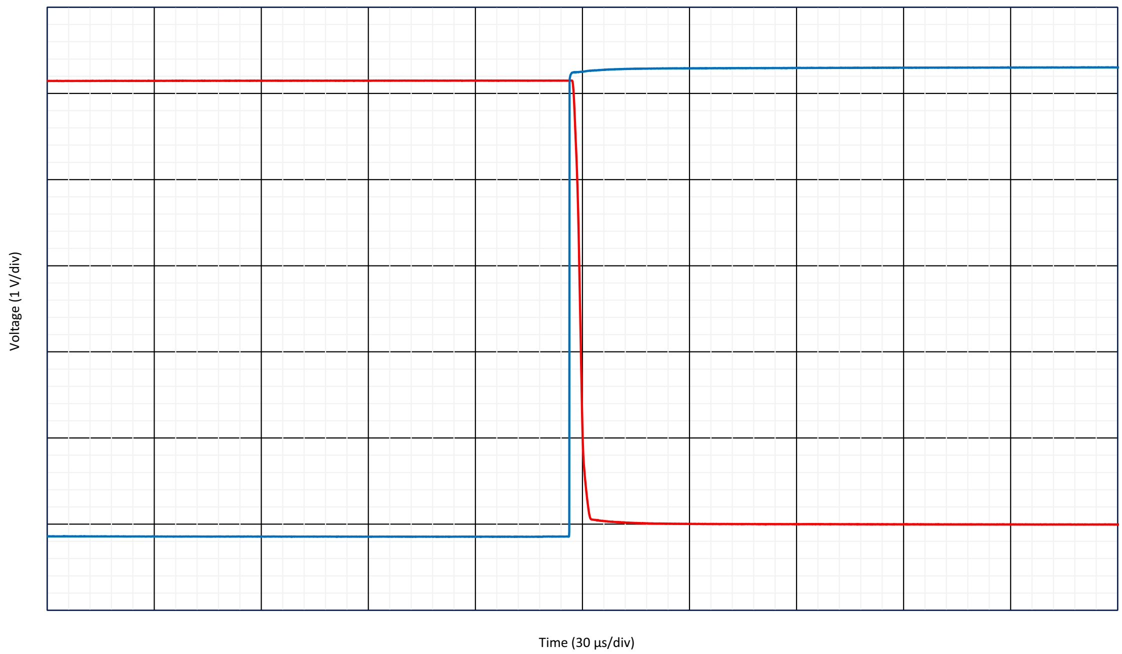


Figure 129. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

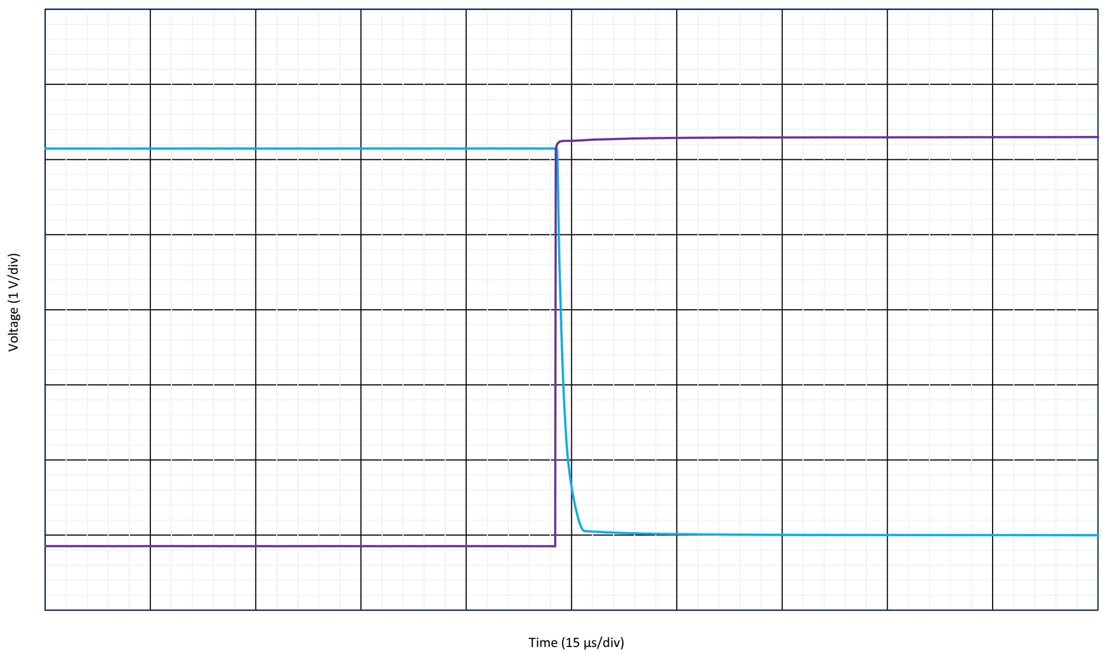


Figure 130. Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

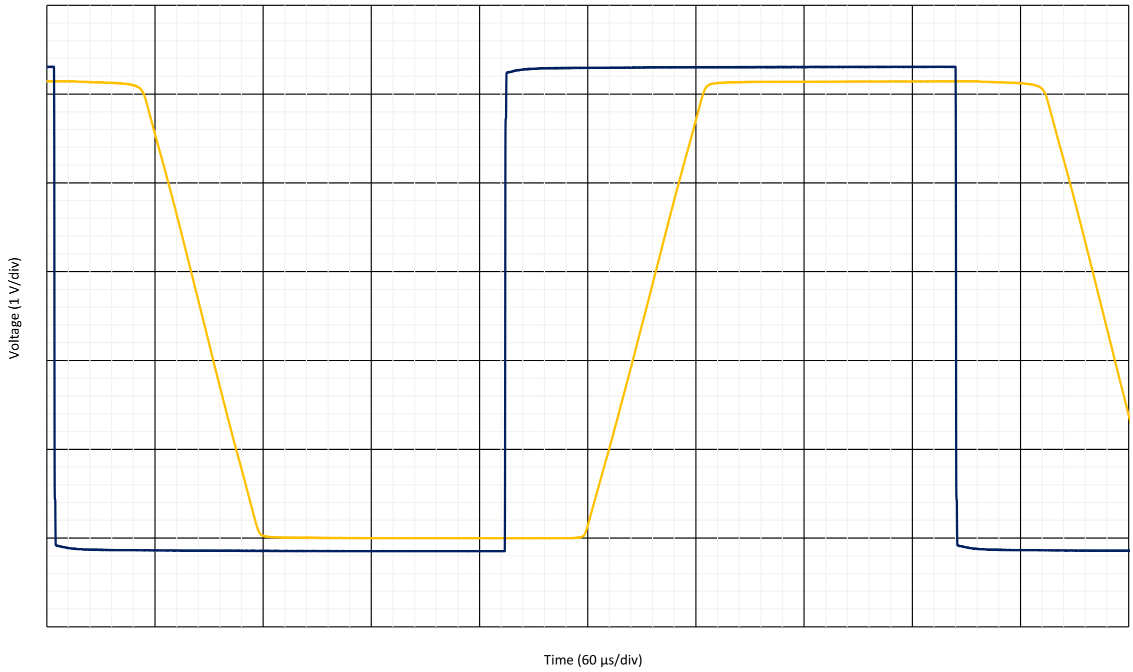


Figure 131. Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 128 kHz

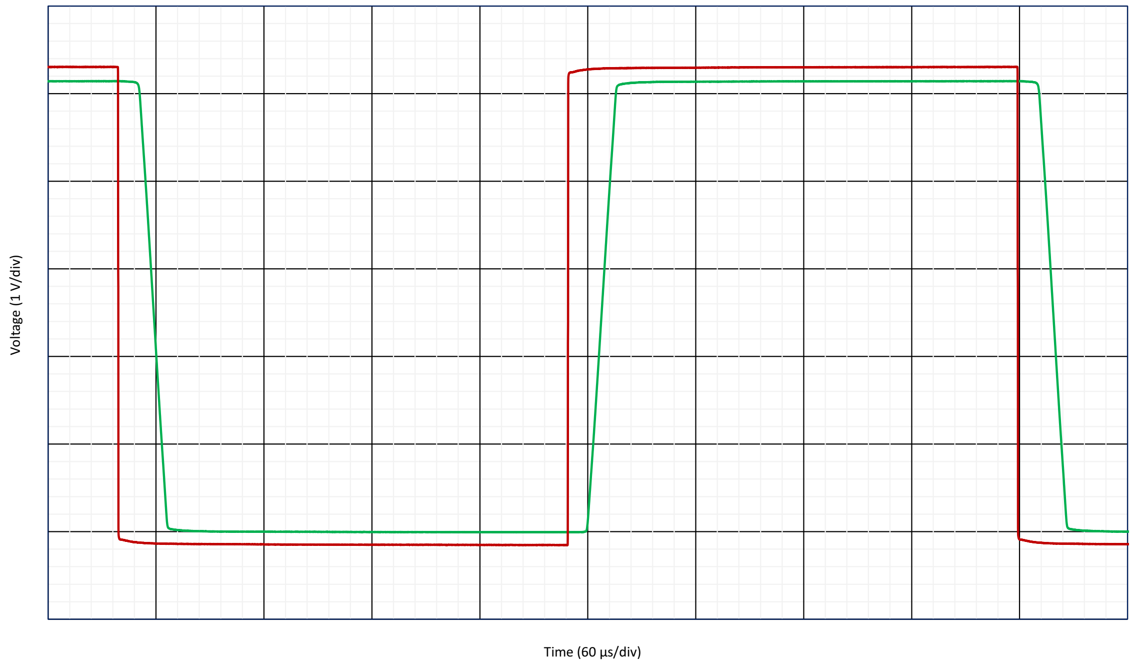


Figure 132. Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 512 kHz

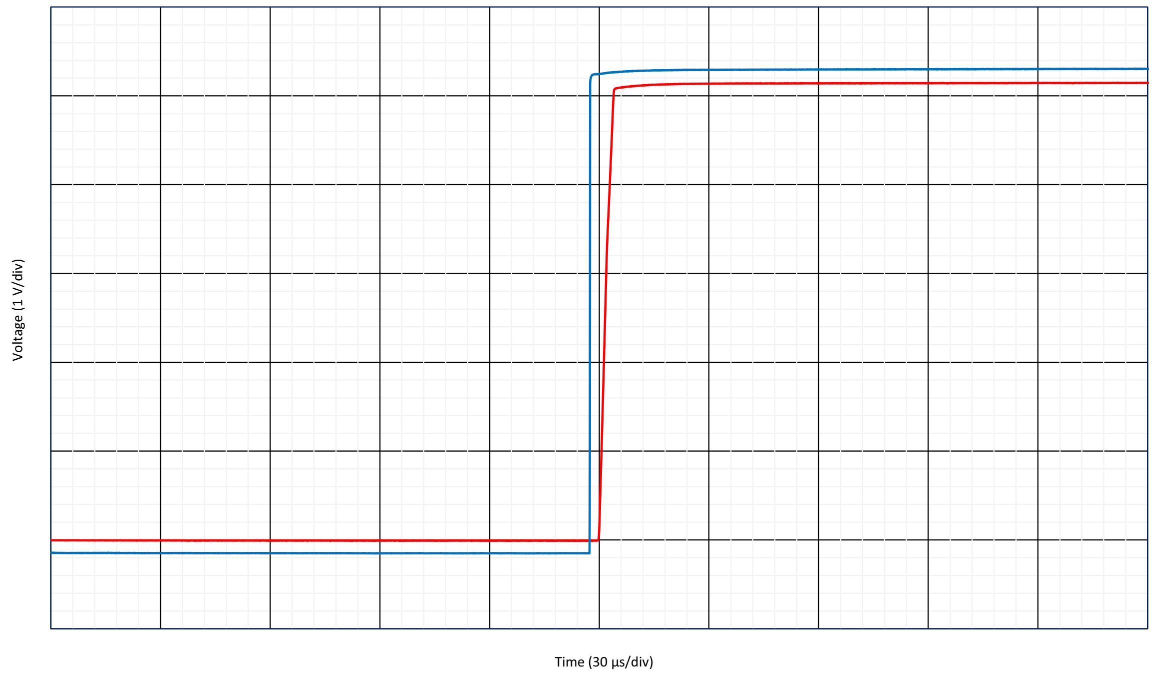


Figure 133. Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 2 MHz

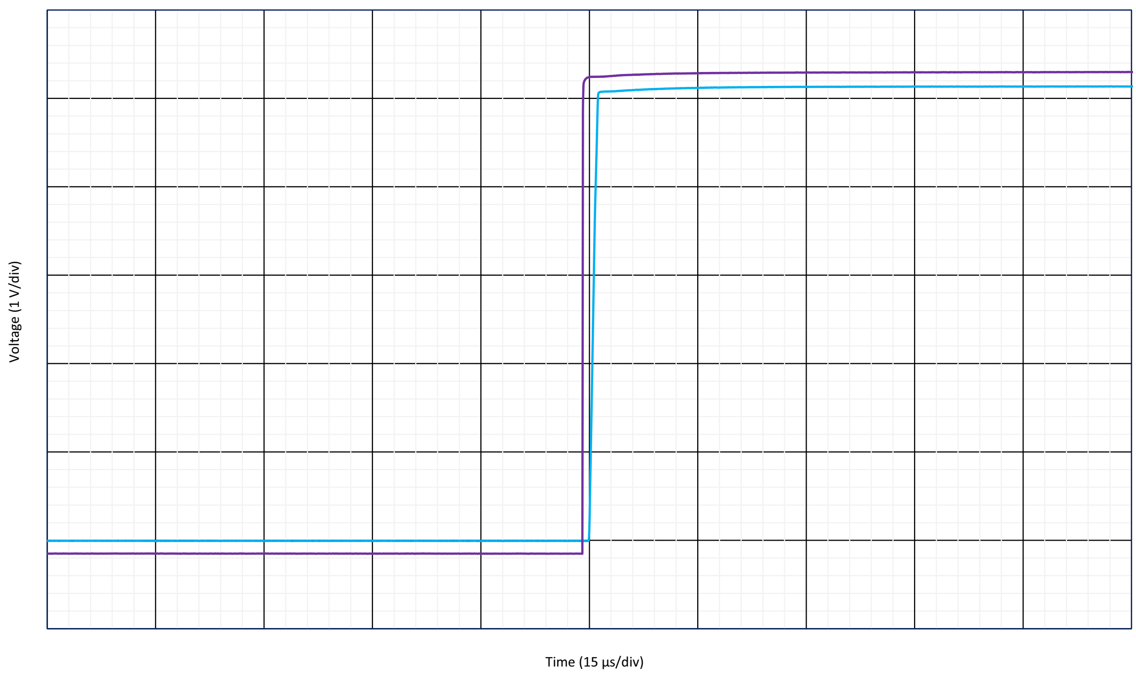


Figure 134. Non-Inverting Overload Recovery G = -1 V/V, R_L = 50 kΩ, C_L = 60 pF, BW = 8 MHz

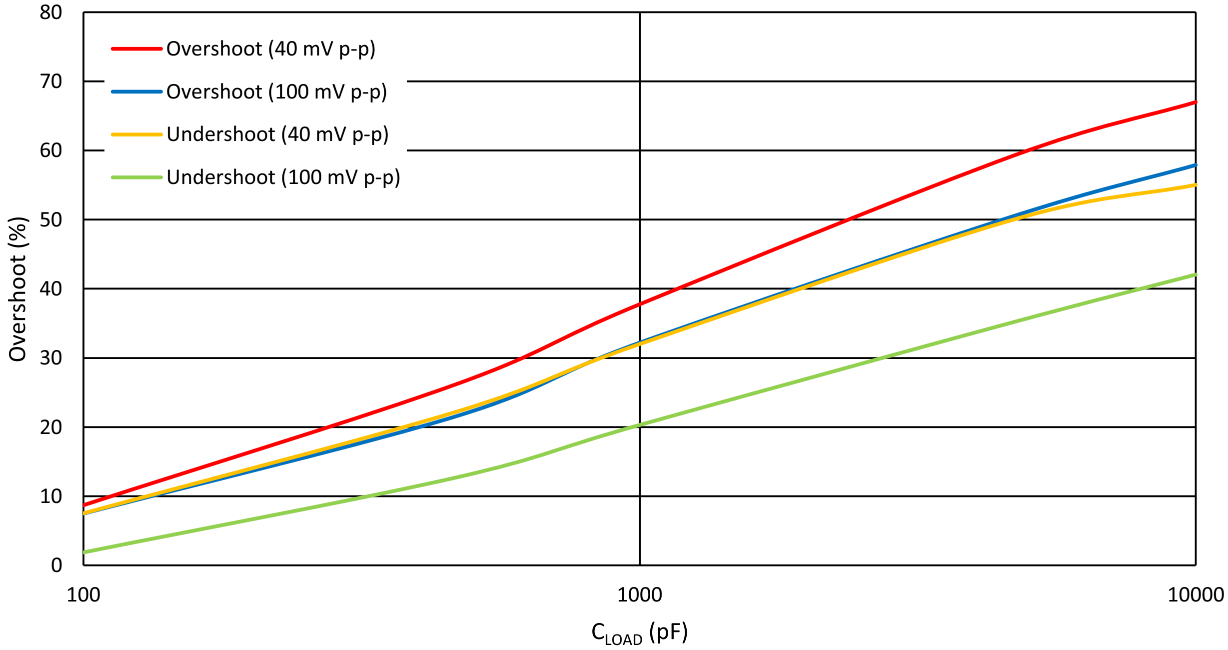


Figure 135. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 128 kHz

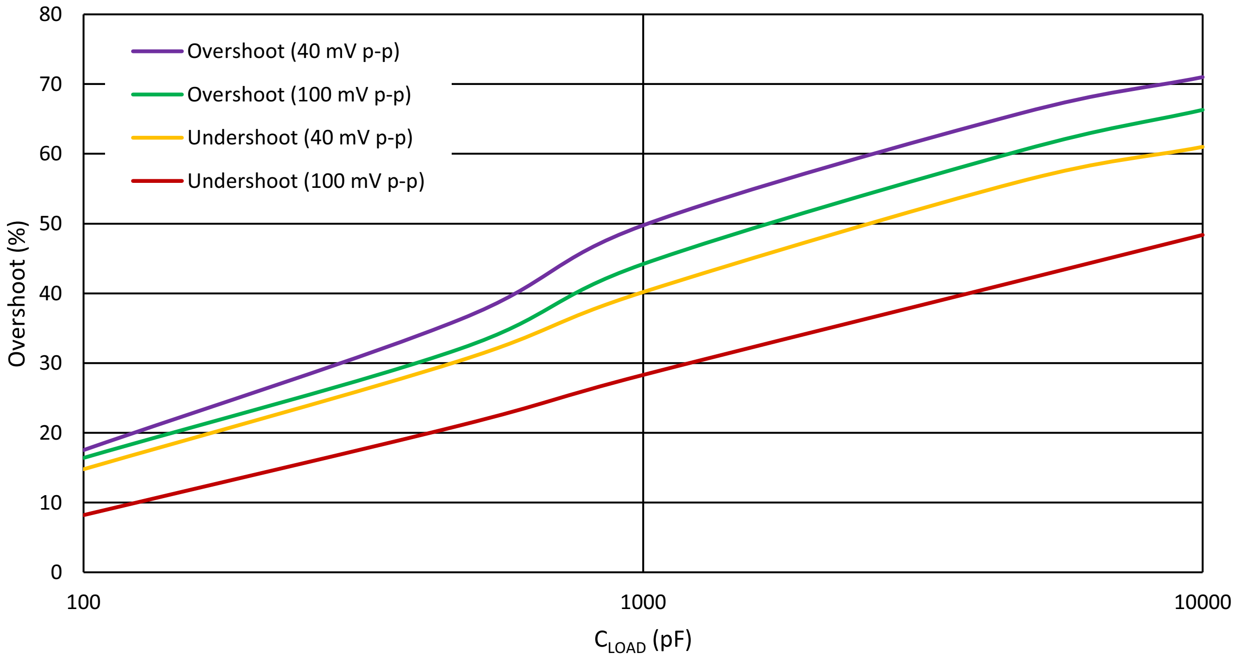


Figure 136. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 512 kHz

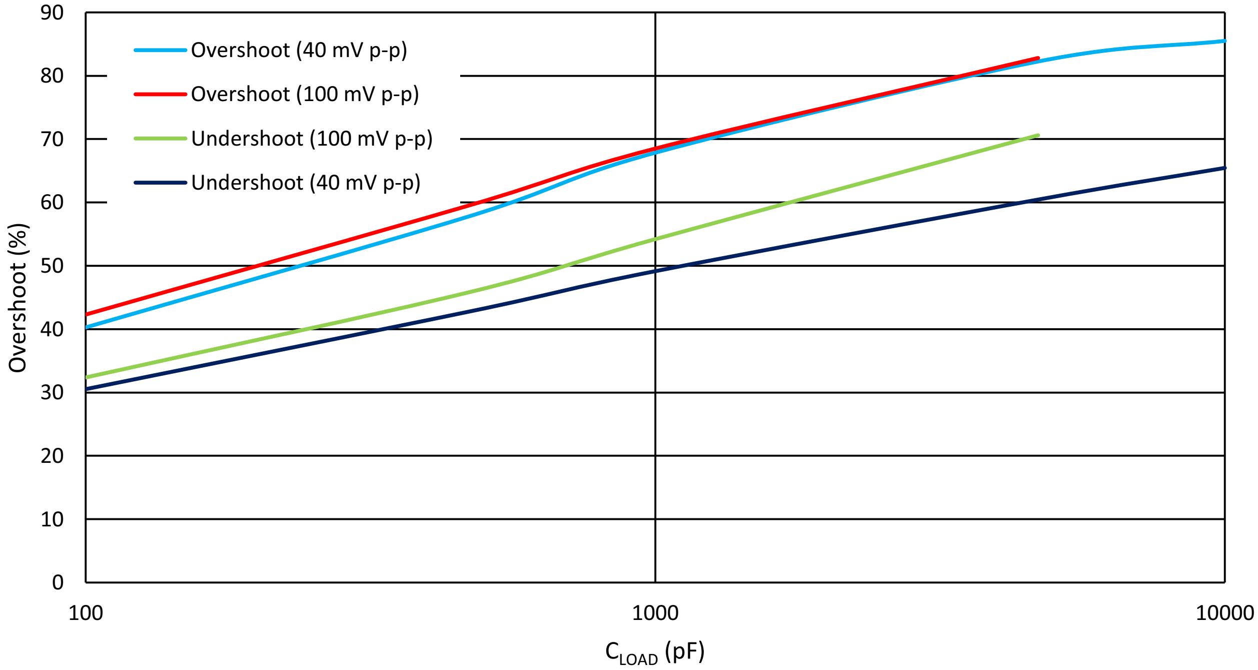


Figure 137. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 2 MHz

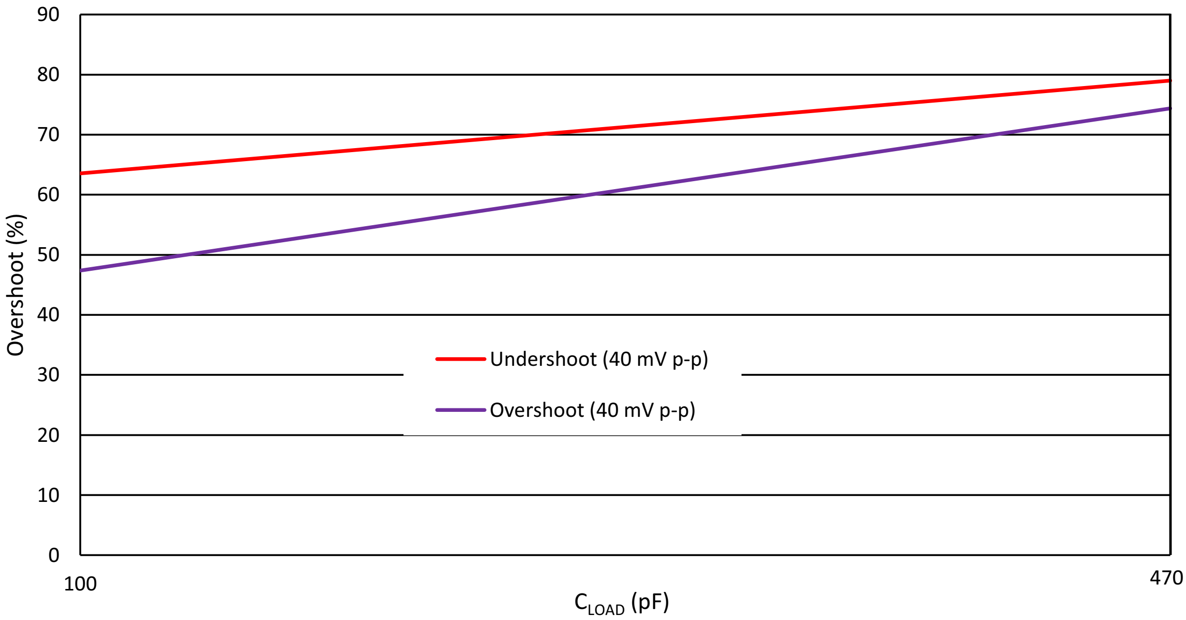


Figure 138. Small Signal Overshoot vs. Capacitive Load V_{DD} = 3.3 V, G = 1 V/V, BW = 8 MHz

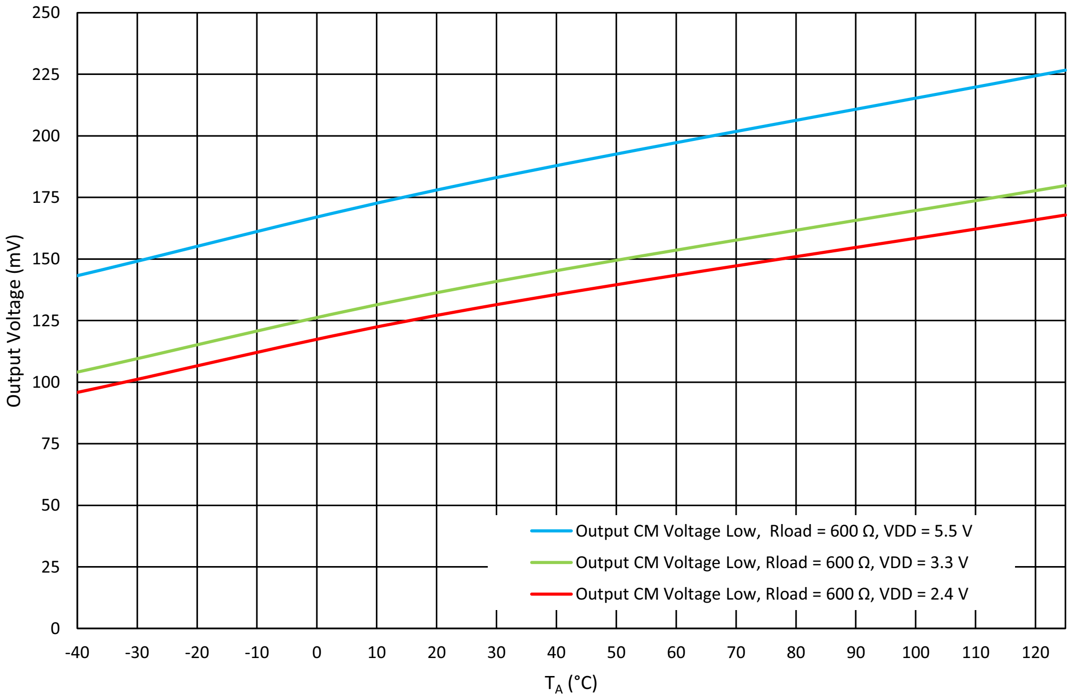


Figure 139. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

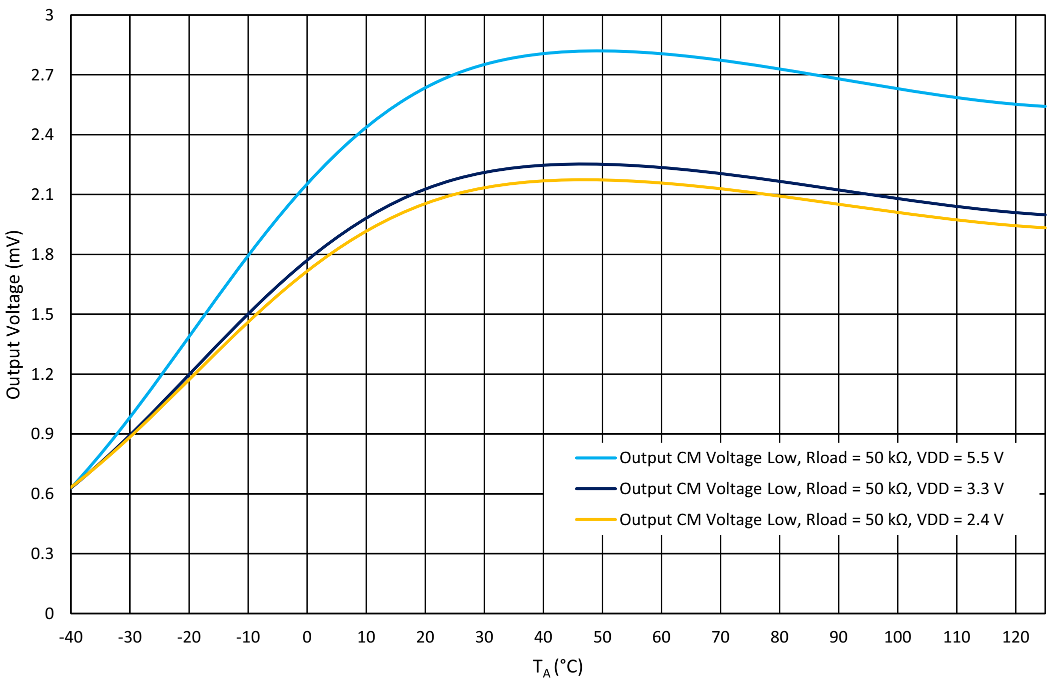


Figure 140. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

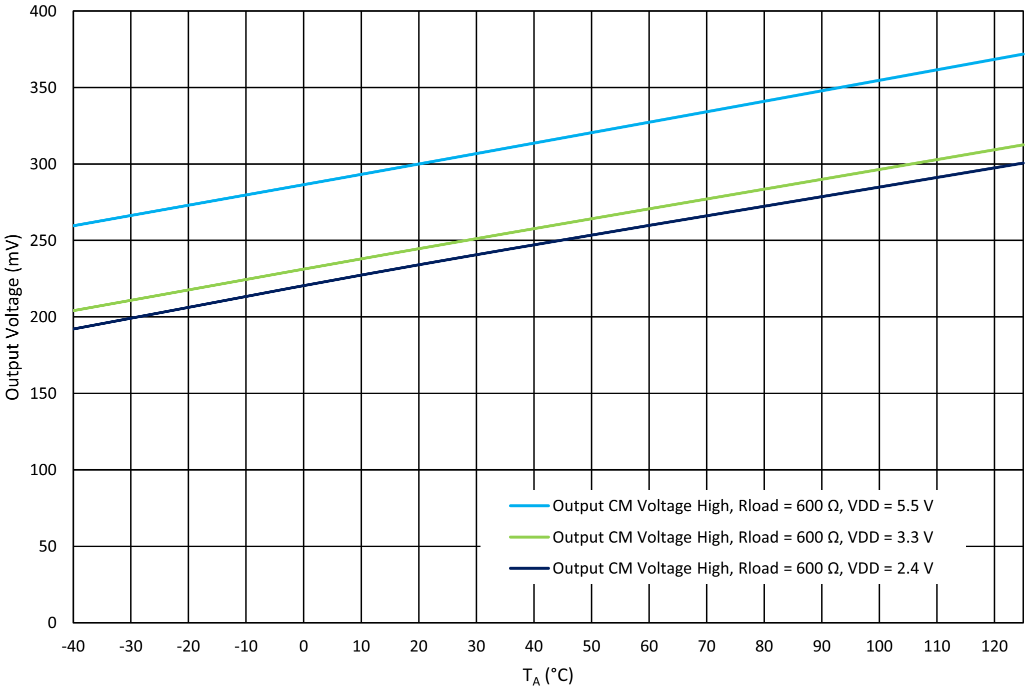


Figure 141. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 128 kHz, R_{LOAD} = 600 Ω

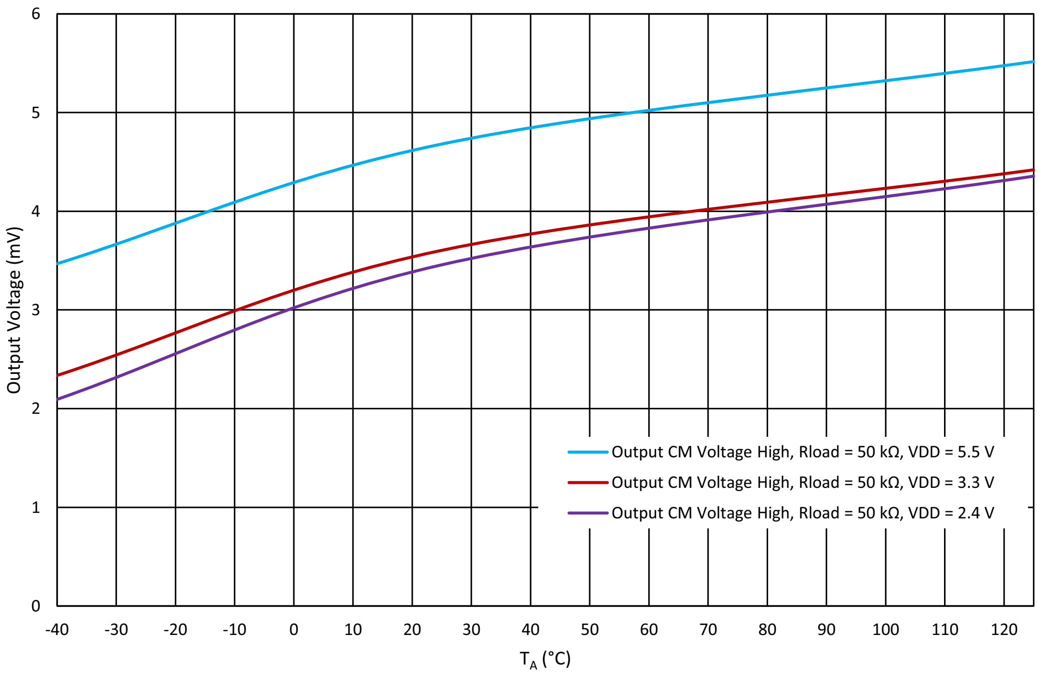


Figure 142. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 128 kHz, R_{LOAD} = 50 kΩ

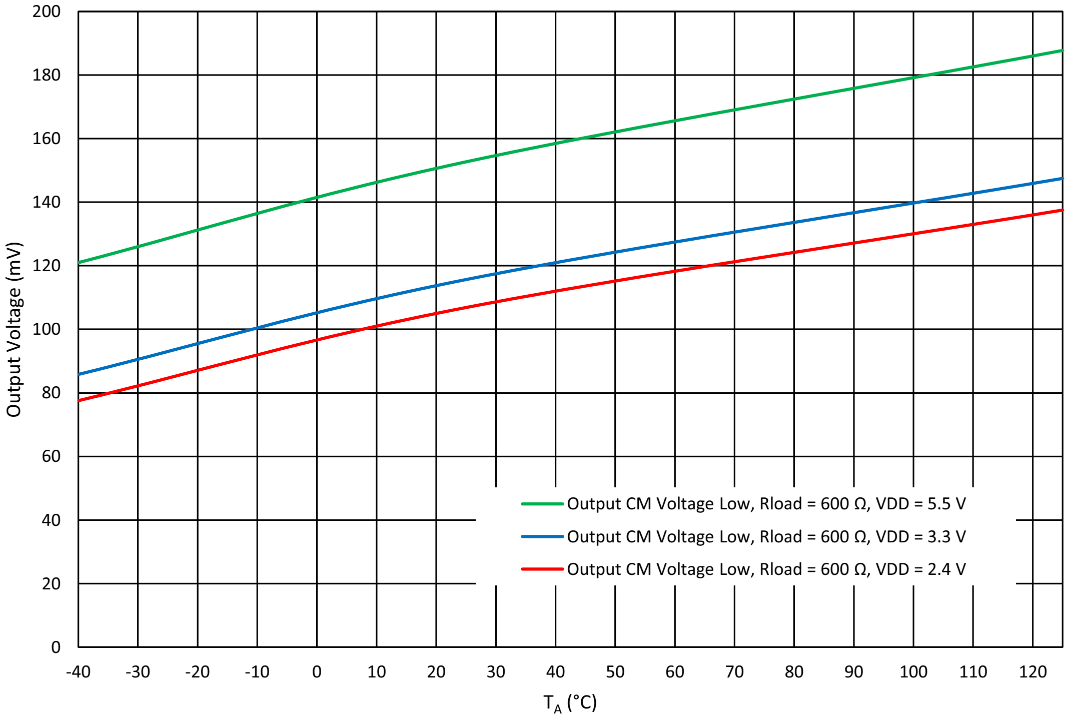


Figure 143. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

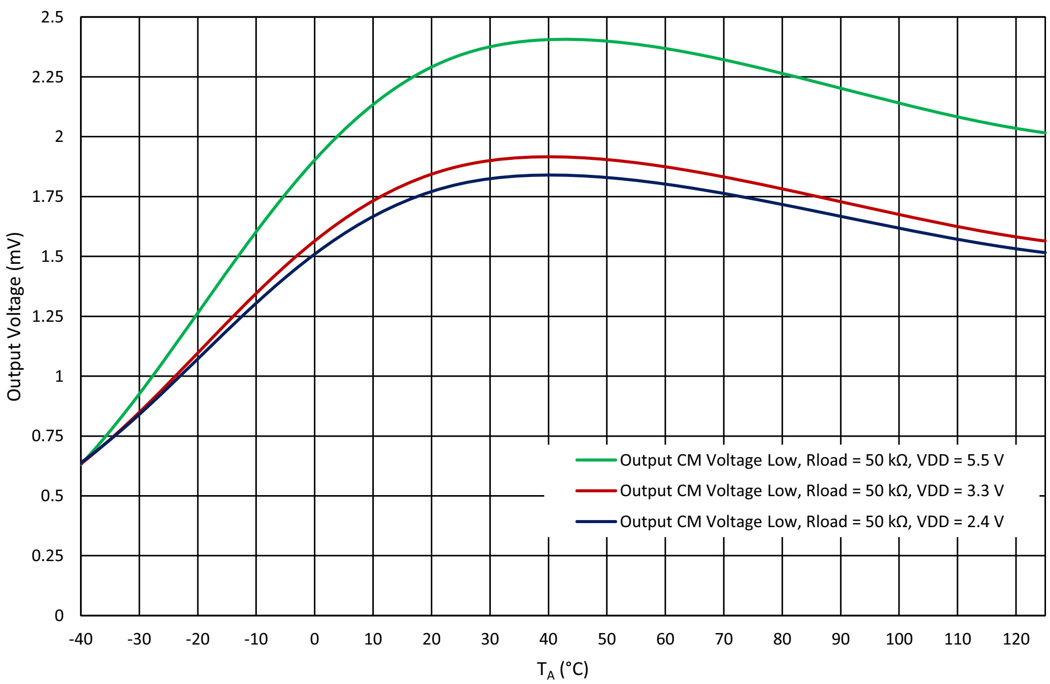


Figure 144. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 512 kHz, R_{LOAD} = 50 kΩ

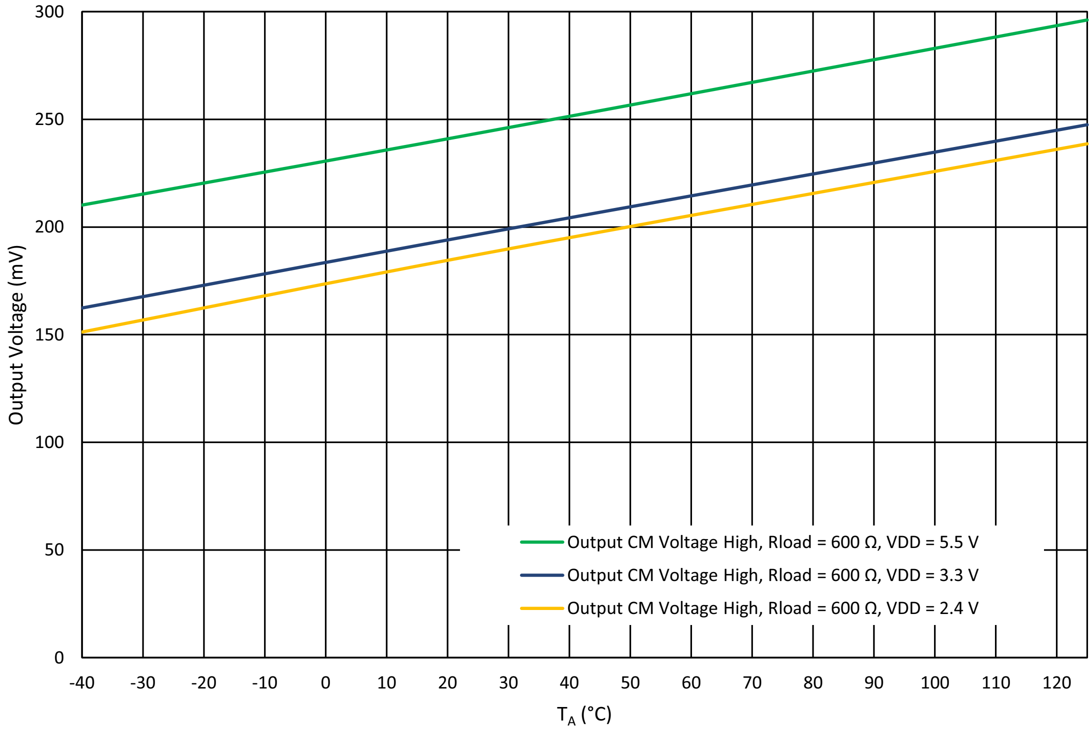


Figure 145. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 512 kHz, R_{LOAD} = 600 Ω

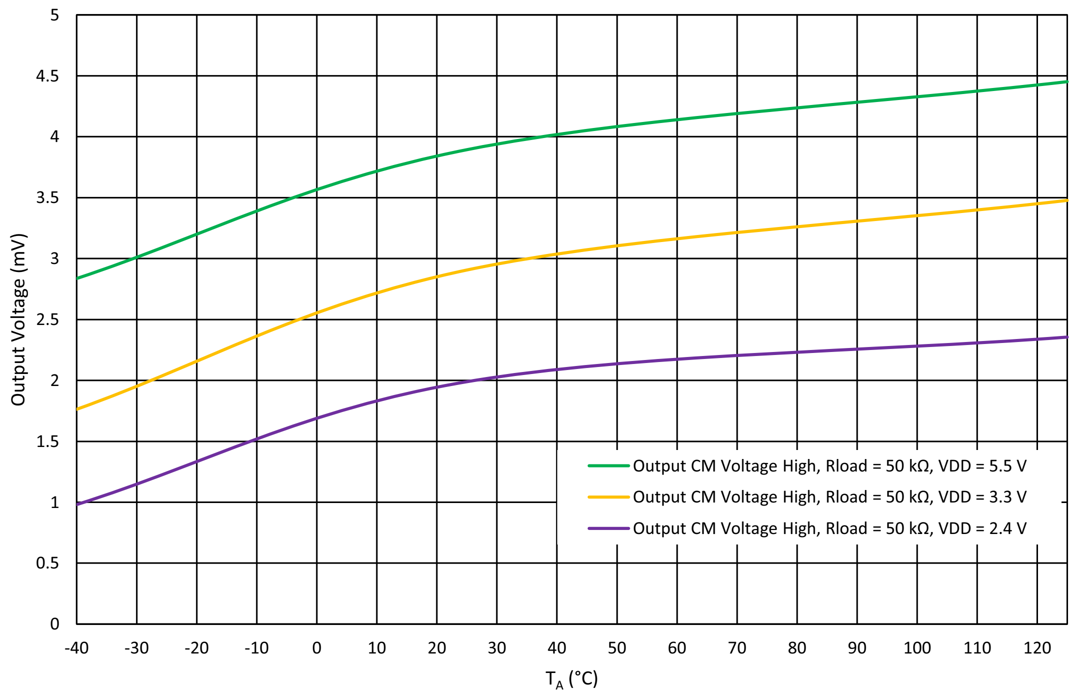


Figure 146. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 512 kHz, R_{LOAD} = 50 kΩ

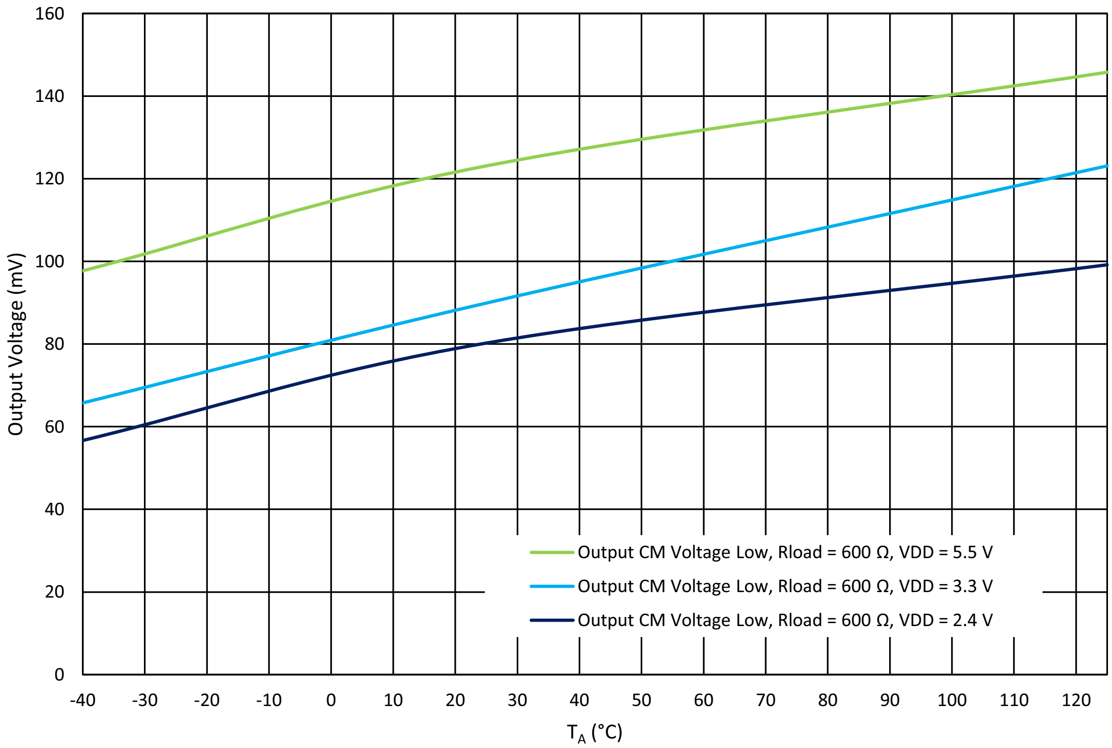


Figure 147. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

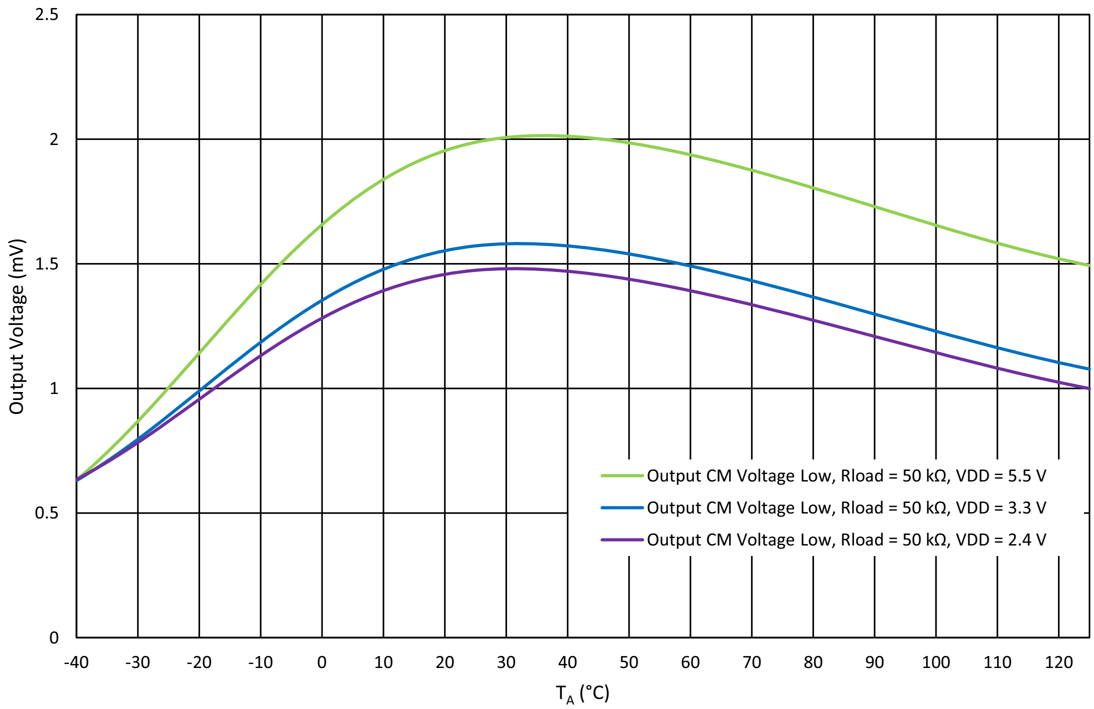


Figure 148. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

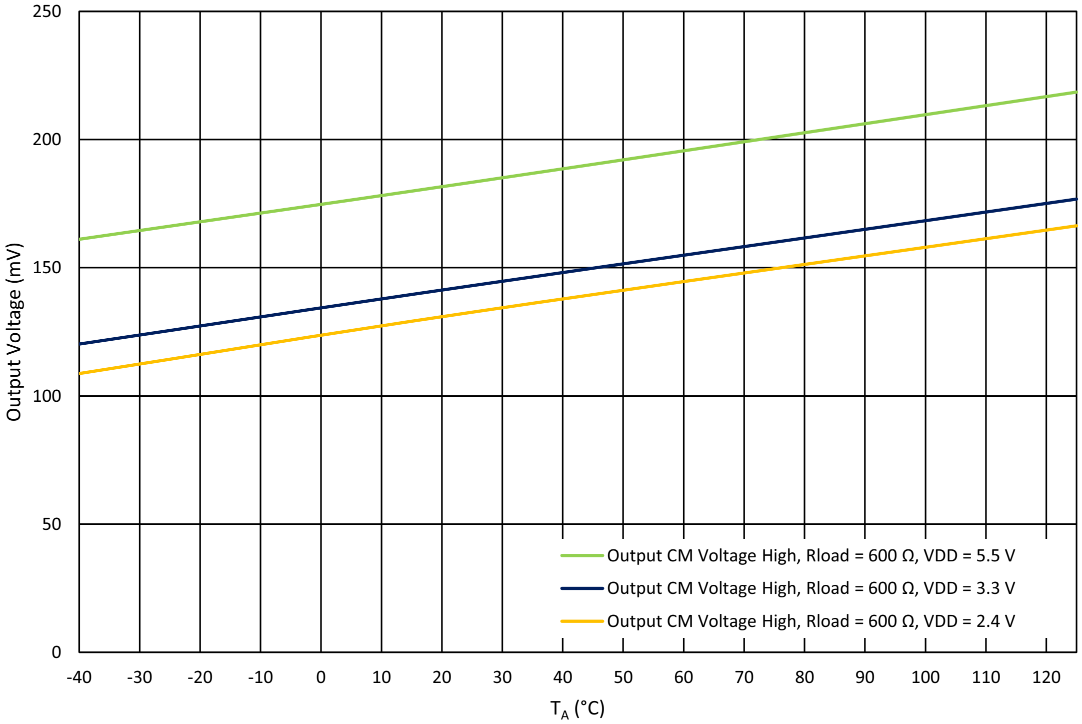


Figure 149. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 2 MHz, R_{LOAD} = 600 Ω

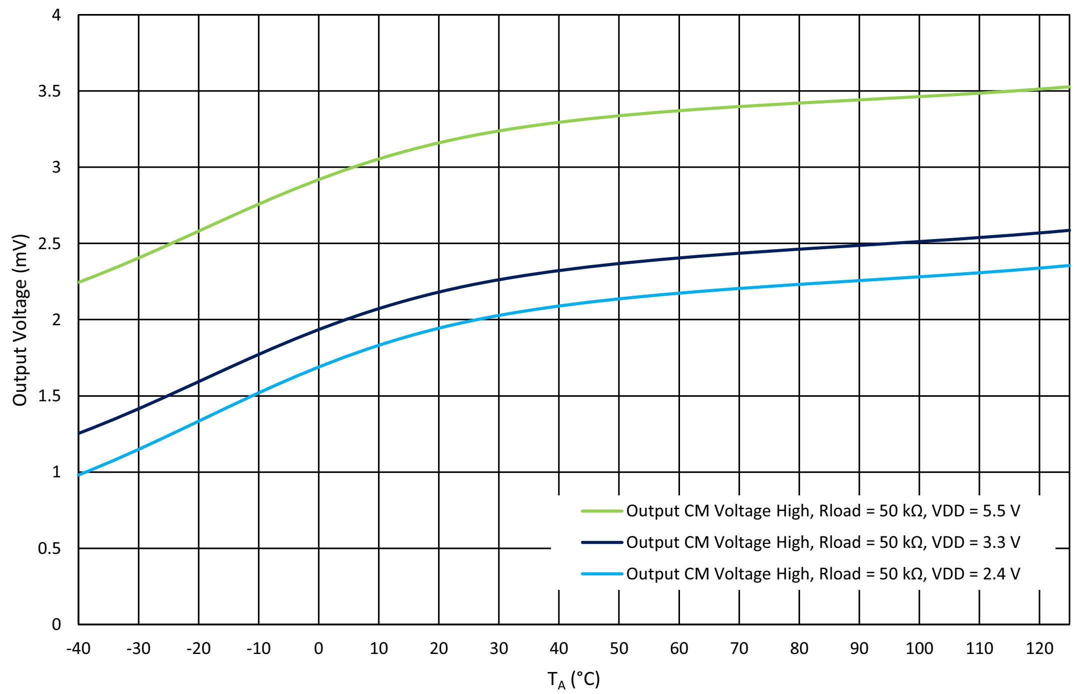


Figure 150. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 2 MHz, R_{LOAD} = 50 kΩ

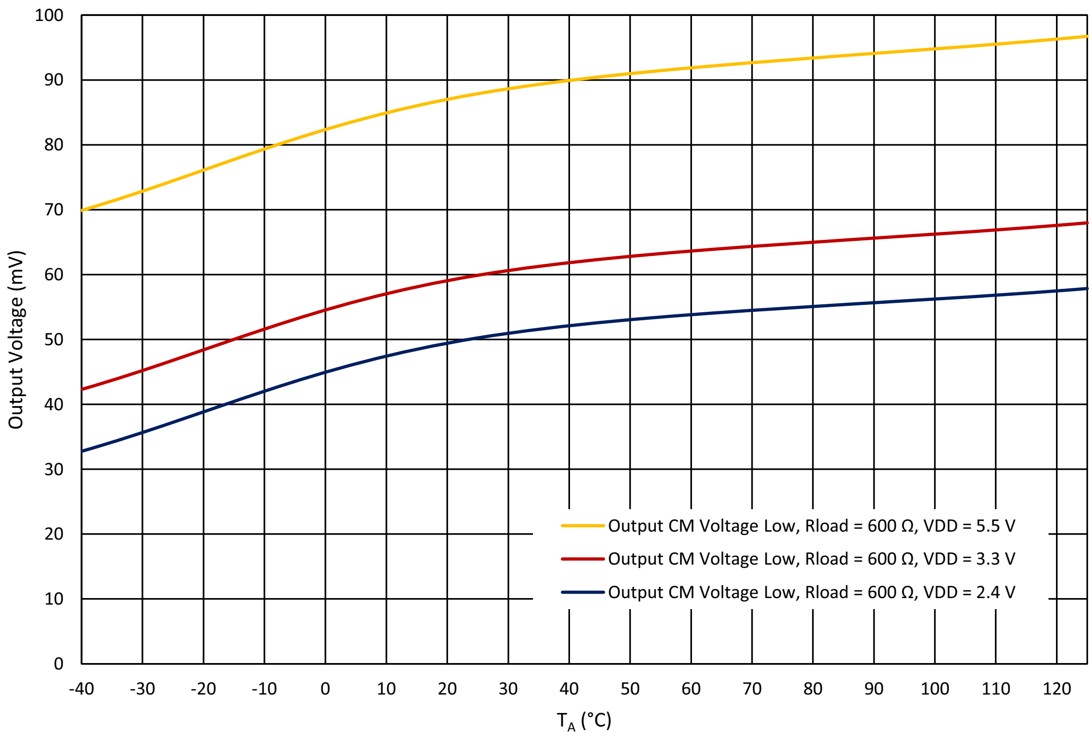


Figure 151. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 8 MHz, R_{LOAD} = 600 Ω

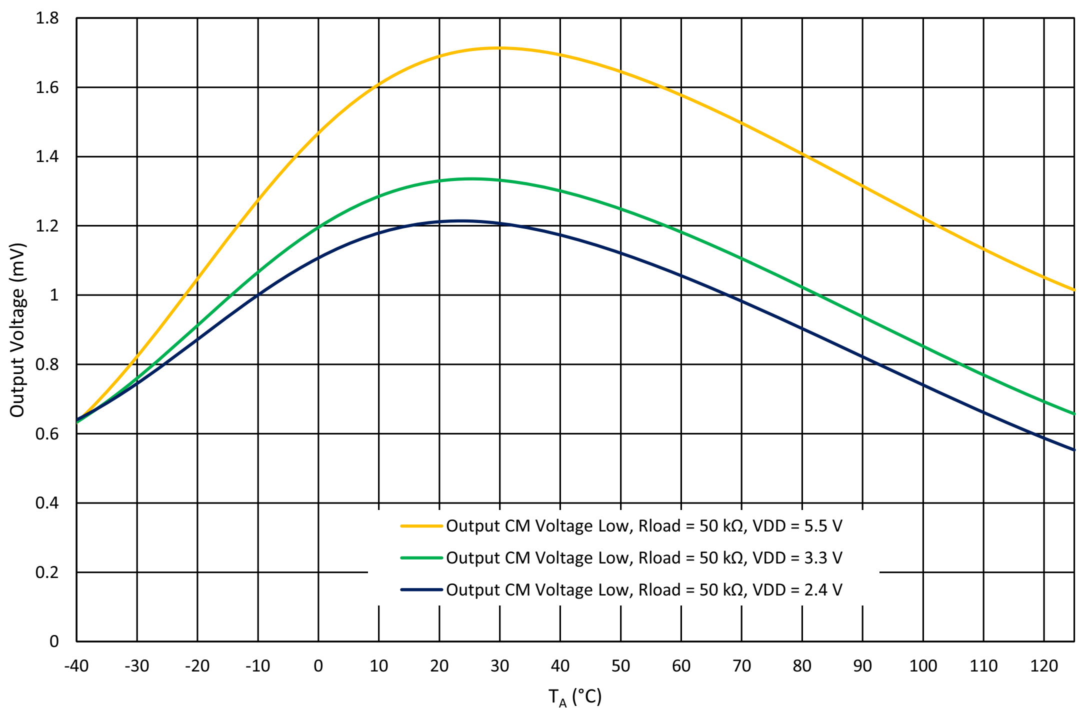


Figure 152. Output Voltage Low (V_{OUT} - GND) vs. Ambient Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

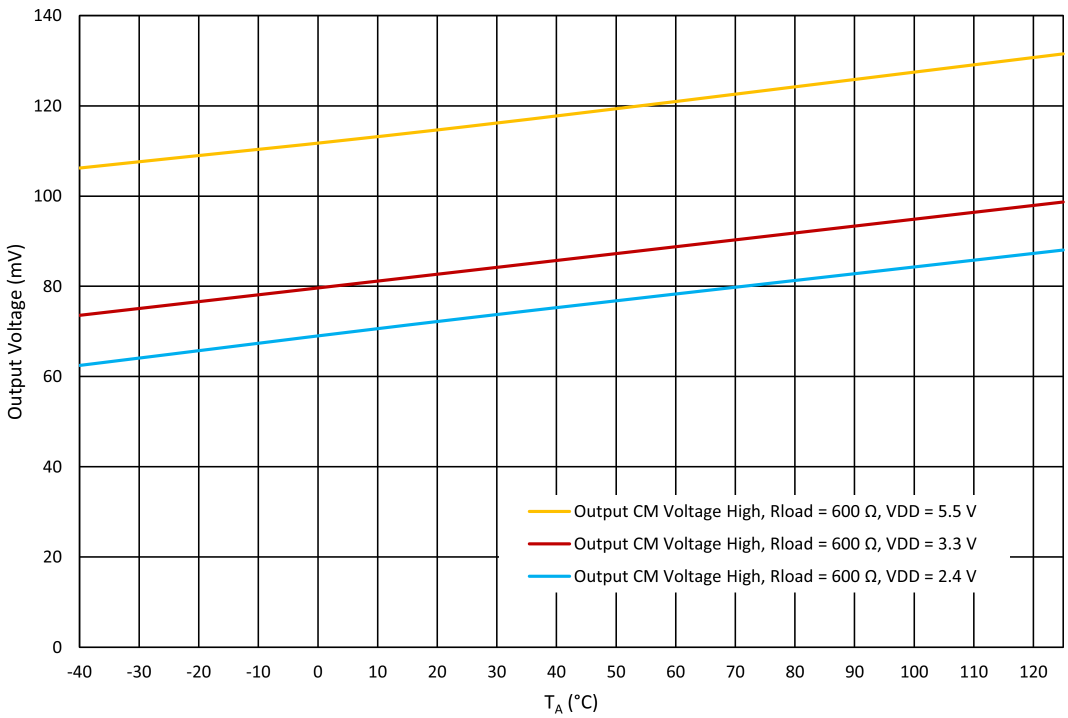


Figure 153. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 8 MHz, R_{LOAD} = 600 Ω

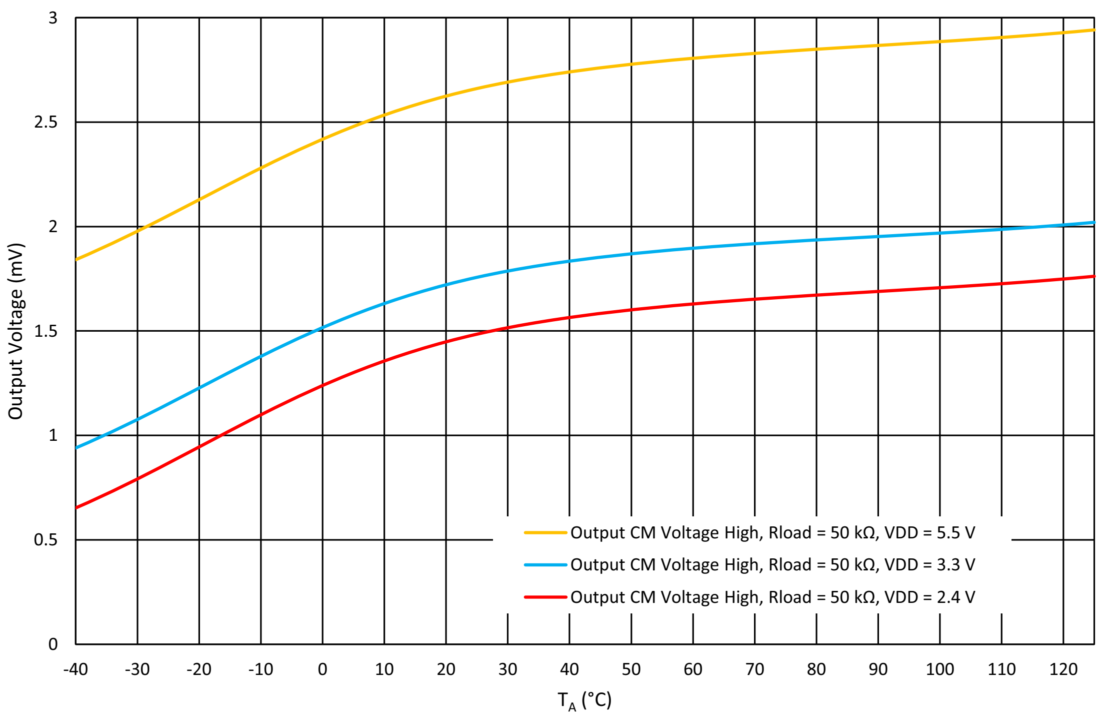


Figure 154. Output Voltage High (V_{DDA} - V_{OUT}) vs. Ambient Temperature at BW = 8 MHz, R_{LOAD} = 50 kΩ

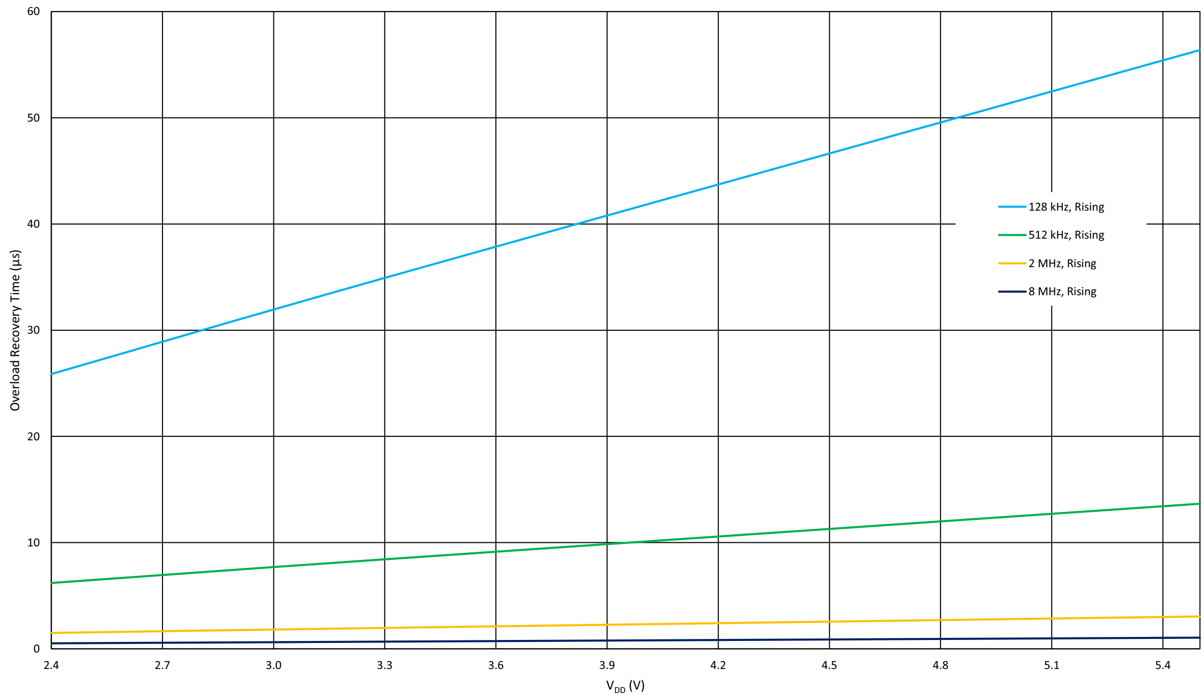


Figure 155. Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Rising

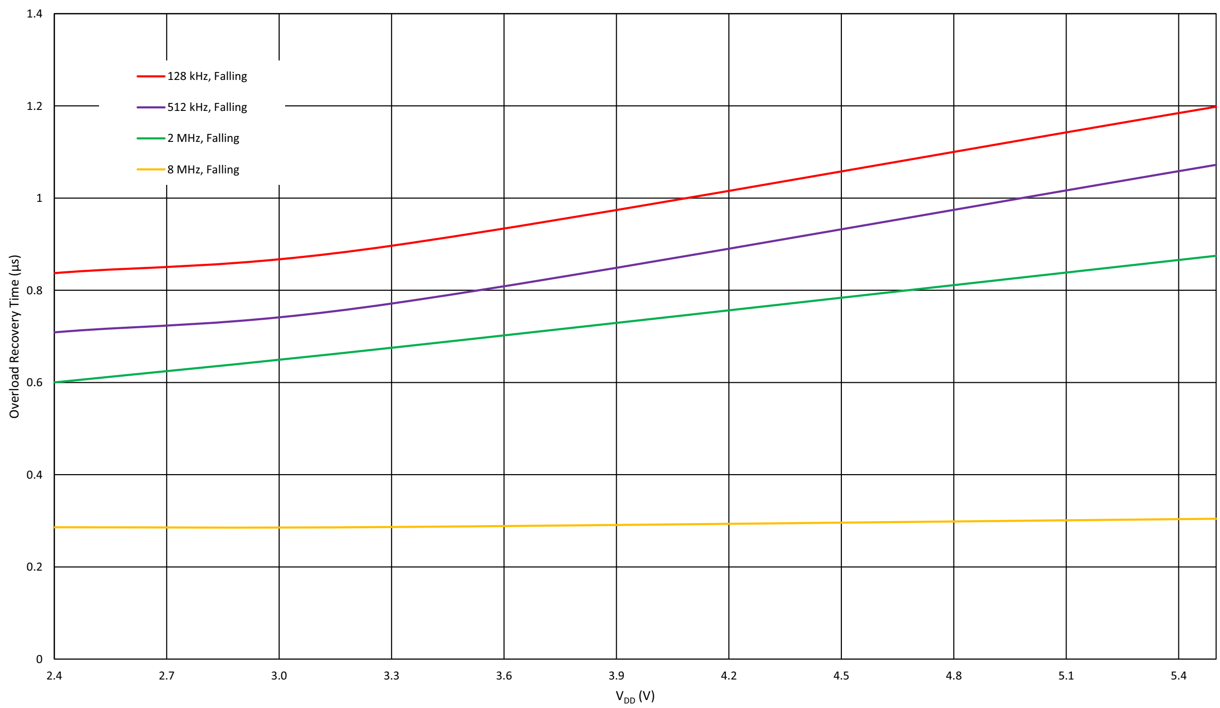


Figure 156. Overload Recovery Time vs. Power Supply Voltage R_L = 50 kΩ; G = 1 V/V, Falling

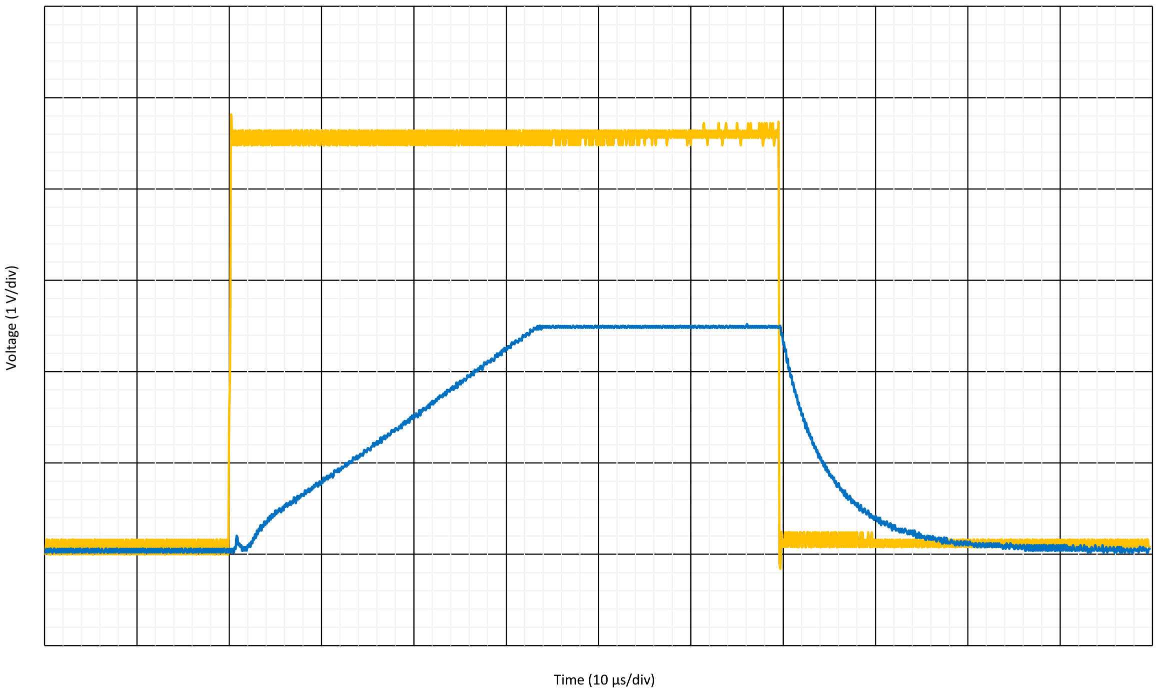


Figure 157. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 128 kHz

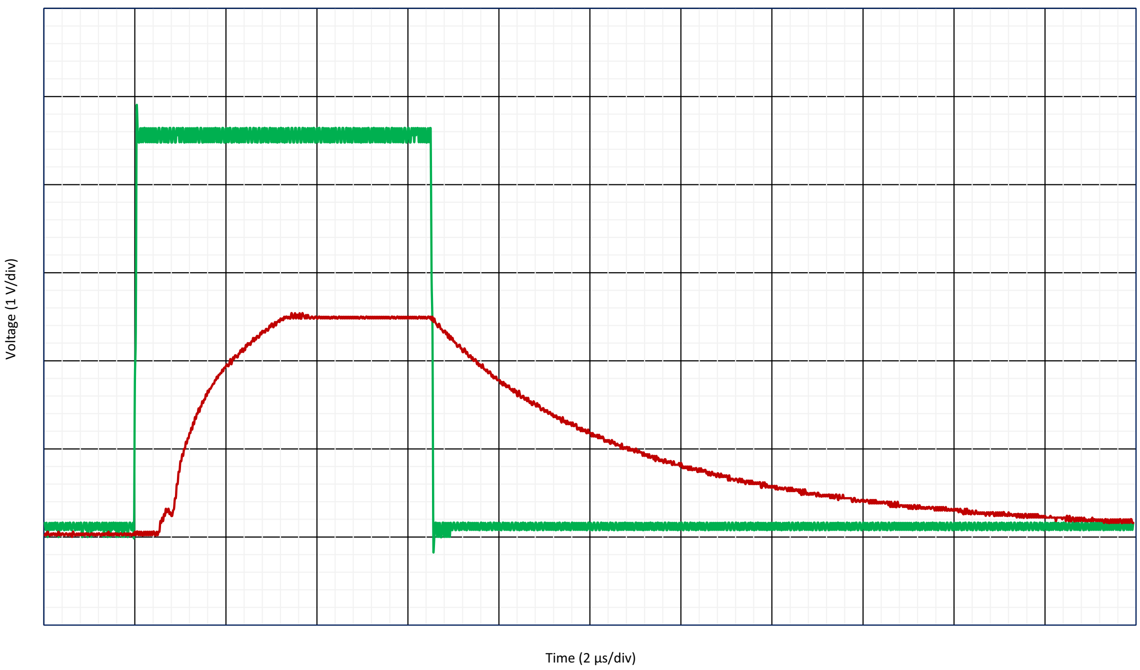


Figure 158. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 512 kHz

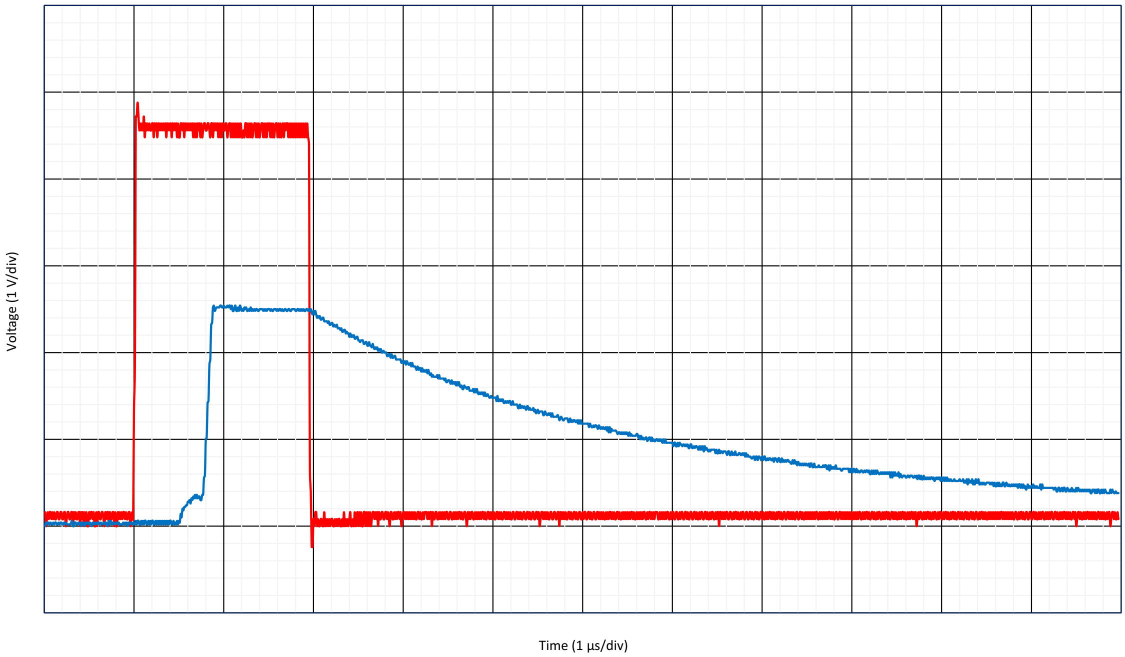


Figure 159. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 2 MHz

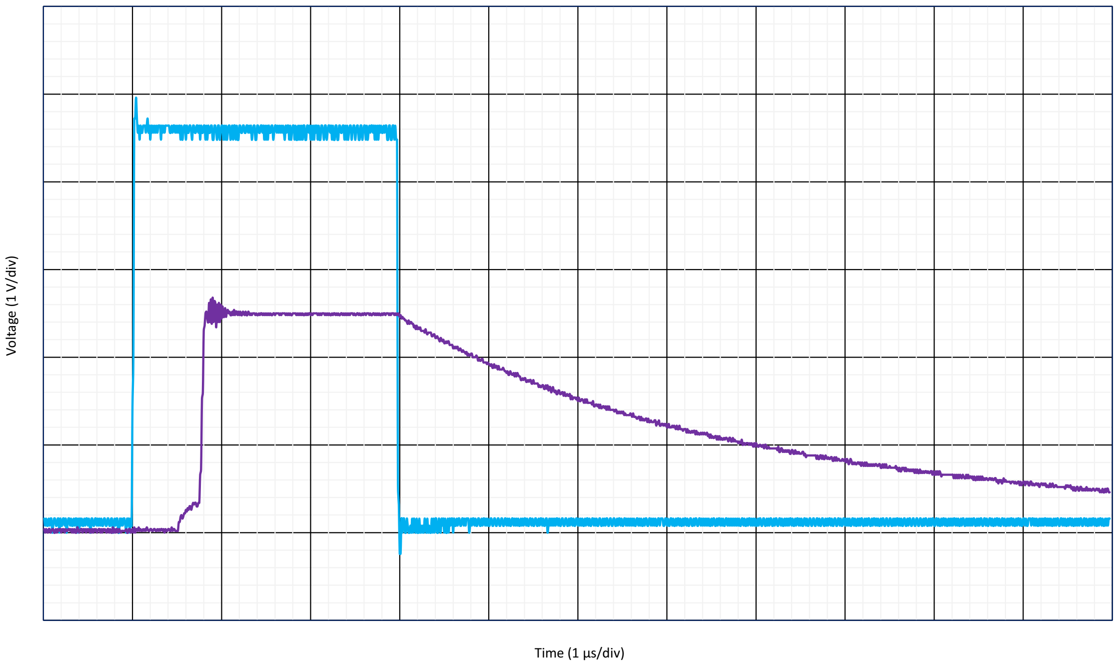


Figure 160. Output Response to Power Down Signal G = 1 V/V; R_L = 50 kΩ; C_L = 20 pF; V_{IN} = V_S/2, BW = 8 MHz

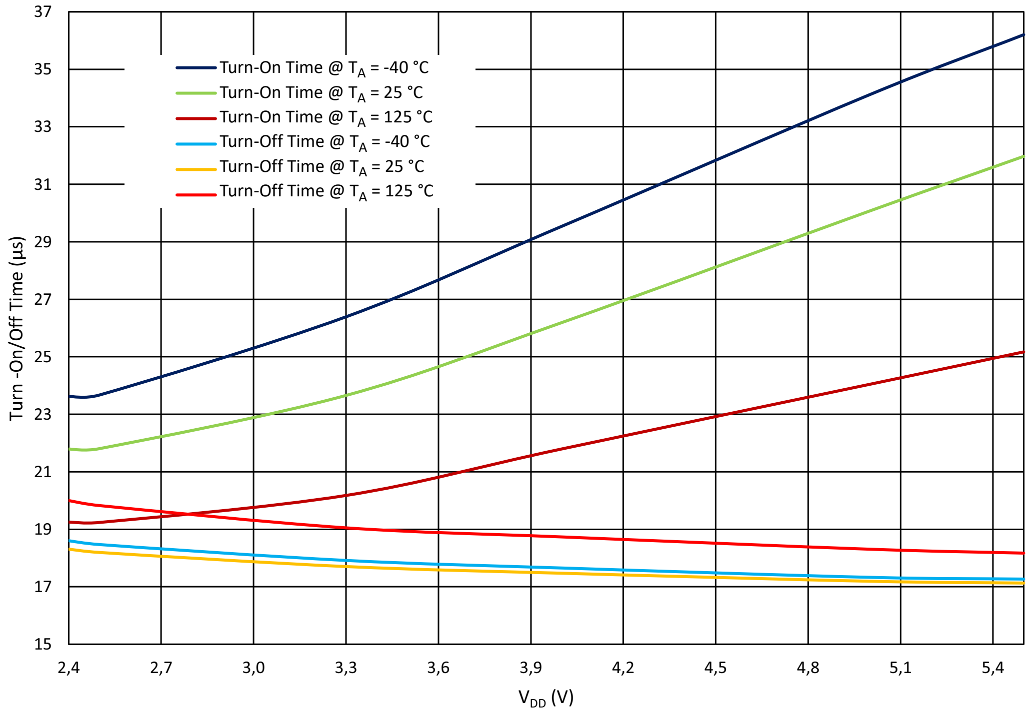


Figure 161. Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 128 kHz

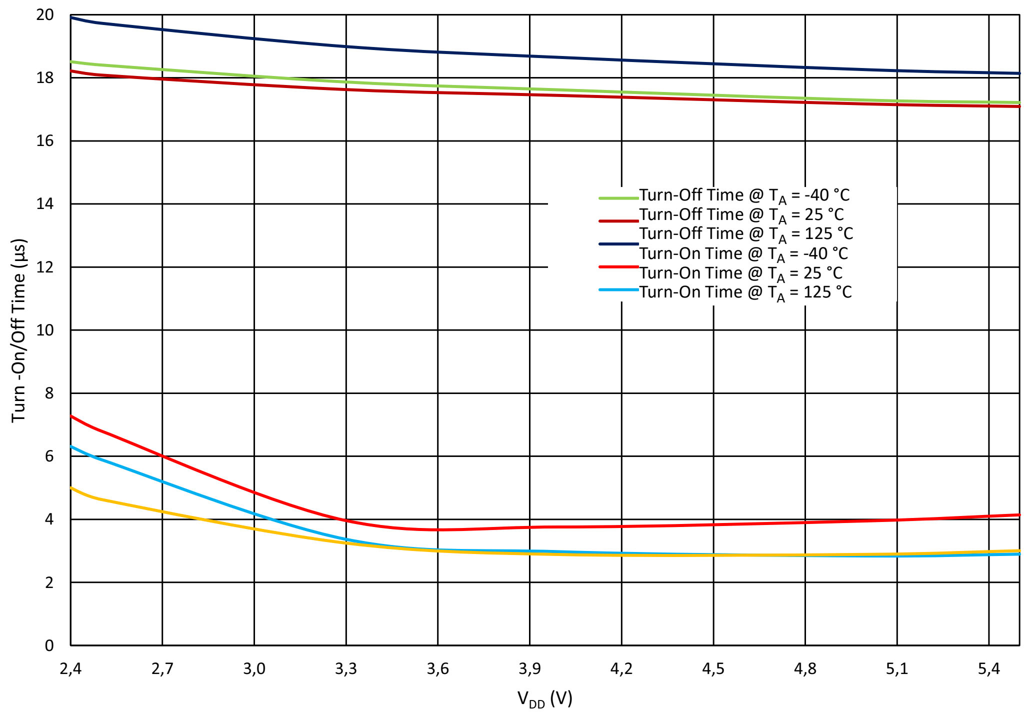


Figure 162. Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 512 kHz

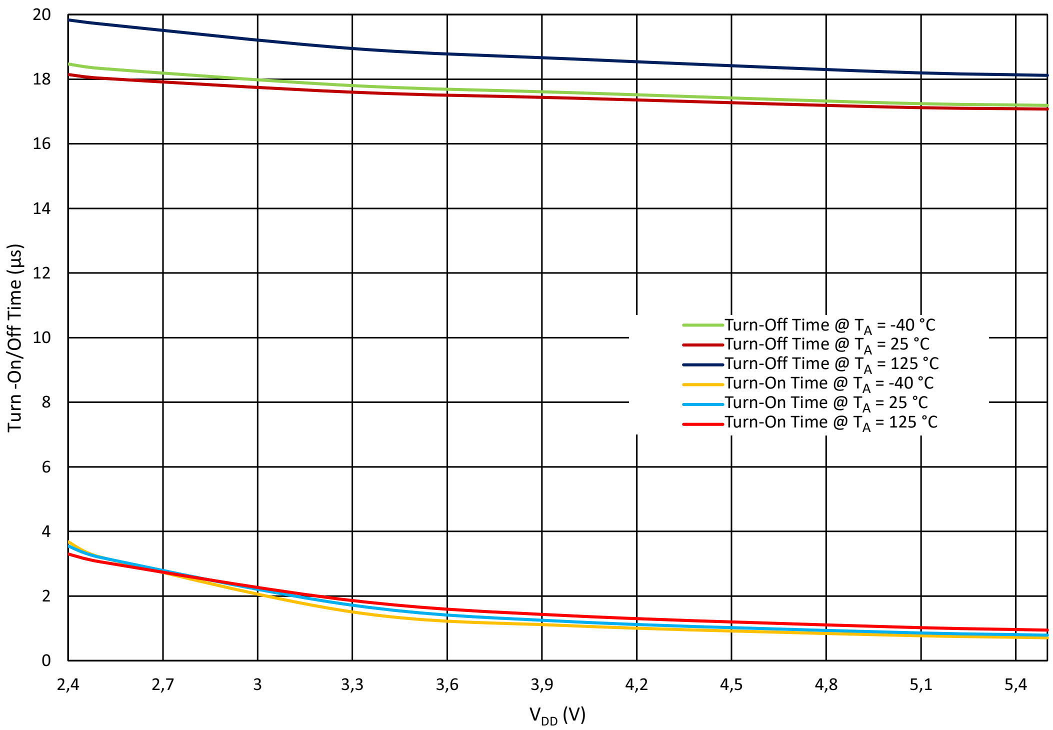


Figure 163. Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 2 MHz

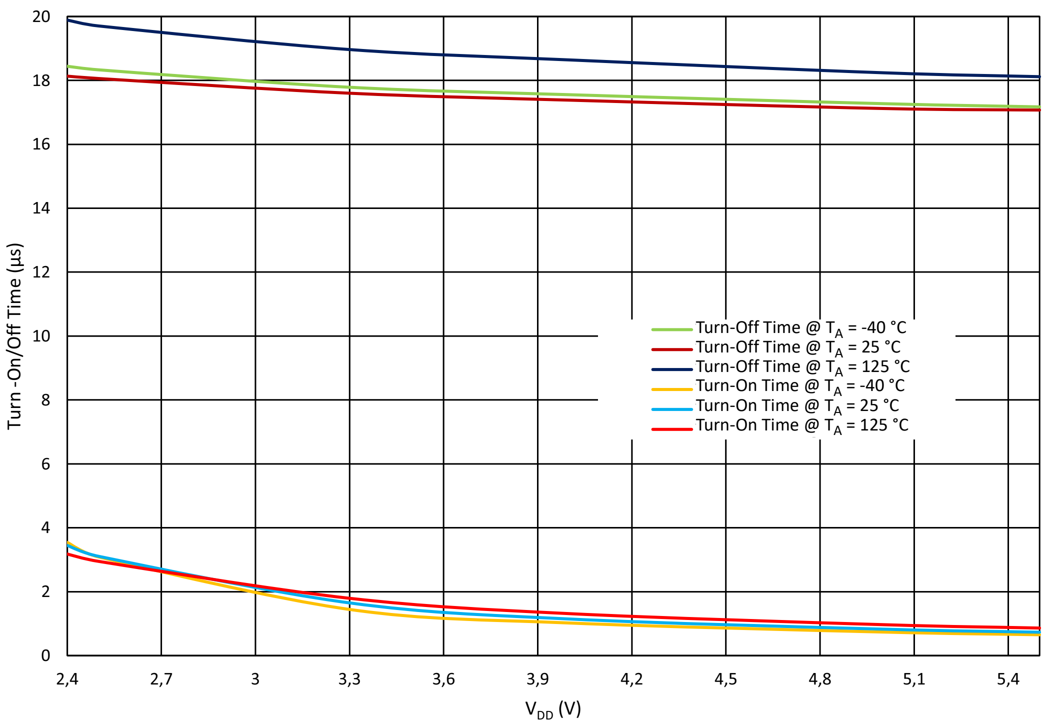


Figure 164. Opampx Turn-On/Off Time vs. V_{DD} at V_{IN} = V_{DD}/2, BW = 8 MHz

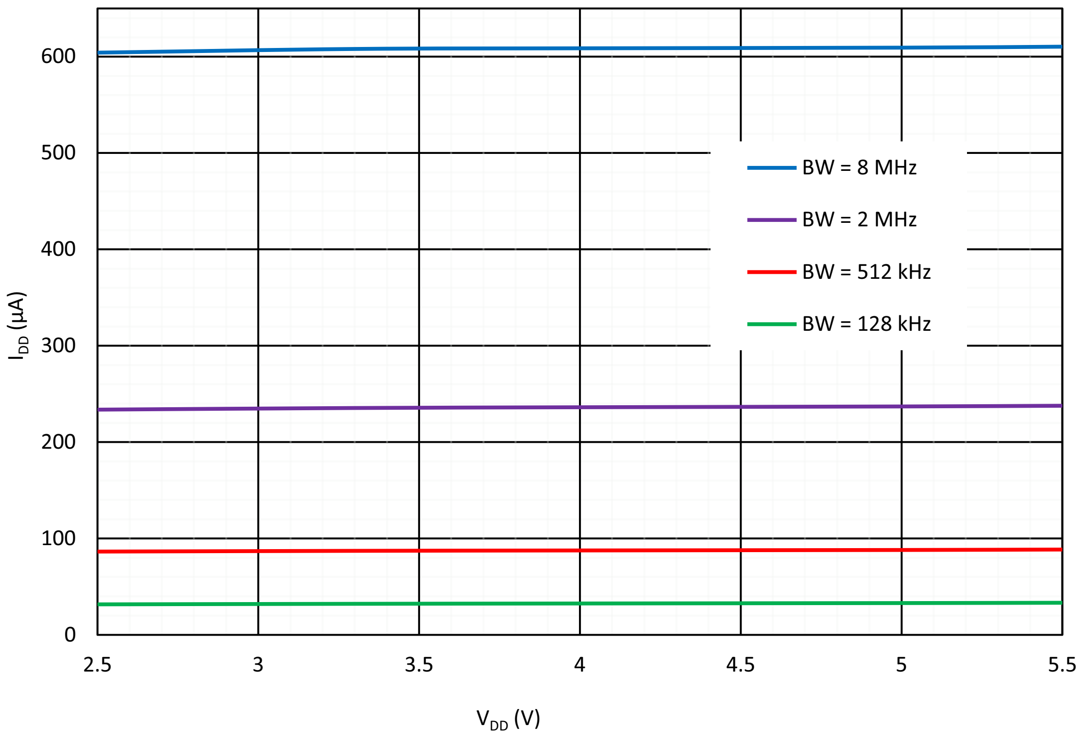


Figure 165. Opamps Quiescent Current Consumption vs. V_{DD}

11. Analog Switch Macrocell

11.1 Analog Switch General Description

The SLG47004-A contains two single-pole/single throw (SPST) normally open analog switches (AS). The structure of the Analog Switches is shown in Figure 166 and Figure 167.

Each analog switch can be controlled from the following sources:

- Connection matrix
- Operational Amplifier macrocell.

Small NMOS (small PMOS) of Analog Switch must be enabled when macrocell is controlled by logic signal from connection matrix. Otherwise, small NMOS (small PMOS) must be disabled when macrocell is controlled by op amp.

Table 59 and Table 60 show possible operation modes of analog switches.

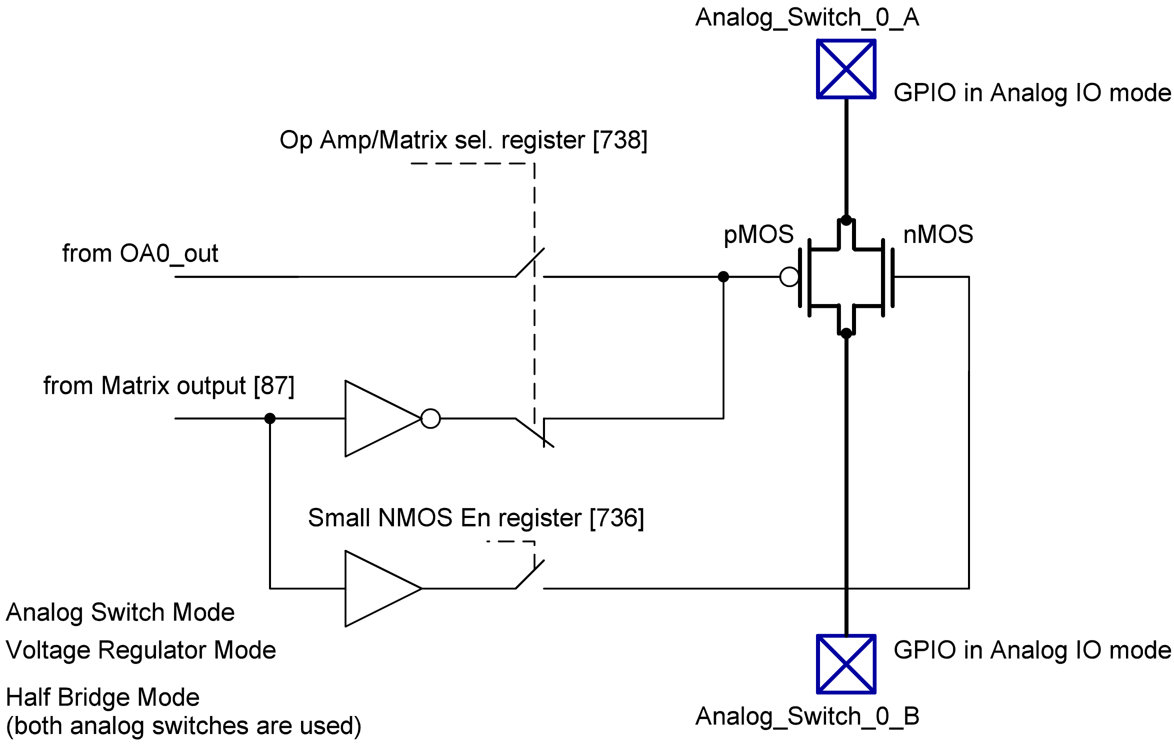


Figure 166. Analog Switch 0 Control Circuit

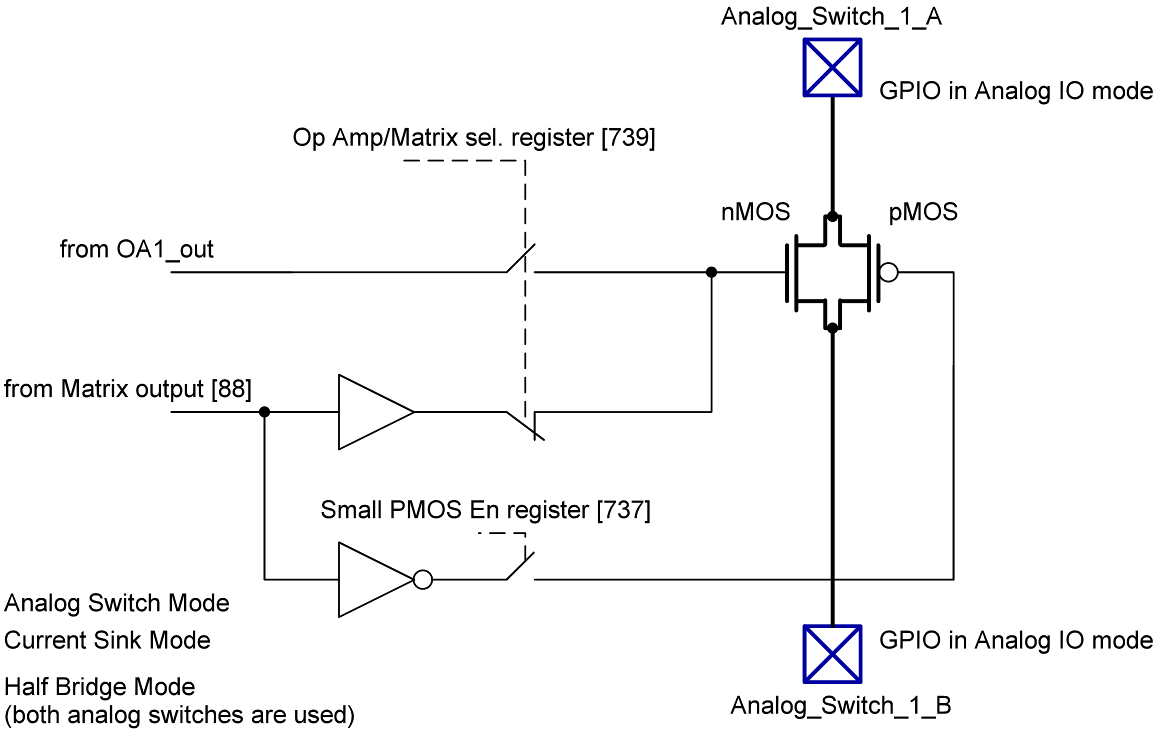


Figure 167. Analog Switch 1 Control Circuit

Table 59. Analog Switch 0 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Register [740]	Matrix Op Amp Control Register [738]	Small nMOS Enable Register [736]
Analog Switch mode with big pMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Voltage Regulator mode	0	1	0
Half Bridge mode with big pMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

Table 60. Analog Switch 1 Modes of Operation

Mode of Operation	Half Bridge Mode Enable Register [740]	Matrix Op Amp Control Register [739]	Small nMOS Enable Register [737]
Analog Switch mode with big nMOS only (control from connection matrix)	0	0	0
Analog Switch mode with all FETs enabled (control from connection matrix)	0	0	1
Current Sink mode	0	1	0
Half Bridge mode with big nMOS only (control from connection matrix)	1	x	0
Half Bridge mode with all FETs enabled (control from connection matrix)	1	x	1

11.2 Half Bridge Mode

Two switches can be externally connected in series to create a half bridge. Please refer to tables Table 59 and Table 60 to enable half bridge mode. Additional logic will be connected to the analog switches to simplify control. Figure 168 shows the half bridge structure with two analog switches.

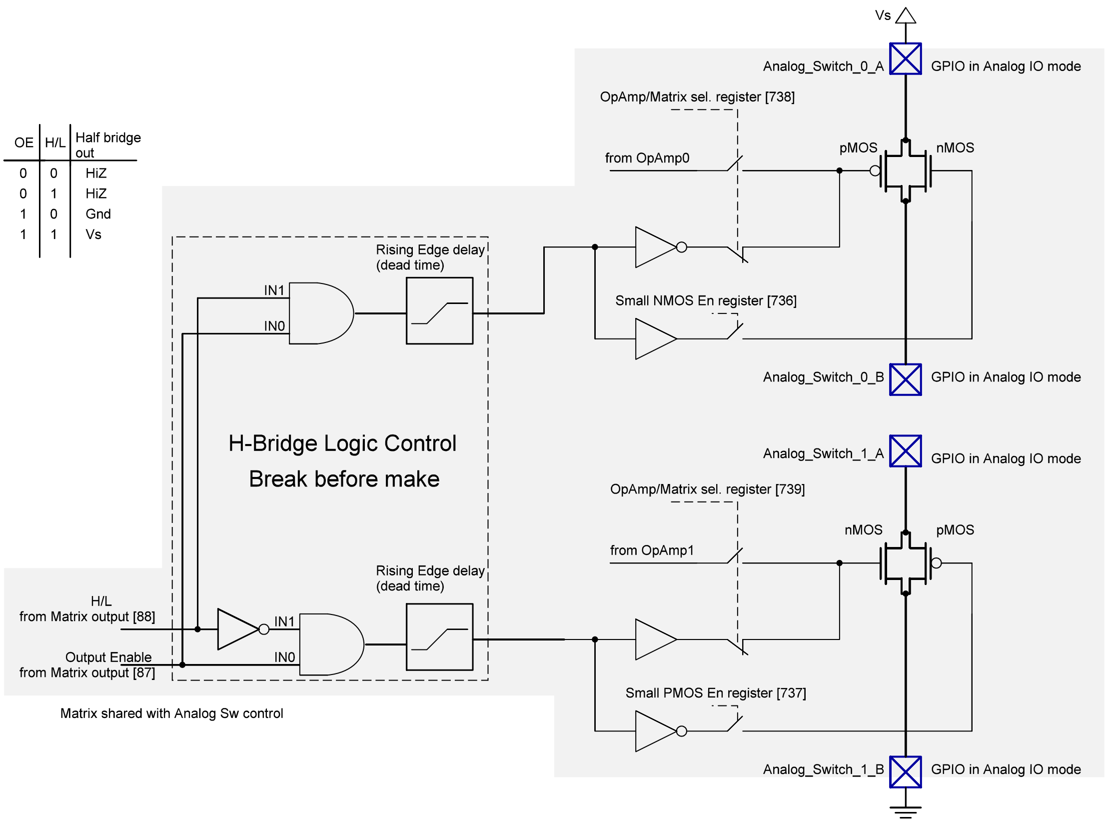


Figure 168. Structure of Half Bridge

11.3 Analog Switches Typical Performance

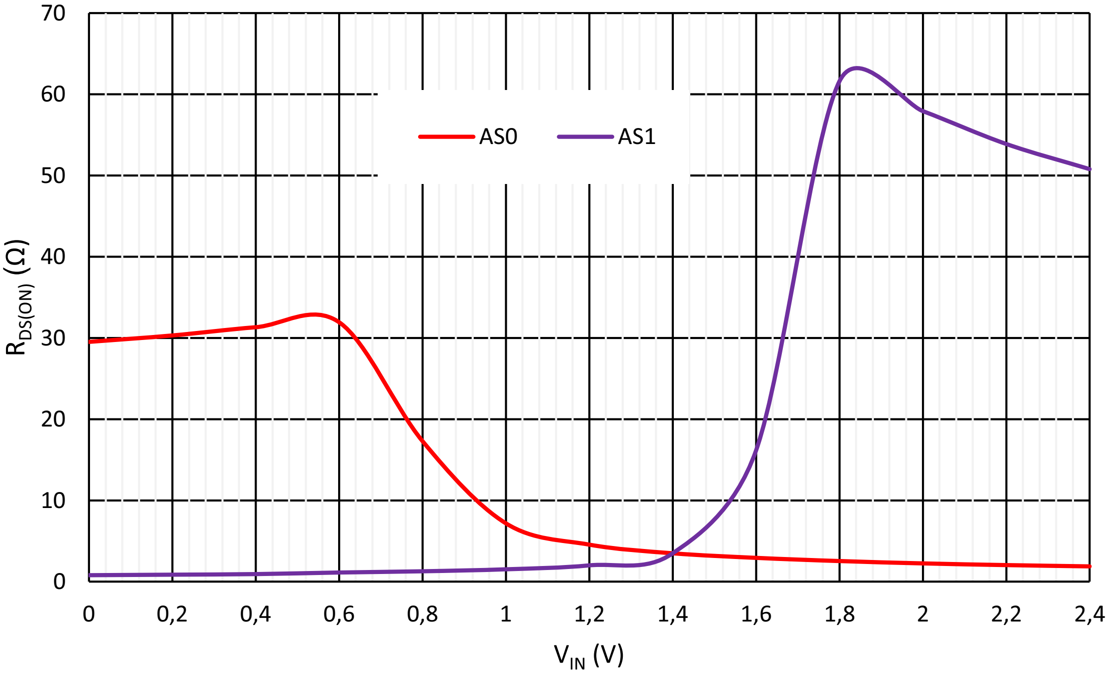


Figure 169. Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA} ,I_{LOAD} = 1 mA, V_{DDA} = 2.4 V

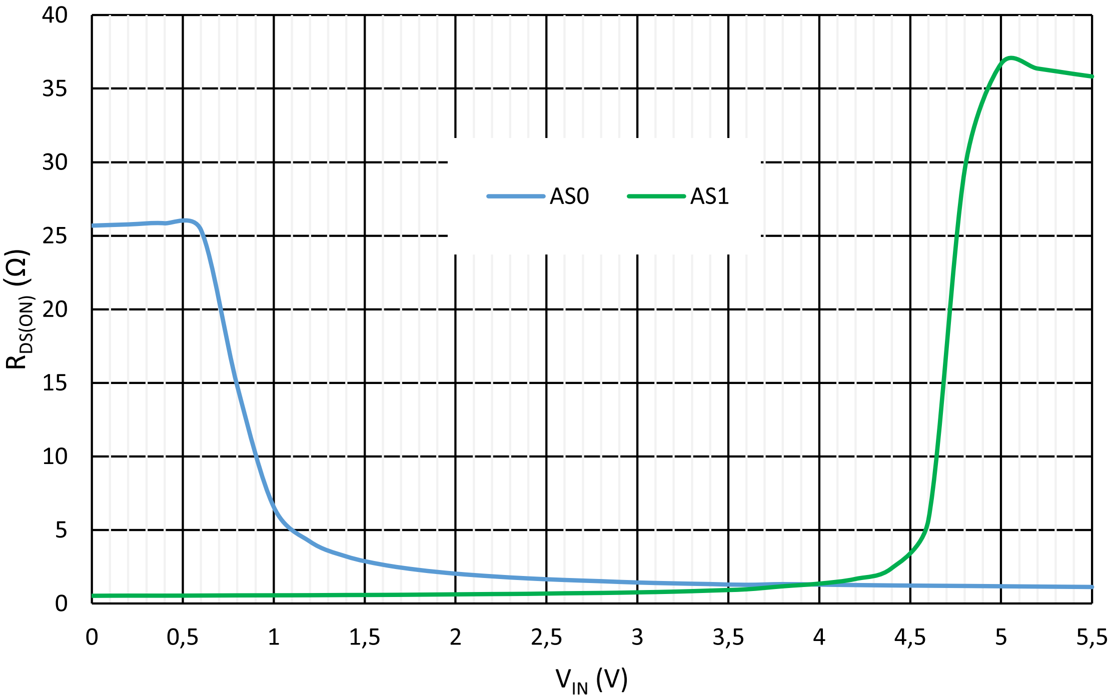


Figure 170. Typical R_{ON} vs. Input Voltage (V_i) for V_i = 0 to V_{DDA} ,I_{LOAD} = 1 mA, V_{DDA} = 5.5 V

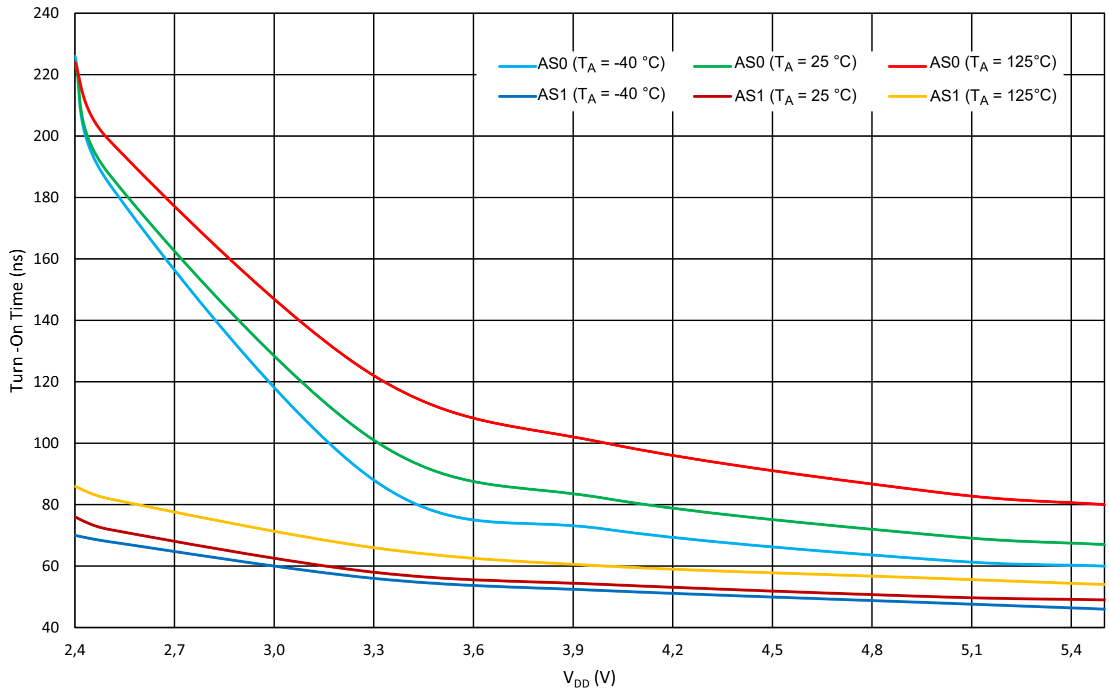


Figure 171. Turn-On Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, V_{IN} = V_{DD}/2

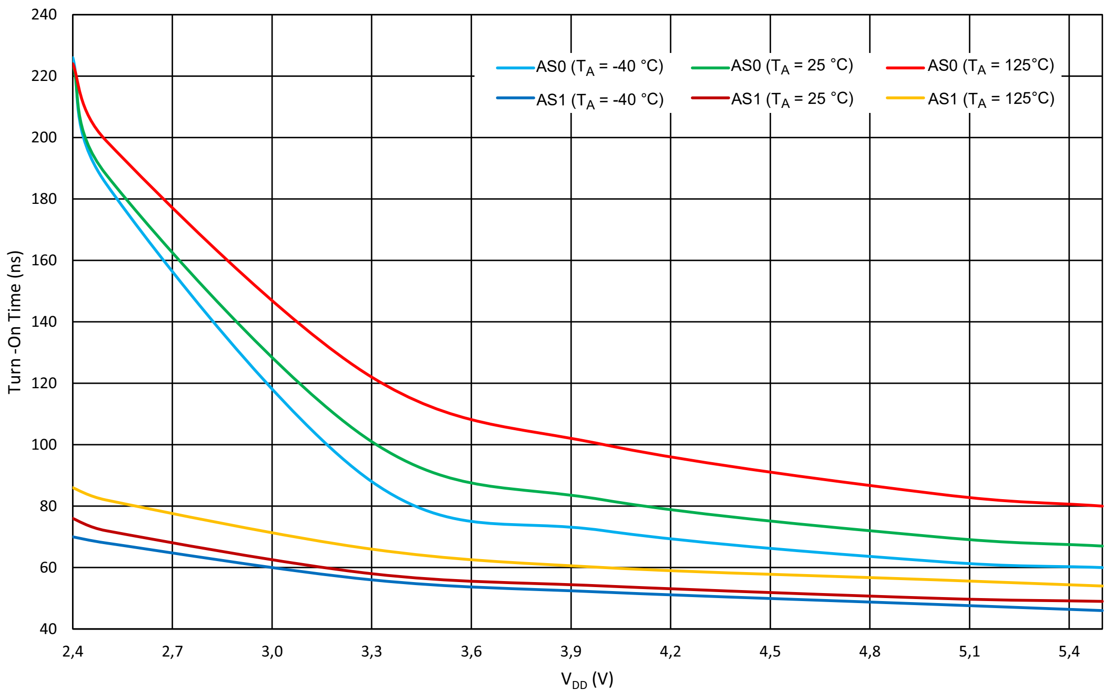


Figure 172. Turn-Off Time vs. V_{DD} at R_{LOAD} = 100 Ω to GND, V_{IN} = V_{DD}/2

12. Digital Rheostats and Programmable Trim Block

The SLG47004-A contains two 10-bit Digital Rheostats. The structure of both macrocells is shown in Figure 173. The range of digital code that corresponds to the rheostat resistance ranges from 0 to 1023 (1024 taps). Code 0 corresponds to the minimum resistance between the RHx_A and RHx_B terminals. As the code value increases, the resistance between the RHx_A and RHx_B terminals monotonically increases. Consequently, when the code value decreases, the resistance between the RH0_A and RH0_B terminals decreases as well (see Section 12.2 Calculating Actual Resistance). The voltage on any rheostat pin can be in the range from AGND to V_{DDA}, as well as be dynamically changed during operation.

To guarantee proper operation of digital rheostats charge pump must be turned on (matrix input [86] must be logic High or registers [912] = 1, [913] = 1). Optionally user can turn off rheostats charge pump to decrease energy consumption. But it's strongly recommended to use the charge pump if V_{DD} < 4.5 V.

The rheostat resistance can be changed in three ways:

- Changing the Rheostat value using the I^2C interface.
- Manually changing the rheostat value using clock and up/down signals, similar to the counter.
- Using the Built-in Auto-Trim mode, where the rheostat value change is done using a special logic based on the signal from the Chopper ACMP.

Each rheostat also has three Switching Speed Modes:

- Regular mode (Register [915] = 0, Register [914] = 0) - up to 1 kHz. In this mode, Low Power Bandgap Chopper Oscillator that oscillates around 120 kHz is used as a source for the charge pump clock. This setting has a lower quiescent current at the expense of a longer recovery time after input voltage spikes.
- Fast mode (Register [915] = 0, Register [914] = 1) - up to 100 kHz. In this mode, the 2 MHz OSC is used as a source for the charge pump clock. This setting has a faster recovery time for input voltage spikes at the expense of a larger quiescent current. Please note that this selection forces On the OSC1 (2.048 MHz).
- Auto Selection (Register [915] = 1, Register [914] = either) when trim is used. When Auto-Trim is active, the fast mode is used. After the Auto-Trim process completes, the regular mode is used.

Note: The maximum switching speed can be achieved if no external capacitive load is connected to the rheostat terminals.

The Programmable Trim (PT) blocks of rheostats macrocell contain analog MUXs, digital MUXs, Chopper ACMP, and additional logic. The two analog MUXs (M1 and M2) and the Chopper ACMP are both shared between the two rheostats. All analog and digital MUXs are set by NVM bits and can be overwritten with I^2C.

The M_CK0 and M_CK1 MUXs select the clock source from internal pre-dividers of the internal oscillators or from the connection matrix. The internal clock sources for the rheostats are OSC0, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144, OSC1, OSC1/8, OSC1/64, and OSC1/512. The PT blocks of the rheostat use the same clock scheme as Counter/Delay Macrocells (refer to Section 16.5 CNT/DLY Clock Scheme). M_CH0 and M_CH1 select the Chopper comparator or a matrix output as the signal source for the main rheostat up/down counter direction. The output of the Chopper ACMP is connected with the Up/Down inputs of the PT blocks by default. The output of the Chopper ACMP can be optionally inverted by setting register [882] to “1”.

M1 MUX selects the input for the Chopper comparator to be connected either internally to one of 3 integrated op amps (Op Amp0 out, Op Amp1 out, In Amp Out) or externally to a PIN. M2 MUX is simplified symbol of Chopper ACMP reference selection blocks. The Chopper ACMP reference ("-" input) can be: analog signal from pin, divided internal Vref voltage (6-bit divider), or divide V_{DDA} voltage (6-bit divider). In Auto-Trim mode each of Rheostats has it own settings for Chopper ACMP inputs. For more information about Chopper ACMP Vref see Section 9.3 Chopper Analog Comparator.

The power-up signal for the Chopper ACMP can be handled either by matrix output signal or Set0/Set1 signal from the PT macrocell. In Auto-Trim mode (Auto_Cal _Dis_RHx NVM bit = 0) additional internal logic enables the clocking of the corresponding PT macrocell counter and disables clocking when one of the stop conditions is reached. See a detailed description in Section 12.3 Trimming Process Using Programmable Trim Block. In Figure 173 when Auto_Cal _Dis_RHx NVM bit = 0 (Auto-Trim mode is enabled), the clocking pulses for the internal PT macrocell counter are under control of additional logic. When Auto_Cal _Dis_RHx NVM bit = 1 (Auto-Trim mode is disabled), all additional logics (Set signal, internal Set signal, Idle/Active signal) operate the same way, but clock pulses are always enabled and generated externally by the user. Calibration channel can be selected automatically (1st channel is channel 0, second channel is channel 1) or can be set manually by registers [893:892].

The inputs of Chopper ACMP can be reconfigured while operating in Auto-Trim mode. There is one configuration of inputs (M1, M2 configuration, Figure 173). for the case when Set0 signal is latched, and another configuration of M1, M2 MUXs when Set1 signal is latched. For example, M1 MUX can be configured to operate with In Amp out when Set0 is latched and Chopper_ACMP+ pin when Set1 is latched. The same way, M2 can be configured to work with any of M2 inputs when Set0 or Set1 are latched. Note that the default configuration is the configuration for Set0 signal. When Chopper ACMP operates as separate ACMP and Auto-Trim function is disabled, M1 and M2 MUXs operates with configuration for Set0 signal.

Keep in mind that two Auto-Trim processes cannot be done simultaneously. When the Auto-Trim process for one rheostat is active, all signals on the Set input for another rheostat will be ignored. See a detailed description in Section 12.3.1 Trimming Process with Auto-Trim Option Enabled. The initial user defined value of Digital Rheostat resistance can be programmed into the NVM. The initial value will be loaded during the Power-On event and this value will be used as the initial rheostat resistance, as well as a starting point for count down or count up.

Both read and write operations are allowed for rheostat resistance value, stored in NVM. Also, both read and write operations are allowed for current rheostat resistance value. RH0 read operation - registers [1561:1552], write operation - registers [1545:1536]. RH1 read operation - registers [1689:1680], write operation - registers [1673:1664].

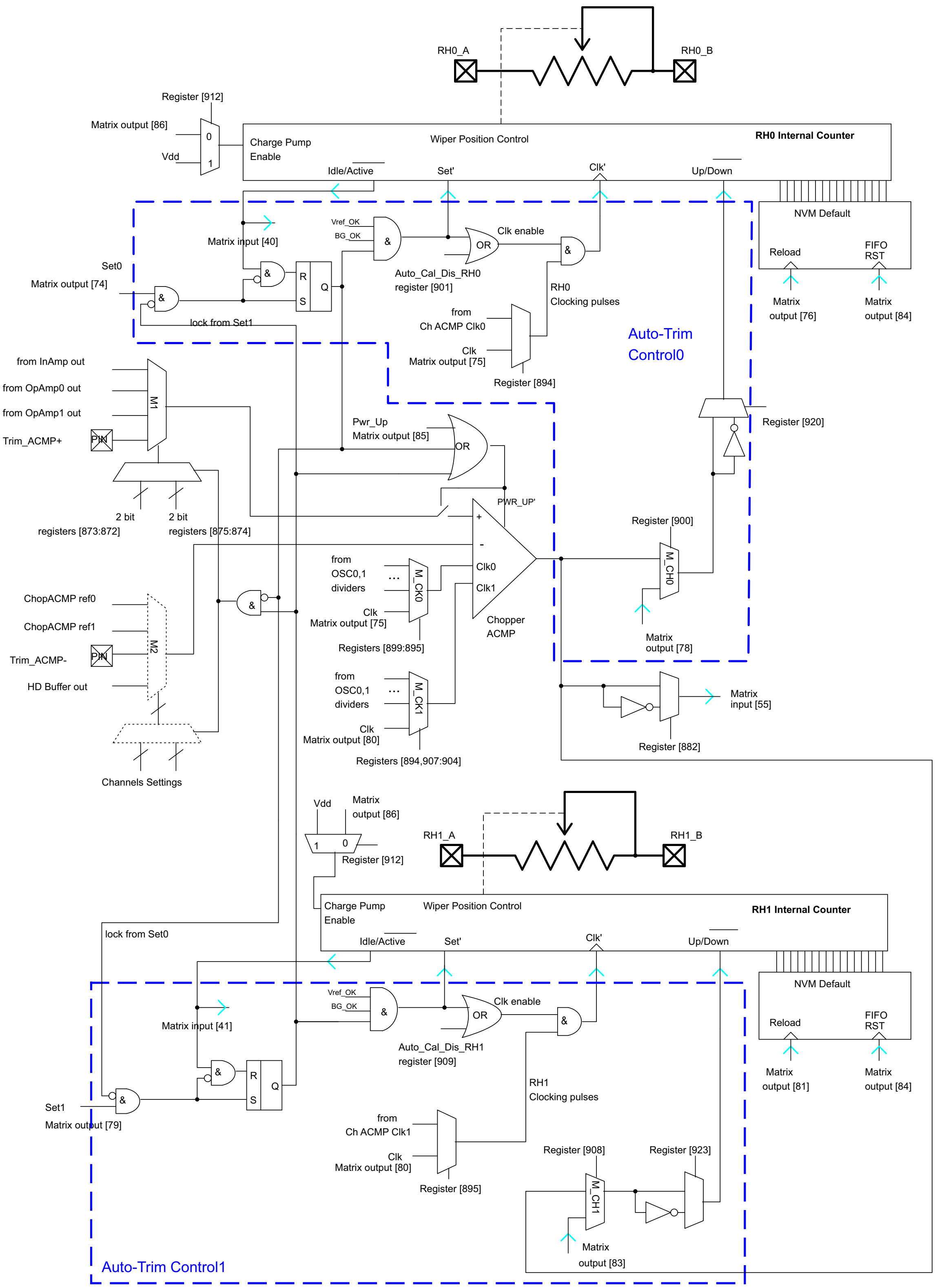


Figure 173. Programmable Trim Blocks and Digital Rheostat's Internal Circuit

PT macrocell signals:

- "Set": external Set signal begins the Auto-Trim process when Auto_Cal _Dis_RHx bit is cleared (registers [901]). Otherwise, this signal has no effect. The behavior of the PT macrocell in Auto-Trim mode is described below.
- "Reload": when Reload goes high the rheostat value stored in the NVM will be loaded into the rheostat (Register and Counter) overwriting any current setting. This signal is edge sensitive. It has no effect while the Auto-Trim procedure is active.
- "Clock": this input has the following options: the PT macrocell can be clocked internally or from matrix. When clocked internally, the clock is automatically enabled/disabled by the Set input logic in Auto-Trim mode. The internal clock is synchronized with the Chopper ACMP clock.
- "Up/Down": the rheostat counter counts up when the signal is High and down when the signal is Low.
- "Idle/Active": this is the connection matrix input, that is logic HIGH by default. It goes LOW with rising edge on SET input if Auto-Trim mode is enabled (Auto_Cal _Dis_RHx NVM bit = 0). After the end of Auto-Trim procedure (one of stop conditions occurs) this signal sets to logic HIGH again.
- "FIFO nReset": low level at this input clears internal FIFO buffer for commands Reload for both rheostats. User should provide high logic level at this input for the normal rheostat operation.

There is also an overflow protection option, for which the counter will stop counting up when the maximum value (0x3FF) is reached or stop counting down when the minimum value (0x00) is reached. The digital rheostat is initialized/powered in the first place. The rheostat value is Hi-Z (or highest resistance if it is impossible to disconnect the rheostat) during the Power-On sequence.

12.1 Potentiometer Mode

This mode allows two 2-pin rheostats to work as one 3-pin potentiometer. When this mode is active (register [917] = 1), user changes the value of RH0 internal counter. In this mode, the value of RH1 counter is the inverted value of RH0 counter (Figure 174). Note that the RH0_B pin and the RH1_A pin must be connected externally. Also, note that the Auto-Trim function isn't allowed in Potentiometer Mode.

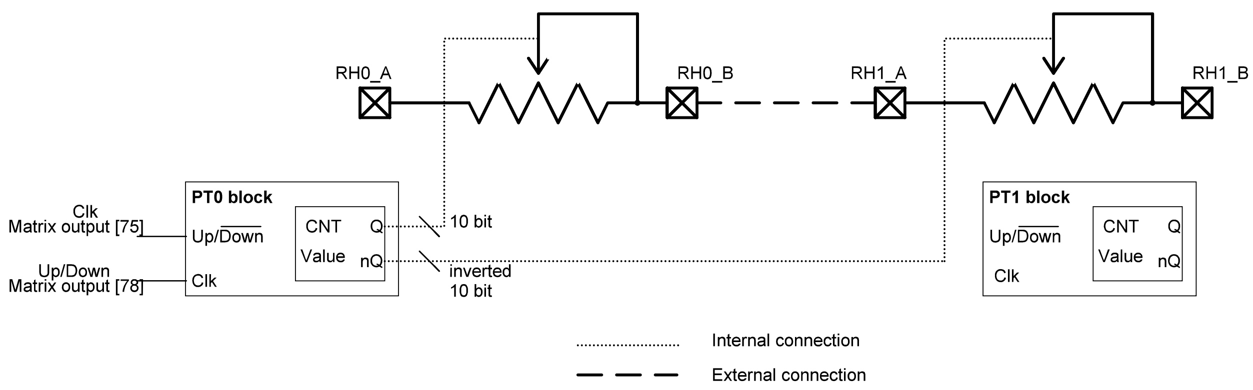


Figure 174. Rheostats in Potentiometer Mode

12.2 Calculating Actual Resistance

In applications where the absolute rheostat resistance is critical, the user can calculate it using the rheostat tolerance data, the minimum rheostat resistance, and the desired code.

The 16-bit tolerance data for both rheostats has been programmed into registers 0xE6 to 0xE9. These registers can be used to calculate the total rheostat resistance. The 16th bit defines the sign (0 = +, 1 = -) of the tolerance.

The other fifteen bits correspond to the absolute value of the rheostat tolerances variation from 100 kΩ measured at 25 °C.

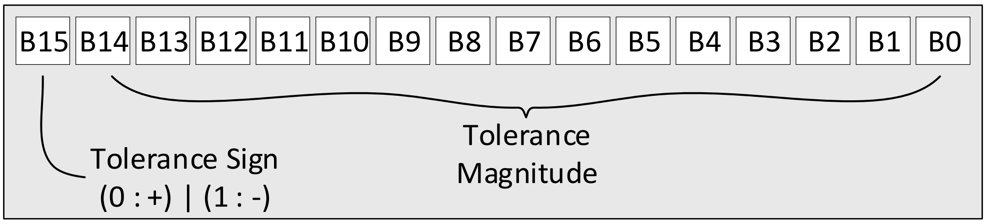


Figure 175. Rheostat Tolerance Registers

Note that the rheostat tolerance data is programmed into registers 0xE6 to 0xE9.

The rheostat value at a given code depends on the total digital rheostat resistance. The equations below can be used to calculate the rheostat resistance.

$$R_{Code} = (R_{DR} - R_{DR\ MIN}) \times (code/1023) + R_{DR\ MIN}$$

$$R_{DR} = 100 \times 10^3 + (sign_{RH\_Tolerance} \times R_{RH\_Tolerance})$$

where:

R_{Code} - Rheostat Resistance at a Given Code

R_{DR} - Total Digital Rheostat Resistance

$R_{DR\ MIN}$ - Minimum Rheostat Resistance

code - Rheostat Position Ranging from 0x000 to 0x3FF

$sign_{RH\_Tolerance}$ - the MSB of the Rheostat’s Tolerance Data

$R_{RH\_Tolerance}$ - the 15 LSBs of the Rheostat’s Tolerance Data.

For example, let's say that 0x2B67 has been written into the rheostat tolerance registers within the GreenPAK's NVM. B15 corresponds to a positive sign while B14:0 translates into a decimal value of 11111. R_{DR} calculates to approximately 111,111 Ω and can be used with the minimum rheostat resistance to calculate the resistance at a given code. Note that the minimum rheostat resistance must be measured to obtain precise results, but a range is provided in Table 27.

12.3 Trimming Process Using Programmable Trim Block

There are several ways of implementing the trimming process using the PT block. One of the essential features of the PT macrocell is the Auto-Trim function described below. It allows the user to design simple calibration circuits for a wide variety of applications.

12.3.1 Trimming Process with Auto-Trim Option Enabled

For using the Auto-Trim function the following preliminary steps must be taken:

- Clear Auto_Cal _Dis_RHx NVM bit (0 is default value). This enables Auto-Trim function.
- Configure M1 MUX (registers [875:872]). It can be user system voltage feedback. If Auto-Trim function is used for two rheostats, M1 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched).

- Configure M2 MUX. It can be user desired set point threshold. If Auto-Trim function is used for two rheostats, M2 MUX must be configured for both rheostats (for cases when Set0 is latched and when Set1 is latched). Remember, that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks.
- Configure M_CH0 (M_CH1) MUX to work with Chopper ACMP (M_CH0,1 MUXs are configured to work with Chop ACMP by default).
- Configure inverting or non-inverting Chopper ACMP output (registers [923], [920] and [882]).
- Select clock source (internal clock from internal pre-dividers or from connection matrix). Note that in Auto-Trim mode clock source frequency for the PT Block is limited by the Chopper Comparator time response. Therefore, the clock source frequency must not be greater than <f_{ChACMP}> kHz.
- Start the Auto-Trim process by setting the Set0 (Set1) input of PT block to a High level. The Auto-Trim process stops if one of three stop conditions occur:

  1) 2nd time change on Up/Down input at the moment of rising edge on Clock input (see Figure 176).

  2) the value of rheostat reaches its maximum (1023).

  3) the value of rheostat reaches its minimum (0).

  Stop conditions result in a change of the Idle/Active signal, which resets the internal Auto-Trim logic.

  Note that the Set input is edge sensitive, but if the user keeps a High logic level at this input after reaching the set point, the PT block will continue to operate and continue to switch rheostat around the set point.
- To start new Auto-Trim process user should reapply a High level on Set input.

The detailed flow of Auto-Trim process is shown in Figure 176, Figure 177, Figure 178.

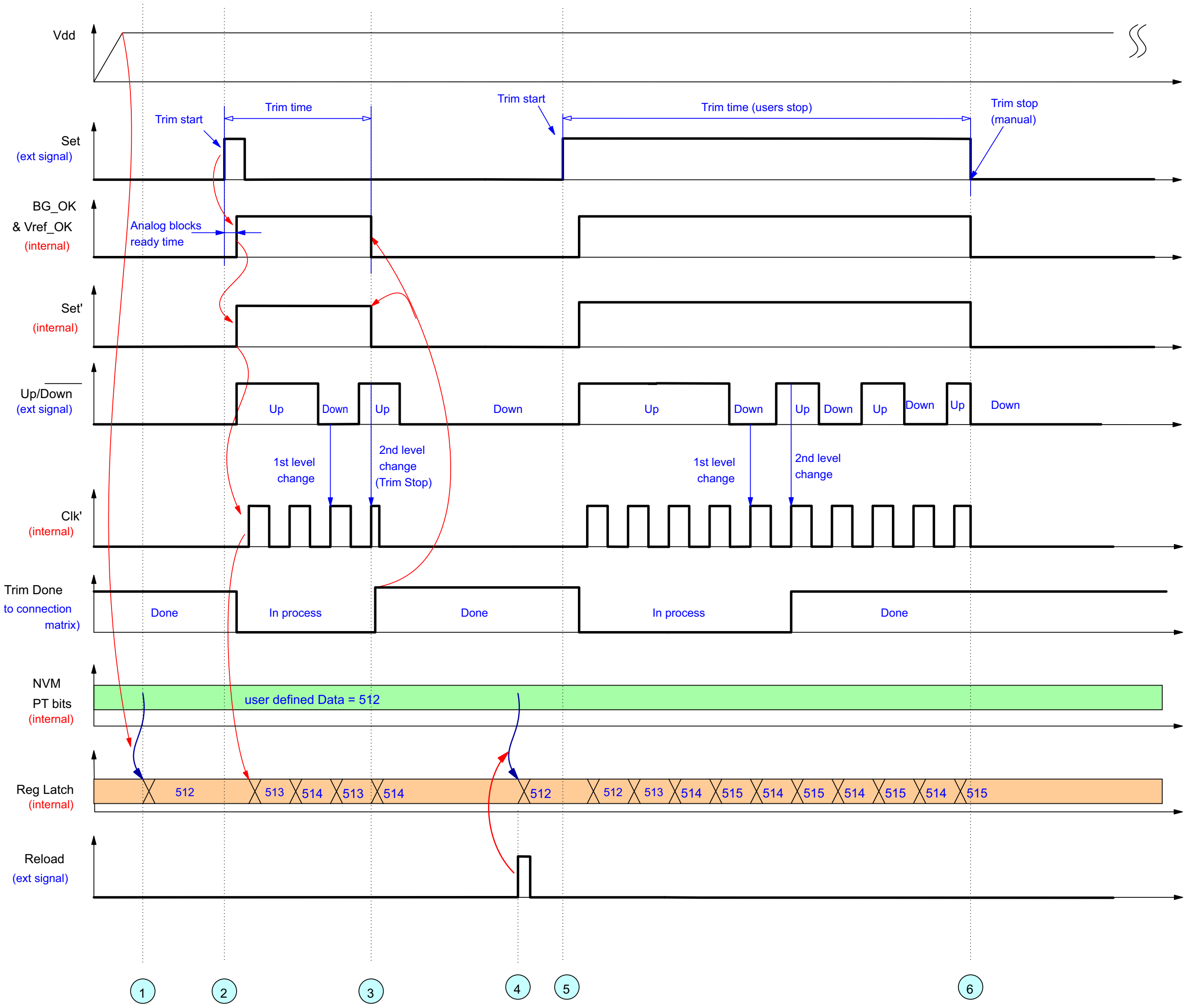


Figure 176. Example of Auto-Trim Process for a Single Rheostat

The key events of the Auto-Trim process are the following (see Figure 176):

1. During the startup event the SLG47004-A loads the rheostat value from NVM to Internal Counter. In this example this value is 512.

2. The Trim process starts with a rising edge on Set input. This Set signal is latched until the end of the Auto-Trim process. The Set signal will enable the Chopper ACMP and the Vref, if they were not enabled earlier. After a ready signal from analog blocks (BG_OK & Vref_OK), the clock pulses for the internal counter are enabled. The counter starts to count up or down depending on the level at the Up/Down input. If user selected the “Internal Clock” option for Clock input, these clock pulses are generated automatically during trim time. Each rising edge of the Clock pulse changes the value of the counter and, consequently, the value of the rheostat.

3. There are three stop conditions for the Auto-Trim process:

1) A subsequent change on Up/Down input at the moment of rising edge on Clock input.

2) The value of the rheostat reaches its maximum (1023).

3) The value of the rheostat reaches its minimum (0).

If the Set input signal is shorter than the trim time, the Auto-Trim process stops automatically after a stop condition occurs (event 3, Figure 176). However, if a stop condition comes and High logic level holds on the Set input, the rheostat value will be switched near the set point until a Low level on the Set input occurs (event 7, Figure 176). Note that the Idle/Active signal changes its level to High (Auto-Trim is done) even if the user keeps a High logic level at the Set input.

After the end of the Auto-Trim process, Chopper ACMP powers down and its output goes to a Low logic level.

4. After a rising edge at the "Reload" signal, the value from NVM is copied to the rheostat Internal Counter overwriting current rheostat settings.

5. During this event user starts Auto-Trim process, but holds High logic level at Set input for a time longer than Auto-Trim process.

6. The Auto-Trim process stops when the signal at the Set input goes to Low level. Note that a logic High level at the Set input was held longer than the time that was needed for the Auto-Trim process.

Figure 177 shows a similar Auto-Trim example. The only difference is that the user defined clock source as "External clock" from connection matrix. The clock pulses are present at the Clock input all the time, but have effect (rheostat value changes) during Trim time only. The stop condition for this case is the following: PT block reaches boundary value of 1023 and the logic level at change Set input is Low.

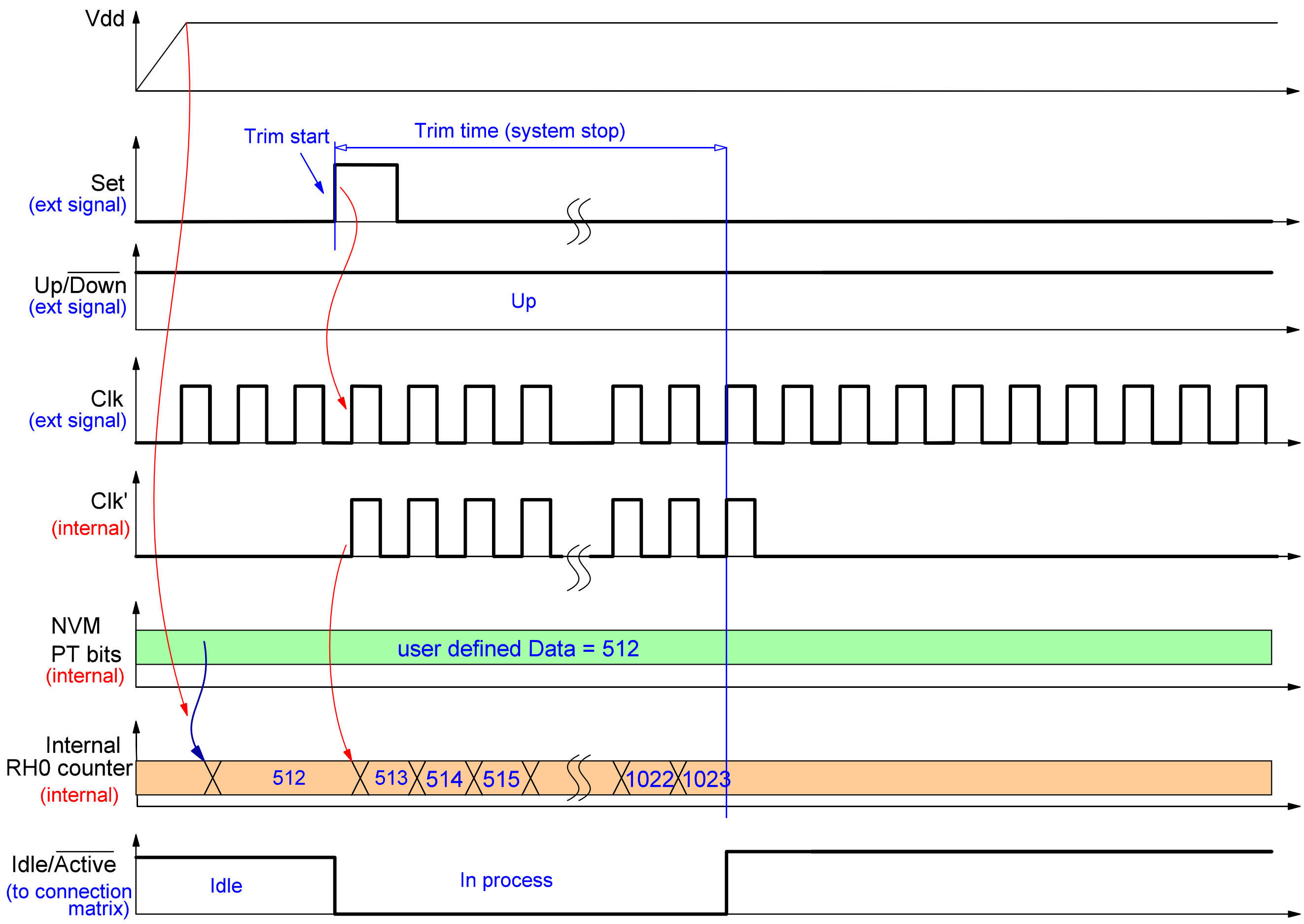


Figure 177. Example of Auto-Trim Process with External Clock Signal

Figure 178 shows Auto-Trim process flow for two rheostats.

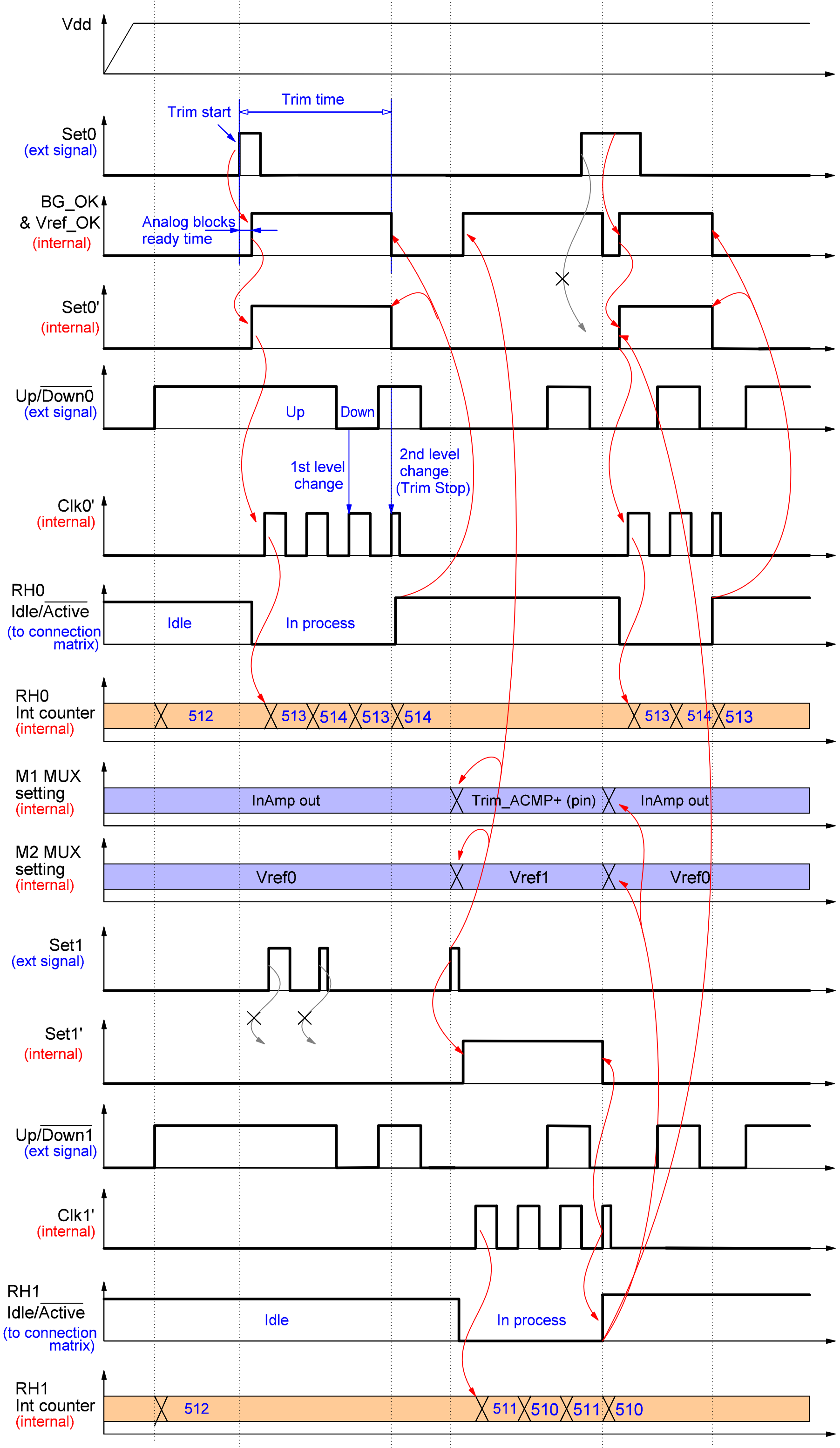


Figure 178. Example of Auto-Trim Process for Two Rheostats

12.3.2 I²C Controlled Trimming Process with Auto-Trim Option Enabled

It's possible to start the Auto-Trim process via I²C interface. In this case the user must configure the SLG47004-A PT macrocell as described in Section 12.3.1 Trimming Process with Auto-Trim Option Enabled. To start the Auto-Trim process via I²C interface the user can use I²C virtual inputs.

Also, an external I²C master device can force the SLG47004-A to reload the rheostat value from NVM ("Reload" command).

See Figure 179 for an example of the Auto-Trim process under external I²C master control.

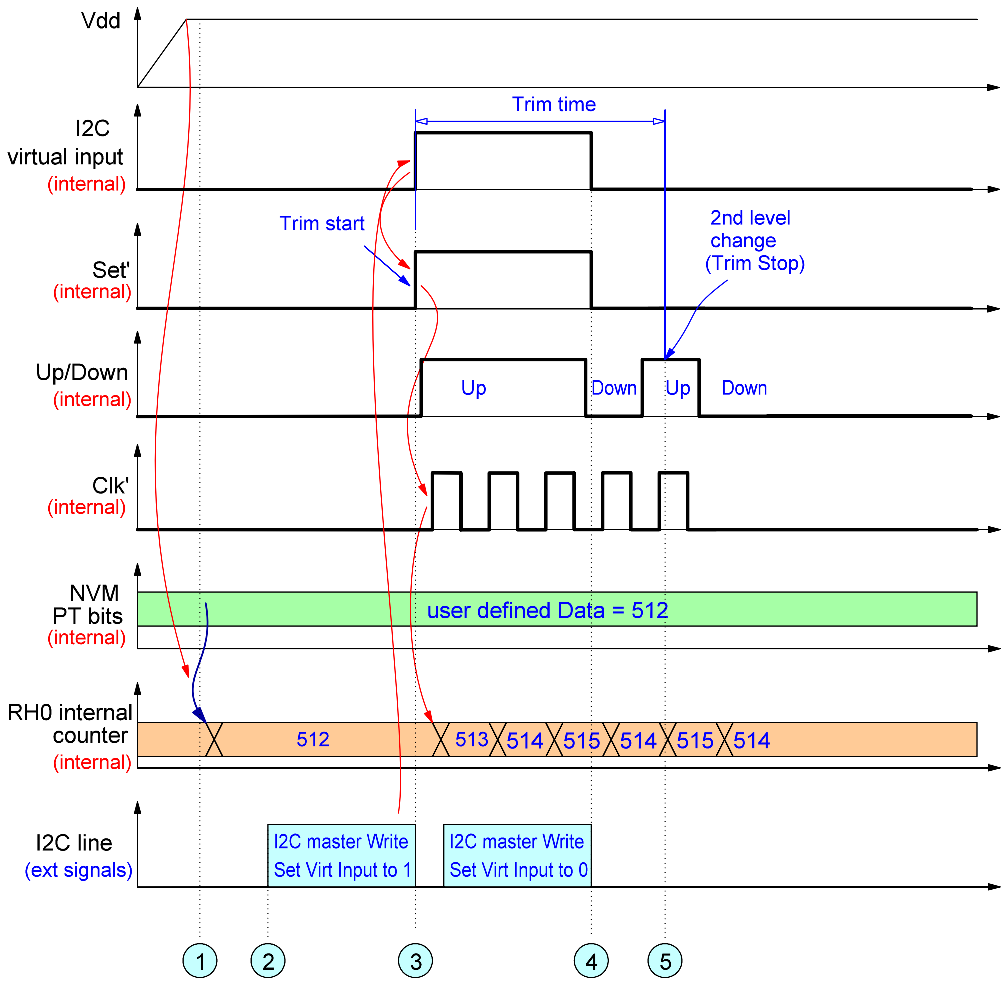


Figure 179. Example of Auto-Trim Process via I²C

The key events of the Auto-Trim process under external I²C master control are as follows:

1. During the startup event the SLG47004-A loads the rheostat value from the NVM to the Internal Counter. In the example this value is 512.

2. I²C master sends the message to set High one of the I²C virtual inputs that is connected with Set input of the PT macrocell.

3. After the I²C message is received and processed, the I²C virtual input and the Set input will be at a High logic level. The Auto-Trim process begins.

4. I²C master clears the virtual input and, consequently, the Set input. The Auto-Trim process goes on until a trim stop condition occurs.

5. The Auto-Trim process ends. The stop condition in this example is a 2nd change on Up/Down input at the moment of rising edge on the Clock input and Low level at the Set input.

12.3.3 Changing Rheostat Value Directly via I2C

The user can perform their own trim algorithm setting the rheostat value directly via I2C interface. In the example below, a microcontroller uses a user defined trim algorithm to change SLG47004-A's rheostat via I2C interface (Figure 180). Note that during Auto-Trim process SLG47004-A will return nACK, if master tries to get access (both read and write) to rheostats registers via I2C.

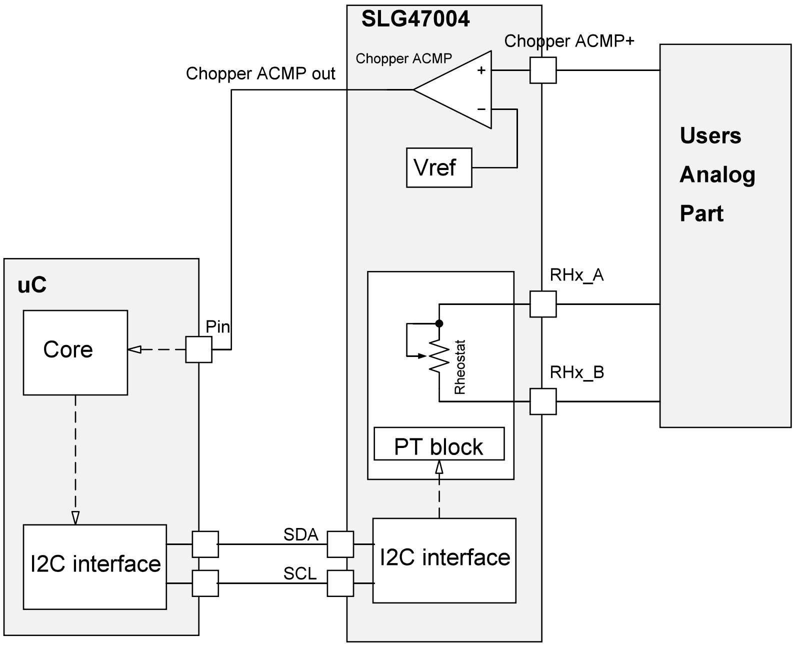


Figure 180. Example of Hardware Configuration

Note that the PT Registers are allowed to read and write via communication interface, if not protected.

The preliminary configuration of system shown in Figure 180 is the following:

- Auto_Cal _Dis_RHx bit is set to 1 (disable Auto-Trim mode).
- M1 MUX (registers [875:872])) is configured to work with user system voltage feedback (pin Chop_ACMP+).
- M2 MUX is configured to work with SLG47004-A programmable Vref. Note that M2 MUX is simplified symbol of Chopper ACMP reference selection blocks (see Section 9.3 Chopper Analog Comparator).
- Chopper ACMP is powered up from connection matrix. Chopper ACMP out is connected to output pin.
- No Clock source for PT block.

The example of a system trim via I2C is shown in the figure below. In this example the I2C master uses a simple approximation algorithm for reaching the set point. Every next step the rheostat code is changed by ±(Previous rheostat code step value/2). The sign depends on the Chopper ACMP output. The algorithm steps are as follows:

- Set rheostat code to 1024/2 = 512.
- Wait until the system settles down and check if Chopper ACMP output = 1, then Next_rheostat_code = 512 + (512/2). If Chopper ACMP output = 0, then Next_rheostat_code = 512 - (512/2).
- Repeat previous step until Next_rheostat_code = Prev_rheostat_code ± 1.

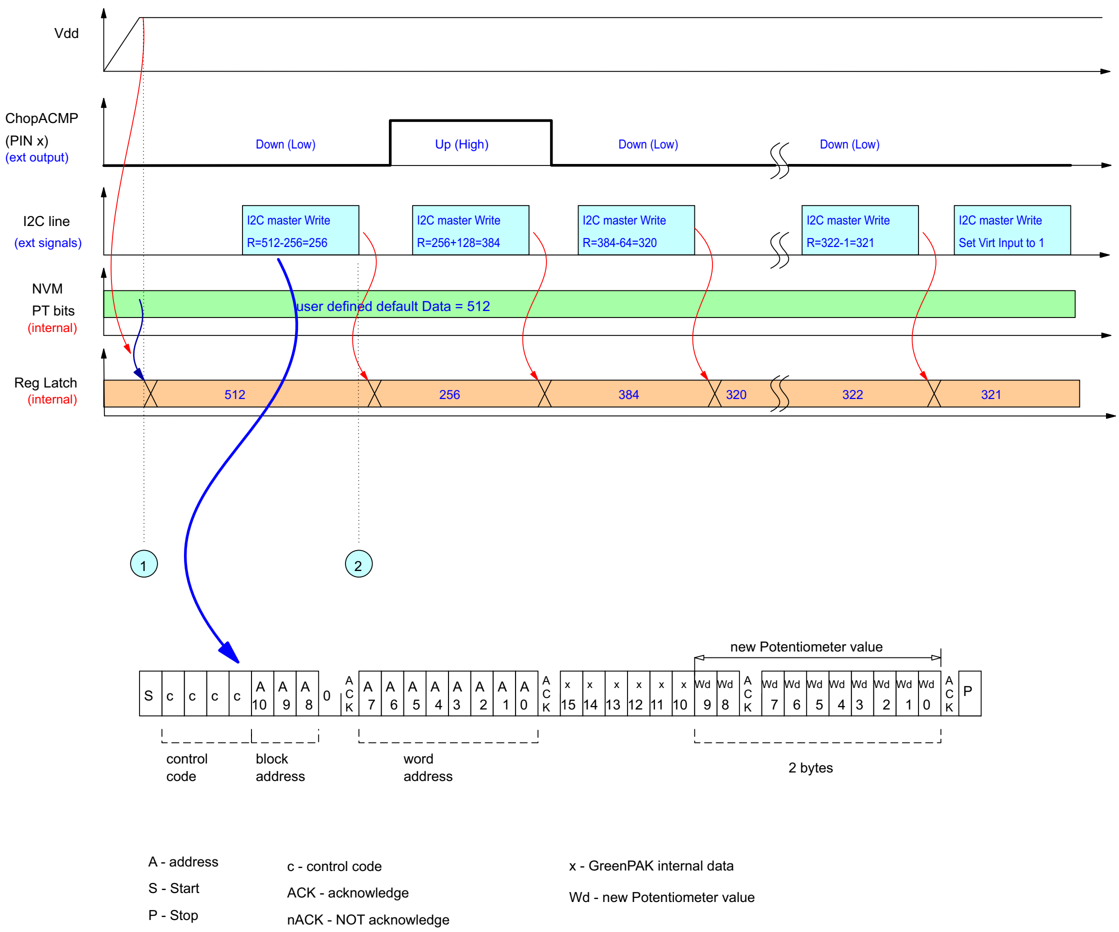


Figure 181. Example of User Specific Trimming Process under I^{2}C Master Control

The key events of a user specific trimming process under I^{2}C master control are as follows:

1. During the startup event the SLG47004-A loads the rheostat value from NVM to Internal Counter. In the example this value is 512.

2. I^{2}C master writes a new value to the Rheostat's Internal Counter according to Chopper ACMP output. Note that the minimum time for changing the rheostat code depends on the time response of the user system.

Additionally, the I^{2}C Master macrocell can use internal resources such as an ADC to read the system data, find the error, and then adjust the Rheostat value. Also, it is possible to change the Rheostat value for different conditions. For example, the I^{2}C Master macrocell can change the Rheostat value based on the temperature change to reduce the system error.

12.4 Using Chopper ACMP

When the Auto-Trim Function is disabled, the Chopper comparator can be used as a standalone analog comparator. Inputs of the Chopper ACMP are selected by the M1 and M2 analog MUXs. Output of the Chopper ACMP can be optionally inverted by register [882]. This comparator output is the input [55] of the connection matrix. In case of a disabled Auto-Trim Function, the power up source for the Chopper ACMP comes from connection matrix. Please refer to Section 9. Analog Comparators for more details.

12.5 Digital Rheostats Typical Performance

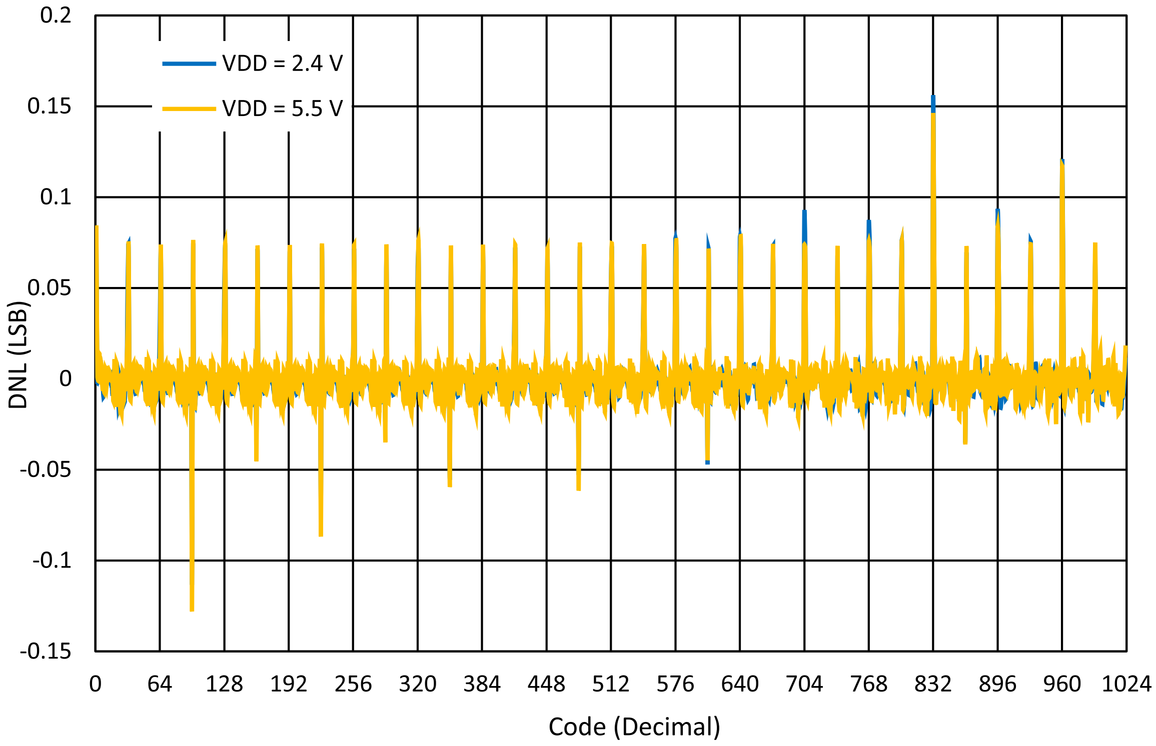


Figure 182. DNL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T_A = 25 °C

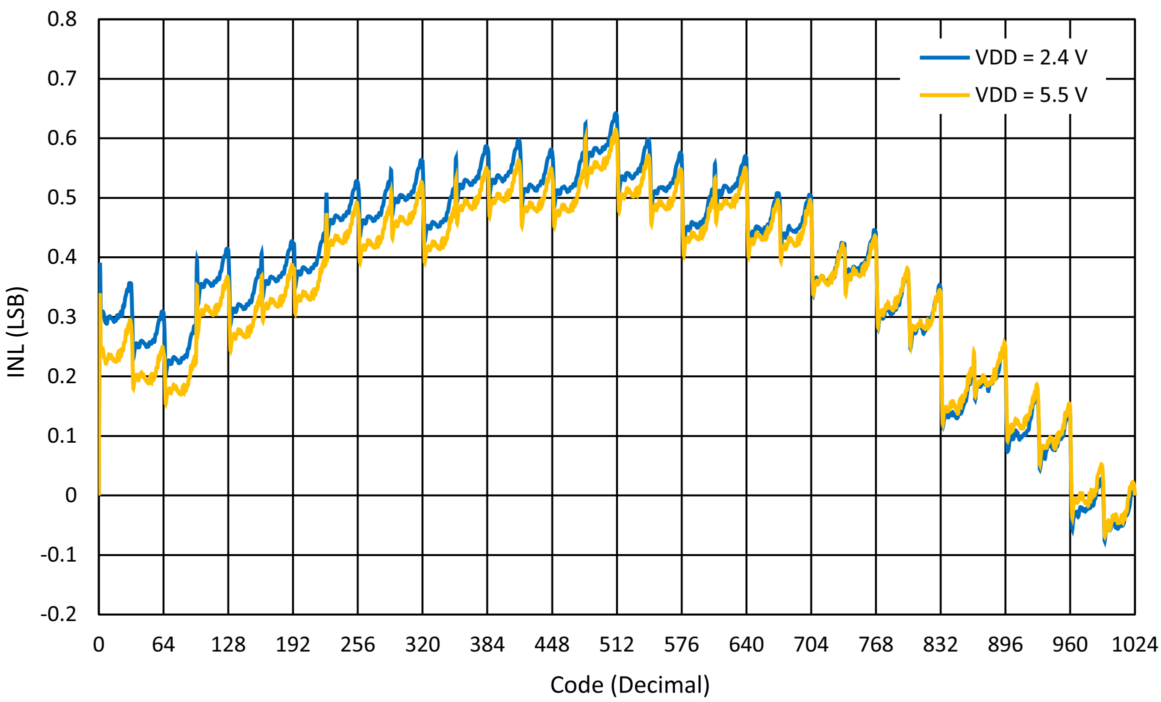


Figure 183. INL vs. Digital Code, Rheostat Mode (V_{AB} = 1 V) at T_A = 25 °C

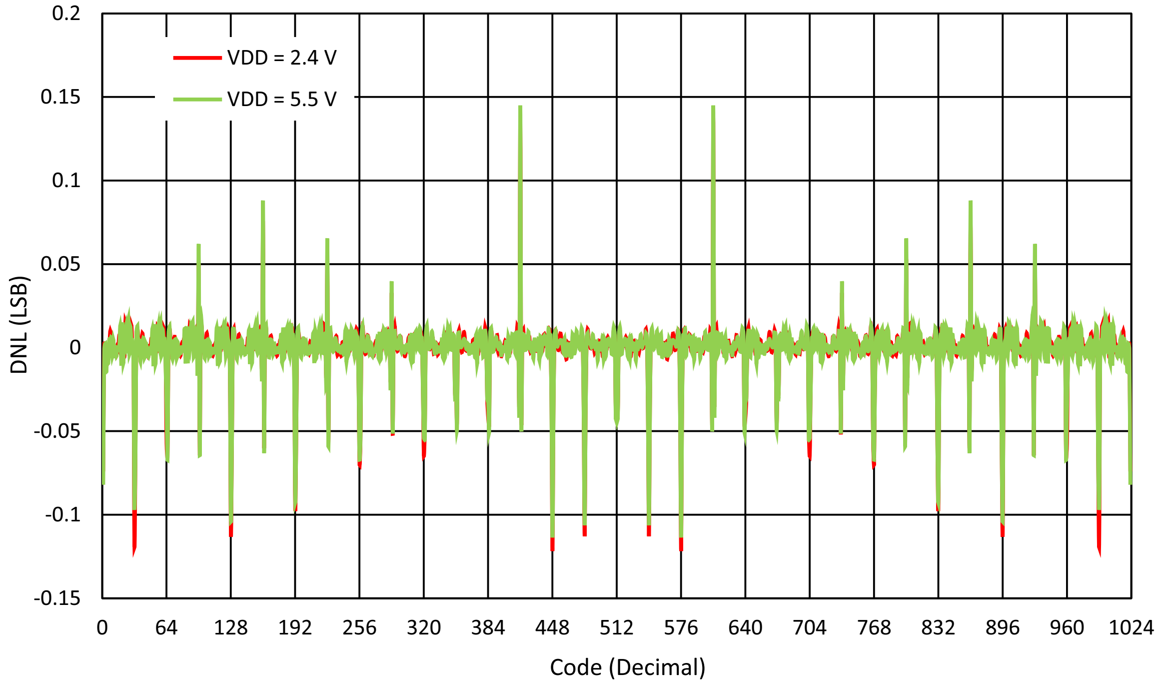


Figure 184. DNL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T_A = 25 °C

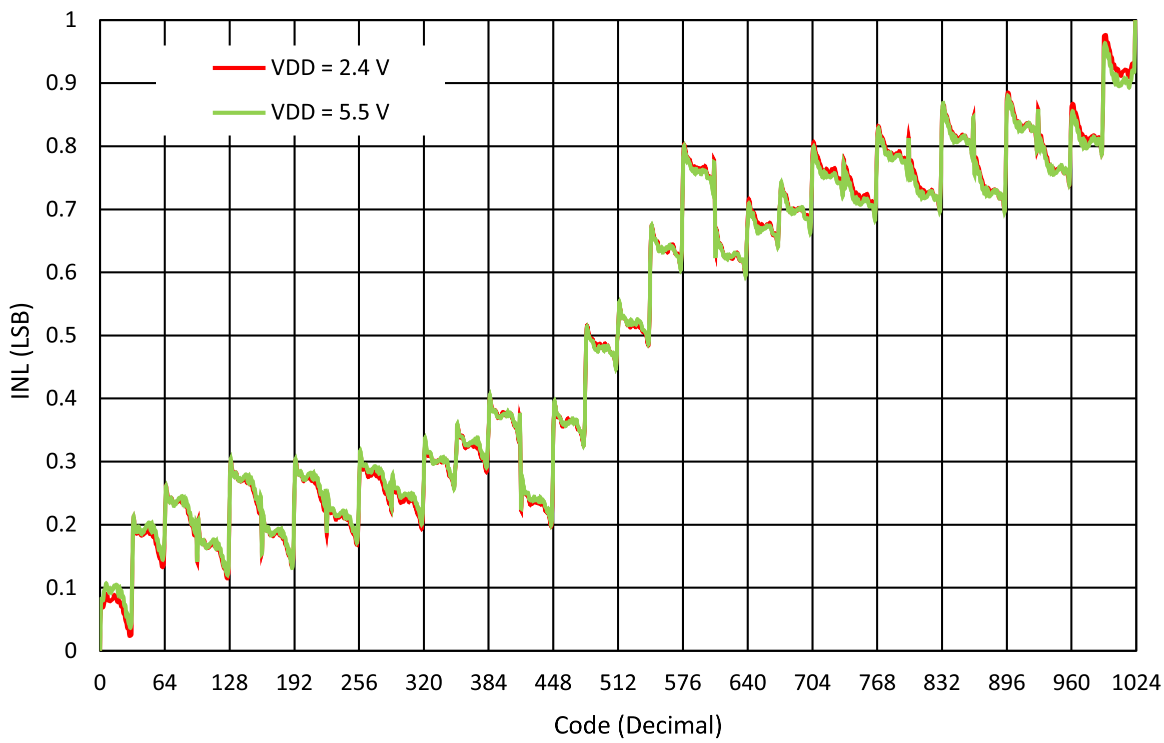


Figure 185. INL vs. Digital Code, Potentiometer Mode (V_{AB} = 1 V) at T_A = 25 °C

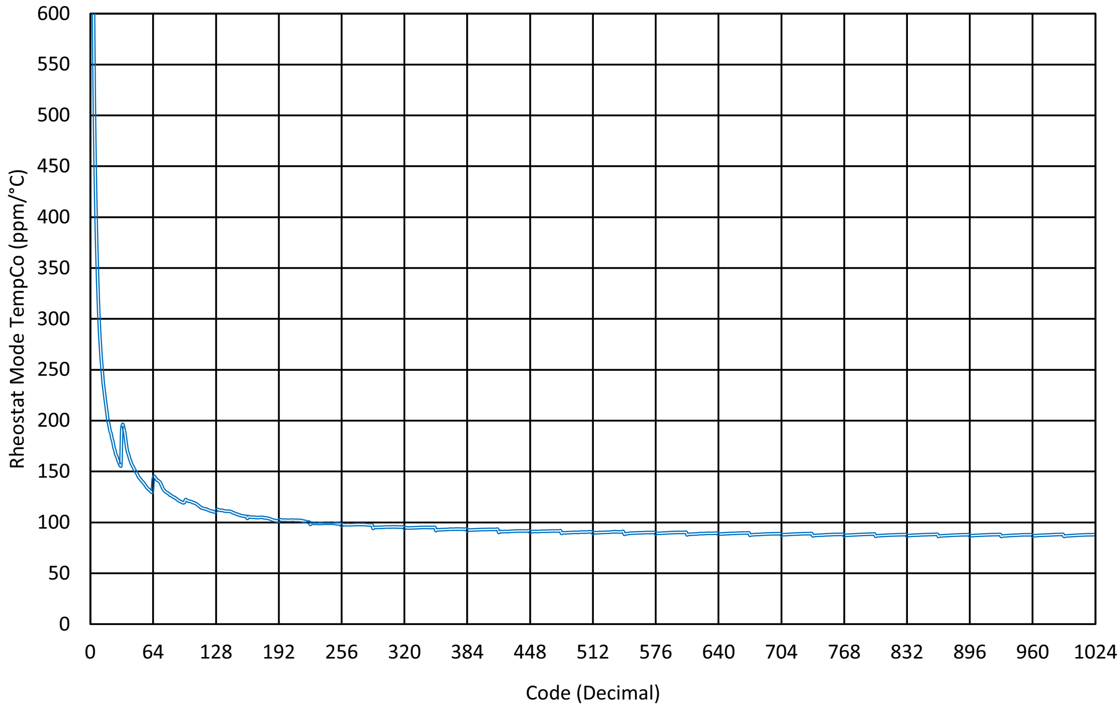


Figure 186. ($\Delta R_{AB}/R_{AB})/\Delta T_A$ Rheostat Mode Tempco

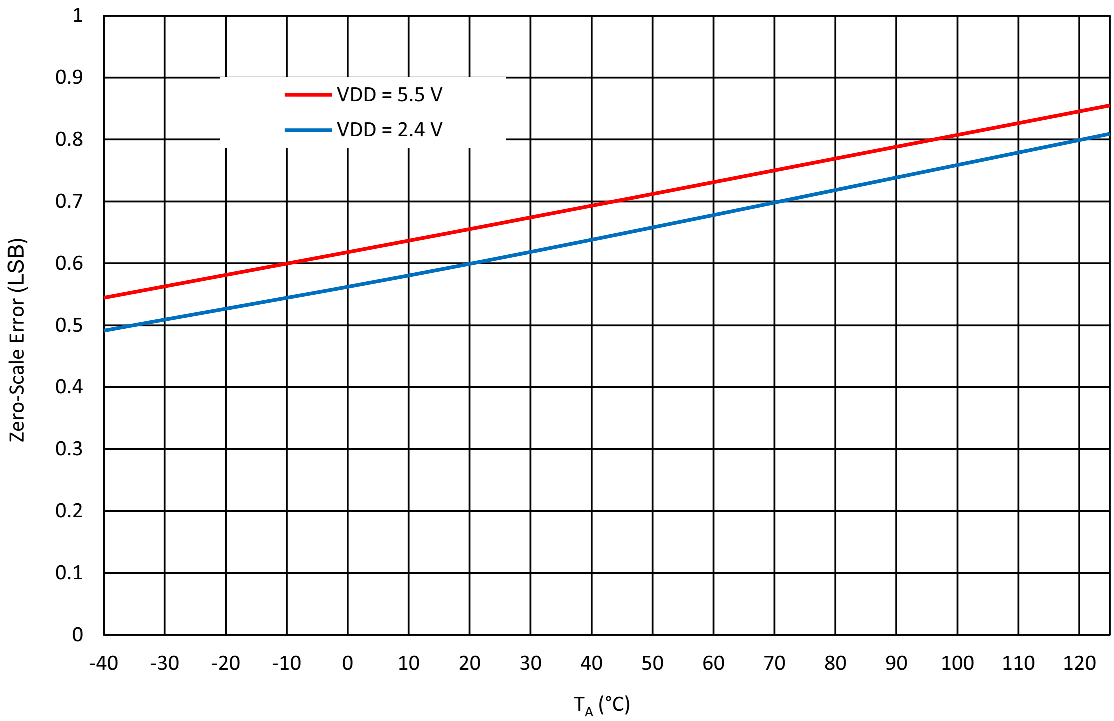


Figure 187. RHx Zero Scale Error vs. Ambient Temperature (V_{IN} = 1 V)

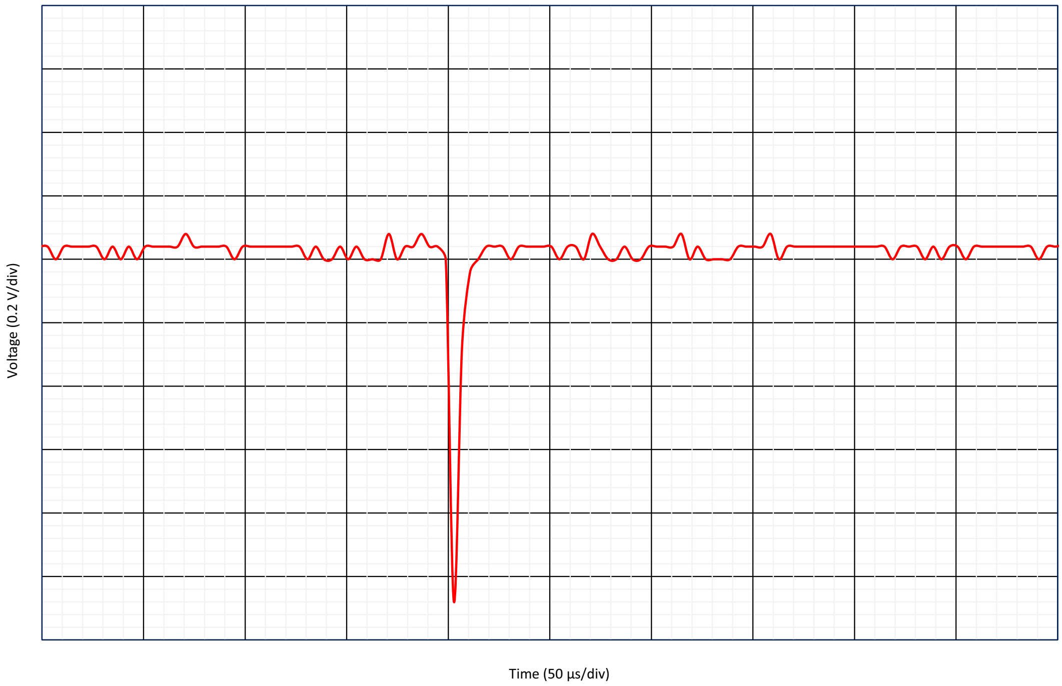


Figure 188. Transition Glitch in Worst Case (Code = 511 to Code = 512)

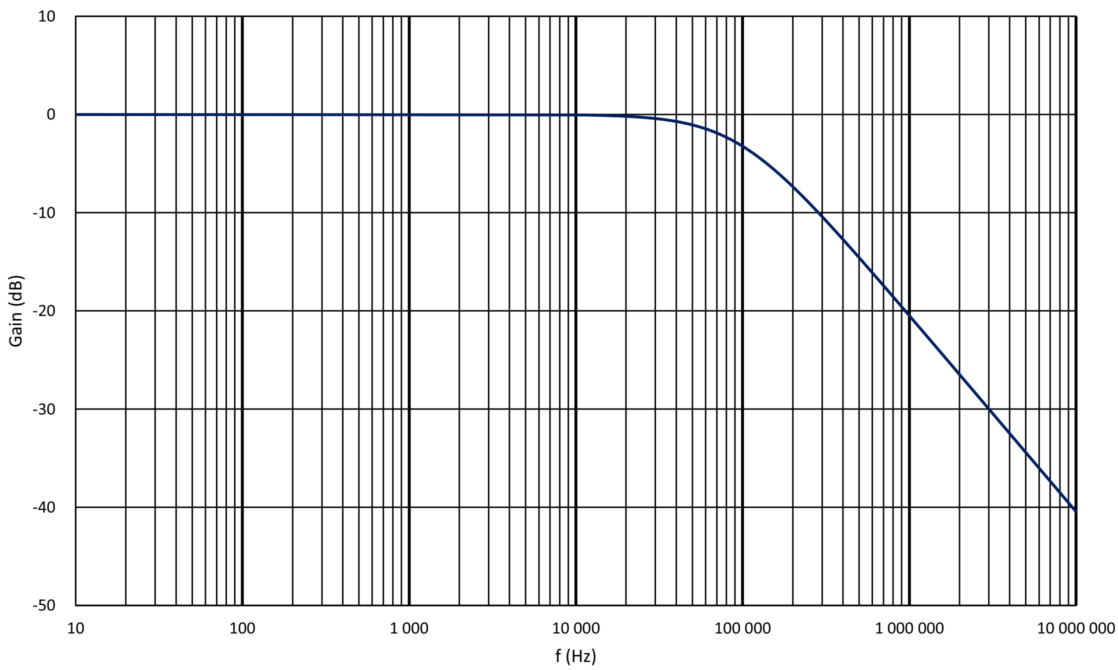


Figure 189. Gain vs. Frequency (Code = 512) at T_A = 25 °C, V_{DDA} = 5 V

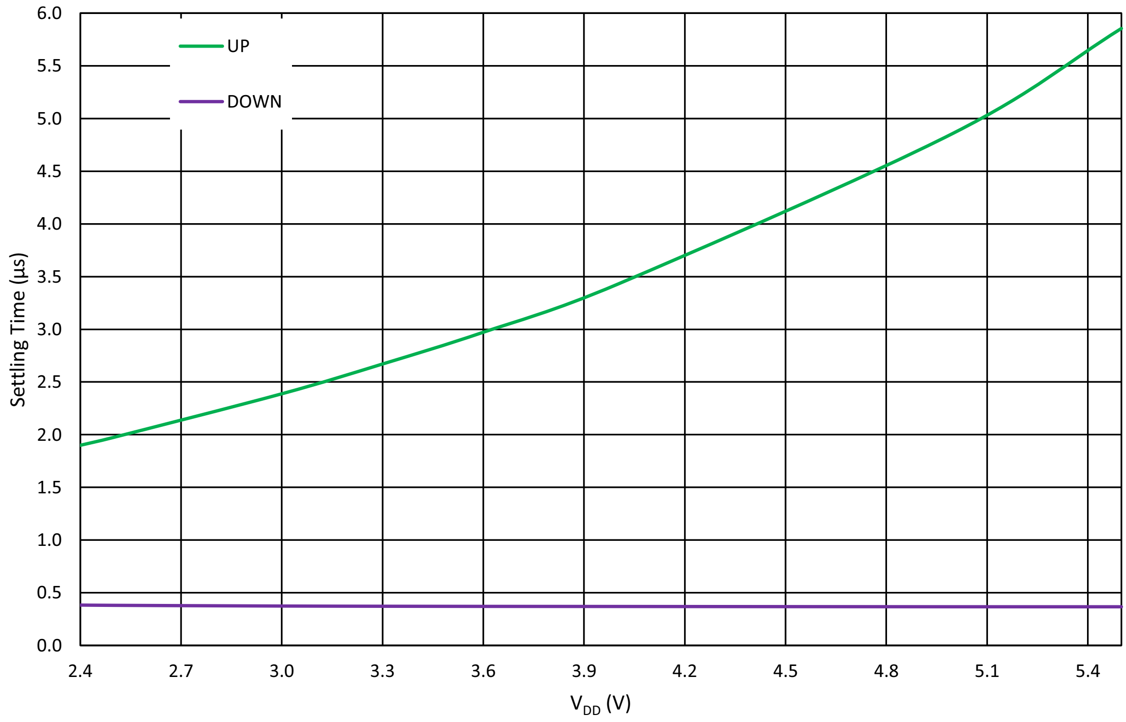


Figure 190. RHx Settling Time vs. V_{DD} at I_{LOAD} = 1 mA, T_A = 25 °C

13. Programmable Delay/Edge Detector

The SLG47004-A has a programmable time delay logic cell available, that can generate a delay that is selectable from one of four timings (time 2) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection, and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay, as well as glitch rejection during the delay period. See Figure 192 for further information.

Note: The input signal must be longer than the delay, otherwise it will be filtered out.

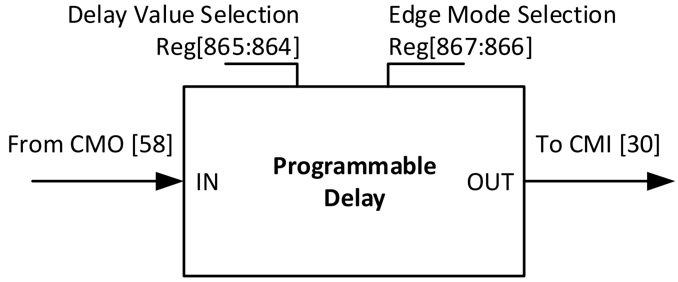


Figure 191. Programmable Delay

13.1 Programmable Delay Timing Diagram - Edge Detector Output

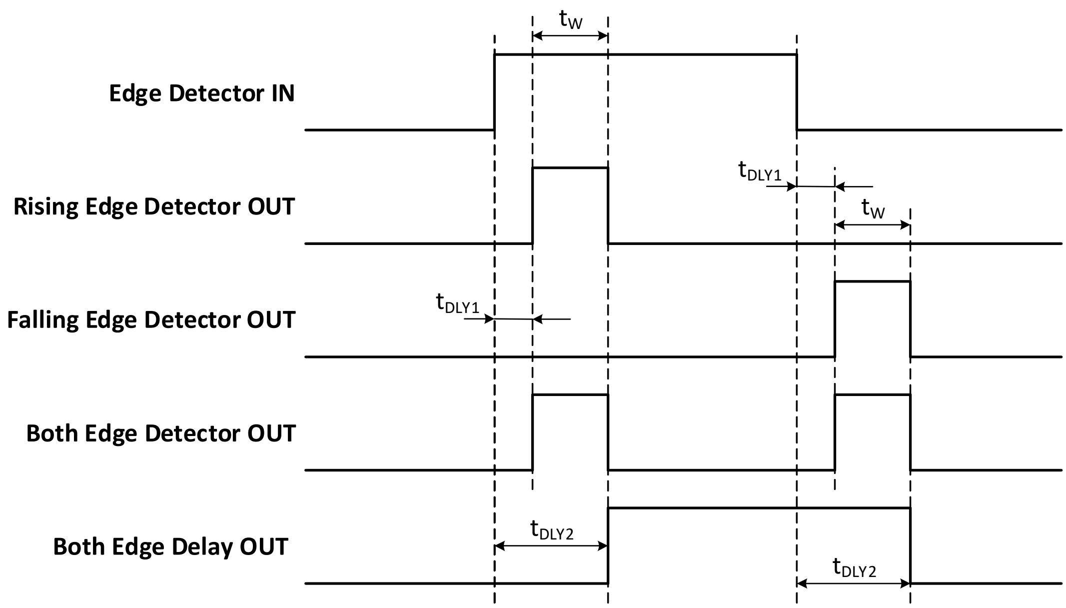


Figure 192. Edge Detector Output

Please refer to Table 14.

14. Additional Logic Function. Deglitch Filter

The SLG47004-A has one Deglitch Filter macrocell with inverter function that is connected directly to the Connection matrix inputs and outputs. In addition, this macrocell can be configured as an Edge Detector, with the following settings:

- Rising Edge Detector
- Falling Edge Detector
- Both Edge Detector
- Both Edge Delay.

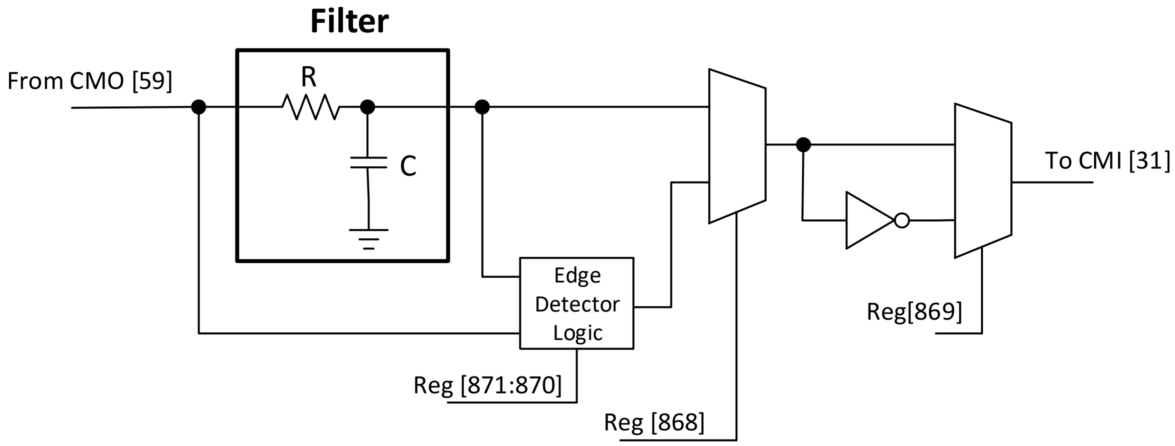


Figure 193. Deglitch Filter or Edge Detector

15. Voltage Reference

15.1 Voltage Reference Overview

The SLG47004-A has a Voltage Reference (Vref) Macrocell to provide reference to analog comparators and operational amplifiers. The macrocell also has the option to output reference voltages on external pins (see Table 2). Vref0 and Vref1 share output buffers with Temperature sensor. Note that user can use any of output buffers, but Temperature sensor is calibrated for Vref1 output buffer. See Table 61 for the available selections for each analog comparator. Also, see Figure 194, Figure 195, and Figure 196, which show the reference output structure.

Also there is a high drive voltage reference macrocell called HD Buffer. The purpose of this macrocell is to provide stable voltage to the relatively high-power load (please refer to Table 22). HD Buffer has shared voltage reference source with the Op Amp0 Vref. User can select output voltage in the range from V_{DD}/64 to V_{DD} with a step V_{DD}/64, or output voltage in a range from 32 mV to 2.048 V with a step 32 mV (see Figure 196).

Note that Chopper ACMP will automatically enable HD Buffer if HD Buffer is selected as a source for Chopper ACMP In-signal (register 946 = 0) and Chopper ACMP is powered up.

15.2 Vref Selection Table

Table 61. Vref Selection Table

SEL[5:0]	Vref	SEL[5:0]	Vref
0	0.032	33	1.088
1	0.064	34	1.12
2	0.096	35	1.152
3	0.128	36	1.184
4	0.16	37	1.216
5	0.192	38	1.248
6	0.224	39	1.28
7	0.256	40	1.312
8	0.288	41	1.344
9	0.32	42	1.376
10	0.352	43	1.408
11	0.384	44	1.44
12	0.416	45	1.472
13	0.448	46	1.504
14	0.48	47	1.536
15	0.512	48	1.568
16	0.544	49	1.6
17	0.576	50	1.632
18	0.608	51	1.664
19	0.64	52	1.696
20	0.672	53	1.728
21	0.704	54	1.76
22	0.736	55	1.792

Table 61. Vref Selection Table (Cont.)

SEL[5:0]	Vref	SEL[5:0]	Vref
23	0.768	56	1.824
24	0.8	57	1.856
25	0.832	58	1.888
26	0.864	59	1.92
27	0.896	60	1.952
28	0.928	61	1.984
29	0.96	62	2.016
30	0.992	63	2.048
31	1.024	64	External
32	1.056	--	--

15.3 Vref Block Diagram

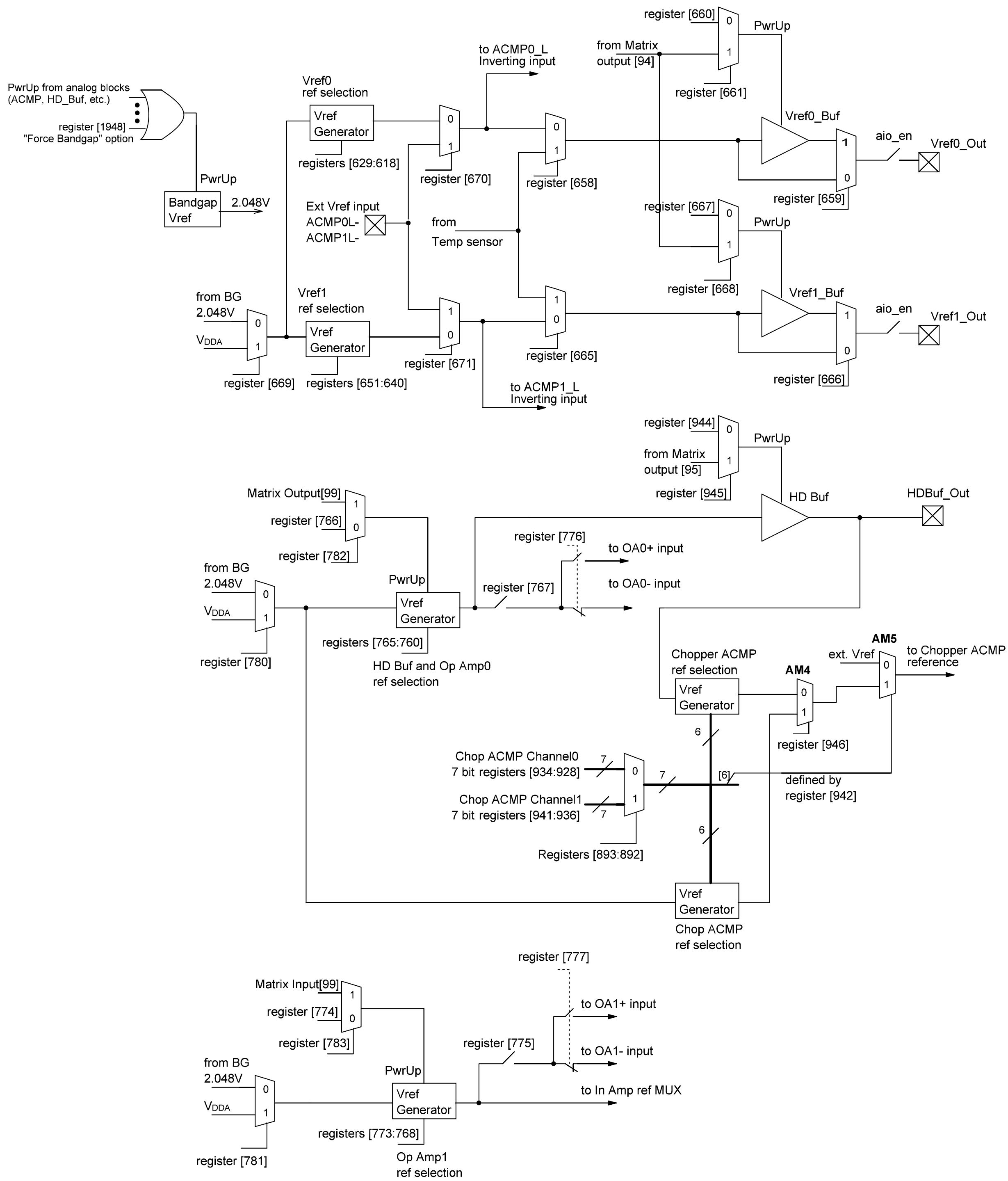


Figure 194. Generalized Vref Structure

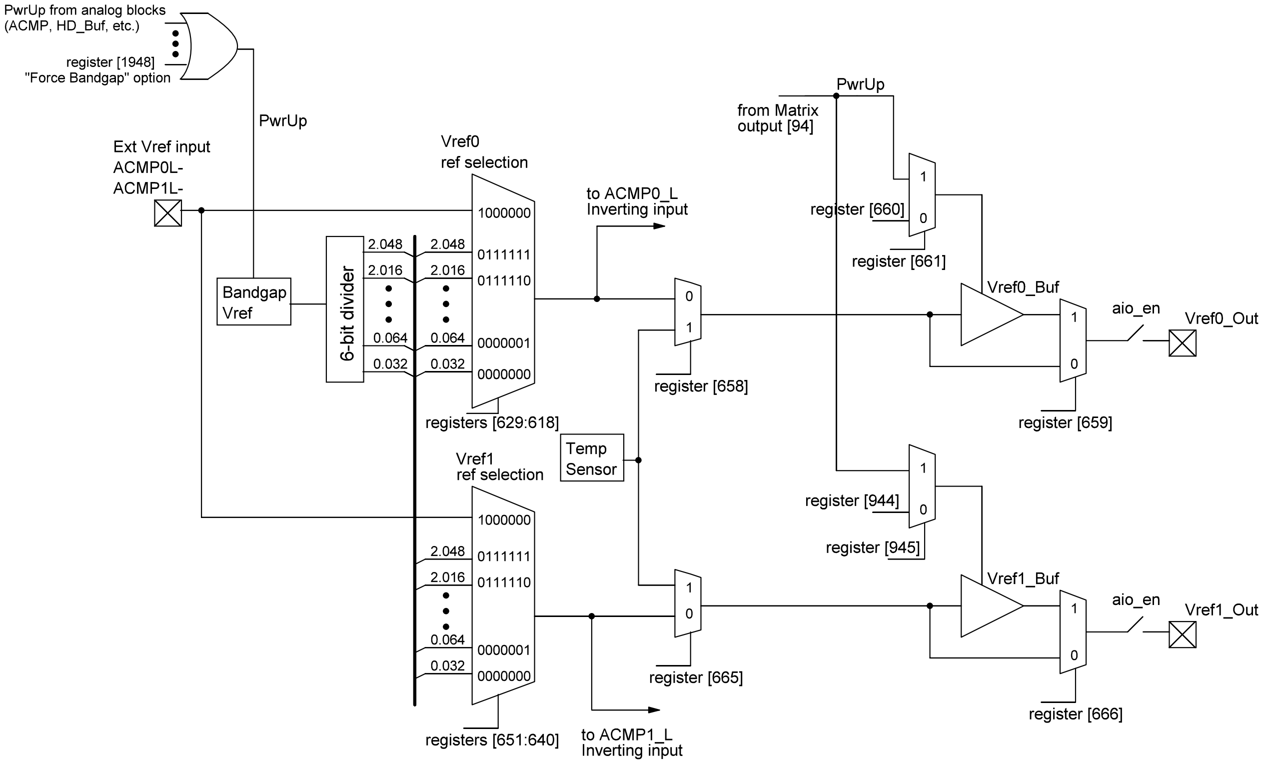


Figure 195. ACMP0L, ACMP1L Voltage Reference Block Diagram

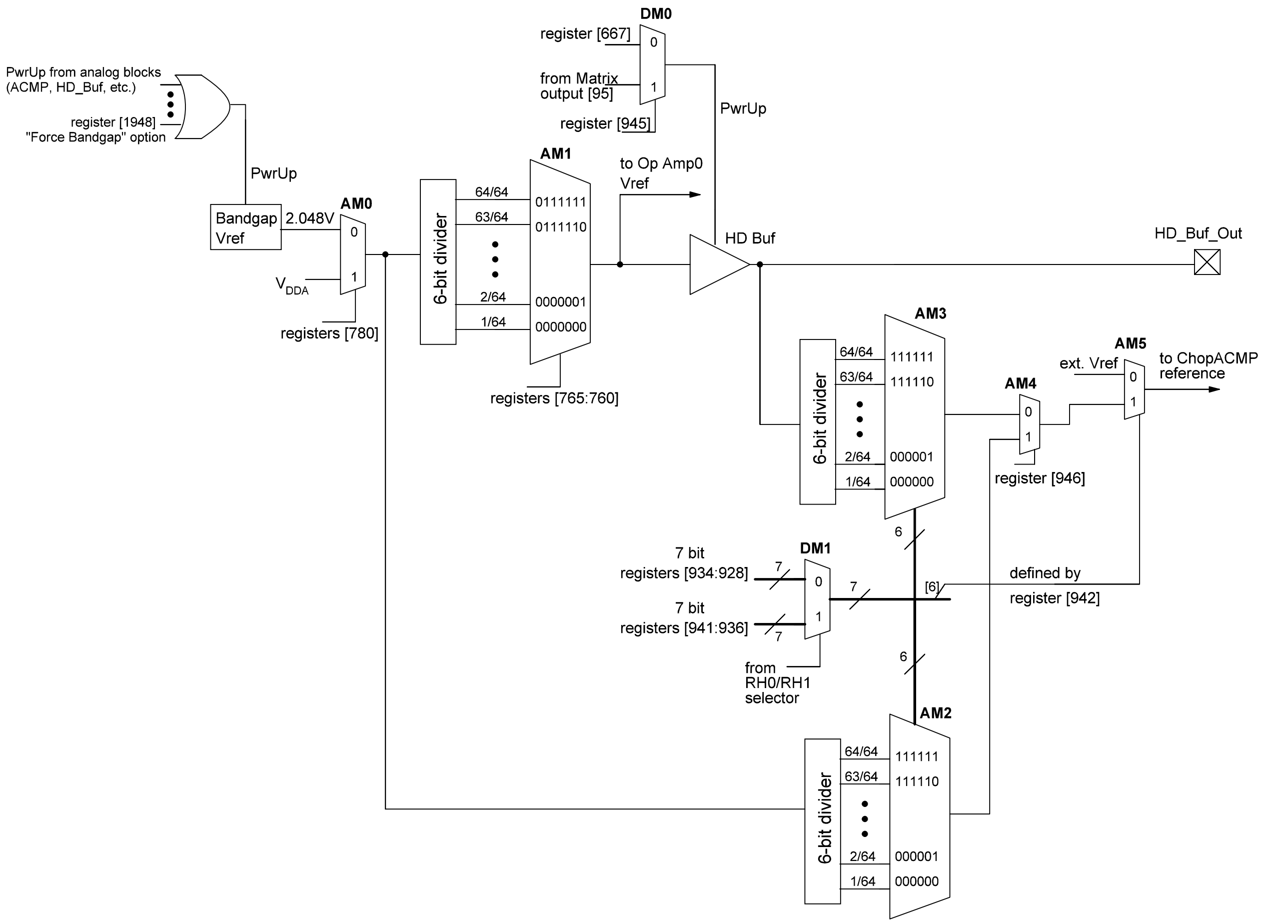


Figure 196. HD Buffer and Chopper ACMP Reference Block Diagram

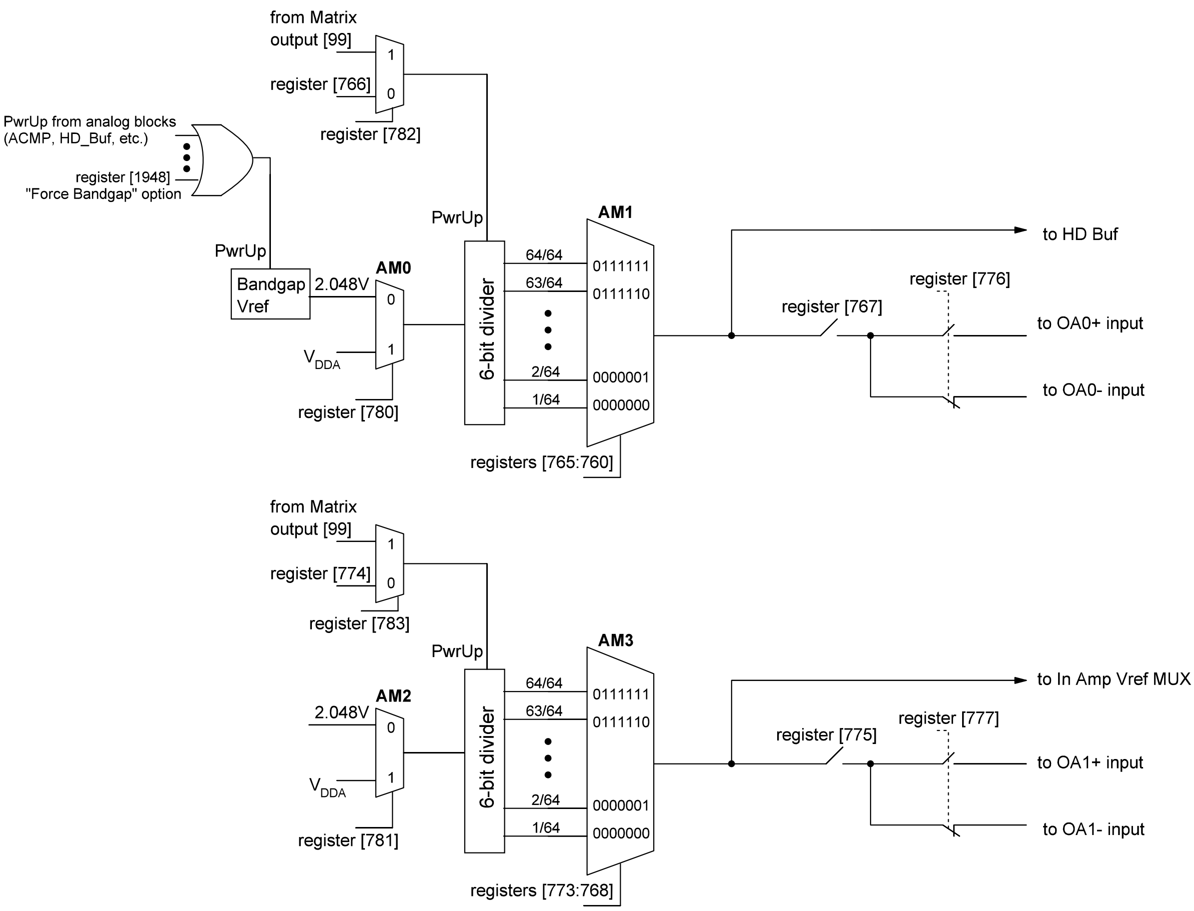


Figure 197. Operational Amplifiers Voltage Reference Block Diagram

15.4 Voltage Reference Typical Performance

Note: It is not recommended to use Vref connected to external pin without buffer.

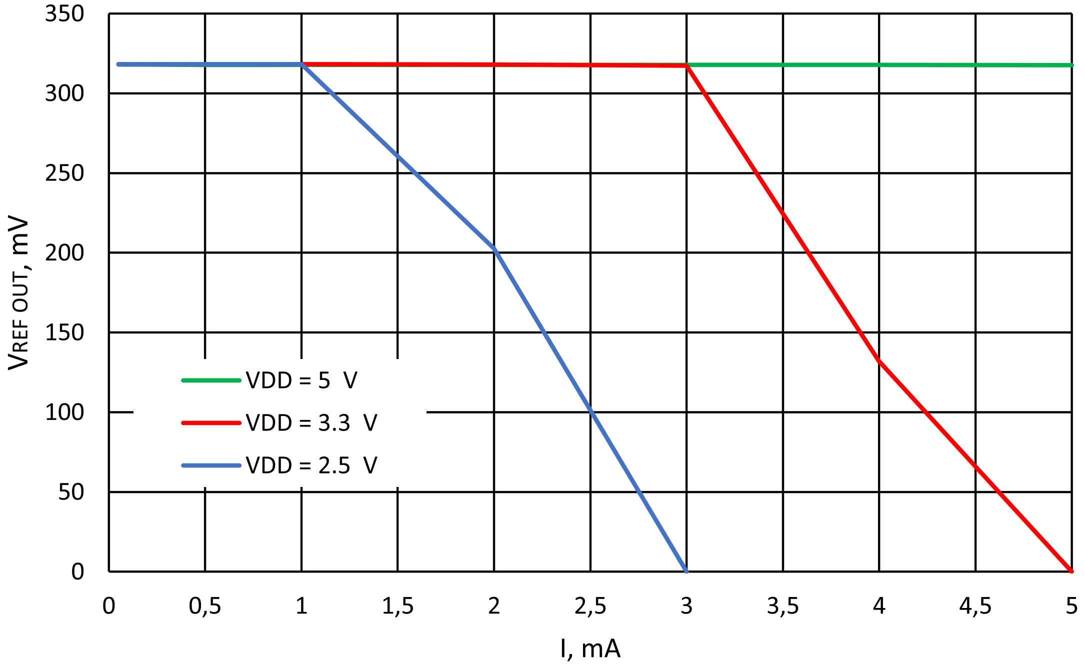


Figure 198. Typical Load Regulation, Vref = 320 mV, T_A = -40 °C to +125 °C, Buffer - Enable

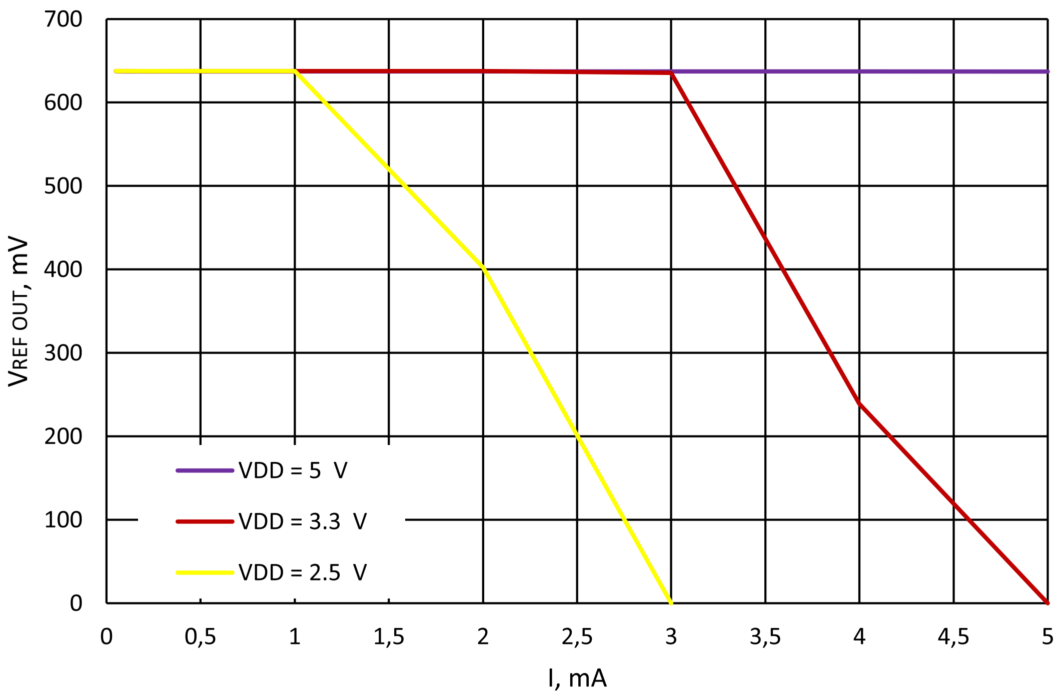


Figure 199. Typical Load Regulation, Vref = 640 mV, T_A = -40 °C to +125 °C, Buffer - Enable

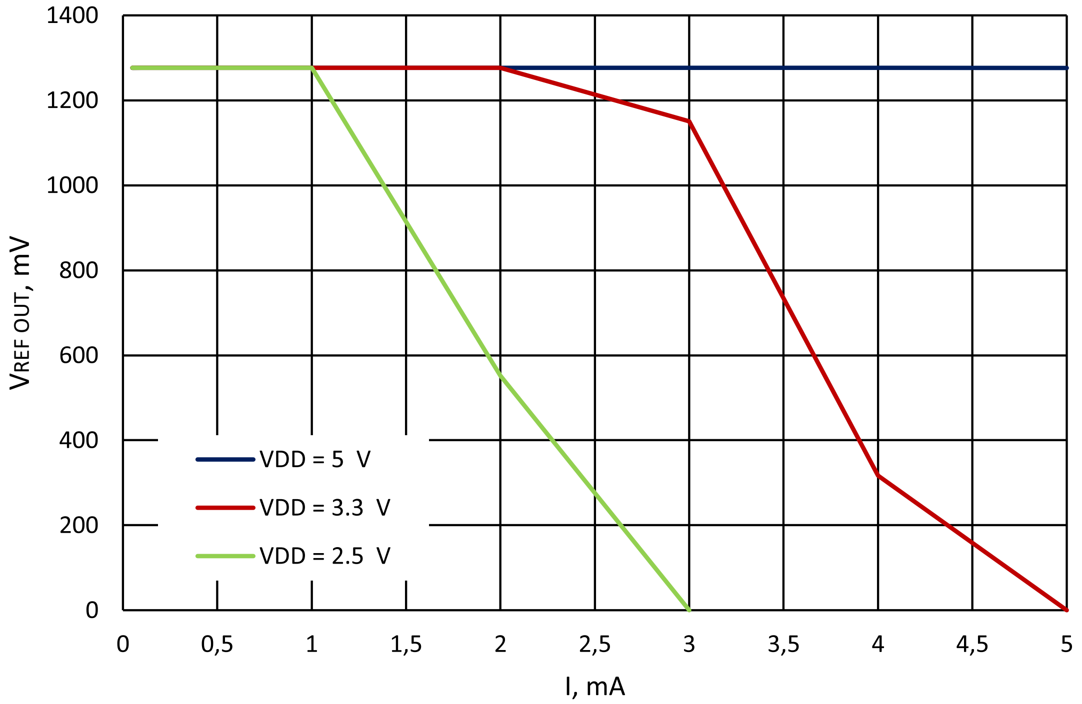


Figure 200. Typical Load Regulation, Vref = 1280 mV, T_A = -40 °C to +125 °C, Buffer - Enable

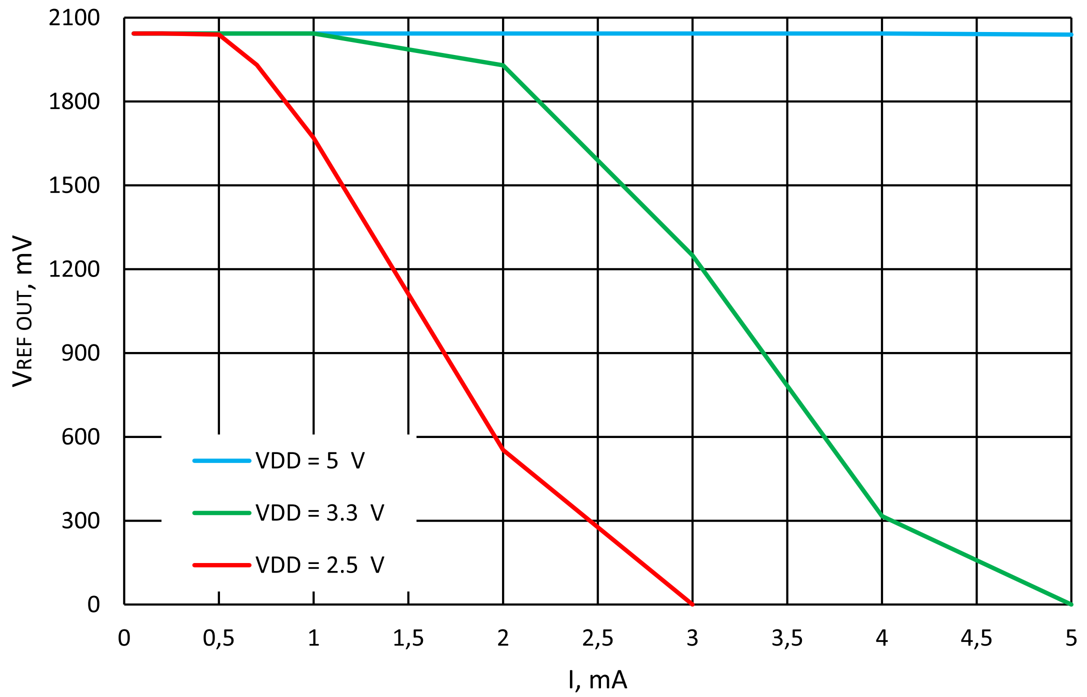


Figure 201. Typical Load Regulation, Vref = 2048 mV, T_A = -40 °C to +125 °C, Buffer - Enable

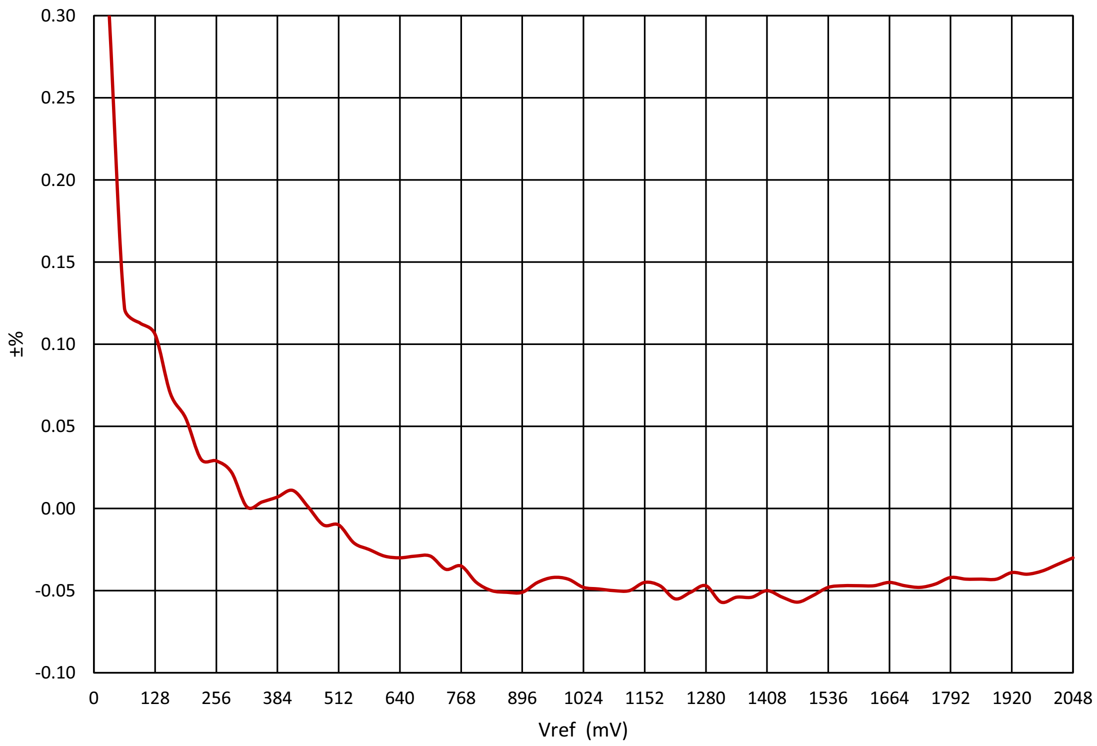


Figure 202. Typical Input Offset Voltage vs. Vref at V_{DD} = 2.4 V to 5.5 V, T_A = 25 °C, Buffer Disabled

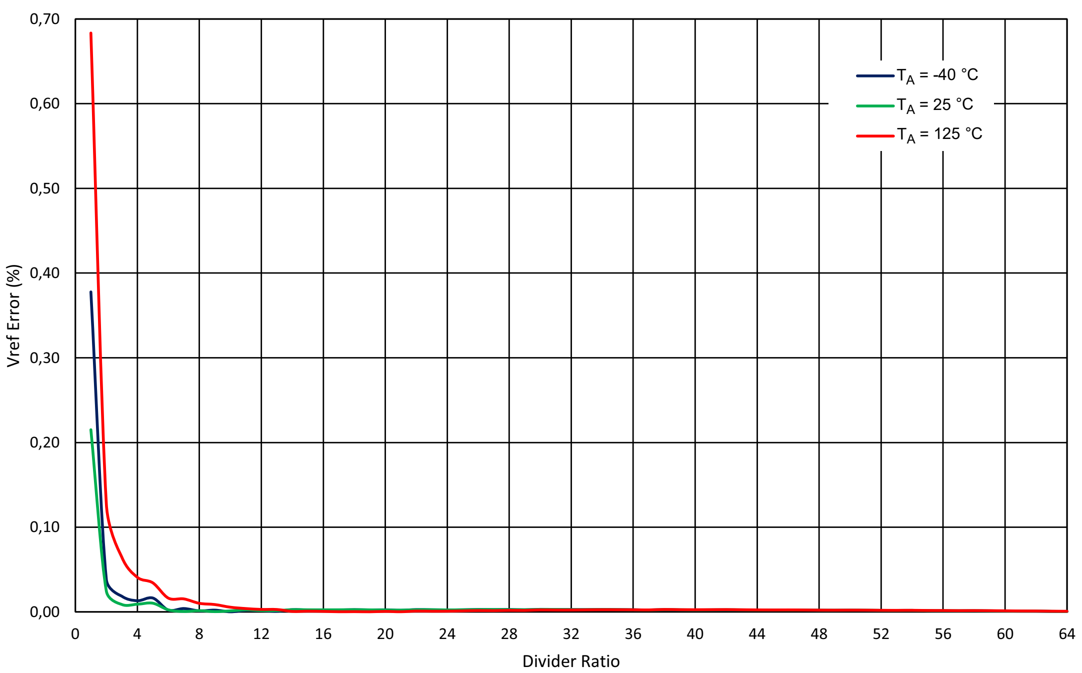


Figure 203. Op Ampx Vref Divider Acuuracy at V_{DD} = 3.3 V

15.5 HD Buffer Typical Performance

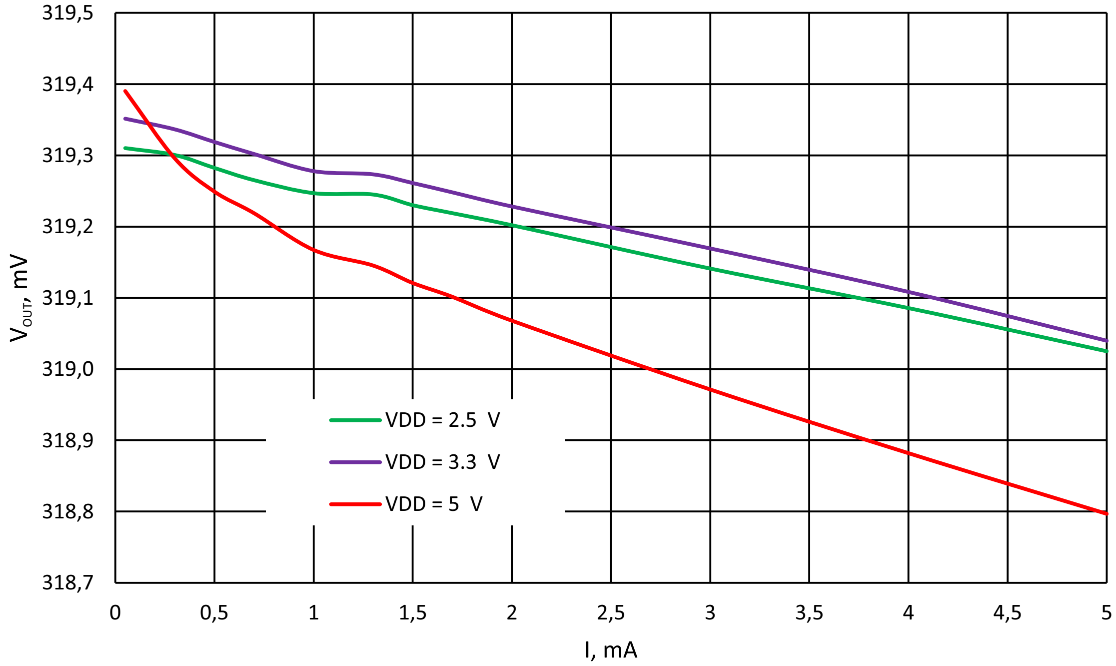


Figure 204. HD Buffer Typical Load Regulation, Vref = 320 mV, T_A = -40 °C to +125 °C

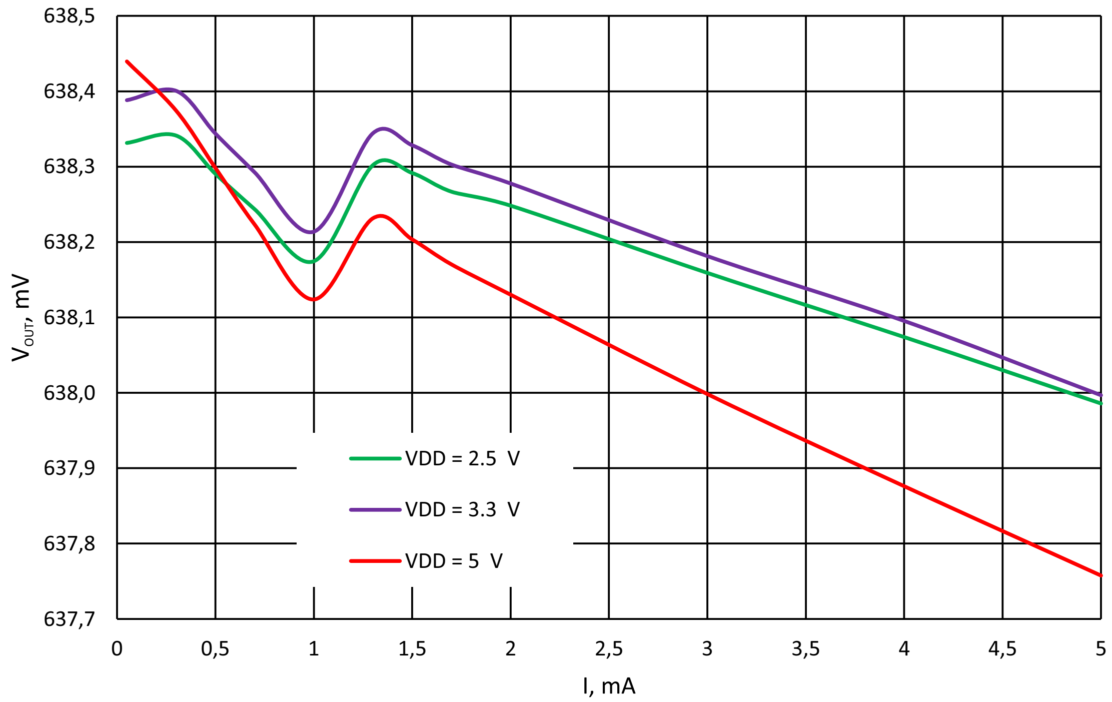


Figure 205. HD Buffer Typical Load Regulation, Vref = 640 mV, T_A = -40 °C to +125 °C

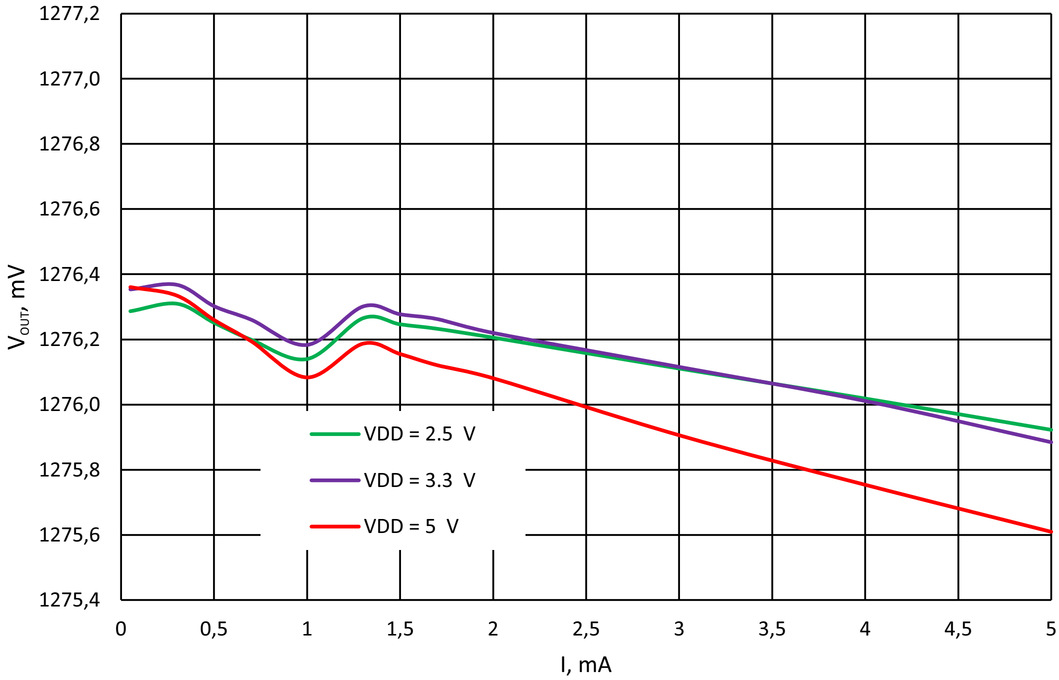


Figure 206. HD Buffer Typical Load Regulation, Vref = 1280 mV, T_A = -40 °C to +125 °C

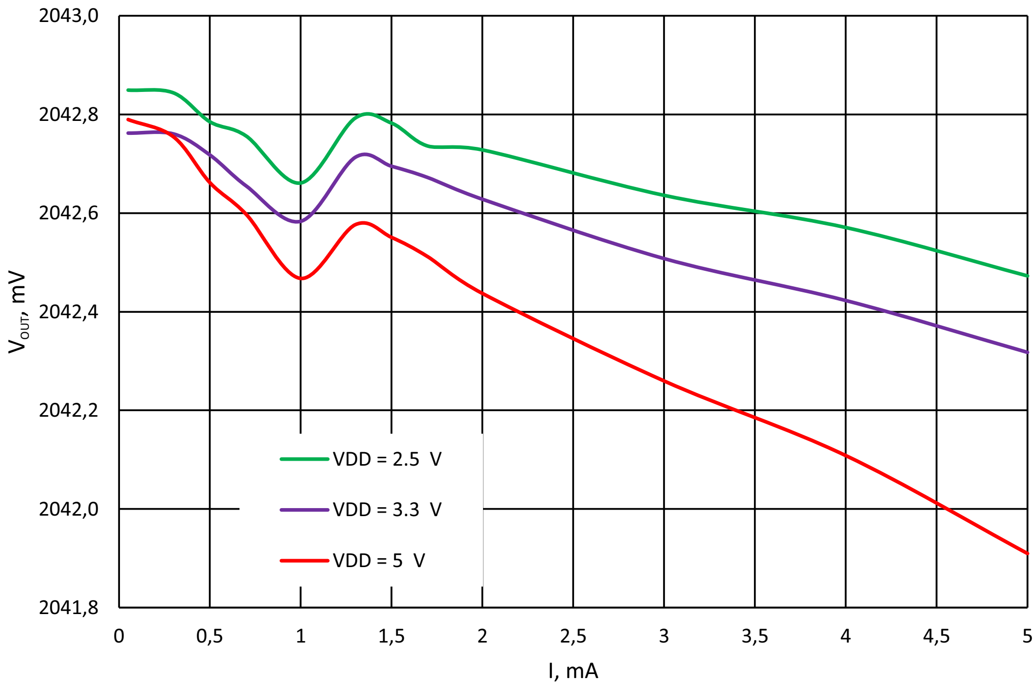


Figure 207. HD Buffer Typical Load Regulation, Vref = 2048 mV, T_A = -40 °C to +125 °C

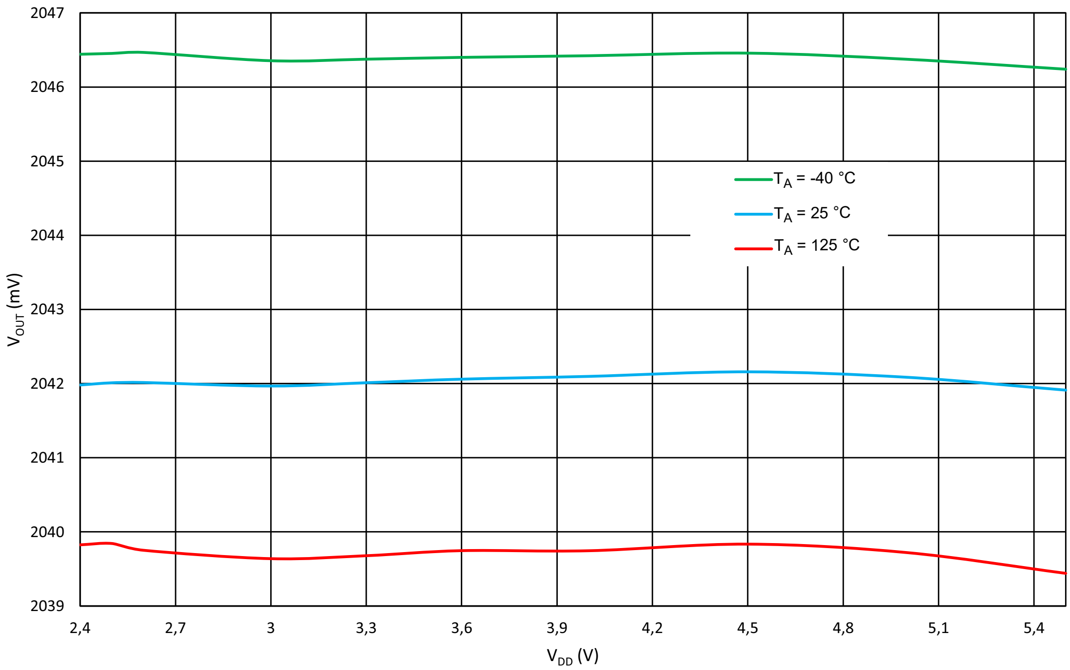


Figure 208. HD Buffer Typical Line Regulation, I_{LOAD} = 5 mA

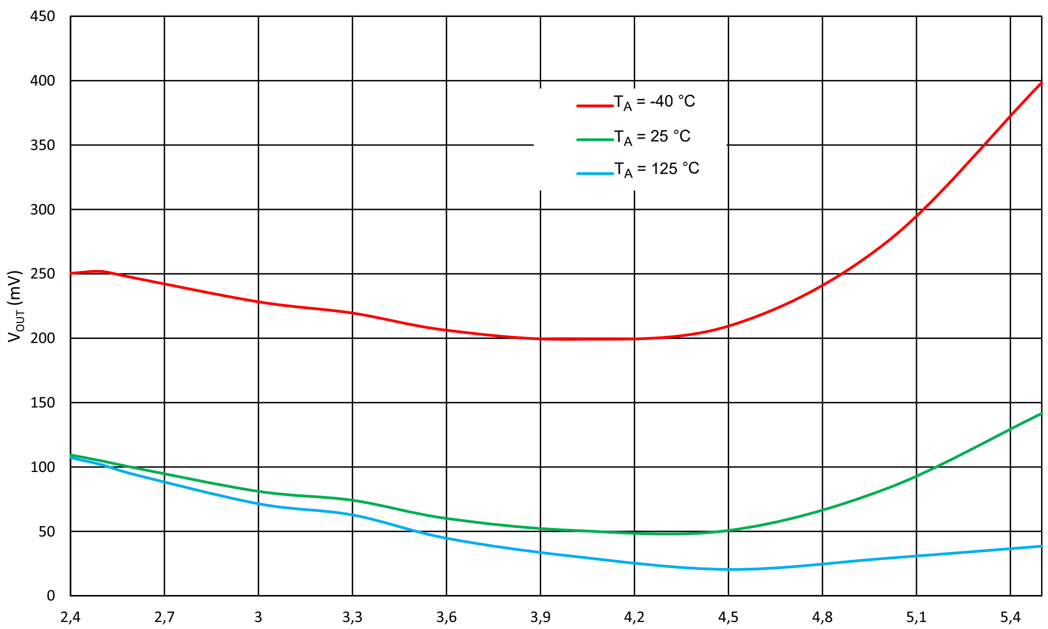


Figure 209. HD Buffer Offset vs. V_{DD}

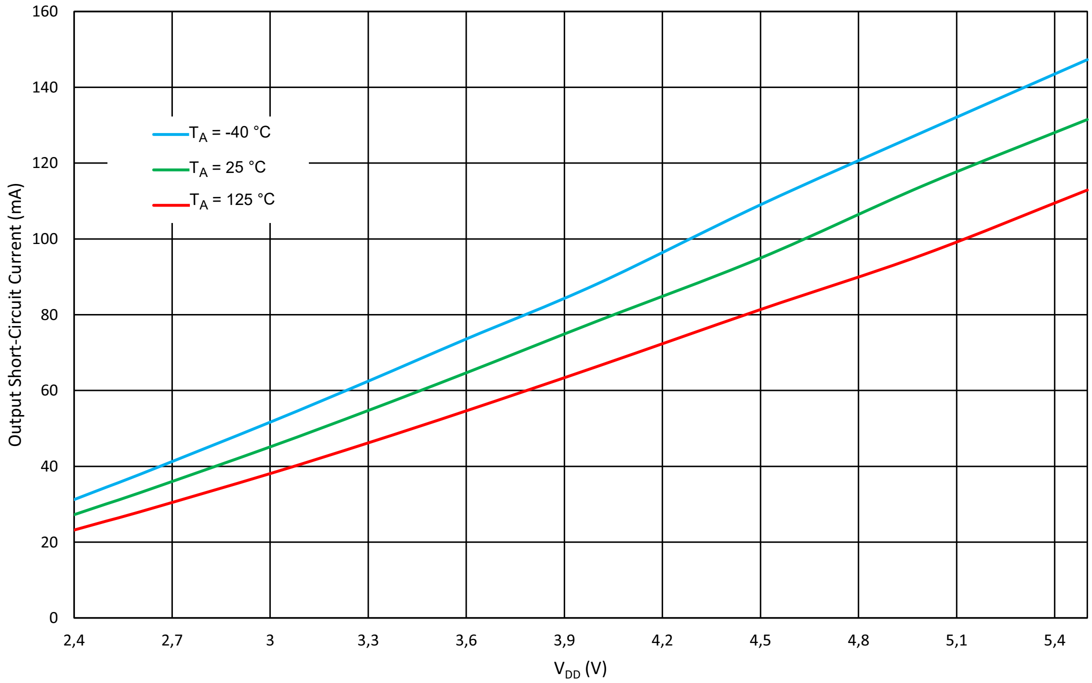


Figure 210. HD Buffer Output Short-Circuit Current vs. V_{DD}

16. Clocking

16.1 OSC General Description

The SLG47004-A has three internal oscillators to support a variety of applications:

- Oscillator0 (2.048 kHz)
- Oscillator1 (2.048 MHz)
- Oscillator2 (25 MHz).

There are two divider stages for each oscillator that give the user flexibility for introducing clock signals to connection matrix, as well as various other Macrocells. The pre-divider (first stage) for Oscillator allows the selection of /1, /2, /4, or /8 to divide down frequency from the fundamental. The second stage divider has an input of frequency from the pre-divider, and outputs one of eight different frequencies divided by /1, /2, /3, /4, /8, /12, /24, or /64 on Connection Matrix Input lines [52], [53], and [54]. Please see Figure 214 for more details on the SLG47004-A clock scheme.

Oscillator2 (25 MHz) has an additional function of 100 ns delayed startup, which can be enabled/disabled by register [713]. This function is recommended to use when analog blocks are used along with the Oscillator.

The Matrix Power-down/Force On function allows switching off or force on the oscillator using an external pin. The Matrix Power-down/Force On (Connection Matrix Output [91], [92], [93]) signal has the highest priority. The OSC operates according to the Table 62.

It is highly recommended to force the bandgap on when OSC1 or OSC2 are used in the project.

Table 62. Oscillator Operation Mode Configuration Settings

POR	External Clock Selection	Signal from Connection Matrix	Register: Power-Down or Force On by Matrix Input	Register: Auto Power-On or Force On	OSC Enable Signal from CNT/DLY Macrocells	OSC Operation Mode
0	X	X	X	X	X	OFF
1	1	X	X	X	X	Internal OSC is OFF, logic is ON
1	0	1	0	X	X	OFF
1	0	1	1	X	X	ON
1	0	0	X	1	X	ON
1	0	0	X	0	CNT/DLY requires OSC	ON
1	0	0	X	0	CNT/DLY does not require OSC	OFF

[1] The OSC will run only when any macrocell that uses OSC is powered on.

16.2 Oscillator0 (2.048 kHz)

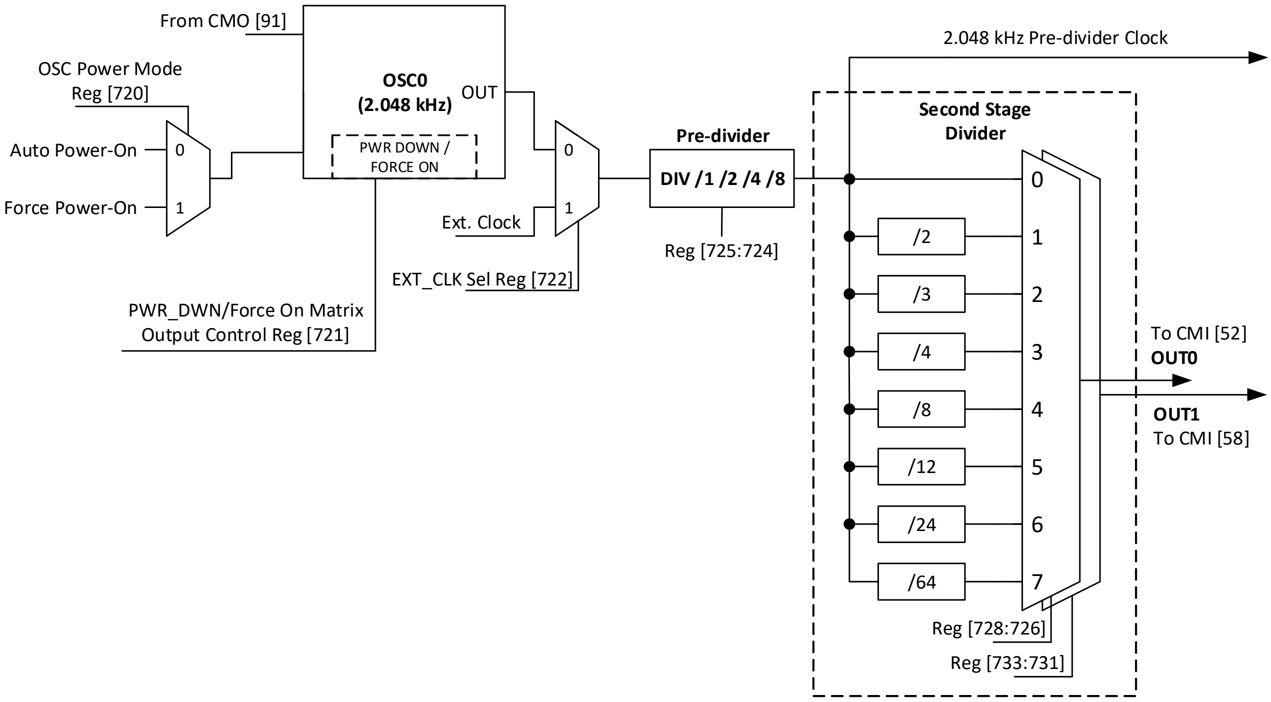


Figure 211. Oscillator0 Block Diagram

16.3 Oscillator1 (2.048 MHz)

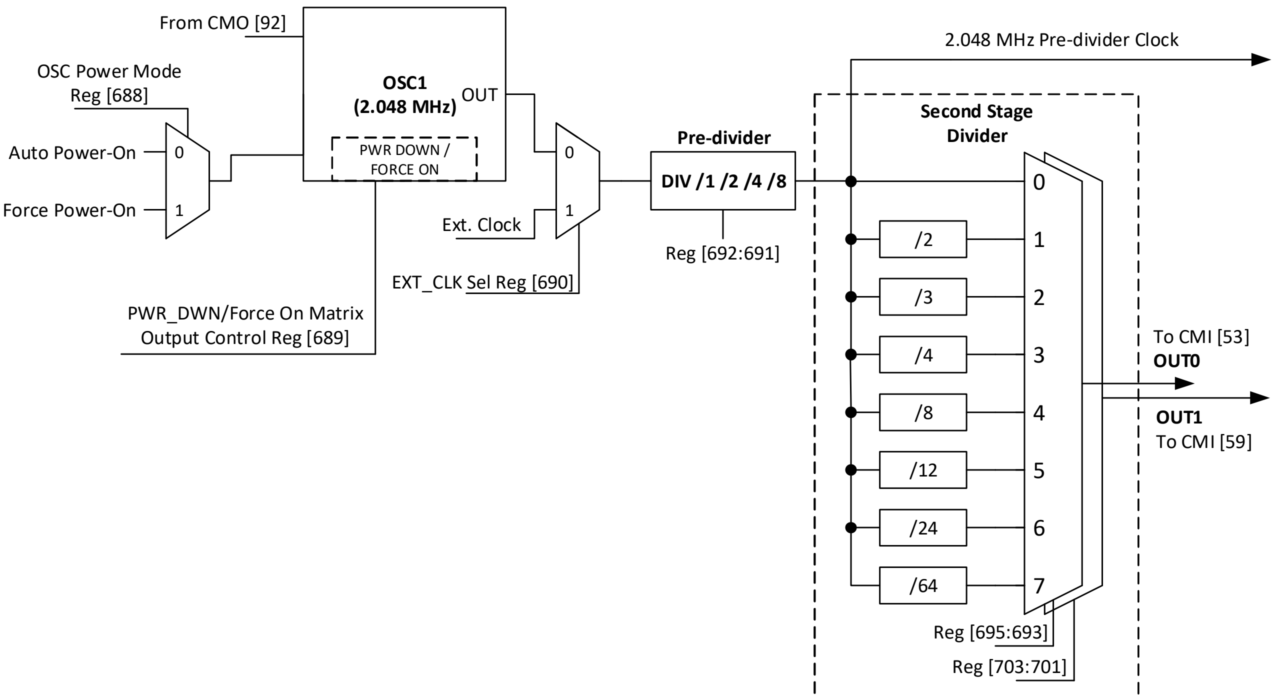


Figure 212. Oscillator1 Block Diagram

16.4 Oscillator2 (25 MHz)

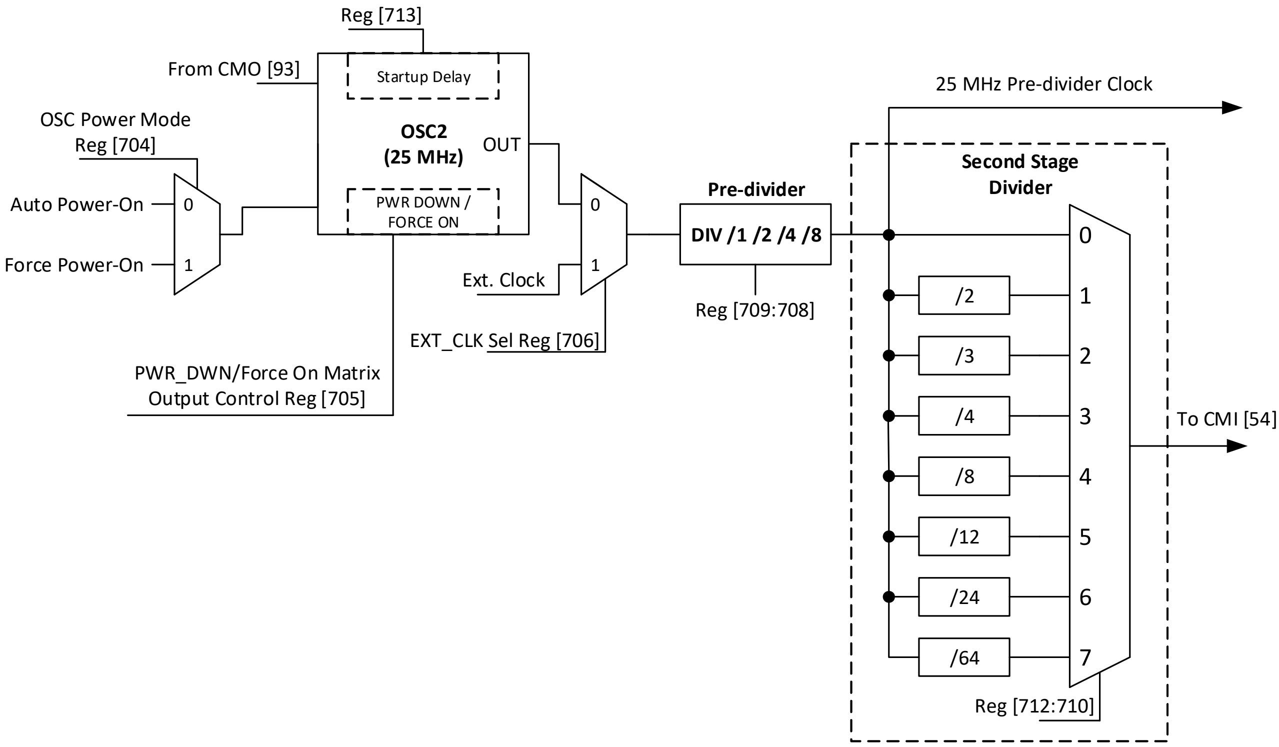


Figure 213. Oscillator2 Block Diagram

16.5 CNT/DLY Clock Scheme

Each CNT/DLY within Multi-Function macrocell has its own additional clock divider connected to oscillators pre-divider. Available dividers are:

- OSC0/1, OSC0/8, OSC0/64, OSC0/512, OSC0/4096, OSC0/32768, OSC0/262144
- OSC1/1, OSC1/8, OSC1/64, OSC1/512
- OSC2/1, OSC2/4

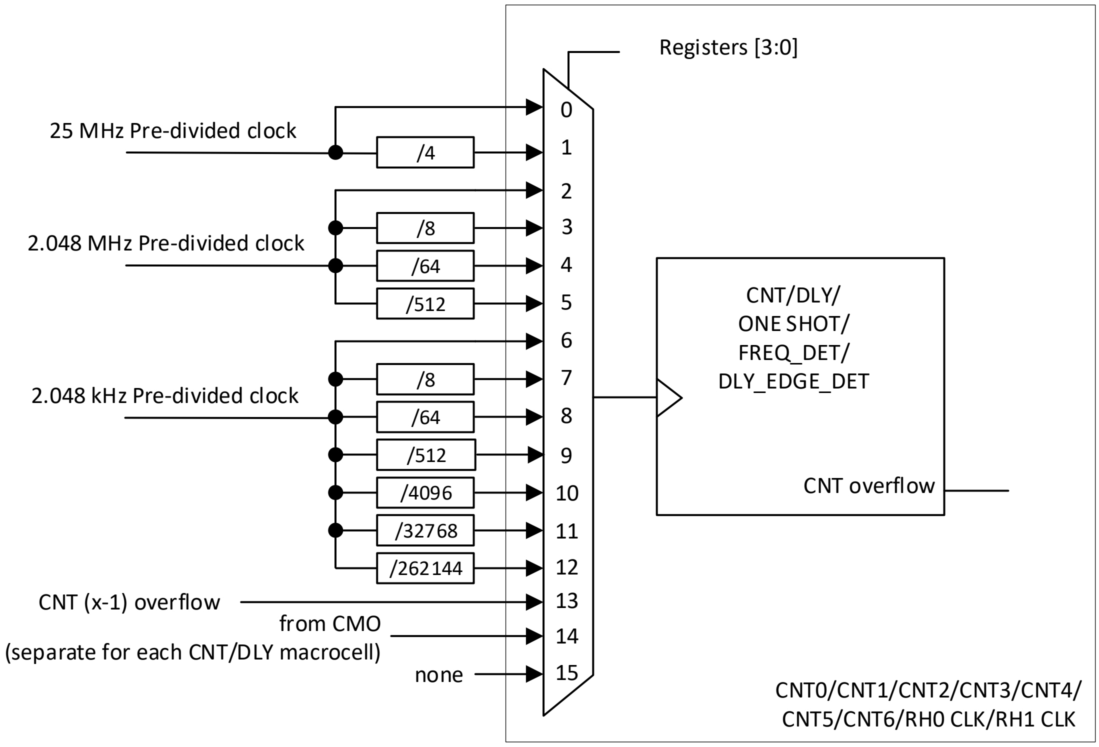


Figure 214. Clock Scheme

16.6 External Clocking

The SLG47004-A supports several ways to use an external, higher accuracy clock as a reference source for internal operations.

16.6.1 IO10 Source for Oscillator0 (2.048 kHz)

When register [722] is set to 1, an external clocking signal on IO0 will be routed in place of the internal oscillator derived 2.048 kHz clock source. See Figure 211. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.2 IO1 Source for Oscillator1 (2.048 MHz)

When register [690] is set to 1, an external clocking signal on IO1 will be routed in place of the internal oscillator derived 2.048 MHz clock source. See Figure 212. The high and low limits for frequency that can be selected are 0 MHz and 10 MHz.

16.6.3 IO2 Source for Oscillator2 (25 MHz)

When register [706] is set to 1, an external clocking signal on IO2 will be routed in place of the internal oscillator derived 25 MHz clock source. See Figure 213. The external frequency range is 0 MHz to 20 MHz at V_{DD} = 2.4 V, 0 MHz to 30 MHz at V_{DD} = 3.3 V, 0 MHz to 50 MHz at V_{DD} = 5.0 V. When an external clock is selected for OSC2, the oscillator's output signal will be inverted with respect to the IO2 input signal.

16.7 Oscillators Power-On Delay

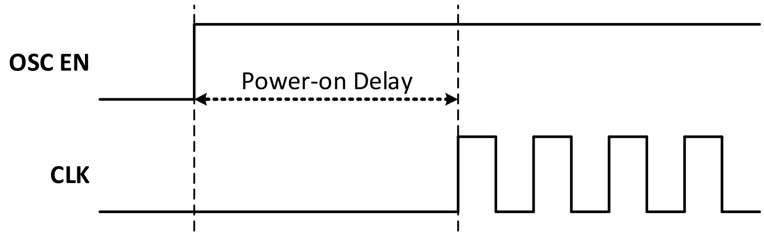


Figure 215. Oscillator Startup Diagram

Note 1: OSC power mode: “Auto Power-On”.
Note 2: OSC enable” signal appears when any macrocell that uses OSC is powered on.

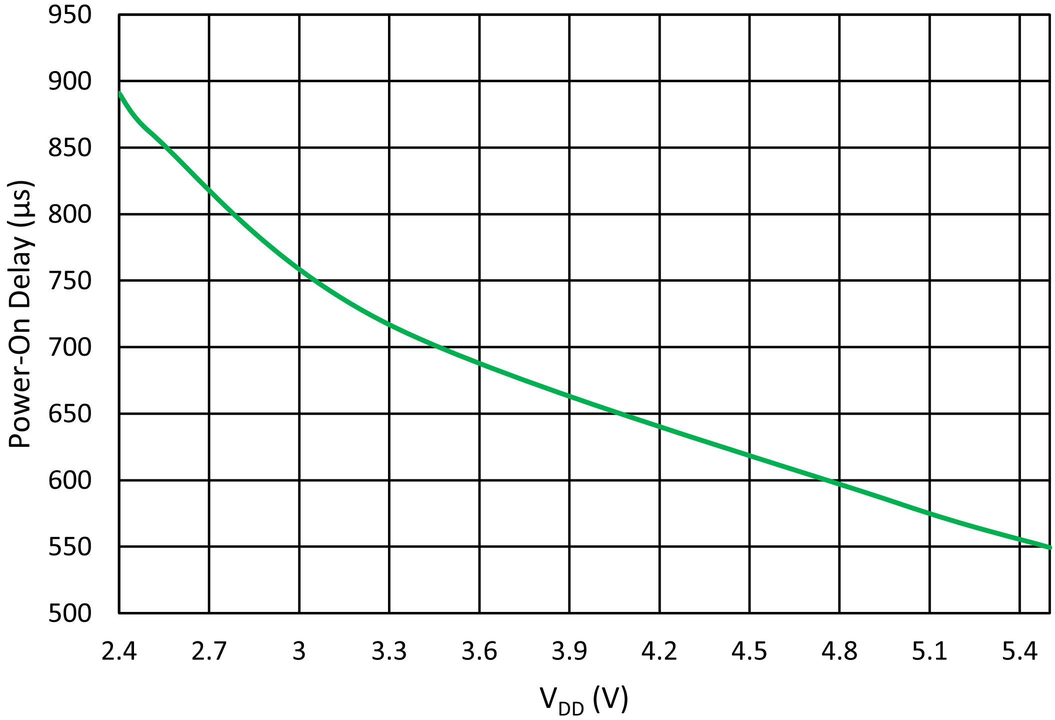


Figure 216. OSC0 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC0 = 2.048 kHz

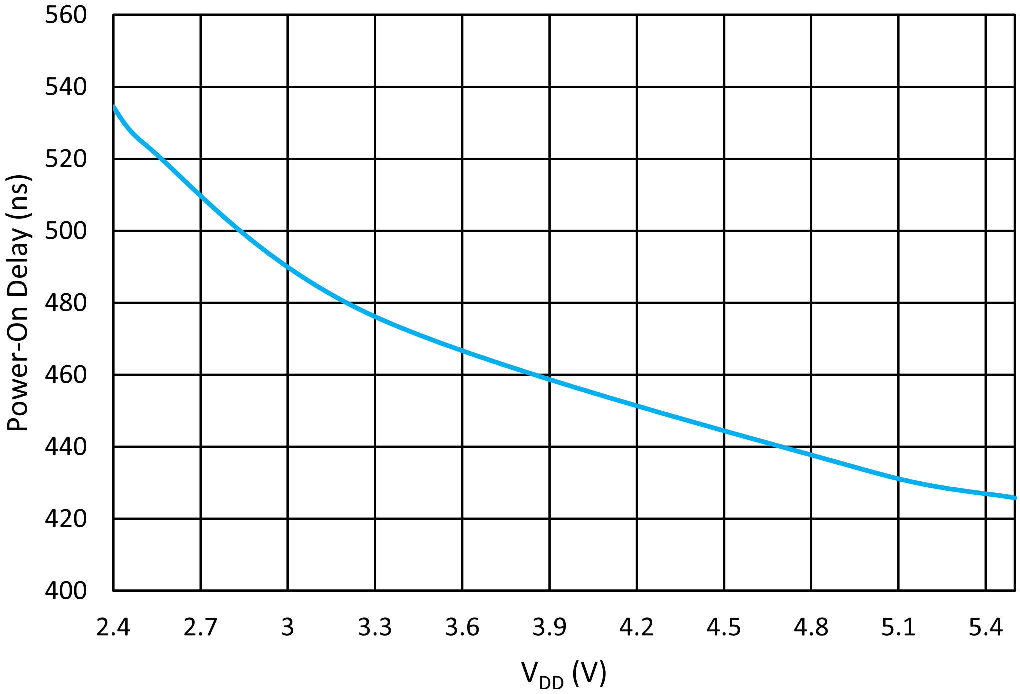


Figure 217. OSC1 Oscillator Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC1 = 2.048 MHz

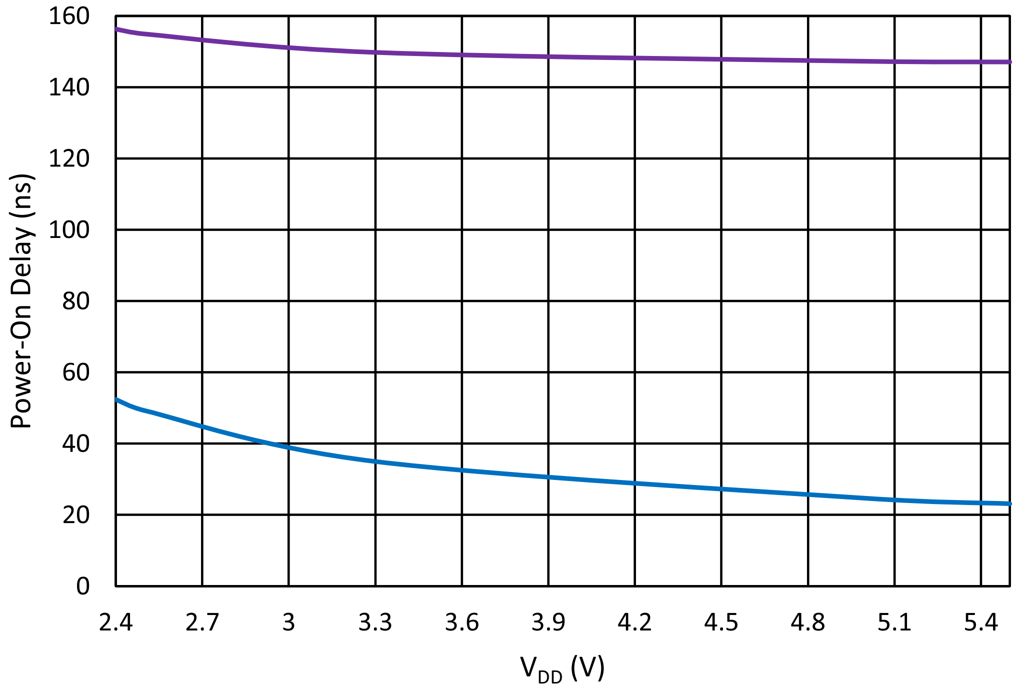


Figure 218. OSC2 Maximum Power-On Delay vs. V_{DD} at T_A = 25 °C, OSC2 = 25 MHz

16.8 Oscillators Accuracy

Note: OSC power setting: Force Power-On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

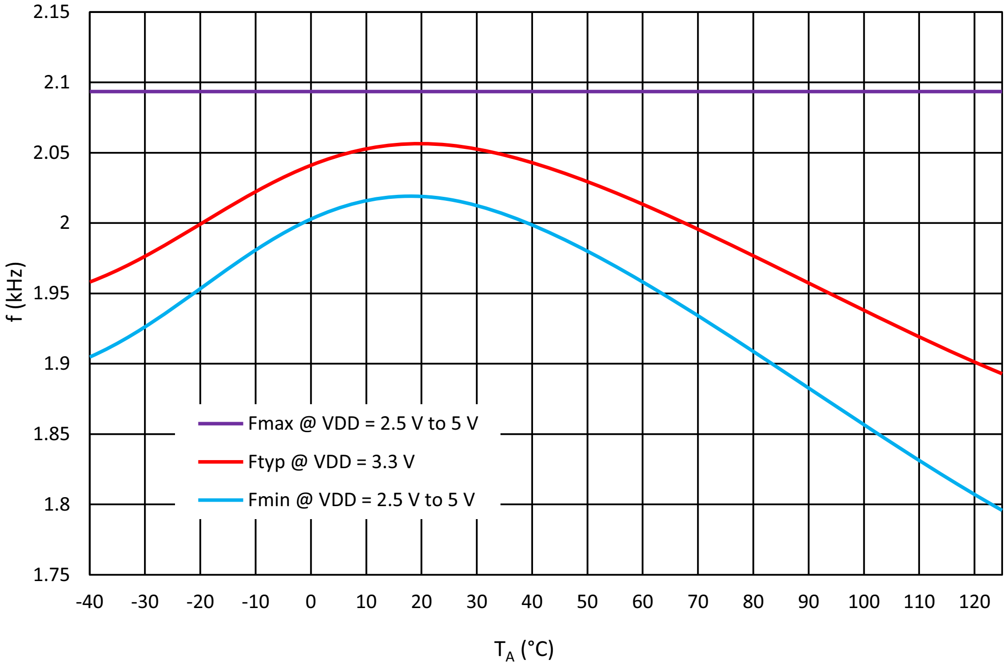


Figure 219. OSC0 Frequency vs. Ambient Temperature, OSC0 = 2.048 kHz

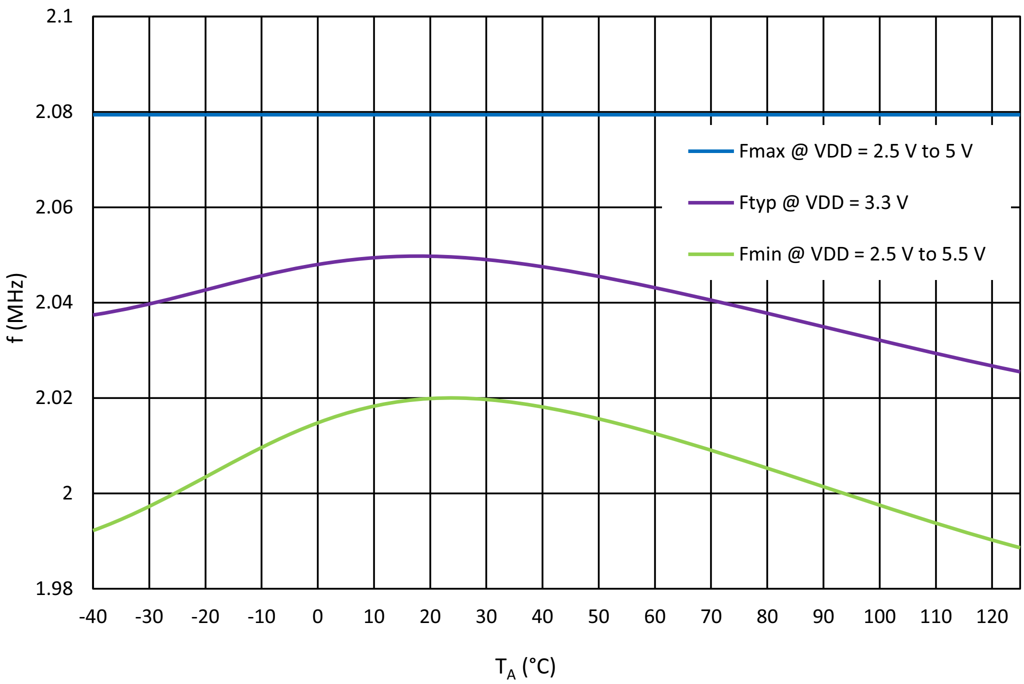


Figure 220. OSC1 Frequency vs. Ambient Temperature, OSC1 = 2.048 MHz

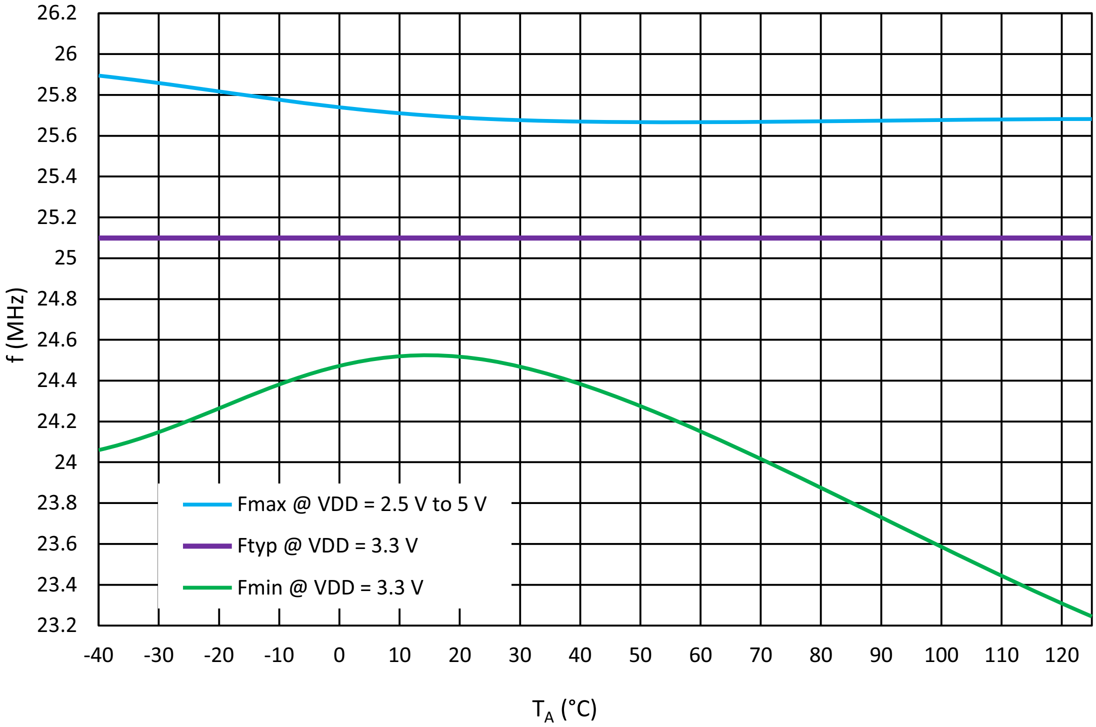


Figure 221. OSC2 Frequency vs. Ambient Temperature, OSC2 = 25 MHz

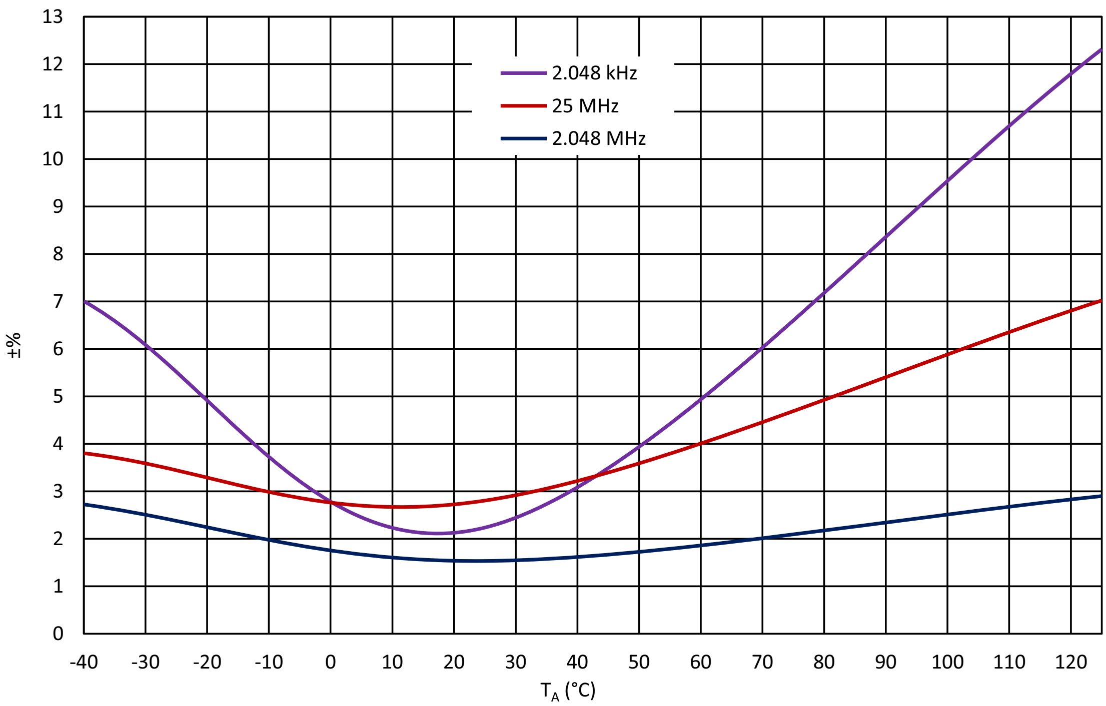


Figure 222. Oscillators Total Error vs. Ambient Temperature at V_{DD} = 2.4 V to 5.5 V

Note: For more information see Section 3.9.

16.9 Oscillators Settling Time

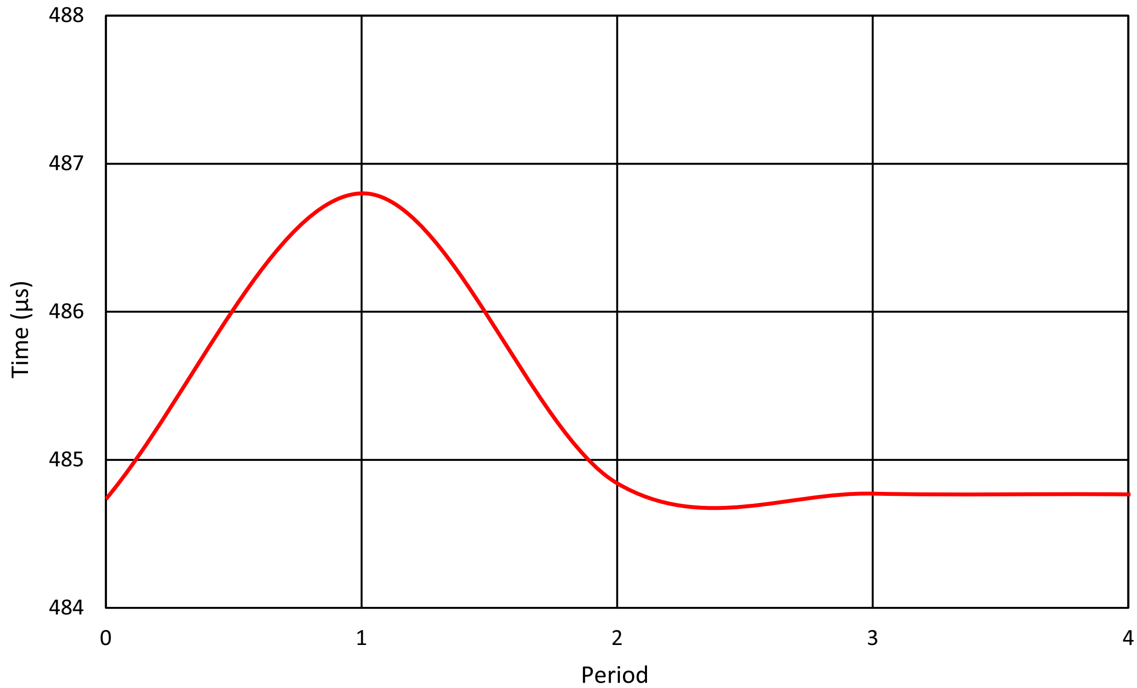


Figure 223. Oscillator0 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC0 = 2 kHz

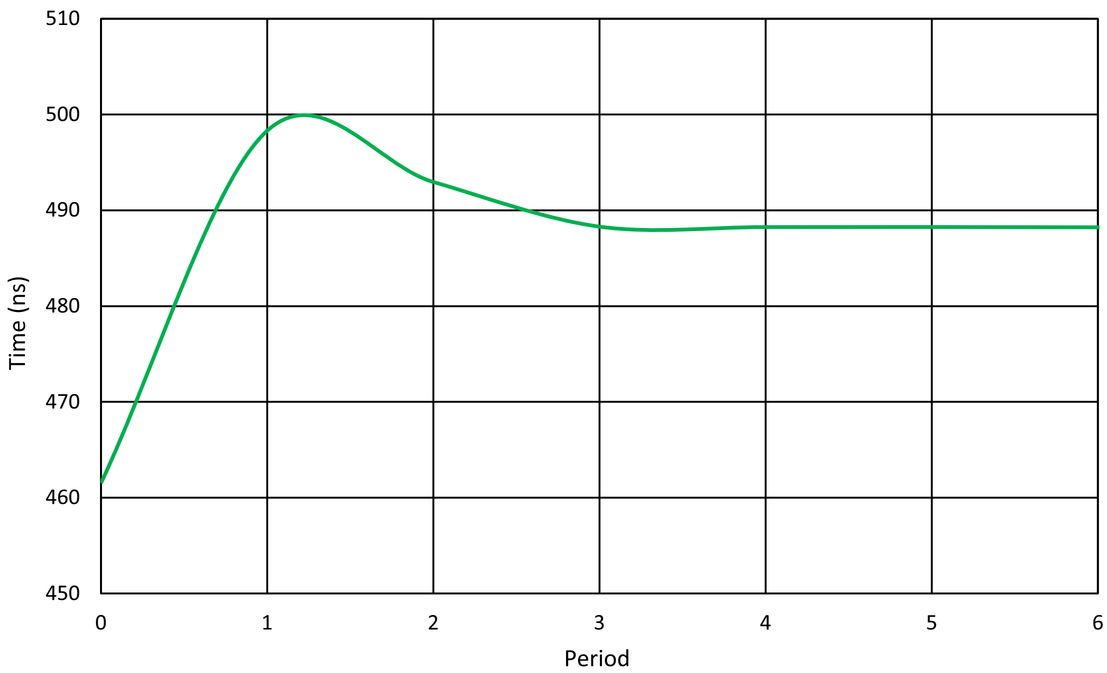


Figure 224. Oscillator1 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC1 = 2 MHz

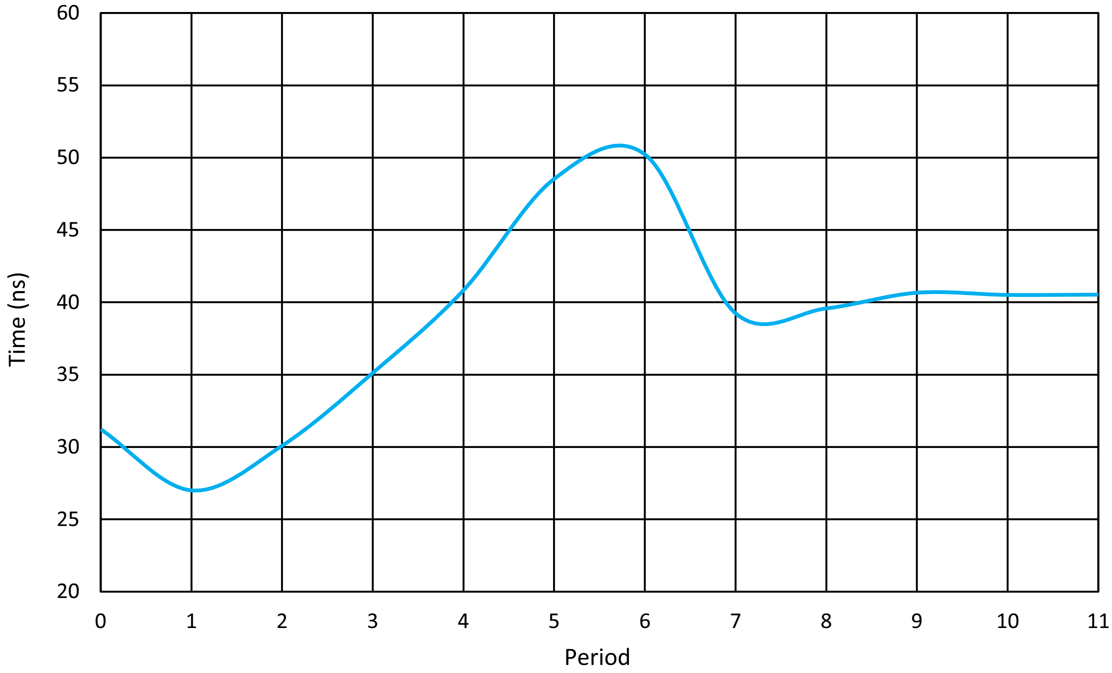


Figure 225. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Normal Start)

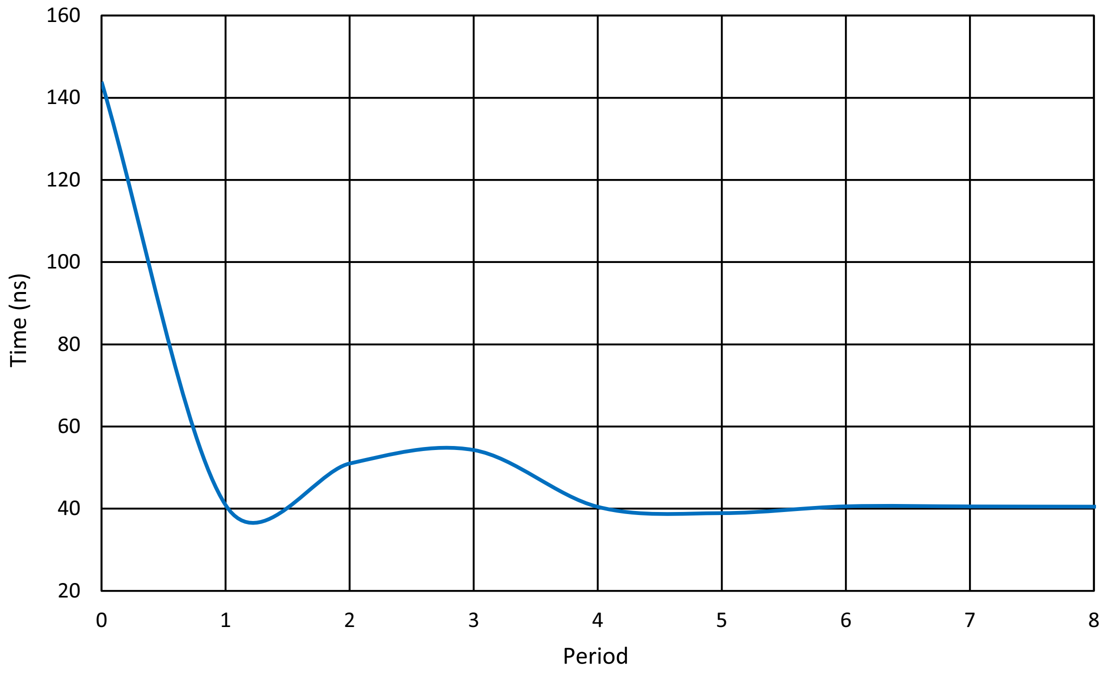


Figure 226. Oscillator2 Settling Time, V_{DD} = 3.3 V, T_A = 25 °C, OSC2 = 25 MHz (Start with Delay)

16.10 Oscillators Current Consumption

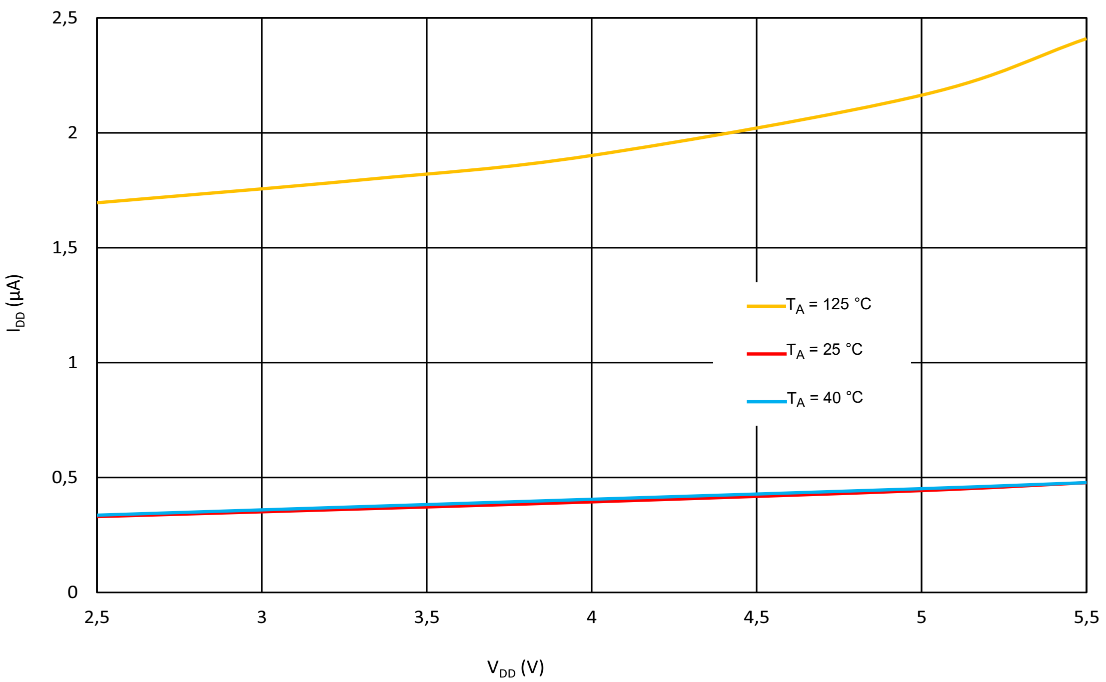


Figure 227. OSC0 Current Consumption vs. V_{DD} (All Pre-Dividers)

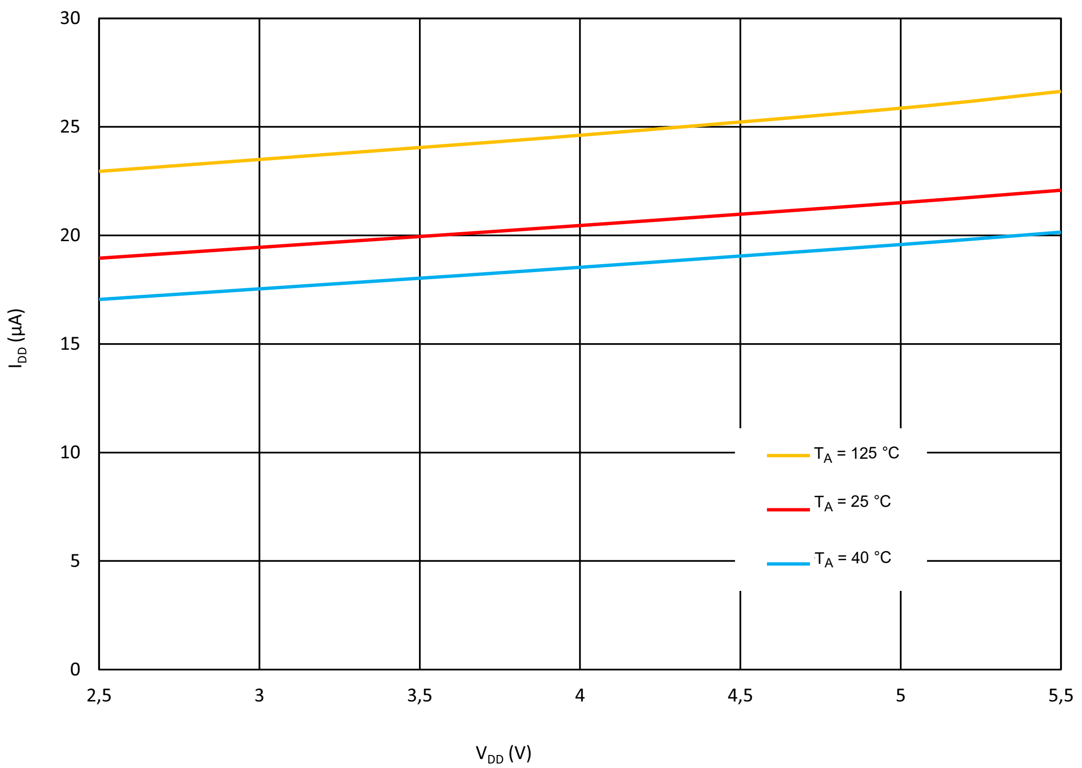


Figure 228. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 1)

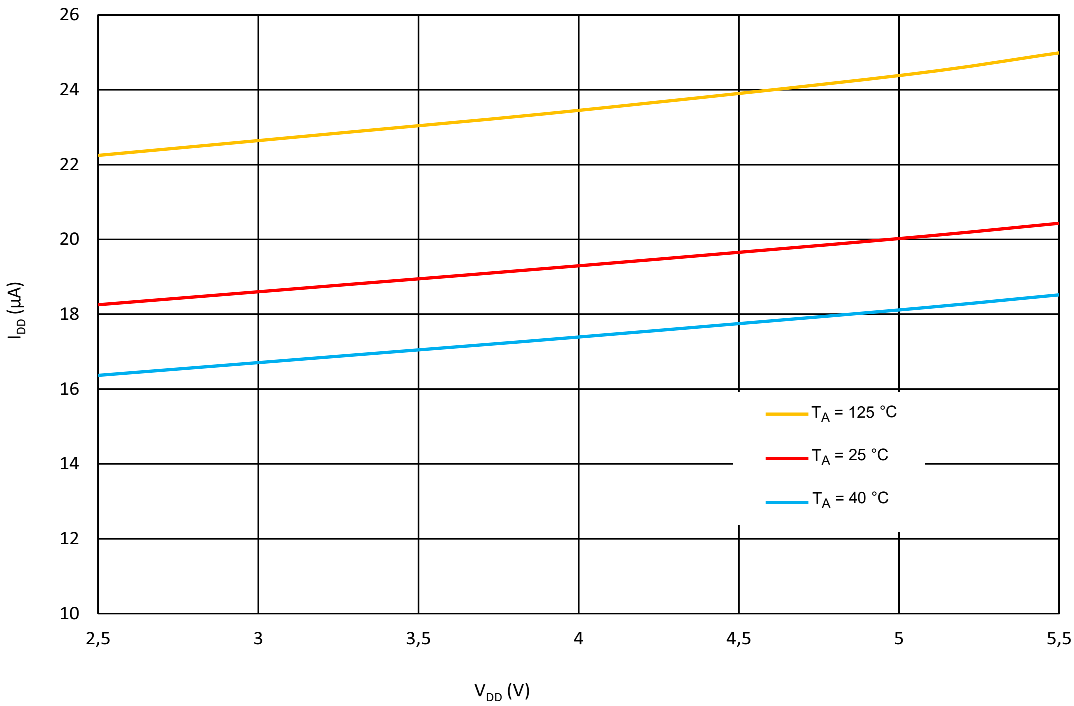


Figure 229. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 4)

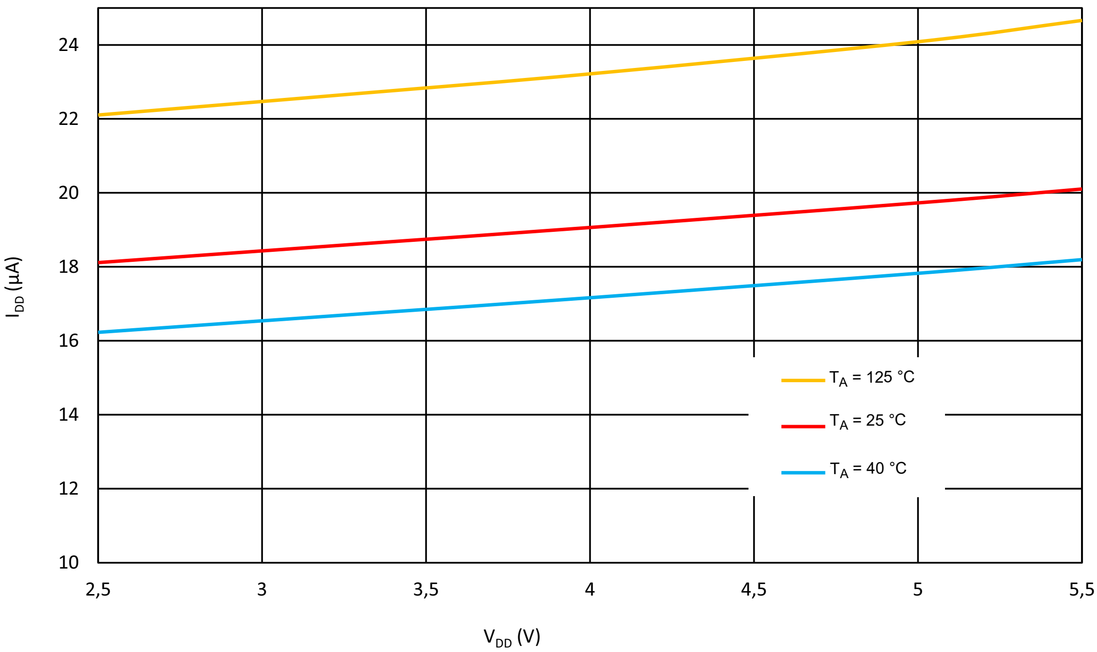


Figure 230. OSC1 Current Consumption vs. V_{DD} (Pre-Divider = 8)

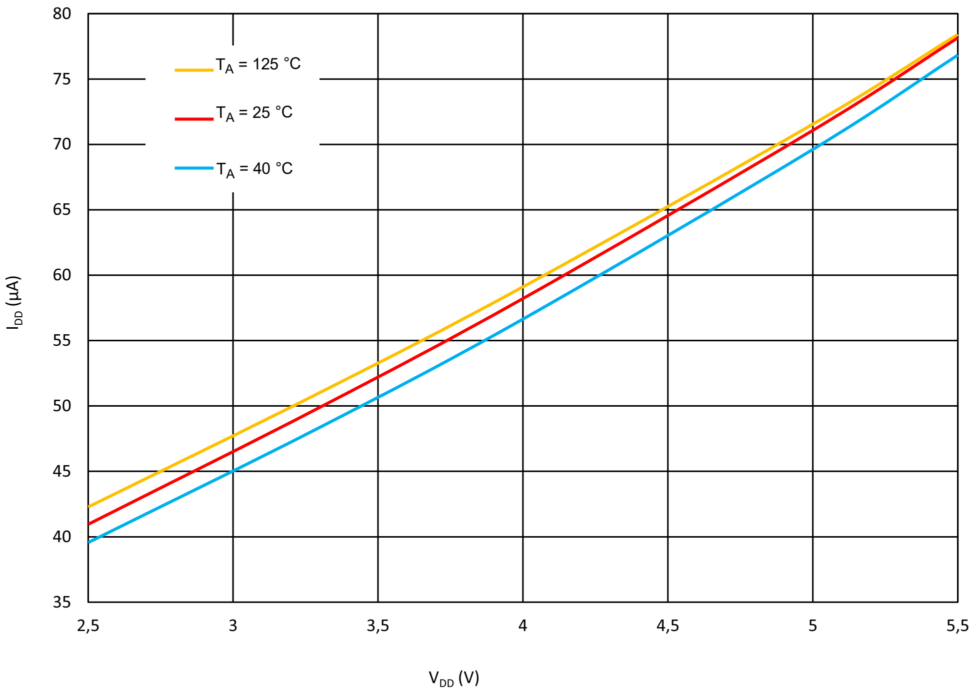


Figure 231. OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 1)

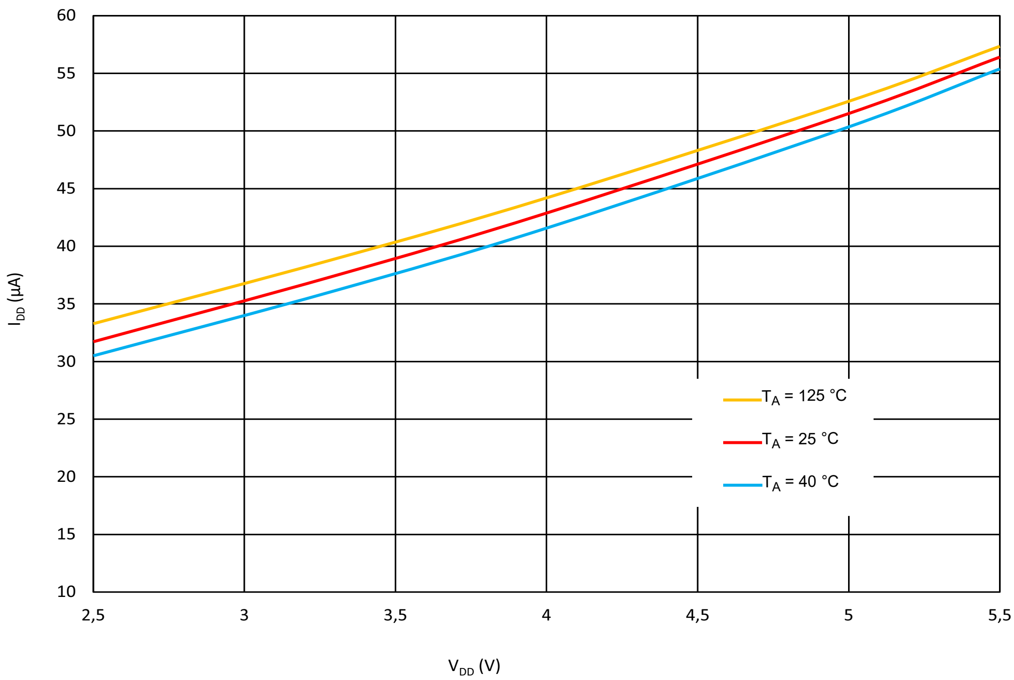


Figure 232. OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 4)

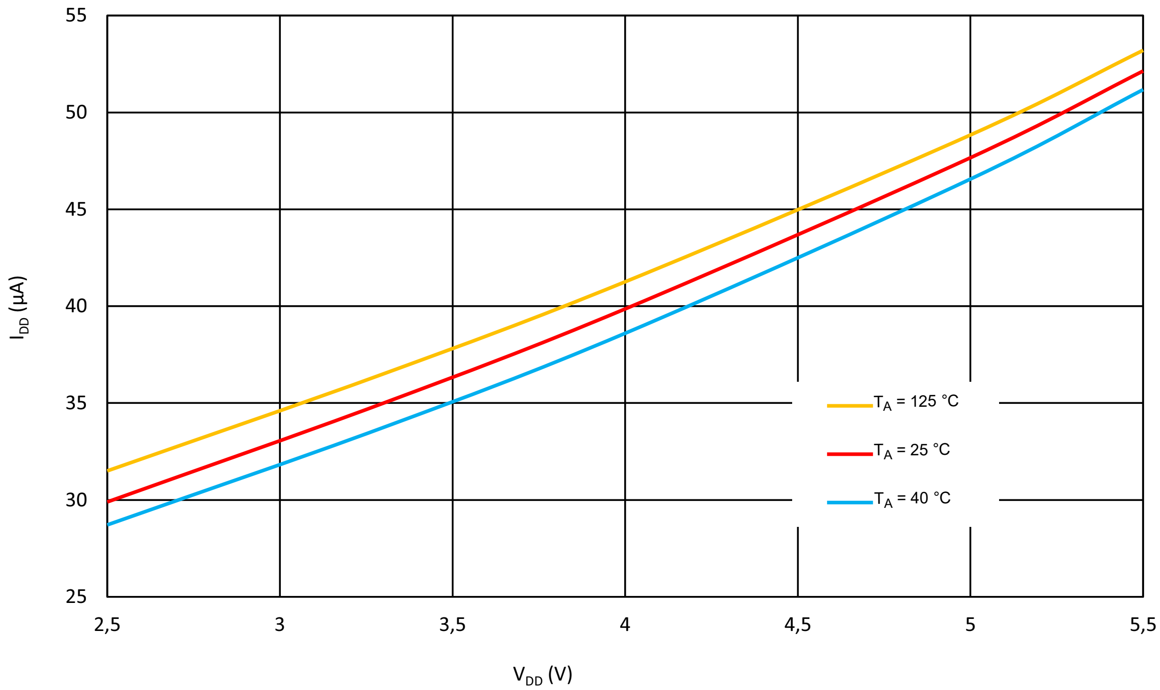


Figure 233. OSC2 Current Consumption vs. V_{DD} (Pre-Divider = 8)

17. Power-On Reset

The SLG47004-A has a Power-On Reset (POR) macrocell to ensure correct device initialization and operation of all macrocells in the device. The purpose of the POR circuit is to have consistent behavior and predictable results when the V_{DD} power is first ramping to the device, and also while the V_{DD} is falling during Power-down. To accomplish this goal, the POR drives a defined sequence of internal events that trigger changes to the states of different macrocells inside the device, and finally to the state of the IOs.

17.1 General Operation

The SLG47004-A is guaranteed to be powered down and non-operational when the V_{DD} voltage (voltage on PIN13) is less than Power-Off Threshold (see in Table 7), but not less than -0.6 V. Another essential condition for the chip to be powered down is that no voltage higher (Note) than the V_{DD} voltage is applied to any other PIN. For example, if V_{DD} voltage is 0.3 V, applying a voltage higher than 0.3 V to any other PIN is incorrect, and can lead to incorrect or unexpected device behavior.

Note: There is a 0.6 V margin due to forward drop voltage of the ESD protection diodes.

To start the POR sequence in the SLG47004-A, the voltage applied on the V_{DD} should be higher than the Power-On Threshold (Note). The full operational V_{DD} range for the SLG47004-A is 2.4 V to 5.5 V. This means that the V_{DD} voltage must ramp up to the operational voltage value, but the POR sequence will start earlier, as soon as the V_{DD} voltage rises to the Power-On Threshold. After the POR sequence has started, the SLG47004-A will have a typical Startup Time (see in Table 7) to go through all the steps in the sequence, and will be ready and completely operational after the POR sequence is complete.

Note: The Power-On Threshold is defined in Table 7.

To power down the chip, the V_{DD} voltage should be lower than the operational and to guarantee that chip is powered down, it should be less than Power-Off Threshold.

All PINs are in high impedance state when the chip is powered down and while the POR sequence is taking place. The last step in the POR sequence releases the IO structures from the high impedance state, at which time the device is operational. The pin configuration at this point in time is defined by the design programmed into the chip. Also, as it was mentioned before, the voltage on PINs can't be bigger than the V_{DD}, this rule also applies to the case when the chip is powered on.

17.2 POR Sequence

The POR system generates a sequence of signals that enable certain macrocells. The sequence is shown in Figure 234.

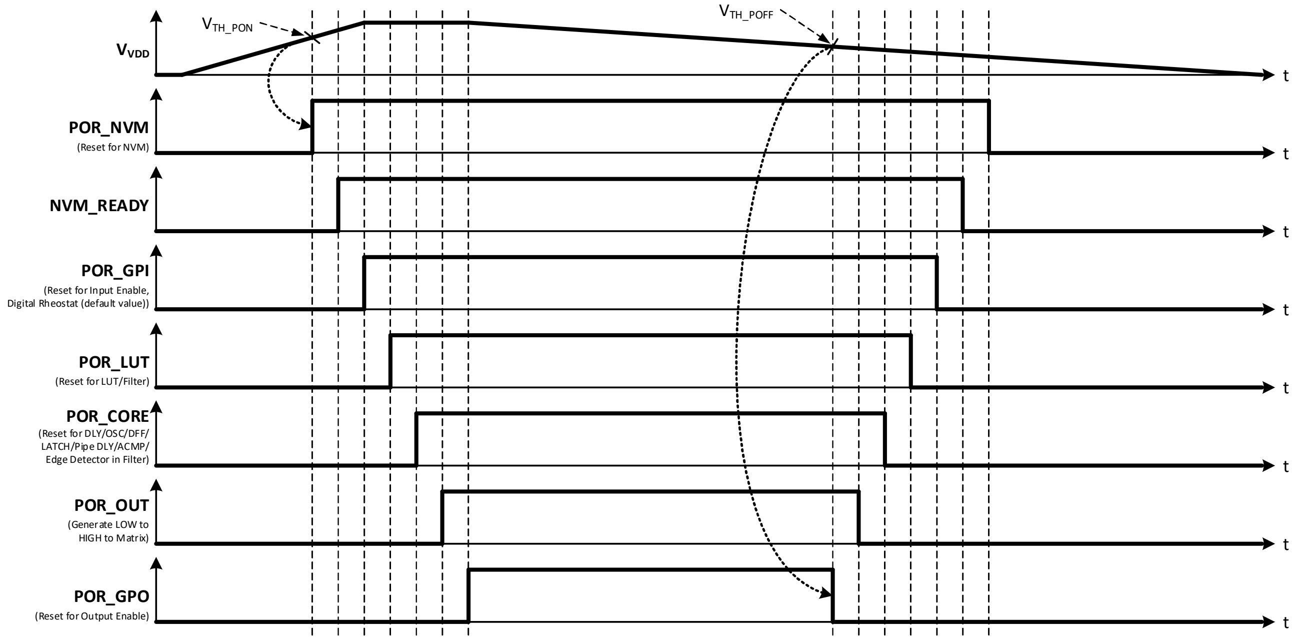


Figure 234. POR Sequence

As can be seen from Figure 234 after the V_{DD} has started ramping up and crossed the Power-On Threshold, first, the on-chip NVM memory is reset. Next, the chip reads the data from NVM and transfers this information to a CMOS LATCH, that serves to configure each macrocell, and the Connection Matrix, which routes signals between macrocells. The third stage causes the reset of the input pins, and then enables them. At that time Digital Rheostats value is set to its default value. After that, the LUTs are reset and become active. After LUTs, the Delay cells, OSCs, DFFs, LATCHES, and Pipe Delay are initialized. Only after all macrocells are initialized, internal POR signal (POR macrocell output) goes from LOW to HIGH (POR_OUT in Figure 234). The last portion of the device to be initialized is the output pins, which transition from high impedance to active at this point.

The typical time that takes to complete the POR sequence varies by device type in the GreenPAK family. It also depends on many environmental factors, such as: slew rate, V_{DD} value, temperature, and even will vary from chip to chip (process influence).

17.3 Macrocells Output States during POR Sequence

To have a full picture of SLG47004-A operation during powering and POR sequence refer to Figure 235, which describes the macrocell output states during the POR sequence.

First, before the NVM has been reset, all macrocells have their output set to logic LOW (except the output pins which are in high impedance state). On the next step, some of the macrocells start initialization: input pins output state becomes LOW; Digital Rheostats value is set to its default value; LUTs also output LOW. After that input pins are enabled. Next, only LUTs are configured. Then, all other macrocells are initialized. After macrocells are initialized, internal POR matrix signal switches from LOW to HIGH. The last are output pins that become active and determined by the input signals.

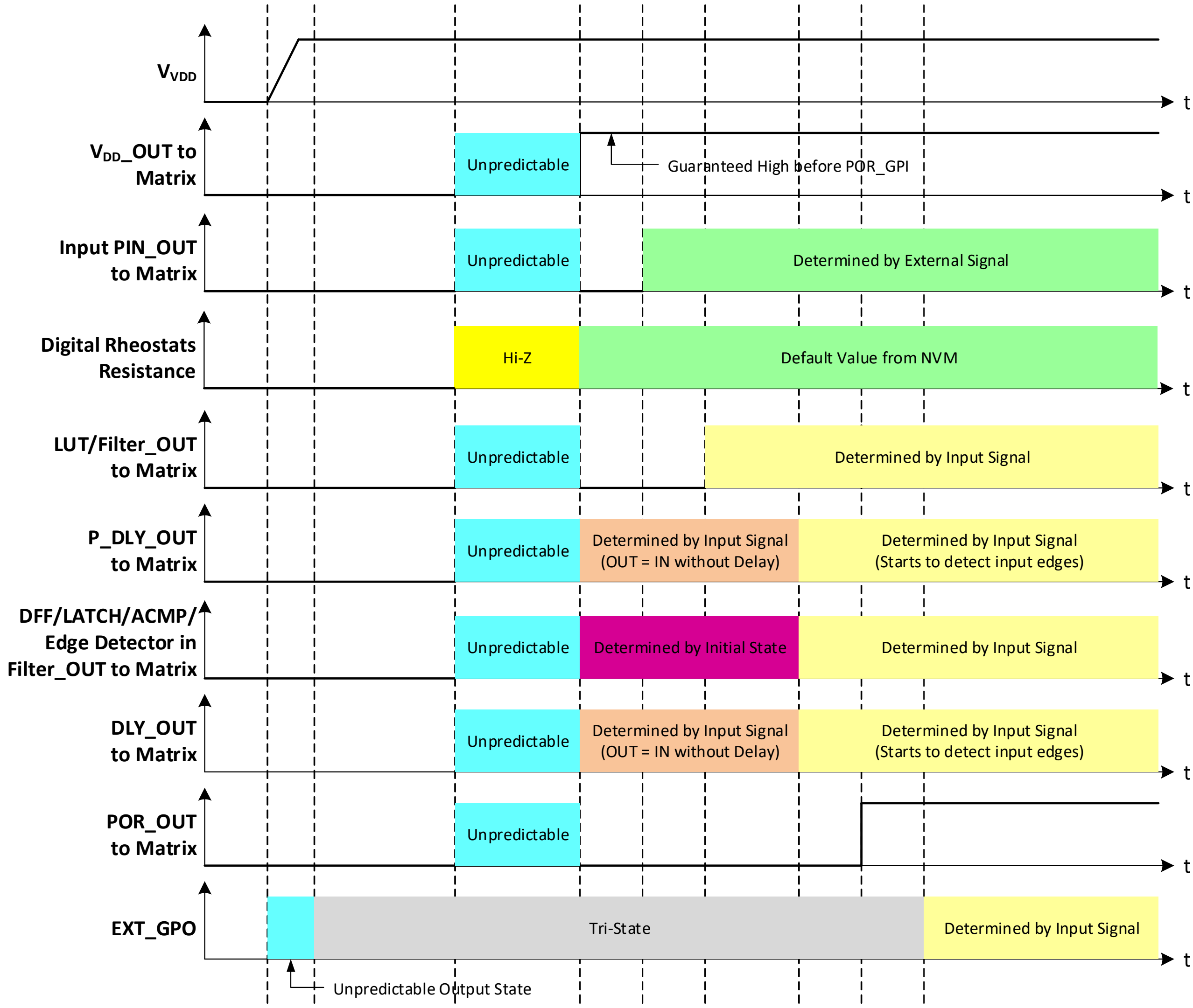


Figure 235. Internal Macrocell States during POR Sequence

17.3.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated power-up time of 1.63 V to 2.05 V, macrocells in SLG47004-A are powered on while forced to the reset state. All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input pins, Pull-up/down, Digital Rheostat, Op Amps.
2. LUTs.
3. DFFs, Delays/Counters, Pipe Delay, OSCs, ACMPs.
4. POR output to matrix.
5. Output pin corresponds to the internal logic.

The Vref output pin driving signal can precede POR output signal going high by 3 µs to 5 µs. The POR signal going high indicates the mentioned power-up sequence is complete.

Note: The maximum voltage applied to any pin should not be higher than the V_{DD} level. There are ESD Diodes between pin → V_{DD} and pin → GND on each pin. Exceeding V_{DD} results in leakage current on the input pin, and V_{DD} will be pulled up, following the voltage on the input pin.

17.3.2 Power-Down

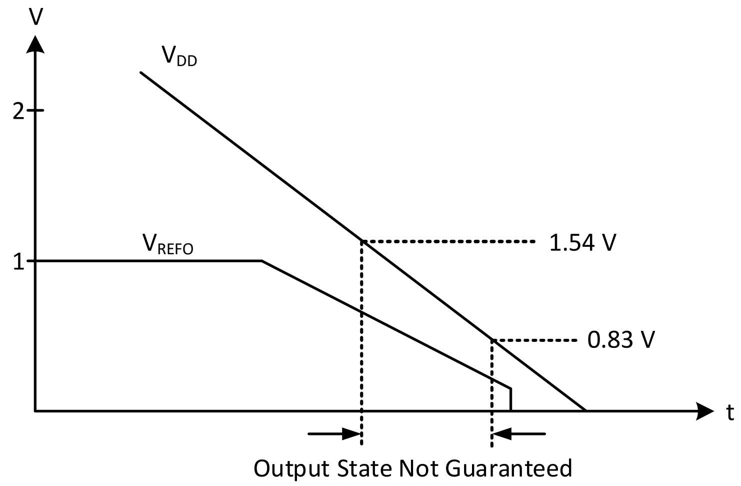


Figure 236. Power-Down

During Power-down, macrocells in SLG47004-A are powered off after V_{DD} falling down below Power-Off threshold. Please note, that during a slow rampdown outputs can possibly switch state.

18. I^2C Serial Communications Macrocell

18.1 I^2C Serial Communications Macrocell Overview

In the standard use case for the GreenPAK devices, the configuration choices made by the user are stored as bit settings in the Non-Volatile Memory (NVM), and this information is transferred at startup time to volatile RAM registers that enable the configuration of the macrocells. Other RAM registers in the device are responsible for setting the connections in the Connection Matrix to route signals in the manner most appropriate for the user's application.

The I^2C Serial Communications Macrocell in this device allows an I^2C bus Master to read and write this information via a serial channel directly to the RAM registers, allowing the remote re-configuration of macrocells, and remote changes to signal chains within the device.

The I^2C bus Master is also able to read and write other register bits that are not associated with NVM memory. As an example, the input lines to the Connection Matrix can be read as digital register bits. These are the signal outputs of each of the macrocells in the device, giving the I^2C bus Master the capability to remotely read the current value of any macrocell.

The user has the flexibility to control read access and write access via registers bits registers [1795:1792]. See Section 19. Non-Volatile Memory for more details on I^2C read/write memory protection.

18.2 I^2C Serial Communications Device Addressing

Each command to the I^2C Serial Communications macrocell begins with a Control Byte. The bits inside this Control Byte are shown in Figure 237. After the Start bit, the first four bits are a control code. Each bit in a control code can be sourced independently from the register or by value defined externally by IO1, IO2, IO3, and IO4. The LSB of the control code is defined by the value of IO1, while the MSB is defined by the value of IO4. The address source (either register bit or PIN) for each bit in the control code is defined by registers [1019:1016]. This gives the user flexibility on the chip level addressing of this device and other devices on the same I^2C bus.The default control code is 0001. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read or written by the command. The last bit in the Control Byte is the R/W bit, which selects whether a read command or write command is requested, with a "1" selecting for a Read command, and a "0" selecting for a Write command. This Control Byte will be followed by an Acknowledge bit (ACK), which is sent by this device to indicate successful communication of the Control Byte data.

In the I^2C-bus specification and user manual there are two groups of eight addresses (0000 xxx and 1111 xxx) that are reserved for the special functions, such as a system General Call address. If the user of this device choses to set the Control Code to either "1111" or "0000" in a system with other slave device, please consult the I^2C-bus specification and user manual to understand the addressing and implementation of these special functions, to ensure reliable operation.

In the read and write command address structure, there are a total of 11 bits of addressing, each pointing to a unique byte of information, resulting in a total address space of 2K bytes. The valid addresses are shown in the memory map in Figure 247.

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address.

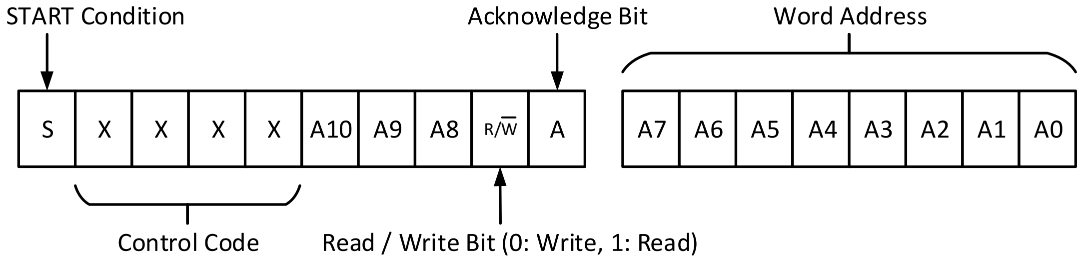


Figure 237. Basic Command Structure

18.3 I²C Serial General Timing

General timing characteristics for the I²C Serial Communications macrocell are shown in Figure 238. Timing specifications can be found in Section 3.4 Electrical Specifications.

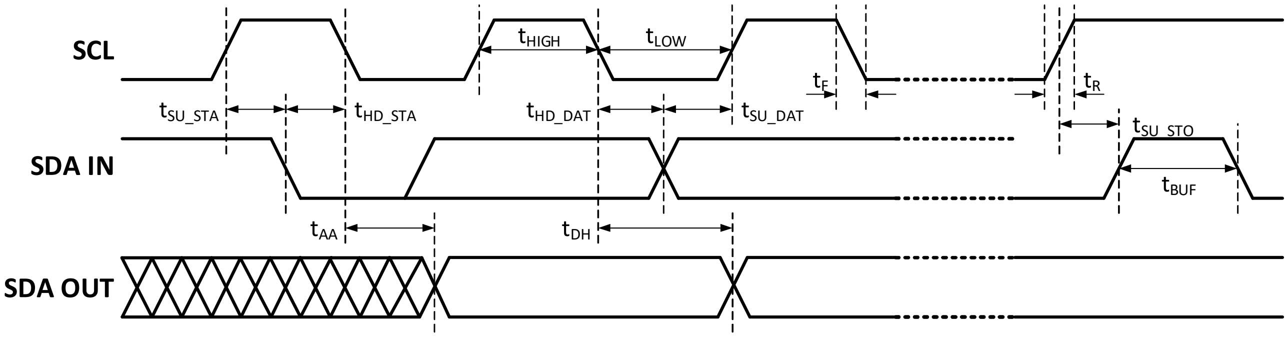


Figure 238. I²C General Timing Characteristics

18.4 I²C Serial Communications Commands

18.4.1 Byte Write Command

Following the Start condition from the Master, the Control Code [4 bits], the Block Address [3 bits], and the R/W bit (set to "0") are placed onto the I²C bus by the Master. After the SLG47004-A sends an Acknowledge bit (ACK), the next byte transmitted by the Master is the Word Address. The Block Address (A10, A9, A8), combined with the Word Address (A7 through A0), together set the internal address pointer in the SLG47004-A, where the data byte is to be written. After the SLG47004-A sends another Acknowledge bit, the Master will transmit the data byte to be written into the addressed memory location. The SLG47004-A again provides an Acknowledge bit and then the Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG47004-A generates the Acknowledge bit.

It is possible to latch all IOs during I²C write command to the register configuration data (block address A10, A9, A8 = 000), register [985] = 1 - Enable. It means that IOs will remain their state until the write command is done.

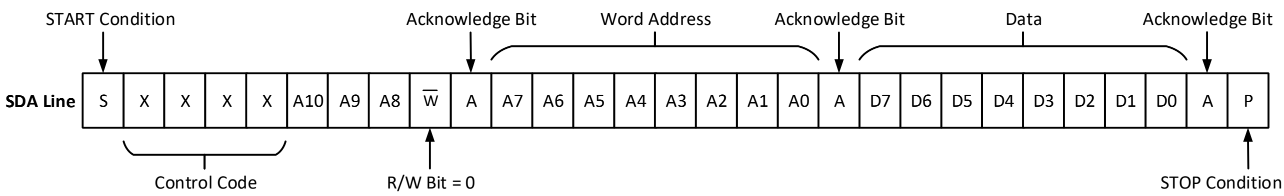


Figure 239. Byte Write Command, R/W = 0

18.4.2 Sequential Write Command

The write Control Byte, Word Address, and the first data byte are transmitted to the SLG47004-A in the same way as in a Byte Write command. However, instead of generating a Stop condition, the Bus Master continues to transmit data bytes to the SLG47004-A. Each subsequent data byte will increment the internal address counter, and will be written into the next higher byte in the command addressing. As in the case of the Byte Write command, the internal write cycle will take place at the time that the SLG47004-A generates the Acknowledge bit.

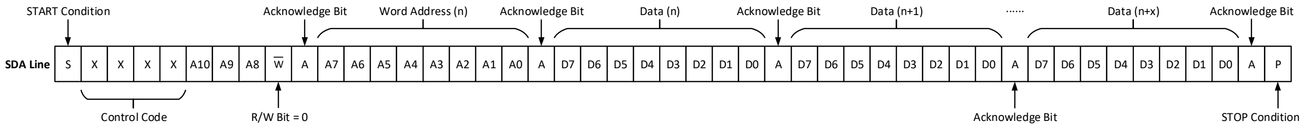


Figure 240. Sequential Write Command

18.4.3 Current Address Read Command

The Current Address Read Command reads from the current pointer address location. The address pointer is incremented at the first STOP bit following any write control byte. For example, if a Sequential Read command (which contains a write control byte) reads data up to address n, the address pointer would get incremented to n + 1 upon the STOP of that command. Subsequently, a Current Address Read that follows would start reading data at n + 1. The Current Address Read Command contains the Control Byte sent by the Master, with the R/W̄ bit = “1”. The SLG47004-A will issue an Acknowledge bit, and then transmit eight data bits for the requested byte. The Master will not issue an Acknowledge bit, and follow immediately with a Stop condition.

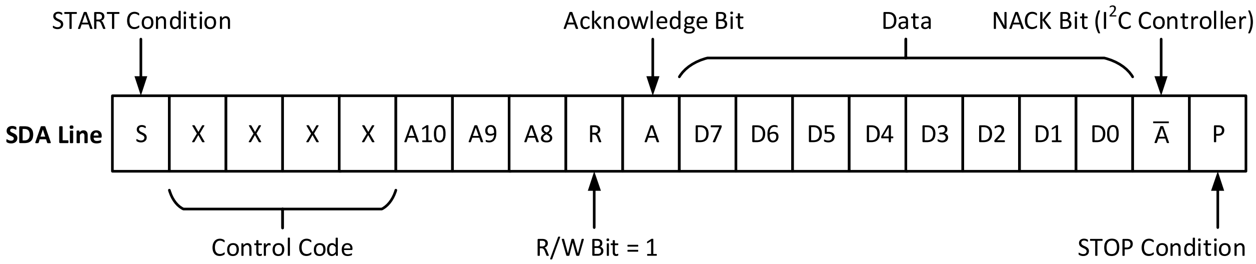


Figure 241. Current Address Read Command, R/W = 1

18.4.4 Random Read Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG47004-A issues an Acknowledge bit followed by the requested eight data bits.

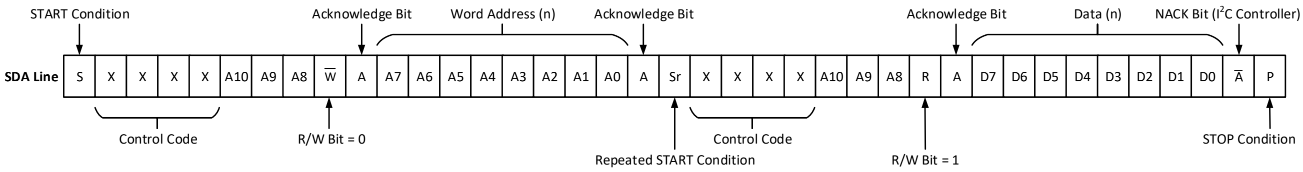


Figure 242. Random Read Command

18.4.5 Sequential Read Command

The Sequential Read command is initiated in the same way as a Random Read command, except that once the SLG47004-A transmits the first data byte, the Bus Master issues an Acknowledge bit as opposed to a Stop condition in a random read. The Bus Master can continue reading sequential bytes of data, and will terminate the command with a Stop condition.

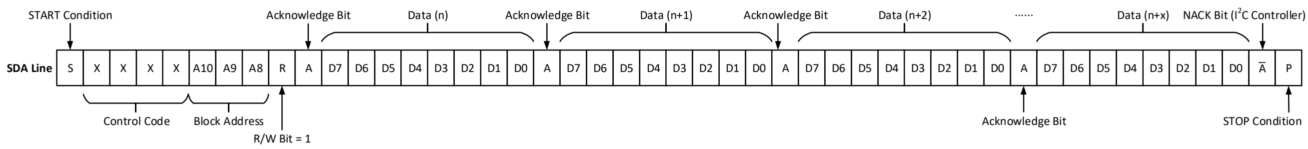


Figure 243. Sequential Read Command

18.4.6 I²C Serial Reset Command

If I²C serial communication is established with the device, it is possible to reset the device to initial power up conditions, including configuration of all macrocells and all connections provided by the Connection Matrix. This is implemented by setting register [984] I²C reset bit to “1”, which causes the device to re-enable the Power-On Reset (POR) sequence, including the reload of all register data from NVM. During the POR sequence, the outputs of the device will be in tri-state. After the reset has taken place, the contents of register [984] will be set to “0” automatically. Figure 244 illustrates the sequence of events for this reset function.

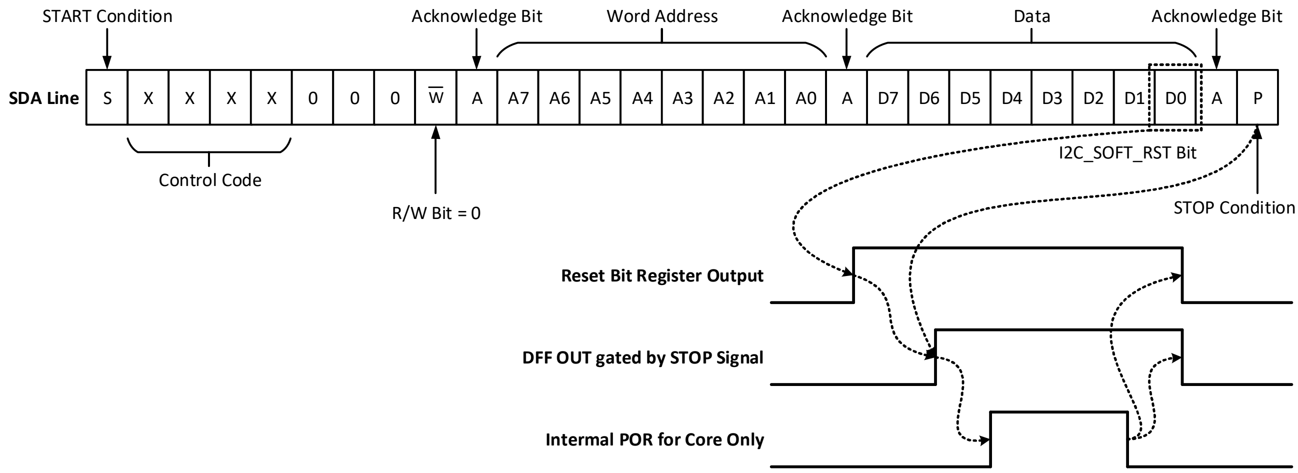


Figure 244. Reset Command Timing

18.5 Chip Configuration Data Protection

The SLG47004-A utilizes a scheme that allows a portion or the entire Register and NVM to be inhibited from being read or written/erased. There are two bytes that define the register and NVM access or change. The second byte NPR defines the chip NVM data configuration read and write protection. The first byte RPR defines the register read and write protection. If desired, the protection lock bit (PRL) can be set so that protection may no longer be modified, thereby making the current protection scheme permanent. The status of the RPR and NPR can be determined by following a Random Read sequence. Changing the state of the RPR and NPR is accomplished with a Byte Write sequence with the requirements outlined in this section.

Special care must be taken when NVM page 14 is rewritten (registers [1919:1792]). This page contains rheostats tolerance data that can be permanently lost during write/erase operation.

The RPR register is located on 0xE0 address, while NPR is located on 0xE1 address.

The RPR format is shown in Table 63, and the RPR bit functions are included in Table 64.

Table 63. RPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
RPR				RH_PRB	RPRB3	RPRB2	RPRB1	RPRB0

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

Table 64. RPR Bit Function Description

Bit	Name		Type	Description
4	RH_PRB	--	R/W*	0: Program signal from connection matrix is enabled 1: Program signal from connection matrix is disabled
3:2	RPRB3	2k Register Write Selection Bits	R/W*	00: 2k register data is unprotected for write 01: 2k register data is partly protected for write, please refer to the Table 67 10: 2k register data is fully protected for write.
	RPRB2		R/W*	
1:0	RPRB1	2k Register Read Selection Bits	R/W*	00: 2k register data is unprotected for read 01: 2k register data is partly protected for read, please refer to the Table 67 10: 2k register data is fully protected for read.
	RPRB0		R/W*	

The NPR format is shown in Table 65, and the NPR bit functions are included in Table 66.

Table 65. NPR Format

	b7	b6	b5	b4	b3	b2	b1	b0
NPR							NPRB1	NPRB0

Table 66. NPR Bit Function Description

Bit	Name		Type	Description
1:0	NPRB1	2k NVM Configuration Selection Bits	R/W*	00: 2k NVM Configuration data is unprotected for read and write/erase 01: 2k NVM Configuration data is fully protected for read 10: 2k NVM Configuration data is fully protected for write/erase 11: 2k NVM Configuration data is fully protected for read and write/erase.
	NPRB0		R/W*	

* Becomes read only after PRL is high. The content is permanently locked for write and erase after PRL is high.

The protection selection bits allow different levels of protection of the register and NVM Memory Array.

There is a dedicated bit RH_PRB, that enables/disables "Program" signal of PT block to change NVM rheostats resistance values. If RH_PRB [1796] = 0, "Program" signal is enabled. If RH_PRB [1796] = 1, "Program" signal is disabled. Note that RH_PRB bit has no effect on I^{2}C access to NVM. To enable/disable I^{2}C access to rheostat resistance value, stored in NVM, user must change NPRB0, NPRB1 bits.

The Protect Lock Bit (PRL) is used to permanently lock (for write and erase) the current state of the RPR and NPR. A Logic 0 indicates that the protection byte can be modified, whereas a Logic 1 indicates the byte has been locked and can no longer be modified.

In this case it is impossible to erase the whole page 0x0E with protection bytes. The PRL is located at 0xE4 address (register [1824]).

18.6 I²C Serial Command Register Map

There are nine read/write protect modes for the design sequence from being corrupted or copied. See Table 67 for details.

Table 67. Read/Write Register Protection Options

Configurations	Raw Die	Protection Modes Configuration									Test Mode	Register Address
		Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]		00	01	00	01	01	10	10	00	10		
RPR[3:2]		00	00	01	01	10	01	00	10	10		
I²C Byte Write Bit Masking (section 18.7.2 I2C Byte Write Bit Masking)	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	-	0xF6
I²C Serial Reset Command (section 18.4.6 I2C Serial Reset Command)	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	-	0x7Bb'0
Outputs Latching During I²C Write (section 18.7 I2C Additional Options)	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	-	0x7Bb'1
Connection Matrix Virtual Inputs (section 6.4 Connection Matrix Virtual Inputs)	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	-	0x7C
RH0_CNT Data	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	R/W	0xC0, 0xC1
RH1_CNT Data	R/W	R/W	R/W	R/W	R/W	R	W	W	R	-	R/W	0xD0, 0xD1
Macrocells Output Values (Connection Matrix Inputs, section 6.2 Matrix Input Table)	R	R	R	R	R	R	-	-	R	-	R	0xC4~ 0xCA
Counter Current Value	R	R	R	R	R	R	-	-	R	-	R	0xCB~ 0xCE
RH0_CNT Value	R/W	R	R	R	R	R	R	R	R	R	R	0xC2, 0xC3
RH1_CNT Value	R/W	R	R	R	R	R	R	R	R	R	R	0xD2, 0xD3
Protection Mode Selection (sections 18.6 I2C Serial Command Register Map)	R/W	R/W	R/W	R	R	R	R	R/W	R	R7	R	0xE4b'0

Table 67. Read/Write Register Protection Options (Cont.)

Configurations	Raw Die	Protection Modes Configuration									Test Mode	Register Address
		Unlock	Partly Lock Read	Partly Lock Write	Partly Lock Read/ Write	Partly Lock Read & Lock Write	Lock Read & Partly Lock Write	Lock Read	Lock Write	Lock Read/ Write		
RPR[1:0]		**00**	**01**	**00**	**01**	**01**	**10**	**10**	**00**	**10**		
RPR[3:2]		**00**	**00**	**01**	**01**	**10**	**01**	**00**	**10**	**10**		
I^{2}C Slave Address	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R	0x7Fb'3~ 0x7Fb'0
Pin slave address select	R/W	R/W	R/W					R/W				0x7Fb'7~ 0x7Fb'4
Service page lock	R/W	R	R	R	R	R	R	R	R	R	R	0xF3b'0
RH0 Tolerance Data	R/W	R	R	R	R	R	R	R	R	R	R	0xE6, 0xE7
RH1 Tolerance Data	R/W	R	R	R	R	R	R	R	R	R	R	0xE8, 0xE9
Protect Mode Config (RH_PRB,RPR, NPR,WPR)	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	0xE0, 0xE1, 0xE2
Page Erase byte	W**	W**	W**	W**	W**	W**	W**	W**	W**	W**	W**	0xE3
Macrocells Inputs Configuration (Connection Matrix Outputs,section 6.3 Matrix Output Table)	R/W	R/W	W	R	-	-	-	W	R	-	-	0x00~ 0x4A (0x4B reserved)
Configuration Bits for All Macrocells (IOs, ACMPs, Combination Function Macrocells, and others)	R/W	R/W	W	R	-	-	-	W	R	-	-	

R/W	Allow Read and Write Data
W	Allow Write Data Only
W**	Pages that can be erased are defined by NVM write protection
R	Allow Read Data Only
-	The Data is protected for Read and Write

Note 1: R/W becomes read only if protection mode selection (lock bit) is set to 1.
Note 2: R/W Readable/writable depend on the "Trim mode enable" bit. If "Trim mode enable" bit value = 1, then trim bits are enable.

It is possible to read some data from macrocells, such as counter current value, connection matrix, and connection matrix virtual inputs. The I^{2}C write will not have any impact on data in case data comes from macrocell output, except Connection Matrix Virtual Inputs. The silicon identification service bits allow identifying silicon family, its revision, and others.

R/W* - Becomes read only after PRL is high.

See Section 21. Register Definitions for detailed information on all registers.

18.7 I^{2}C Additional Options

When Output latching during I^{2}C write to the register configuration data (block address A10, A9, A8 = 000), registers [985] = 1 allows all PINs output value to be latched while register content is changing. It will protect the output change due to configuration process during I^{2}C write in case multiple register bytes are changed. Inputs and internal macrocells retain their status during I^{2}C write.

See Section 21. Register Definitions for detailed information on all registers.

18.7.1 Reading Counter Data via I^{2}C

The current count value in three counters in the device can be read via I^{2}C. The counters that have this additional functionality are 16-bit CNT0, and 8-bit counters CNT2 and CNT4.

18.7.2 I^{2}C Byte Write Bit Masking

The I^{2}C macrocell inside SLG47004-A supports masking of individual bits within a byte that is written to the RAM memory space. This function is supported across the entire RAM memory space. To implement this function, the user performs a Byte Write Command (see Section 18.4.1 Byte Write Command for details) on the I^{2}C Byte Write Mask Register (address 0xF6) with the desired bit mask pattern. This sets a bit mask pattern for the target memory location that will take effect on the next Byte Write Command to this register byte. Any bit in the mask that is set to “1” in the I^{2}C Byte Write Mask Register will mask the effect of changing that particular bit in the target register, during the next Byte Write Command. The contents of the I^{2}C Byte Write Mask Register are reset (set to 0x00) after valid Byte Write Command. If the next command received by the device is not a Byte Write Command, the effect of the bit masking function will be aborted, and the I^{2}C Byte Write Mask Register will be reset with no effect. Figure 245 shows an example of this function.

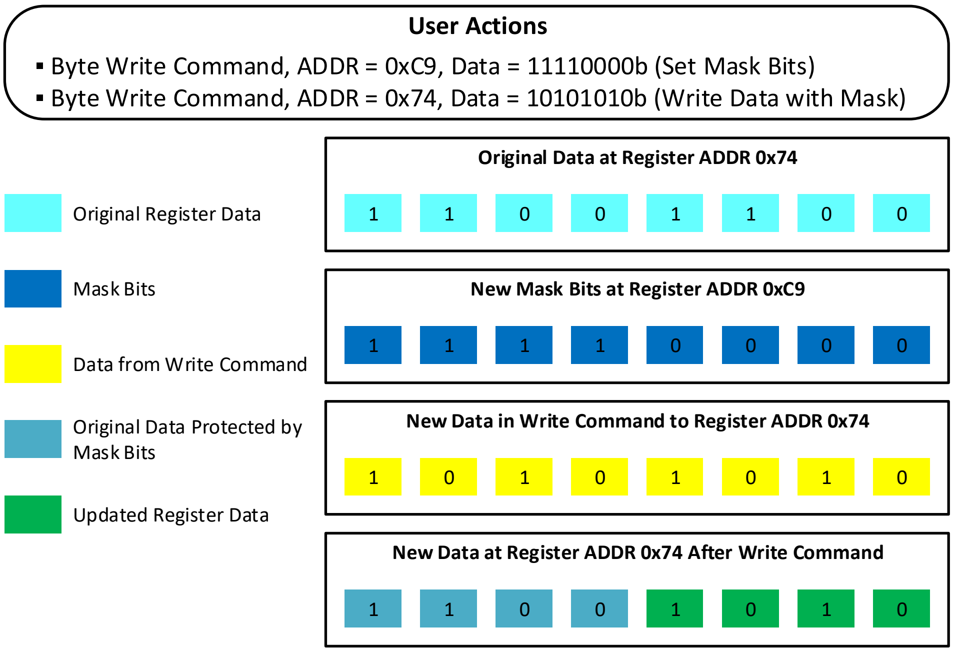


Figure 245. Example of I^2C Byte Write Bit Masking

19. Non-Volatile Memory

The SLG47004-A provides 2,048 bits of Serial Electrically Erasable Configuration Register memory that is used for device configuration.

Key features:

- Low-voltage Operation
  - for Read: VCC = 2.4 V to 5.5 V
- I²C-Compatible (2-Wire) Serial Interface
  - 100 kHz Standard Mode
  - 400 kHz Fast Mode (FM)
- Low Current Consumption
  - Read Current 0.5 mA max
  - Page Write Current 3.0 mA max
  - Chip Erase Current 3.0 mA max
  - Standby Current (1.0 µA max)
- 16-byte Page Write Mode
- Self-timed Write/Erase Cycle (20 ms max)
- Reliability
  - Endurance: 1,000 write cycles
  - Data retention: 10 years at 125 °C

19.1 Serial NVM Write Operations

Write access to the NVM is possible by setting A3, A2, A1, A0 to “0000”, which allows serial write data for a single page only. Upon receipt of the proper Control Byte and Word Address bytes, the SLG47004-A will send an ACK. The device will then be ready to receive page data, which is 16 sequential writes of 8-bit data words. The SLG47004-A will respond with an ACK after each data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition after all page data is written. At that time the device will enter an internally self-timed write cycle, which will be completed within t_{WR} (20 ms). While the data is being written into the NVM Memory Array, all inputs, outputs, internal logic, and I²C access to the Register data will be operational/valid. Please refer to Figure 247 for the SLG47004-A Memory Map.

Note 1: The 16 programmed bytes should be in the same page. Any I²C command that does not meet specific requirements will be ignored and NVM will remain unprogrammed.
Note 2: Special care must be taken when NVM page 14 is rewritten (registers [1919:1792]). This page contains rheostats tolerance data that can be permanently lost during write/erase operation.

SLG47004-A will ignore the Serial NVM Write command in case the self-programming procedure for programming rheostat value into the NVM is in progress. The SLG47004-A will respond with NACK in this case. Please refer to the Acknowledge Polling section for more details.

Data “1” cannot be re-programmed as data “0” without erasure. Each byte can only be programmed one time without erasure.

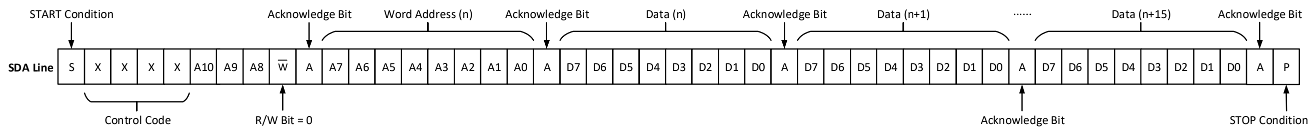


Figure 246. Page Write Command

A10 will be ignored during communication to SLG47004-A.

A9 = 1 will enable access to the NVM.

A9 = 1 and A8 = 0 corresponds to the 2K bits chip configuration NVM data.

A3, A2, A1, and A0 should be 0000 for the page write operation.

In a single page, if the data written to any byte is 0x00, the contents of the matching byte in NVM memory will not be altered.

Lowest I^2C Address = 000h

I^2C Block Address			Memory Space
A10 = 0	A9 = 0	A8 = 0	**2 kbits Register Data Configuration**
A10 = 0	A9 = 0	A8 = 1	**Not Used**
A10 = 0	A9 = 1	A8 = 0	**2 kbits NVM Data Configuration**
A10 = 0	A9 = 1	A8 = 1	**Not Used**
A10 = 1	A9 = X	A8 = X	**Not Used**

Highest I^2C Address = 7FFh

Figure 247. I^2C Block Addressing

19.2 Serial NVM Read Operations

There are three read operations:

- Current Address Read
- Random Address Read
- Sequential Read

Please refer to the Section 18. I2C Serial Communications Macrocell for more details.

19.3 Serial NVM Erase Operations

The erase scheme allows a portion or the 2K bits NVM chip configuration to be erased by modifying the contents of the Erase Registers (ERSE <2:0>). Changing the state of the ERSE is accomplished with a Byte Write sequence with the requirements outlined in this section.

The ERSE registers are located on byte 0xE3.

The ERSE format is shown in Table 68, and the ERSE bit functions are included in Table 69.

Table 68. Erase Register Bit Format

	b7	b6	b5	b4	b3	b2	b1	b0
Page Erase Register	ERSE2	ERSE1	ERSE0	ERSEB4	ERSEB3	ERSEB2	ERSEB1	ERSEB0

Table 69. Erase Register Bit Function Description

Bit	Name		Type	Description
7	ERSE2	Erase Enable	W	000: erase disable 110: cause the NVM erase
6	ERSE1		W	
5	ERSE0		W	
4	ERSEB4	Page Selection for Erase	W	Define the page address, which will be erased: ERSB4 = 0 corresponds to the Upper 2K NVM used for chip configuration;
3	ERSEB3		W	
2	ERSEB2		W	
1	ERSEB1		W	
0	ERSEB0		W	

Upon receipt of the proper Device Address and Erase Registers Address, the SLG47004-A will send an ACK. The device will then be ready to receive Erase Registers data. The SLG47004-A will respond with an ACK after Erase Registers data word is received. The addressing device, such as a bus Master, must then terminate the write operation with a Stop condition. At that time the device will enter an internally self-timed erase cycle, which will be completed within t_{ER} ms. While the data is being written into the Memory Array, all inputs, outputs, internal logic, and I^2C access to the Register data will be operational/valid.

After the erase has taken place, the contents of ERSE bits will be set to “0” automatically. The internal erase cycle will be triggered at the time the Stop Bit in the I^2C command is received.

19.4 Acknowledge Polling

An Acknowledge Polling routine can be implemented to optimize time sensitive applications that would prefer not to wait the fixed maximum write cycle time (t_{WR}) or erase maximum cycle time (t_{ER}). This method allows the application to know immediately when the NVM write/erase cycle has completed, so a subsequent operation can be started. Once the internally self-timed write/erase cycle has started, an Acknowledge Polling routine can be initiated. This involves repeatedly sending a Start condition followed by a valid Device Address byte (NVM block address) with the R/W bit set at Logic 0. The device will not respond with an ACK while the write cycle is ongoing. Once the internal write/erase cycle has completed, NVM will respond with an ACK, allowing a new read, erase, or write operation to be immediately initiated.

The same behavior will happen during the self-programming procedure when the rheostat value is written into the NVM.

The length of the self-timed write cycle (t_{WR}) and self-timed erase cycle (t_{ER}) is defined as the amount of time from the Stop condition that begins the internal write operation to the Start condition of the first Device Address byte that includes NVM address (A9 = 1; A8 = X) sent to the SLG47004-A, that it subsequently responds to with an ACK.

20. Analog Temperature Sensor

The SLG47004-A has an Analog Temperature sensor (TS) with an output voltage linearly-proportional to the Centigrade junction temperature. The TS cell shares buffer with Vref0, so it is impossible to use both cells simultaneously, its output can be connected directly to the IO0 or IO1, or the ACMP1_L positive input. Using buffer causes low-output impedance, linear output and makes interfacing to readout or control circuitry especially easy. Vref0 and Vref1 share output buffers with Temperature sensor. Note that user can use any of output buffers, but Temperature sensor is calibrated for Vref1 output buffer. The TS is rated to operate over a -40 °C to 125°C junction temperature range.The error in the whole temperature range does not exceed ±2.13 %. For more details refer to Section 3.13 Analog Temperature Sensor Specifications.

The equations below calculates the typical analog voltage at the sensor's output and the junction temperature at this voltage accordingly. It is important to note that there will be a chip to chip variation of about ±2 °C.

$$V_{TS1} = -0.0009 \times T_J^2 - 2.312 \times T_J + 898.26$$

$$T_{TS1} = \frac{10}{9} \times (\sqrt{2144770 - 900 \times V_{TS1}} - 1156)$$

$$V_{TS2} = -0.0011 \times T_J^2 - 2.7878 \times T_J + 1083.8$$

$$T_{TS2} = \frac{1}{11} \times (\sqrt{313512721 - 110000 \times V_{TS2}} - 13939)$$

where:

V_{TS1} (mV) - TS output voltage, range 1

V_{TS2} (mV) - TS output voltage, range 2

T_J (°C) - Junction Temperature

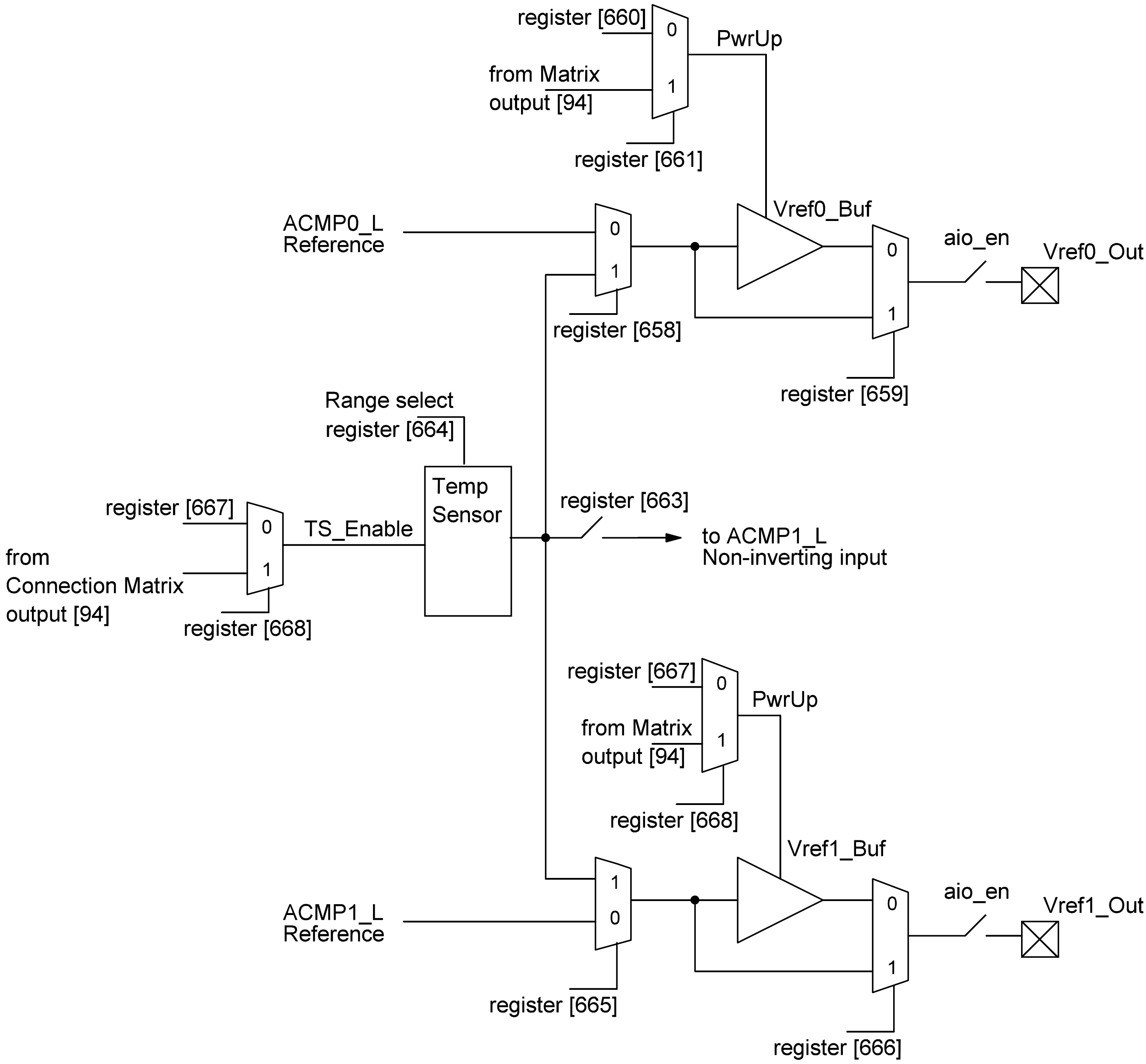


Figure 248. Analog Temperature Sensor Structure Diagram

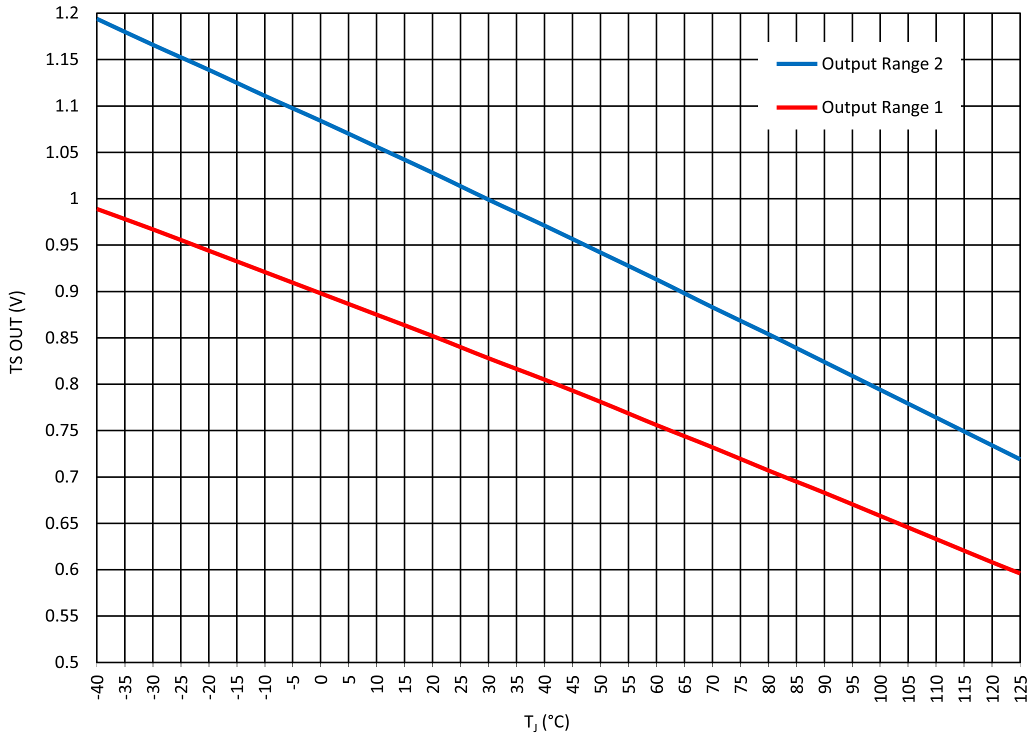


Figure 249. TS Output vs. Junction Temperature, V_{DD} = 3.3 V

21. Register Definitions

21.1 Register Map

Table 70. Register Map

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
Matrix Output				
0x00	0	LUT2_0 & DFF0	R/W	OUT0: IN0 of LUT2_0 or Clock Input of DFF0
	1			
	2			
	3			
	4			
	5			
	6		R/W	OUT1: IN1 of LUT2_0 or Data Input of DFF0
	7			
0x01	8			
	9			
	10			
	11			
	12	LUT2_1 & DFF1	R/W	OUT2: IN0 of LUT2_1 or Clock Input of DFF1
	13			
	14			
	15			
0x02	16			
	17			
	18		R/W	OUT3: IN1 of LUT2_1 or Data Input of DFF1
	19			
	20			
	21			
	22			
	23			
0x03	24	LUT2_2 & DFF2	R/W	OUT4: IN0 of LUT2_2 or Clock Input of DFF2
	25			
	26			
	27			
	28			
	29			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x03	30	LUT2_2 & DFF2	R/W	OUT5: IN1 of LUT2_2 or Data Input of DFF2
	31			
0x04	32			
	33			
	34			
	35			
	36	LUT2_3 & PGen	R/W	OUT6: IN0 of LUT2_3 or Clock Input of PGen
	37			
	38			
	39			
0x05	40			
	41			
	42		R/W	OUT7: IN1 of LUT2_3 or nRST of PGen
	43			
	44			
	45			
	46			
	47			
0x06	48	LUT3_0 & DFF3	R/W	OUT8: IN0 of LUT3_0 or CLK Input of DFF3
	49			
	50			
	51			
	52			
	53			
	54		R/W	OUT9: IN1 of LUT3_0 or Data Input of DFF3
	55			
0x07	56			
	57			
	58			
	59			
	60		R/W	OUT10: IN2 of LUT3_0 or nRST (nSET) of DFF3
	61			
	62			
	63			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x08	64	LUT3_0 & DFF3	R/W	OUT10: IN2 of LUT3_0 or nRST (nSET) of DFF3
	65			
	66	LUT3_1 & DFF4	R/W	OUT11: IN0 of LUT3_1 or CLK Input of DFF4
	67			
	68			
	69			
	70			
	71			
0x09	72		R/W	OUT12: IN1 of LUT3_1 or Data Input of DFF4
	73			
	74			
	75			
	76			
	77			
	78		R/W	OUT13: IN2 of LUT3_1 or nRST (nSET) of DFF4
	79			
0x0A	80			
	81			
	82			
	83			
	84	LUT3_2 & DFF5	R/W	OUT14: IN0 of LUT3_2 or CLK Input of DFF5
	85			
	86			
	87			
0x0B	88			
	89			
	90		R/W	OUT15: IN1 of LUT3_2 or Data Input of DFF5
	91			
	92			
	93			
	94			
	95			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x0C	96	LUT3_2 & DFF5	R/W	OUT16: IN2 of LUT3_2 or nRST (nSET) of DFF5
	97			
	98			
	99			
	100			
	101			
	102	LUT3_3 & DFF6	R/W	OUT17: IN0 of LUT3_3 or CLK Input of DFF6
	103			
0x0D	104			
	105			
	106			
	107			
	108		R/W	OUT18: IN1 of LUT3_3 or Data Input of DFF6
	109			
	110			
	111			
0x0E	112			
	113			
	114		R/W	OUT19: IN2 of LUT3_3 or nRST (nSET) of DFF6
	115			
	116			
	117			
	118			
	119			
0x0F	120	LUT3_4 & DFF7	R/W	OUT20: IN0 of LUT3_4 or CLK Input of DFF7
	121			
	122			
	123			
	124			
	125			
	126		R/W	OUT21: IN1 of LUT3_4 or Data Input of DFF7
	127			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x10	128	LUT3_4 & DFF7	R/W	OUT21: IN1 of LUT3_4 or Data Input of DFF7
	129			
	130			
	131			
	132		R/W	OUT22: IN2 of LUT3_4 or nRST (nSET) of DFF7
	133			
	134			
	135			
0x11	136			
	137			
	138	LUT3_5 & DFF8	R/W	OUT23: IN0 of LUT3_5 or CLK Input of DFF8
	139			
	140			
	141			
	142			
	143			
0x12	144		R/W	OUT24: IN1 of LUT3_5 or Data Input of DFF8
	145			
	146			
	147			
	148			
	149			
	150		R/W	OUT25: IN2 of LUT3_5 or nRST (nSET) of DFF8
	151			
0x13	152			
	153			
	154			
	155			
	156	LUT3_6 & DFF9	R/W	OUT26: IN0 of LUT3_6 or CLK Input of DFF9
	157			
	158			
	159			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x14	160	LUT3_6 & DFF9	R/W	OUT26: IN0 of LUT3_6 or CLK Input of DFF9
	161			
	162		R/W	OUT27: IN1 of LUT3_6 or Data Input of DFF9
	163			
	164			
	165			
	166			
	167			
0x15	168		R/W	OUT28: IN2 of LUT3_6 or nRST (nSET) of DFF9
	169			
	170			
	171			
	172			
	173			
	174	Multi_function1	R/W	OUT29: IN0 of LUT3_7 or CLK Input of DFF11 Delay1 Input (or Counter1 nRST Input)
	175			
0x16	176			
	177			
	178			
	179			
	180		R/W	OUT30: IN1 of LUT3_7 or nRST (nSET) of DFF11 Delay1 Input (or Counter1 nRST Input)
	181			
	182			
	183			
0x17	184			
	185			
	186		R/W	OUT31: IN2 of LUT3_7 or Data of DFF11 Delay1 Input (or Counter1 nRST Input)
	187			
	188			
	189			
	190			
	191			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x18	192	Multi_function2	R/W	OUT32: IN0 of LUT3_8 or CLK Input of DFF12 Delay2 Input (or Counter2 nRST Input)
	193			
	194			
	195			
	196			
	197			
	198		R/W	OUT33: IN1 of LUT3_8 or nRST (nSET) of DFF12 Delay2 Input (or Counter2 nRST Input)
	199			
0x19	200			
	201			
	202			
	203			
	204		R/W	OUT34: IN2 of LUT3_8 or Data of DFF12 Delay2 Input (or Counter2 nRST Input)
	205			
	206			
	207			
0x1A	208			
	209			
	210	Multi_function3	R/W	OUT35: IN0 of LUT3_9 or CLK Input of DFF13 Delay3 Input (or Counter3 nRST Input)
	211			
	212			
	213			
	214			
	215			
0x1B	216	Multi_function3	R/W	OUT36: IN1 of LUT3_9 or nRST (nSET) of DFF13 Delay3 Input (or Counter3 nRST Input)
	217			
	218			
	219			
	220			
	221			
	222		R/W	OUT37: IN2 of LUT3_9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)
	223			

Table 70. Register Map (Cont.)

Address Byte	Register Bit	Signal Function	Access Type	Register Bit Definition
0x1C	224	Multi_function3	R/W	OUT37: IN2 of LUT3_9 or Data of DFF13 Delay3 Input (or Counter3 nRST Input)
	225			
	226			
	227			
	228	Multi_function4	R/W	OUT38: IN0 of LUT3_10 or CLK Input of DFF14 Delay4 Input (or Counter4 nRST Input)
	229			
	230			
	231			
0x1D	232			
	233			
	234		R/W	OUT39: IN1 of LUT3_10 or nRST (nSET) of DFF14 Delay4 Input (or Counter4 nRST Input)
	235			
	236			
	237			
	238			
	239			
0x1E	240		R/W	OUT40: IN2 of LUT3_10 or Data of DFF14 Delay4 Input (or Counter4 nRST Input)
	241			
	242			
	243			
	244			
	245			
	246	Multi_function5	R/W	OUT41: IN0 of LUT3_11 or CLK Input of DFF15 Delay5 Input (or Counter5 nRST Input)
	247			
0x1F	248			
	249			
	250			
	251			
	252		R/W	OUT42: IN1 of LUT3_11 or nRST (nSET) of DFF15 Delay5 Input (or Counter5 nRST Input)
	253			
	254			
	255			
0x20	256			
	257			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x20	258	Multi_function5	R/W	OUT43: IN2 of LUT3_11 or Data of DFF15 Delay5 Input (or Counter5 nRST Input)
	259			
	260			
	261			
	262			
	263			
0x21	264	Multi_function6	R/W	OUT44: IN0 of LUT3_12 or CLK Input of DFF16 Delay6 Input (or Counter6 nRST Input)
	265			
	266			
	267			
	268			
	269			
	270		R/W	OUT45: IN1 of LUT3_12 or nRST (nSET) of DFF16 Delay6 Input (or Counter6 nRST Input)
	271			
0x22	272			
	273			
	274			
	275			
	276		R/W	OUT46: IN2 of LUT3_12 or Data of DFF16 Delay6 Input (or Counter6 nRST Input)
	277			
	278			
	279			
0x23	280			
	281			
	282	LUT3_13 & Pipe Delay (RIPP CNT)	R/W	OUT47: IN0 of LUT3_13 or Input of Pipe Delay or UP signal of RIPP CNT
	283			
	284			
	285			
	286			
	287			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x24	288	LUT3_13 & Pipe Delay (RIPP CNT)	R/W	OUT48: IN1 of LUT3_13 or nRST of Pipe Delay or nSET of RIPP CNT
	289			
	290			
	291			
	292			
	293			
	294		R/W	OUT49: IN2 of LUT3_13 or Clock of Pipe Delay_RIPP CNT
	295			
0x25	296			
	297			
	298			
	299			
	300	LUT4_DFF10	R/W	OUT50: IN0 of LUT4_0 or CLK Input of DFF10
	301			
	302			
	303			
0x26	304			
	305			
	306		R/W	OUT51: IN1 of LUT4_0 or Data of DFF10
	307			
	308			
	309			
	310			
	311			
0x27	312		R/W	OUT52: IN2 of LUT4_0 or nRST (nSET) of DFF10
	313			
	314			
	315			
	316			
	317			
	318		R/W	OUT53: IN3 of LUT4_0
	319			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x28	320	LUT4_DFF10	R/W	OUT53: IN3 of LUT4_0
	321			
	322			
	323			
	324	Multi_function0	R/W	OUT54: IN0 of LUT4_1 or CLK Input of DFF17 Delay0 Input (or Counter0 nRST Input)
	325			
	326			
	327			
0x29	328			
	329			
	330		R/W	OUT55: IN1 of LUT4_1 or nRST of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source
	331			
	332			
	333			
	334			
	335			
0x2A	336		R/W	OUT56: IN2 of LUT4_1 or nSET of DFF17 Delay0 Input (or Counter0 nRST Input) Delay/Counter0 External CLK source KEEP Input of FSM0
	337			
	338			
	339			
	340			
	341			
	342		R/W	OUT57: IN3 of LUT4_1 or Data of DFF17 Delay0 Input (or Counter0 nRST Input) UP Input of FSM
	343			
0x2B	344			
	345			
	346			
	347			
	348	Programmable delay	R/W	OUT58: Programmable delay/edge detect input
	349			
	350			
	351			
0x2C	352			
	353			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x2C	354	Filter/Edge detector	R/W	OUT59: Filter/Edge detect input
	355			
	356			
	357			
	358			
	359			
0x2D	360	IO0	R/W	OUT60: IO0 DOUT
	361			
	362			
	363			
	364			
	365			
	366		R/W	OUT61: IO0 DOUT OE
	367			
0x2E	368			
	369			
	370			
	371			
	372	IO1	R/W	OUT62: IO1 DOUT
	373			
	374			
	375			
0x2F	376			
	377			
	378		R/W	OUT63: IO1 DOUT OE
	379			
	380			
	381			
	382			
	383			
0x30	384	IO2	R/W	OUT64: IO2 DOUT
	385			
	386			
	387			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x30	388	IO2	R/W	OUT64: IO2 DOUT
	389			
	390		R/W	OUT65: IO2 DOUT OE
	391			
0x31	392			
	393			
	394			
	395			
	396	IO3	R/W	OUT66: IO3 DOUT
	397			
	398			
	399			
0x32	400			
	401			
	402		R/W	OUT67: IO3 DOUT OE
	403			
	404			
	405			
	406			
	407			
0x33	408	IO4	R/W	OUT68: IO4 DOUT
	409			
	410			
	411			
	412			
	413			
	414		R/W	OUT69: IO4 DOUT OE
	415			
0x34	416			
	417			
	418			
	419			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x34	420	IO5	R/W	OUT70: IO5 DOUT
	421			
	422			
	423			
0x35	424			
	425			
	426		R/W	OUT71: IO5 DOUT OE
	427			
	428			
	429			
	430			
	431			
0x36	432	IO6	R/W	OUT72: IO6 DOUT
	433			
	434			
	435			
	436			
	437			
	438		R/W	OUT73: IO6 DOUT OE
	439			
0x37	440			
	441			
	442			
	443			
	444	Programmable Trim Block0	R/W	OUT74: set0 of Auto Calibration
	445			
	446			
	447			
0x38	448			
	449			
	450		R/W	OUT75: clock0 of Auto Calibration
	451			
	452			
	453			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x38	454	Programmable Trim Block0	R/W	OUT75: clock0 of Auto Calibration
	455			
0x39	456		R/W	OUT76: reload0 of Auto Calibration
	457			
	458			
	459			
	460			
	461			
	462		R/W	OUT77: Reserved
	463			
0x3A	464			
	465			
	466			
	467			
	468	Digital Rheostat	R/W	OUT78: Rheostat Counter0 up/down 0: down, 1: up. (register [920] = 0) 0: up, 1: down. (register [920] = 1)
	469			
	470			
	471			
0x3B	472			
	473			
	474	Programmable Trim Block1	R/W	OUT79: set1 of Auto Calibration
	475			
	476			
	477			
	478			
	479			
0x3C	480		R/W	OUT80: clock1 of Auto Calibration
	481			
	482			
	483			
	484			
	485			
	486		R/W	OUT81: reload1 of Auto Calibration
	487			

Table 70. Register Map (Cont.)

<table>
<tr><th colspan="2">Address</th><th rowspan="2">Signal Function</th><th rowspan="2">Access Type</th><th rowspan="2">Register Bit Definition</th></tr>
<tr><th>Byte</th><th>Register Bit</th></tr>
<tr><td rowspan="8">0x3D</td><td>488</td><td rowspan="10">Programmable Trim Block1</td><td rowspan="4">R/W</td><td rowspan="4">OUT81:
reload1 of Auto Calibration</td></tr>
<tr><td>489</td></tr>
<tr><td>490</td></tr>
<tr><td>491</td></tr>
<tr><td>492</td><td rowspan="6">R/W</td><td rowspan="6">OUT82:
Reserved</td></tr>
<tr><td>493</td></tr>
<tr><td>494</td></tr>
<tr><td>495</td></tr>
<tr><td rowspan="8">0x3E</td><td>496</td></tr>
<tr><td>497</td></tr>
<tr><td>498</td><td rowspan="6">Digital Rheostat</td><td rowspan="6">R/W</td><td rowspan="6">OUT83:
Rheostat Counter1 up/down
0: down, 1: up. (register [923] = 0)
0: up, 1: down. (register [923] = 1)</td></tr>
<tr><td>499</td></tr>
<tr><td>500</td></tr>
<tr><td>501</td></tr>
<tr><td>502</td></tr>
<tr><td>503</td></tr>
<tr><td rowspan="8">0x3F</td><td>504</td><td rowspan="6">FIFO Reset of PT blocks</td><td rowspan="6">R/W</td><td rowspan="6">OUT84:
FIFO nRST of the control logic of reload0/re-load1/auto program0/auto program1</td></tr>
<tr><td>505</td></tr>
<tr><td>506</td></tr>
<tr><td>507</td></tr>
<tr><td>508</td></tr>
<tr><td>509</td></tr>
<tr><td>510</td><td rowspan="6">Chopper ACMP</td><td rowspan="6">R/W</td><td rowspan="6">OUT85:
Chopper ACMP Power Up</td></tr>
<tr><td>511</td></tr>
<tr><td rowspan="8">0x40</td><td>512</td></tr>
<tr><td>513</td></tr>
<tr><td>514</td></tr>
<tr><td>515</td></tr>
<tr><td>516</td><td rowspan="4">Digital Rheostat</td><td rowspan="4">R/W</td><td rowspan="4">OUT86:
Rheostat Charge pump enable</td></tr>
<tr><td>517</td></tr>
<tr><td>518</td></tr>
<tr><td>519</td></tr>
</table>

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x41	520	Digital Rheostat	R/W	OUT86: Rheostat Charge pump enable
	521			
	522	Analog Switch0	R/W	OUT87: ASW0 enable/Half bridge enable
	523			
	524			
	525			
	526			
	527			
0x42	528	Analog Switch1	R/W	OUT88: ASW1 enable/Half bridge data
	529			
	530			
	531			
	532			
	533			
	534	ACMP0	R/W	OUT89: ACMP0 Power Up
	535			
0x43	536			
	537			
	538			
	539			
	540	ACMP1	R/W	OUT90: ACMP1 Power Up
	541			
	542			
	543			
0x44	544			
	545			
	546	OSC0	R/W	OUT91: OSC0 ENABLE
	547			
	548			
	549			
	550			
	551			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x45	552	OSC1	R/W	OUT92: OSC1 ENABLE
	553			
	554			
	555			
	556			
	557			
	558	OSC2	R/W	OUT93: OSC2 ENABLE
	559			
0x46	560			
	561			
	562			
	563			
	564	Temperature Sensor	R/W	OUT94: VREFO TEMPSEN/VREFO Power Up
	565			
	566			
	567			
0x47	568			
	569			
	570	HDBUF	R/W	OUT95: HDBUF ENABLE
	571			
	572			
	573			
	574			
	575			
0x48	576	Op Amp0	R/W	OUT96: OP0(Op Amp ACMP0) Power Up
	577			
	578			
	579			
	580			
	581			
	582	Op Amp1	R/W	OUT97: OP1(Op Amp ACMP1) Power Up
	583			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x49	584	Op Amp1	R/W	OUT97: OP1(Op Amp ACMP1) Power Up
	585			
	586			
	587			
	588	Op Amp2	R/W	OUT98: OP2 Power Up (In Amp Mode)
	589			
	590			
	591			
0x4A	592			
	593			
	594	Op amps	R/W	OUT99: OP VREF ENABLE
	595			
	596			
	597			
	598			
	599			
0x4B	600	Reserved	R/W	
	601	Reserved	R/W	
	602	Reserved	R/W	
	603	Reserved	R/W	
	604	Reserved	R/W	
	605	Reserved	R/W	
	606	Reserved	R/W	
	607	Reserved	R/W	
ACMP0				
0x4C	608	ACMP Low Energy Power Up enable (ACMP power after bg_ok)	R/W	1: enable
	609	ACMP input path LPF enable	R/W	1: enable
	610	ACMP sampling mode enable	R/W	1: enable
	611	ACMP short time wake sleep mode disable	R/W	0: short time wake sleep enable 1: short time wake sleep disable
	612	ACMP wake sleep function enable	R/W	1: enable
	613	ACMP Vref path LPF enable (when ACMP hysteresis > 196 mV)	R/W	1: enable
0x4C	614	ACMP input divider selection	R/W	00: 1 01: 0.5 10: 1/3 11: 1/4
	615			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x4D	616	ACMP input mux selection	R/W	00: OP0 output 01: from Pin 10: tie VDD
	617			
	618	ACMP Low to High Vref selection	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	619			
	620			
	621			
	622			
	623			
0x4E	624	ACMP High to Low Vref selection	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	625			
	626			
	627			
	628			
	629			
ACMP1				
0x4E	630	ACMP Low Energy Power Up enable (ACMP power after bg_ok)	R/W	1: enable
	631	ACMP input path LPF enable	R/W	1: enable
0x4F	632	ACMP sampling mode enable	R/W	1: enable
	633	ACMP short time wake sleep mode disable	R/W	0: short time wake sleep enable 1: short time wake sleep disable
	634	ACMP wake sleep function enable	R/W	1: enable
	635	ACMP Vref path LPF enable (when ACMP hysteresis > 196 mV)	R/W	1: enable
	636	ACMP input divider selection	R/W	00: 1 01: 0.5 10: 1/3 11: 1/4
	637			
	638	ACMP input mux selection	R/W	00: OP1 output 01: from Pin 10: ACMP0 input mux output 11: VrefO1 Temp sensor output
	639			

Table 70. Register Map (Cont.)

Address Byte	Register Bit	Signal Function	Access Type	Register Bit Definition
0x50	640	ACMP Low to High Vref selection	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	641			
	642			
	643			
	644			
	645			
	646	ACMP High to Low Vref selection	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	647			
0x51	648			
	649			
	650			
	651			
Vref				
0x51	652	Reserved	R/W	
	653	Reserved	R/W	
	654	Reserved	R/W	
	655	Reserved	R/W	
0x52	656	Reserved	R/W	
	657	Reserved	R/W	
	658	VREFO0 input source selection	R/W	0: ACMP0 VREF 1: Temp Sensor
	659	VREFO0 output buffer enable	R/W	1: enable
	660	VREFO0 register Power Up	R/W	VREFO0 register power on signal
	661	VREFO0 Power Up selection	R/W	0: Power Up from reg 1: from matrix
	662	Reserved	R/W	no use
	663	VREFO1's temp sensor to ACMP1 input path enable	R/W	Temp Sensor output to ACMP1 enable 1: enable
0x53	664	VREFO1's temp sensor range selection	R/W	0:1V; 1:1.2V
	665	VREFO1 input source selection	R/W	0: ACMP1 Vref 1: TS
	666	VREFO1 output buffer enable	R/W	1: enable
	667	VREFO1 register Power Up	R/W	VrefO1 register power on signal
	668	VREFO1 Power Up selection	R/W	0: Power Up from reg 1: from matrix
	669	ACMP Vrefs source selection	R/W	ACMP Vref gen source selection (0: VBG, 1: V_{DD})

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x53	670	ACMP0 external Vref enable	R/W	1:enable
	671	ACMP1 external Vref enable	R/W	1:enable
0x54	672	Reserved	R/W	
0x54	673	Reserved	R/W	
	674	Reserved	R/W	
	675	Reserved	R/W	
	676		R/W	
	677		R/W	
	678	Reserved	R/W	
	679	Reserved	R/W	
0x55	680	Reserved	R/W	
	681	Reserved	R/W	
	682	Reserved	R/W	
	683	Reserved	R/W	
	684	Reserved	R/W	
	685	Reserved	R/W	
	686	Reserved	R/W	
	687	Reserved	R/W	
OSC1				
0x56	688	OSC1 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	689	OSC1 matrix power down or on select	R/W	0: matrix down 1: matrix on
	690	OSC1 external clock source enable	R/W	0: internal OSC1 1: external clock from Pin15
	691 692	OSC1 post divider ratio control	R/W	00: div 1 01: div 2 10: div 4 11: div8
	693 694 695	OSC1 matrix divider ratio control	R/W	000: /1 001:/2 010:/4 011: /3 100: /8 101: /12 110: /24 111: /64

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x57	696	OSC1 matrix out enable	R/W	0: disable 1: enable
	697	Reserved	R/W	
	698	Reserved	R/W	
	699	Reserved	R/W	
	700	OSC1 2nd output to matrix enable	R/W	0: disable 1: enable
	701	OSC1 2nd matrix divider ratio control	R/W	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	702			
	703			
OSC2				
0x58	704	OSC2 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	705	OSC2 matrix power down or on select	R/W	0: matrix down 1: matrix on
	706	OSC2 external clock source enable	R/W	0: internal OSC2 1: external clock from IO2
	707	OSC2 matrix out enable	R/W	0: disable 1: enable
	708	OSC2 post divider ratio control	R/W	00: div 1 01: div 2 10: div 4 11: div8
	709			
	710	OSC2 matrix divider ratio control	R/W	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	711			
0x59	712			
	713	OSC2 startup delay with 100ns	R/W	0: enable 1: disable
	714	Reserved	R/W	
	715	Reserved	R/W	
	716	Reserved	R/W	
	717	Op Amp0 sr boost for OP 8 MHz	R/W	0: enable, 1: disable
	718	Op Amp1 sr boost for OP 8 MHz	R/W	0: enable, 1: disable
	719	Op Amp2 sr boost for OP 8 MHz	R/W	0: enable, 1: disable

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
OSC0				
0x5A	720	OSC0 turn on by register	R/W	when matrix output enable/pd control signal = 0: 0: auto on by delay cells 1: always on
	721	OSC0 matrix power down or on select	R/W	0: matrix down 1: matrix on
	722	OSC0 external clock source enable	R/W	0: internal OSC0 1: external clock from IO0
	723	OSC0 matrix out enable	R/W	0: disable 1: enable
	724	OSC0 post divider ratio control	R/W	00: div 1 01: div 2 10: div 4 11: div8
	725			
	726	OSC0 matrix divider ratio control	R/W	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	727			
0x5B	728			
	729	enable OSC0 output gating by wake_sleep signal (note: the wake_sleep clock is separated path, so it is not gated)	R/W	0: no gating 1: enable
	730	OSC0 2nd output to matrix enable	R/W	0: disable 1: enable
	731	OSC0 2nd matrix divider ratio control	R/W	000: /1 001: /2 010: /4 011: /3 100: /8 101: /12 110: /24 111: /64
	732			
	733			
	734	Reserved	R/W	
	735	Reserved	R/W	
Analog Switch				
0x5C	736	ASW0 small NMOS enable selection	R/W	0: small NMOS disable 1: small NMOS enable by matrix87
	737	ASW1 small PMOS enable selection	R/W	0: small PMOS disable 1: small PMOS enable by matrix88
	738	ASW0 big PMOS control selection	R/W	0: control by matrix87 1:control by Op Amp0
	739	ASW1 big NMOS control selection	R/W	0: control by matrix88 1:control by Op Amp1
	740	ASW half bridge mode enable	R/W	0: analog switch mode 1: half bridge (enable from matrix87; data from matrix88)

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x5C	741	ASW half bridge dead time select	R/W	00: bypass 01: 20ns 10: 100ns 11: 500ns
	742			
	743	Reserved	R/W	
Op Amp0/1/2				
0x5D	744	Op Amp0 bandwidth selection	R/W	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	745			
	746	Op Amp1 bandwidth selection	R/W	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	747			
	748	Op Amp2 bandwidth selection	R/W	00: 128 kHz 01: 512 kHz 10: 2 MHz 11: 8 MHz
	749			
	750	ACMP/Op Amp0 mode	R/W	0: Op amp mode 1: ACMP mode
	751	ACMP/Op Amp1 mode	R/W	0: Op amp mode 1: ACMP mode
0x5E	752	Op Amp0 charge pump disable	R/W	0: Op amp input common voltage higher than V_{DD}-1.5 V, enable CP 1: Op amp input common voltage lower than V_{DD}-1.5 V, disable CP
	753	Op Amp1 charge pump disable	R/W	0: Op amp input common voltage higher than V_{DD}-1.5 V, enable CP; 1: Op amp input common voltage lower than V_{DD}-1.5 V, disable CP
	754	Op Amp2 charge pump disable	R/W	0: Op amp input common voltage higher than V_{DD}-1.5 V, enable CP 1: Op amp input common voltage lower than V_{DD}-1.5 V, disable CP
	755	Path between Op Amp0/1 and Op Amp2	R/W	0: path on (for normal function) 1: path off (for trim function)
	756	Op Amp2's Vref buffer bypass control	R/W	0: without buffer 1: with buffer
	757	Supporting blocks for Op Amp0 on/off	R/W	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5 V
	758	Supporting blocks for Op Amp1 on/off	R/W	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5V
	759	Supporting blocks for Op Amp2 on/off	R/W	0: on/off follows op amp 1: always on except input common voltage of op amp lower than V_{DD}-1.5V

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x5F	760	Op amp ACMP Vref0 output selection[0]	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	761	Op amp ACMP Vref0 output selection[1]		
	762	Op amp ACMP Vref0 output selection[2]		
	763	Op amp ACMP Vref0 output selection[3]		
	764	Op amp ACMP Vref0 output selection[4]		
	765	Op amp ACMP Vref0 output selection[5]		
	766	Op amp ACMP Vref0 register enable (select by register [782])	R/W	0: dynamic on/off 1: Vref enable
	767	Vref0 to op amp/ACMP input enable	R/W	0:disable; 1: enable
0x60	768	Op amp ACMP Vref1 output selection[0]	R/W	000000-111111: 32 mV ~2.048 V/step = 32 mV
	769	Op amp ACMP Vref1 output selection[1]		
	770	Op amp ACMP Vref1 output selection[2]		
	771	Op amp ACMP Vref1 output selection[3]		
	772	Op amp ACMP Vref1 output selection[4]		
	773	Op amp ACMP Vref1 output selection[5]		
	774	Op amp ACMP Vref1 register enable (select by register [783])	R/W	0: dynamic on/off 1: Vref enable
	775	Vref1 to op amp/ACMP input enable	R/W	0:disable; 1: enable
0x61	776	Op amp ACMP Vref0 output selection	R/W	0: Vref to ACMP negative input 1: Vref to ACMP positive input
	777	Op amp ACMP Vref1 output selection	R/W	0: Vref to ACMP negative input 1: Vref to ACMP positive input
	778	Reserved	R/W	
	779	Reserved	R/W	
	780	Op amp ACMP Vref0 input voltage selection	R/W	0: 2.048 V 1: V_{DD}
	781	Op amp ACMP Vref1 input voltage selection	R/W	0: 2.048 V 1: V_{DD}
	782	Op amp ACMP vref0 enable selection	R/W	0: from register [766] 1: from matrix99
	783	Op amp ACMP vref1 enable selection	R/W	0: from register [774] 1: from matrix99
LUT3_2/DFF5				
0x62	784	LUT3_2_DFF5 setting	R/W	<2:0>: LUT3_2 <2:0>
	785			
	786			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x62	787	LUT3_2_DFF5 setting	R/W	<3>:LUT3_2 <3>/DFF5 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	788			<4>:LUT3_2<4>/DFF5 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	789			<5>:LUT3_2 <5>/DFF5 Initial Polarity Select 0: Low, 1: High
	790			<6>:LUT3_2 <6>/DFF5 Output Select 0: Q output, 1: QB output
	791			<7>:LUT3_2 <7>/DFF5 or Latch Select 0: DFF function, 1: Latch function
LUT3_3/DFF6				
0x63	792	LUT3_3_DFF6 setting	R/W	<2:0>: LUT3_3 <2:0>
	793			
	794			
	795		R/W	<3>:LUT3_3 <3>/DFF6 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	796		R/W	<4>:LUT3_3<4>/DFF6 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	797		R/W	<5>:LUT3_3 <5>/DFF6 Initial Polarity Select 0: Low, 1: High
	798		R/W	<6>:LUT3_3 <6>/DFF6 Output Select 0: Q output, 1: QB output
	799		R/W	<7>:LUT3_3 <7>/DFF6 or Latch Select 0: DFF function, 1: Latch function
LUT3_4/DFF7				
0x64	800	LUT3_4_DFF7 setting	R/W	<2:0>: LUT3_4 <2:0>
	801			
	802			
	803		R/W	<3>:LUT3_4 <3>/DFF7 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	804		R/W	<4>:LUT3_4<4>/DFF7 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	805		R/W	<5>:LUT3_4 <5>/DFF7 Initial Polarity Select 0: Low, 1: High
	806		R/W	<6>:LUT3_4 <6>/DFF7 Output Select 0: Q output, 1: QB output
0x64	807	LUT3_4_DFF7 setting	R/W	<7>:LUT3_4 <7>/DFF7 or Latch Select 0: DFF function, 1: Latch function

Table 70. Register Map (Cont.)

Address: Byte	Address: Register Bit	Signal Function	Access Type	Register Bit Definition
LUT3_5/DFF8				
0x65	808	LUT3_5_DFF8 setting	R/W	<2:0>: LUT3_5 <2:0>
	809			
	810			
	811		R/W	<3>:LUT3_5 <3>/DFF8 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	812		R/W	<4>:LUT3_5<4>/DFF8 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	813		R/W	<5>:LUT3_5 <5>/DFF8 Initial Polarity Select 0: Low, 1: High
	814		R/W	<6>:LUT3_5 <6>/DFF8 Output Select 0: Q output, 1: QB output
	815		R/W	<7>:LUT3_5 <7>/DFF8 or Latch Select 0: DFF function, 1: Latch function
LUT3_6/DFF9				
0x66	816	LUT3_6_DFF9 setting	R/W	<2:0>: LUT3_6 <2:0>
	817			
	818			
	819		R/W	<3>:LUT3_6 <3>/DFF9 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	820		R/W	<4>:LUT3_6<4>/DFF9 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	821		R/W	<5>:LUT3_6 <5>/DFF9 Initial Polarity Select 0: Low, 1: High
	822		R/W	<6>:LUT3_6 <6>/DFF9 Output Select 0: Q output, 1: QB output
	823		R/W	<7>:LUT3_6 <7>/DFF9 or Latch Select 0: DFF function, 1: Latch function
0x67	824	LUT3_2 or DFF5 Select	R/W	0: LUT3_2 1: DFF5
	825	LUT3_3 or DFF6 Select	R/W	0: LUT3_3 1: DFF6
	826	LUT3_4 or DFF7 Select	R/W	0: LUT3_4 1: DFF7
	827	LUT3_5 or DFF8 Select	R/W	0: LUT3_5 1: DFF8

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x67	828	LUT3_6 or DFF9 Select	R/W	0: LUT3_5 1: DFF8
	829	LUT4_0 or DFF10 Select	R/W	0: LUT4_0 1: DFF10
	830	Reserved	R/W	
	831	Reserved	R/W	
LUT4_0/DFF10				
0x68	832	LUT4_0_DFF10 setting	R/W	<9:0>: LUT4_0 <9:0>
	833			
	834			
	835			
	836			
	837			
	838			
	839			
0x69	840			
	841			
	842		R/W	<10>:LUT4_0 <10>/DFF10 stage selection 0: Q of first DFF; 1 Q of second DFF
	843		R/W	<11>:LUT4_0 <11>/DFF10 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	844		R/W	<12>:LUT4_0 <12>/DFF10 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	845		R/W	<13>:LUT4_0 <13> /DFF10 Initial Polarity Select 0: Low, 1: High
	846		R/W	<14>:LUT4_0 <14>/DFF10 Output Select 0: Q output, 1: QB output
	847		R/W	<15>:LUT4_0 <15>/DFF10 or Latch Select 0: DFF function, 1: Latch function
LUT3_13/Pipe Delay (RIPP CNT)				
0x6A	848	LUT value or pipe delay out sel or nSET/END value	R/W	at LUT/pipe delay mode bit<7:4>: LUT3_13 <7:4> / REG_S1<3:0> pipe delay out1 sel bit<3:0>: LUT3_13 <3:0> / REG_S0<3:0> pipe delay out0 sel at RIPP CNT mode bit<2:0> is the nSET value. bit<5:3> is the END value bit<6> is the range control: 0: full cycle, 1: range cycle bit<7> No used
	849			
	850			
	851			
	852			
	853			
	854			
	855			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x6B	856	Active level selection for RST/SET	R/W	0: Active low level reset/set 1: Active high level reset/set
	857	Out of LUT3_13 or Out0 of Pipe Delay/RIPP CNT Select	R/W	0: LUT3_13 1: OUT0 of Pipe Delay or RIPP CNT
	858	PIPE_RIPP_CNT_S	R/W	0: Pipe delay mode selection 1: Ripple Counter mode selection
	859	Pipe Delay OUT1 Polarity Select	R/W	0: Non-inverted 1: Inverted
	860	Reserved	R/W	
	861	Reserved	R/W	
	862	Reserved	R/W	
	863	Reserved	R/W	
Programmable Delay				
0x6C	864 865	Delay Value Select for Programmable Delay & Edge Detector	R/W	00: 125ns 01: 250ns 10: 375ns 11: 500ns
	866 867	Select the Edge Mode of Programmable Delay & Edge Detector	R/W	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Filter/Edge Detector				
0x6C	868	Filter or Edge Detector selection	R/W	0: filter 1: edge detect
	869	Output Polarity Select	R/W	0: output non-invert 1: output invert
	870 871	Select the edge mode	R/W	00: Rising Edge Detect 01: Falling Edge Detect 10: Both Edge Detect 11: Both Edge DLY
Chopper ACMP				
0x6D	872 873	Chopper ACMP positive input selection for calibration channel0	R/W	00: from In Amp out 01: from Op Amp0 out 10: from Op Amp1 out 11: IO1
	874 875	Chopper ACMP positive input selection for calibration channel1	R/W	00: from In Amp out 01: from Op Amp0 out 10: from Op Amp1 out 11: IO1
	876	Reserved	R/W	
	877	Reserved	R/W	
	878	Reserved	R/W	
	879	Reserved	R/W	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x6E	880	Reserved	R/W	
	881	Reserved	R/W	
	882	Output Polarity Select	R/W	0: output non-invert 1: output invert
	883	Reserved	R/W	
	884		R/W	
	885		R/W	
	886		R/W	
	887		R/W	
0x6F	888	Reserved	R/W	
	889		R/W	
	890	Reserved	R/W	
	891	Reserved	R/W	
Calibration				
0x6F	892	auto calibration channel selection by register	R/W	0: calibration channel0 1: calibration channel1
	893	auto calibration channel selection source selection	R/W	0:calibration channel auto selection 1: from register [892]
	894	RH_CNT1 clock source selection	R/W	0: From Chopper ACMP (Chopper ACMP changes one time per rheostat clock) 1: from matrix directly
	895	RH_CNT0 clock source selection	R/W	0: From Chopper ACMP (Chopper ACMP changes one time per rheostat clock) 1: from matrix directly
0x70	896	Calibration0 clock divider	R/W	0000: Reserved 0001: Reserved 0010: OSC1/64 0011: OSC1/512 0100: OSC0 0101:OSC0/8 0110: OSC0/64 0111: OSC0/512 1000: OSC0/4096 1001: OSC0/32768 1010: OSC0/262144 1011/1100/1101/1110: GND 1111: EXTCLK
	897			
	898			
	899			
	900	Up/down selection	R/W	0: chopper ACMP 1: matrix83
	901	auto_calibration disable	R/W	0: auto calibration enable 1: disable
	902	Reserved	R/W	
	903	Reserved	R/W	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x71	904	Calibration1 clock divider	R/W	0000: Reserved 0001: Reserved 0010: OSC1/64 0011: OSC1/512 0100: OSC0 0101: OSC0/8 0110: OSC0/64 0111: OSC0/512 1000: OSC0/4096 1001: OSC0/32768 1010: OSC0/262144 1011/1100/1101/1110: GND 1111: EXTCLK
	905			
	906			
	907			
	908	Up/down selection	R/W	0: chopper ACMP 1: matrix83
	909	auto_calibration disable	R/W	0: auto calibration enable 1: disable
	910	Reserved	R/W	
	911	Reserved	R/W	
Digital Rheostats				
0x72	912	POTCP0 turn on by register	R/W	0: control by matrix86 1: on
	913	POTCP1 turn on by register	R/W	0: control by matrix86 1: on
	914	POTCP0/1 clock source selection	R/W	0: from LPBG chopper OSC 1: from OSC1
	915	POTCP0/1 clock source select from register	R/W	0: by register [914] 1: calibration auto on
	916	Reserved	R/W	
	917	Reserved	R/W	
	918	Reserved	R/W	
0x72	919	Reserved	R/W	
0x73	920	Polarity selection of RH_CNT0 UP signal	R/W	0: default (up = 0 down mode, up = 1 up mode) 1: (up = 0 up mode, up = 1 down mode)
	921	Reserved	R/W	
	922	Reserved	R/W	
	923	Polarity selection of RH_CNT1 UP signal	R/W	0: default (up = 0 down mode, up = 1 up mode) 1: (up = 0 up mode, up = 1 down mode)
	924	Reserved	R/W	
	925	Reserved	R/W	
	926	Reserved	R/W	
	927	Reserved	R/W	
HD Buffer				

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x74	928	Chop ACMP Vref selection for calibration channel 0	R/W	000000-111111: 1/64 ~ 64/64 (divider input select by register [946])
	929			
	930			
	931			
	932			
	933			
	934	Chop ACMP calibration channel0 external Vref selection	R/W	0: external Vref (pin18) 1: internal Vref
	935	Reserved	R/W	
0x75	936	Chop ACMP Vref selection for calibration channel 1	R/W	000000-111111: 1/64 ~ 64/64 (divider input select by register [946])
	937			
	938			
	939			
	940			
	941			
	942	Chop ACMP calibration channel1 external Vref selection	R/W	0: external Vref (pin18) 1: internal Vref
	943	Reserved	R/W	
0x76	944	HD buffer register enable (select by register [945])	R/W	0: disable 1: enable
	945	HD buffer enable selection	R/W	0: from register [944] 1: from matrix95
0x76	946	Chop ACMP Vref divider input selection	R/W	0: from HD buffer output 1: from op amp Vref voltage (2.048/V_{DD} selection register in Vref block)
	947	Reserved	R/W	
	948	Reserved	R/W	
	949	Reserved	R/W	
	950	Reserved	R/W	
	951	Reserved	R/W	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
CP OSC/Regulator				
0x77	952	CPOSC single or multiple mode select	R/W	0: multiple OSC mode 1: single OSC mode
	953	Reserved	R/W	
	954 955	CPOSC0 frequency select	R/W	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	956	Reserved	R/W	
	957	Reserved	R/W	
	958		R/W	
	959	Reserved	R/W	
0x78	960	Reserved	R/W	
	961	Reserved	R/W	
	962 963	CPOSC1 frequency select	R/W	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	964	Reserved	R/W	
	965	Reserved	R/W	
	966		R/W	
	967	Reserved	R/W	
0x79	968	Reserved	R/W	
	969	Reserved	R/W	
	970 971	CPOSC2 frequency select	R/W	00: 250 kHz 01: 1 MHz 10: 4 MHz 11: 8 MHz
	972	Reserved	R/W	
	973	Reserved	R/W	
	974		R/W	
	975	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x7A	976	Buffer Vref select	R/W	00: none 01: internal Vref 10: Rheostat Vref 11: external Vref
	977			
	978	Reserved	R/W	
	979	Reserved	R/W	
	980	Reserved	R/W	
	981	Reserved	R/W	
	982	Reserved	R/W	
	983	Reserved	R/W	
0x7B	984	I^2C soft reset	R/W	0: Keep existing condition 1: Reset execution, reload NVM to registers
	985	IO latch enable during I^2C write	R/W	0: disable 1: enable
	986	Reserved	R/W	
	987	Reserved	R/W	
	988	Reserved	R/W	
	989	Reserved	R/W	
	990	Reserved	R/W	
	991	Reserved	R/W	
0x7C	992	Matrix Input 32	R/W	I^2C_virtual_0 Input
	993	Matrix Input 33	R/W	I^2C_virtual_1 Input
	994	Matrix Input 34	R/W	I^2C_virtual_2 Input
	995	Matrix Input 35	R/W	I^2C_virtual_3 Input
	996	Matrix Input 36	R/W	I^2C_virtual_4 Input
	997	Matrix Input 37	R/W	I^2C_virtual_5 Input
	998	Matrix Input 38	R/W	I^2C_virtual_6 Input
	999	Matrix Input 39	R/W	I^2C_virtual_7 Input
0x7D	1000	8-bit Pattern ID Byte 0 (from NVM): ID[23:16]	R/W	
	1001			
	1002			
	1003			
	1004			
	1005			
	1006			
	1007			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x7E	1008	Reserved	R/W	
	1009			
	1010			
	1011			
	1012			
	1013			
	1014			
	1015			
0x7F	1016	I^2C slave address	R/W	
	1017		R/W	
	1018		R/W	
	1019		R/W	
	1020	slave address selection bit0	R/W	0: from register [1016] 1: from Pin15
	1021	slave address selection bit1	R/W	0: from register [1017] 1: from Pin16
	1022	slave address selection bit2	R/W	0: from register [1018] 1: from Pin17
	1023	slave address selection bit3	R/W	0: from register [1019] 1: from Pin18
0x80	1024	Reserved	R	
	1025			
	1026			
	1027			
	1028			
	1029			
	1030			
	1031			
0x81	1032	Reserved	R	
	1033			
	1034			
	1035			
	1036			
	1037			
	1038	Reserved	R	
	1039	Reserved	R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x82	1040	Reserved	R	
	1041			
	1042			
	1043			
	1044			
	1045			
	1046	Reserved	R	
	1047	Reserved	R	
0x83	1048	Reserved	R	
	1049			
	1050			
	1051			
	1052			
	1053			
	1054	Reserved	R	
	1055	Reserved	R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x84	1056	Reserved	R	
	1057			
	1058			
	1059			
	1060			
	1061	Reserved	R	
	1062			
	1063			
0x85	1064			
	1065			
	1066	Reserved	R	
	1067			
	1068			
	1069			
	1070			
	1071	Reserved	R	
0x86	1072			
	1073			
	1074			
	1075			
	1076	Reserved	R	
	1077			
	1078			
	1079			
0x87	1080			
	1081	Reserved	R	
	1082			
	1083			
	1084			
	1085			
	1086	Reserved	R	
	1087			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x88	1088	Reserved	R	
	1089			
	1090			
	1091	Reserved	R	
	1092			
	1093			
	1094			
	1095			
0x89	1096	Reserved	R	
	1097			
	1098			
	1099			
	1100			
	1101	Reserved	R	
	1102			
	1103			
0x8A	1104			
	1105			
	1106	Reserved	R	
	1107			
	1108			
	1109			
	1110			
	1111	Reserved	R	
0x8B	1112			
	1113			
	1114			
	1115			
	1116	Reserved	R	
	1117	Reserved	R	
	1118	Reserved	R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x8B	1119	Reserved	R	
0x8C	1120			
	1121			
	1122			
	1123			
	1124	Reserved	R	
	1125			
	1126			
	1127			
0x8D	1128			
	1129	Reserved	R	
	1130	Reserved	R	
	1131			
	1132			
	1133			
	1134			
	1135	Reserved	R	
0x8E	1136			
	1137			
	1138			
	1139			
	1140	Reserved	R	
	1141	Reserved	R	
	1142			
	1143			
0x8F	1144			
	1145			
	1146	Reserved	R	
	1147			
	1148			
	1149			
	1150			
	1151	Reserved	R	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
SCL/SDA				
0x90	1152	I^2C SCL/SDA input mode select bits (for low voltage in purpose)	R/W	00: digital without Schmitt trigger 01: digital with Schmitt trigger 10: low voltage digital in 11: analog IO
	1153			
	1154	Reserved	R/W	
	1155	I^2C mode selection	R/W	0: I^2C fast mode + 1: I^2C standard/fast mode
IO0				
0x90	1156	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	1157			
	1158	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	1159			
0x91	1160	Pull-up/down resistance selection	R/W	00: floating 01: 10k 10: 100k 11: 1M
	1161			
	1162	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO1				
0x91	1163	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	1164			
	1165	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	1166			
	1167	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
0x92	1168			
	1169	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO2				
0x92	1170	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	1171			
	1172	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	1173			
	1174	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	1175			

Table 70. Register Map (Cont.)

Address Byte	Register Bit	Signal Function	Access Type	Register Bit Definition
0x93	1176	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO3				
0x93	1177 1178	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
0x93	1179 1180	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x93	1181 1182	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
0x93	1183	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO4				
0x94	1184 1185	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
0x94	1186 1187	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x94	1188 1189	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
0x94	1190	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO5				
0x94 0x95	1191 1192	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
0x95	1193 1194	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
0x95	1195 1196	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
0x95	1197	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
IO6				
0x95	1198 1199	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x96	1200	output mode configuration	R/W	00: Push-Pull 1x 01: Push-Pull 2x 10: 1x Open-Drain 11: 2x Open-Drain
	1201			
	1202	Pull-up/down resistance selection	R/W	00: floating 01: 10K 10: 100K 11: 1M
	1203			
	1204	Pull-up/down selection	R/W	0: Pull-down 1: Pull-up
I0				
0x96	1205	input mode configuration	R/W	00: digital without Schmitt Trigger 01: digital with Schmitt Trigger 10: low voltage digital in 11: analog IO
	1206			
	1207	IO fast Pull-up/down enable	R/W	0: disable 1: enable
0x97	1208	Reserved	R/W	
	1209	Reserved	R/W	
	1210	Reserved	R/W	
	1211	Reserved	R/W	
	1212	Reserved	R/W	
	1213	Reserved	R/W	
	1214	Reserved	R/W	
	1215	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x98	1216	Multi0 register configure	R/W	mulit_function selection
	1217			
	1218		R/W	dly2lut selection
	1219			
	1220		R/W	output selection of LUT4_1/DFF17: 0: LUT4_1 1: DFF17
	1221		R/W	external clock selection
	1222			
	1223	DLY/CNT0 Mode Selection	R/W	00: DLY 01: one shoot 10: frequency detect 11: CNT register [1238] = 0
0x99	1224			
	1225	DLY/CNT0 edge Mode Selection	R/W	00: both edge 01: falling edge 10: rising edge 11: High Level Reset (only in CNT mode)
	1226			
	1227	DLY/CNT0 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT6_END 1110: External 1111: Not used
	1228			
	1229			
	1230			
	1231	FSM0 SET/RST Selection	R/W	0: Reset to 0 1: Set to data
0x9A	1232	wake sleep mode selection	R/W	0: Default Mode, 1: Wake Sleep Mode (registers [1224:1223] = 11)
	1233	Wake sleep power down state selection	R/W	0: low 1: high
	1234	Keep signal sync selection	R/W	0: bypass 1: after two DFF
	1235	UP signal sync selection	R/W	0: bypass 1: after two DFF
	1236	CNT0 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1237	CNT0 output pol selection	R/W	0: Default Output 1: Inverted Output
0x9A	1238	CNT0 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1224:1223] = 00)
	1239	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0x9B	1240	Multi1 register configure	R/W	mulit_function selection
	1241			
	1242		R/W	dly2lut selection
	1243			
	1244		R/W	output selection of LUT3_7/DFF11: 0: LUT3_7 1: DFF11
	1245	CNT1 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1251:1248] = 0000/0001/0010)
	1246	CNT1 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1247	CNT1 output pol selection	R/W	0: Default Output 1: Inverted Output
0x9C	1248	CNT1 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1249			
	1250			
	1251			
	1252	DLY/CNT1 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT0_END 1110: External 1111: Not used
	1253			
	1254			
	1255			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x9D	1256	Multi2 register configure	R/W	mulit_function selection
	1257			
	1258		R/W	dly2lut selection
	1259			
	1260		R/W	output selection of LUT3_8/DFF12: 0: LUT3_8 1: DFF12
	1261	CNT2 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1267:1264] = 0000/0001/0010)
	1262	CNT2 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1263	CNT2 output pol selection	R/W	0: Default Output 1: Inverted Output
0x9E	1264	CNT2 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 111: high level reset CNT
	1265			
	1266			
	1267			
	1268	DLY/CNT2 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT1_END 1110: External 1111: Not used
	1269			
	1270			
	1271			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0x9F	1272	Multi3 register configure	R/W	mulit_function selection
	1273			
	1274		R/W	dly2lut selection
	1275			
	1276		R/W	output selection of LUT3_9/DFF13: 0: LUT3_9 1: DFF13
	1277	CNT3 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection(registers [1283:1280] = 0000/0001/0010)
	1278	CNT3 CNT mode SYNC selection	R/W	0: bypass; 1: after two DFF
	1279	CNT3 output pol selection	R/W	0: Default Output, 1: Inverted Output
0xA0	1280	CNT3 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1281			
	1282			
	1283			
	1284	DLY/CNT3 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT2_END 1110: External 1111: Not used
	1285			
	1286			
	1287			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA1	1288	Multi4 register configure	R/W	mulit_function selection
	1289			
	1290		R/W	dly2lut selection
	1291			
	1292		R/W	output selection of LUT3_10/DFF14: 0: LUT3_10 1: DFF14
	1293	CNT4 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1299:1296] = 0000/0001/0010)
	1294	CNT4 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1295	CNT4 output pol selection	R/W	0: Default Output 1: Inverted Output
0xA2	1296	CNT4 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect; 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1297			
	1298			
	1299			
	1300	DLY/CNT4 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT3_END 1110: External 1111: Not used
	1301			
	1302			
	1303			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA3	1304	Multi5 register configure	R/W	mulit_function selection
	1305			
	1306		R/W	dly2lut selection
	1307			
	1308		R/W	output selection of LUT3_11/DFF15: 0: LUT3_11 1: DFF15
	1309	CNT5 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1315:1312] = 0000/0001/0010)
	1310	CNT5 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1311	CNT5 output pol selection	R/W	0: Default Output 1: Inverted Output
0xA4	1312	CNT5 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1313			
	1314			
	1315			
	1316	DLY/CNT5 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT4_END 1110: External 1111: Not used
	1317			
	1318			
	1319			

Table 70. Register Map (Cont.)

Address Byte	Register Bit	Signal Function	Access Type	Register Bit Definition
0xA5	1320	Multi6 register configure	R/W	mulit_function selection
	1321			
	1322		R/W	dly2lut selection
	1323			
	1324		R/W	output selection of LUT3_12/DFF16: 0: LUT3_12 1: DFF16
	1325	CNT6 DLY EDET FUNCTION Selection	R/W	0: normal 1: DLY function edge detection (registers [1331:1328] = 0000/0001/0010)
	1326	CNT6 CNT mode SYNC selection	R/W	0: bypass 1: after two DFF
	1327	CNT6 output pol selection	R/W	0: Default Output 1: Inverted Output
0xA6	1328	CNT6 function and edge mode selection	R/W	0000: both edge Delay 0001: falling edge delay 0010: rising edge delay 0011: both edge One Shot 0100: falling edge One Shot 0101: rising edge One Shot 0110: both edge freq detect 0111: falling edge freq detect 1000: rising edge freq detect 1001: both edge detect 1010: falling edge detect 1011: rising edge detect 1100: both edge reset CNT 1101: falling edge reset CNT 1110: rising edge reset CNT 1111: high level reset CNT
	1329			
	1330			
	1331			
	1332	DLY/CNT6 Clock Source Select	R/W	Clock source sel[3:0] 0000: 25M(OSC2) 0001: 25M/4 0010: 2M(OSC1) 0011: 2M/8 0100: 2M/64 0101: 2M/512 0110: 2K(OSC0) 0111: 2K/8 1000: 2K/64 1001: 2K/512 1010: 2K/4096 1011: 2K/32768 1100: 2K/262144 1101: CNT5_END 1110: External 1111: Not used
	1333			
	1334			
	1335			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA7	1336	CNT0 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1337			
	1338	CNT1 initial value selection	R/W	00:bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1339			
	1340	CNT6 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1341			
	1342	Reserved	R/W	
	1343	Reserved	R/W	
0xA8	1344	CNT2 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1345			
	1346	CNT3 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1347			
	1348	CNT4 initial value selection	R/W	00: bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1349			
	1350	CNT5 initial value selection	R/W	00:bypass the initial 01: initial 0 10: initial 1 11: initial 1
	1351			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xA9	1352	Multi0_LUT4_DFF setting	R/W	<12:0>:LUT4_1 <12:0>
	1353			
	1354			
	1355			
	1356			
	1357			
	1358			
	1359			
0xAA	1360			
	1361			
	1362			
	1363			
	1364			
	1365		R/W	<13>:LUT4_1 <13>/DFF17 Initial Polarity Select 0: Low, 1: High
	1366		R/W	<14>:LUT4_1 <14>/DFF17 Output Select 0: Q output, 1: QB output
	1367		R/W	<15>:LUT4_1 <15>/DFF17 or Latch Select 0: DFF function, 1: Latch function
0xAB	1368	REG_CNT0_D<15:0>	R/W	Data[15:0]
	1369			
	1370			
	1371			
	1372			
	1373			
	1374			
	1375			
0xAC	1376			
	1377			
	1378			
	1379			
	1380			
	1381			
	1382			
	1383			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xAD	1384	Multi1_LUT3_DFF setting	R/W	<3:0>:LUT3_7 <3:0>
	1385			
	1386			
	1387			
	1388		R/W	<4>:LUT3_7 <4>/DFF11 Initial Polarity Select 0: Low, 1: High
	1389		R/W	<5>:LUT3_7 <5>/DFF11 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1390		R/W	<6>:LUT3_7 <6>/DFF11 Output Select 0: Q output, 1: QB output
	1391		R/W	<7>:LUT3_7 <7>/DFF11 or Latch Select 0: DFF function, 1: Latch function
Multi1_CNT1				
0xAE	1392	REG_CNT1_D<7:0>	R/W	Data[7:0]
	1393			
	1394			
	1395			
	1396			
	1397			
	1398			
	1399			
0xAF	1400	Multi2_LUT3_DFF setting	R/W	<3:0>:LUT3_8 <3:0>
	1401			
	1402			
	1403			
	1404		R/W	<4>:LUT3_8 <4>/DFF12 Initial Polarity Select 0: Low, 1: High
	1405		R/W	<5>:LUT3_8 <5>/DFF12 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1406		R/W	<6>:LUT3_8 <6>/DFF12 Output Select 0: Q output, 1: QB output
	1407		R/W	<7>:LUT3_8 <7>/DFF12 or Latch Select 0: DFF function, 1: Latch function

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB0	1408	REG_CNT2_D<7:0>	R/W	Data[7:0]
	1409			
	1410			
	1411			
	1412			
	1413			
	1414			
	1415			
0xB1	1416	Multi3_LUT3_DFF setting	R/W	<3:0>:LUT3_9 <3:0>
	1417			
	1418			
	1419			
	1420		R/W	<4>:LUT3_9 <4>/DFF13 Initial Polarity Select 0: Low, 1: High
	1421		R/W	<5>:LUT3_9 <5>/DFF13 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1422		R/W	<6>:LUT3_9 <6>/DFF13 Output Select 0: Q output, 1: QB output
	1423		R/W	<7>:LUT3_9 <7>/DFF13 or Latch Select 0: DFF function, 1: Latch function
0xB2	1424	REG_CNT3_D<7:0>	R/W	Data[7:0]
	1425			
	1426			
	1427			
	1428			
	1429			
	1430			
	1431			
0xB3	1432	Multi4_LUT3_DFF setting	R/W	<3:0>:LUT3_10 <3:0>
	1433			
	1434			
	1435			
	1436		R/W	<4>:LUT3_10 <4>/DFF14 Initial Polarity Select 0: Low, 1: High
	1437		R/W	<5>:LUT3_10 <5>/DFF14 0: RSTB from Matrix Output, 1: SETB from Matrix Output

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB3	1438	Multi4_LUT3_DFF setting	R/W	<6>:LUT3_10 <6>/DFF14 Output Select 0: Q output, 1: QB output
	1439		R/W	<7>:LUT3_10 <7>/DFF14 or Latch Select 0: DFF function, 1: Latch function
0xB4	1440	REG_CNT4_D<7:0>	R/W	Data[7:0]
	1441			
	1442			
	1443			
	1444			
	1445			
	1446			
	1447			
0xB5	1448	Multi5_LUT3_DFF setting	R/W	<3:0>:LUT3_11<3:0>
	1449			
	1450			
	1451			
	1452		R/W	<4>:LUT3_11<4>/DFF15 Initial Polarity Select 0: Low, 1: High
	1453		R/W	<5>:LUT3_11 <5>/DFF15 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1454		R/W	<6>:LUT3_11 <6>/DFF15 Output Select 0: Q output, 1: QB output
	1455		R/W	<7>:LUT3_11 <7>/DFF15 or Latch Select 0: DFF function, 1: Latch function
0xB6	1456	REG_CNT5_D<7:0>	R/W	Data[7:0]
	1457			
	1458			
	1459			
	1460			
	1461			
	1462			
	1463			
0xB7	1464	Multi6_LUT3_DFF setting	R/W	<3:0>:LUT3_12 <3:0>
	1465			
	1466			
	1467			

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xB7	1468	Multi6_LUT3_DFF setting	R/W	<4>:LUT3_12 <4>/DFF16 Initial Polarity Select 0: Low, 1: High
	1469		R/W	<5>:LUT3_12 <5>/DFF16 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1470		R/W	<6>:LUT3_12 <6>/DFF16 Output Select 0: Q output, 1: QB output
	1471		R/W	<7>:LUT3_12 <7>/DFF16 or Latch Select 0: DFF function, 1: Latch function
0xB8	1472	REG_CNT6_D<7:0>	R/W	Data[7:0]
	1473			
	1474			
	1475			
	1476			
	1477			
	1478			
	1479			

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xB9	1480	LUT2_0/DFF0 setting	R/W	<0>:LUT2_0 <0>
	1481		R/W	<1>:LUT2_0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1482		R/W	<2>:LUT2_0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1483		R/W	<3>:LUT2_0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
	1484	LUT2_1/DFF1 setting	R/W	<0>:LUT2_0 <0>
	1485		R/W	<1>:LUT2_0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1486		R/W	<2>:LUT2_0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1487		R/W	<3>:LUT2_0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
0xBA	1488	LUT2_2/DFF2 setting	R/W	<0>:LUT2_0 <0>
	1489		R/W	<1>:LUT2_0 <1>/DFF0 Initial Polarity Select 0: Low, 1: High
	1490		R/W	<2>:LUT2_0 <2>/DFF0 Output Select 0: Q output, 1: QB output
	1491		R/W	<3>:LUT2_0 <3>/DFF0 or Latch Select 0: DFF function, 1: Latch function
	1492	LUT2_0 or DFF0 Select	R/W	0: LUT2_0 1: DFF0
	1493	LUT2_1 or DFF1 Select	R/W	0: LUT2_1 1: DFF1
	1494	LUT2_2 or DFF2 Select	R/W	0: LUT2_2 1: DFF2
	1495	Reserved	R/W	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xBB	1496	PGen data	R/W	PGen Data[15:0]
	1497			
	1498			
	1499			
	1500			
	1501			
	1502			
	1503			
0xBC	1504			
	1505			
	1506			
	1507			
	1508			
	1509			
	1510			
	1511			
0xBD	1512	LUT2_3_VAL or PGen_data	R/W	LUT2_3<3:0> or PGen 4bit counter data<3:0>
	1513			
	1514			
	1515			
	1516	LUT2_3 or PGen Select	R/W	0: LUT2_3 1: PGen
	1517	Active level selection for RST/SET	R/W	0: Active low level reset/set 1: Active high level reset/set
	1518	LUT3_0 or DFF3 Select	R/W	0: LUT3_0 1: DFF3
	1519	LUT3_1 or DFF4 Select	R/W	0: LUT3_1 1: DFF4
0xBE	1520	LUT3_0_DFF3 setting	R/W	<1:0>: LUT3_0 <1:0>
	1521			
	1522		R/W	<2>:LUT3_0 <2>/DFF3 stage selection 0: Q of first DFF; 1 Q of second DFF
	1523		R/W	<3>:LUT3_0 <3>/DFF3 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xBE	1524	LUT3_0_DFF3 setting	R/W	<4>:LUT3_0 <4>/DFF3 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1525		R/W	<5>:LUT3_0 <5>/DFF3 Initial Polarity Select 0: Low, 1: High
	1526		R/W	<6>:LUT3_0 <6>/DFF3 Output Select 0: Q output, 1: QB output
	1527		R/W	<7>:LUT3_0 <7>/DFF3 or Latch Select 0: DFF function, 1: Latch function
0xBF	1528	LUT3_1_DFF4 setting	R/W	<2:0>: LUT3_1 <2:0>
	1529			
	1530			
	1531		R/W	<3>:LUT3_1 <3>/DFF4 Active level selection for RST/SET 0: Active low level reset/set, 1: Active high level reset/set
	1532		R/W	<4>:LUT3_1 <4>/DFF4 0: RSTB from Matrix Output, 1: SETB from Matrix Output
	1533		R/W	<5>:LUT3_1 <5>/DFF4 Initial Polarity Select 0: Low, 1: High
	1534		R/W	<6>:LUT3_1 <6>/DFF4 Output Select 0: Q output, 1: QB output
	1535		R/W	<7>:LUT3_1 <7>/DFF4 or Latch Select 0: DFF function, 1: Latch function
0xC0	1536	Rheostat0 data selection	R/W	0000000000: 0 ~ 1111111111:100k
	1537			
	1538			
	1539			
	1540			
	1541			
	1542			
	1543			
0xC1	1544			
	1545			
	1546	Reserved	R/W	
	1547	Reserved	R/W	
	1548	Reserved	R/W	
	1549	Reserved	R/W	
	1550	Reserved	R/W	
	1551	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xC2	1552	Rheostat0 current value (read only)	R	
	1553		R	
	1554		R	
	1555		R	
	1556		R	
	1557		R	
	1558		R	
	1559		R	
0xC3	1560		R	
	1561		R	
	1562	Reserved	R	
	1563	Reserved	R	
	1564	Reserved	R	
	1565	Reserved	R	
	1566	Reserved	R	
	1567	Reserved	R	
0xC4	1568	Matrix Input 0	R	GND
	1569	Matrix Input 1	R	LUT2_0/DFF0 output
	1570	Matrix Input 2	R	LUT2_1/DFF1 output
	1571	Matrix Input 3	R	LUT2_2/DFF2 output
	1572	Matrix Input 4	R	LUT2_3/PGen output
	1573	Matrix Input 5	R	LUT3_0/DFF3 output
	1574	Matrix Input 6	R	LUT3_1/DFF4 output
	1575	Matrix Input 7	R	LUT3_2/DFF5 output
0xC5	1576	Matrix Input 8	R	LUT3_3/DFF6 output
	1577	Matrix Input 9	R	LUT3_4/DFF7 output
	1578	Matrix Input 10	R	LUT3_5/DFF8 output
	1579	Matrix Input 11	R	LUT3_6/DFF9 output
	1580	Matrix Input 12	R	CNT_DLY0 output
	1581	Matrix Input 13	R	MLT0_LUT4_1/DFF17_OUT
	1582	Matrix Input 14	R	CNT_DLY1 output
	1583	Matrix Input 15	R	MLT1_LUT3_7/DFF11_OUT

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xC6	1584	Matrix Input 16	R	CNT_DLY2 output
	1585	Matrix Input 17	R	MLT2_LUT3_8/DFF12_OUT
	1586	Matrix Input 18	R	CNT_DLY3 output
	1587	Matrix Input 19	R	MLT3_LUT3_9/DFF13_OUT
	1588	Matrix Input 20	R	CNT_DLY4 output
	1589	Matrix Input 21	R	MLT4_LUT3_10/DFF14_OUT
	1590	Matrix Input 22	R	CNT_DLY5 output
	1591	Matrix Input 23	R	MLT5_LUT3_11/DFF15_OUT
0xC7	1592	Matrix Input 24	R	CNT_DLY6 output
	1593	Matrix Input 25	R	MLT6_LUT3_12/DFF16_OUT
	1594	Matrix Input 26	R	LUT3_13/Pipe Delay/RippleCNT_out0
	1595	Matrix Input 27	R	Pipe Delay/RippleCNT_out1
	1596	Matrix Input 28	R	Pipe Delay/RippleCNT_out2
	1597	Matrix Input 29	R	LUT4_0/DFF10 output
	1598	Matrix Input 30	R	Programmable Delay Edge Detect Output
	1599	Matrix Input 31	R	Edge Detect Filter Output
0xC8	1600	Matrix Input 40	R	RH0 Idle/Active
	1601	Matrix Input 41	R	RH1 Idle/Active
	1602	Matrix Input 42	R	Output of Op Amp0 in ACMP mode
	1603	Matrix Input 43	R	Output of Op Amp1 in ACMP mode
	1604	Matrix Input 44	R	IO0 Digital Input
	1605	Matrix Input 45	R	IO1 Digital Input
	1606	Matrix Input 46	R	IO2 Digital Input
	1607	Matrix Input 47	R	IO3 Digital Input
0xC9	1608	Matrix Input 48	R	IO4 Digital Input
	1609	Matrix Input 49	R	IO5 Digital Input
	1610	Matrix Input 50	R	IO6 Digital Input
	1611	Matrix Input 51	R	I0 Digital Input
	1612	Matrix Input 52	R	Oscillator0 output 0
	1613	Matrix Input 53	R	Oscillator1 output 0
	1614	Matrix Input 54	R	Oscillator2 output
	1615	Matrix Input 55	R	Chopper ACMP Out

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xCA	1616	Matrix Input 56	R	ACMP0 Output (low speed)
	1617	Matrix Input 57	R	ACMP1 Output (low speed)
	1618	Matrix Input 58	R	Oscillator0 output 1
	1619	Matrix Input 59	R	Oscillator1 output 1
	1620	Matrix Input 60	R	POR OUT
	1621	Matrix Input 61	R	V_{DD}
	1622	Matrix Input 62	R	V_{DD}
	1623	Matrix Input 63	R	V_{DD}
0xCB	1624	CNT0_Q	R	
	1625		R	
	1626		R	
	1627		R	
	1628		R	
	1629		R	
	1630		R	
	1631		R	
0xCC	1632		R	
	1633		R	
	1634		R	
	1635		R	
	1636		R	
	1637		R	
	1638		R	
	1639		R	
0xCD	1640	CNT5_Q	R	
	1641		R	
	1642		R	
	1643		R	
	1644		R	
	1645		R	
	1646		R	
	1647		R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xCE	1648	CNT6_Q	R	
	1649		R	
	1650		R	
	1651		R	
	1652		R	
	1653		R	
	1654		R	
	1655		R	
0xCF	1656	Reserved	R/W	
	1657	Reserved	R/W	
	1658	Reserved	R/W	
	1659	Reserved	R/W	
	1660	Reserved	R/W	
	1661	Reserved	R/W	
	1662	Reserved	R/W	
	1663	Reserved	R/W	
0xD0	1664	Rheostat1 data selection	R/W	0000000000: 0 ~ 1111111111:100k
	1665			
	1666			
	1667			
	1668			
	1669			
	1670			
	1671			
0xD1	1672			
	1673			
	1674	Reserved	R/W	
	1675	Reserved	R/W	
	1676	Reserved	R/W	
	1677	Reserved	R/W	
	1678	Reserved	R/W	
	1679	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xD2	1680	Rheostat1 current value (read only)	R	
	1681		R	
	1682		R	
	1683		R	
	1684		R	
	1685		R	
	1686		R	
	1687		R	
0xD3	1688		R	
	1689		R	
	1690	Reserved	R	
	1691	Reserved	R	
	1692	Reserved	R	
	1693	Reserved	R	
	1694	Reserved	R	
	1695	Reserved	R	
0xD4	1696	Reserved	R/W	
	1697	Reserved	R/W	
	1698	Reserved	R/W	
	1699	Reserved	R/W	
	1700	Reserved	R/W	
	1701	Reserved	R/W	
	1702	Reserved	R/W	
	1703	Reserved	R/W	
0xD5	1704	Reserved	R/W	
	1705	Reserved	R/W	
	1706	Reserved	R/W	
	1707	Reserved	R/W	
	1708	Reserved	R/W	
	1709	Reserved	R/W	
	1710	Reserved	R/W	
	1711	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xD6	1712	Reserved	R/W	
	1713	Reserved	R/W	
	1714	Reserved	R/W	
	1715	Reserved	R/W	
	1716	Reserved	R/W	
	1717	Reserved	R/W	
	1718	Reserved	R/W	
	1719	Reserved	R/W	
0xD7	1720	Reserved	R/W	
	1721	Reserved	R/W	
	1722	Reserved	R/W	
	1723	Reserved	R/W	
	1724	Reserved	R/W	
	1725	Reserved	R/W	
	1726	Reserved	R/W	
	1727	Reserved	R/W	
0xD8	1728	Reserved	R/W	
	1729	Reserved	R/W	
	1730	Reserved	R/W	
	1731	Reserved	R/W	
	1732	Reserved	R/W	
	1733	Reserved	R/W	
	1734	Reserved	R/W	
	1735	Reserved	R/W	
0xD9	1736	Reserved	R/W	
	1737	Reserved	R/W	
	1738	Reserved	R/W	
	1739	Reserved	R/W	
	1740	Reserved	R/W	
	1741	Reserved	R/W	
	1742	Reserved	R/W	
	1743	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xDA	1744	Reserved	R/W	
	1745	Reserved	R/W	
	1746	Reserved	R/W	
	1747	Reserved	R/W	
	1748	Reserved	R/W	
	1749	Reserved	R/W	
	1750	Reserved	R/W	
	1751	Reserved	R/W	
0xDB	1752	Reserved	R/W	
	1753	Reserved	R/W	
	1754	Reserved	R/W	
	1755	Reserved	R/W	
	1756	Reserved	R/W	
	1757	Reserved	R/W	
	1758	Reserved	R/W	
	1759	Reserved	R/W	
0xDC	1760	Reserved	R/W	
	1761	Reserved	R/W	
	1762	Reserved	R/W	
	1763	Reserved	R/W	
	1764	Reserved	R/W	
	1765	Reserved	R/W	
	1766	Reserved	R/W	
	1767	Reserved	R/W	
0xDD	1768	ID[24]: Reserved	R	
	1769	ID[25]: Reserved	R	Reserved for NVM Power-Up Check Pattern Status (A55A match from Flag)
	1770	ID[27:26]: Reserved for Silicon Identification Service Bits (metal hard code)	R	
	1771		R	
	1772	Reserved	R	
	1773		R	
	1774		R	
	1775		R	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xDE	1776	Reserved	R	
	1777			
	1778			
	1779			
	1780			
	1781			
	1782			
	1783			
0xDF	1784	Reserved	R	
	1785			
	1786			
	1787			
	1788			
	1789			
	1790			
	1791			
0xE0	1792	RPR<1:0> (2k register read selection bits)	R/W* (see section 18.6)	00: 2k register data is unprotected for read 01: 2k register data is partly protected for read 10: 2k register data is fully protected for read 11: reserved
	1793			
	1794	RPR<3:2> (2k register write selection bits)	R/W* (see section 18.6)	00: 2k register data is unprotected for write 01: 2k register data is partly protected for write 10: 2k register data is fully protected for write 11: reserved
	1795			
	1796	RH_PRB	R/W* (see section 18.6)	0: Rheostat Program Input from matrix enabled 1: Rheostat Program Input from matrix disabled
	1797	Reserved	R/W* (see section 18.6)	
	1798	Reserved	R/W* (see section 18.6)	
	1799	Reserved	R/W* (see section 18.6)	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xE1	1800 1801	NPR<1:0> (2k NVM configuration selection bits)	R/W* (see section 18.6)	00: 2k NVM Configuration data is unprotected for read and write/erase 01: 2k NVM Configuration data is fully protected for read 10: 2k NVM Configuration data is fully protected for write/erase 11: 2k NVM Configuration data is fully protected for read and write/erase
	1802 1803	NPR<3:2> (Rheostat0 NVM configuration selection bits)	R/W* (see section 18.6)	00: Rheosta0 NVM Configuration data is unprotected for read and write/erase 01: Rheosta0 NVM Configuration data is fully protected for read 10: Rheosta0 NVM Configuration data is fully protected for write/erase 11: Rheosta0 NVM Configuration data is fully protected for read and write/erase
	1804 1805	NPR<5:4> (Rheostat1 NVM configuration selection bits)	R/W* (see section 18.6)	00: Rheosta1 NVM Configuration data is unprotected for read and write/erase 01: Rheosta1 NVM Configuration data is fully protected for read 10: Rheosta1 NVM Configuration data is fully protected for write/erase 11: Rheosta1 NVM Configuration data is fully protected for read and write/erase
	1806	Reserved	R/W* (see section 18.6)	
	1807	Reserved	R/W* (see section 18.6)	
0xE2	1808 1809	Reserved	R/W* (see section 18.6)	
	1810	Reserved	R/W* (see section 18.6)	
	1811	Reserved	R/W* (see section 18.6)	
	1812	Reserved	R/W* (see section 18.6)	
	1813	Reserved	R/W* (see section 18.6)	
	1814	Reserved	R/W* (see section 18.6)	
	1815	Reserved	R/W* (see section 18.6)	
0xE3	1816 1817 1818 1819 1820	ERSE<4:0> (Page selection for erase)	W** (see section 18.6)	Define the page address which will be erased ERSE<4> = 0 corresponds to the upper 2k NVM used for chip configuration
	1821 1822 1823	ERSE <2:0> (Erase enable)	W** (see section 18.6)	000/001/010/011/100/101/111: erase disable 110: cause the NVM erase: full NVM (4k bits) erase for ERSCHIP = 1 if DIS_ERSCHIP=0 or page erase for ERSCHIP=0.

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xE4	1824	PRL (Protection lock)	R/W	0: RPR/WPR/NPR setting can be changed 1: RPR/WPR/NPR setting cannot be changed
	1825	Reserved	R/W	
	1826	Reserved	R/W	
	1827	Reserved	R/W	
	1828	Reserved	R/W	
	1829	Reserved	R/W	
	1830	Reserved	R/W	
	1831	Reserved	R/W	
0xE5	1832	Reserved	R/W	
	1833		R/W	
	1834		R/W	
	1835		R/W	
	1836		R/W	
	1837		R/W	
	1838		R/W	
	1839		R/W	
0xE6	1840	Rheostat0 tolerance data <0>	R	
	1841	Rheostat0 tolerance data <1>	R	
	1842	Rheostat0 tolerance data <2>	R	
	1843	Rheostat0 tolerance data <3>	R	
	1844	Rheostat0 tolerance data <4>	R	
	1845	Rheostat0 tolerance data <5>	R	
	1846	Rheostat0 tolerance data <6>	R	
	1847	Rheostat0 tolerance data <7>	R	
0xE7	1848	Rheostat0 tolerance data <8>	R	
	1849	Rheostat0 tolerance data <9>	R	
	1850	Rheostat0 tolerance data <10>	R	
	1851	Rheostat0 tolerance data <11>	R	
	1852	Rheostat0 tolerance data <12>	R	
	1853	Rheostat0 tolerance data <13>	R	
	1854	Rheostat0 tolerance data <14>	R	
	1855	Sign of Rheostat0 tolerance data	R	0: “+” 1: "-"

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xE8	1856	Rheostat1 tolerance data <0>	R	
	1857	Rheostat1 tolerance data <1>	R	
	1858	Rheostat1 tolerance data <2>	R	
	1859	Rheostat1 tolerance data <3>	R	
	1860	Rheostat1 tolerance data <4>	R	
	1861	Rheostat1 tolerance data <5>	R	
	1862	Rheostat1 tolerance data <6>	R	
	1863	Rheostat1 tolerance data <7>	R	
0xE9	1864	Rheostat1 tolerance data <8>	R	
	1865	Rheostat1 tolerance data <9>	R	
	1866	Rheostat1 tolerance data <10>	R	
	1867	Rheostat1 tolerance data <11>	R	
	1868	Rheostat1 tolerance data <12>	R	
	1869	Rheostat1 tolerance data <13>	R	
	1870	Rheostat1 tolerance data <14>	R	
	1871	Sign of Rheostat1 tolerance data	R	0: "+"; 1: "-"
0xEA	1872	Reserved	R	
	1873			
	1874			
	1875			
	1876	Reserved	R	
	1877			
	1878			
	1879			
0xEB	1880	Reserved	R	
	1881			
	1882			
	1883			
	1884	Reserved	R	
	1885	Reserved	R	
	1886	Reserved	R	
	1887	Reserved	R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xEC	1888	Reserved	R/W	
	1889	Reserved	R/W	
	1890	Reserved	R/W	
	1891	Reserved	R/W	
	1892	Reserved	R/W	
	1893	Reserved	R/W	
	1894	Reserved	R/W	
	1895	Reserved	R/W	
0xED	1896	Reserved	R/W	
	1897	Reserved	R/W	
	1898	Reserved	R/W	
	1899	Reserved	R/W	
	1900	Reserved	R/W	
	1901	Reserved	R/W	
	1902	Reserved	R/W	
	1903	Reserved	R/W	
0xEE	1904	Reserved	R/W	
	1905	Reserved	R/W	
	1906	Reserved	R/W	
	1907	Reserved	R/W	
	1908	Reserved	R/W	
	1909	Reserved	R/W	
	1910	Reserved	R/W	
	1911	Reserved	R/W	
0xEF	1912	Reserved	R/W	
	1913	Reserved	R/W	
	1914	Reserved	R/W	
	1915	Reserved	R/W	
	1916	Reserved	R/W	
	1917	Reserved	R/W	
	1918	Reserved	R/W	
	1919	Reserved	R/W	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xF0	1920	Reserved	R	
	1921			
	1922			
	1923			
	1924			
	1925			
	1926			
	1927			
0xF1	1928	Reserved	R	
	1929			
	1930			
	1931			
	1932			
	1933			
	1934			
	1935			
0xF2	1936	Reserved	R	
	1937			
	1938			
	1939			
	1940			
	1941			
	1942			
	1943			
0xF3	1944	Service page lock bit	R	0: Service page can be changed 1: Service page is locked
	1945	BG Chopper off	R	0: chopper enable 1: chopper off
	1946	Reserved	R	
	1947	Reserved	R	
	1948	BG register power down	R	0: power on 1: power off
	1949	Reserved	R	
	1950	Reserved	R	
	1951	Reserved	R	

Table 70. Register Map (Cont.)

Address Byte	Address Register Bit	Signal Function	Access Type	Register Bit Definition
0xF4	1952	Reserved	R	
	1953	Reserved	R	
	1954	Reserved	R	
	1955	Reserved	R	
	1956	Reserved	R	
	1957	Reserved	R	
	1958	Reserved	R	
	1959	Reserved	R	
0xF5	1960	Reserved	R/W	
	1961	Reserved	R/W	
	1962	Reserved	R/W	
	1963	Reserved	R/W	
	1964	Reserved	R/W	
	1965	Reserved	R/W	
	1966	Reserved	R/W	
	1967	Reserved	R/W	
0xF6	1968	I^2C write mask bits	R/W	0: overwrite; 1: mask the bit which set to high
	1969			
	1970			
	1971			
	1972			
	1973			
	1974			
	1975			
0xF7	1976	Reserved	R	
	1977		R	
	1978		R	
	1979		R	
	1980		R	
	1981		R	
	1982		R	
	1983		R	

Table 70. Register Map (Cont.)

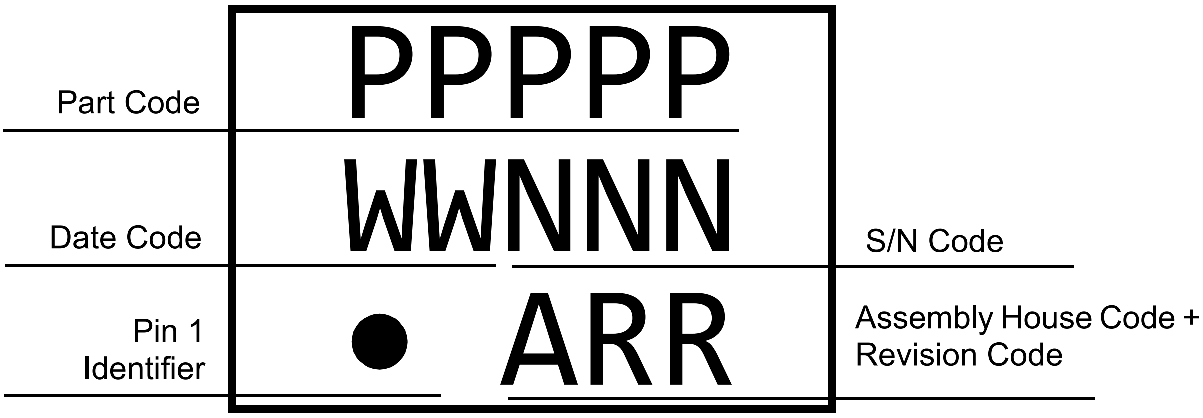
Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xF8	1984	Reserved	R	
	1985		R	
	1986		R	
	1987		R	
	1988		R	
	1989		R	
	1990		R	
	1991		R	
0xF9	1992	Reserved	R	
	1993		R	
	1994		R	
	1995		R	
	1996		R	
	1997		R	
	1998		R	
	1999	Reserved	R	
0xFA	2000	Reserved	R	
	2001		R	
	2002		R	
	2003		R	
	2004		R	
	2005	Reserved	R	
	2006	Reserved	R	
	2007	Reserved	R	
0xFB	2008	Reserved	R	
	2009		R	
	2010		R	
	2011		R	
	2012		R	
	2013	Reserved	R	
	2014	Reserved	R	
	2015	Reserved	R	

Table 70. Register Map (Cont.)

Address		Signal Function	Access Type	Register Bit Definition
Byte	Register Bit			
0xFC	2016	Reserved	R	
	2017			
	2018			
	2019			
	2020			
	2021	Reserved	R	
	2022	Reserved	R	
	2023	Reserved	R	
0xFD	2024	Reserved	R	
	2025			
	2026			
	2027			
	2028			
	2029	Reserved	R	
	2030	Reserved	R	
	2031	Reserved	R	
0xFE	2032	Reserved	R	
	2033		R	
	2034		R	
	2035		R	
	2036		R	
	2037	Reserved	R	
	2038	Reserved	R	
	2039	Reserved	R	
0xFF	2040	Reserved	R/W	
	2041	Reserved	R/W	
	2042	Reserved	R/W	
	2043	Reserved	R/W	
	2044	Reserved	R/W	
	2045	Reserved	R/W	
	2046	Reserved	R/W	
	2047	Reserved	R/W	

22. Package Top Marking Definitions

22.1 TQFN-24 4 mm x 4 mm x 0.75 mm 0.5P

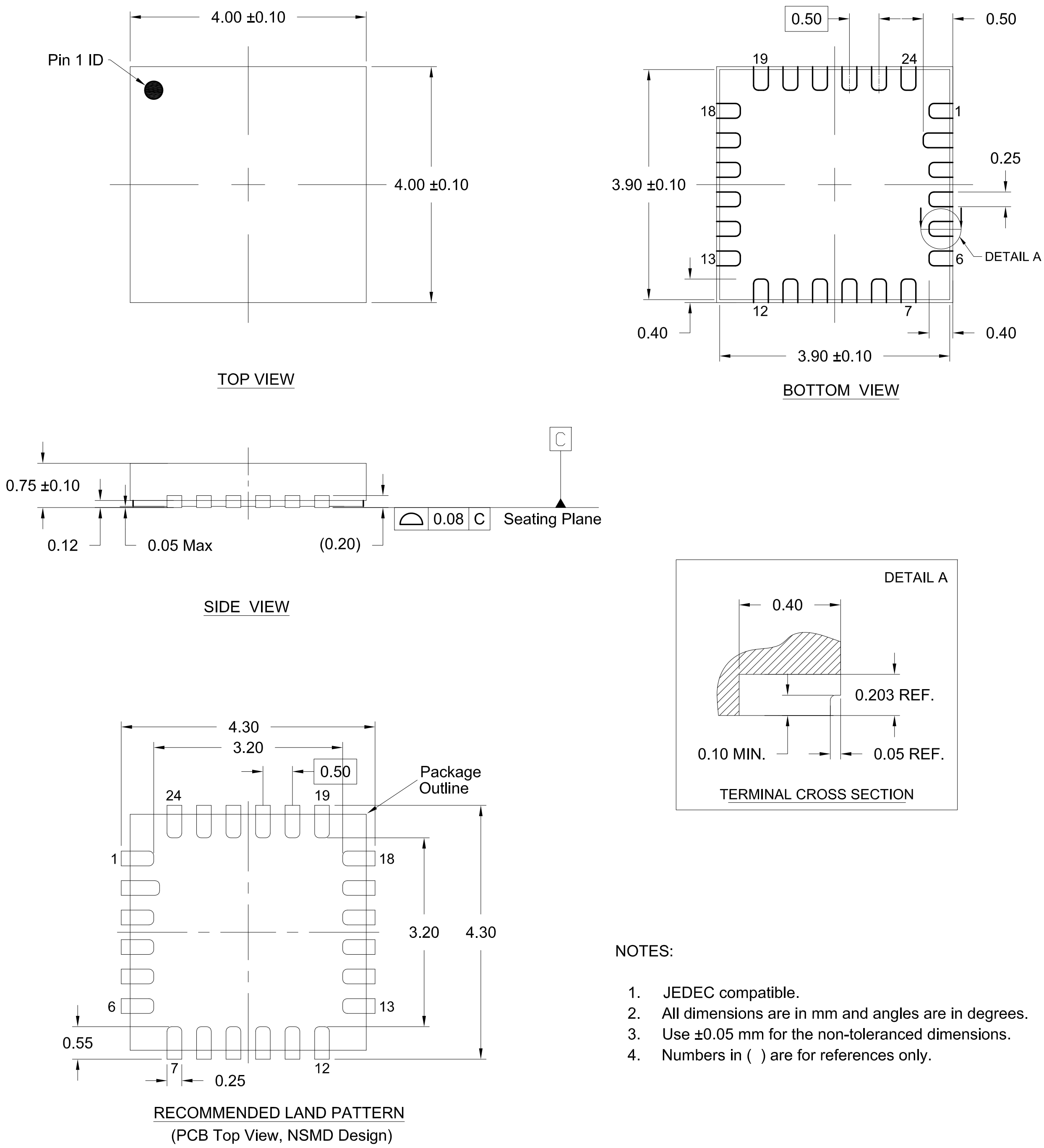


23. Package Information

23.1 Package Outlines for TQFN-24 4 mm x 4 mm x 0.75 mm, 0.5P

JEDEC MO-220

IC Net Weight: 0.0116 g



NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.

Figure 250. TQFN-24 4x4 mm 0.5P

23.2 TQFN Handling

Be sure to handle TQFN package only in a clean, ESD-safe environment. Tweezers or vacuum pick-up tools are suitable for handling. Do not handle TQFN package with fingers as this can contaminate the package pins and interface with solder reflow.

23.3 Soldering Information

Please see IPC/JEDEC J-STD-020: for relevant soldering information. More information can be found at www.jedec.org.

24. Layout Guidelines

SLG47004-A has two analog supply pins and two ground pins: V_{DD}, V_{DDA}, GND, and AGND. Separating analog supply voltage from digital one helps to minimize noise generated by the digital part of IC.

Analog supply voltage domain: operational amplifiers, charge pumps for op amps, charge pumps for Oscillators, bias generators and regulators for op amps, digital rheostats, Chopper ACMP, HD Buffer, Vref of op amp and HD Buffer, Low Power Bandgap.

Digital supply voltage domain: ACMPs, Vref of ACMPs, Vref output buffers, Oscillator 0, Oscillator 1, Oscillator 2, I^2C macrocell, NVM logic, Multi-function, and Combination Function macrocells.

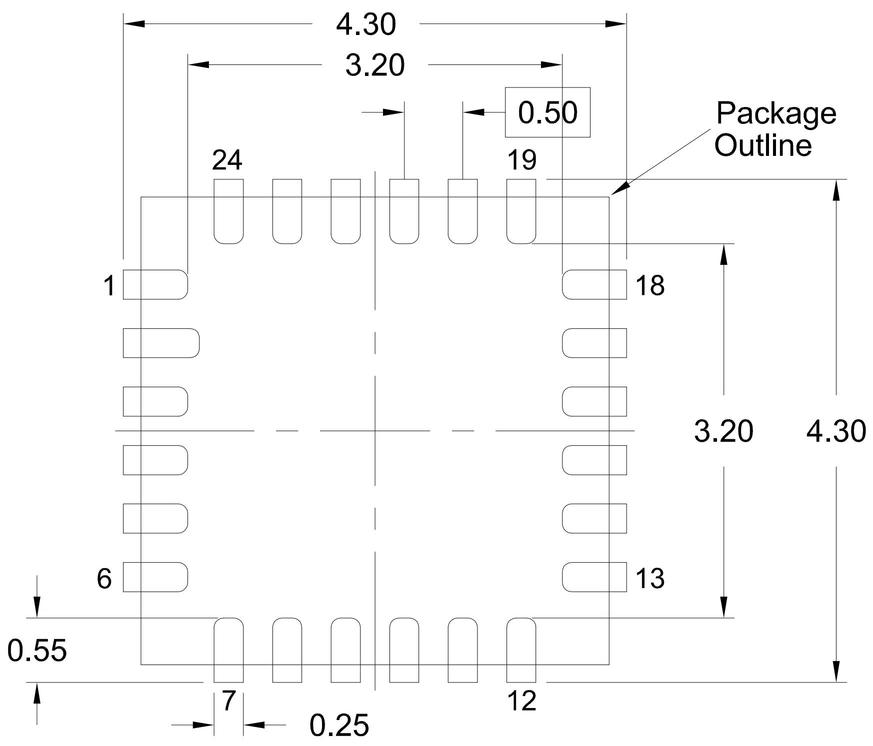
Analog and digital grounds must be connected together on the PCB board. The place of connection depends on users schematic. For application cases with low digital current of SLG47004-A, both AGND and GND should be connected to analog ground plane.

It is strongly recommended to connect I0 (Pin21) to the ground if it is not used in the project.

The following suggestions allow to minimize the impact of digital blocks operation on the analog macrocells:

- decrease the slew rate of input digital signals
- use proper grounding. If possible, use grounding polygons along the input/output digital traces
- to interface digital signals first use IO1, IO2, IO3, IO4, then use other GPIOs.

24.1 TQFN-24 4 mm x 4mm x 0.75 mm, 0.5P



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

25. Ordering Information

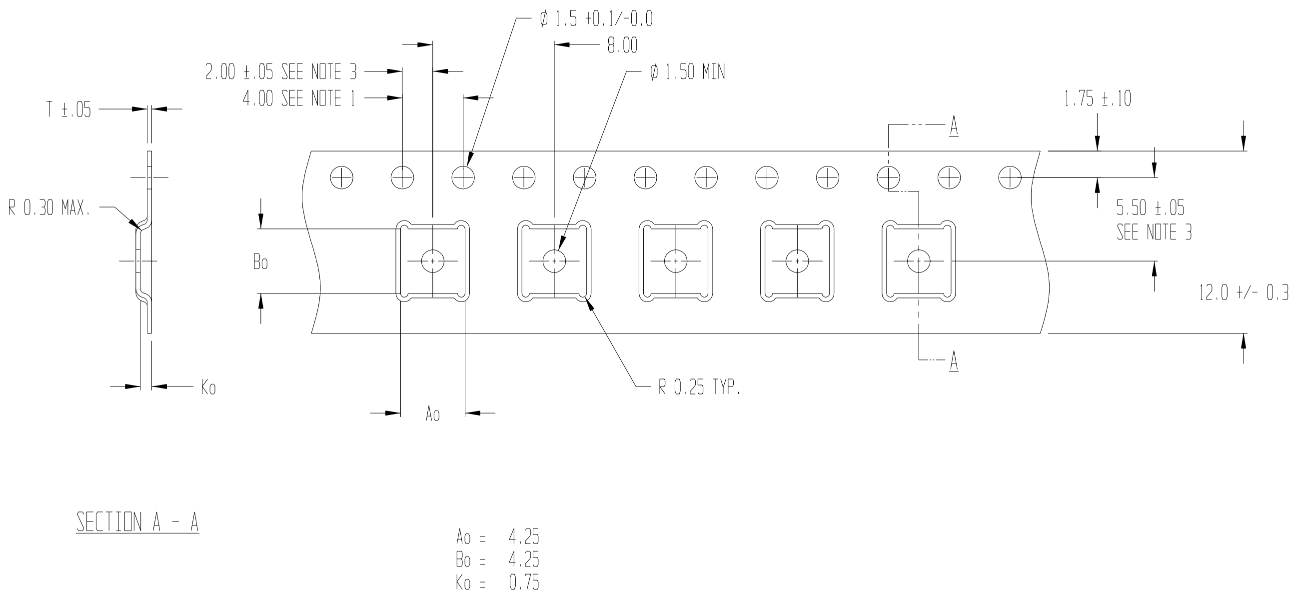
Part Number	Type
SLG47004-AP	24-pin TQFN

25.1 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Leader (min)		Trailer (min)		Tape Width (mm)	Part Pitch (mm)
			per Reel	per Box		Pockets	Length (mm)	Pockets	Length (mm)		
TQFN 24 4 mm x 4 mm 0.5P	24	4.0x4.0x0.75	6000	6000	330/102	42	336	42	336	12	8

25.2 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TQFN 24 4 mm x 4 mm 0.5P	4.25	4.25	0.75	4.00	8.00	1.50	1.75	5.50	12.00



Note 1: 10 sprocket hole pitch cumulative tolerance ±0.2.
Note 2: Camber in compliance with EIA 481.
Note 3: Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole.
Note 4: A0 and B0 are calculated on a plane at a distance “R” above the bottom of the pocket.
Note 5: Orientation in carrier: Pin1 is at upper left corner (Quadrant1).

Glossary

A

ACK	Acknowledge bit
ACMP	Analog Comparator
ACMPH	Analog Comparator High-speed
ACMPL	Analog Comparator Low Power
AS	Analog Switch

B

BG	Bandgap

C

CLK	Clock
CMI	Connection Matrix Input
CMO	Connection Matrix Output
CNT	Counter

D

DFF	D Flip-Flop
DI	Digital Input
DILV	Low Voltage Digital Input
DLY	Delay
DNL	Differential Non-Linearity
DR	Digital Rheostat

E

EC	Electrical Characteristics
ERSE	Erase Enable
ERSR	Erase Register
ESD	Electrostatic Discharge
EV	End Value

F

FSM	Finite State Machine

G

GPI	General Purpose Input
GPIO	General Purpose Input/Output
GPO	General Purpose Output

I

IN	Input
InAmp	Instrumentation Amplifier
INL	Integral Non-Linearity
IO	Input/Output

L

LPF	Low-Pass Filter
LSB	Least Significant Bit
LUT	Look Up Table
LV	Low Voltage

M

MSB	Most Significant Bit
MUX	Multiplexer

N

NPR	Non-Volatile Memory Read/Write/Erase Protection
nRST	Reset
NVM	Non-Volatile Memory

O

OA	Operational Amplifier
OD	Open-Drain
OE	Output Enable
Op Amp	Operational Amplifier
OSC	Oscillator
OTP	Multiple-Time-Programmable
OUT	Output

P

PD	Power-Down
PGen	Pattern Generator
POR	Power-On Reset
PP	Push-pull
PRL	Protect Lock Bit
PT	Programmable Trim
PWR	Power

P DLY Programmable Delay

R

RPR Register Read/Write Protection

RPRB Register Read/Write Protection Bit

RPRL Register Protection Read/Write/Erase Lock

R/W Read/Write

S

SCL I^2C Clock Input

SDA I^2C Data Input/Output

SLA Slave Address

SMT With Schmitt Trigger

SPST Single-pole/Single Throw

SV nSET Value

T

TS Temperature Sensor

V

Vref Voltage Reference

W

WOSMT Without Schmitt Trigger

WPB Write Protect Bit

WPR Write Protection Register

WPRE Write Protect Enable

WS Wake and Sleep Controller

Revision History

Revision	Date	Description
1.01	Oct 4, 2024	Corrected typos on graphs
1.00	Oct 2, 2024	Initial release

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.