PMIC with High PSRR, Low Noise, Multi-Output LDOs and Integrated Load Switches

General Description

SLG51002 contains eight compact and customizable low dropout regulators and is designed for high performance camera modules and other small multi-rail applications.

Key Features

- Input voltage range:
  - 1.7 V to 5.0 V (3 x HV LDO)
  - 1.7 V to 5.0 V (2 x HC LDO)
  - 0.8 V to 1.5 V (3 x LV LDO)
- Separate input supply and enable for flexible power configurations
- Output voltage range:
  - 1.2 V to 3.75 V (3 x HV LDO)
  - 1.2 V to 3.75 V (2 x HC LDO)
  - 0.5 V to 1.4 V (3 x LV LDO)
- Output current levels:
  - Up to 500 mA (3 x HV LDO)
  - Up to 500 mA (2 x HC LDO)
  - Up to 1000 mA (2 x LV LDO)
  - Up to 1300mA (1 x LV LDO)
- LDO_HC and LDO_LV channels have Bypass Mode
- PSRR of 83 dB at 1 kHz and 47 dB at 1 MHz (3 x HV LDO)
- Low output voltage noise of 152 µV (3 x HV LDO)
- Low dropout voltage of 10 mV per 100 mA of load (3 x LV LDO)
- Ultra-low R_{ON} load switches with low leakage and slew rate control for low V_{IN} supplies (3 x LV LDO)
- Tight output voltage accuracy of ±1 % over-temperature
- Low shutdown current of 300 nA
- Low quiescent current of 14 µA
- Seven Combination Function Macrocells
- Three Delay Macrocells
- One Multi-Function Macrocell
- User configurable settings via I^2C interface and OTP
  - Including output voltage, power sequencing, soft-start timing, and current limit threshold
- Soft start and soft shutdown
- Under-voltage lockout (UVLO)
- Thermal shutdown
- Configurable temperature alerts
- Wide -40 °C to +85 °C operating temperature
- 25-pin WLCSP: 1.992 mm x 1.992 mm x 0.440 mm, 0.35 mm pitch

Applications

- High End Camera Module Applications
- Smartphones
- Digital Cameras
- Smart Devices with Imaging

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1 Block Diagram

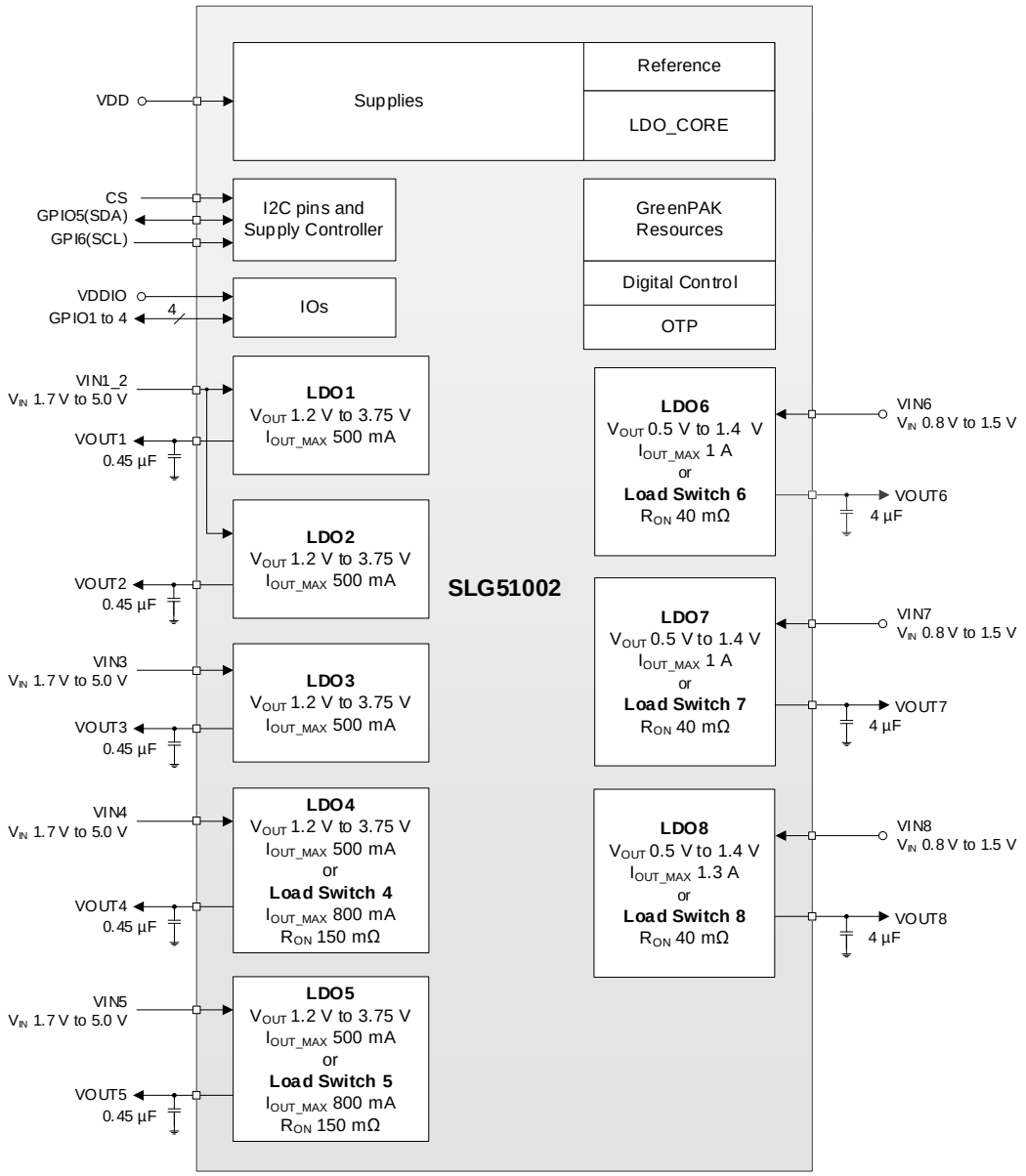


Figure 1: Block Diagram

2 Pinout

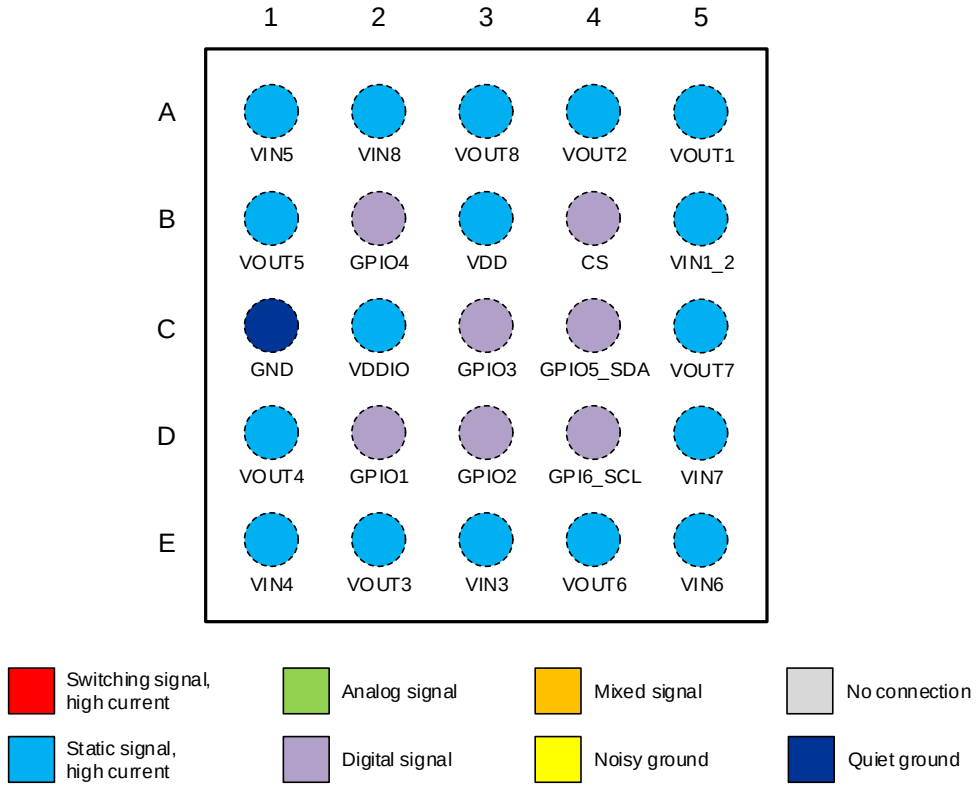


Figure 2: Pinout Diagram (Top View, Face Down)

Table 1: Pin Description

Pin No.	Pin Name	Signal Name	Function	Input Options	Output Options
	CS	CS	Chip select (CS).	--	--
	VDD	VDD	Supply voltage for overall chip control.	--	--
	GND	GND	Ground.	--	--
	VDDIO	VDDIO	Supply voltage for GPIO1-GPIO4	--	--
	GPIO1	GPIO1	High voltage General Purpose IO	Digital Input with/without Schmitt trigger, Low voltage digital input, Ultra-Low voltage digital input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
		I2C_SA1	I2C Slave address 1	--	--

Pin No.	Pin Name	Signal Name	Function	Input Options	Output Options
	GPIO2	GPIO2	High voltage General Purpose IO	Digital Input with/without Schmitt trigger, Low voltage digital input, Ultra-Low voltage digital input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
		I2C_SA2	I2C Slave address 2	--	--
	GPIO3	GPIO3	High voltage General Purpose IO	Digital Input with/without Schmitt trigger, Low voltage digital input, Ultra-Low voltage digital input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
		I2C_SA3	I2C Slave address 3	--	--
	GPIO4	GPIO4	High voltage General Purpose IO	Digital Input with/without Schmitt trigger, Low voltage digital input, Ultra-Low voltage digital input	Push-Pull, Open-Drain NMOS, Open-Drain PMOS
		I2C_SA4	I2C Slave address 4	--	--
	GPIO5	GPIO5	1.2 V/1.8 V input cell, Low voltage General Purpose IO	Digital Input	Open-Drain NMOS
		SDA	1.2 V/1.8 V input cell, I^2C Serial Data Line (SDA)	Digital Input	Open-Drain NMOS
	GPI6	GPI6	1.2 V/1.8 V input cell, Low voltage General purpose input	Digital Input	--
		SCL	1.2 V/1.8 V input cell, I^2C Serial Clock Line (SCL)	Digital Input	--
	VIN1_2	VIN1_2	Controller and power FET supply voltage for LDO1 and LDO2.	--	--
	VIN3	VIN3	Controller and power FET supply voltage for LDO3.	--	--
	VIN4	VIN4	Controller and power FET supply voltage for LDO4.	--	--
	VIN5	VIN5	Controller and power FET supply voltage for LDO5.	--	--

Pin No.	Pin Name	Signal Name	Function	Input Options	Output Options
	VIN6	VIN6	Controller and power FET supply voltage for LDO6.	--	--
	VIN7	VIN7	Controller and power FET supply voltage for LDO7.	--	--
	VIN8	VIN8	Controller and power FET supply voltage for LDO8.	--	--
	VOUT1	VOUT1	LDO1 power output.	--	--
	VOUT2	VOUT2	LDO2 power output.	--	--
	VOUT3	VOUT3	LDO3 power output.	--	--
	VOUT4	VOUT4	LDO4 power output.	--	--
	VOUT5	VOUT5	LDO5 power output.	--	--
	VOUT6	VOUT6	LDO6 power output.	--	--
	VOUT7	VOUT7	LDO7 power output.	--	--
	VOUT8	VOUT8	LDO8 power output.	--	--

Table 2: Pin Type Definition

Pin Type	Description	Pin Type	Description
GPI	General purpose input	GPIO	General purpose input/output
GPO	General purpose output	CS	Chip select
DIWST	Digital Input with Schmitt trigger	DIWOSH	Digital Input without Schmitt trigger
LVDI	Low voltage digital input	ULVDI	Ultra-Low voltage digital input
SDA	Serial data	PU	Pull-up resistor
SCL	Serial clock	PD	Pull-down resistor
PWR	Power	GND	Ground

2.1 Input Pins

2.1.1 CS – Chip Select

This active-high pin is used to wake SLG51002 from a low-power reset state.

To guarantee correct operation, CS must be de-asserted whenever the voltage at the VDD pin is out of the operating conditions boundary (that is VDD < 2.8 V, or VDD > 5.0 V).

When de-asserting the CS pin, it can have a programmable shutdown debounce time (from 0 µs to 256 µs, register CS_T_DEB).

When CS is de-asserted, all digital is forced to shut down, and any volatile memory is reset.

While CS pin is high, memory status can be checked with the MEM_STATUS bit. The MEM_STATUS bit is reset upon any UVLO, CS de-assert, POR event, Over-temperature detection, Power Sequencer Crash Request or Software Reset Request event, and is intended for user to write high when loading configurations via I2C, thus allowing user to check for any event that may affect integrity of the I2C written data.

2.1.2 SCL – I²C Clock

The SCL signal is the I²C clock.

2.2 Bidirectional Pins

2.2.1 GPIO1 to GPIO5 and GPI6 – General Purpose Input/Output

The general-purpose input/output pins are configurable by dedicated registers (IO_GPIO<x>_CONF). GPIO1 to GPIO5 can be configured as an input or an open-drain NMOS output. GPIO1 to GPIO4 also can be configured as a push pull output or open-drain PMOS output. GPI6 is always an input pin.

In the LOW IQ RESET state, GPIO1 to GPIO4 are configured as input with 1MOhm pull down resistor. GPIO5 and GPI6 are configured as inputs with no pull-up/pull-down resistor.

GPIO5 and GPI6 are low voltage pins. The user-configurable input levels for low voltage pins are 1.2 V and 1.8 V.

GPIO1 to GPIO4 are high voltage pins and are supplied by VDDIO for input and output modes. There are four input modes for GPIO1 to GPIO4 to get better input performance and cover voltage range from 1.2 V to 5 V:

- Digital input without Schmitt trigger (recommended operation input voltage range - 1.5 V to VDDIO)
- Digital input with Schmitt trigger (recommended operation input voltage range - 1.5 V to VDDIO)
- Low voltage digital input (recommended operation input voltage range - 1.5 V to VDDIO)
- Ultra-Low voltage digital input (recommended operation input voltage range - 1.2 V to 1.8V)

Digital input without Schmitt trigger, Digital input with Schmitt trigger and Low voltage digital input modes are intended for 1.5 V to VDDIO input voltage range. Ultra-Low voltage digital input mode is intended for 1.2 V to 1.8 V input voltage range, but this mode also can be used up to VDDIO voltage. The Ultra-Low voltage digital input mode has a fixed V_{IH} and V_{IL} thresholds, unlike other modes, which thresholds depends on VDDIO voltage.

2.2.2 SDA – I²C Data

The SDA signal is the I²C data signal. It is an open-drain signal so that either side can pull it down to a logic low level.

3 Characteristics

3.1 Absolute Maximum Ratings

Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, so functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specification are not implied. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Table 3: Absolute Maximum Ratings

Parameter	Description	Conditions	Min	Max	Unit
T_{STG}	Storage temperature	Non operational	-40	+150	°C
T_J	Junction temperature		-25	+125	°C
T_A	Ambient temperature		-40	+85	°C
V_{DD}	Power supply voltage on VDD pin		-0.3	+6.0	V
V_{DDIO}	Power supply voltage on VDDIO pin		-0.3	V_{DD}	V
	Power supply voltage on VIN1_2, VIN3, VIN4, VIN5, VOUT1, VOUT2, VOUT3, VOUT4, VOUT5 pins		-0.3	+6.0	V
	Power supply voltage on VIN6, VIN7, VIN8 pin		-0.3	+1.8	V
	Voltage on VOUT6, VOUT7, VOUT8 pin		-0.3	+1.65	V
V_{PIN}	Voltage on low voltage pins	GPIO5 and GPI6	-0.3	+1.98	V
	Voltage on high voltage pins	GPIO1 to GPIO4	-0.3	V_{DDIO} + 0.3	
		CS	-0.3	V_{DD} + 0.3	
	Voltage on LDO output pins		-0.3	V_{IN} + 0.3	
ESD	ESD Protection (Human Body Model)		2000		V
	ESD Protection (Charged Device Model)		500		V
$I_{MAX\_LDO\_LV}$	Maximum Average or DC Current through VIN6, VIN7, VIN8 or VOUT6, VOUT7, VOUT8 Pins	T_J = 100 °C		1.3	A
		T_J = 110 °C		0.938	

3.1.1 Guidelines for Reliable Operation

- Low Voltage Pins (GPIO5 and GPI6): take care that the low voltage pins do not exceed their Abs. Max. ratings, even briefly. Transients both positive (above max) and negative (below min) can cause EOS (Electrical Overstress) damage.
- Power sequencing: CS should be held low before VDD is powered up. CS pin should also be pulled low before VDD falls out of operating range. VIN supplies for LDO_HV, LDO_HC and LDO_LV channels can be safely biased even if VDD is not present. VIN supplies should be powered up before enabling their respective LDO channels. Low voltage pins (GPIO5 and GPI6) configured as inputs are

allowed to be forced high before VDD is powered up. All other GPIOs are not allowed to be forced high before VDD and VDDIO are powered up.

- Outputs of LDOs should not exceed their respective input voltages.
- Voltage at VDDIO should not exceed voltage at VDD. VDDIO and VDD can be tied together.

3.2 Recommended Operating Conditions

Table 4: Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_A	Ambient temperature		-40	+25	+85	°C
V_{DD}	Power supply voltage on VDD pin		2.8	3.8	5.0	V
V_{DDIO}	Power supply voltage on VDDIO pin		1.2		V_{DD}	V
	Power supply voltage on VIN1_2, VIN3, VIN4, VIN5 pins		1.7		5.0	V
	Power supply voltage on VIN6, VIN7, VIN8 pin	LDO Mode	0.8		1.5	V
	Power supply voltage on VIN6, VIN7, VIN8 pin	Load Switch Mode	0.5		1.4	V
	Voltage on low voltage pins	GPIO5 and GPI6	0		1.8	V
	Voltage on high voltage pins	GPIO1 to GPIO4	-0.3		V_{DDIO}	V
		CS	-0.3		V_{DD}	

3.3 Thermal Characteristics

Table 5: Package Ratings

Parameter	Description	Conditions	Min	Typ	Max	Unit
R_{Θ_JA}	Package thermal resistance	Junction to ambient JEDEC standard PCB		54.8		K/W

3.4 Current Consumption

Note: Current consumption electrical characteristics apply over the full operating temperature range.

Table 6: Current Consumption

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
I_{Q_SLEEP}	Current consumption in SLEEP. I_{Q_SLEEP} is the I_Q in LOW IQ RESET State	V_{IN} = 3.8 V All references disabled I^2C interface disabled All rails disabled VIN6, VIN7, VIN8 = 0 V		0.24		µA
$I_{Q\_READY\_DIS}$	Current consumption in READY State	V_{IN} = 3.8 V All references enabled I^2C interface enabled All rails disabled		14		µA
$I_{Q\_READY\_EN}$	Current consumption in READY State	V_{IN} = 3.8 V All references enabled I^2C interface enabled All rails enabled as LDO Mode, no load		120		µA

3.5 Chip Select Digital I/O Characteristics

Digital I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1.

Table 7: High-Voltage Digital I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
V_{IH}	CS input high voltage		0.9		VDD	V
V_{IL}	CS input low voltage		0		0.2	V
I_{LKG}	CS input leakage current	CS < 2V			1	µA
t_{ON_READY}	Turn-on time from CS HIGH to Ready State				10	ms

3.6 Digital I/O Characteristics

I/O electrical characteristics apply over the full operating temperature range, see Section 3.1.1.

Table 8: I/O Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
GPIO1 to GPIO4						
V_{IH}	HIGH-Level Input Voltage	Digital input without Schmitt trigger mode	0.7*VDDIO		VDDIO+0.3	V
		Digital input with Schmitt trigger mode	0.8*VDDIO		VDDIO+0.3	
		Low voltage digital input mode	1.25		VDDIO+0.3	
		Ultra-Low voltage digital input mode	1.05		VDDIO+0.3	
V_{IL}	LOW-Level Input Voltage	Digital input without Schmitt trigger mode	GND-0.3		0.3*VDDIO	V
		Digital input with Schmitt trigger mode	GND-0.3		0.2*VDDIO	
		Low voltage digital input mode	GND-0.3		0.5	
		Ultra-Low voltage digital input mode	GND-0.3		0.45	
V_{OH}	HIGH-Level Output Voltage	Push-Pull, PMOS OD, I_{OH} = 100 µA, VDD = 2.8V, VDDIO = 1.2 V	1.18			V
		Push-Pull, PMOS OD, I_{OH} = 100 µA, VDD = 2.8V, VDDIO = 1.8 V	1.6			
		Push-Pull, PMOD OD, I_{OH} = 1 mA, VDD = 2.8V, VDDIO = 2.8 V	2.71			
		Push-Pull, PMOS OD, I_{OH} = 3 mA, VDD = 3.8V, VDDIO = 3.8 V	3.17			
		Push-Pull, PMOS OD, I_{OH} = 5 mA, VDD = 5.0V, VDDIO = 5.0 V	4.19			

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull, I_{OL} = 100 µA, VDD = 2.8V, VDDIO = 1.2 V			0.005	V
		Push-Pull, I_{OL} = 100 µA, VDD = 2.8V, VDDIO = 1.8 V			0.005	
		Push-Pull, I_{OL} = 1 mA, VDD = 2.8V, VDDIO = 2.8 V			0.05	
		Push-Pull, I_{OL} = 3 mA, VDD = 3.8V, VDDIO = 3.8 V			0.13	
		Push-Pull, I_{OL} = 5 mA, VDD = 5.0V, VDDIO = 5.0 V			0.18	
		NMOS OD, I_{OL} = 100 µA , VDD = 2.8V, VDDIO = 1.2 V			0.004	
		NMOS OD, I_{OL} = 100 µA , VDD = 2.8V, VDDIO = 1.8 V			0.004	
		NMOS OD, I_{OL} = 1 mA , VDD = 2.8V, VDDIO = 2.8 V			0.04	
		NMOS OD, I_{OL} = 3 mA , VDD = 3.8V, VDDIO = 3.8 V			0.1	
		NMOS OD, I_{OL} = 5 mA, VDD = 5.0V, VDDIO = 5.0 V			0.13	
I_{OH}	HIGH-Level Output Current	Push-Pull, PMOS OD, V_{OH} = V_{DDIO}-0.2 V, VDD = 2.8V, VDDIO = 1.2 V	1.15			mA
		Push-Pull, PMOS OD, V_{OH} = V_{DDIO}-0.2 V, VDD = 2.8V, VDDIO = 1.8 V	1			
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, VDD = 2.8V, VDDIO = 2.8 V	4.5			
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, VDD = 3.8V, VDDIO = 3.8 V	11.3			
		Push-Pull, PMOS OD, V_{OH} = 2.4 V, VDD = 5.0V, VDDIO = 5.0 V	25.1			
I_{OL}	LOW-Level Output Current	Push-Pull, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 1.2 V	3.48			mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
		Push-Pull, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 1.8 V	3.48			
		Push-Pull, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 2.8 V	3.48			
		Push-Pull, V_{OL} = 0.4 V, VDD = 3.8V, VDDIO = 3.8 V	10.03			
		Push-Pull, V_{OL} = 0.4 V, VDD = 5.0V, VDDIO = 5.0 V	11.4			
		NMOS, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 1.2 V	4.64			
		NMOS, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 1.8 V	4.64			
		NMOS, V_{OL} = 0.15 V, VDD = 2.8V, VDDIO = 2.8 V	4.64			
		NMOS, V_{OL} = 0.4 V, VDD = 3.8V, VDDIO = 3.8 V	13.4			
		NMOS, V_{OL} = 0.4 V, VDD = 5.0V, VDDIO = 5.0 V	15.2			
R_{PULL}	Pull-up or Pull-down Resistance	1 M for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = VDDIO		1		MΩ
		100 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = VDDIO		100		kΩ
		10 k for Pull-up: V_{IN} = GND; for Pull-down: V_{IN} = VDDIO		10		kΩ
I_{LKG}	Input leakage				500	nA
C_{IN}	Input Capacitance			4		pF
SDA, SCL, GPIO5 and GPI6						
V_{IH}	HIGH-Level Input Voltage		0.4*V DDLV		0.7*V DDLV	V
V_{IL}	LOW-Level Input Voltage		0.3*V DDLV		0.6*V DDLV	V
V_{HYS}	Schmitt trigger hysteresis		0.1*V DDLV			V
V_{OL}	Output low voltage SDA, GPIO5	IOUT ≤ IOL	0		0.3	V

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{OL}	Output current	VOL = 0.3 V	20			mA
I_{LKG}	Input leakage				500	nA
C_{IN}	Pin capacitance				10	pF

Note 1 VDDLV defines voltage thresholds for low voltage pins and can be selected 1.2 V or 1.8 V.

Table 9: Typical Delay Estimated for GPIO at T = 25 C. If VDDIO is not defined, VDDIO is same with VDD.

Symbol	Parameter	Note	VDD = 2.8 V		VDD = 3.8 V		VDD = 5 V		Unit
			rising	falling	rising	falling	rising	falling	
GPIO1 to GPIO4									
tpd	Delay	Digital Input without Schmitt Trigger to PP	17	16	15	13	14	12	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP	17	16	15	13	14	12	ns
tpd	Delay	Low Voltage Digital Input to PP	34	149	41	67	52	38	Ns
tpd	Delay	Ultra-Low Voltage Digital Input to PP (VDDIO=1.2V)	29	32	28	30	28	29	ns
tpd	Delay	Ultra-Low Voltage Digital Input to PP (VDDIO=1.8V)	30	32	28	30	28	29	ns
tpd	Delay	Digital Input without Schmitt Trigger to NMOS OD	-	16	-	13	-	12	ns
tpd	Delay	Digital Input without Schmitt Trigger to PMOS OD	17	-	15	-	14	-	ns

3.7 LDO_HV Characteristics

The characteristics for the LDOs in Load Switch Mode are given in Section 3.7.1.

Table 10: LDO_HV (LDO1, 2 and 3) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		1.7	3.8	5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	0.45	2.2	20	µF
I_{OUT_MAX}	Maximum output current	V_{OUT} drops 50 mV Note 1	500			mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable Conditions						
V_{OUT}	Selectable output voltage		1.2	3.3	3.75	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			10		mV
SR	Slew rate, programmable to (1, 2.5, 5, 7.5, 10, 12.5, 25, 50, 100) mV/us Note 2	VOUT = VOUT (Typ)	1		100	mV/µs
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 12 mA steps Note 3	At 90 % V_{OUT}	30	150	606	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 12 mA steps Note 3		30	550	606	mA
R_{PD_OFF}	Output pull down resistance, programable to (38, 43, 50, 60, 75, 100, 150, 300) Ohm	VOUT = 0.5 V LDO disabled	38		300	Ω
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 4	IOUT = 1 mA TA = 25 °C	-10 Note 5		10 Note 5	mV
V_{OUT_TEMP}	Temperature dependence of VOUT Note 4	IOUT = 1 mA Note 6	-0.65		0.65	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 4	IOUT = 1 mA VIN = VOUT + VDROPOUT (Max) to VIN (Max)	-2		2	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 4	1 mA < IOUT < IOUT_MAX LDO1,2	-7		3	mV
		1 mA < IOUT < IOUT_MAX LDO3	-8		3	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{DROPOUT}$	Dropout voltage LDO1, 2	@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 230 mA VIN > 1.8 V			200 Note 7	mV
		@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 300mA VIN > 1.9 V			240 Note 7	
		@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 300mA VIN > 3 V			120 Note 7	
	Dropout voltage LDO3	@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 250mA VIN > 1.8 V			180 Note 7	
		@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 300mA VIN > 1.9 V			190 Note 7	
		@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 300mA VIN > 3 V			90 Note 7	
$R_{PD\_OFF\_ACC}$	Output pull down resistance accuracy	VOUT = 0.5 V LDO disabled		30		%
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	VIN = VOUT + VDROPOUT (Max) + 0.6 V to VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = IOUT_MAX tR = tF = 100 mV/µs		2	5 Note 8	mV
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = 1 mA to IOUT_MAX/2 tR = tF = 1 µs		28	37	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
t_{ON}	Turn-on time	Time to 90 % of VOUT IOUT = 0 mA Note 9		0.15		ms
t_{OFF}	Turn-off time	Time to 10 % of VOUT IOUT = 0 mA R_{PD_OFF}=100Ohm		0.8		ms
AC Parameters						
$PSRR_{1kHz}$	Power supply rejection ratio LDO1,2	f = 1 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2		77		dB
	Power supply rejection ratio LDO3	f = 1 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2		73		dB
$PSRR_{100kHz}$	Power supply rejection ratio LDO1,2	f = 100 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		58		dB
	Power supply rejection ratio LDO3	f = 100 kHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		65		dB
$PSRR_{1MHz}$	Power supply rejection ratio	f = 1 MHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		48		dB
$PSRR_{2MHz}$	Power supply rejection ratio	f = 2 MHz VIN = VOUT + 500 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF Note 12		59		dB

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_N	Output noise	f = 10 Hz to 100 kHz IOUT = IOUT_MAX/2		152		µV
Current Sink						
I_{OV_SINK}	Current sink at over-voltage	VOV = VOUT + 100 mV Note 10	10	77		mA
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current	IOUT = 0 mA VDD = VIN = 3.8 V Note 11		13	19	µA
$I_{Q\_ON\_1mA}$	Quiescent current LDO1, 2	IOUT = 1 mA Note 11		36	48	µA
	Quiescent current LDO3	IOUT = 1 mA Note 11		44	56	
$I_{Q\_ON\_IMAX}$	Quiescent current LDO1, 2	IOUT = IOUT_MAX Note 11		1.7	3.5	mA
	Quiescent current LDO3	IOUT = IOUT_MAX Note 11		2	3.7	mA

Note 1 Guaranteed for LDO1 and LDO2 for V_{IN} > 2.1 V. Between V_{IN} of 1.7 V to 2.1 V, the I_{OUT_MAX} guaranteed is 200 mA. Guaranteed for LDO3 for V_{IN} > 2.1 V. Between V_{IN} of 1.7 V to 2.1 V, the I_{OUT_MAX} guaranteed is 300 mA.

Note 2 Slew rate ≥ 25mV/us is guaranteed for Cout ≤ 4.7uF

Note 3 Accuracy ±30%, IOUT_LIM > 100 mA

Note 4 The overall accuracy can be calculated by summing V_{OUT_PP} + V_{OUT_TEMP} + $V_{OUT\_STATIC\_LD}$ + $V_{OUT\_STATIC\_LINE}$.

Note 5 +10 mV / -10 mV accuracy applies to factory-trimmed VOUT values targeted between 1.23 V to 3.72 V. VOUT targets from 1.20 V to 1.22 V can be trimmed to +24 mV/ -10 mV accuracy. VOUT targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy

Note 6 Guaranteed for V_{IN} ≥ 2.5 V.

Note 7 Dropout voltage is linear for the same VIN voltage with the load current, if using a lower I_{OUT_MAX} than specified.

Note 8 Guaranteed for V_{IN} > 2.1 V. Otherwise, maximum line transient is 20 mV.

Note 9 For slew rate set at 100 mV/us, V_{OUT} = 3.3 V

Note 10 Guaranteed for V_{IN} > 2.35 V.

Note 11 Internal regulator current flowing to ground.

Note 12 Strongly related to trace parasitic inductance, COUT & ESL

3.8 LDO_HC Characteristics

The characteristics for the LDOs in Load Switch Mode are given in Section 3.9.1.

Table 11: LDO_HC (LDO4 and 5) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		1.7	3.8	5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	0.45	2.2	20	µF
I_{OUT_MAX}	Maximum output current	VOUT drops 50 mV Note 1	500			mA
Programmable Conditions						
V_{OUT}	Selectable output voltage		1.2	3.3	3.75	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			10		mV
SR	Slew rate, programmable to (1, 2.5, 5, 7.5, 10, 12.5, 25, 50, 100) mV/us Note 2	VOUT = VOUT (Typ)	1		100	mV/µs
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 12 mA steps Note 3	At 90 % VOUT	30	550	970	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 12 mA steps Note 3		30	550	970	mA
R_{PD_OFF}	Output pull down resistance, programable to (38, 43, 50, 60, 75, 100, 150, 300) Ohm	VOUT = 0.5 V LDO disabled	38		300	Ω
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 4	IOUT = 1 mA TA = 25 °C	-10 Note 5		10 Note 5	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
V_{OUT_TEMP}	Temperature dependence of VOUT Note 4	IOUT = 1 mA Note 6	-0.65		0.65	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 4	IOUT = 1 mA VIN = VOUT + VDROPOUT (Max) to VIN (Max)		3		mV
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 4	1 mA < IOUT < IOUT_MAX	-8		3	mV
$V_{DROPOUT}$	Dropout voltage	@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = IOUT_MAX Note 7			130	mV
$R_{PD\_OFF\_ACC}$	Output pull down resistance accuracy	VOUT = 0.5 V LDO disabled		30		%
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	VIN = VOUT + VDROPOUT (Max) + 0.6 V to VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = IOUT_MAX tR = tF = 100 mV/µs		6		mV
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = 1 mA to IOUT_MAX/2 tR = tF = 1 µs		30		mV
t_{ON}	Turn-on time	Time to 90 % of VOUT IOUT = 0 mA Note 8		0.15		ms
t_{OFF}	Turn-off time	Time to 10 % of VOUT IOUT = 0 mA R_{PD_OFF}=100Ohm		0.8		ms

Parameter	Description	Conditions	Min	Typ	Max	Unit
AC Parameters						
$PSRR1_{KHZ}$	Power supply rejection ratio	f = 1 kHz VIN = VOUT + 300 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		69		dB
$PSRR_{100kHz}$	Power supply rejection ratio	f = 100 kHz VIN = VOUT + 300 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		50		dB
$PSRR_{1MHz}$	Power supply rejection ratio	f = 1 MHz VIN = VOUT + 300 mV VOUT = VOUT (Typ) IOUT = IOUT_MAX/2 C_{OUT} = 4.7 µF		46		dB
V_N	Output noise	f = 10 Hz to 100 kHz IOUT = IOUT_MAX/2		152		µV
Current Limit Accuracy						
I_{OV_SINK}	Current sink at over-voltage	VOV = VOUT + 100 mV Note 9	10	77		mA
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current	IOUT = 0 mA, VDD = VIN = 3.8 V Note 10		19	25	µA
$I_{Q\_ON\_1mA}$	Quiescent current	IOUT = 1 mA VDD=VIN=3.8V Note 10		73	95	µA
$I_{Q\_ON\_IMAX}$	Quiescent current	IOUT = IOUT_MAX Note 10		5		mA

Note 1 Guaranteed for VIN > 2.1 V, between 1.7 V and 2.1 V the IOUT_MAX guaranteed is 200 mA.

Note 2 Slew rate ≥ 25mV/us is guaranteed for Cout ≤ 4.7uF

Note 3 Accuracy ±30%, IOUT_LIM > 100 mA

Note 4 The overall accuracy can be calculated by summing VOUT_PP + VOUT_TEMP + VOUT_STATIC_LD + VOUT_STATIC_LINE.

Note 5 +10 mV / -10 mV accuracy applies to factory-trimmed VOUT values targeted between 1.23 V to 3.72 V. VOUT targets from 1.20 V to 1.22 V can be trimmed to +24 mV/ -10 mV accuracy. VOUT targets from 3.73 V to 3.75 V can be trimmed to +10 mV / -30 mV accuracy

Note 6 Guaranteed for VIN > 1.7 V.

Note 7 Guaranteed for $V_{OUT} \geq 2.8$ V.

Note 8 For slew rate set at 100 mV/us, V_{OUT} = 3.3 V

Note 9 Guaranteed for VIN > 2.35 V.

Note 10 Internal regulator current flowing to ground.

3.8.1 Load Switch Mode Characteristics

Table 12: Load Switch Mode Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		1.7		5	V
I_{OUT_MAX}	Maximum output current		800			mA
Programmable Conditions						
I_{LIM}	Current limit, programmable from 30 mA to 970 mA in 12 mA steps		30	880	970	mA
Electrical Performance						
R_{ON}	On resistance	VOUT = 2.8V		150		mΩ
I_{LIM_ACC}	Current limit accuracy		-35		35	%

3.9 LDO_LV Characteristics

The characteristics for the LDOs in Load Switch Mode are given in Section 3.9.1

Table 13: LDO_LV (LDO6, 7 and 8) Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input supply (pass device + part of controller)		0.8	1.25	1.5	V
C_{OUT}	Output capacitance	Effective capacitance after derating	4 Note 1	20	80	µF
ESL_{COUT}	Output capacitor series inductance	f > 100 kHz			1	nH
I_{OUT_MAX}	Maximum output current LDO6, 7	VOUT drops 50 mV	1000 Note 2			mA
	Maximum output current LDO8	VOUT drops 50 mV	1300 Note 2			
Programmable Conditions						
V_{OUT}	Selectable output voltage		0.5 Note 3	1.175	1.4	V
V_{OUT_LSB}	LSB of output voltage programming DAC (8-bit control)			5		mV
SR	Slew rate, programmable to (1, 2.5, 5, 7.5, 10, 12.5, 25, 50, 100) mV/us Note 4	VOUT = VOUT (Typ)	1		100	mV/µs
$I_{OUT\_STARTUP\_LIM}$	Start-up current limit, programmable in 29.2 mA steps LDO6, 7 Note 5	At 90 % VOUT	29.2	321.2	1430.8	mA
	Start-up current limit, programmable in 29.2 mA steps LDO8 Note 5	At 90 % VOUT	29.2	321.2	1693.6	mA
$I_{OUT\_FUNC\_LIM}$	Functional current limit, programmable in 29.2 mA steps LDO6, 7 Note 5		29.2	1255.6	1430.8	mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
	Functional current limit, programmable in 29.2 mA steps LDO8 Note 5		29.2	1255.6	1693.6	mA
R_{PD_OFF}	Output pull down resistance, programable to (38, 43, 50, 60, 75, 100, 150, 300) Ohm	VOUT = 0.5 V LDO disabled	38		300	Ω
Electrical Performance						
Static Parameters						
V_{OUT_PP}	Part to part output voltage accuracy Note 6	IOUT = 1 mA TA = 25 °C	-5		5	mV
V_{OUT_TEMP}	Temperature dependence of VOUT Note 6	IOUT = 1 mA	-1.1		1.1	%
$V_{OUT\_STATIC\_LINE}$	Static line regulation Note 6	IOUT = 1 mA VIN = VOUT + VDROPOUT (Max) to VIN (Max)	-2		2	mV
$V_{OUT\_STATIC\_LD}$	Static load regulation Note 6	1 mA < IOUT < 1A I_{LOAD} = 0.8 A, VIN - VOUT = ~100 mV	-8		2	mV
$V_{DROPOUT}$	Dropout voltage LDO6, 7	@ VOUT = VOUT (VIN (Max)) - 10 mV IOUT = 1A			100 Note 7	mV
	Dropout voltage LDO8	@ VOUT = VOUT (VIN (Max)) - 10 mV for VOUT < 1.37V IOUT = 1.3A			130 Note 7	mV
$R_{PD\_OFF\_ACC}$	Output pull down resistance accuracy	VOUT = 0.5 V LDO disabled		30		%
Dynamic Parameters						
$V_{OUT\_TR\_LINE}$	Line transient response	VIN = VOUT + VDROPOUT (Max) + 100 mV to VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = 1A tR = tF = 100 mV/µs		2	5	mV

Parameter	Description	Conditions	Min	Typ	Max	Unit
$V_{OUT\_TR\_LD\_1mA}$	Load transient response	VIN = VOUT + VDROPOUT (Max) VOUT = VOUT (Typ) IOUT = 1 mA to 500mA tR = tF = 1 µs		21	29	mV
t_{ON}	Turn-on time	Time to 90 % of VOUT IOUT = 0 mA COUT = 20 µF Note 8		0.2		ms
t_{OFF}	Turn-off time	Time to 10 % of VOUT IOUT = 0 mA COUT = 20 µF R_{PD_OFF}=100Ohm		4.7		ms
AC Parameters						
$PSRR_{1kHz}$	Power supply rejection ratio	f = 1 kHz VIN = VOUT + VDROPOUT (Max) + 200 mV VOUT = VOUT (Typ) IOUT = 500mA C_{OUT} = 20 µF		68		dB
$PSRR_{100kHz}$	Power supply rejection ratio	f = 100 kHz VIN = VOUT + VDROPOUT (Max) + 200 mV VOUT = VOUT (Typ) IOUT = 500mA C_{OUT} = 20 µF		52		dB
$PSRR_{1MHz}$	Power supply rejection ratio	f = 1 MHz VIN = VOUT + VDROPOUT (Max) + 200 mV VOUT = VOUT (Typ) IOUT = 500mA C_{OUT} = 20 µF		68		dB
V_N	Output noise	f = 10 Hz to 100 kHz IOUT = 500mA		100		µV
Current Limit Accuracy						
I_{OV_SINK}	Current sink at over-voltage	VOV = VOUT + 100 mV	10			mA

Parameter	Description	Conditions	Min	Typ	Max	Unit
Quiescent Current Specifications						
$I_{Q\_ON\_0mA}$	Quiescent current, no load	IOUT = 0 mA Note 9		8	15	µA
$I_{Q\_ON\_1mA}$	Quiescent current, low load	IOUT = 1 mA Note 9		10	16	µA
$I_{Q\_ON\_IMAX}$	Quiescent current, IOUT_MAX	IOUT = 1000 mA Note 9		0.42	1.5	mA

Note 1 For currents less than 400 mA, a minimum of 1.2 µF (after derating) can be used.

Note 2 For I_{OUT_MAX}, see $I_{MAX\_LDO\_LV}$ Absolute Maximum Ratings table.

Note 3 Output is capable down to 0.4 V at reduced accuracy. Please contact Renesas Electronics Corporation for more information

Note 4 Slew rate ≥ 50mV/us is guaranteed for Cout ≤ 10uF

Note 5 Accuracy -42% … +50%, IOUT_LIM > 100 mA

Note 6 The overall accuracy can be calculated by summing VOUT_PP + VOUT_TEMP + VOUT_STATIC_LD + VOUT_STATIC_LINE.

Note 7 Dropout voltage is linear with the load current. If using a lower IOUT_MAX than specified, the dropout can be calculated using 10 mV per 100 mA of load.

Note 8 For slew rate set at 100 mV/us, V_{OUT} = 1.175 V

Note 9 Internal regulator current flowing to ground.

3.9.1 Load Switch Mode Characteristics

Table 14: Load Switch Mode Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
External Electrical Conditions						
V_{IN}	Input voltage		0.5 Note 1	1.25	1.4	V
I_{OUT_MAX}	Maximum output current LDO6, 7		1000			mA
	Maximum output current LDO8		1300			mA
Programmable Conditions						
SR	Slew rate, programmable to (4, 6, 8, 10) mV/µs		4		10	mV/µs

Parameter	Description	Conditions	Min	Typ	Max	Unit
I_{LIM}	Current limit, programmable from 29.2 mA to 1.14308 A in 29.2 mA steps LDO6, 7 Note 2		29.2	1255.6	1430.8	mA
	Current limit, programmable from 29.2 mA to 1.6936 A in 29.2 mA steps LDO8 Note 2		29.2	1255.6	1693.6	mA
Electrical Performance						
R_{ON}	On resistance			40		mΩ
SR_{ACC}	Slew rate accuracy		-35		35	%
I_{LIM_ACC}	Current limit accuracy		-35		35	%
I_{Q_OFF}	Quiescent current in off mode	TA = 25 °C			2	µA

Note 1 Register bit SEL_BYP_VGATE must be set to 0 for VIN between 0.5 V and 0.8 V, and is recommended to be set to 1 for VIN between 0.8 V and 1.25 V.

Note 2 Current limit is guaranteed for VIN > 0.7 V. Below 0.7 V, a functional current limit is not guaranteed.

3.10 VREF, IREF, Temperature Supervision Characteristics

Table 15: VREF, IREF, Temperature Supervision Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable Conditions						
V_{REF}	Reference voltage	Internal VREF		1.2		V
T_{WARN}	Warning temperature threshold, programmable to (90, 100, 110, 120) °C		90		120	°C
T_{WARN_HYS}	Warning temperature hysteresis, programmable to (0, 14) °C			14		°C
Electrical Performance						
V_{REF_ACC}	Reference voltage accuracy	Internal VREF	-1		1	%
T_{OT}	Thermal shutdown over-temperature		125	140	155	°C

Parameter	Description	Conditions	Min	Typ	Max	Unit
T_{WARN_ACC}	Warning temperature threshold accuracy		-5		5	°C

3.11 Internal Oscillator Characteristics

Table 16: Internal Oscillator Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Electrical Performance						
f_{CLK}	Internal clock frequency		7.2	8	8.8	MHz

3.12 UVLO Characteristics

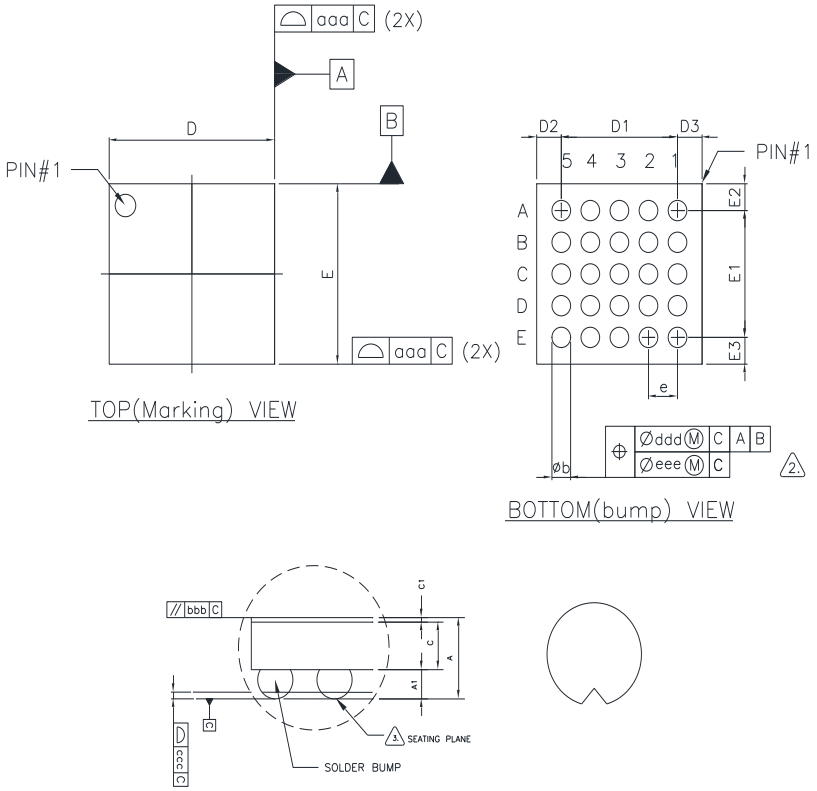
Table 17: UVLO Electrical Characteristics

Parameter	Description	Conditions	Min	Typ	Max	Unit
Programmable Conditions						
VDD_UVLO_LWR	Under-voltage lower threshold (falling edge), programmable in 24.6 mV steps Note 1		2.215		2.658	V
VDD_UVLO_UPPER	Under-voltage upper threshold (rising edge)			VDD_UVLO_LWR + 3 %		V
Electrical Performance						
VDD_POR_UPPER	Deep discharge lockout upper threshold			2.1	2.2	V
VDD_POR_LWR	Deep discharge lockout lower threshold			1.9		V
VDD_UVLO_STAT_ACC	Under-voltage lower threshold static accuracy with flip gate bandgap reference		-1.5		1.5	%

Note 1 This voltage is programmed from OTP in 24.6 mV steps.

4 Package Information

4.1 Package Outlines



Symbol	Dimension in mm			Dimension in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4100	0.4400	0.4700	0.0161	0.0173	0.0185
A1	0.1500	0.1650	0.1800	0.0059	0.0065	0.0071
c	0.2250	0.2500	0.2750	0.0089	0.0098	0.0108
c1	0.0220	0.0250	0.0280	0.0009	0.0010	0.0011
D	1.9670	1.9920	2.0170	0.0774	0.0784	0.0794
E	1.9670	1.9920	2.0170	0.0774	0.0784	0.0794
b	0.1950	0.2250	0.2550	0.0077	0.0089	0.0100
D1	---	1.4000	---	---	0.0551	---
D2	---	0.2960	---	---	0.0117	---
D3	---	0.2960	---	---	0.0117	---
E1	---	1.4000	---	---	0.0551	---
E2	---	0.2960	---	---	0.0117	---
E3	---	0.2960	---	---	0.0117	---
e	---	0.3500	---	---	0.0138	---
aaa	---	0.025	---	---	0.001	---
bbb	---	0.060	---	---	0.002	---
ccc	---	0.030	---	---	0.001	---
ddd	---	0.050	---	---	0.002	---
eee	---	0.050	---	---	0.002	---

Figure 3: Package Outline Drawing

4.2 Moisture Sensitivity Level

The Moisture Sensitivity Level (MSL) is an indicator for the maximum allowable time period (floor lifetime) in which a moisture sensitive plastic device, once removed from the dry bag, can be exposed to an environment with a specified maximum temperature and a maximum relative humidity before the solder reflow process. The MSL classification is defined in

Table 18.

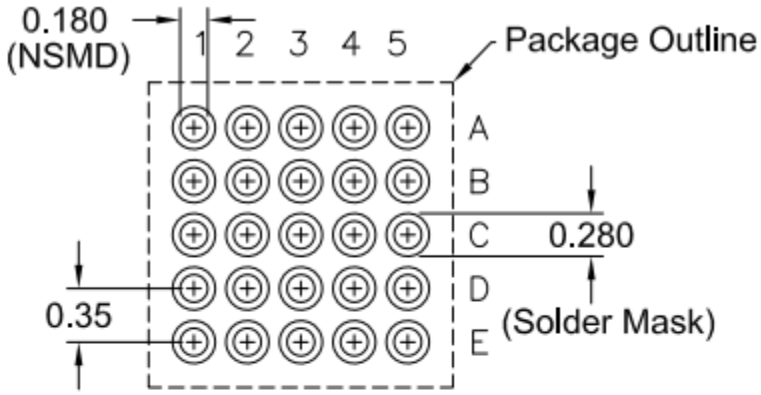
For detailed information on MSL levels refer to the IPC/JEDEC standard J-STD-020, which can be downloaded from http://www.jedec.org.

MSL rating does not apply to this device as it is not plastic encapsulated.

Table 18: MSL Classification

MSL Level	Floor Lifetime	Conditions
MSL 4	72 hours	30 °C / 60 % RH
MSL 3	168 hours	30 °C / 60 % RH
MSL 2A	4 weeks	30 °C / 60 % RH
MSL 2	1 year	30 °C / 60 % RH
MSL 1	Unlimited	30 °C / 85 % RH

4.3 Recommended Landing Pattern



RECOMMENDED LAND PATTERN
(PCB Top View, NSMD Design)

NOTES:

1. JEDEC compatible.
2. All dimensions are in mm and angles are in degrees.
3. Use ±0.05 mm for the non-toleranced dimensions.
4. Numbers in ( ) are for references only.
5. Pre-reflow solder ball diameter is Ø0.21 mm.
6. UBM diameter is Ø0.2 mm.

Figure 4: Recommended Landing Pattern

4.4 WLCSP Handling

Manual handling of WLCSP packages should be reduced to the absolute minimum. In cases where it is still necessary, a vacuum pick-up tool should be used. In extreme cases plastic tweezers could be used, but metal tweezers are not acceptable, since contact may easily damage the silicon chip.

Removal of a WLCSP package will cause damage to the solder balls. Therefore a removed sample cannot be reused.

WLCSP packages are sensitive to visible and infrared light. Precautions should be taken to properly shield the chip in the final product.

4.5 Soldering Information

Refer to the IPC/JEDEC standard J-STD-020 for relevant soldering information. This document can be downloaded from http://www.jedec.org.

5 Ordering Information

The ordering number consists of the part number followed by a suffix indicating the packing method. For details and availability, please consult Renesas Electronics Corporation or your local sales representative.

Table 19: Ordering Information

Part Number	Package	Size (mm)	Shipment Form	Pack Quantity
SLG51002C	WLCSP-25	1.992x1.992	T & R	

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