# A 13 mΩ, 5 A, Load Switch with Soft-start, Protection Features, and MOSFET Current Monitor Output

## General Description

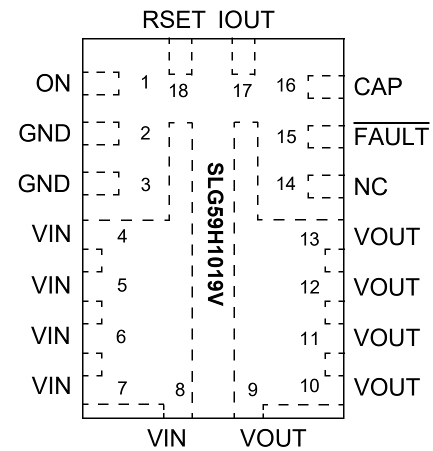
The SLG59H1019V is a high-performance 13 mΩ NMOS load switch designed to control 4.5 V to 25.2 V power rails up to 5 A. Using a proprietary MOSFET design, the SLG59H1019V achieves a stable 13 mΩ $RDS_{ON}$ across a wide input voltage range. In combining novel FET design and copper pillar interconnects, the SLG59H1019V package also exhibits a low thermal resistance for high-current operation.

Designed to operate over a -40 °C to 85 °C range, the SLG59H1019V is available in a low thermal resistance, RoHS-compliant, 1.6 x 3.0 mm STQFN package.

## Features

- Wide Operating Input Voltage: 4.5 V to 25.2 V
- Maximum Continuous Current: 5 A
  - Automatic nFET SOA Protection
- 10 W SOA Protection Threshold
- High-performance MOSFET Switch
  - Low $RDS_{ON}$: 13 mΩ at $V_{IN}$ = 25.2 V
  - Low $\Delta RDS_{ON}/\Delta V_{IN}$: <0.05 mΩ/V
  - Low $\Delta RDS_{ON}/\Delta T$: <0.06 mΩ/°C
- Capacitor-adjustable Inrush Current Control
- Two stage Current Limit Protection:
  - Resistor-adjustable Active Current Limit
  - Internal Short-circuit Current limit
- Open Drain FAULT Signaling
- MOSFET Current Analog Output Monitor: 10 µA/A
- Fast 0.75 kΩ Output Discharge
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

## Pin Configuration

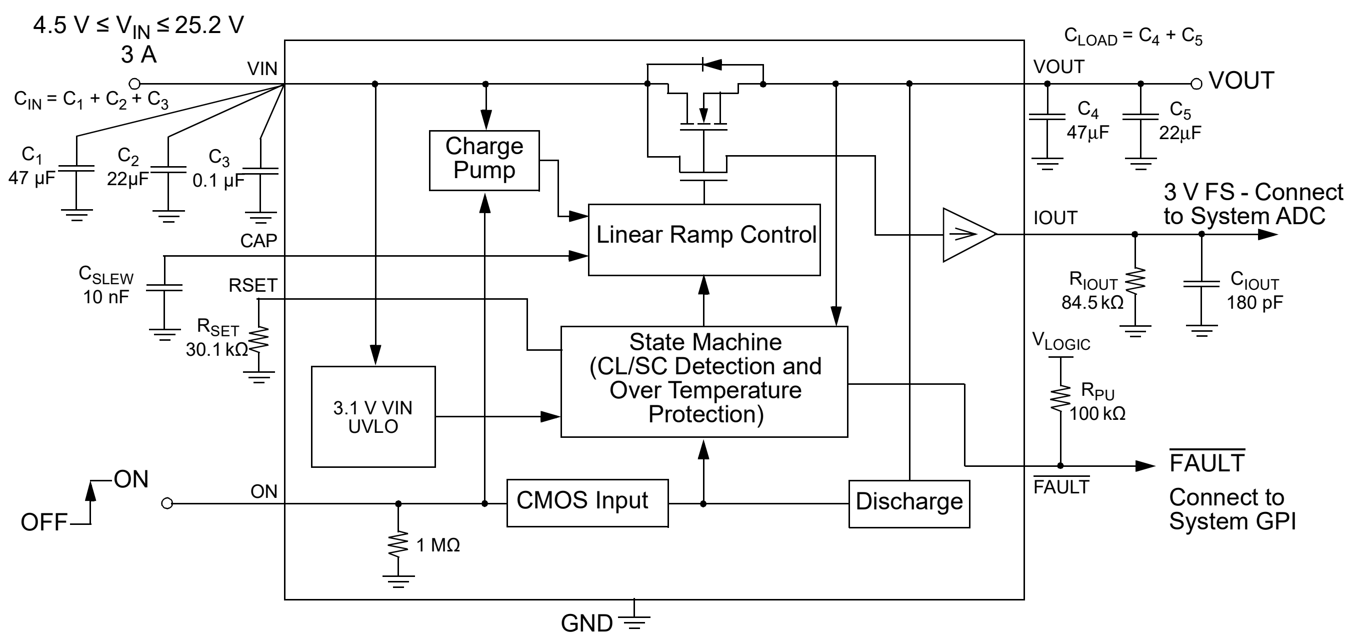



**18-pin STQFN**
1.6 x 3.0 mm, 0.40mm pitch
(Top View)

## Applications

- Telecommunications Equipment
- High-performance Computing
  - Point-of-Load Power Distribution
- Motor Drives

## Block Diagram



## Pin Description

| Pin # | Pin Name | Type | Pin Description |
|---|---|---|---|
| 1 | ON | Input | A low-to-high transition on this pin initiates the operation of the SLG59H1019V's state machine. ON is an asserted HIGH, level-sensitive CMOS input with $ON\_V_{IL}$ < 0.3 V and $ON\_V_{IH}$ > 0.9 V. Even though the ON pin circuit has a 1 MΩ internal pull-down resistor internally grounded, connect this pin to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. |
| 2 | GND | GND | Pin 2 is a low-current GND terminal for the SLG59H1019V. Connect directly to Pin 3 |
| 3 | GND | GND | Pin 3 is the main ground connection for the SLG59H1019V's internal charge pump, its gate driver and current-limit circuits as well as its internal state machine. Therefore, use a short, stout connection from Pin 3 to the system's analog or power plane. |
| 4-8 | VIN | MOSFET | VIN supplies the power for the operation of the SLG59H1019V, its internal control circuitry, and the drain terminal of the nFET load switch. With 5 pins fused together at VIN, connect a 47 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VIN should be rated at 50 V or higher. |
| 9-13 | VOUT | MOSFET | Source terminal of n-channel MOSFET (5 pins fused for VOUT). Connect a 47 µF (or larger) low-ESR capacitor from this pin to ground. Capacitors used at VOUT should be rated at 50 V or higher. |
| 14 | NC | Null | No Connect – Do not make any connection to this pin. |
| 15 | $\overline{FAULT}$ | Output | An open drain output, $\overline{FAULT}$ is asserted within $T\overline{FAULT}_{LOW}$ when a current-limit or an over-temperature condition is detected. $\overline{FAULT}$ is deasserted within $T\overline{FAULT}_{HIGH}$ when the fault condition is removed. Connect an 100 kΩ external resistor from the $\overline{FAULT}$ pin to local system logic supply. |
| 16 | CAP | Output | A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the $V_{OUT}$ slew rate and overall turn-on time of the SLG59H1019V. For best performance, the range for $C_{SLEW}$ values are 10 nF ≤ $C_{SLEW}$ ≤ 20 nF – please see typical characteristics for additional information. Capacitors used at the CAP pin should be rated at 10 V or higher. Please consult Applications Section on how to select $C_{SLEW}$ based on $V_{OUT}$ slew rate and loading conditions. |
| 17 | IOUT | Output | IOUT is the SLG59H1019V's power MOSFET load current monitor output. As an analog current output, this signal when applied to a ground-reference resistor generates a voltage proportional to the current through the n-channel MOSFET. The $I_{OUT}$ transfer characteristic is typically 10 µA/A with a voltage compliance range of 0.5 V ≤ $V_{IOUT}$ ≤ 4 V. Optimal $I_{OUT}$ linearity is exhibited for 0.5 A ≤ $I_{DS}$ ≤ 5 A. In addition, it is recommended to bypass the IOUT pin to GND with a 0.18 nF capacitor. |
| 18 | RSET | Input | A 1%-tolerance, metal-film resistor between 18 kΩ and 91 kΩ sets the SLG59H1019V's active current limit. A 91 kΩ resistor sets the SLG59H1019V's active current limit to 1 A and a 18 kΩ resistor sets the active current limit to 5 A. |

## Ordering Information

| Part Number | Type | Production Flow |
|---|---|---|
| SLG59H1019V | STQFN 18L FC | Industrial, -40 °C to 85 °C |
| SLG59H1019VTR | STQFN 18L FC (Tape and Reel) | Industrial, -40 °C to 85 °C |

## Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ to GND | Load Switch Input Voltage to GND | Continuous | -0.3 | -- | 30 | V |
| | | Maximum pulsed $V_{IN}$, pulse width < 0.1 s | -- | -- | 32 | V |
| $V_{OUT}$ to GND | Load Switch Output Voltage to GND | | -0.3 | -- | $V_{IN}$ | V |
| ON, CAP, RSET, IOUT, and $\overline{FAULT}$ to GND | ON, CAP, RSET, IOUT, and $\overline{FAULT}$ Pin Voltages to GND | | -0.3 | -- | 7 | V |
| $T_S$ | Storage Temperature | | -65 | -- | 150 | °C |
| $ESD_{HBM}$ | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| $ESD_{CDM}$ | ESD Protection | Charged Device Model | 500 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | | 1 | | |
| $\theta_{JA}$ | Thermal Resistance | 1.6 x 3.0 mm 18L STQFN; Determined with the device mounted onto a 1 $in^2$, 1 oz. copper pad of FR-4 material | -- | 40 | -- | °C/W |
| $T_{J,MAX}$ | Maximum Junction Temperature | | -- | 150 | -- | °C |
| MOSFET $IDS_{CONT}$ | Continuous Current from VIN to VOUT | $T_J$ < 150 °C | -- | -- | 5 | A |
| MOSFET $IDS_{PEAK}$ | Peak Current from VIN to VOUT | Maximum pulsed switch current, pulse width < 1 ms, 1% duty cycle | -- | -- | 6 | A |

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## Electrical Characteristics

4.5 V ≤ $V_{IN}$ ≤ 25.2 V; $C_{IN}$ = 47 µF, $T_A$ = -40 °C to 85 °C, unless otherwise noted. Typical values are at $T_A$ = 25 °C

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IN}$ | Operating Input Voltage | | 4.5 | -- | 25.2 | V |
| $V_{IN(UVLO)}$ | $V_{IN}$ Undervoltage Lockout Threshold | $V_{IN}$ ↓ | 2.4 | -- | 3.8 | V |
| $I_Q$ | Quiescent Supply Current | ON = HIGH; $I_{DS}$ = 0 A | -- | 0.5 | 0.6 | mA |
| $I_{SHDN}$ | OFF Mode Supply Current | ON = LOW; $I_{DS}$ = 0 A | -- | 1 | 3 | µA |
| $RDS_{ON}$ | ON Resistance | $T_A$ = 25 °C; $I_{DS}$ = 0.1 A | -- | 13 | 14 | mΩ |
| | | $T_A$ = 85 °C; $I_{DS}$ = 0.1 A | -- | 17.2 | 19.2 | mΩ |
| MOSFET IDS | Current from VIN to VOUT | Continuous | -- | -- | 5 | A |
| $I_{LIMIT}$ | Active Current Limit, $I_{ACL}$ | $V_{OUT}$ > 0.5 V; $R_{SET}$ = 30.1 kΩ | 2.7 | 3.19 | 3.4 | A |
| | Short-circuit Current Limit, $I_{SCL}$ | $V_{OUT}$ < 0.5 V | -- | 0.5 | - | A |
| $T_{ACL}$ | Active Current Limit Response Time | $R_{SET}$ = 51.6 kΩ | -- | 120 | -- | µs |
| $R_{DISCHRG}$ | Output Discharge Resistance | | 650 | 750 | 900 | Ω |
| $I_{OUT}$ | MOSFET Current Analog Monitor Output | $I_{DS}$ = 1 A | 9.3 | 10 | 11.1 | µA |
| | | $I_{DS}$ = 3 A | 29 | 30.3 | 32 | µA |

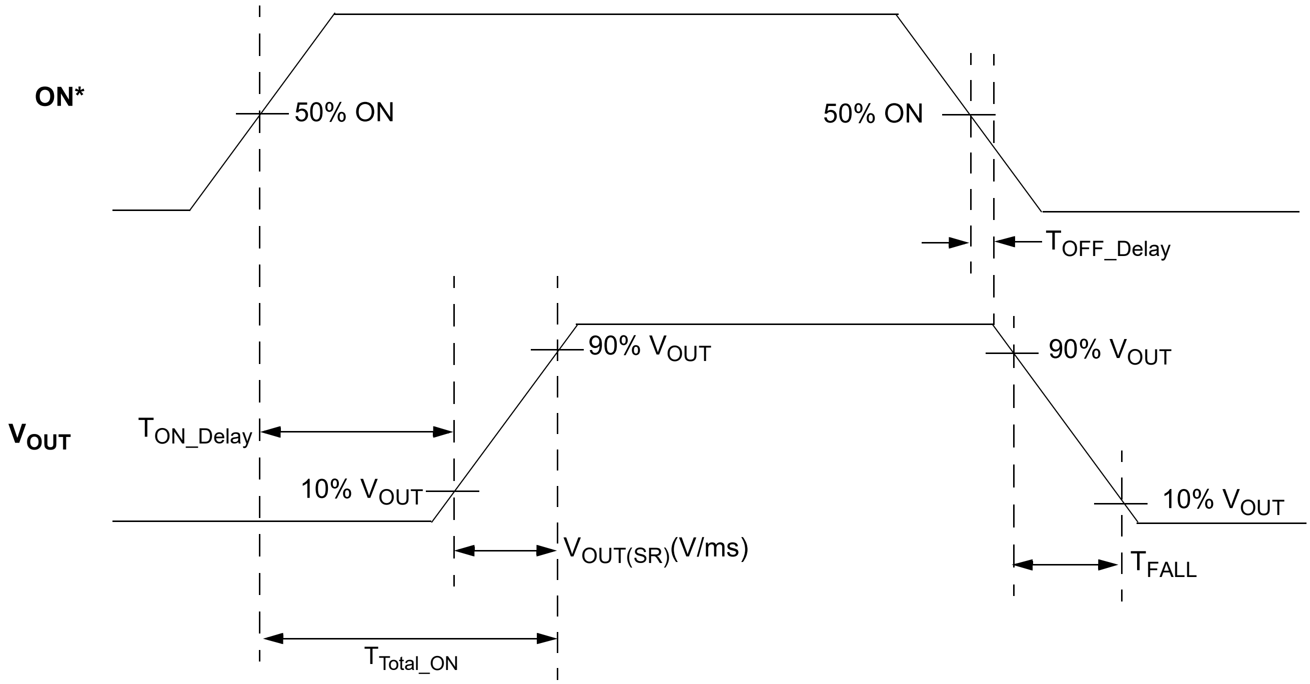
## Electrical Characteristics (continued)

4.5 V ≤ $V_{IN}$ ≤ 25.2 V; $C_{IN}$ = 47 µF, $T_A$ = -40 °C to 85 °C, unless otherwise noted. Typical values are at $T_A$ = 25 °C

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $T_{IOUT}$ | $I_{OUT}$ Response Time to Change in Main MOSFET Current | $C_{IOUT}$ = 180 pF;<br>Step load 0 to 2.4 A; 0% to 90% $I_{OUT}$ | -- | 45 | -- | µs |
| $C_{LOAD}$ | Output Load Capacitance | $C_{LOAD}$ connected from VOUT to GND | -- | 47 | -- | µF |
| $T_{ON\_Delay}$ | ON Delay Time | 50% ON to 10% $V_{OUT}$ ↑;<br>$V_{IN}$ = 4.5 V; $C_{SLEW}$ = 10 nF;<br>$R_{LOAD}$ = 100 Ω, $C_{LOAD}$ = 10 µF | 300 | 400 | 600 | µs |
| | | 50% ON to 10% $V_{OUT}$ ↑;<br>$V_{IN}$ = 25.2 V; $C_{SLEW}$ = 10 nF;<br>$R_{LOAD}$ = 100 Ω, $C_{LOAD}$ = 10µF | 0.9 | 1.0 | 1.2 | ms |
| $T_{Total\_ON}$ | Total Turn ON Time | 50% ON to 90% $V_{OUT}$ ↑ | Set by External $C_{SLEW}$[1] | | | ms |
| | | 50% ON to 90% $V_{OUT}$ ↑;<br>$V_{IN}$ = 4.5 V; $C_{SLEW}$ = 10 nF;<br>$R_{LOAD}$ = 100 Ω, $C_{LOAD}$ = 10 µF | 1.8 | 1.9 | 2.1 | ms |
| | | 50% ON to 90% $V_{OUT}$ ↑;<br>$V_{IN}$ = 25.2 V; $C_{SLEW}$ = 10 nF;<br>$R_{LOAD}$ = 100 Ω, $C_{LOAD}$ = 10 µF | 8.9 | 9.0 | 9.2 | ms |
| $V_{OUT(SR)}$ | $V_{OUT}$ Slew rate | 50% ON to 90% $V_{OUT}$ ↑ | Set by External $C_{SLEW}$[1] | | | V/ms |
| | | 10% to 90% $V_{OUT}$ ↑;<br>$V_{IN}$ = 4.5 to 25.2 V; $C_{SLEW}$ = 10 nF;<br>$R_{LOAD}$ = 100 Ω, $C_{LOAD}$ = 10 µF | 3 | 3.2 | 3.5 | V/ms |
| $T_{OFF\_Delay}$ | OFF Delay Time | 50% ON to $V_{OUT}$ Fall Start ↓;<br>ON = HIGH-to-LOW;<br>$V_{IN}$ = 4.5 V to 25.2 V;<br>$R_{LOAD}$ = 100 Ω, No $C_{LOAD}$ | -- | 15 | -- | µs |
| $T_{FALL}$ | $V_{OUT}$ Fall Time | 90% $V_{OUT}$ to 10% $V_{OUT}$ ↓;<br>ON = HIGH-to-LOW;<br>$V_{IN}$ = 4.5 V to 25.2 V;<br>$R_{LOAD}$ = 100 Ω, No $C_{LOAD}$ | 10 | 12 | 18 | µs |
| $T\overline{FAULT}_{LOW}$ | $\overline{FAULT}$ Assertion Time | Abnormal Step Load Current event to $\overline{FAULT}$↓;<br>$I_{ACL}$ = 1 A; $V_{IN}$ = 25.2 V; $R_{SET}$ = 91 kΩ;<br>switch in 20 Ω load | -- | 80 | -- | µs |
| $T\overline{FAULT}_{HIGH}$ | $\overline{FAULT}$ De-assertion Time | Delay to $\overline{FAULT}$↑ after fault condition is removed; $I_{ACL}$ = 1 A; $V_{IN}$ = 25.2 V;<br>$R_{SET}$ = 91 kΩ; switch out 20 Ω load | -- | 180 | -- | µs |
| $\overline{FAULT}_{VOL}$ | $\overline{FAULT}$ Output Low Voltage | $I_{\overline{FAULT}}$ = 1 mA | -- | 0.2 | -- | V |
| $ON\_V_{IH}$ | ON Pin Input High Voltage | Internal 1 MΩ ±20% from ON Pin to GND | 0.9 | -- | 5 | V |
| $ON\_V_{IL}$ | ON Pin Input Low Voltage | | -0.3 | 0 | 0.3 | V |
| $I_{ON(Leakage)}$ | ON Pin Leakage Current | 0.9 V ≤ ON ≤ 5 V or ON = GND | -- | -- | 2 | µA |
| $THERM_{ON}$ | Thermal Protection Shutdown Threshold | | -- | 145 | -- | °C |
| $THERM_{OFF}$ | Thermal Protection Restart Threshold | | -- | 120 | -- | °C |

Notes:
1. Refer to typical Timing Parameter vs. $C_{SLEW}$ performance charts for additional information when available.

### $T_{Total\_ON}$, $T_{ON\_Delay}$, and Slew Rate Measurement Timing Details

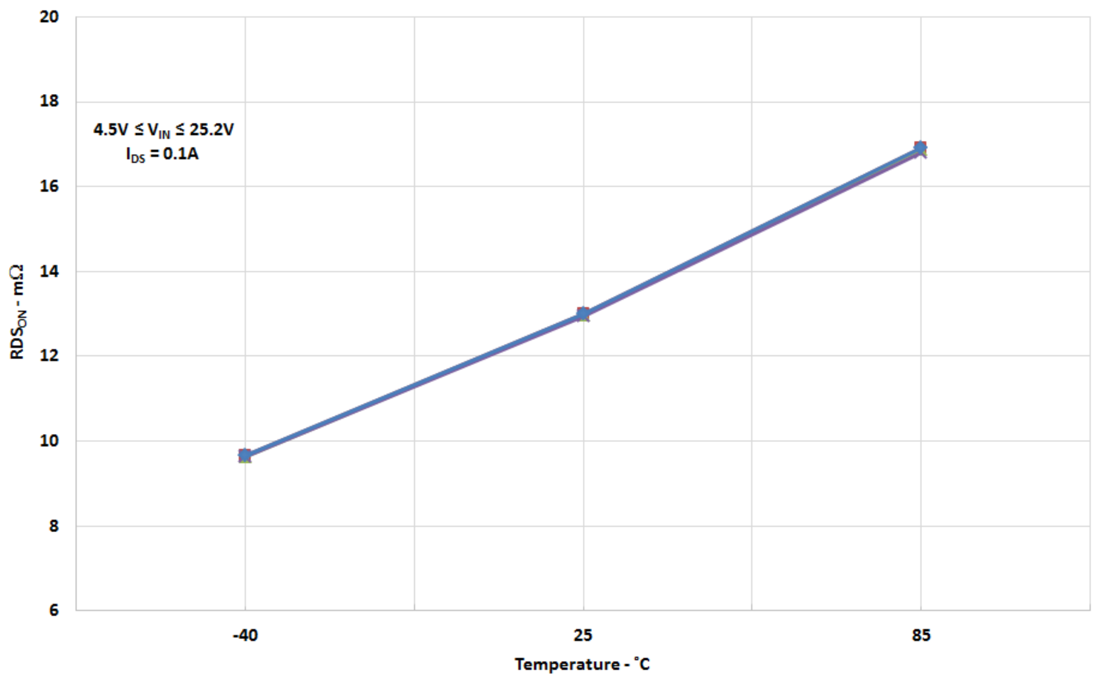



* Rise and Fall times of the ON signal are 100 ns

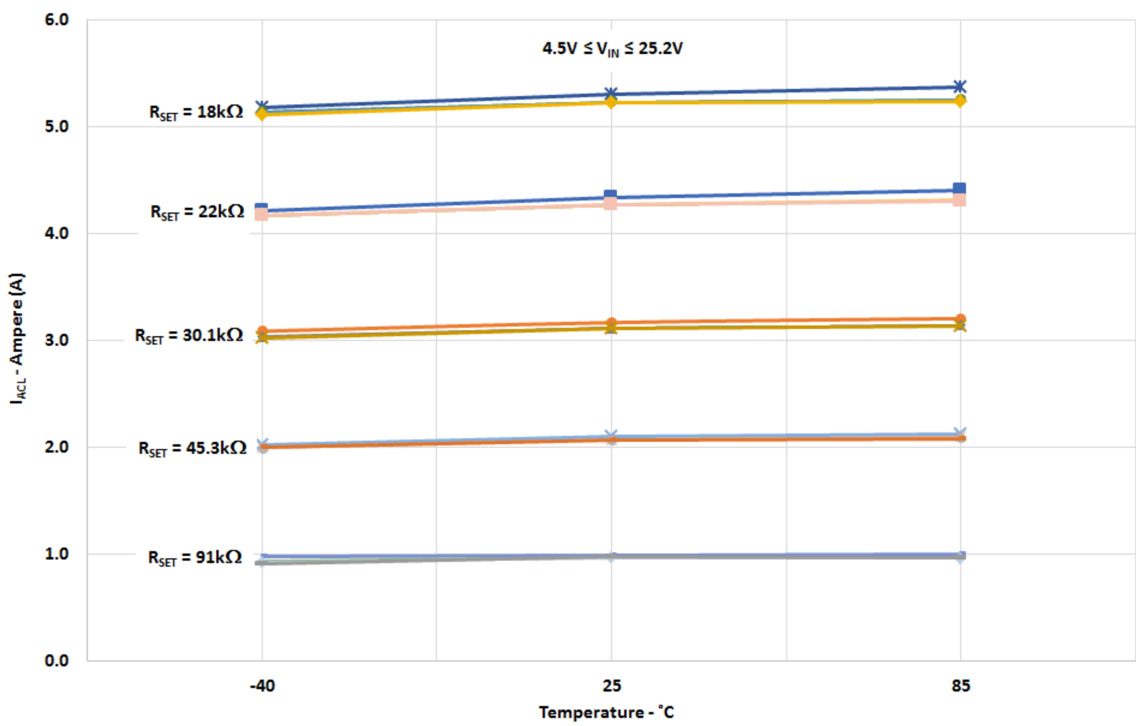
 

## Typical Performance Characteristics

### $RDS_{ON}$ vs. Temperature and $V_{IN}$

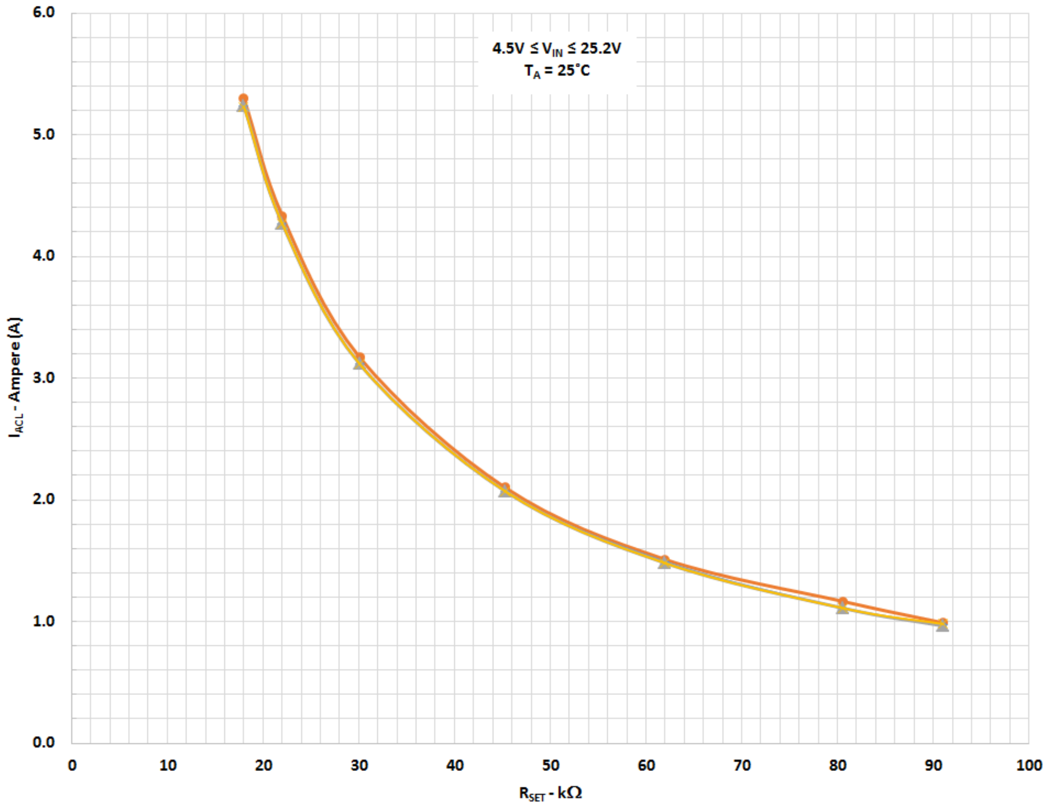



### $I_{ACL}$ vs. Temperature and $R_{SET}$

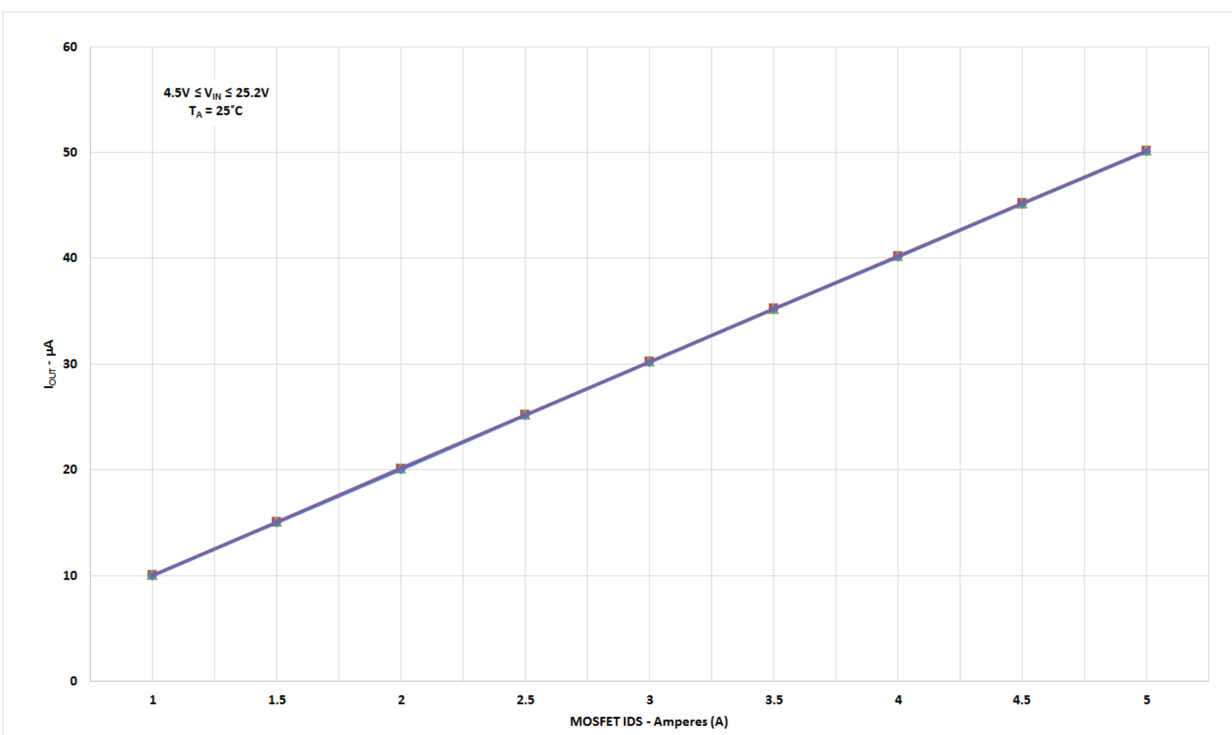


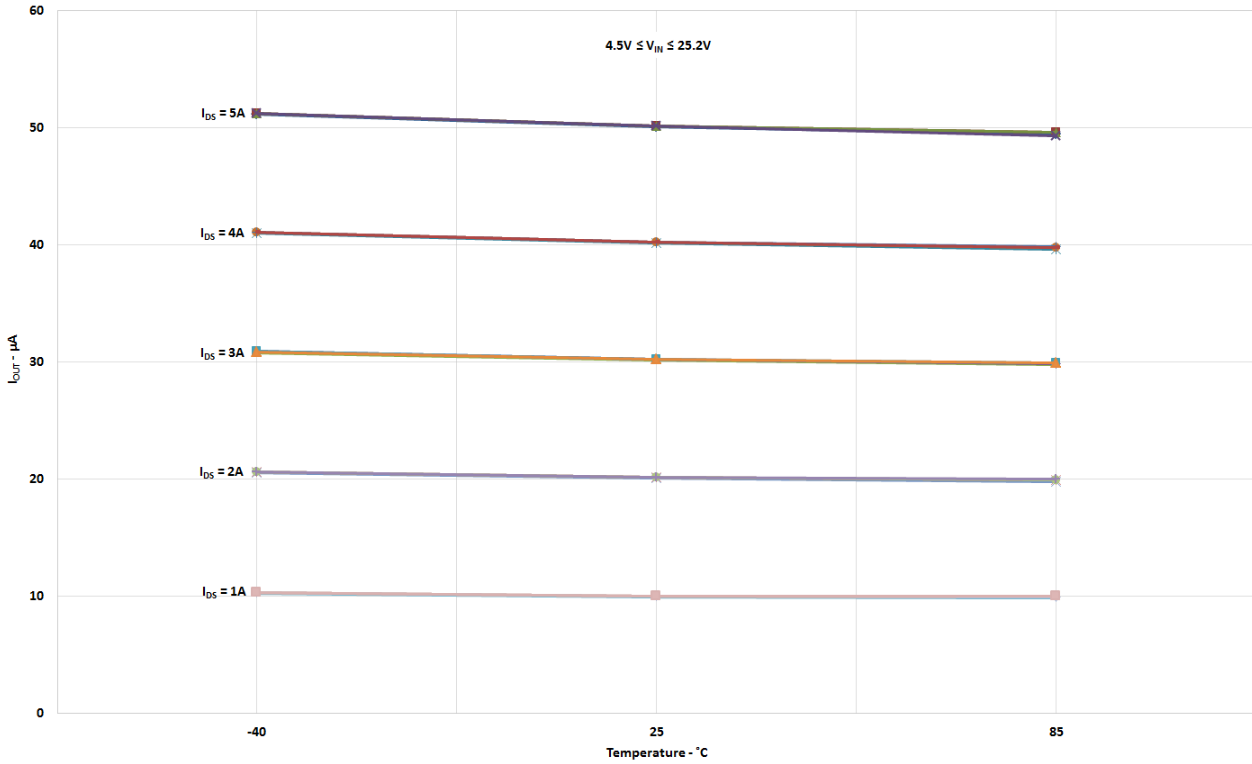
### $I_{ACL}$ vs. $R_{SET}$ and $V_{IN}$



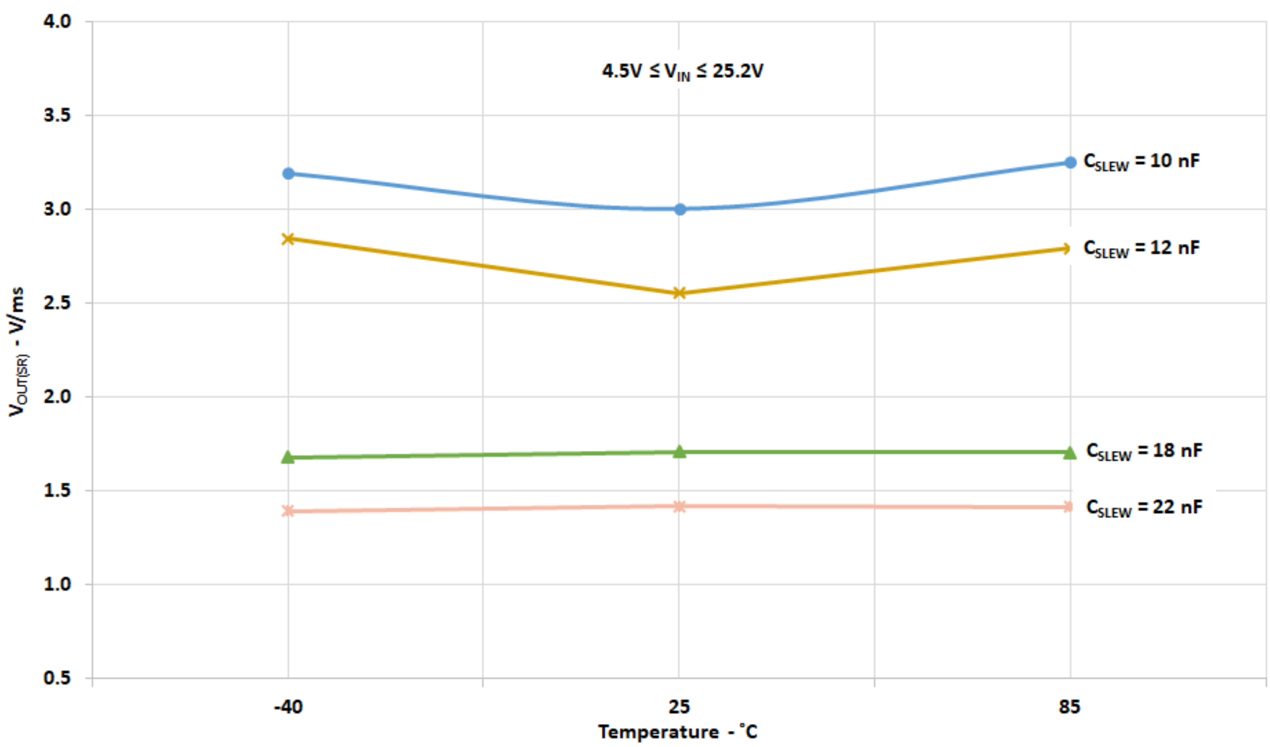

### $I_{OUT}$ vs. MOSFET IDS and $V_{IN}$



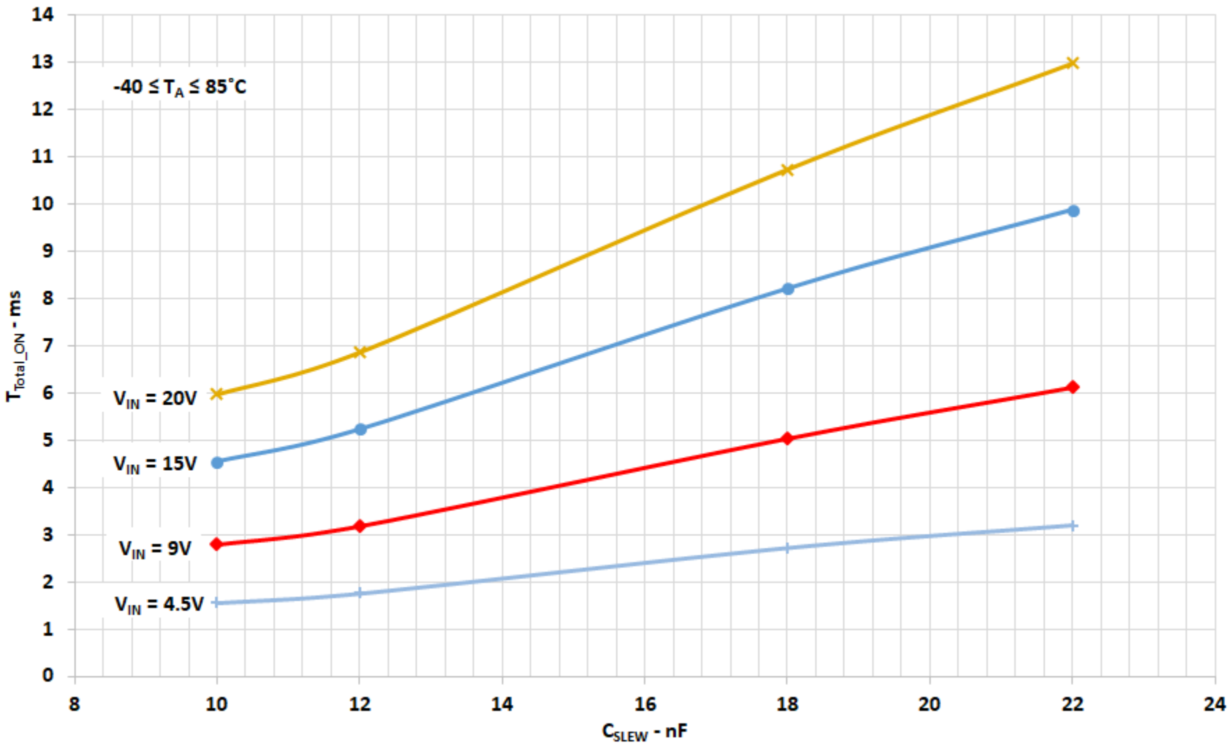
### $I_{OUT}$ vs. Temperature and MOSFET IDS




### $V_{OUT}$ Slew Rate vs. Temperature, $V_{IN}$, and $C_{SLEW}$

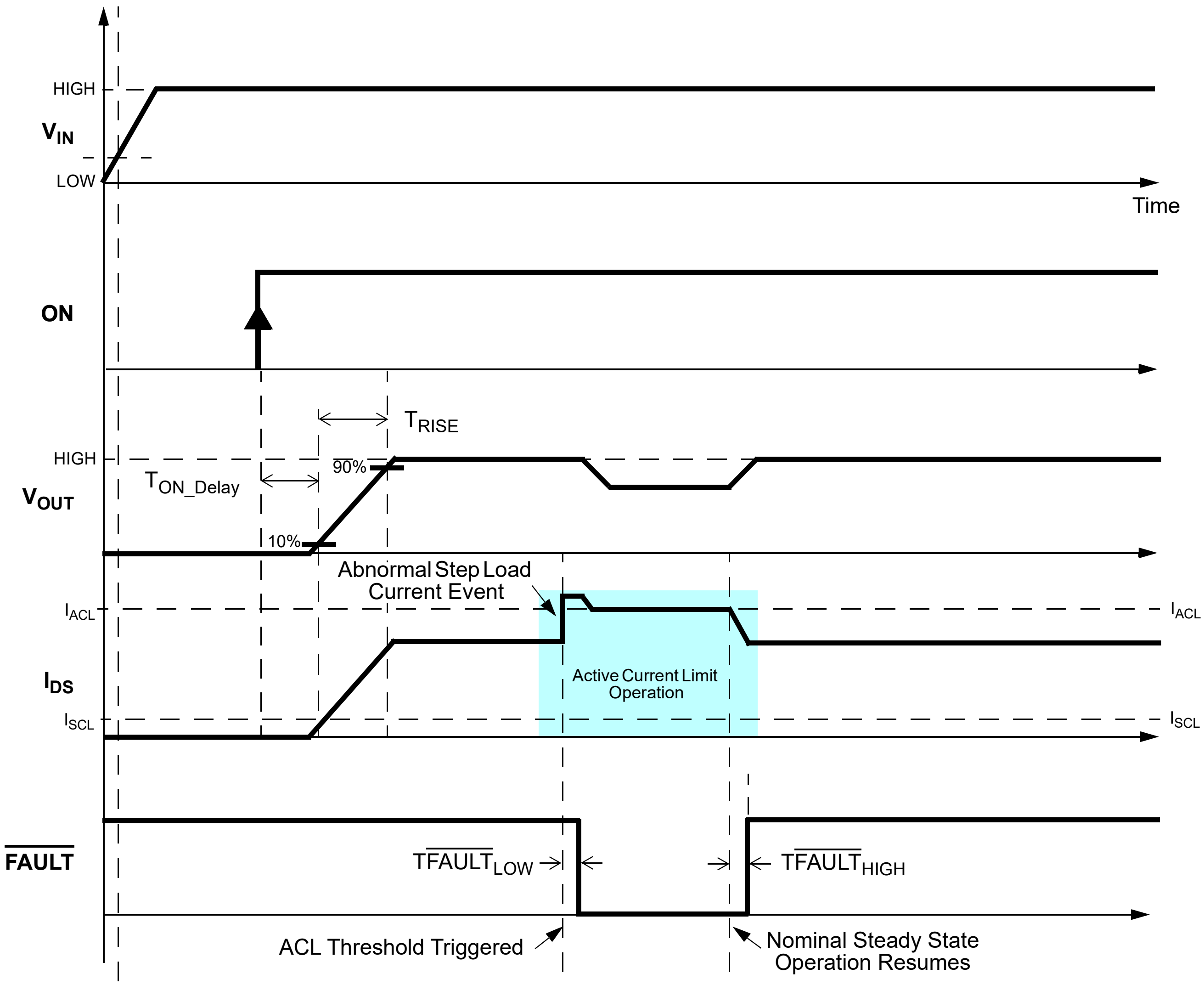


### $T_{Total\_ON}$ vs. $C_{SLEW}$, $V_{IN}$, and Temperature



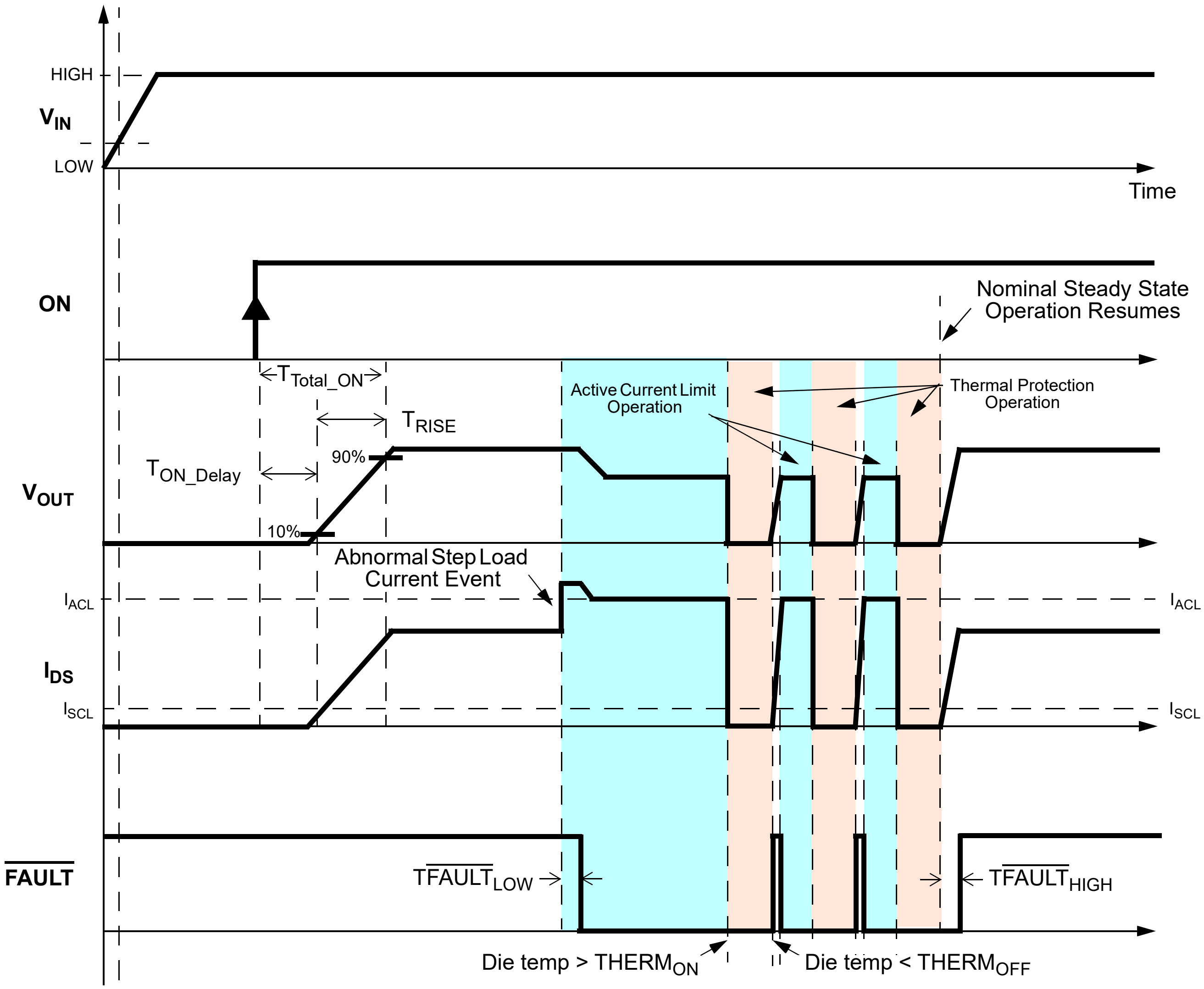

 

### Timing Diagram - Basic Operation including Active Current Limit Protection

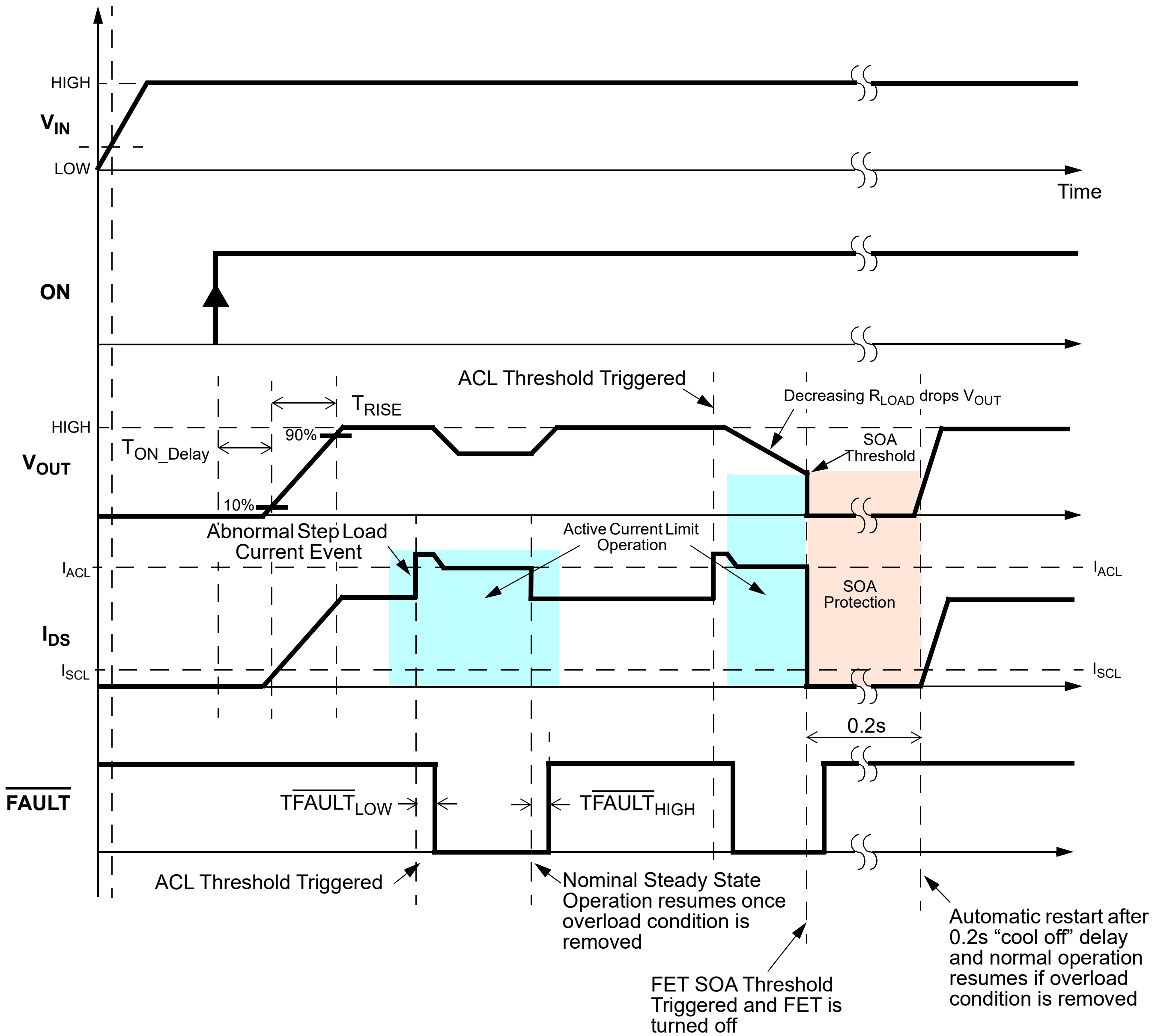


### Timing Diagram - Active Current Limit & Thermal Protection Operation



## Timing Diagram - Basic Operation including Active Current + Internal FET SOA Protection



## SLG59H1019V Application Diagram

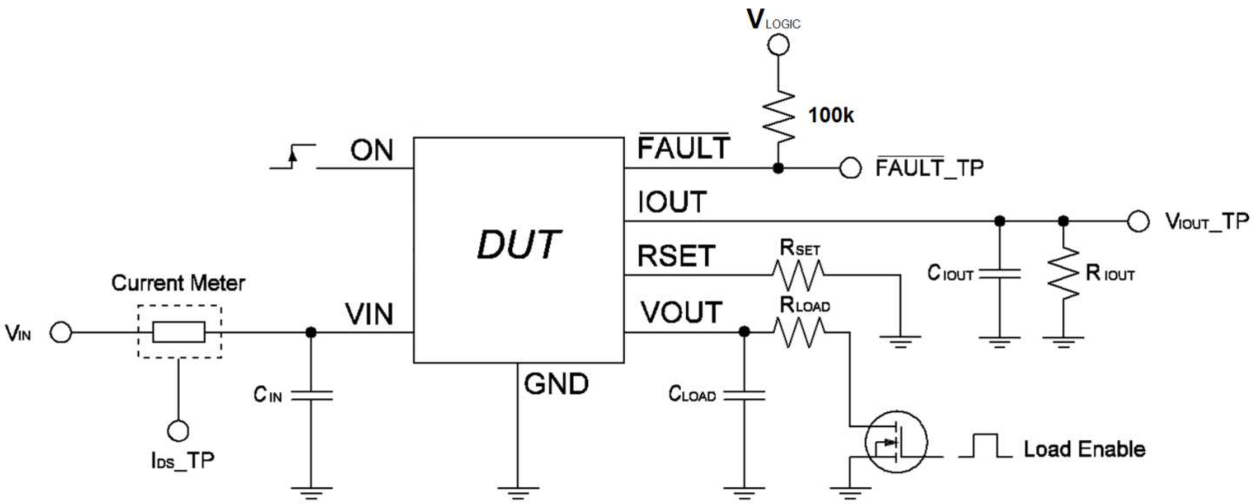



**Figure 1. Test setup Application Diagram**

## Typical Turn-on Waveforms

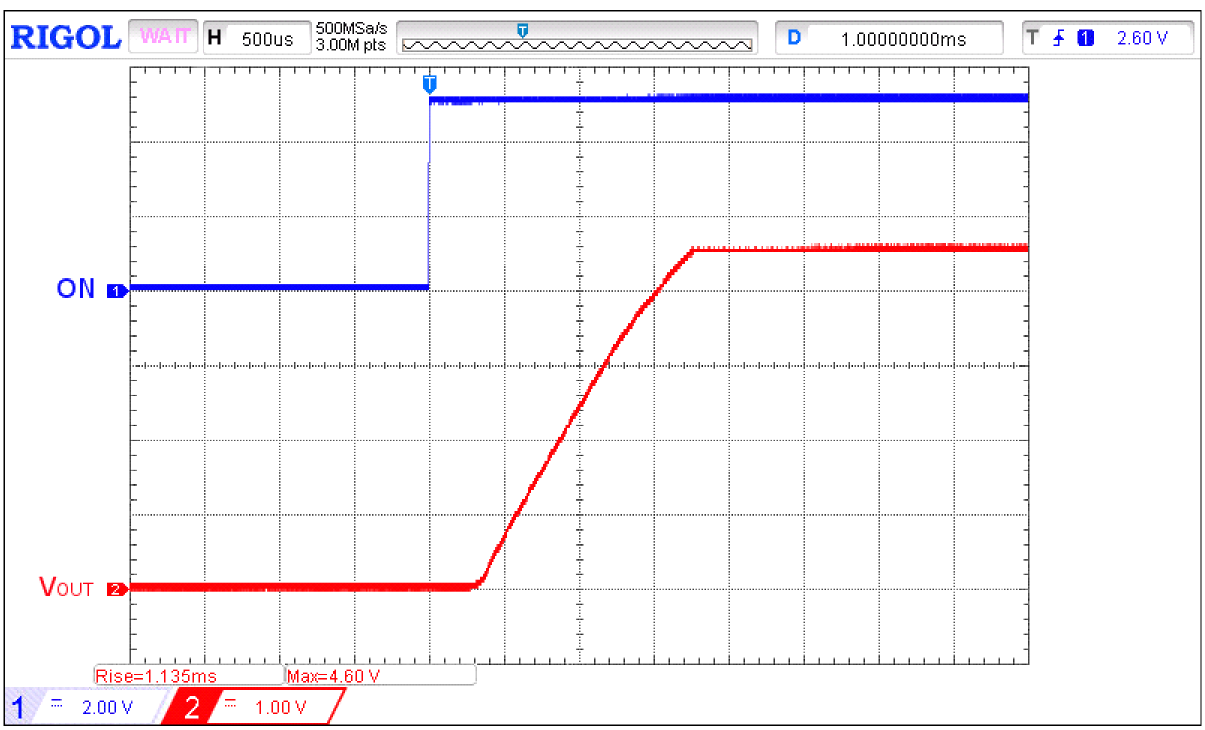



**Figure 2. Typical Turn ON operation waveform for $V_{IN}$ = 4.5 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω**

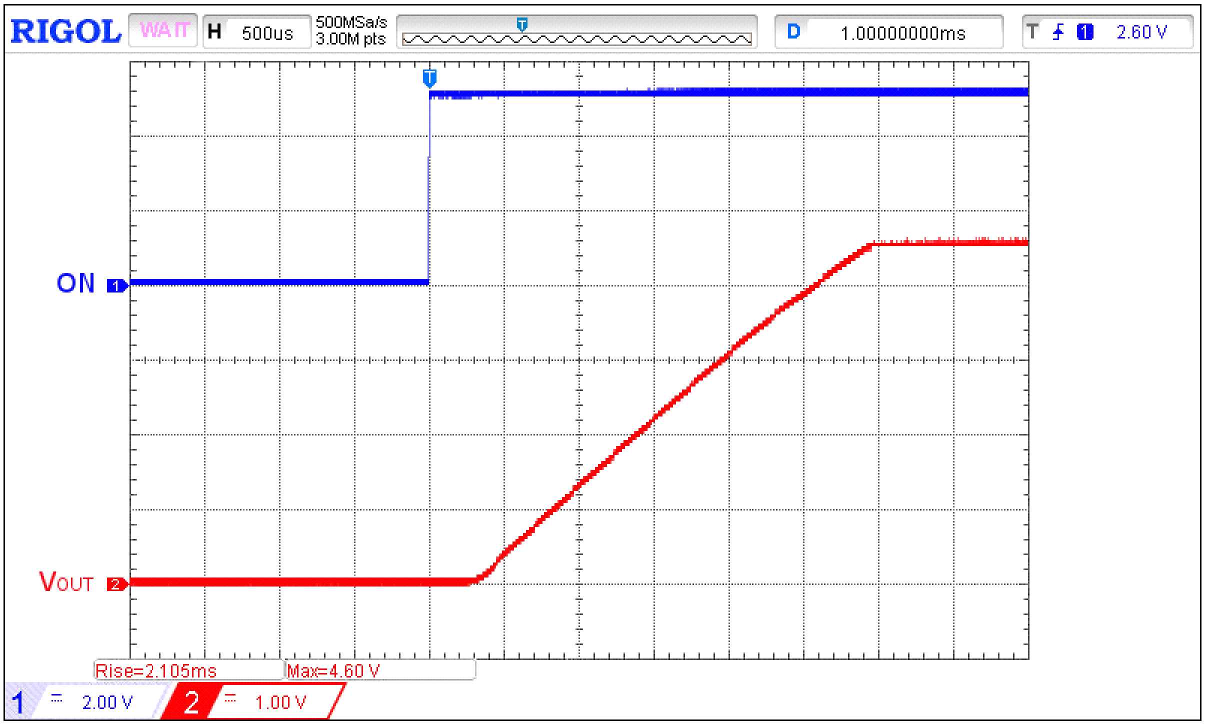



**Figure 3. Typical Turn ON operation waveform for $V_{IN}$ = 4.5 V, $C_{SLEW}$ = 18 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω**

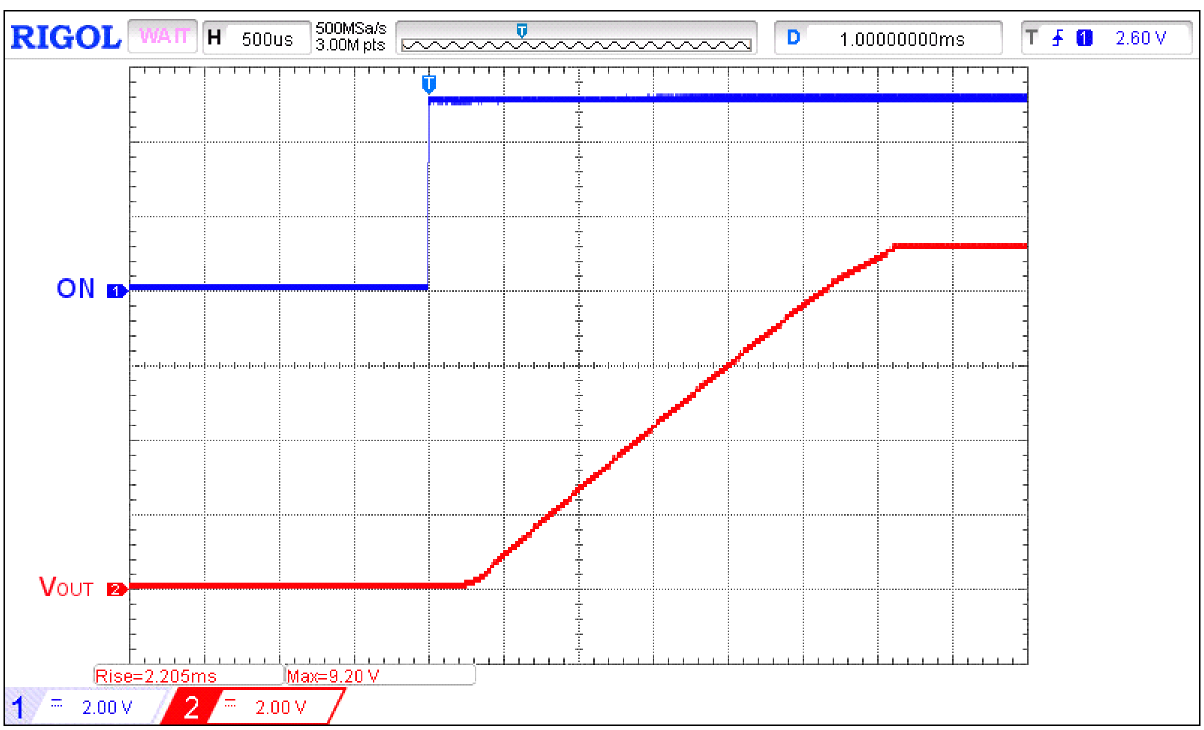



**Figure 4. Typical Turn ON operation waveform for $V_{IN}$ = 9 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω**

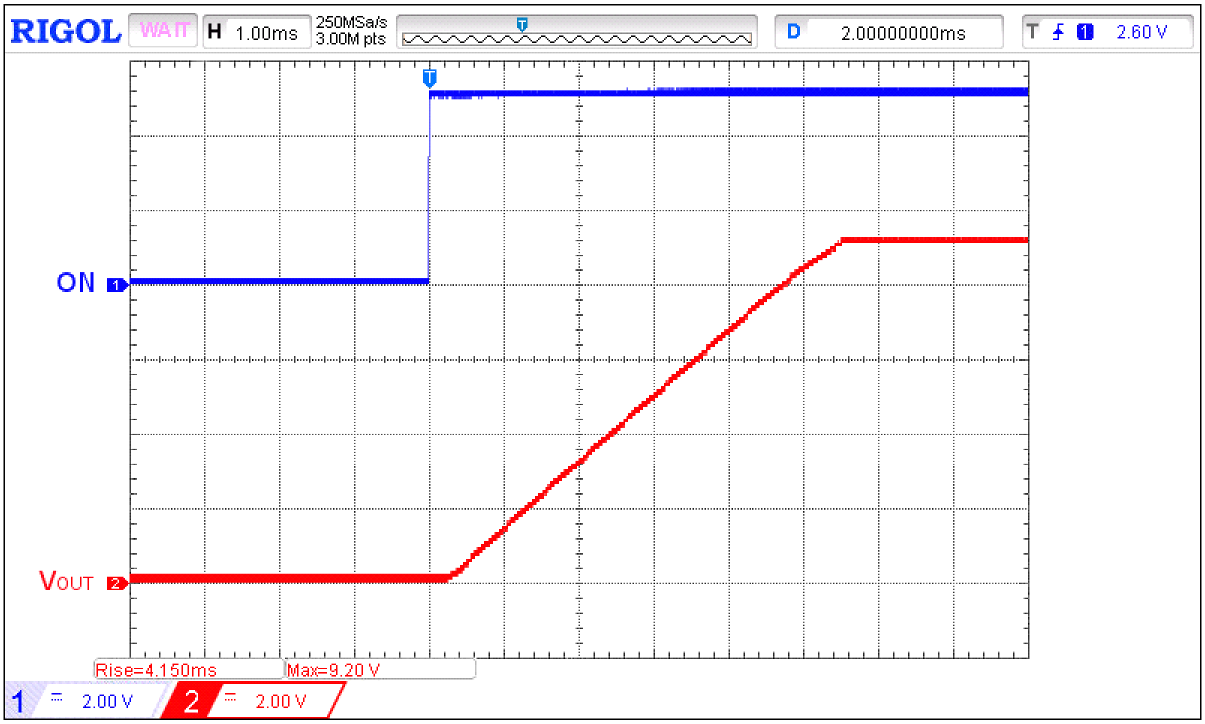



**Figure 5. Typical Turn ON operation waveform for $V_{IN}$ = 9 V, $C_{SLEW}$ = 18 nF, $C_{LOAD}$ = 10 μF, $R_{LOAD}$ = 100 Ω**

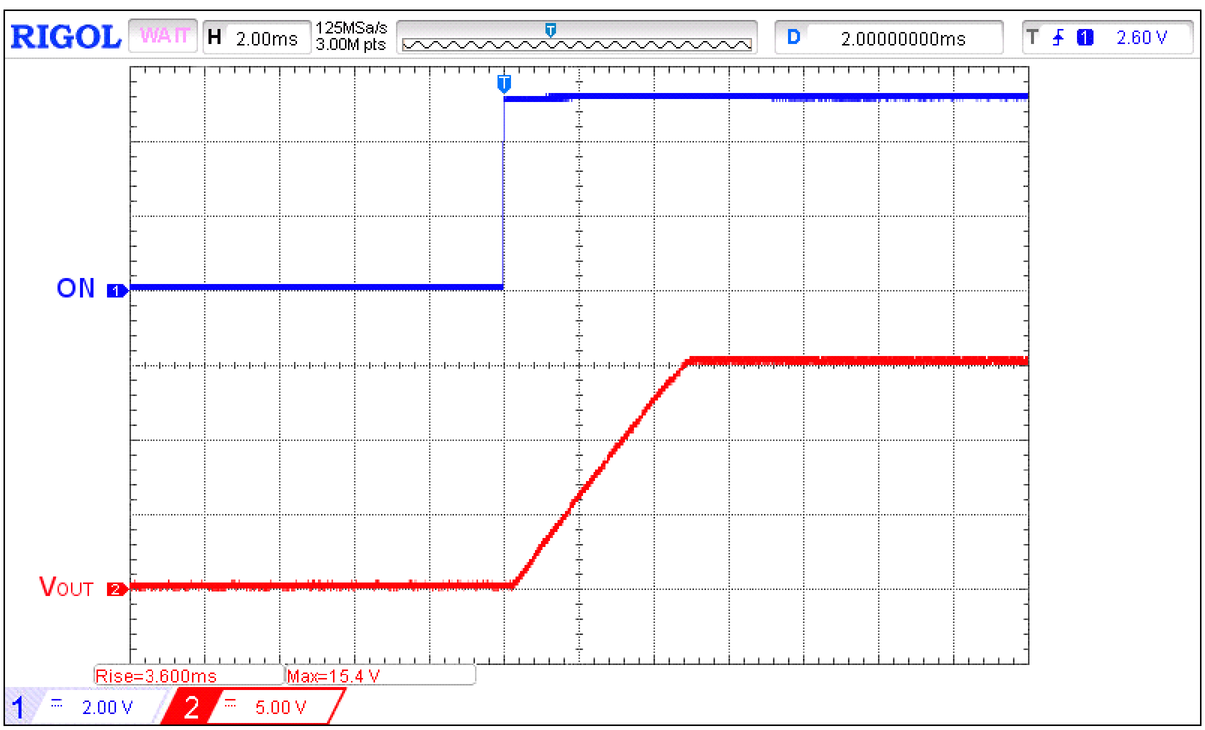



**Figure 6. Typical Turn ON operation waveform for $V_{IN}$ = 15 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 μF, $R_{LOAD}$ = 100 Ω**

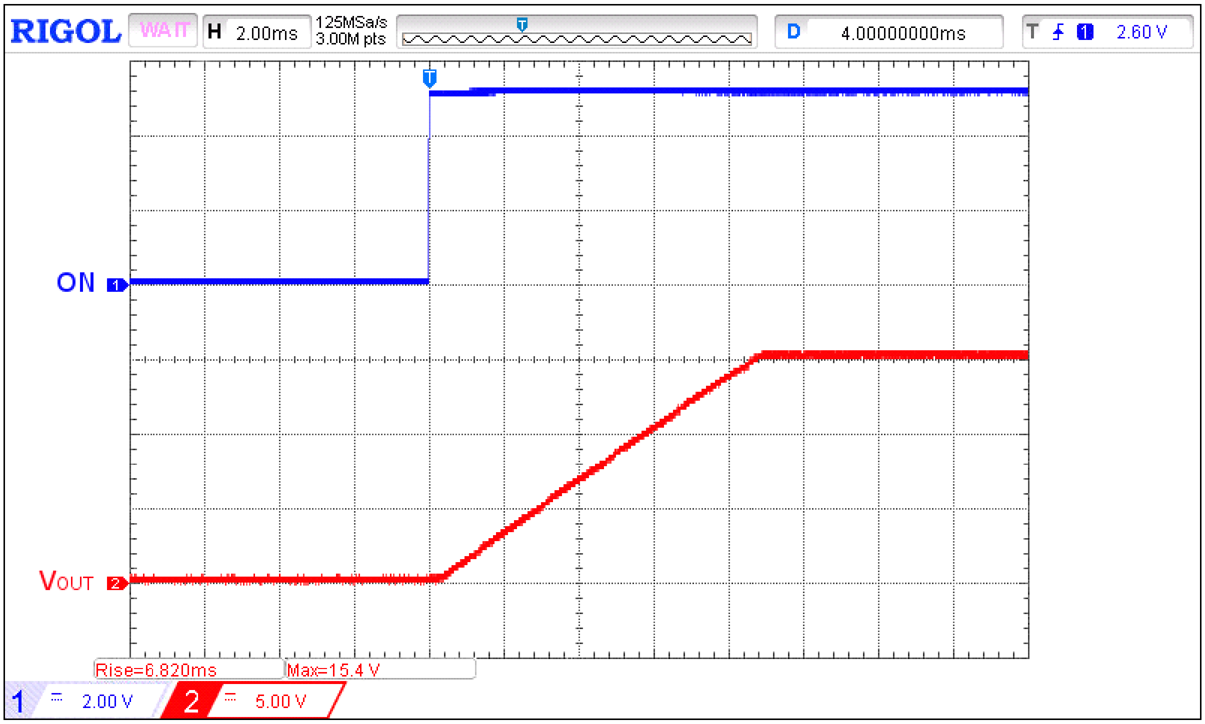



Figure 7. Typical Turn ON operation waveform for $V_{IN}$ = 15 V, $C_{SLEW}$ = 18 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω

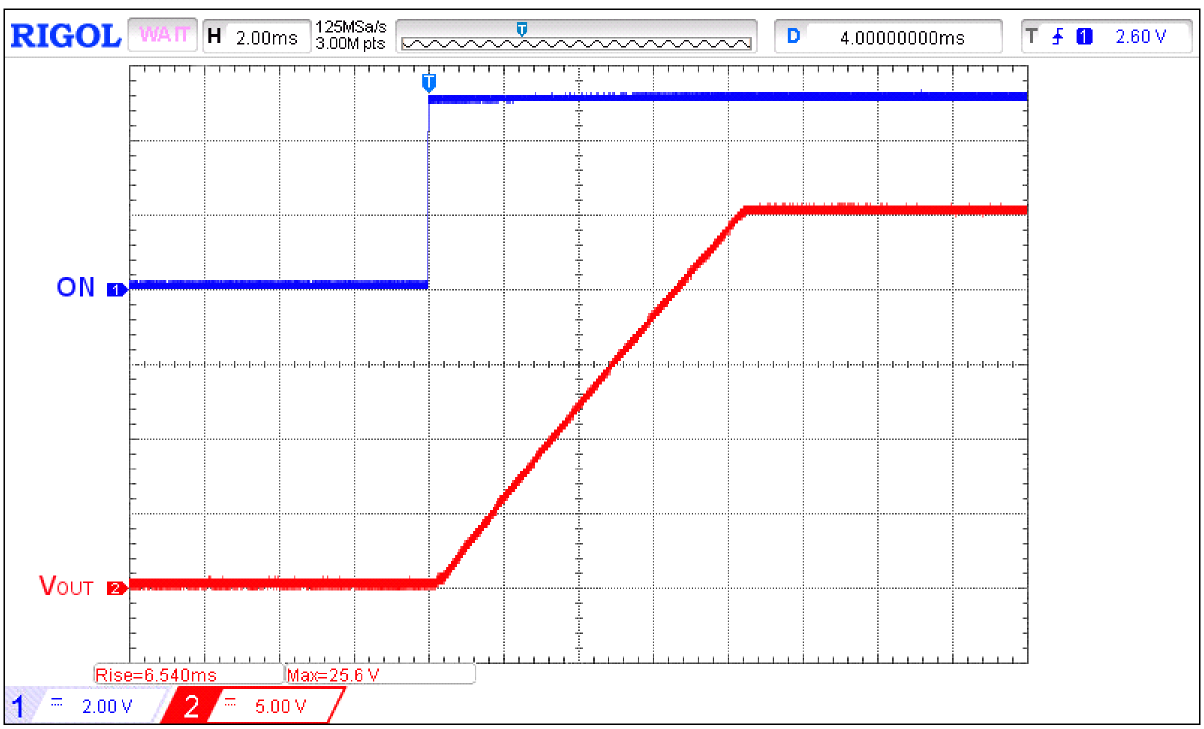



Figure 8. Typical Turn ON operation waveform for $V_{IN}$ = 25.2 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω

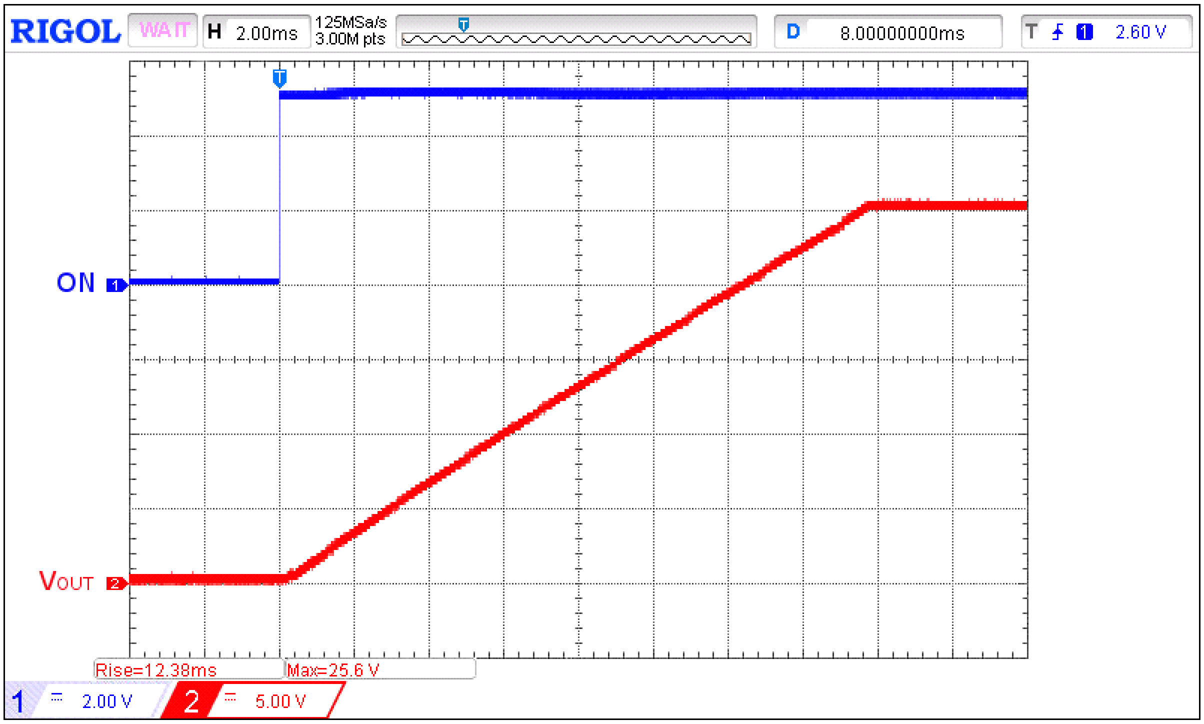



Figure 9. Typical Turn ON operation waveform for $V_{IN}$ = 25.2 V, $C_{SLEW}$ = 18 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω

## Typical Turn-off Waveforms

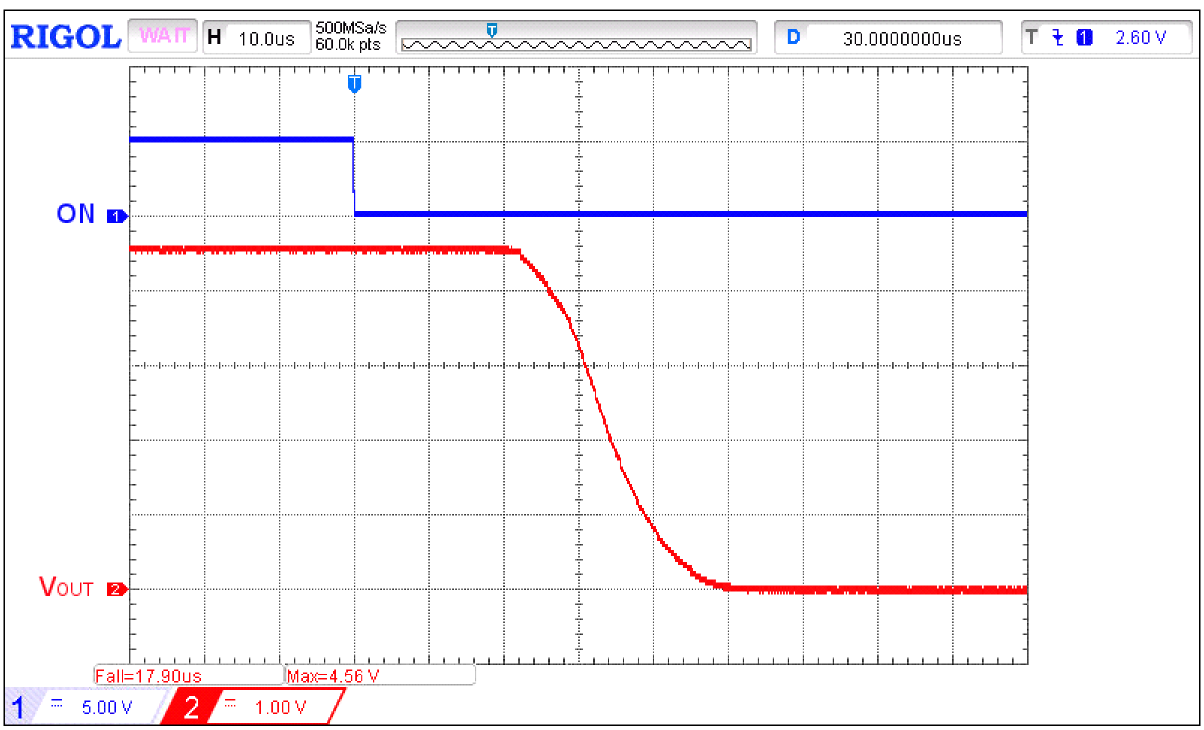



Figure 10. Typical Turn OFF operation waveform for $V_{IN}$ = 4.5 V, $C_{SLEW}$ = 10 nF, no $C_{LOAD}$ , $R_{LOAD}$ = 100 Ω

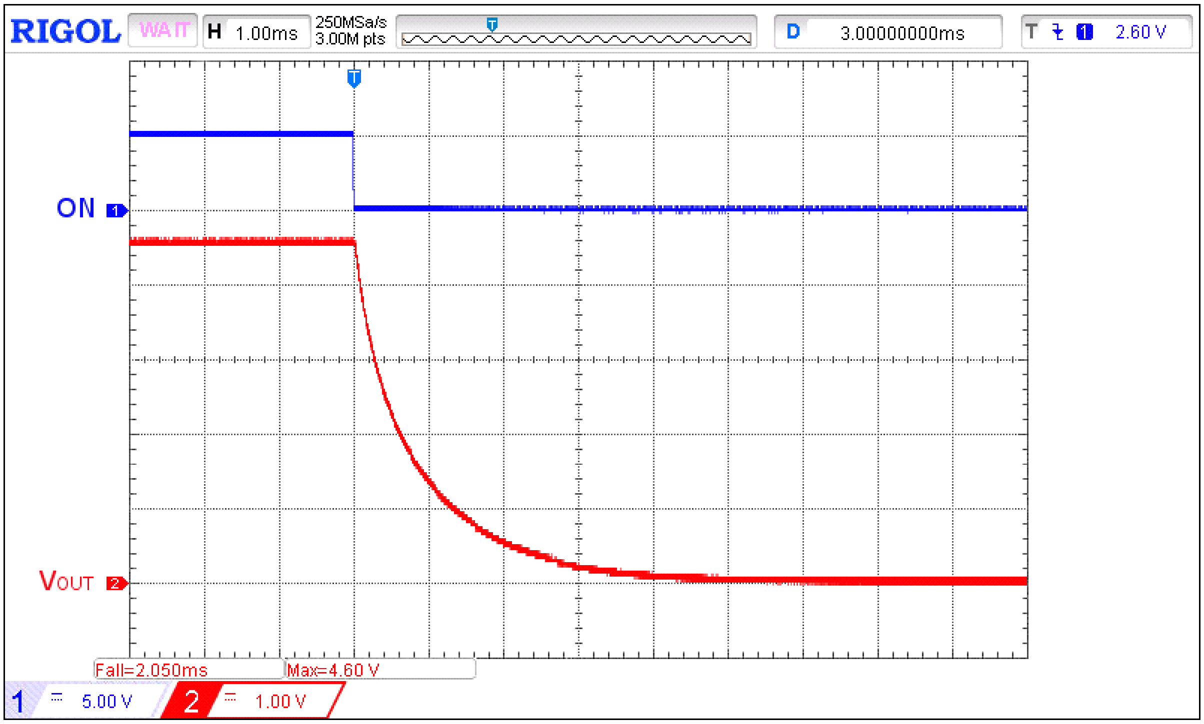



Figure 11. Typical Turn OFF operation waveform for $V_{IN}$ = 4.5 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω

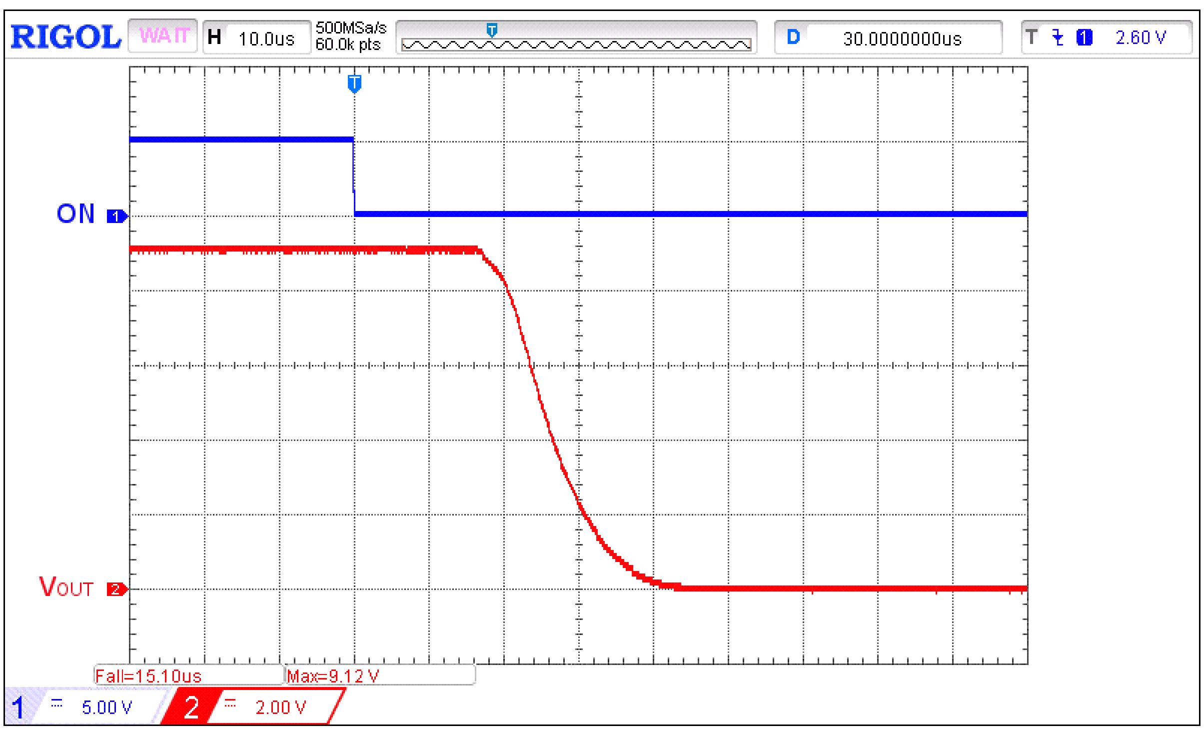



Figure 12. Typical Turn OFF operation waveform for $V_{IN}$ = 9 V, $C_{SLEW}$ = 10 nF, no $C_{LOAD}$ , $R_{LOAD}$ = 100 Ω

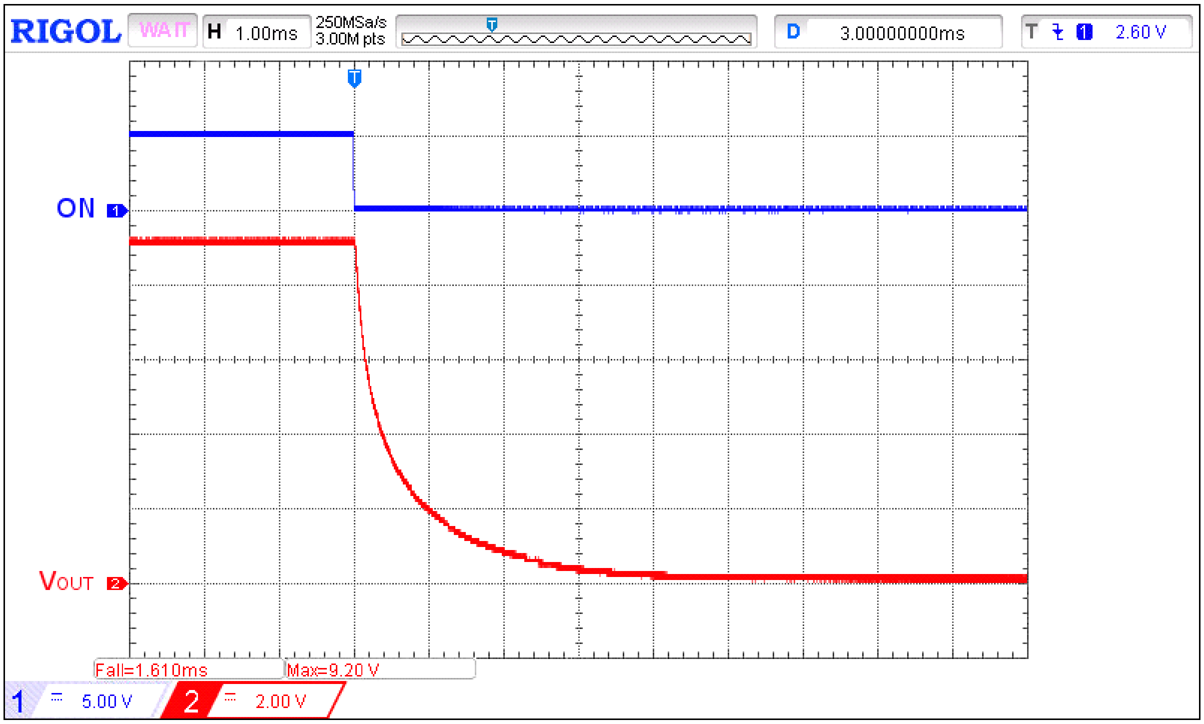



**Figure 13. Typical Turn OFF operation waveform for $V_{IN}$ = 9 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω**

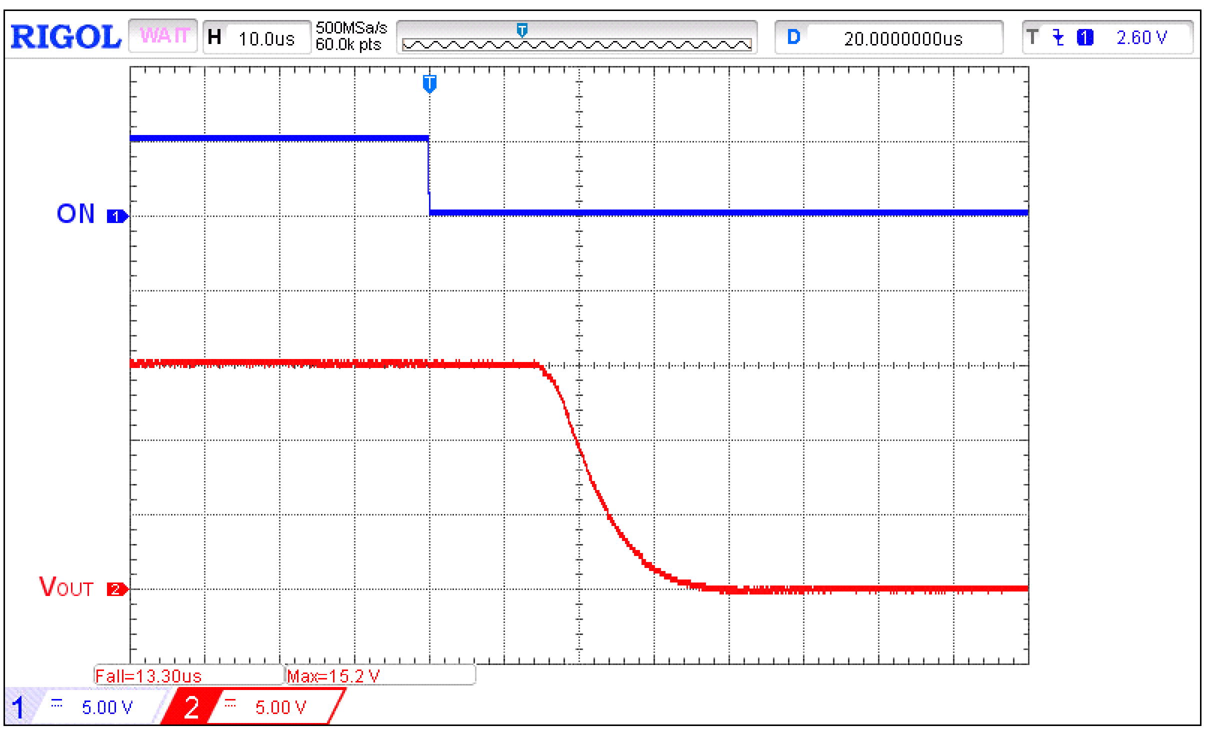



**Figure 14. Typical Turn OFF operation waveform for $V_{IN}$ = 15 V, $C_{SLEW}$ = 10 nF, no $C_{LOAD}$ , $R_{LOAD}$ = 100 Ω**

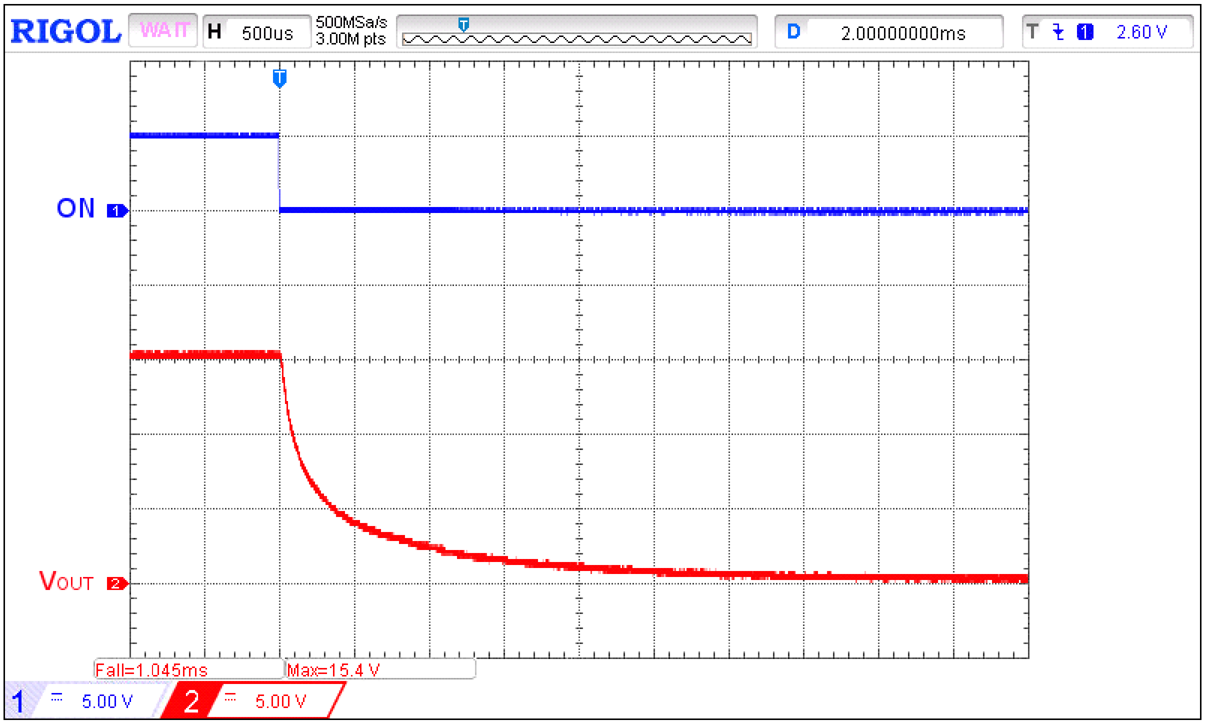



**Figure 15. Typical Turn OFF operation waveform for $V_{IN}$ = 15 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω**

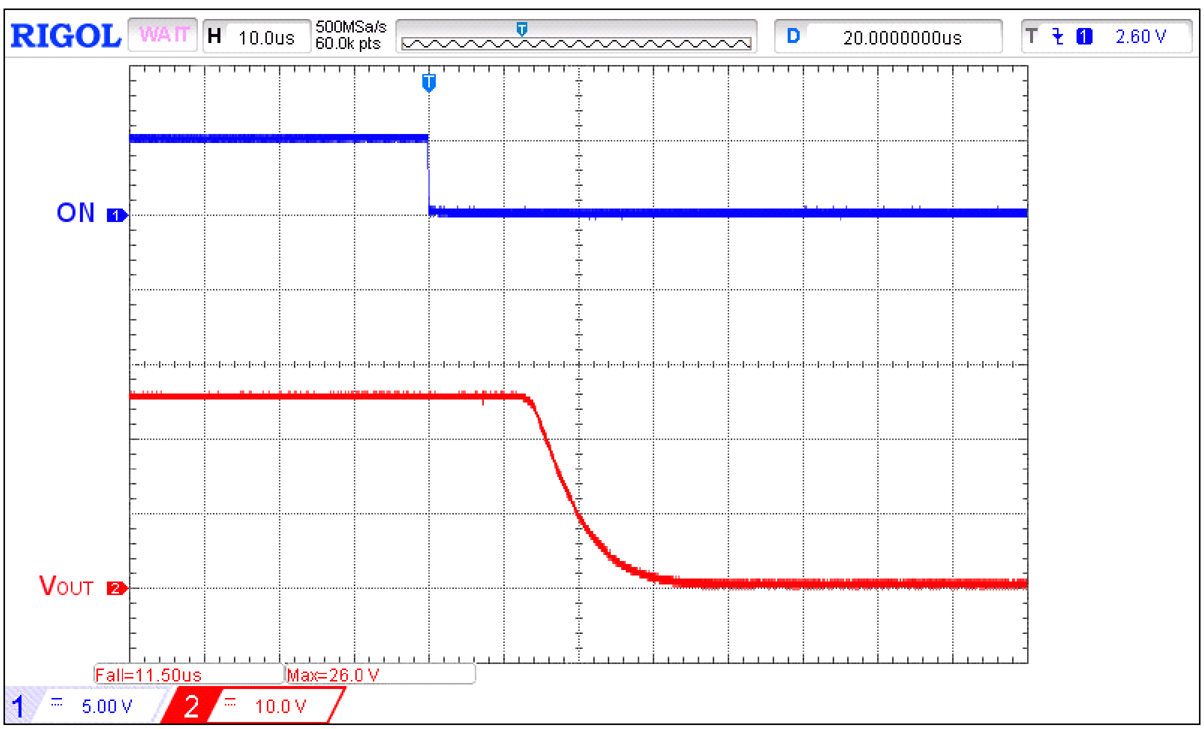



**Figure 16. Typical Turn OFF operation waveform for $V_{IN}$ = 25.2 V, $C_{SLEW}$ = 10 nF, no $C_{LOAD}$ , $R_{LOAD}$ = 100 Ω**

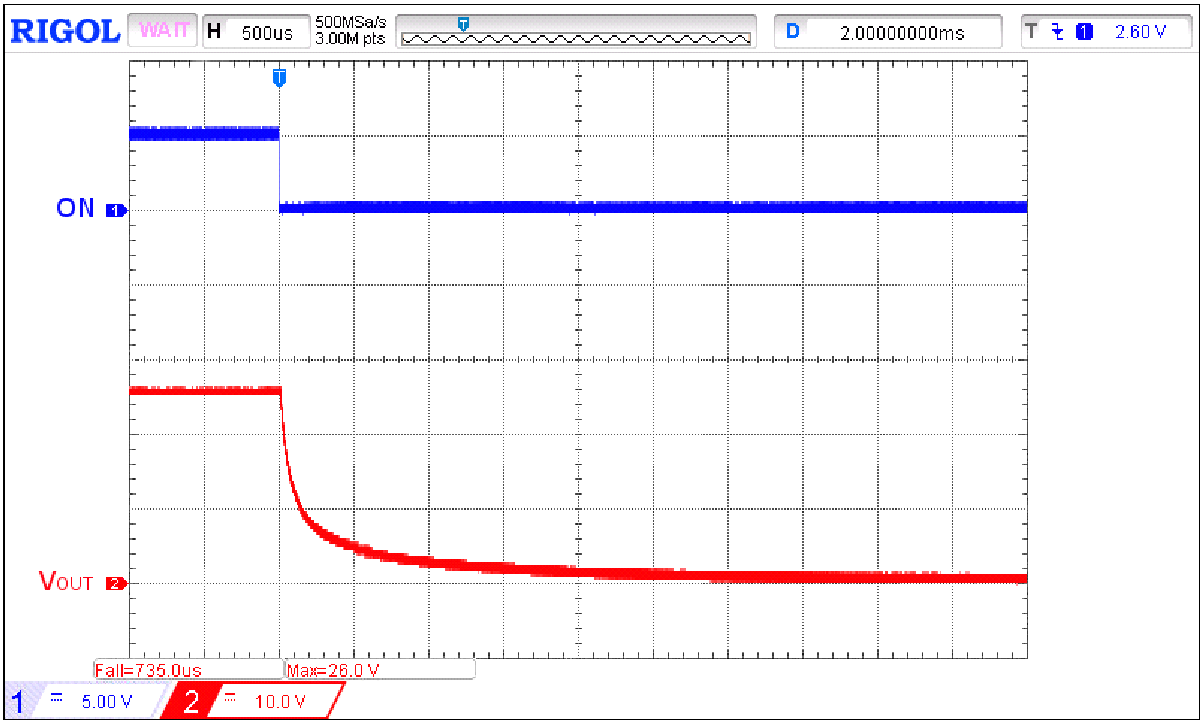



Figure 17. Typical Turn OFF operation waveform for $V_{IN}$ = 25.2 V, $C_{SLEW}$ = 10 nF, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 100 Ω

## Typical ACL Operation Waveforms

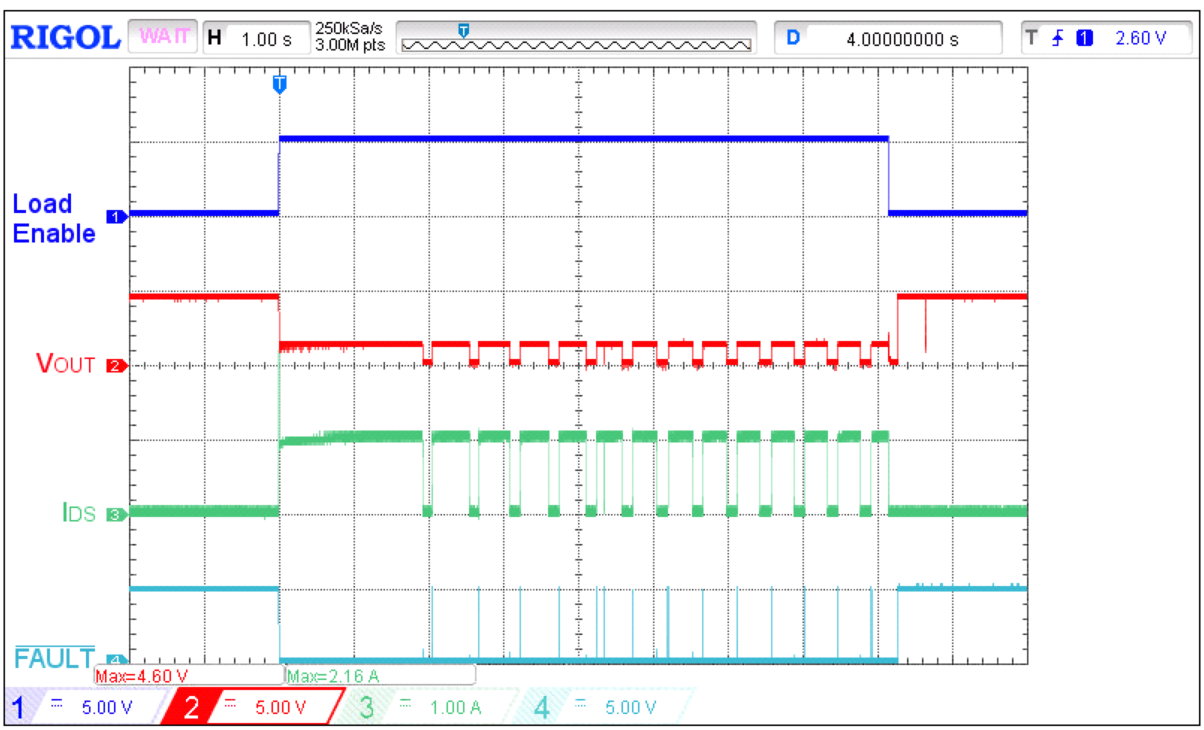



Figure 18. Typical ACL operation waveform for $V_{IN}$ = 4.5 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ

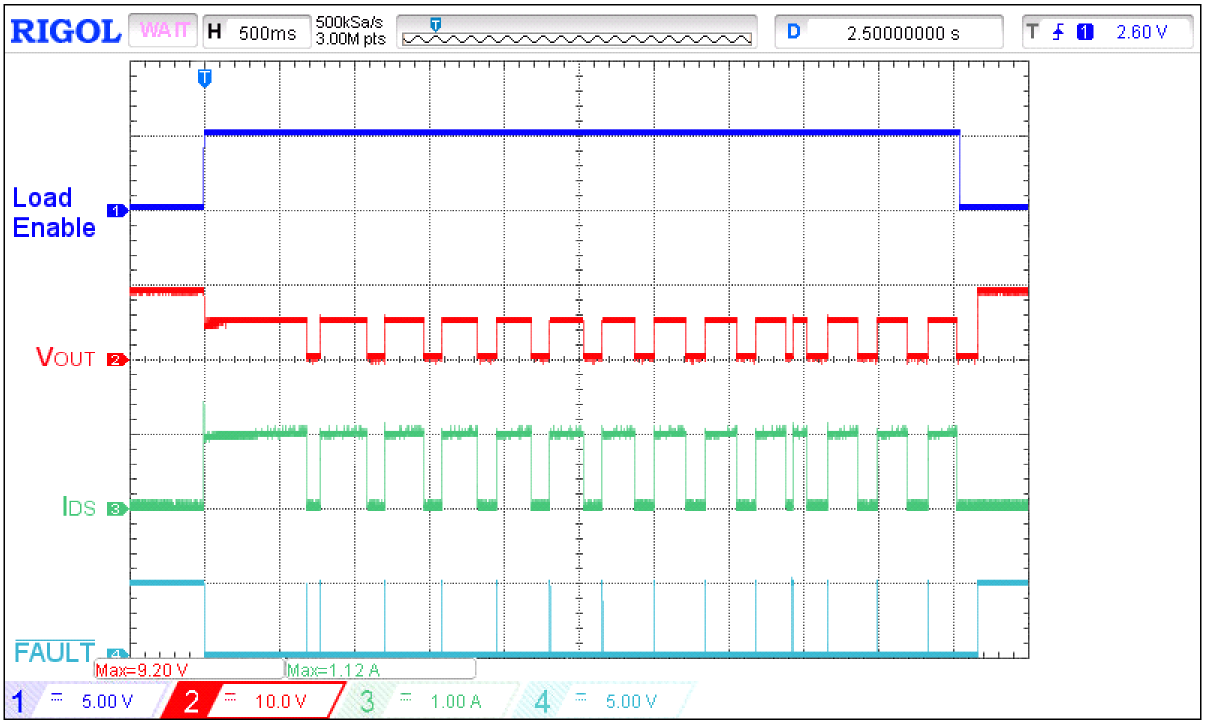



Figure 19. Typical ACL operation waveform for $V_{IN}$ = 9 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ

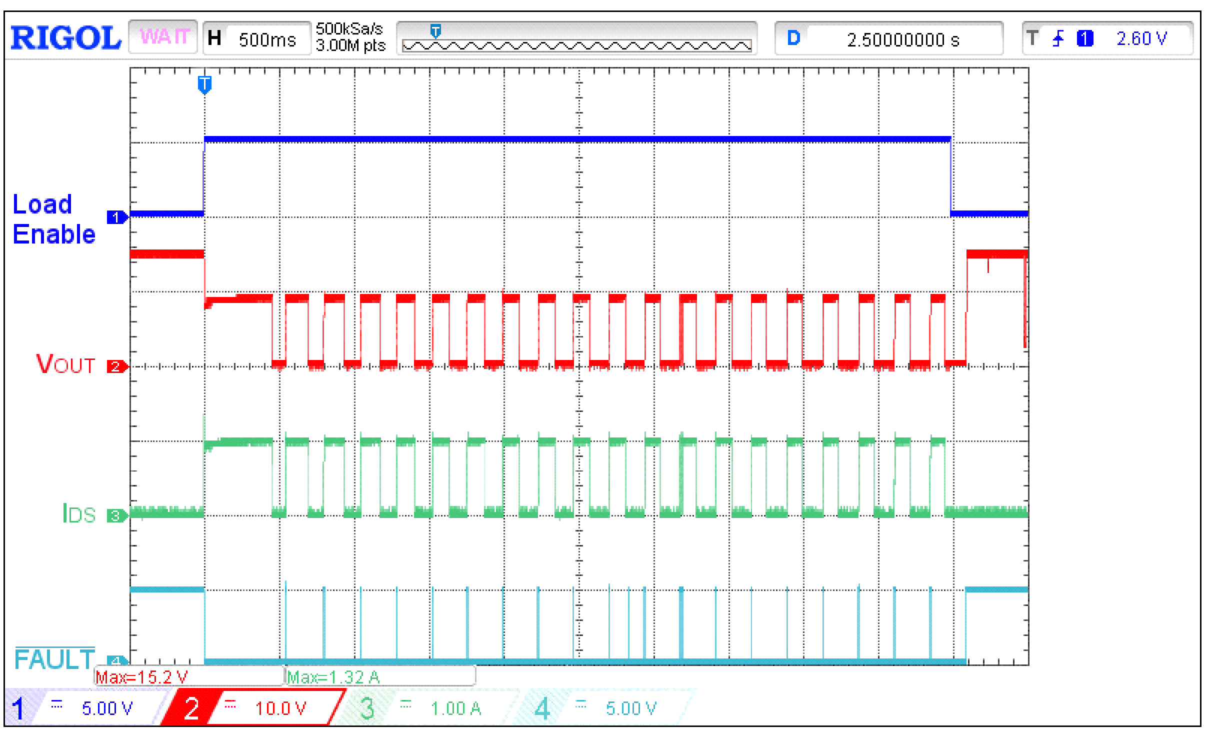



Figure 20. Typical ACL operation waveform for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ

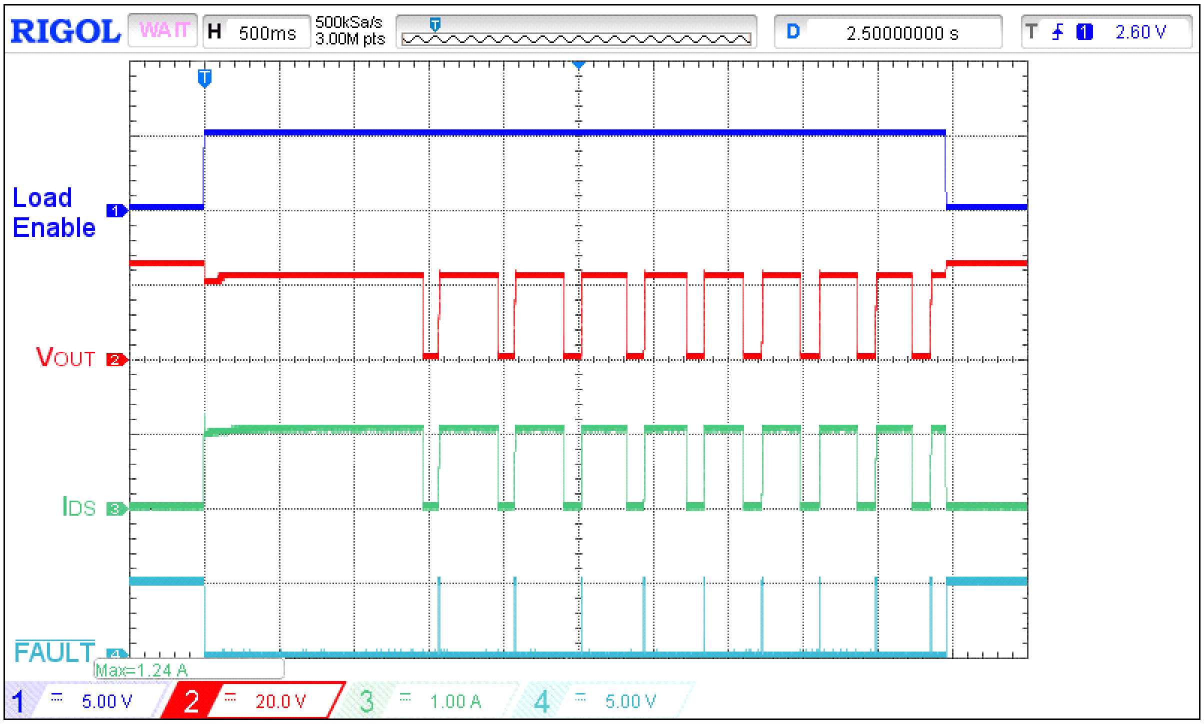



Figure 21. Typical ACL operation waveform for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ

## Typical FAULT Operation Waveforms

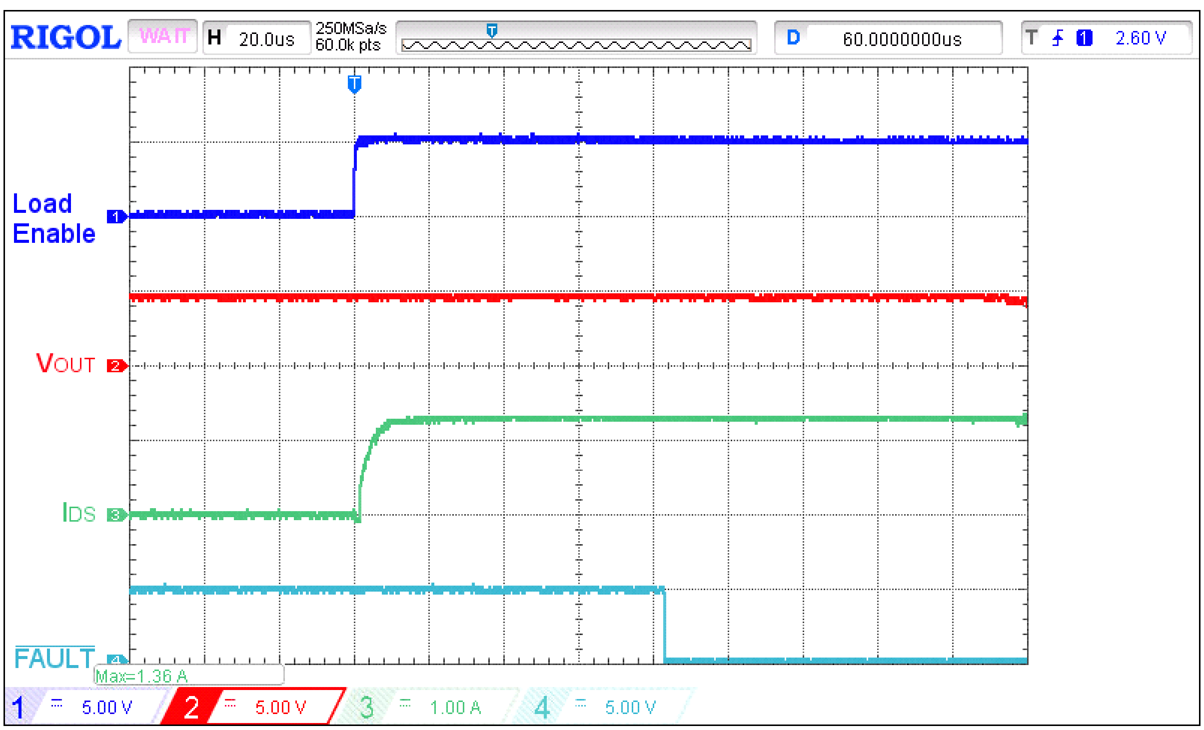



Figure 22. Typical FAULT assertion waveform for $V_{IN}$ = 4.5 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch on 3.3 Ω load

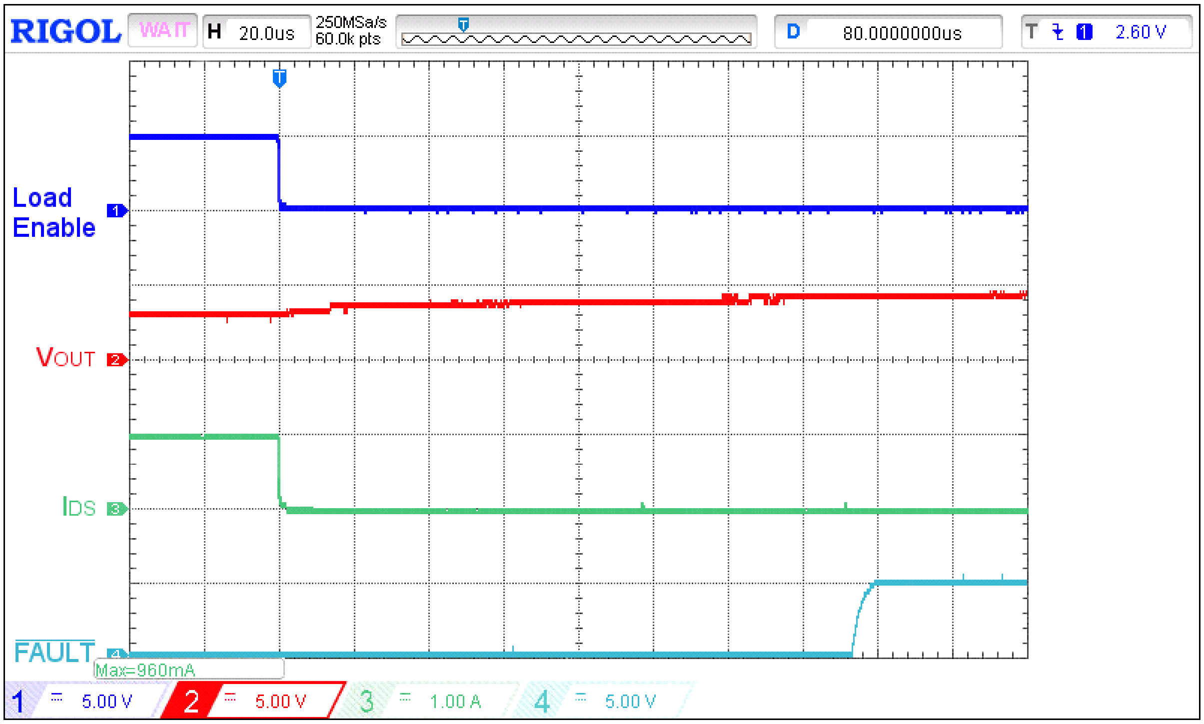



Figure 23. Typical FAULT de-assertion waveform for $V_{IN}$ = 4.5 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch out 3.3 Ω load

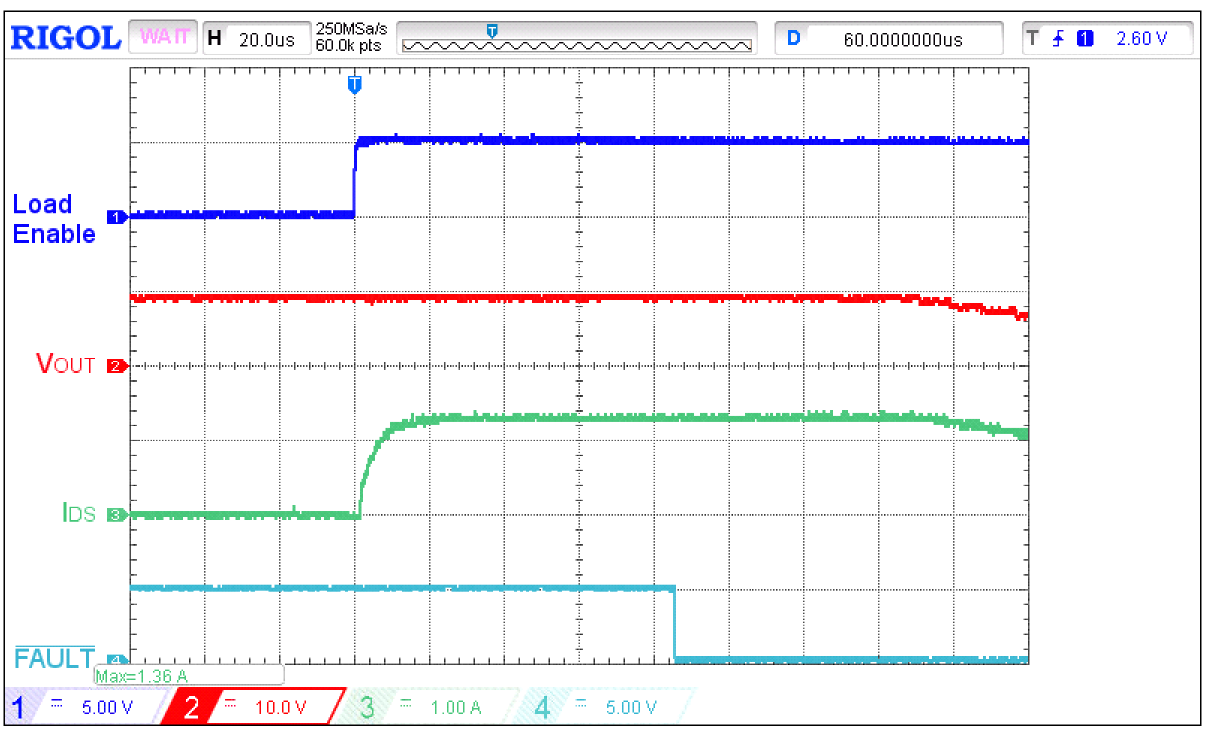



Figure 24. Typical FAULT assertion waveform for $V_{IN}$ = 9 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch on 6.6 Ω load

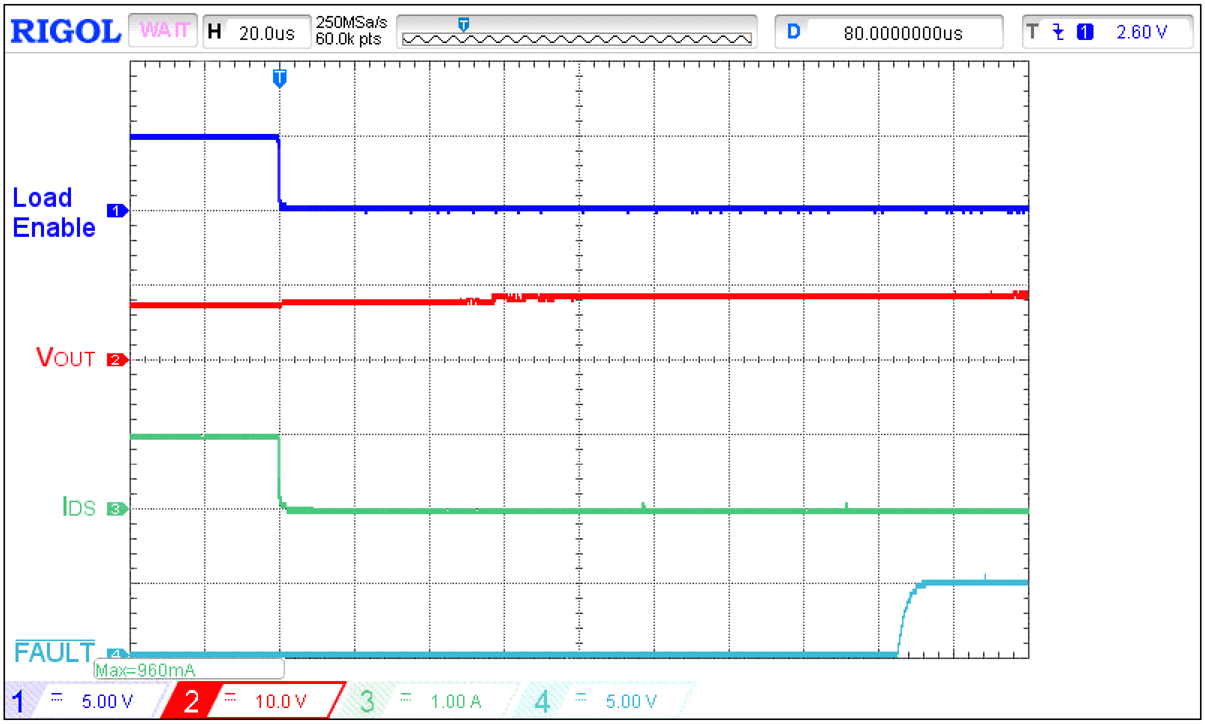



Figure 25. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{IN}$ = 9 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch out 6.6 Ω load

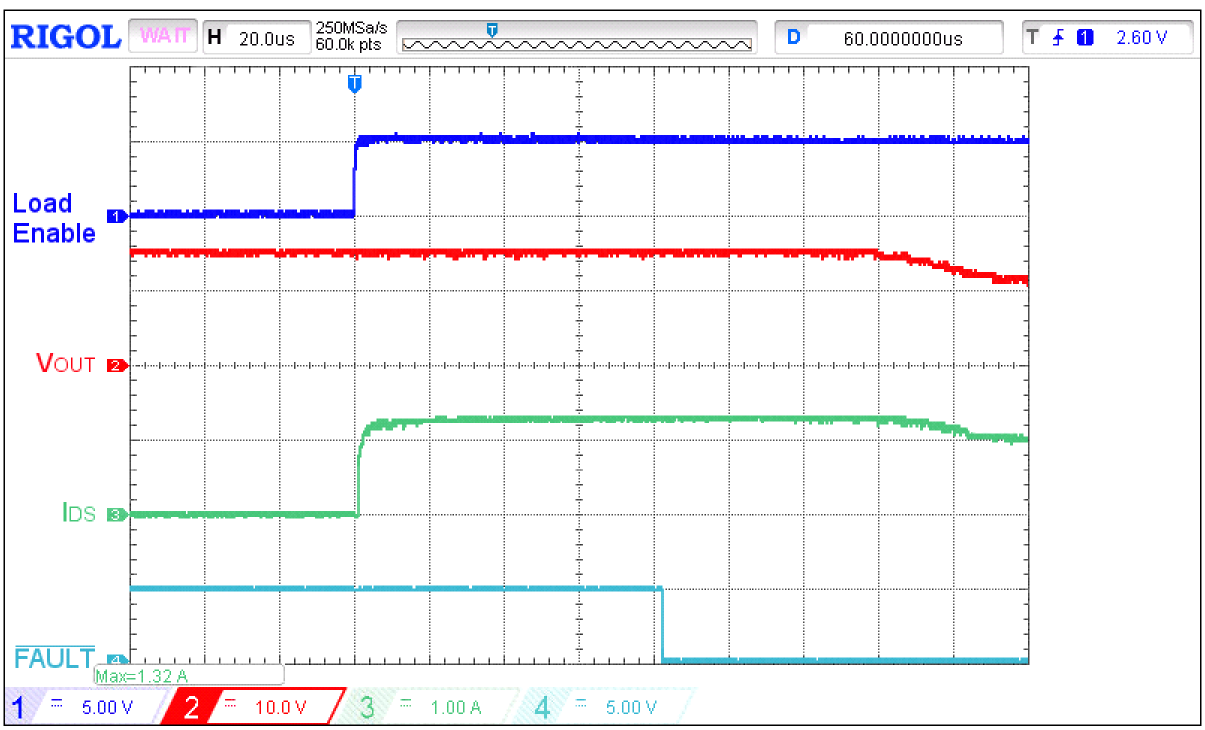



Figure 26. Typical $\overline{\text{FAULT}}$ assertion waveform for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch on 11.3 Ω load

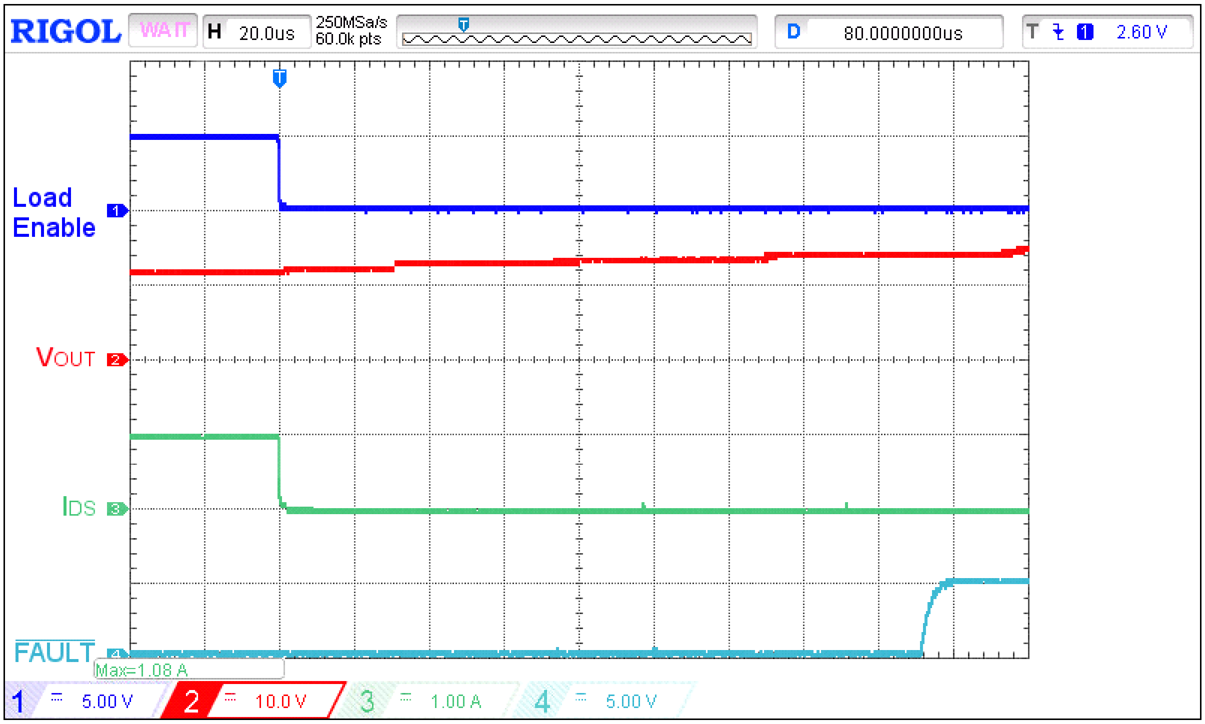



**Figure 27. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch out 11.3 Ω load**

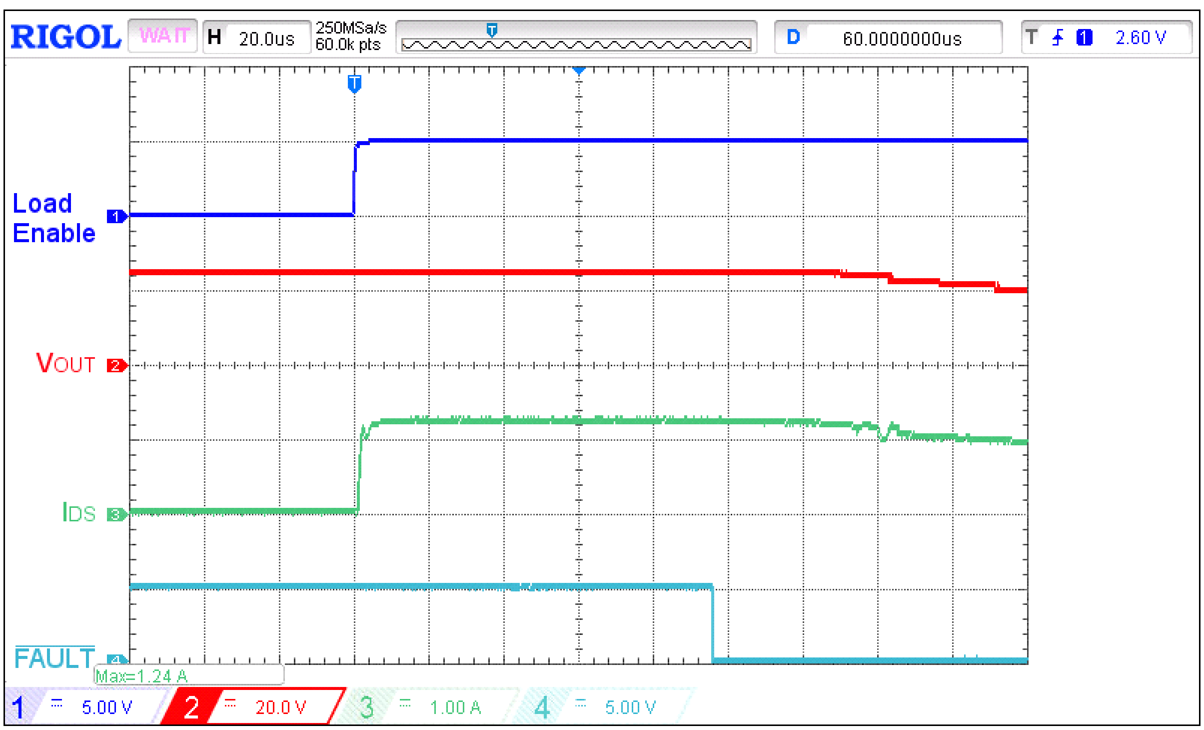



**Figure 28. Typical $\overline{\text{FAULT}}$ assertion waveform for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch on 20.5 Ω load**

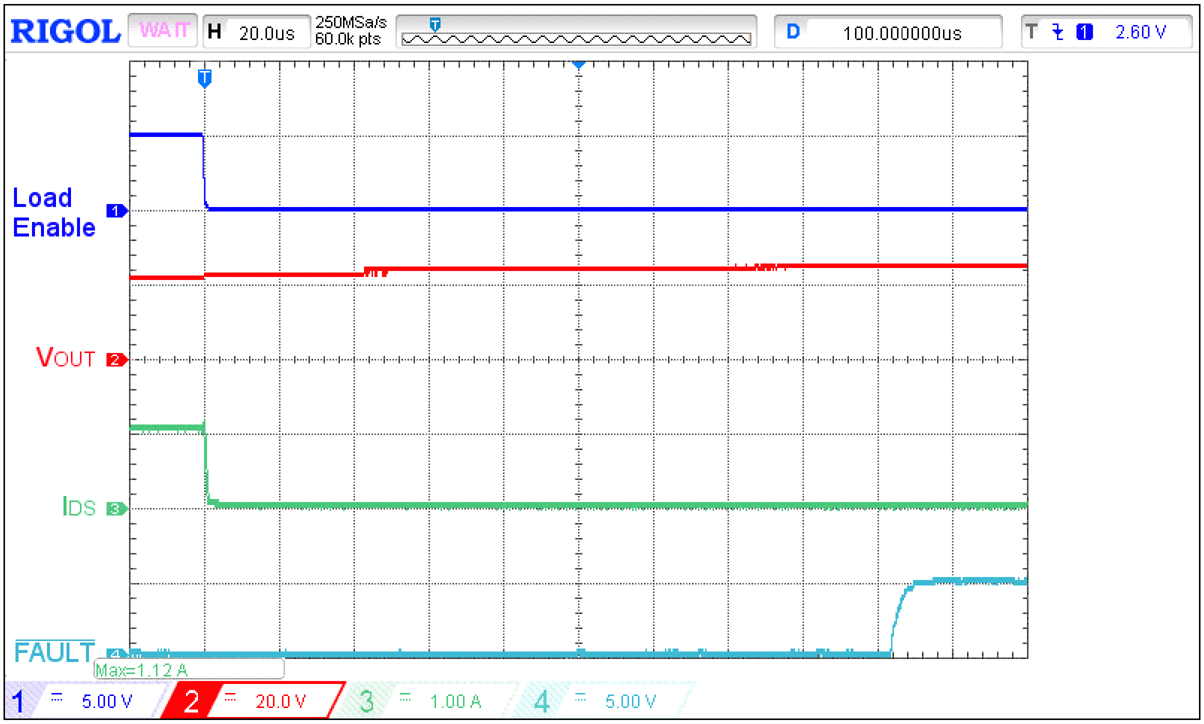



**Figure 29. Typical $\overline{\text{FAULT}}$ de-assertion waveform for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $I_{ACL}$ = 1 A, $R_{SET}$ = 91 kΩ, switch out 20.5 Ω load**

## Typical IOUT Response Time Waveforms

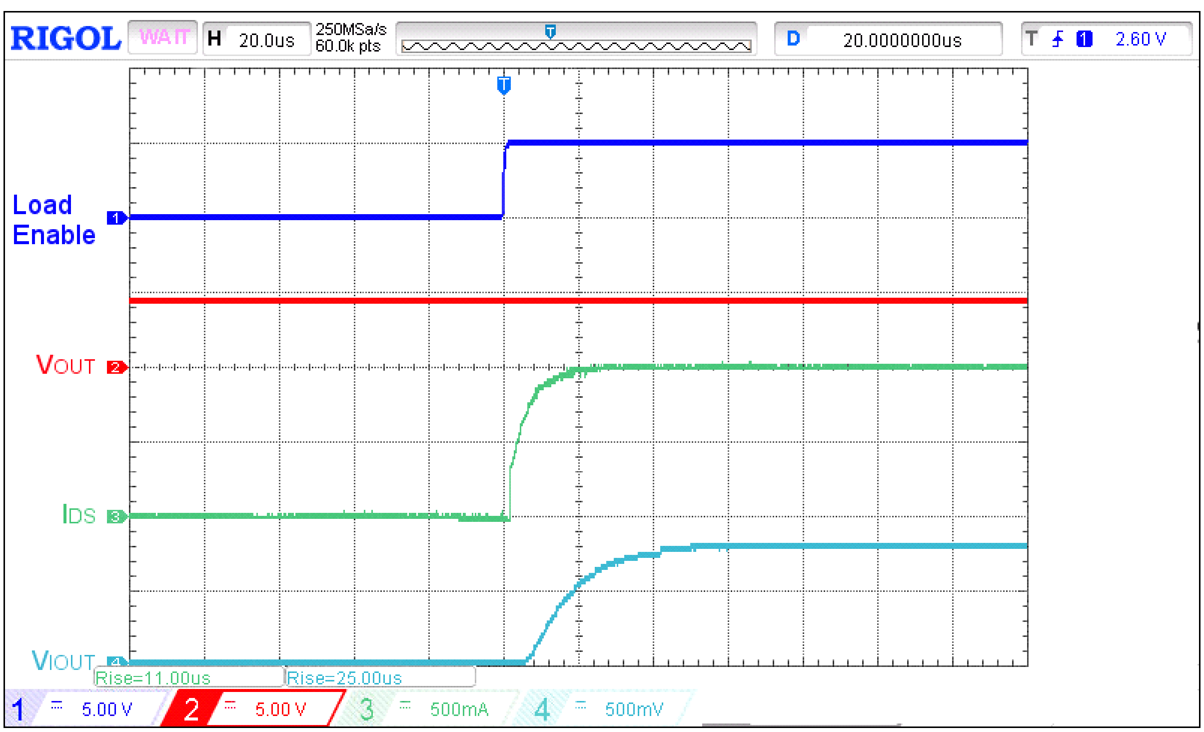



**Figure 30. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 4.5 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 4.5 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 0 A to 1 A**

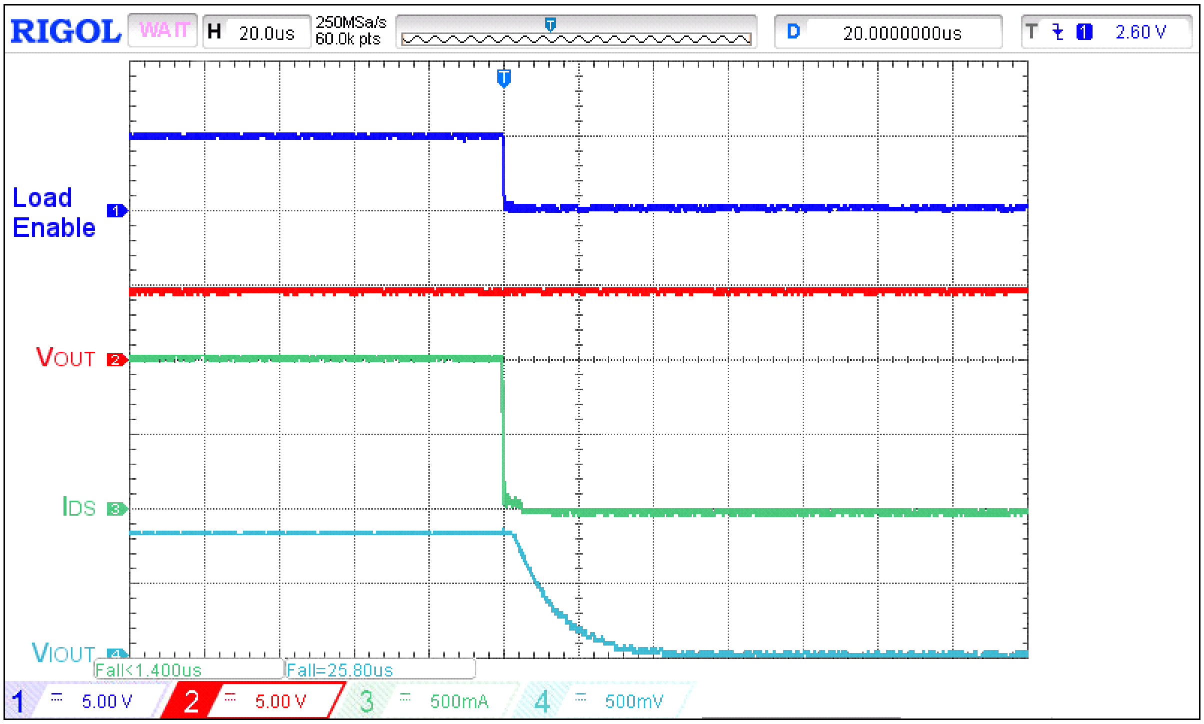



**Figure 31. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 4.5 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 4.5 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 1 A to 0 A**

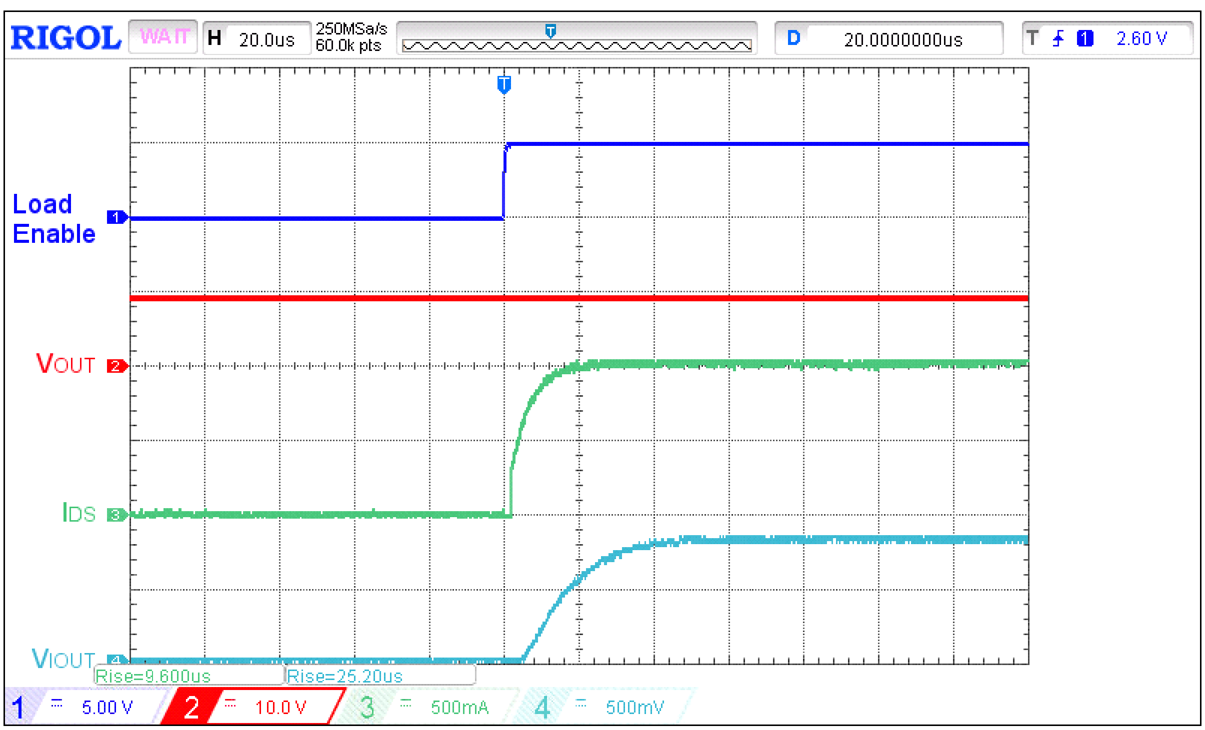



**Figure 32. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 9 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 9 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 0 A to 1 A**

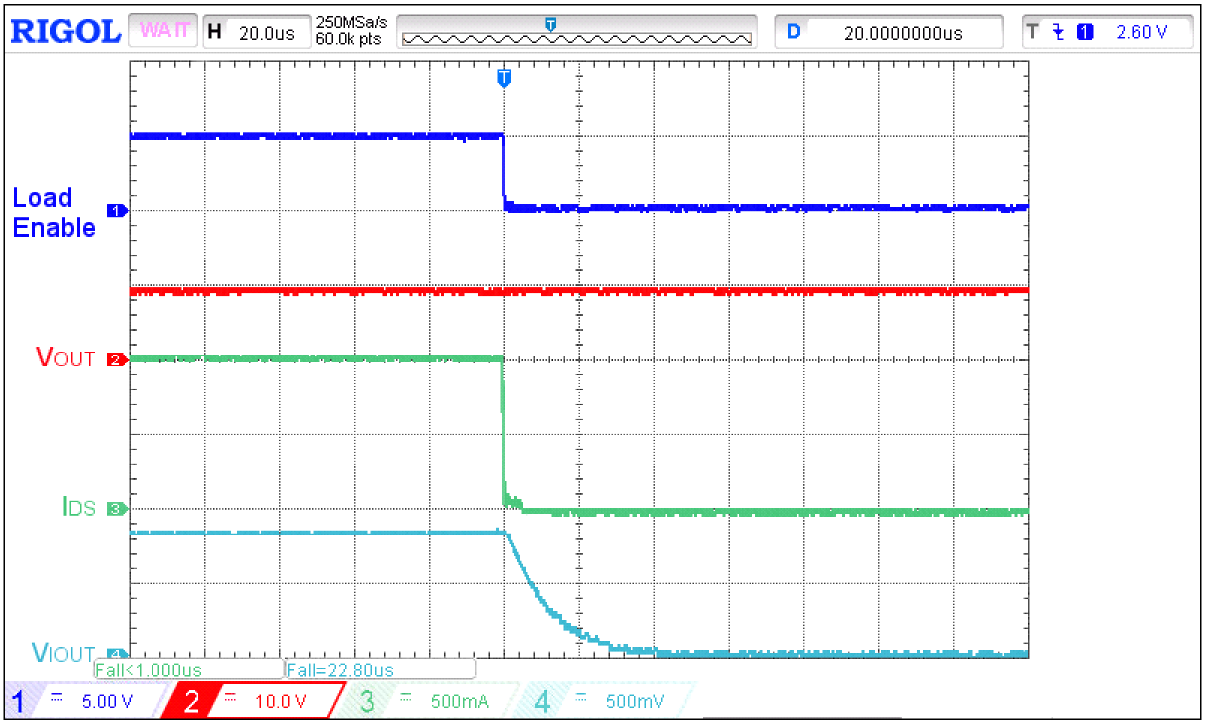



**Figure 33. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 9 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 9 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 1 A to 0 A**

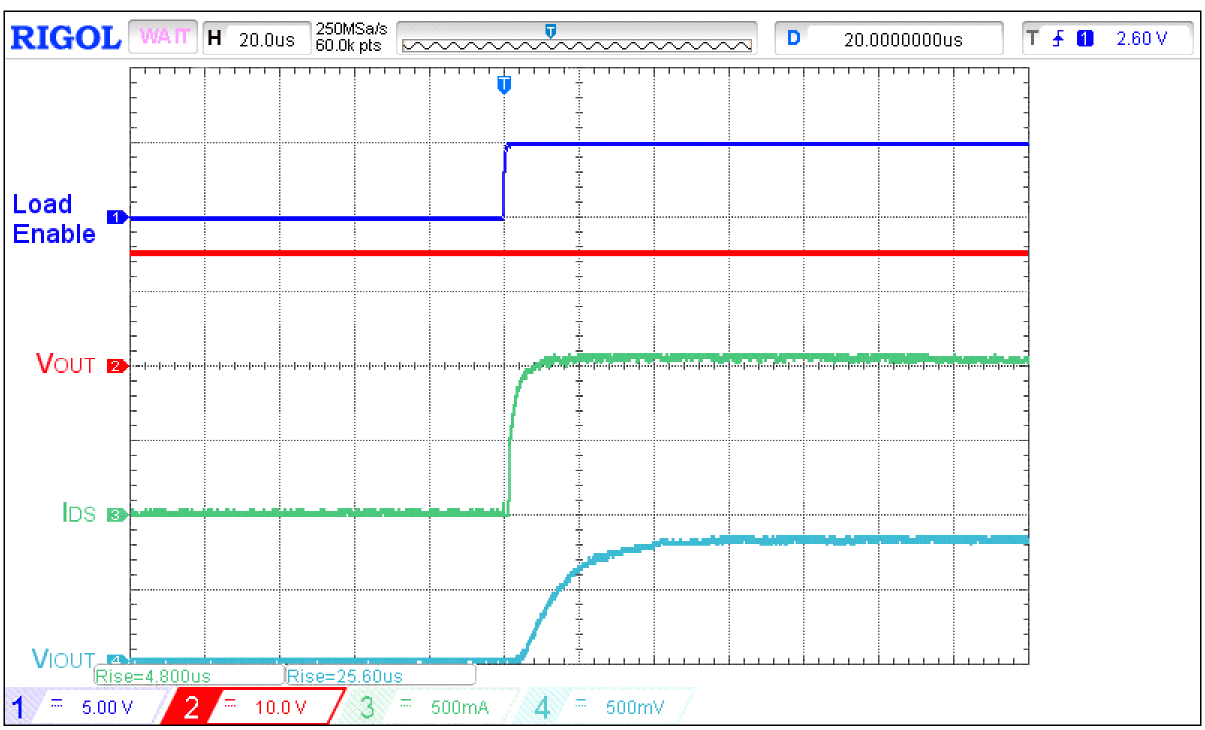



**Figure 34. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 15 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 0 A to 1 A**

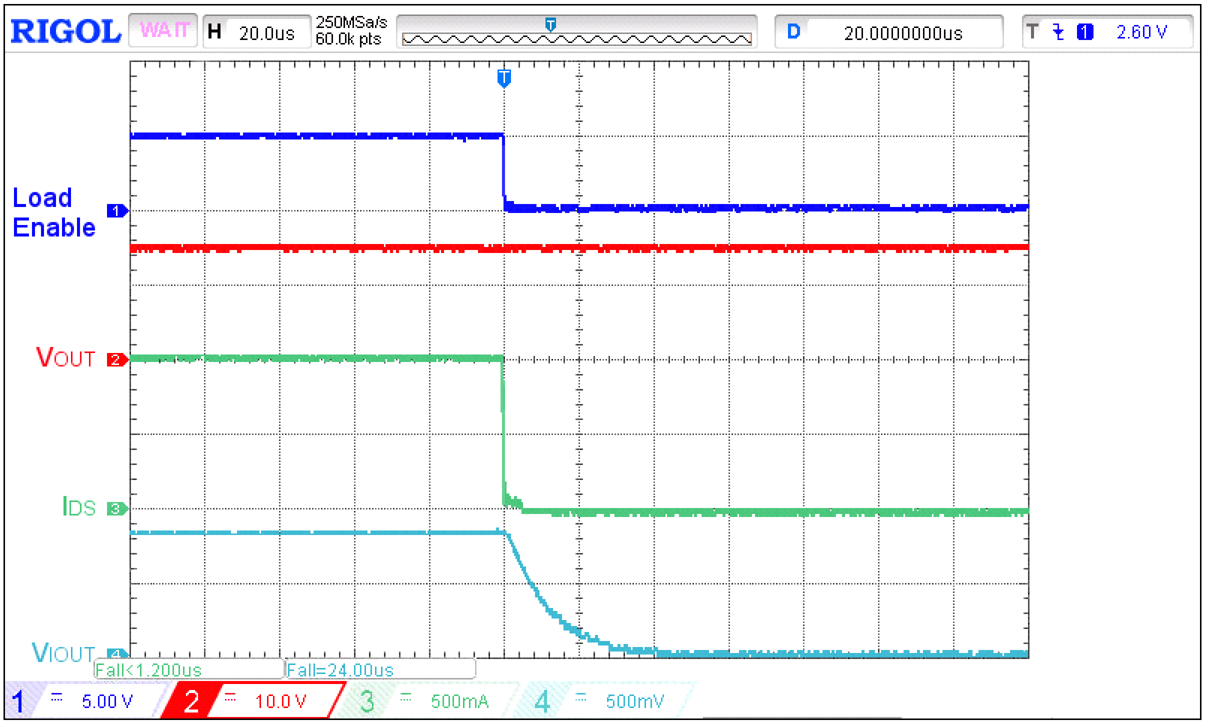



**Figure 35. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 15 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 1 A to 0 A**

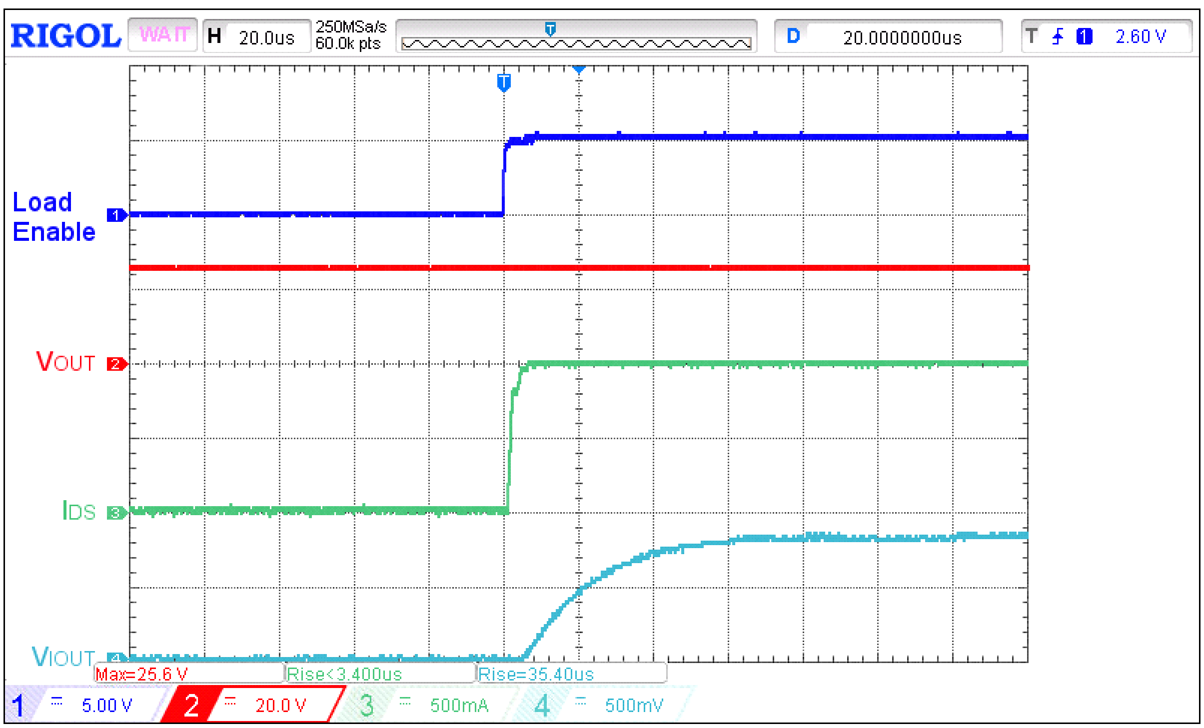



**Figure 36. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 25 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 0 A to 1 A**

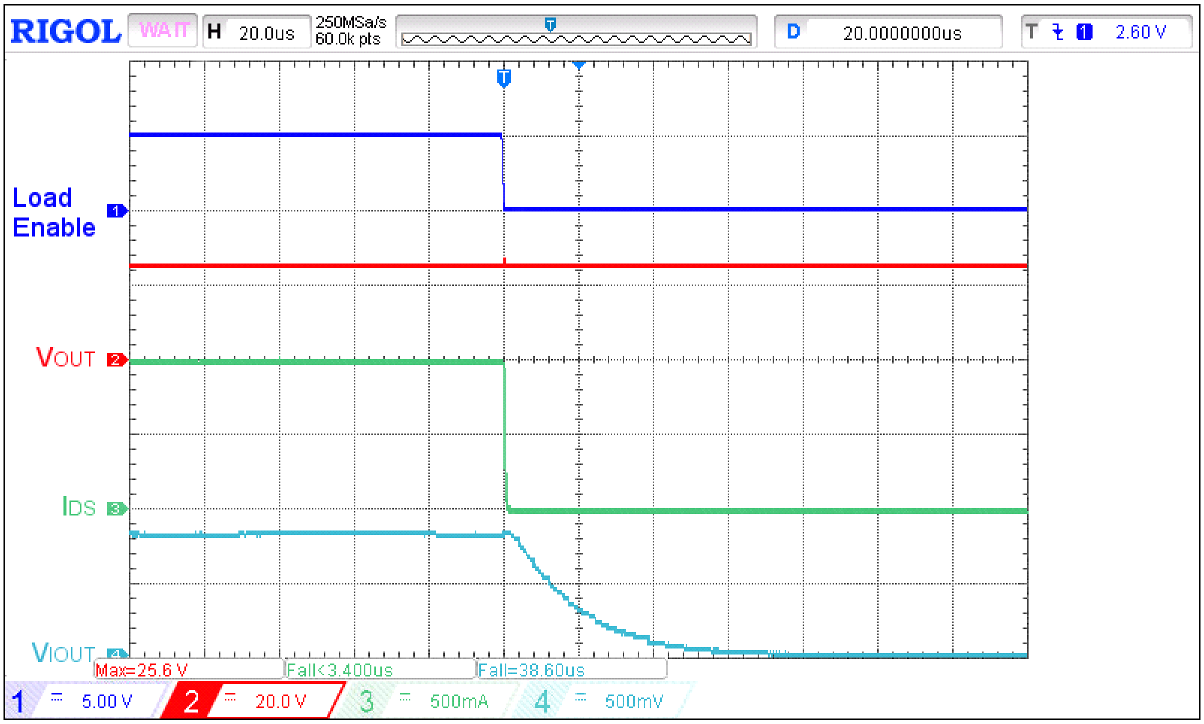



Figure 37. Typical $I_{OUT}$ response time waveform for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $R_{LOAD}$ = 25 Ω $C_{IOUT}$ = 0.18 nF, $R_{IOUT}$ = 84.5 kΩ, Load step 1 A to 0 A

## Typical SOA Waveforms

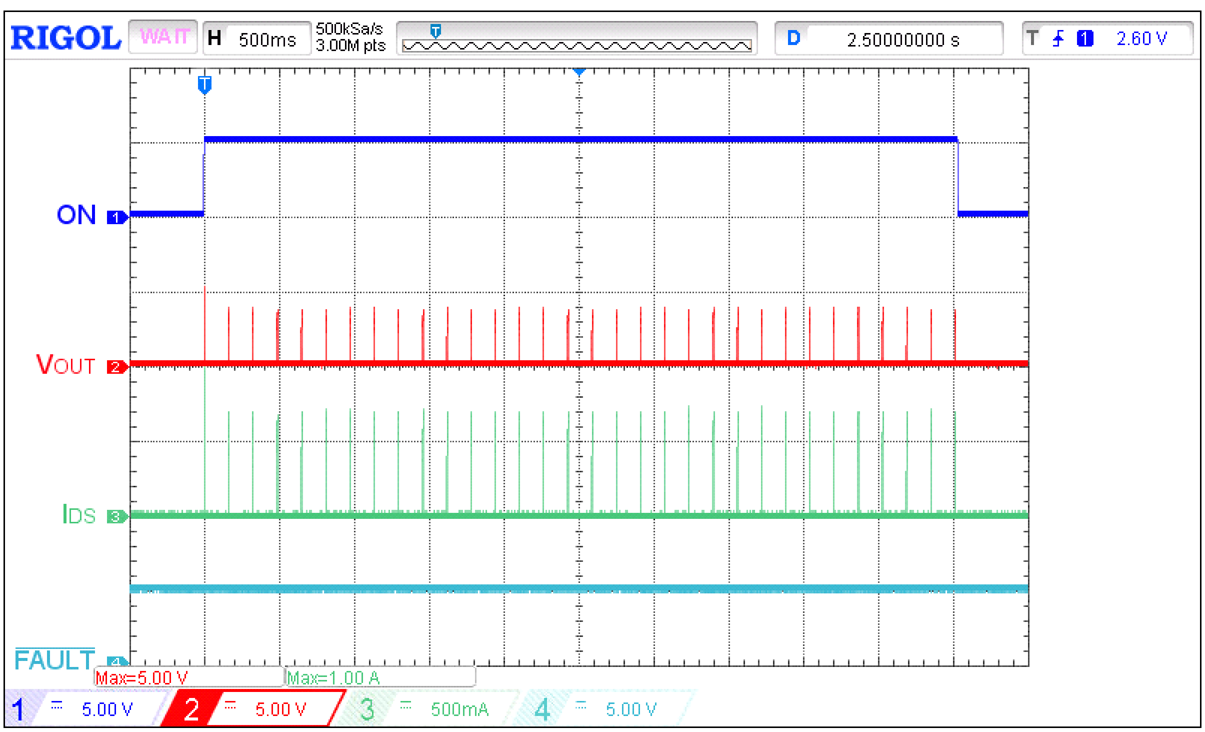



Figure 38. Typical SOA waveform during power up on heavy load for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $R_{SET}$ = 18 kΩ, $R_{LOAD}$ = 4.5 Ω

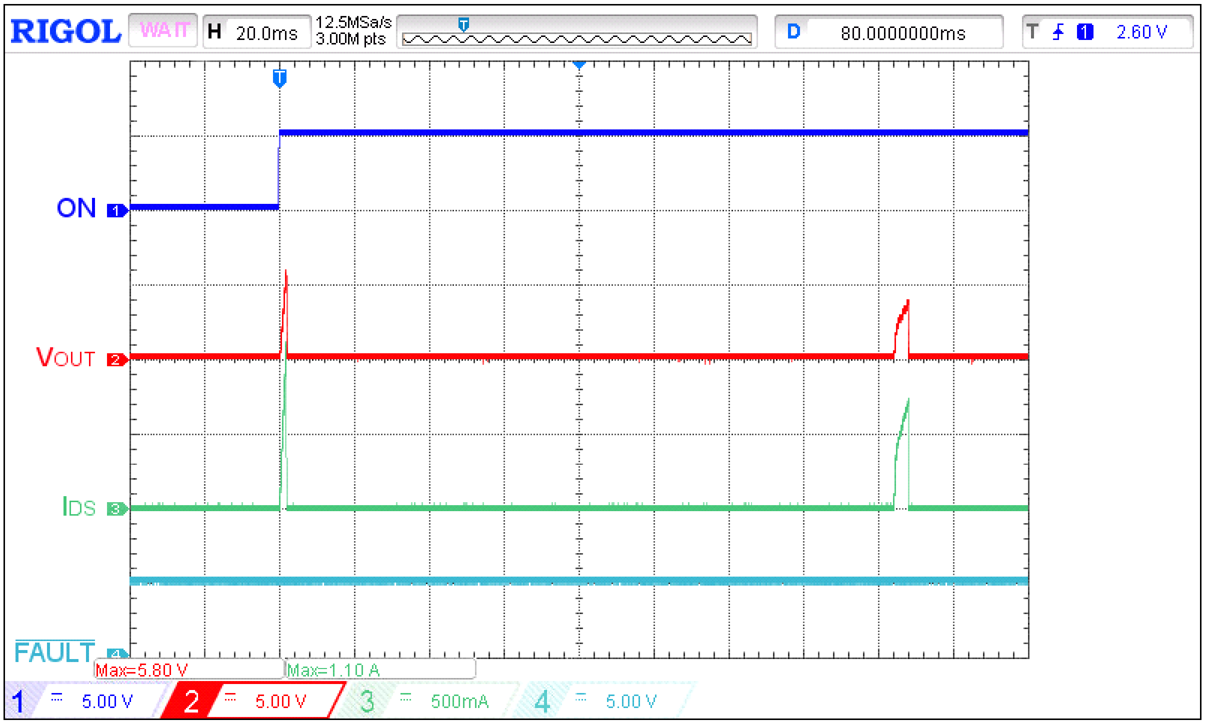



**Figure 39. Extended typical SOA waveform during power up under heavy load for $V_{IN}$ = 15 V, $C_{LOAD}$ = 10 µF, $R_{SET}$ = 18 kΩ, $R_{LOAD}$ = 4.5 Ω**

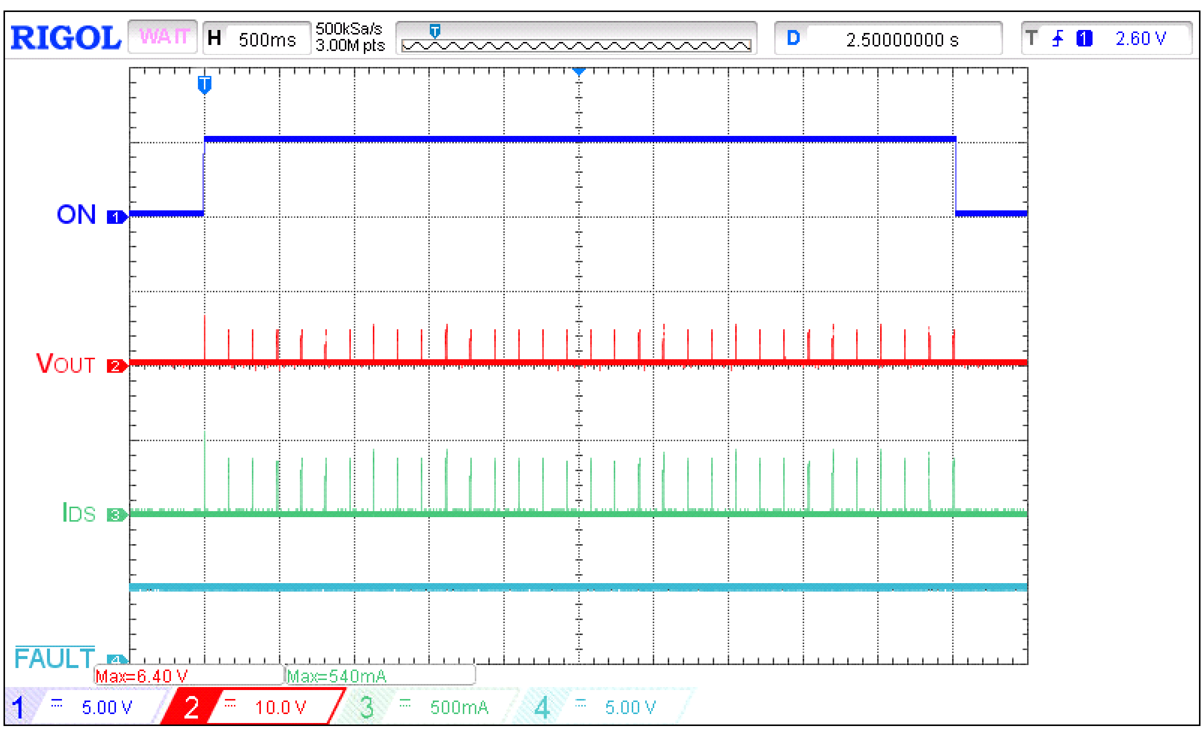



**Figure 40. Typical SOA waveform during power up under heavy load for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $R_{SET}$ = 18 kΩ, $R_{LOAD}$ = 12 Ω**

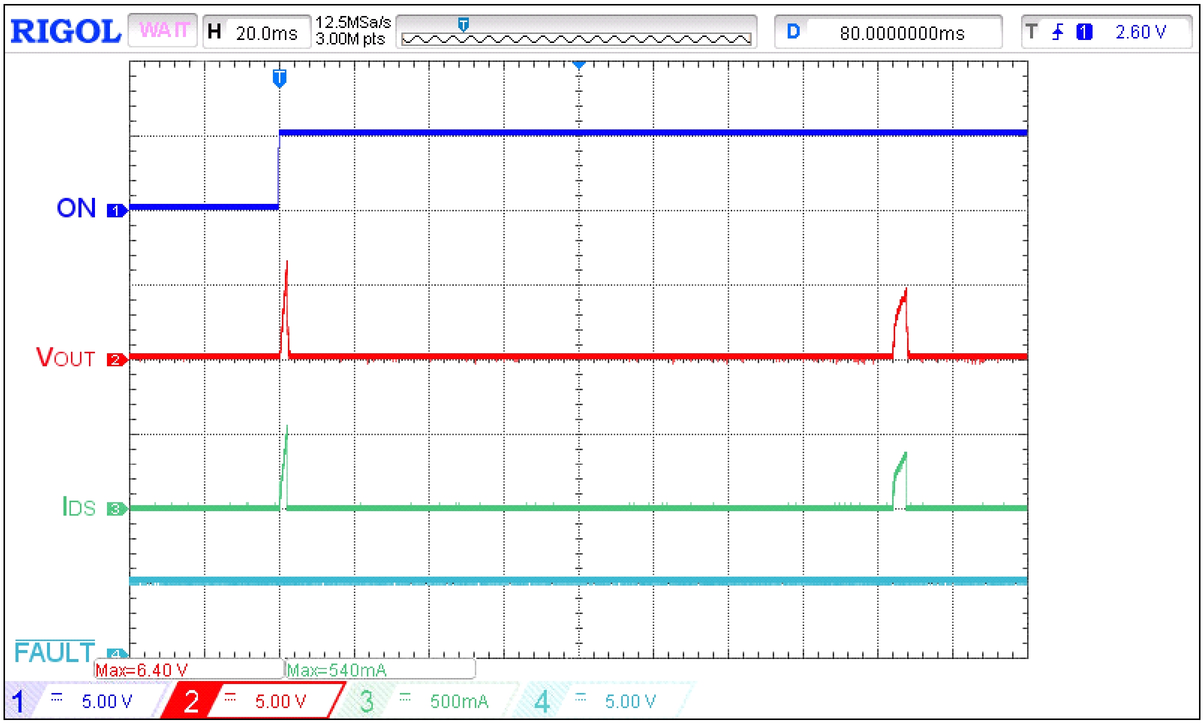



**Figure 41. Extended typical SOA waveform during power up under heavy load for $V_{IN}$ = 25.2 V, $C_{LOAD}$ = 10 µF, $R_{SET}$ = 18 kΩ, $R_{LOAD}$ = 12 Ω**

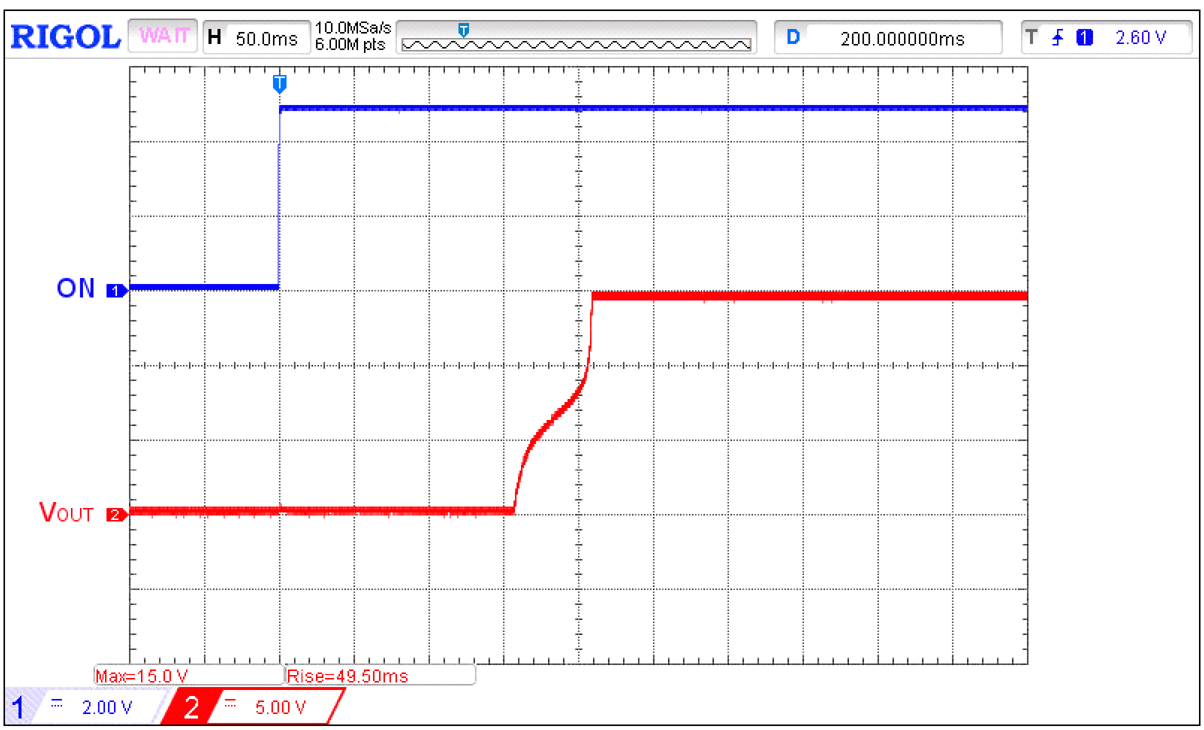



**Figure 42. Typical non-monotonic $V_{OUT}$ ramping waveform during power up on heavy load for $V_{IN}$ = 15 V, $C_{LOAD}$ = 470 µF, $C_{SLEW}$ = 10nF, $R_{SET}$ = 18 kΩ, $R_{LOAD}$ = 9.6 Ω**

# Applications Information

## High Voltage GreenFET Safe Operating Area Explained

Renesas's High Voltage GreenFET load switches incorporate a number of internal protection features that prevents them from damaging themselves or any other circuit or subcircuit downstream of them. One particular protection feature is their Safe Operation Area (SOA) protection. SOA protection is automatically activated under overpower and, in some cases, under overcurrent conditions. Overpower SOA is activated if package power dissipation exceeds an internal 10 W threshold and High Voltage GreenFET devices will quickly switch off (open circuit) upon overpower detection and automatically resume (close) nominal operation once overpower condition no longer exists.

One of the possible ways to have an overpower condition trigger SOA protection is when High Voltage GreenFET products are enabled into heavy output resistive loads and/or into large load capacitors. It is under these conditions to follow carefully the "Safe Start-up Loading" guidance in the Applications section of the datasheet. During an overcurrent condition, High Voltage GreenFET devices will try to limit the output current to the level set by the external $R_{SET}$ resistor. Limiting the output current, however, causes an increased voltage drop across the FET's channel because the FET's $RDS_{ON}$ increased as well. Since the FET's $RDS_{ON}$ is larger, package power dissipation also increases. If the resultant increase in package power dissipation is higher/equal than 10 W, internal SOA protection will be triggered and the FET will open circuit (switch off). Every time SOA protection is triggered, all High Voltage GreenFET devices will automatically attempt to resume nominal operation after 160 ms. The automatic retry attempt only allows power-up with SOA at 5 W. This SOA fold back power ensures that the FET survives a short circuit condition. To clear the 5 W SOA fold back, switch the ON pin to "LOW" to power reset SOA to 10 W.

## Safe Start-up Condition

SLG59H1019V has built-in protection to prevent over-heating during start-up into a heavy load. Overloading the VOUT pin with a capacitor and a resistor may result in non-monotonic $V_{OUT}$ ramping (Figure 42) or repeated restarts (Figure 38 to Figure 41). In general, under light loading on VOUT, $V_{OUT}$ ramping can be controlled with $C_{SLEW}$ value. The following equation serves as a guide:

$$C_{SLEW} = \frac{T_{RISE}}{V_{IN}} \times 4.9\,\mu A \times \frac{20}{3}$$

where
$T_{RISE}$ = Total rise time from 10% $V_{OUT}$ to 90% $V_{OUT}$
$V_{IN}$ = Input Voltage
$C_{SLEW}$ = Capacitor value for CAP pin

When capacitor and resistor loading on VOUT during start up, the following tables will ensure $V_{OUT}$ ramping is monotonic without triggering internal SOA protection:

| Safe Start-up Loading for $V_{IN}$ = 15 V (Monotonic Ramp) | | | |
|---|---|---|---|
| **Slew Rate (V/ms)** | **$C_{SLEW}$ (nF)[2]** | **$C_{LOAD}$ (µF)** | **$R_{LOAD}$ (Ω)** |
| 1 | 33.3 | 500 | 12 |
| 2 | 16.7 | 250 | 12 |
| 3 | 11.1 | 160 | 12 |
| 4 | 8.3 | 120 | 12 |
| 5 | 6.7 | 100 | 12 |

| Safe Start-up Loading for $V_{IN}$ = 25.2 V (Monotonic Ramp) | | | |
|---|---|---|---|
| Slew Rate (V/ms) | $C_{SLEW}$ (nF)[2] | $C_{LOAD}$ (µF) | $R_{LOAD}$ (Ω) |
| 0.5 | 66.7 | 500 | 60 |
| 1.0 | 33.3 | 250 | 60 |
| 1.5 | 22.2 | 160 | 60 |
| 2.0 | 16.7 | 120 | 60 |
| 2.5 | 13.3 | 100 | 60 |

Note 2: Select the closest-value tolerance capacitor.

### Setting the SLG59H1019V's Active Current Limit

| $R_{SET}$ (kΩ) | Active Current Limit (A)[3] |
|---|---|
| 91 | 1 |
| 45 | 2 |
| 30 | 3 |
| 18 | 5 |

Note 3: Active Current Limit accuracy is ±15% over voltage range and over temperature range.

### Power Dissipation

The junction temperature of the SLG59H1019V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG59H1019V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = RDS_{ON} \times I_{DS}^2$$

where:

PD = Power dissipation, in Watts (W)
$RDS_{ON}$ = Power MOSFET ON resistance, in Ohms (Ω)
$I_{DS}$ = Output current, in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

$T_J$ = Junction temperature, in Celsius degrees (°C)
$\theta_{JA}$ = Package thermal resistance, in Celsius degrees per Watt (°C/W)
$T_A$ = Ambient temperature, in Celsius degrees (°C)

In current-limit mode, the SLG59H1019V's power dissipation can be calculated by taking into account the voltage drop across the load switch ($V_{IN}$-$V_{OUT}$) and the magnitude of the output current in current-limit mode ($I_{ACL}$):

$$PD = (V_{IN} - V_{OUT}) \times I_{ACL} \text{ or}$$

$$PD = (V_{IN} - (R_{LOAD} \times I_{ACL})) \times I_{ACL}$$

where:

PD = Power dissipation, in Watts (W)
$V_{IN}$ = Input Voltage, in Volts (V)
$R_{LOAD}$ = Load Resistance, in Ohms (Ω)
$I_{ACL}$ = Output limited current, in Amps (A)
$V_{OUT}$ = $R_{LOAD}$ x $I_{ACL}$

## Layout Guidelines:

1. Since the VIN and VOUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 43, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input $C_{IN}$ and output $C_{LOAD}$ low-ESR capacitors as close as possible to the SLG59H1019V's VIN and VOUT pins;

3. The GND pin should be connected to system analog or power ground plane.

4. 2 oz. copper is recommended for high current operation.

## SLG59H1019V Evaluation Board:

A High Voltage GreenFET Evaluation Board for SLG59H1019V is designed according to the statements above and is illustrated on Figure 43. Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for $RDS_{ON}$ evaluation.

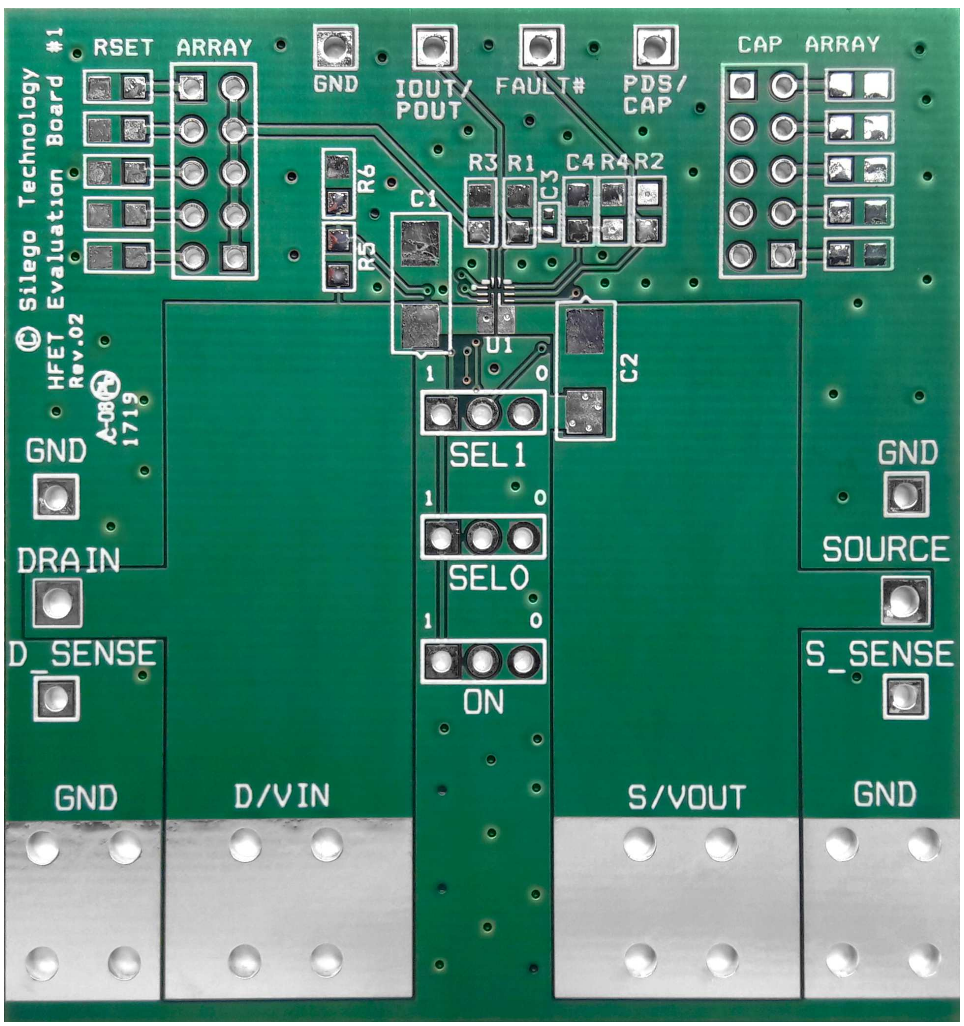



**Figure 43. SLG59H1019V Evaluation Board**

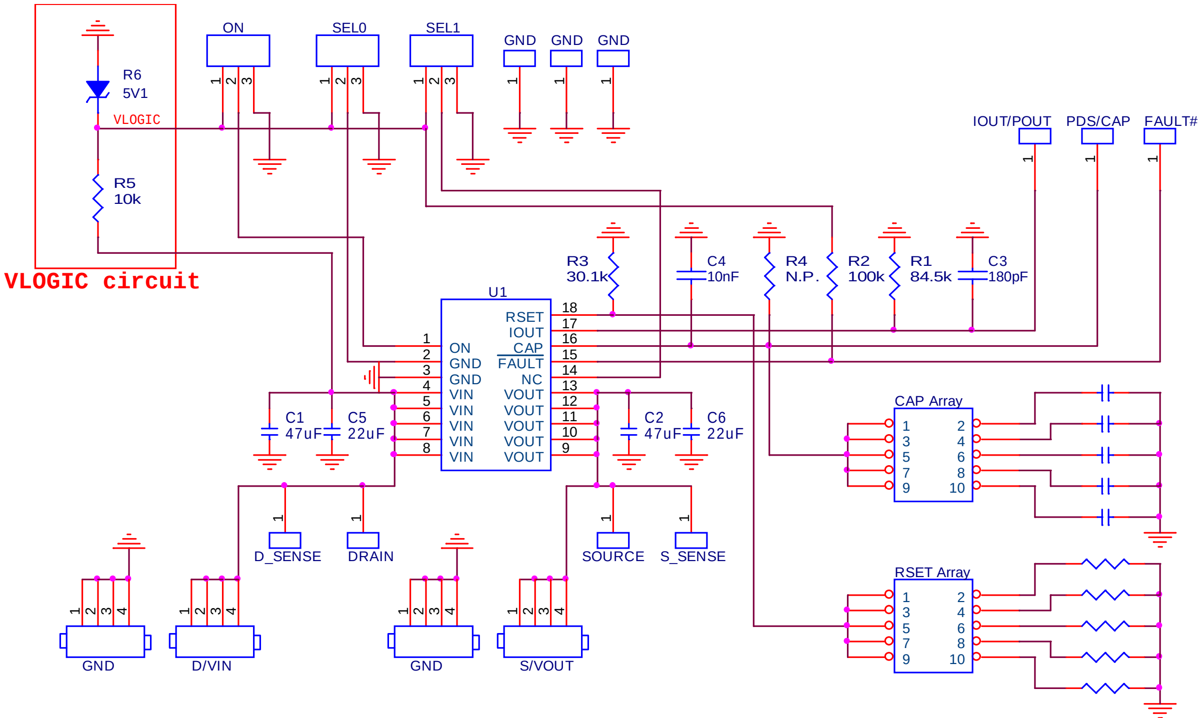


Figure 44. SLG59H1019V Evaluation Board Connection Circuit

## Basic Test Setup and Connections

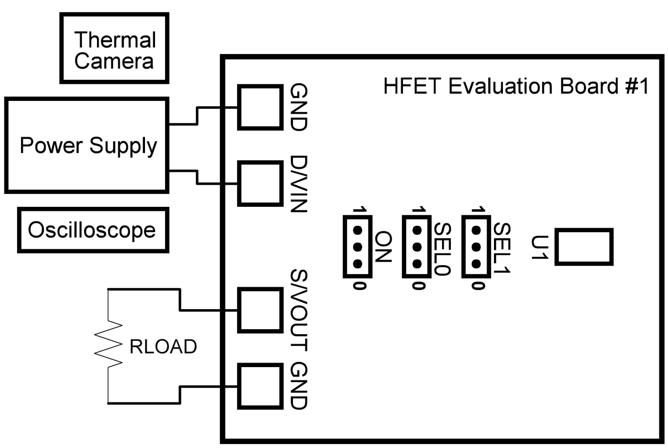


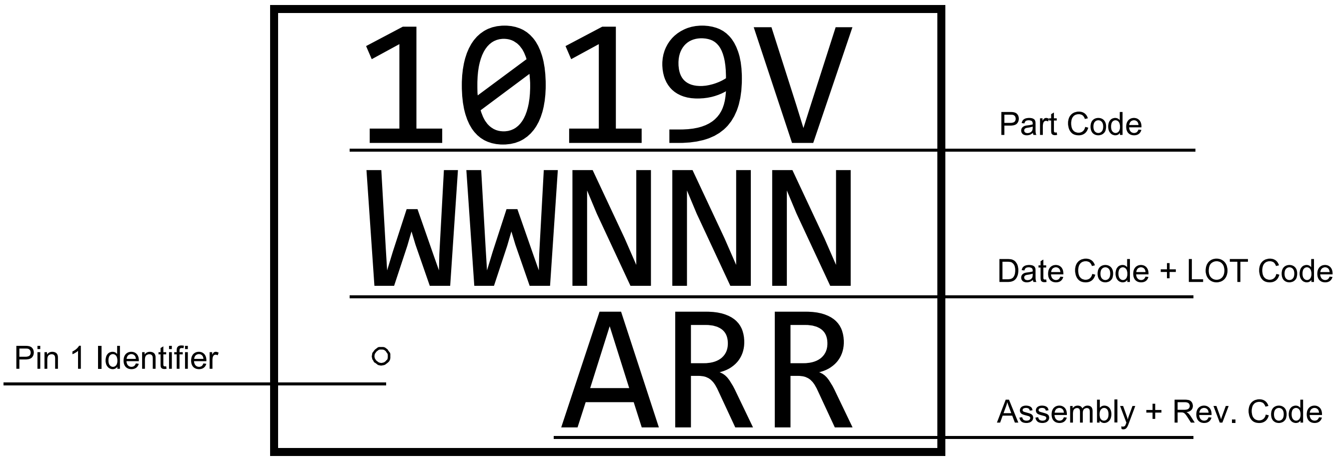

Figure 45. SLG59H1019V Evaluation Board Connection Circuit

**EVB Configuration**

1. Set SEL0 to GND and leave SEL1 floating;
2. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
3. Turn on Power Supply and set desired $V_{IN}$ from 4.5 V ... 25.2 V;
4. Toggle the ON signal High or Low to observe SLG59H1019V operation.

### Package Top Marking System Definition

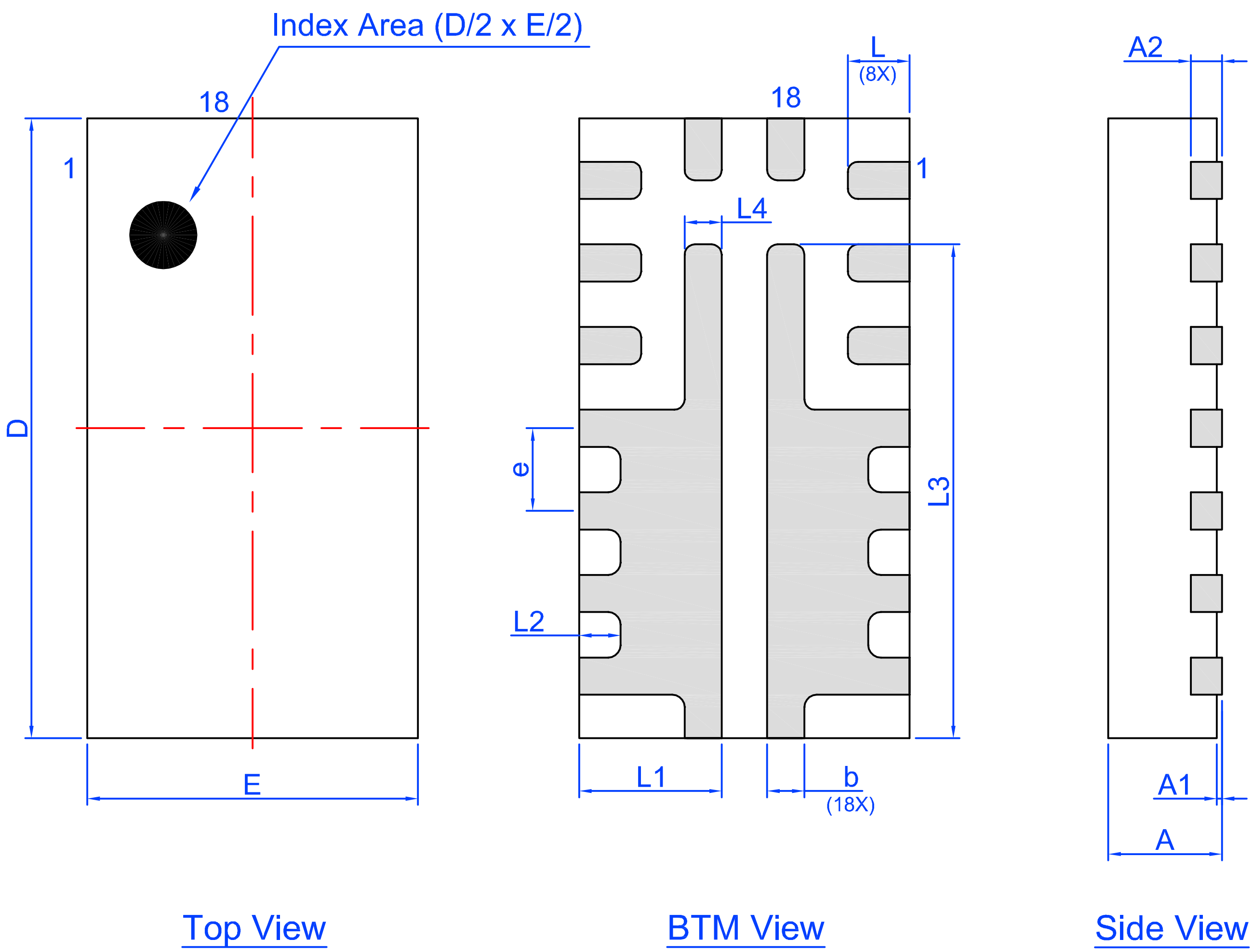



1019V - Part ID Field
WW - Date Code Field[1]
NNN - Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

## Package Drawing and Dimensions

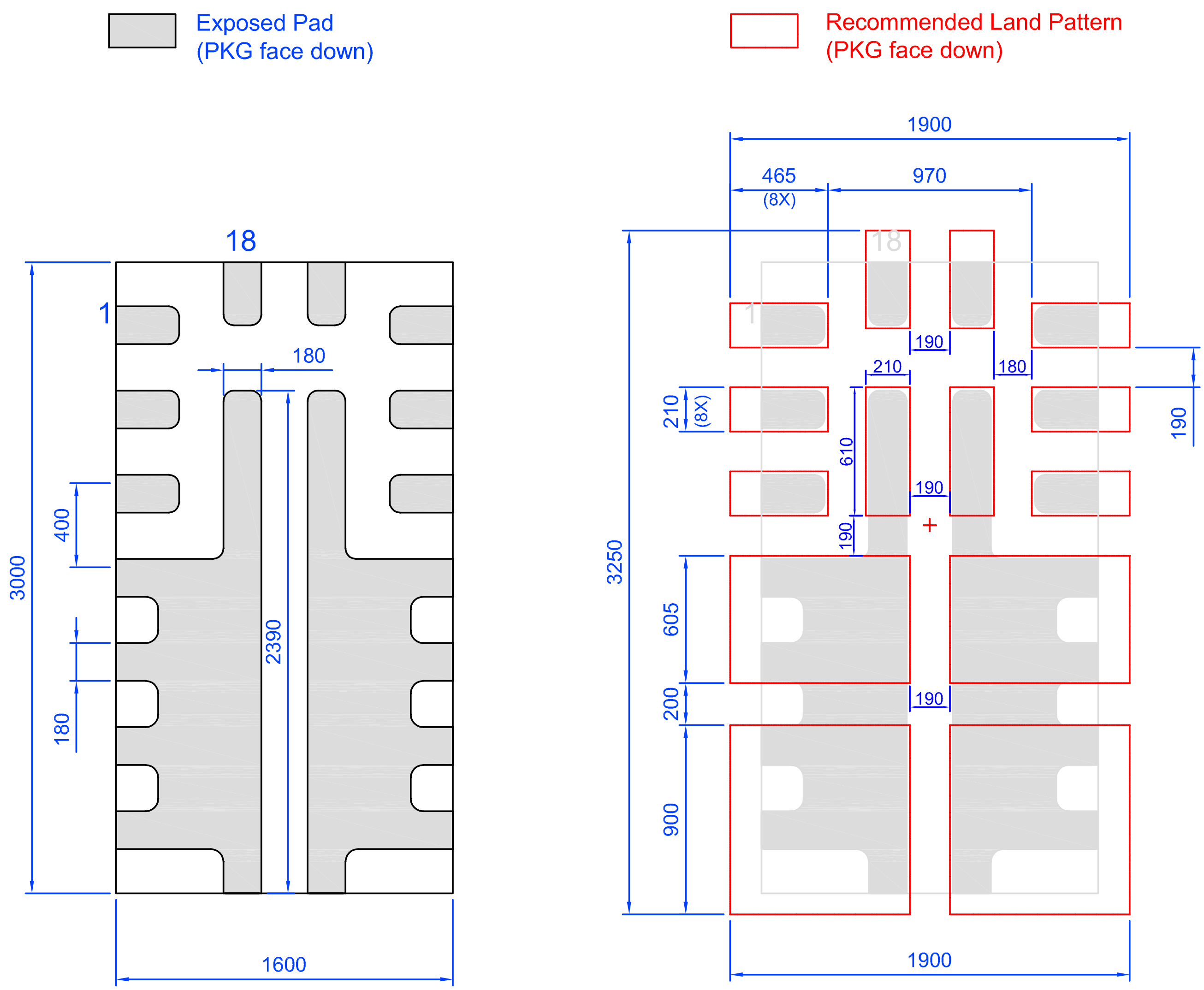
**18 Lead TQFN Package 1.6 x 3 mm (Fused Lead)**
**JEDEC MO-220, Variation WCEE**




Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|---|---|---|---|---|---|---|---|
| A | 0.50 | 0.55 | 0.60 | D | 2.95 | 3.00 | 3.05 |
| A1 | 0.005 | - | 0.05 | E | 1.55 | 1.60 | 1.65 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.25 | 0.30 | 0.35 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.64 | 0.69 | 0.74 |
| e | 0.40 BSC | | | L2 | 0.15 | 0.20 | 0.25 |
| L3 | 2.34 | 2.39 | 2.44 | L4 | 0.13 | 0.18 | 0.23 |

### SLG59H1019V 18-pin STQFN PCB Landing Pattern



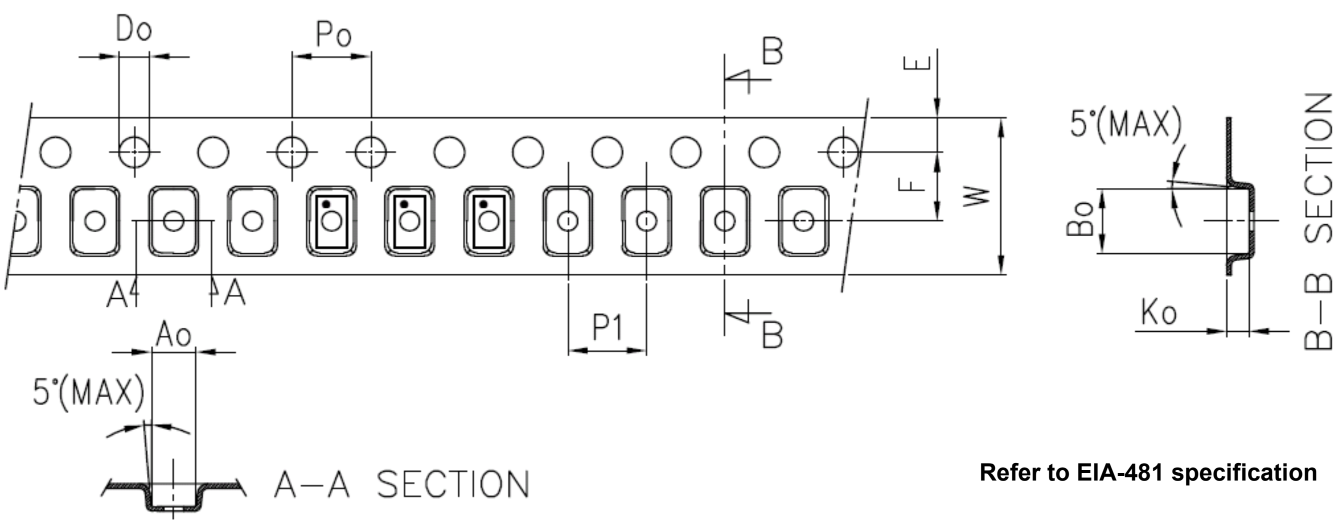

Note: All dimensions shown in micrometers (µm)

## Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STQFN 18L 0.4P FC Green | 18 | 1.6 x 3 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

## Carrier Tape Drawing and Dimensions

| Package Type | PocketBTM Length | PocketBTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|---|---|---|---|---|---|---|---|---|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STQFN 18L 0.4P FC Green | 1.78 | 3.18 | 0.76 | 4 | 4 | 1.5 | 1.75 | 3.5 | 8 |




**Refer to EIA-481 specification**

## Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 $mm^3$ (nominal). More information can be found at www.jedec.org.

## Revision History

| Date | Version | Change |
|---|---|---|
| 2/2/2022 | 1.04 | Updated Company name and logo<br>Added SOA Protection Threshold to Features<br>Fixed typos |
| 10/17/2019 | 1.03 | Updated Applications Info SOA Description<br>Updated HFET Evaluation Board image |
| 12/19/2018 | 1.02 | Updated Charts<br>Added Layout Guidelines<br>Fixed typos |
| 7/19/2018 | 1.01 | Updated style and formatting |
| 12/15/2017 | 1.00 | Production Release |

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com



### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.