A Surge-protected, 28 V Tolerant Power Splitter in WLCSP

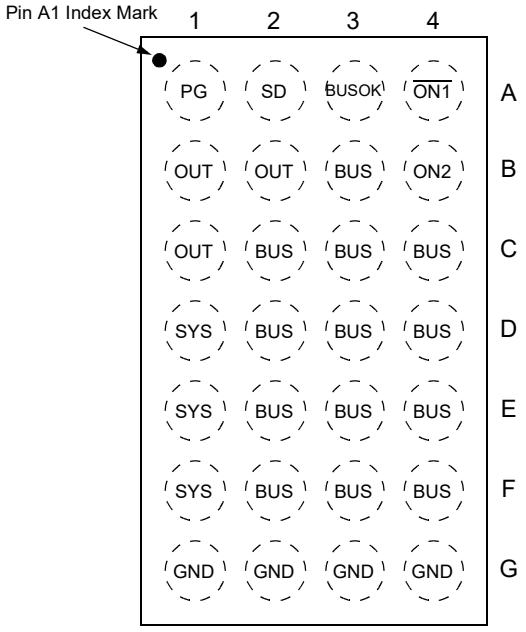
General Description

The SLG59H1302C is a 130-V surge-protected, 28-V tolerant power splitter with two high-current switches and a 0.1 A capable LDO in 28-ball WLCSP. With independent control for each channel, the SLG59H1302C contains a 6 A capable, 12 mΩ nFET switch for the BUS-to-OUT path and a reverse-blocking 6 A capable, 24 mΩ nFET switch for the BUS-to-SYS path. An internal, "always ON" LDO is 0.1 A capable and can be used to supply power to downstream devices when the BUS terminal voltage is higher than 2.7 V. When the SYS terminal turns on, the IC's push-pull PG output becomes asserted. The SLG59H1302C is fully specified over the industrial -40 °C to 85 °C temperature range.

Features

- 130 V-tolerant TVS (IEC61000-4-5)
- BUS-to-OUT nFET: 12 mΩ/6 A, 28 V tolerant
- BUS-to-SYS nFET: 24 mΩ/6 A B2B RB
- Always ON, BUS LDO: ±10% tol, 0.1 A capable
- BUS UVLO & OVLO Protection
  - OVP Response Time: 200 ns
- Push-pull PG (Power Good) Output
- Thermal Shutdown Protection
- Active-HIGH IC Shutdown Input
- Active-LOW $\overline{ON1}$ Input (BUS-to-OUT)
- Active-HIGH ON2 Input (BUS-to-SYS)
- 28-ball CSP, 2.98 x 1.69 x 0.44 mm, 0.4 mm pitch
- Pb-Free / Halogen-Free / RoHS Compliant Packaging

Pin Configuration

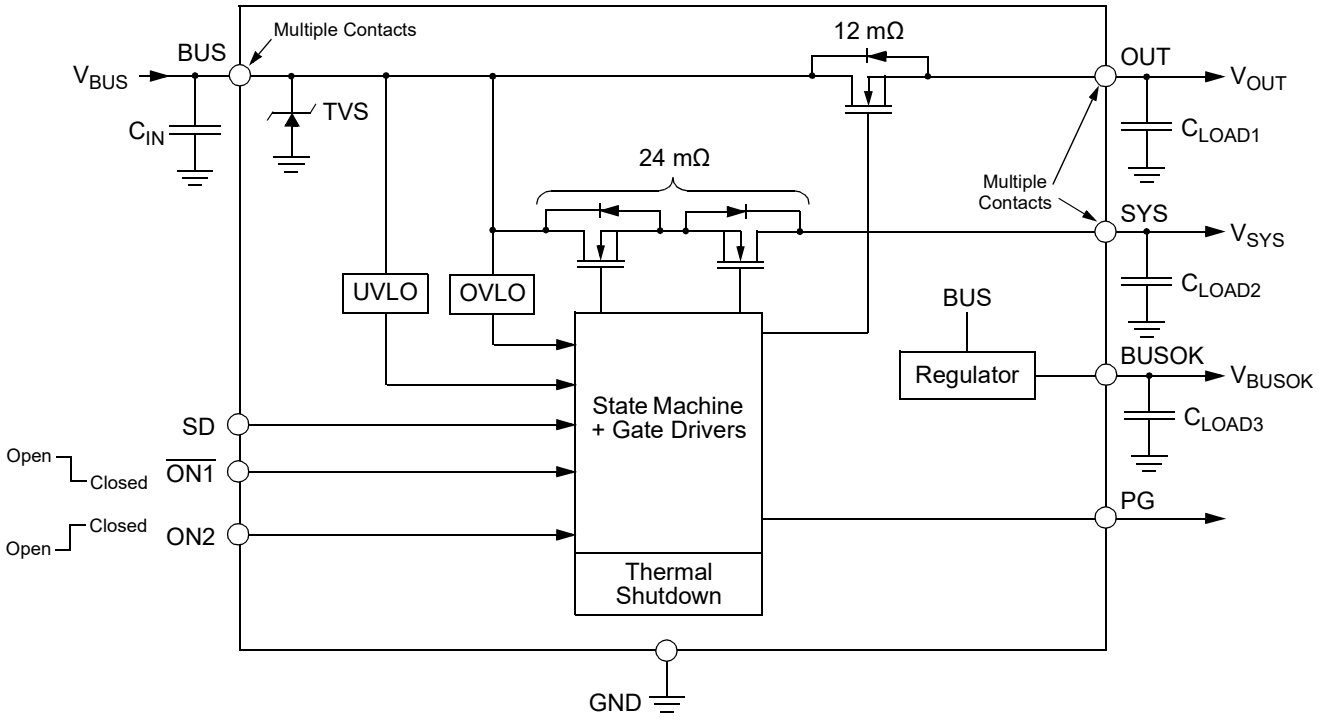


(Laser Marking View)
2.98 x 1.69 x 0.44 mm, 0.4 mm pitch

Applications

- Wearable Device
- Tablet PCs and Smartphones

Block Diagram



Pin Description

Pin Name	Pin #	Type	Pin Description
BUS	B3, C2, C3, C4, D2, D3, D4, E2, E3, E4, F2, F3, F4	Input	IC power supply and load switch input (13 contacts)
OUT	B1, B2, C1	Output	Load switch output to Load (3 contacts)
SYS	D1, E1, F1	Output	Load switch output to VBAT (3 contacts)
BUSOK	A3	Output	Always ON fixed output voltage from internal LDO
ON2	B4	Digital Input	BUS-to-SYS Switch Enable; Asserted active high digital input; 1 MΩ pull-down
$\overline{ON1}$	A4	Digital Input	BUS-to-OUT Switch Enable; Asserted active low digital input; 1 MΩ pull-down
SD	A2	Digital Input	IC shutdown; asserted active high; 1 MΩ pull-down
PG	A1	Digital Output	Asserted active-high push-pull output.
GND	G1, G2, G3, G4	GND	Analog GND (4 contacts)

Ordering Information

Part Number	Type	Production Flow
SLG59H1302C	WLCSP 28L	Industrial, -40 °C to 85 °C
SLG59H1302CTR	WLCSP 28L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
V_{BUS} to GND	Load Switch Input Voltage to Ground	Continuous	-0.3	--	28	V
V_{SYS} to GND	Load Switch Output Voltage to Ground	Continuous	-0.3	--	6	V
		Max pulse width 0.1 s	-0.3	--	7	V
V_{OUT} to GND	Load Switch Output Voltage to GND	$\overline{ON1}$ = LOW	-0.3	--	V_{BUS}	V
ESD_{HBM}	ESD Protection	Human Body Model, All pins	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model, All pins	1000	--	--	V
ESD_{SURGE}	ESD Protection	VBUS Surge Protection, IEC 61000-4-5	+130	--	--	V
OUT IDS	Maximum Current from BUS to OUT	Continuous	-0.3	--	6	A
		Max pulse width 10 ms	-0.3	--	7	A
SYS IDS	Maximum Current from BUS to SYS	Continuous	-0.3	--	6	A
		Max pulse width 10 ms	-0.3	--	7	A
BUSOK IDS	Maximum Current from BUS to BUSOK	Continuous	-0.3	--	100	mA
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	2.98 x 1.69 mm 28L WLCSP; Determined using a 1 in^2, 1 oz. copper pad under each BUS, SYS, and OUT terminal and FR4 pcb material.	--	45	--	°C/W

Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operating Conditions

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Min.	Typ.	Max.	Unit
Basic Operation					
V_{BUS}	IC Power supply and load switch input voltage	2.7	--	13.3	V
C_{IN}/C_{OUT}	Input and Output Capacitance	--	1	--	µF
C_{SYS}	SYS Capacitance	47	--	--	µF
C_{BUSOK}	Output Capacitance	--	4.7	--	µF
T_A	Operating Temperature	-40	--	85	°C

Electrical Characteristics

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
Basic Operation (V_{BUS} = 12 V, no load)						
I_Q	Input Quiescent Current	V_{BUS} = 4 V, $\overline{ON1}$ = LOW, No Load	--	180	--	µA

Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{IN_Q}	Input Supply Current when V_{OUT_OVLO} or V_{SYS_OVLO} threshold is reached	V_{BUS} = 15 V, $\overline{ON1}$ = LOW, ON2 = HIGH, BUSOK = 1 kΩ Load	--	4.2	--	mA
I_{SD}	Shutdown Current	V_{BUS} = 12 V	--	1	2	µA
V_{BUS_UVLO}	Under Voltage Trip Level	T_A = 0 °C to 85 °C	2.3	2.4	2.7	V
t_{BUS_START}	Soft-Start Time	See timing diagram	--	30	--	ms
$THERM_{ON}$	Thermal Shutdown Turn-on Temperature		--	145	--	°C
$THERM_{HYS}$	Thermal Shutdown Hysteresis		--	20	--	°C
BUS To OUT Switch						
V_{OUT_OVLO}	Over Voltage Trip Level	V_{BUS} Rising	13.3	13.9	14.5	V
V_{OUT_HYS}	V_{OUT} Hysteresis		--	350	--	mV
RDS_{ON}	ON Resistance	V_{BUS} = 12 V, I_{OUT} = 0.1 A, T_A = 25 °C	--	12	14	mΩ
		V_{BUS} = 12 V, I_{OUT} = 0.1 A, T_A = 85 °C	--	16	18	mΩ
t_{DEB_OUT}	Debounce Time	$\overline{ON1}$ = 0 V; V_{BUS} > V_{BUS_UVLO} to 0.1 x V_{OUT}; See timing diagram	--	15	--	ms
t_{ON_OUT}	Switch Turn-On Time	R_{LOAD} = 100 Ω, C_{LOAD} = 4.7 µF; V_{OUT} from 0.1 x V_{BUS} to 0.9 x V_{BUS}	--	2.5	--	ms
t_{OVP_OUT}[1]	Overvoltage Protection Time	I_{LOAD} = 100 mA, no C_{LOAD}; V_{BUS} step up over V_{OUT_OVLO} to V_{OUT} start separate from V_{BUS}	--	200	--	ns
t_{OFF_OUT}	Switch Turn-Off Time	50 % $\overline{ON1}$ ↑ to 0.9 x V_{OUT}; V_{BUS} = 12 V R_{LOAD} = 100 Ω, no C_{LOAD}	--	5	--	µs
BUS To SYS Switch						
V_{SYS_OVLO}	Over Voltage Trip Level	V_{BUS} Rising	4.9	5.25	5.5	V
V_{SYS_HYS}	V_{SYS} Hysteresis		--	110	--	mV
RDS_{ON}	ON Resistance	V_{BUS} = 4.5 V, I_{SYS} = 0.1 A, T_A = 25 °C	--	24	29.6	mΩ
		V_{BUS} = 4.5 V, I_{SYS} = 0.1 A, T_A = 85 °C	--	30	38	mΩ
I_{RCB}	Reverse Current	V_{SYS} = 4.4 V, measured from V_{BUS} to GND[1]	--	10	--	nA
t_{DEB_SYS}	Debounce Time	See timing diagram	--	15	--	ms
t_{SYS_START}	Soft-Start Time	See timing diagram	--	30	--	ms
t_{ON_SYS}	Switch Turn-On Time	R_{LOAD} = 100 Ω, C_{LOAD} = 4.7 µF; V_{SYS} from 0.1 x V_{BUS} to 0.9 x V_{BUS}	--	3.0	--	ms

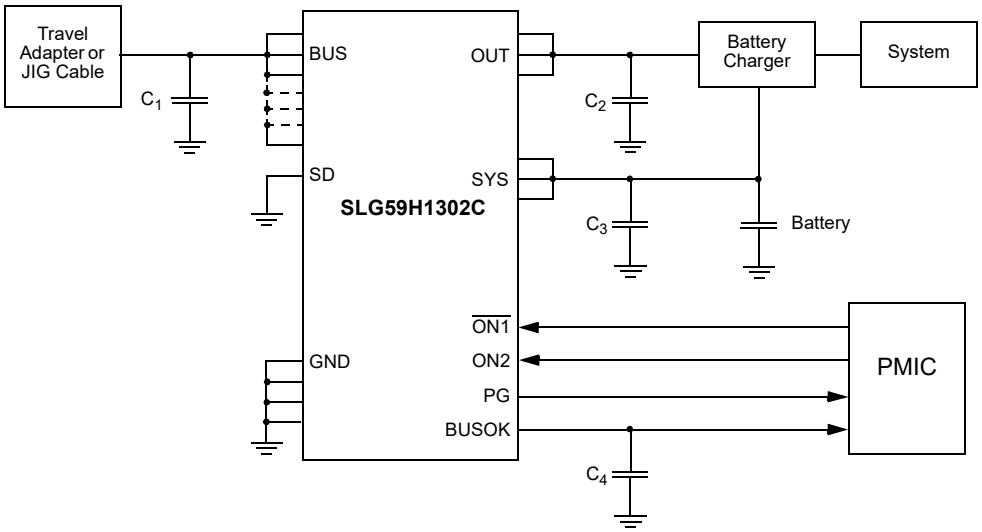
Electrical Characteristics (continued)

T_A = -40 °C to 85 °C (unless otherwise stated)

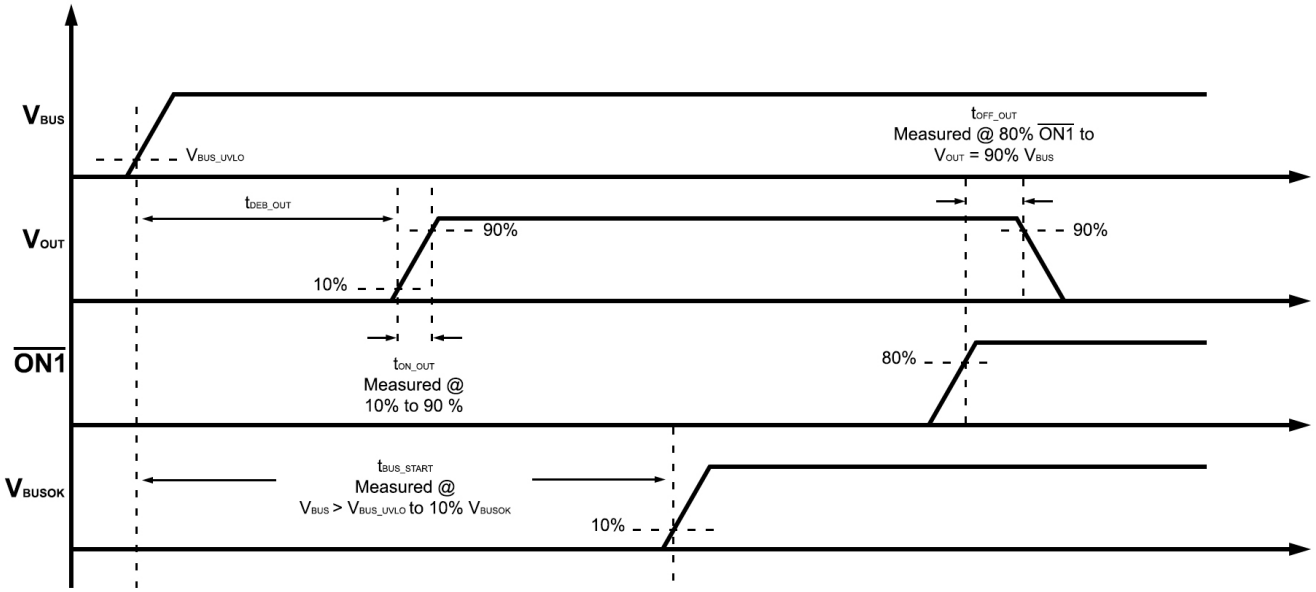
Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
t_{OVP_SYS}[1]	Overvoltage Protection Time	I_{LOAD} = 100 mA, no C_{LOAD}; V_{BUS} step up over V_{SYS_OVLO} to V_{SYS} start separate from V_{BUS}	--	200	--	ns
t_{OFF_SYS}	Switch Turn-Off Time	50 % ON2 ↓ to 0.9 x V_{SYS}; V_{BUS} = 5 V; R_{LOAD} = 100 Ω, no C_{LOAD}	--	5	--	µs
BUSOK						
V_{BUSOK}	BUSOK Output voltage	V_{BUS} = 5 V, no load	3.8	4.0	4.4	V
		V_{BUS} = 12 V, no load	3.8	4.0	4.4	V
		V_{BUS} = 5 V; BUSOK IDS = 100 mA	3.6	3.8	4.1	V
		V_{BUS} = 12 V; BUSOK IDS = 100 mA	3.6	3.8	4.1	V
Digital Signals						
V_{OH_PG}	PG Output HIGH Voltage	ON2 = Low to High, V_{BUS} = 3.4 V to 5 V	--	1.8	--	V
V_{OL_PG}	PG Output LOW Voltage	ON2 = High to Low, V_{BUS} = 3.4 V to 5 V	--	--	0.3	V
$R_{PD(ONx, SD)}$	Internal Pull-Down Resistor at $\overline{ON1}$, ON2, and SD		--	1	--	MΩ
$V_{IH(ONx, SD)}$	Logic Enable HIGH Voltage		0.9	--	--	V
$V_{IL(ONx, SD)}$	Logic Enable LOW Voltage		--	--	0.3	V
$I_{LKG(BUSOK)}$	BUSOK Leakage Current		--	--	1	µA
$I_{LKG(ONx, SD)}$	SD, ONx Leakage current	V_{BUS} = 12 V	--	--	5	µA

Notes:
1. Based on bench measurement only.

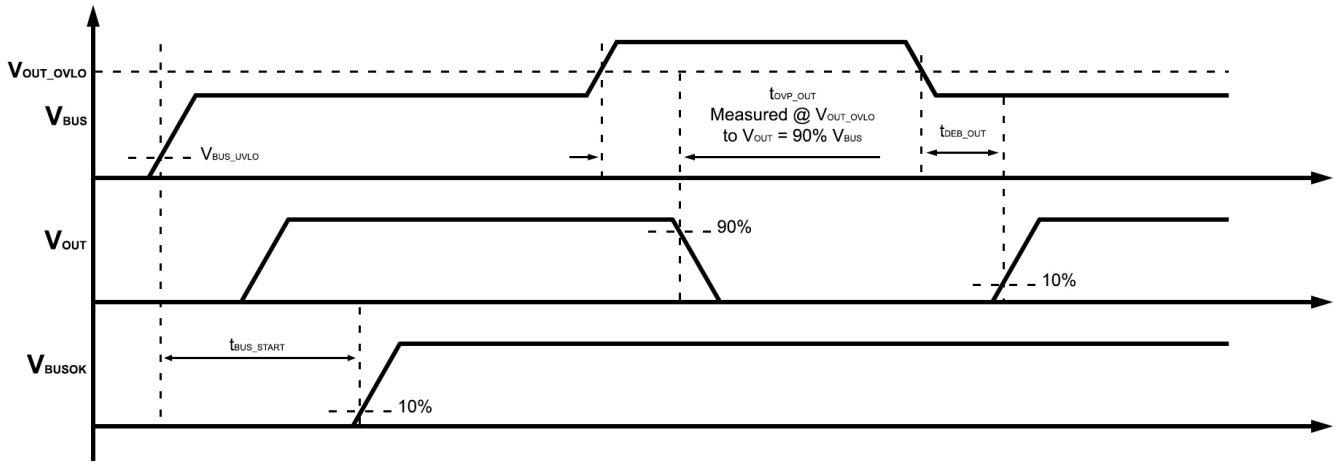
Typical Application Diagram



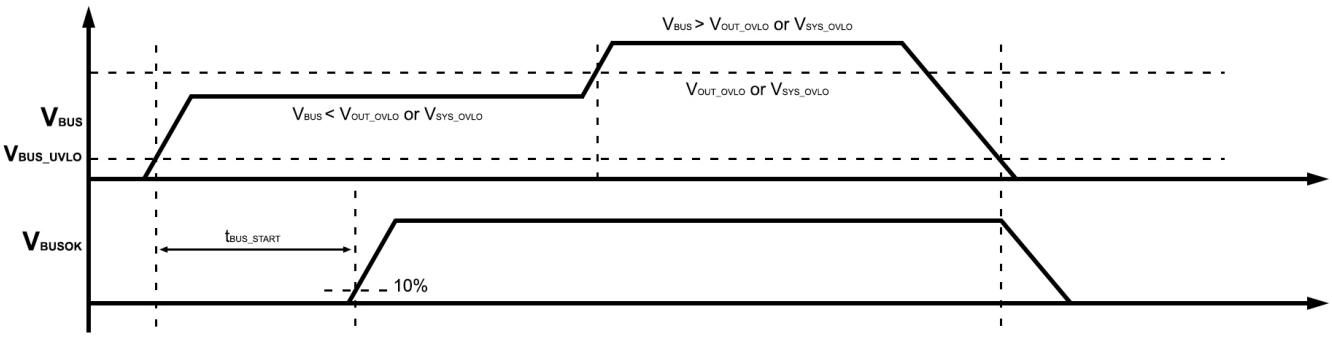
Timing for BUS to OUT Power Up/Down and Normal Operation



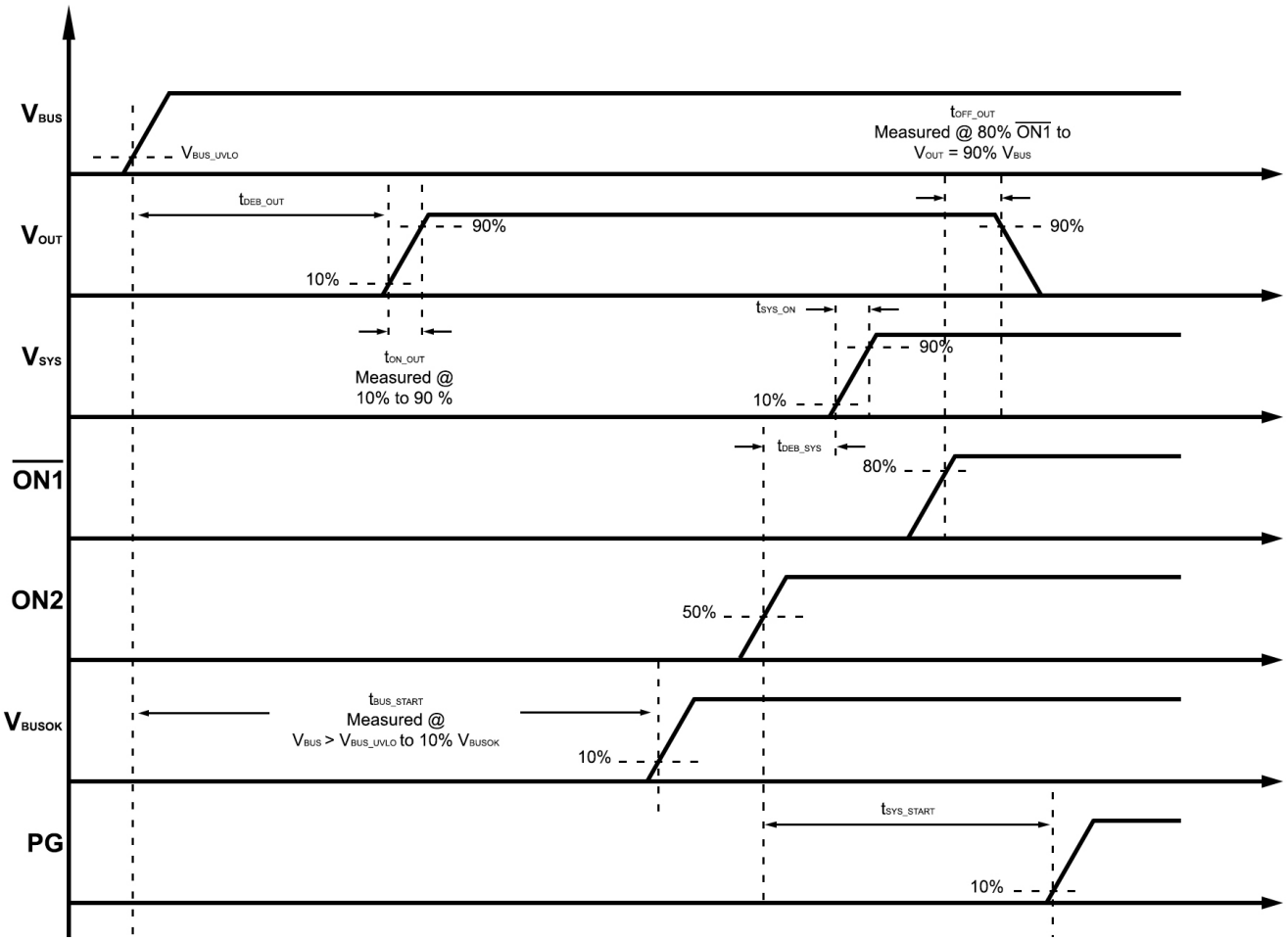
Timing for BUS to OUT OVLO Operation (ON1 = LOW)



"Always ON" based BUSOK Operation (ON1 = X, ON2 = X, SD = LOW)



Timing for Overall ON/OFF Operation (SD = LOW)



Layout Guidelines:

1. Since the BUS, SYS and OUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 1, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1302C's BUS, SYS and OUT pins;

3. The GND pin should be connected to system analog or power ground plane.

SLG59H1302C Evaluation Board:

A High Voltage GreenFET Evaluation Board for SLG59H1302C is designed according to the statements above and is illustrated on Figure 1. Please note that evaluation board has BUS_Sense, SYS_Sense and OUT_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation. evaluation.

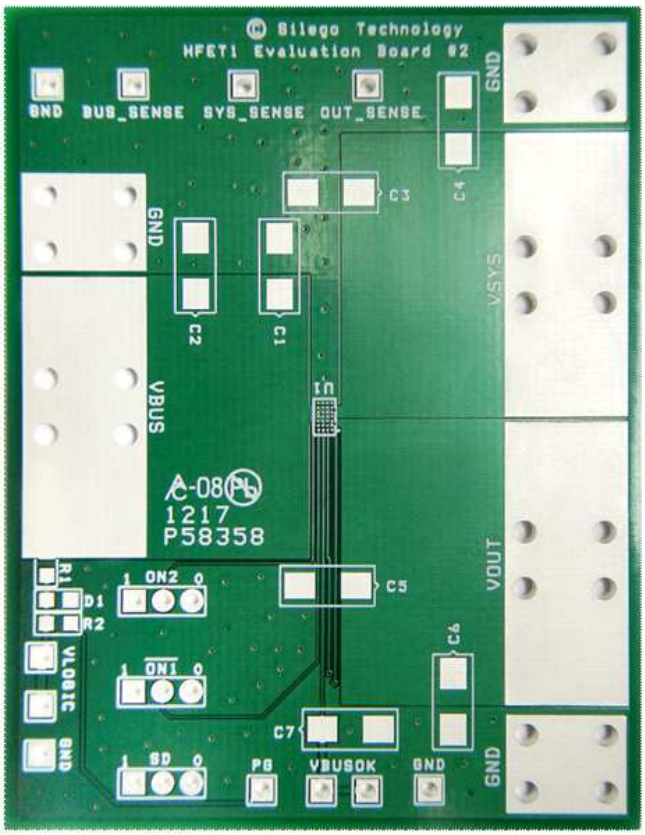


Figure 1. SLG59H1302C Evaluation Board

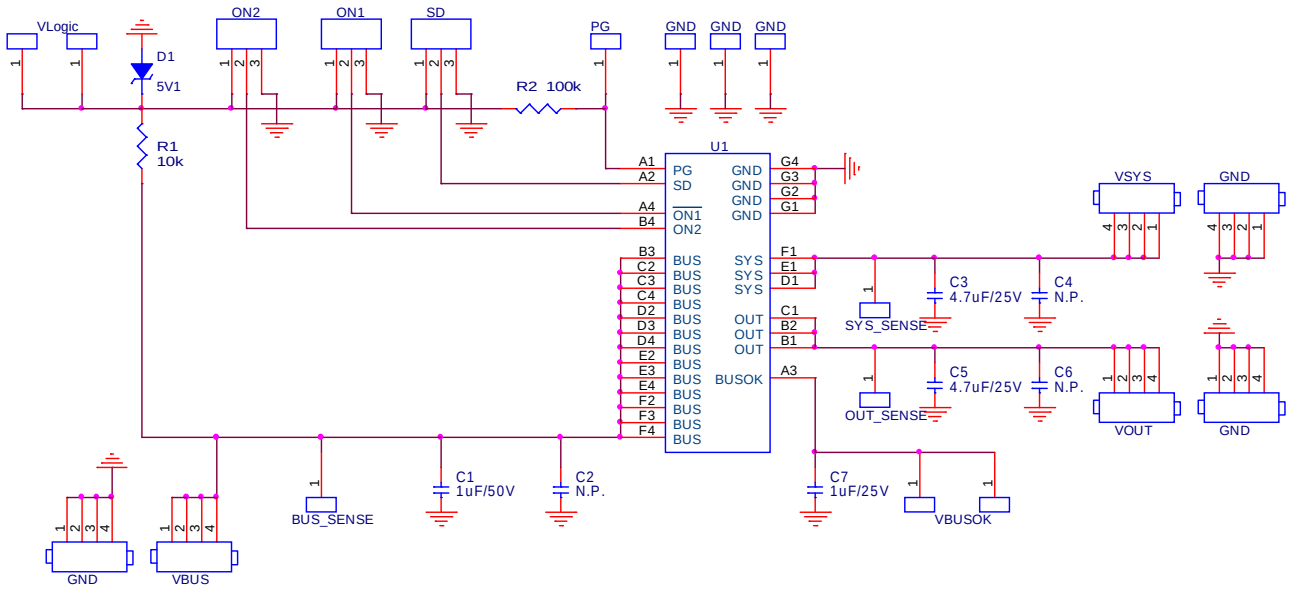


Figure 2. SLG59H1302C Evaluation Board Connection Circuit

Basic Test Setup and Connections

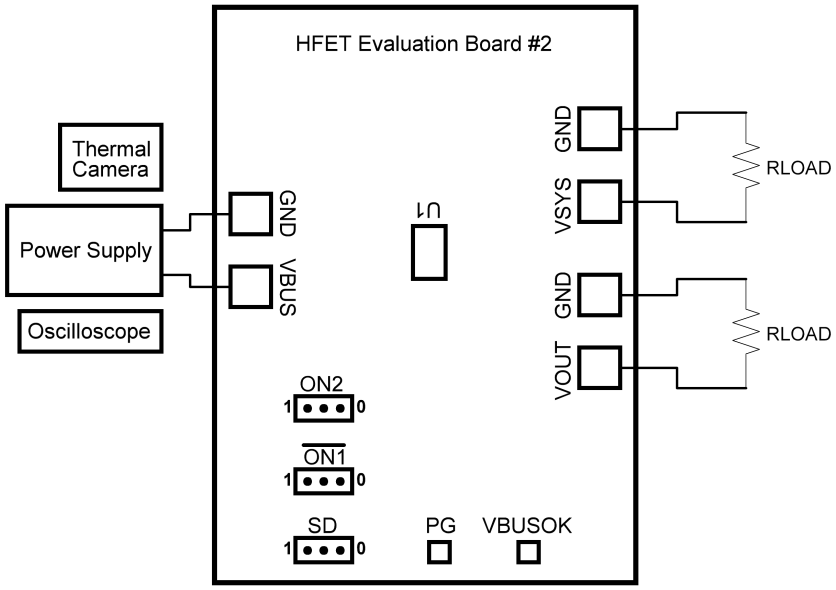
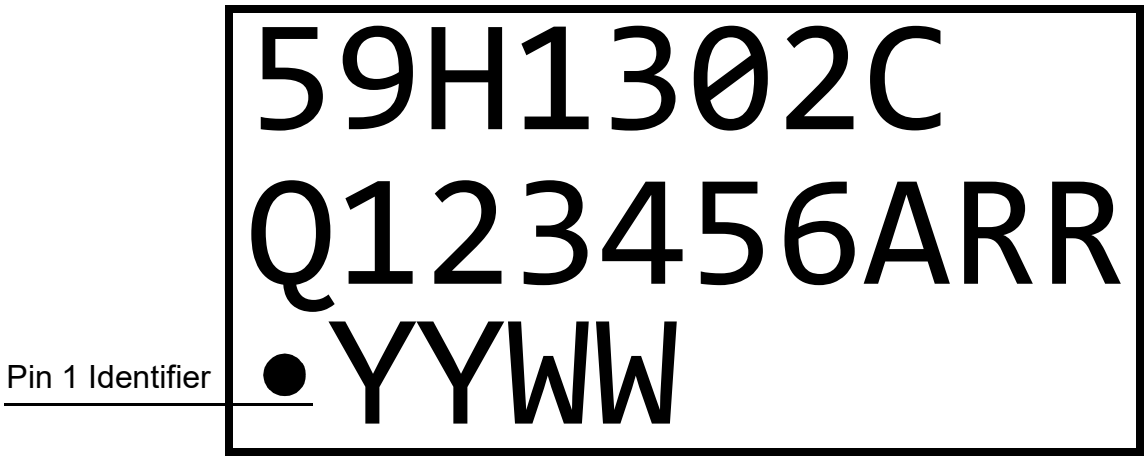


Figure 3. SLG59H1302C Evaluation Board Connection Circuit

EVB Configuration

1. Set SD to GND;
2. Connect oscilloscope probes to VBUS, VOUT, VSYS, ON1, ON2, etc.;
3. Turn on Power Supply and set desired V_{BUS} from 2.7 V … 13.3 V;
4. Toggle the ON1 signal High or Low to test SLG59H1302C's OUT rail operation;
5. Toggle the ON2 signal High or Low to test SLG59H1302C's SYS rail operation;

Package Top Marking System Definition



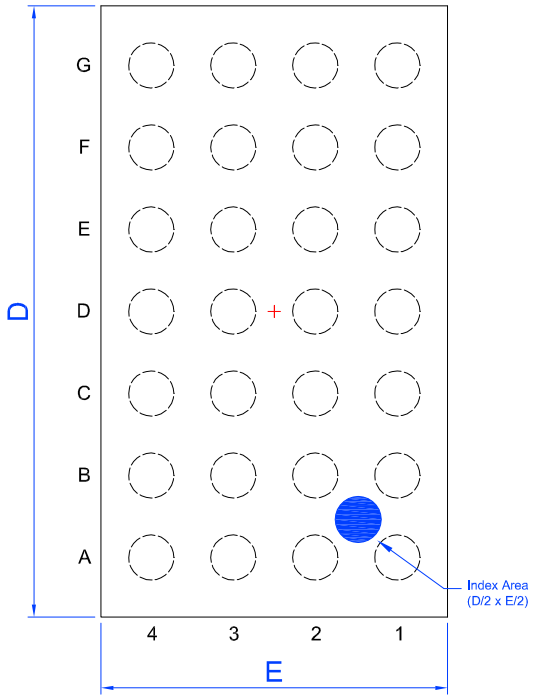
59H1302C - Part ID Field
Q123456 - Assembly Lot Traceability Code Field[1]
A - Assembly Site Code Field [2]
RR - Part Revision Code Field[2]
YY - Year Code Field[1]
WW - Week Code Field[1]

Note 1: Each character in code field can be alphanumeric A-Z and 0-9
Note 2: Character in code field can be alphabetic A-Z

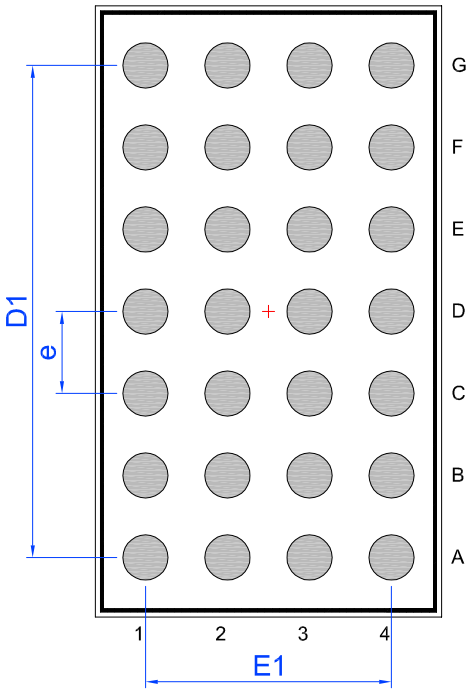
Package Drawing and Dimensions

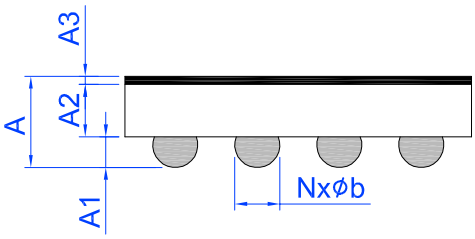
28 Lead WLCSP Package

Laser Marking View



Bump View





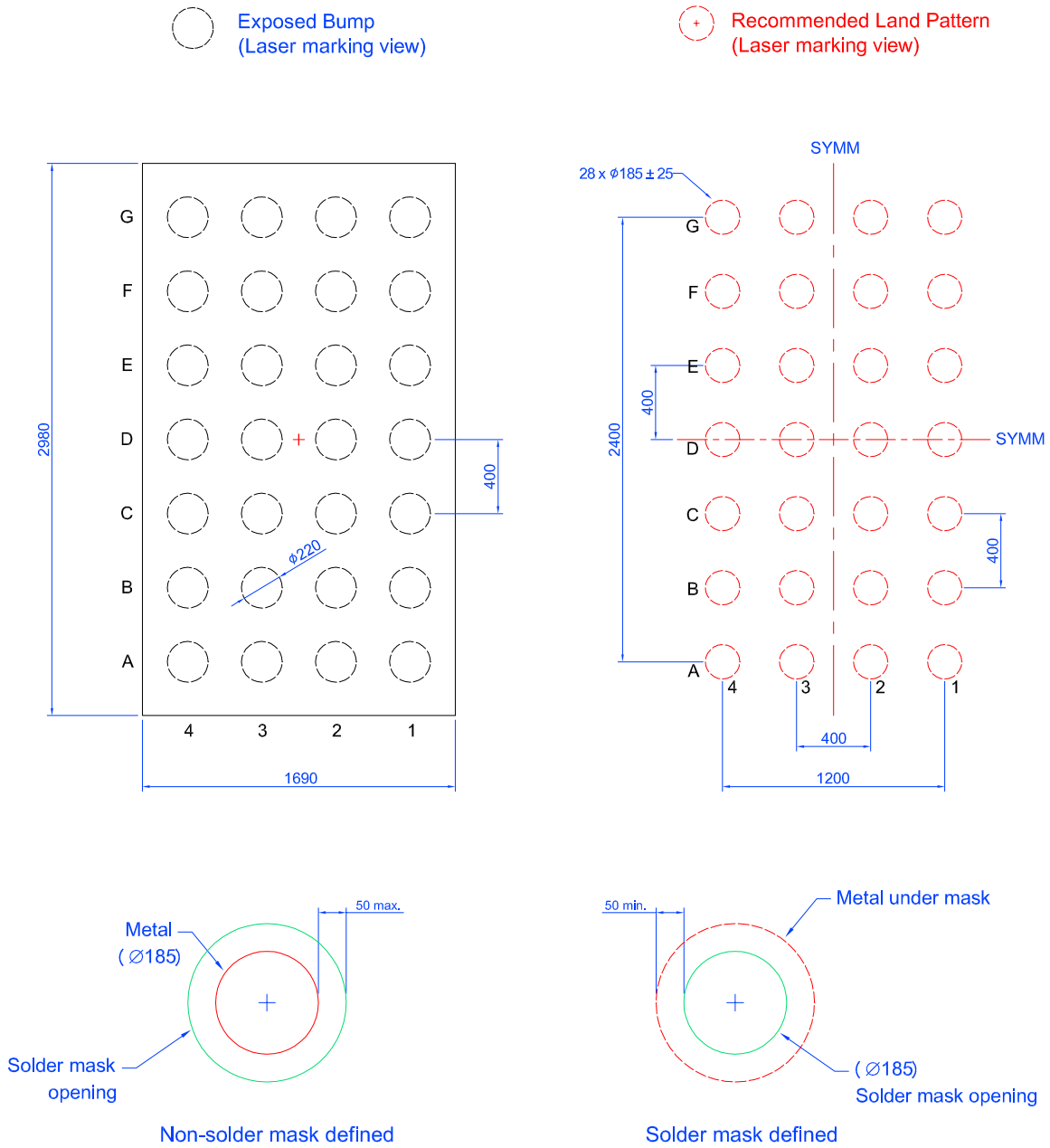
SIDE View

TERMINALS ASSIGNMENTS				
G	GND	GND	GND	GND
F	SYS	BUS	BUS	BUS
E	SYS	BUS	BUS	BUS
D	SYS	BUS	BUS	BUS
C	OUT	BUS	BUS	BUS
B	OUT	OUT	BUS	$\overline{ON1}$
A	SD	PG	BUSOK	ON2
	1	2	3	4

Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.380	-	0.500	D	2.95	2.98	3.01
A1	0.125	0.150	0.175	E	1.66	1.69	1.72
A2	0.240	0.265	0.290	D1	2.40 BSC		
A3	0.015	0.025	0.035	E1	1.20 BSC		
b	0.195	0.220	0.245	e	0.40 BSC		
N	28 (Bump)						

SLG59H1302C 28-pin WLCSP PCB Landing Pattern



Solder mask detail (not to scale)

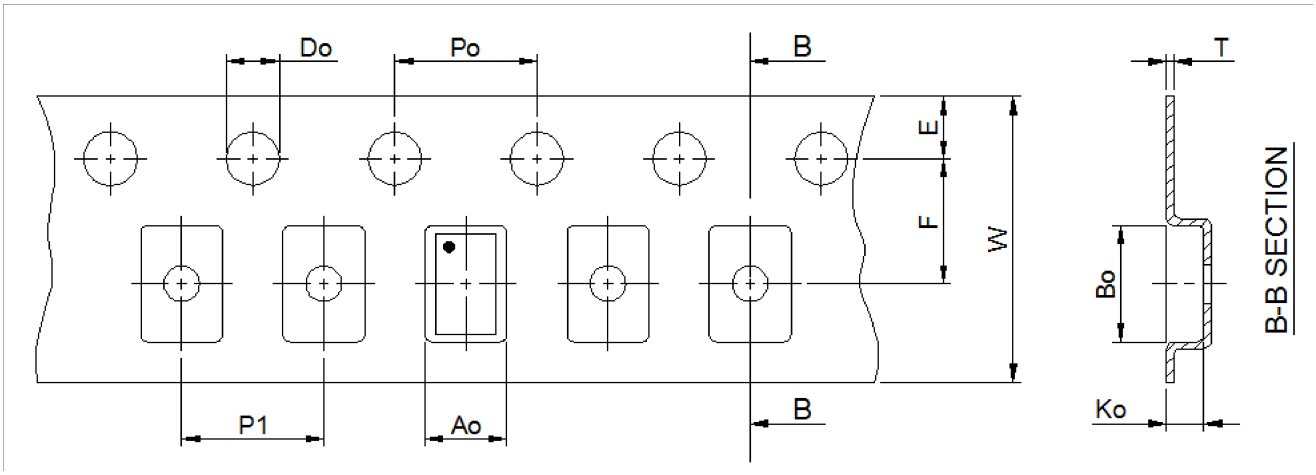
Unit: um

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
WLCSP 28L 2.98x1.69 mm 0.4P Green	28	2.98 x 1.69 x 0.44	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width	Tape Thickness
	A0	B0	K0	P0	P1	D0	E	F	W	T
WLCSP 28L 2.98x1.69 mm 0.4P Green	1.85	3.25	0.7	4	4	1.55	1.75	3.5	8	0.25



Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.64 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
2/2/2022	1.03	Updated Company name and logo Fixed typos
1/6/2019	1.02	Added Layout Guidelines Fixed typos
9/18/2017	1.01	Updated EC Table
6/14/2017	1.00	Production Release

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