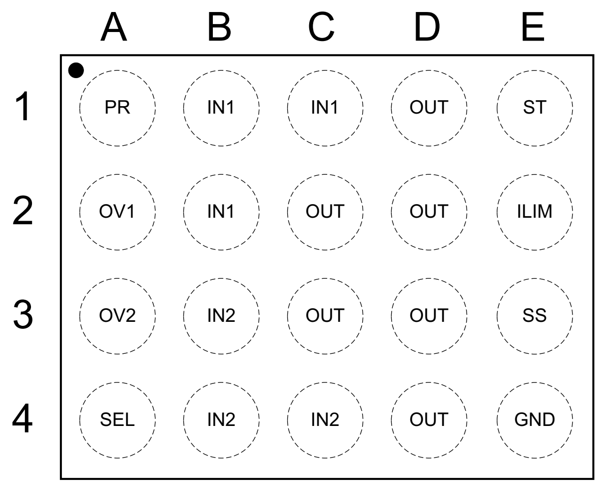
General Description

The SLG59H1401C is designed for OR'ing or manual Power MUX applications. The part comes with two 3 A rated load switches that are well suited for a variety of systems having multiple power sources. The device will automatically detect, select, and seamlessly transition between available inputs. Additionally, manual switching between two power rails allowed.

Features

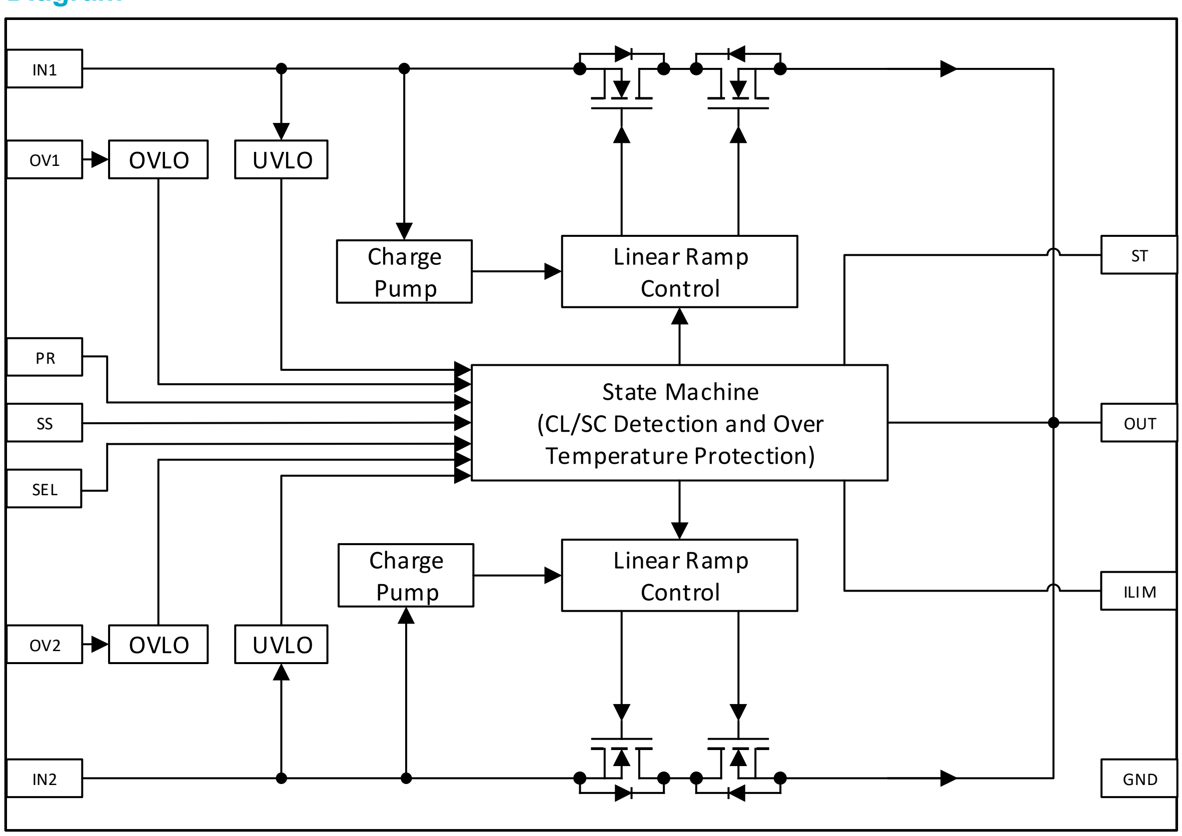
- Two 3 A load switches with common output
- Two Integrated VGS Charge Pumps
- Wide operating range: 2.8 V to 6 V
- Adjustable output soft start time (SS)
- Low RDS_{ON}: 52 mΩ (typical)
- Adjustable priority
  - Accuracy < ±5%
- Adjustable Overvoltage Protection
  - Accuracy < ±5%
- Channel status indication (ST)
- Undervoltage Lockout
- True Reverse-Current Blocking
- Protected by thermal shutdown and adjustable current limit
- 1.585 mm x 1.985 mm, 0.4 mm pitch, 20L WLCSP
  - Pb-Free / Halogen-Free / RoHS Compliant

Pin Configuration



20-pin WLCSP
(Bottom View)

Block Diagram



Pin Description

Pin #	Pin Name	Type	Pin Description
A1	PR	Input	Analog input which sets the priority to Channel 1. PR is compared to internal reference voltage V_{REF}. Connect to GND if not required.
A2	OV1	Input	Analog input which together with an external resistor divider, is used to set the overvoltage threshold for Channel 1. OV1 is compared to internal reference voltage V_{REF}. If $V_{OV1} \geq V_{REF}$, Channel 1 is turned off and returns to normal operation once $V_{OV1} < V_{REF}$. Connect to GND if not used.
A3	OV2	Input	Analog input which together with an external resistor divider, is used to set the overvoltage threshold for Channel 2. OV2 is compared to internal reference voltage V_{REF}. If $V_{OV2} \geq V_{REF}$, Channel 2 is turned off and returns to normal operation once $V_{OV2} < V_{REF}$. Connect to GND if not used.
A4	SEL	Input	Select makes it possible to override the priority and manually select IN2. SEL is compared to internal reference voltage V_{REF}. Connect to GND if not required.
B1, B2, C1	IN1	Power	Input terminal of load switch Channel 1. Capacitors at IN1 should be rated at a voltage higher than maximum input voltage ever present.
B3, B4, C4	IN2	Power	Input terminal of load switch Channel 2. Capacitors at IN2 should be rated at a voltage higher than maximum input voltage ever present.
C2, C3, D1, D2, D3, D4	OUT	Power	Output terminal. Capacitors at OUT should be rated at a voltage higher than maximum input voltage ever present.
E1	ST	Output	Status is an open-drain, active LOW output. When asserted HIGH, IN1 is selected. When asserted LOW, IN2 is selected. Connect to GND if not required.
E2	ILIM	Output	A 1%-tolerance resistor connected between ILIM and GND sets the load switch's active current limit for both channels. Please refer to the Setting the SLG59H1401C's Active Current Limit section
E3	SS	Output	A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from SS pin to GND, sets the V_{OUT} slew rate and overall turn-on time of the SLG59H1401C.
E4	GND	GND	Ground connection. Connect this pin to system analog or power ground plane.

Ordering Information

Part Number	Type	Production Flow
SLG59H1401C	WLCSP-20L	Industrial, -40 °C to 85 °C
SLG59H1401CTR	WLCSP-20L (Tape and Reel)	Industrial, -40 °C to 85 °C

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN[1,2]}$	Maximum Input Voltage		-0.3	--	6.6	V
V_{OUT}	Maximum Output Voltage		-0.3	--	6.6	V
V_{OV1}, V_{OV2}	Maximum Overvoltage Pin Voltage		-0.3	--	6	V
V_{PR}, V_{SEL}	Maximum Control Input Pin Voltage		-0.3	--	6	V
V_{ST}	Maximum Control Output Pin Voltage		-0.3	--	6	V
T_S	Storage Temperature		-65	--	150	°C
ESD_{HBM}	ESD Protection	Human Body Model	2000	--	--	V
ESD_{CDM}	ESD Protection	Charged Device Model	500	--	--	V
MOSFET IDS_{PK}	Peak Current from Drain to Source	For no more than 10 continuous seconds out of every 100 seconds	--	--	3.5	A
Note: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.						

Electrical Characteristics

T_A = -40 °C to 85 °C, unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{IN[1,2]}$	Power Switch Input Voltage		2.8	--	6	V
$V_{IN[1,2](UVLO)}$	$V_{IN[1,2]}$ Undervoltage Lockout Threshold	$V_{IN[1,2]}$ ↑;	2.5	2.65	2.8	V
		$V_{IN[1,2]}$ ↓;	2.4	2.55	2.7	V
$I_{Q\_IN[1,2]}$	Quiescent Current (IN[1,2] powering OUT)	OUT = Open, $V_{PR} < V_{REF}$; $\|V_{IN1}-V_{IN2}\| < 1$ V	--	300	400	µA
$I_{STBY\_IN[1,2]}$	Standby Current (IN[1,2] not powering OUT)	$V_{OUT} = V_{IN[1,2]}$, $V_{PR} < V_{REF}$; $\|V_{IN1} - V_{IN2}\| < 1$ V, T_A = 25 °C	0	15	25	µA
		$V_{OUT} = V_{IN[1,2]}$, $V_{PR} < V_{REF}$; $\|V_{IN1} - V_{IN2}\| < 1$ V, T_A = -40 °C to 85 °C	--	--	25	µA
$I_{IN[1,2]\_Leakage}$	Leakage Current from IN[1,2] to OUT	$\|V_{IN[1,2]} - V_{OUT}\| \le 5$ V; T_A = 25 °C	-1	--	1	µA
		$\|V_{IN[1,2]} - V_{OUT}\| \le 5$ V; T_A = -40 °C to 85 °C	-5	--	5	µA
		$\|V_{IN[1,2]} - V_{OUT}\| \le 6$ V; T_A = 25 °C	-1	--	1	µA
		$\|V_{IN[1,2]} - V_{OUT}\| \le 6$ V; T_A = -40 °C to 85 °C	-35	--	35	µA
$RDS_{ON[1,2]}$	ON Resistance	T_A = 25 °C; I_{DS} = 200 mA; $V_{PR} > V_{REF}$; $V_{IN[1,2]} \ge 5.0$ V	--	52	75	mΩ
		T_A = -40 °C to 85 °C; I_{DS} = 200 mA; $V_{PR} > V_{REF}$; $V_{IN[1,2]} \ge 5.0$ V	--	--	90	mΩ
MOSFET IDS	Current from IN[1,2] to OUT	Continuous	--	--	3	A
T_{ON_Delay}	ON Delay Time	$V_{IN[1,2](UVLO)}$ ↑ to V_{OUT} Ramp Start	8	--	--	ms

Electrical Characteristics (continued)

T_A = -40 °C to 85 °C, unless otherwise noted.

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
$V_{OUT(SR)}$	V_{OUT} Slew Rate	10% V_{OUT} to 90% V_{OUT}	Set by External C_{SS}[1]			V/ms
		Example: C_{SS} = 220 nF, $V_{IN[1,2]}$ = 5 V; C_{LOAD} = 2 µF; R_{LOAD} = 100 Ω	--	0.3	--	V/ms
T_{Total_ON}	Total Turn On Time	$V_{IN[1,2](UVLO)}$ ↑ to 90% V_{OUT}	Set by External C_{SS}[1]			ms
		Example: C_{SS} = 220 nF, $V_{IN[1,2]}$ = 5 V; C_{LOAD} = 2 µF; R_{LOAD} = 100 Ω	--	23	--	ms
V_{PR}, V_{SEL}	Voltage on PR and SEL pins		0	--	5.5	V
V_{ST}	Voltage on ST pin		0	--	5.5	V
$V_{OV[1,2]}$	Voltage on OV[1,2] Pins		0	--	5.5	V
V_{REF}	Internal Voltage Reference	V_{PR}, V_{OV1}, V_{OV2}, V_{SEL} ↑	1.02	1.06	1.10	V
		V_{PR}, V_{OV1}, V_{OV2}, V_{SEL} ↓	1.00	1.04	1.08	V
$I_{Pin\_Leakage}$	Pin Leakage Current	V_{PR}, V_{OV1}, V_{OV2}, V_{ST} = 0 V to 5.5 V	-0.1	--	0.1	µA
t_{ST}	Status Pin Signal Delay	Transition from Low to High	--	1	--	µs
R_{ST}	Recommended Pull Up Resistance for Status Pin		--	6	20	kΩ
I_{RCB}	Fast Reverse Current Detection Threshold	V_{OUT} > $V_{IN[1,2]}$	0.1	0.5	2	A
V_{RCB}	RCB Release Voltage	V_{OUT} > $V_{IN[1,2]}$	0	25	50	mV
t_{RCB}	Fast Reverse-current Blocking Response Time		--	10	--	µs
t_{SW}	Switchover time	V_{OUT} < $V_{IN[1,2]}$, V_{SEL} < V_{REF}	--	100	--	µs
V_{COMP}	Input Voltage Comparator (V_{IN2} referenced to V_{IN1})	$V_{IN1} \geq V_{IN2}$	0	280	600	mV
		V_{IN1} > V_{IN2}, Falling Hysteresis	2.5	3.5	4.5	%
I_{LIMIT}	Active Current Limit, I_{ACL}	R_{ILIM} = 31.6 kΩ	3.0	3.5	4.0	A
		R_{ILIM} = 46.4 kΩ	2.0	2.5	3.0	A
		R_{ILIM} = 85 kΩ	1.0	1.5	2.0	A
		R_{ILIM} < 1 kΩ	1.5	2.5	3.5	A
t_{LIMIT}[2]	Current Limit Response Time	From I_{DS} > I_{ACL} to I_{DS} regulated to I_{ACL}	--	250	--	µs
$THERM_{ON}$	Thermal shutoff turn-on temperature		--	160	--	°C
$THERM_{OFF}$	Thermal shutoff turn-off temperature		--	140	--	°C
$THERM_{TIME}$[3]	Thermal shutoff time		--	--	1	ms

Notes:

1. Refer to typical Timing Parameter vs. C_{SS} performance charts for additional information when available.
2. For more information on device behavior during short-circuit conditions please see SLG59H1401C Current Limiting section.
3. See Current Limit Behavior Timing Diagram

SLG59H1401C Normal Operation State Table

Mode	Condition	PR ≥ V_{REF}	SEL ≥ V_{REF}	OUT	ST	Note
VCOMP mode	IN1 > IN2	0	0	IN1	H	Largest Input Voltage Determines Output
VCOMP mode	IN1 ≤ IN2	0	0	IN2	L	Largest Input Voltage Determines Output
Priority mode	X	1	0	IN1	H	Select Channel 1 on OUT as priority
Manual Channel Selection mode	X	X	1	IN2	L	Override priority and select Channel 2 on OUT

SLG59H1401C Fault Operation State Table

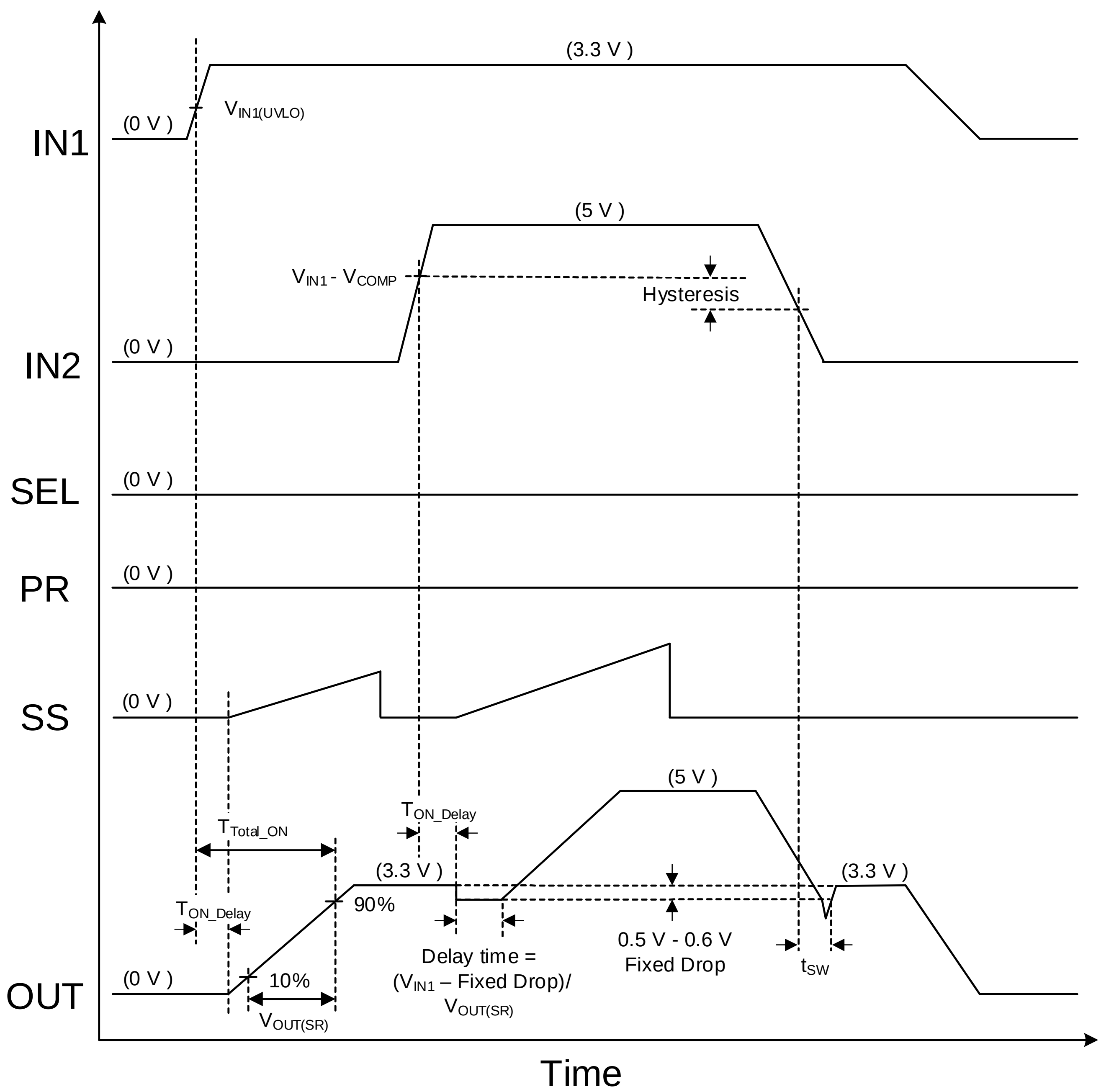
Channel 1 Fault	Channel 2 Fault	SEL ≥ V_{REF}	OUT	ST	Note
IN1 ≤ $V_{IN1(UVLO)}$ Or OV1 ≥ V_{REF}	IN2 ≤ $V_{IN2\ (UVLO)}$ Or OV2 ≥ V_{REF}				
0	0	X	-	-	Output Behavior Determined by "Normal Operation State" Table
1	0	X	IN2	L	Channel 1 is not valid, switch to Channel 2
0	1	0	IN1	H	Channel 2 is not valid, switch to Channel 1
1	1	0	Hi-Z	H	Channel 1 and Channel 2 are not valid, output is in Hi-Z state
X	1	1	Hi-Z	H	Selected Channel 2 is not valid, output is in Hi-Z state

A summary of the SLG59H1401C device operation:

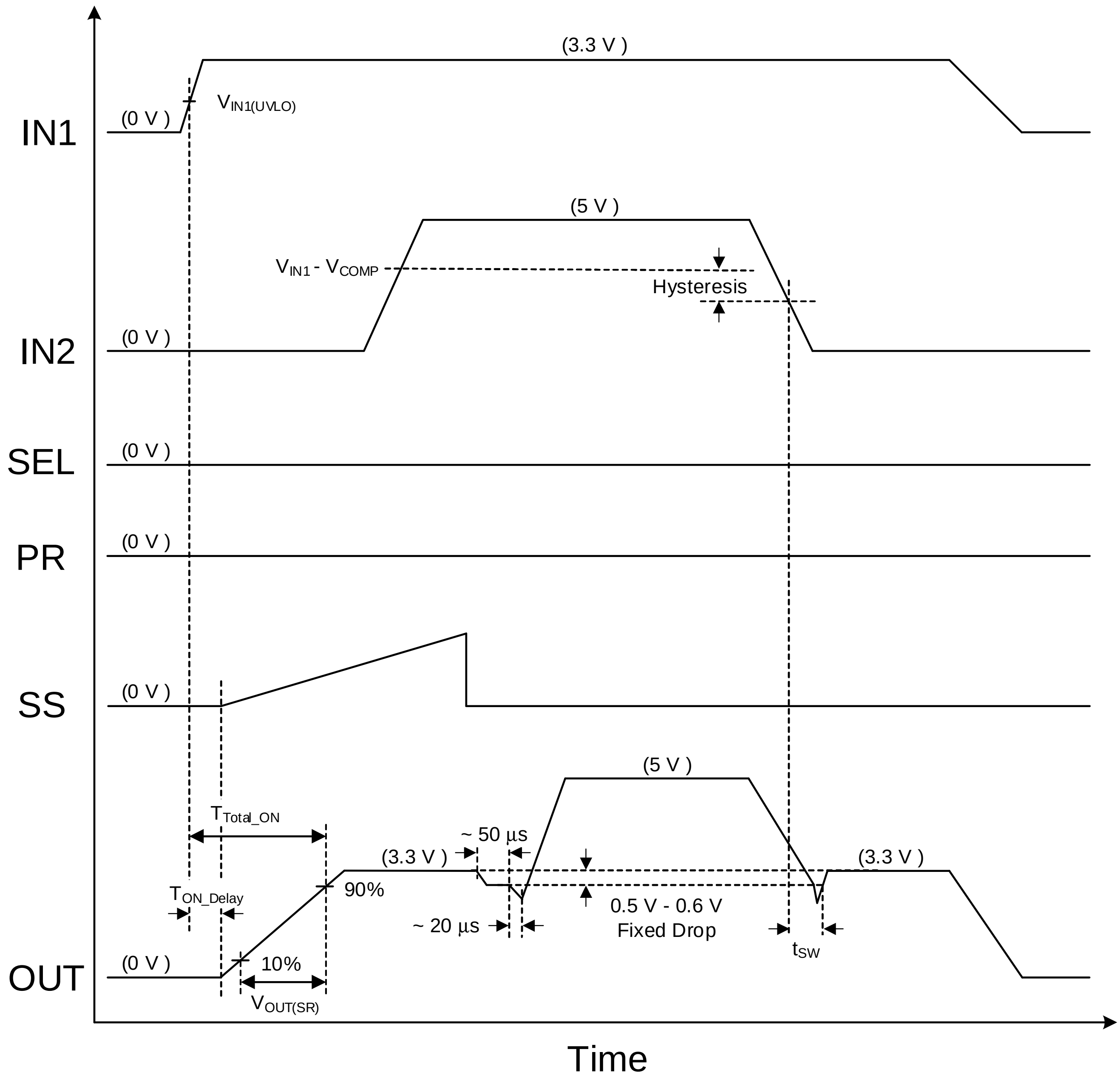
- If the valid voltages are applied at both inputs and PR is higher than V_{REF}, then IN1 will power the output.
- If the valid voltages are applied at both inputs and PR is lower than V_{REF}, then the highest input voltage will power the output.
- If both inputs are not valid, then the output is Hi-Z.
- ST pin indicates which of the inputs is powering output. ST pulled high when IN1 is powering the output or the output is Hi-Z. ST pulled low when IN2 is powering the output.
- SEL pin can override the PR. When SEL is pulled high IN2 is powering the output.

Timing Diagrams

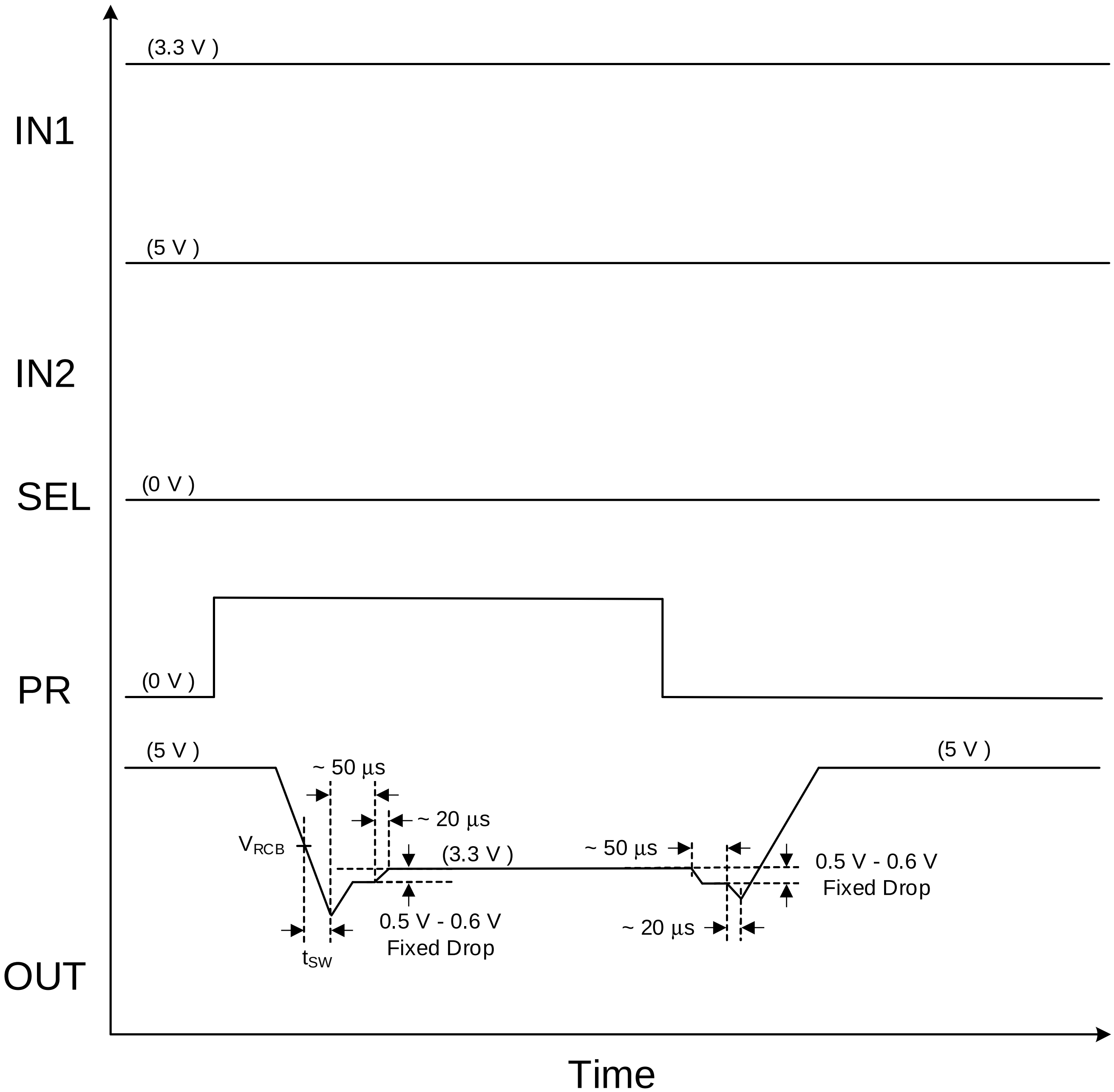
VCOMP Mode operating timing diagram when IN2 is applied after first SS rise is done



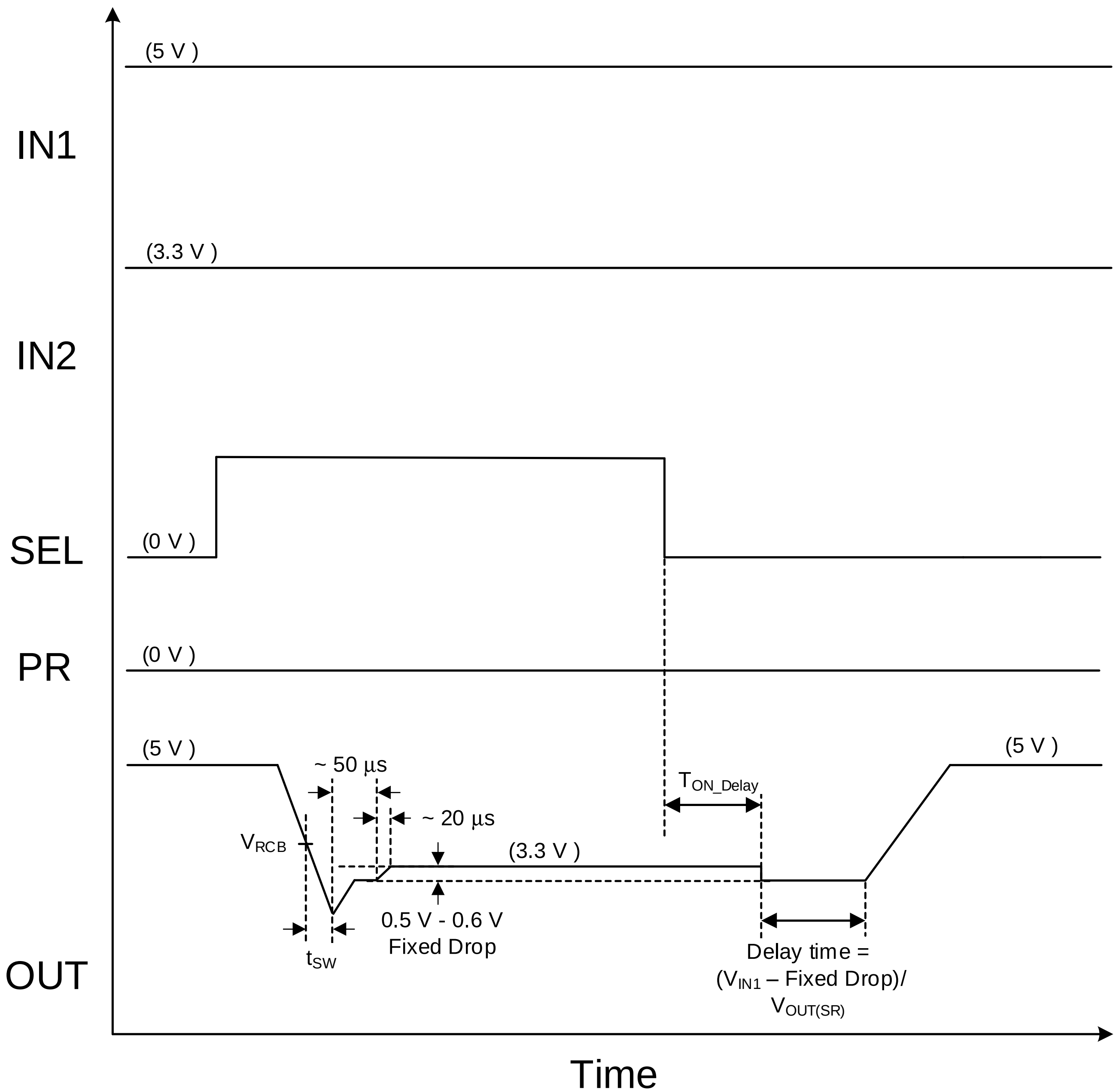
VCOMP Mode operating timing diagram when IN2 is applied before first SS rise is done



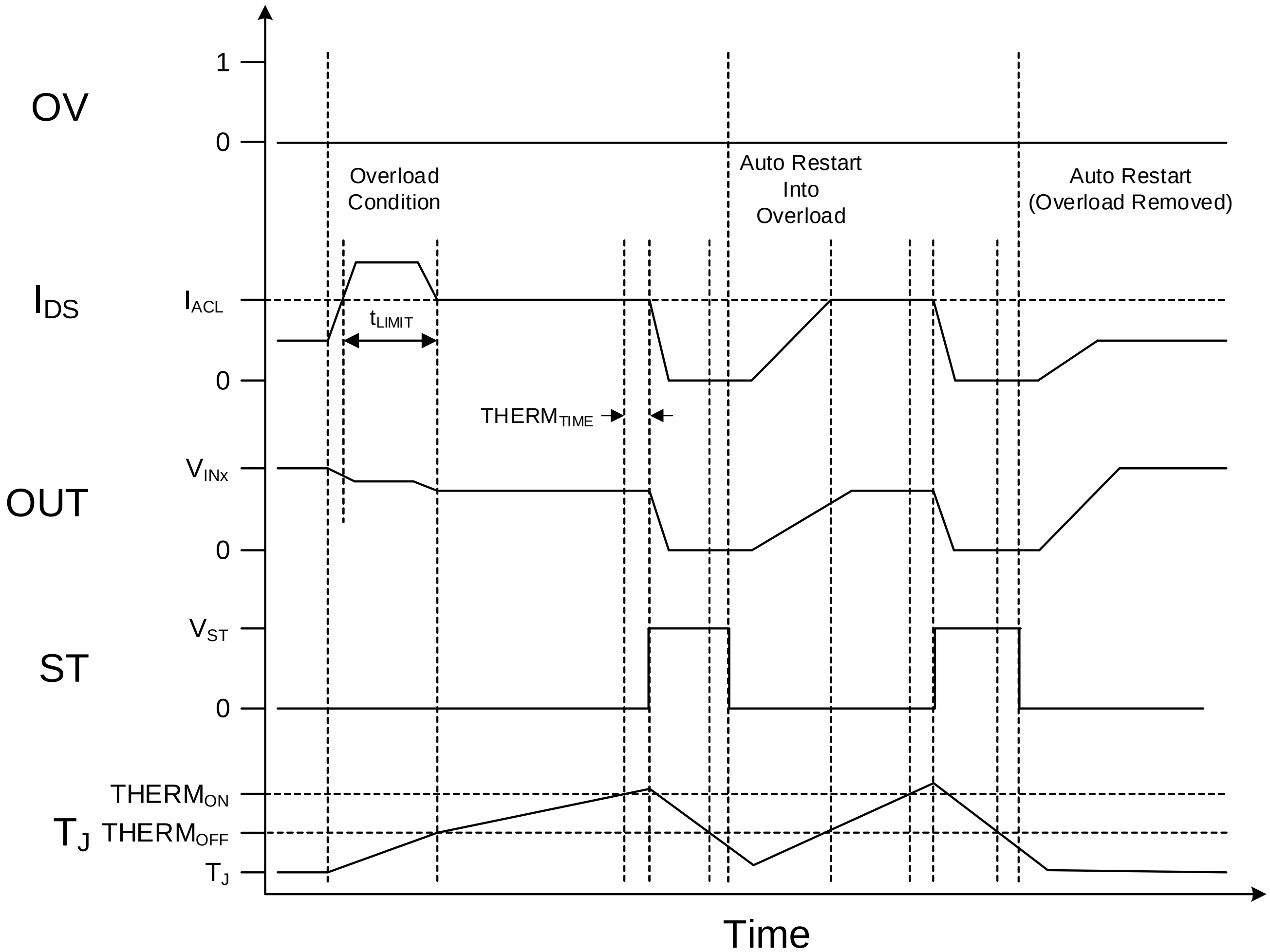
Switchover operating timing diagram by PR signal



Switchover operating timing diagram by SEL signal

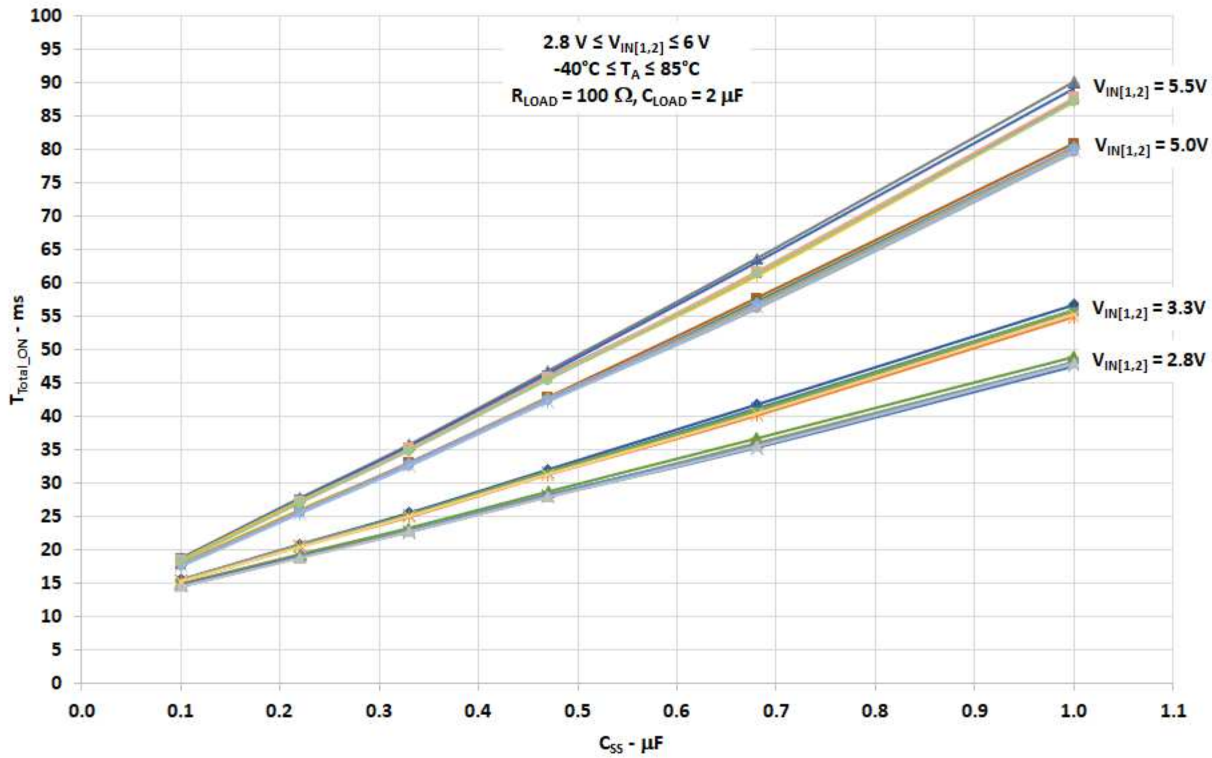


Current Limit Behavior Timing Diagram

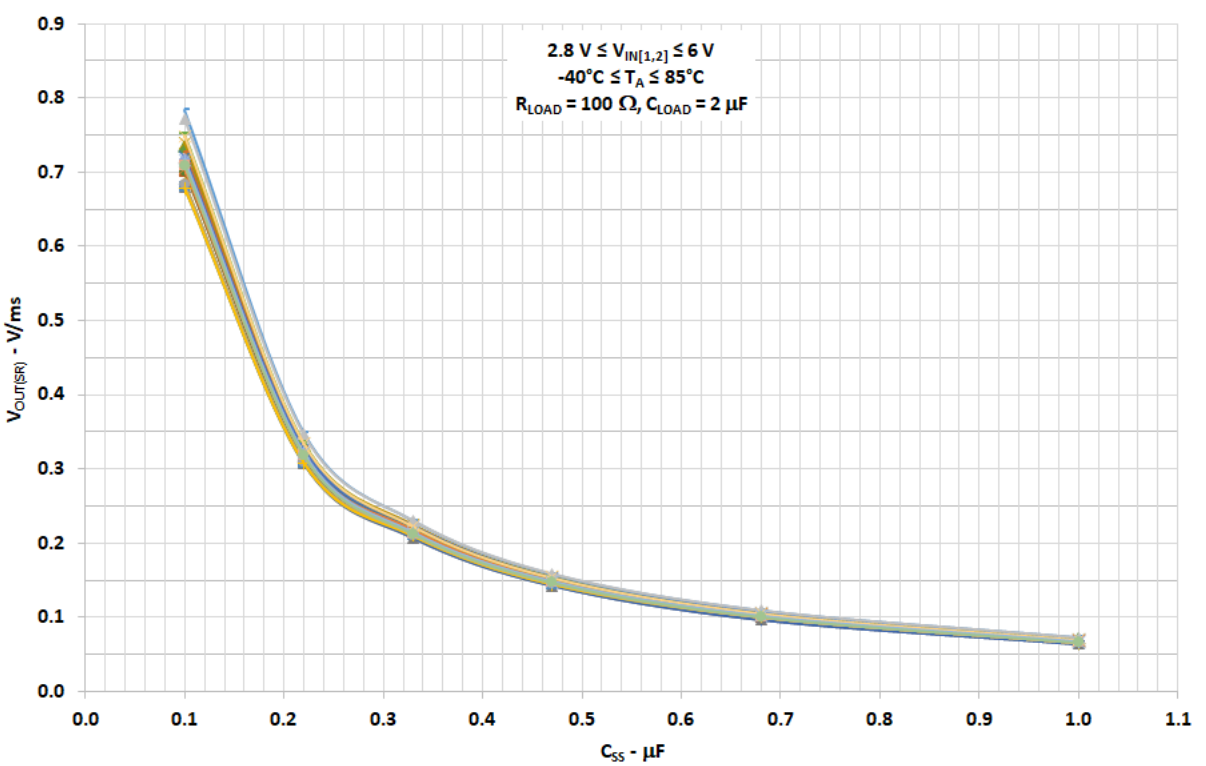


Typical Performance Characteristics

T_{Total_ON} vs C_{SS}, $V_{IN[1,2]}$, and Temperature



V_{OUT} Slew Rate vs C_{SS}, $V_{IN[1,2]}$, and Temperature



Typical Turn ON Operation Waveforms

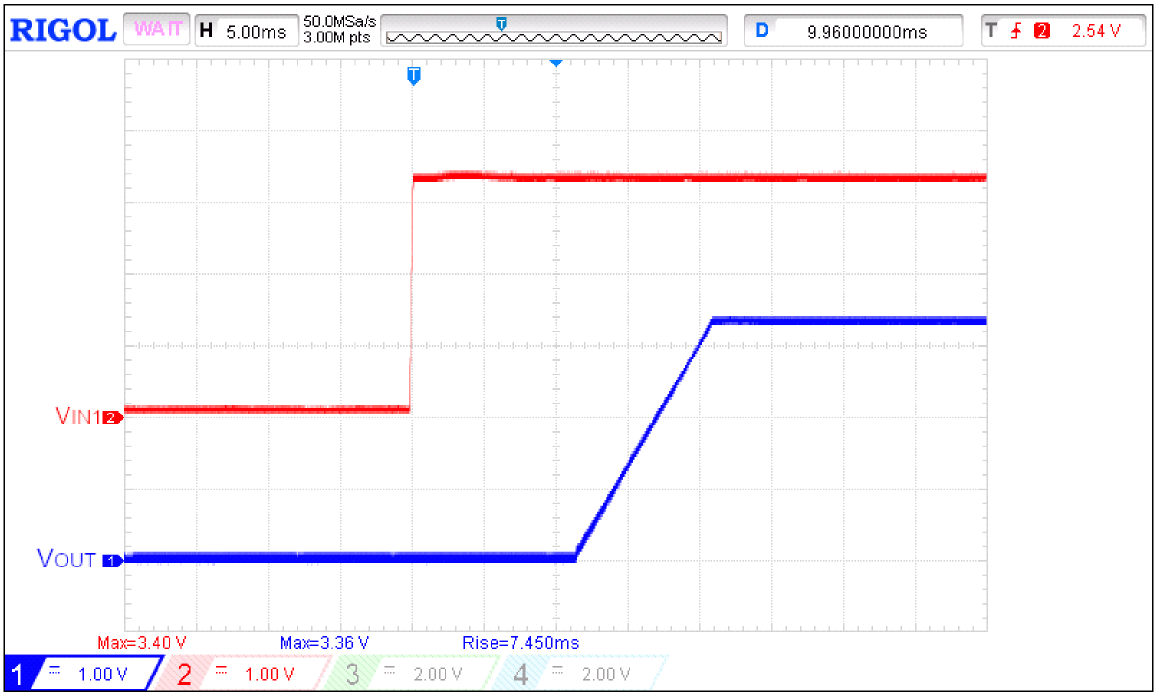


Figure 1. Typical Turn ON operation waveform for V_{IN1} = 3.3 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 μF

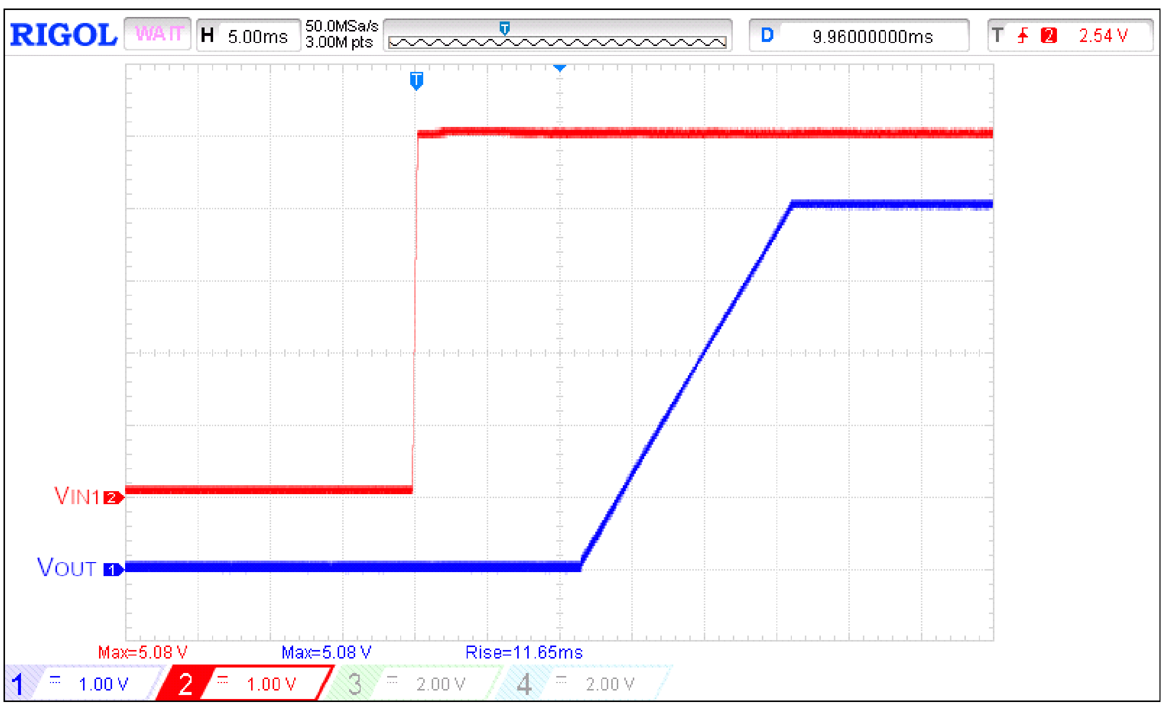


Figure 2. Typical Turn ON operation waveform for V_{IN1} = 5 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 μF

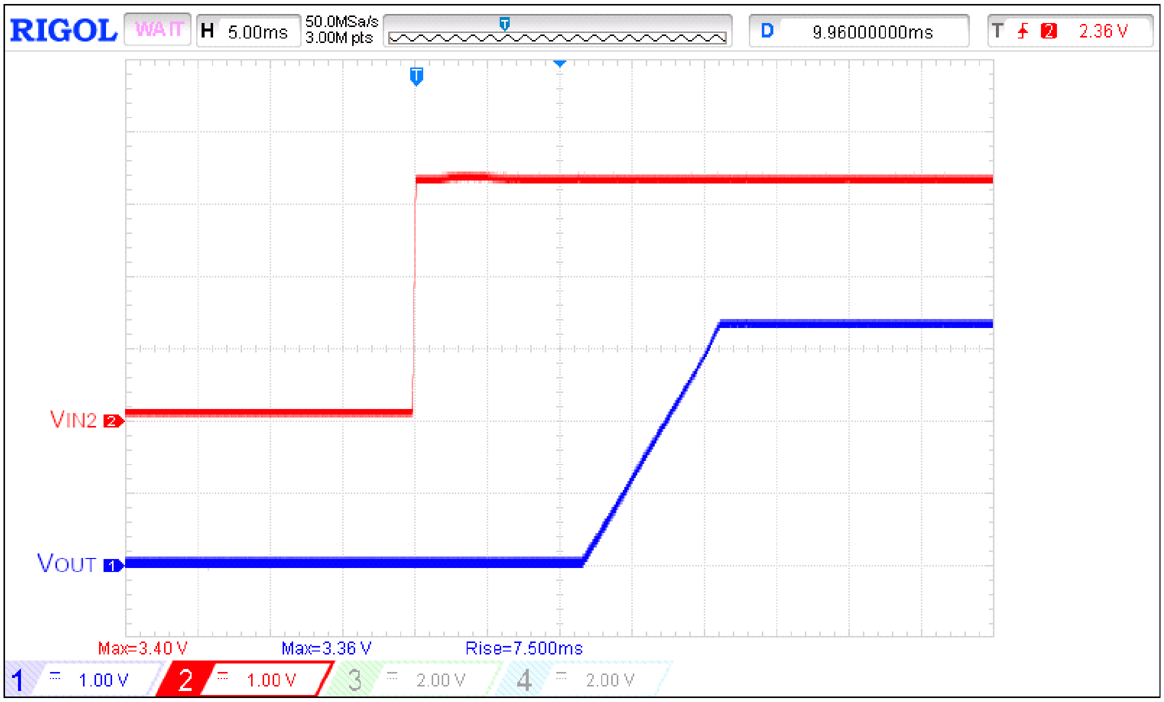


Figure 3. Typical Turn ON operation waveform for V_{IN2} = 3.3 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

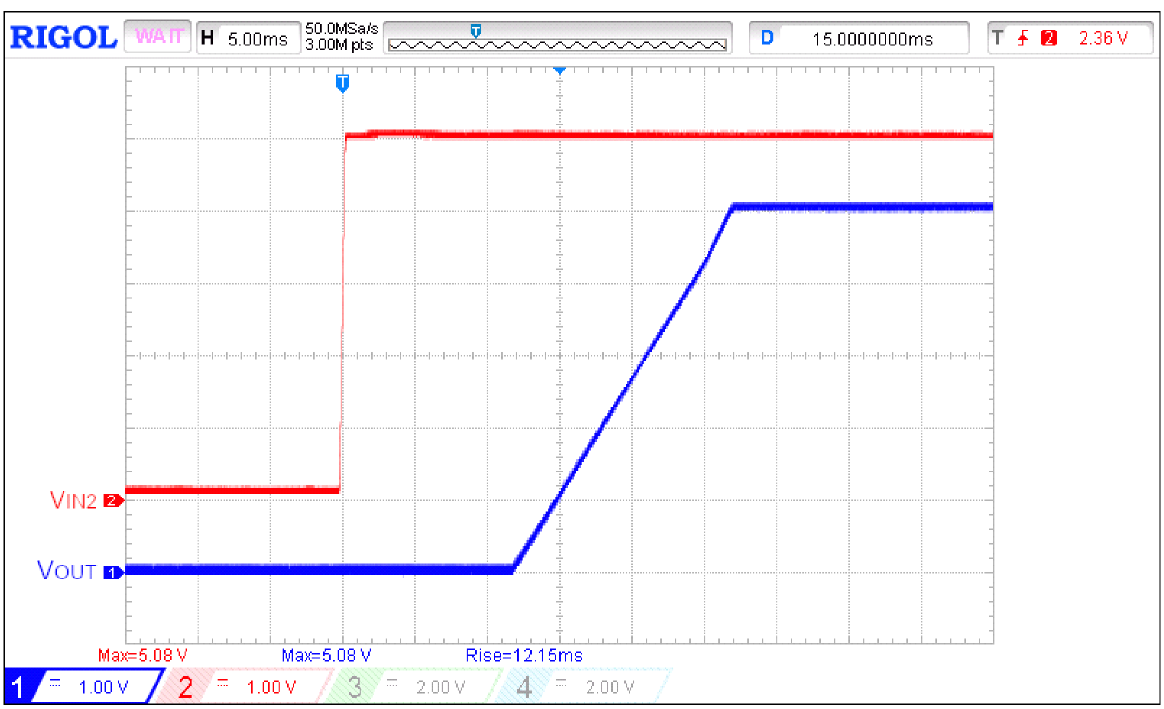


Figure 4. Typical Turn ON operation waveform for V_{IN2} = 5 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

Switchover Operation Waveforms

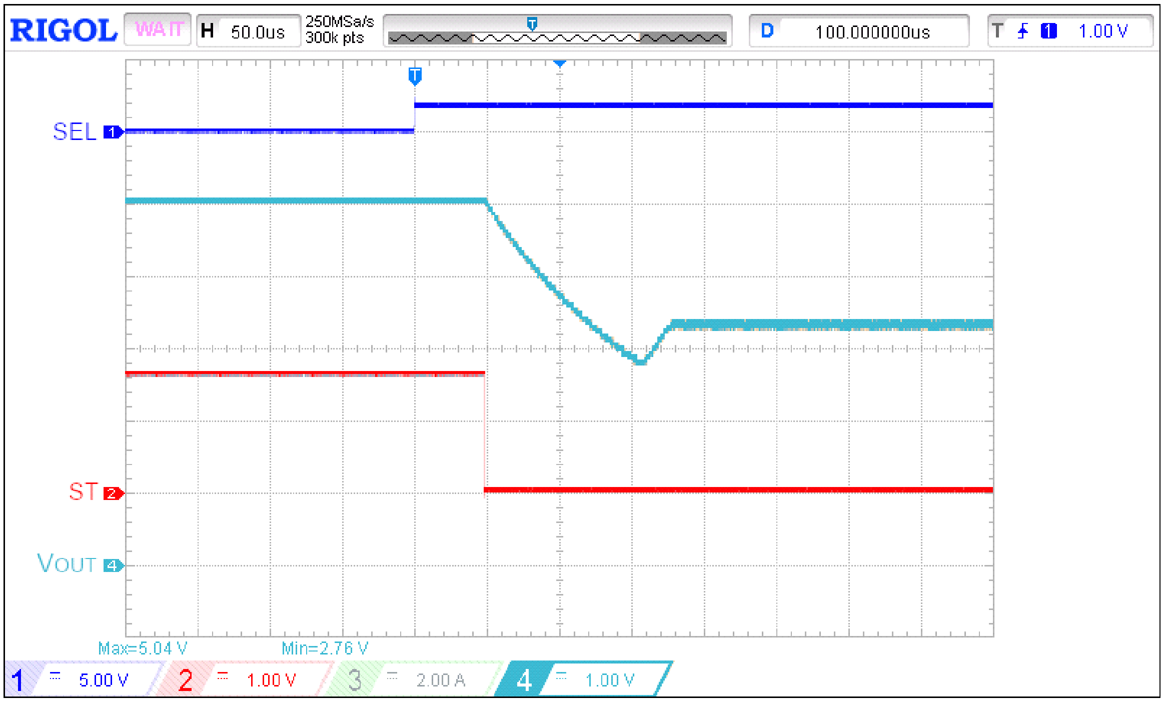


Figure 5. Switchover operation waveform for V_{IN1} = 5 V, V_{IN2} = 3.3 V, C_{SS} = 220 nF, PR = 0 V, SEL = Low -> High, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

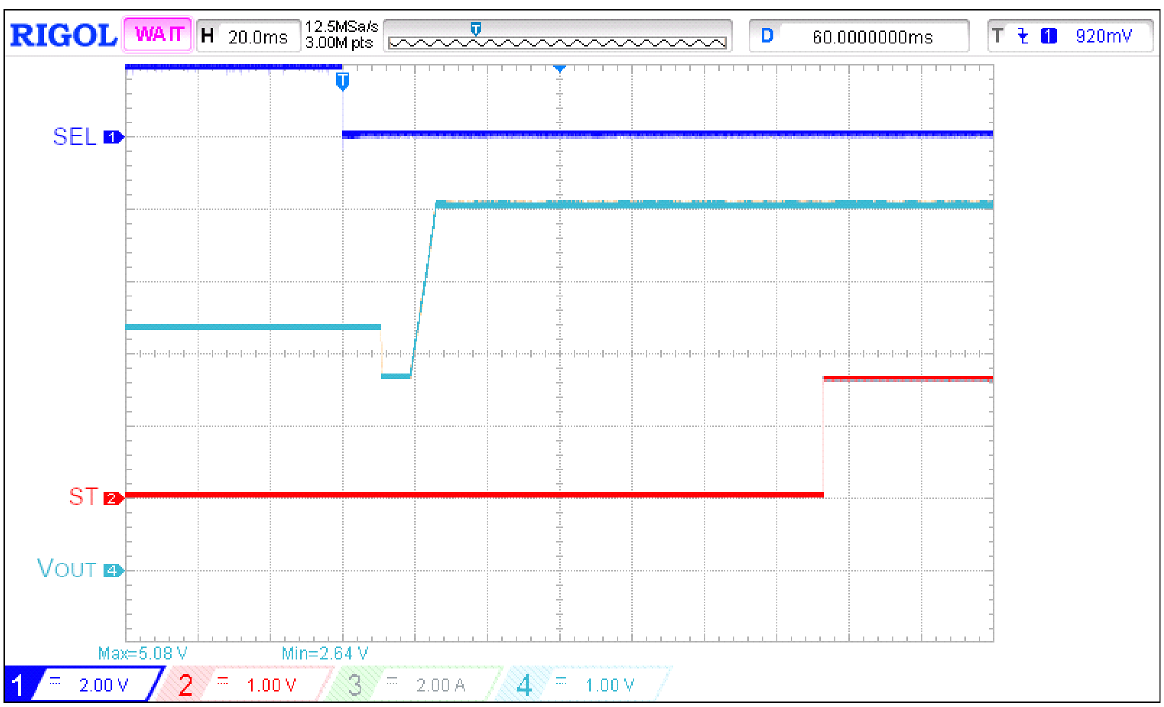


Figure 6. Switchover operation waveform for V_{IN1} = 5 V, V_{IN2} = 3.3 V, C_{SS} = 220 nF, PR = 0 V, SEL = High -> Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

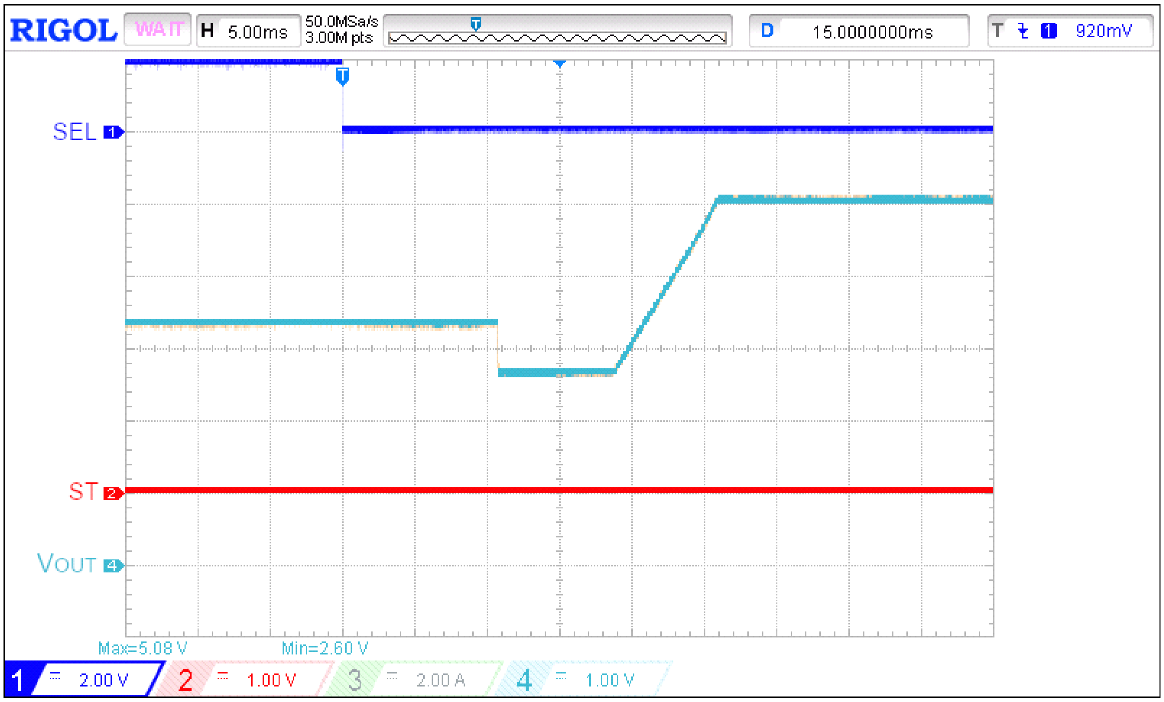


Figure 7. Switchover operation waveform for V_{IN1} = 5 V, V_{IN2} = 3.3 V, C_{SS} = 220 nF, PR = 0 V, SEL = High -> Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

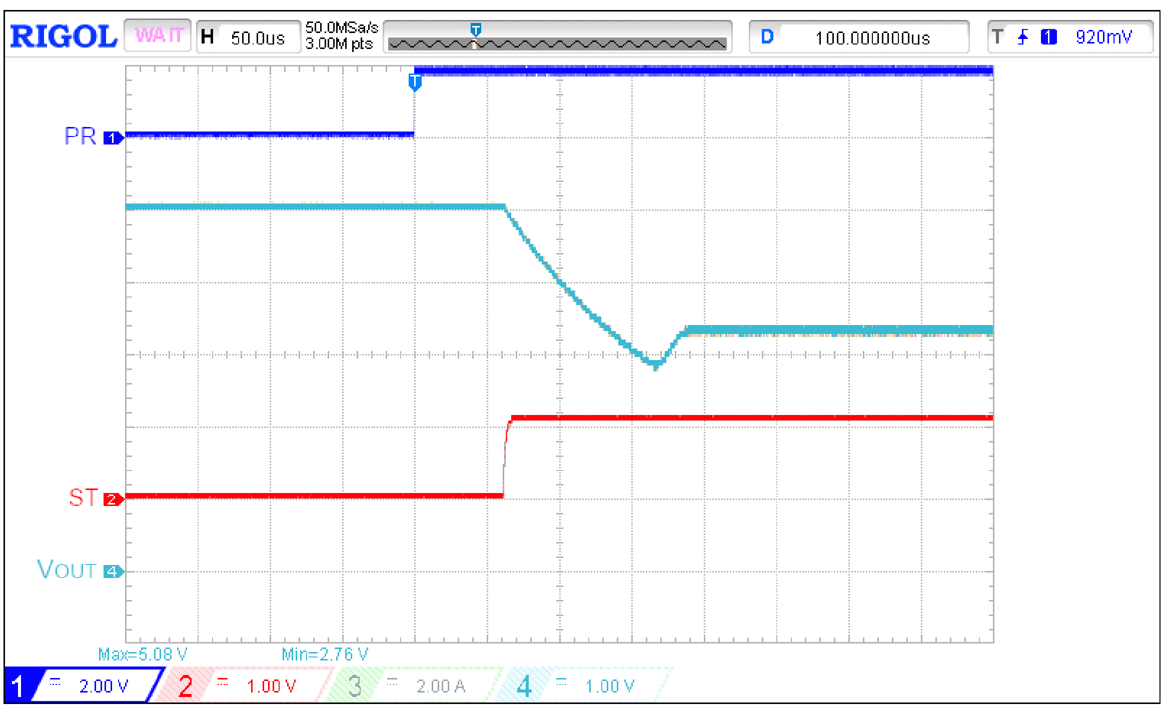


Figure 8. Switchover operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, C_{SS} = 220 nF, SEL = 0 V, PR = Low -> High, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

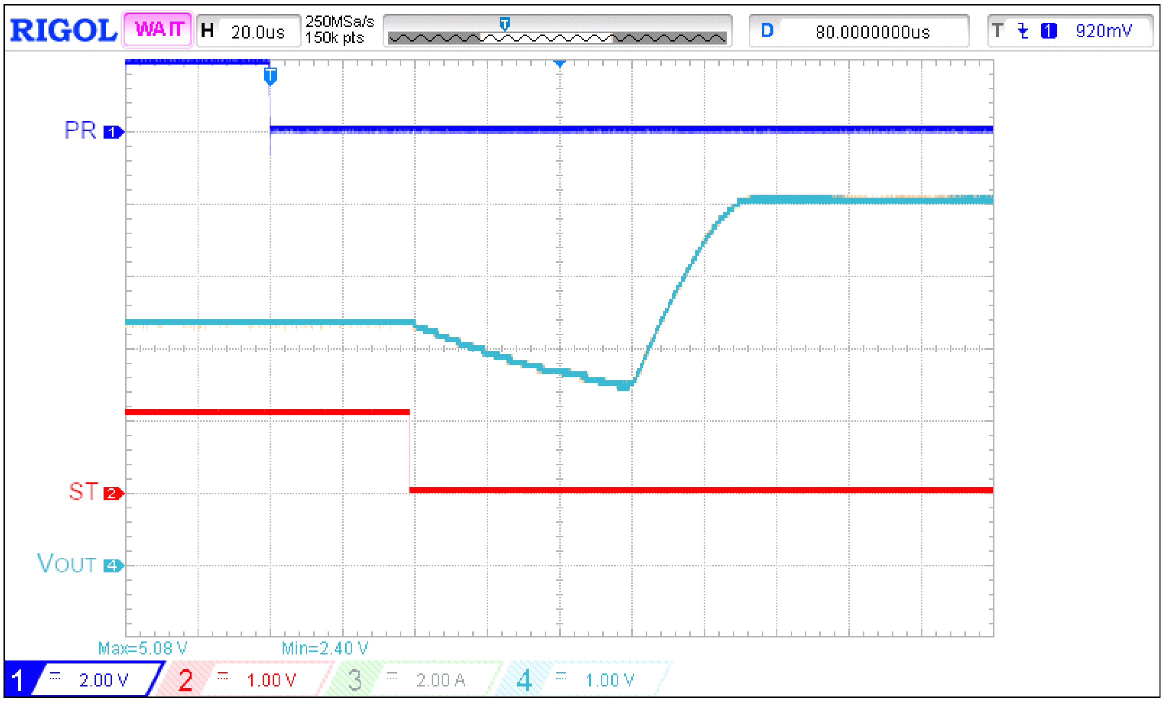


Figure 9. Switchover operation waveform for V_{IN1} = 3.3 V, V_{IN2} = 5 V, C_{SS} = 220 nF, SEL = 0 V, PR = High -> Low, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

Higher Voltage Level Priority Operation Waveforms

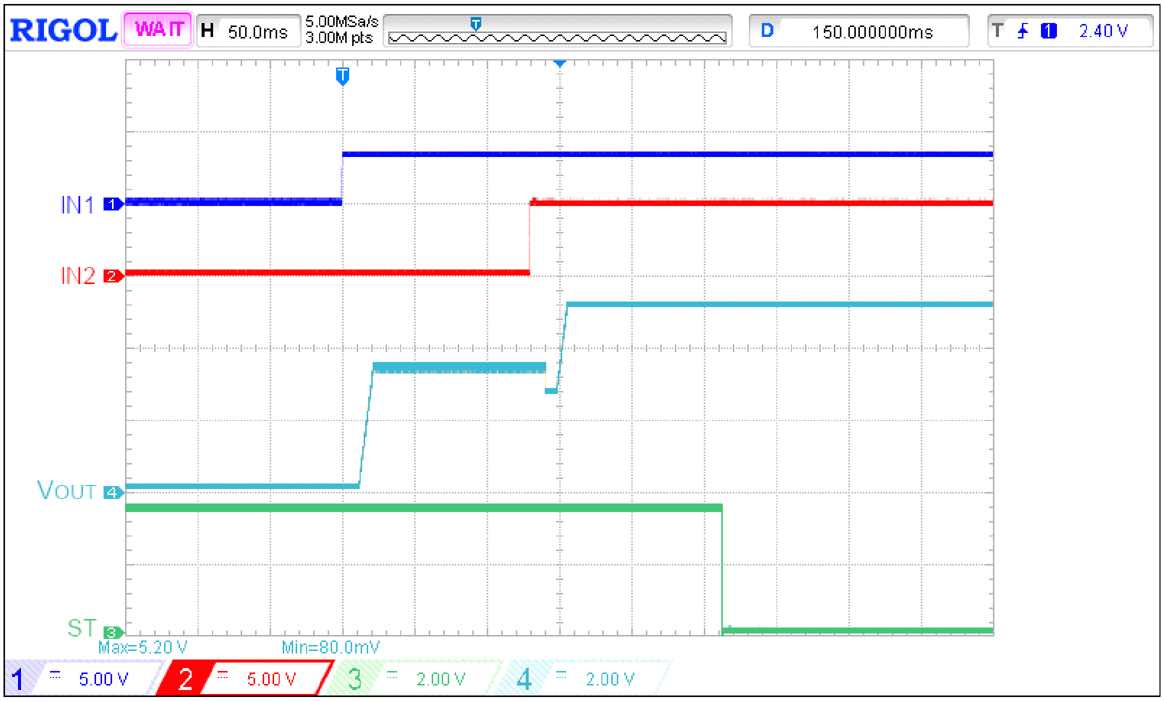


Figure 10. Higher voltage level priority operation waveform when IN2 is applied after first SS rise is done for V_{IN1} = 3.3 V, V_{IN2} = 5 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

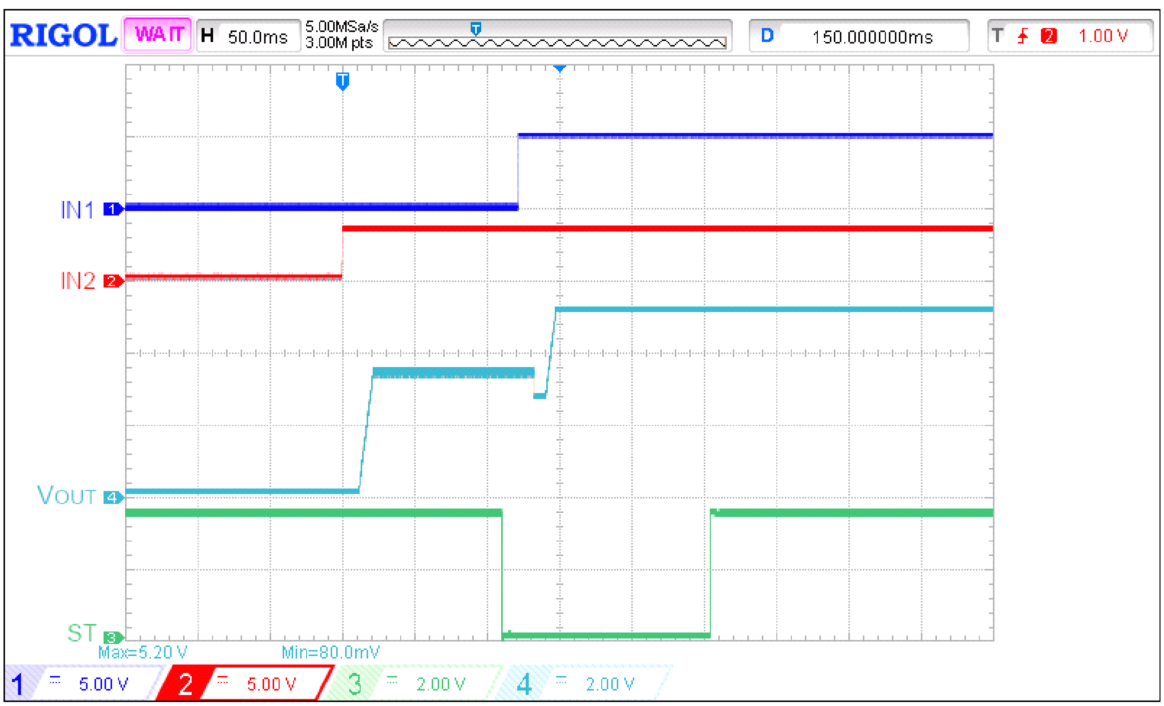


Figure 11. Higher voltage level priority operation waveform when IN1 is applied after first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

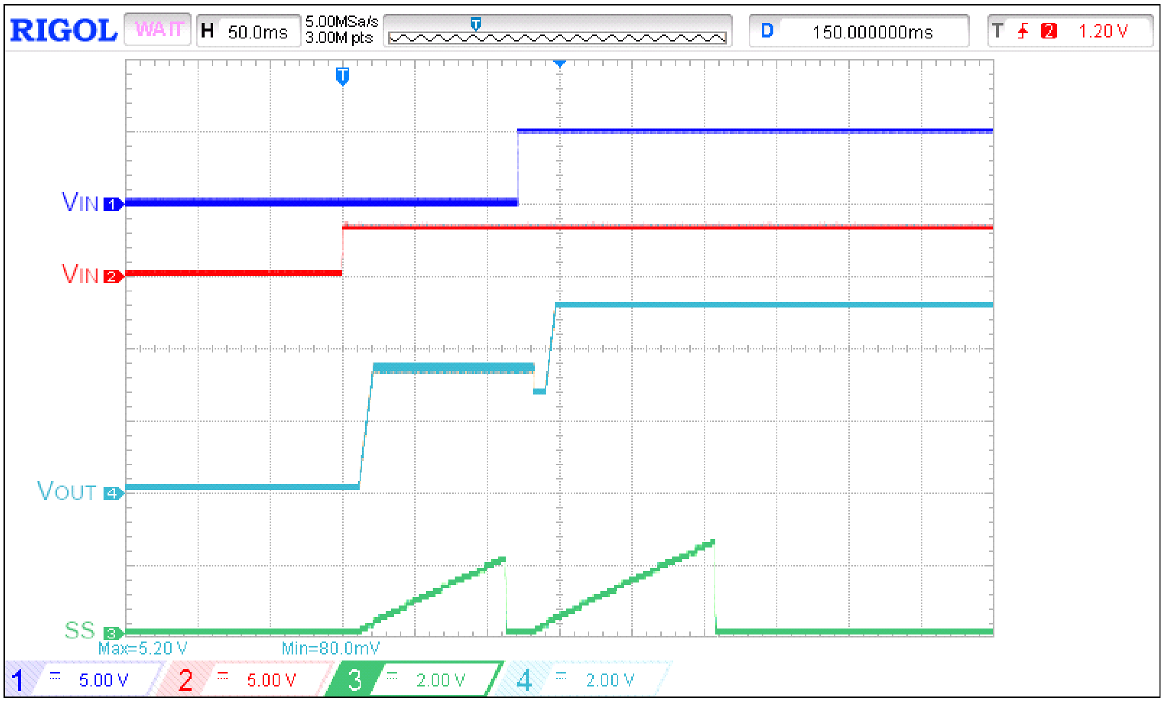


Figure 12. Higher voltage level priority operation waveform when IN1 is applied after first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 μF

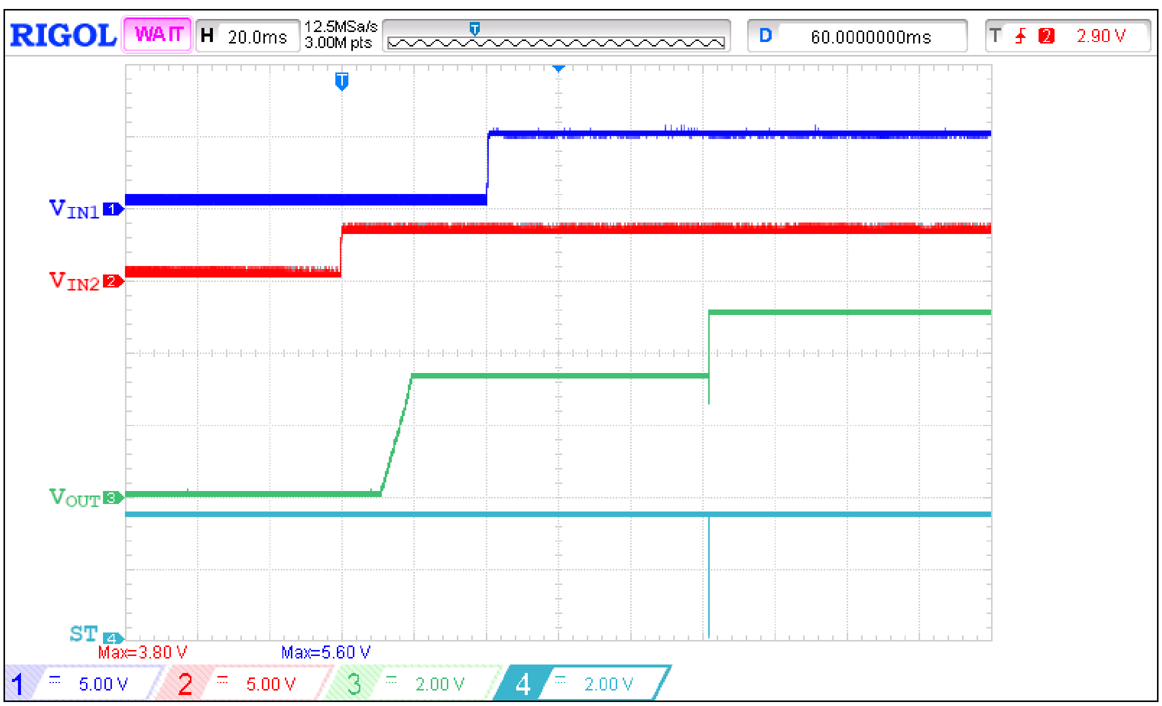


Figure 13. Higher voltage level priority operation waveform when IN1 is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 μF

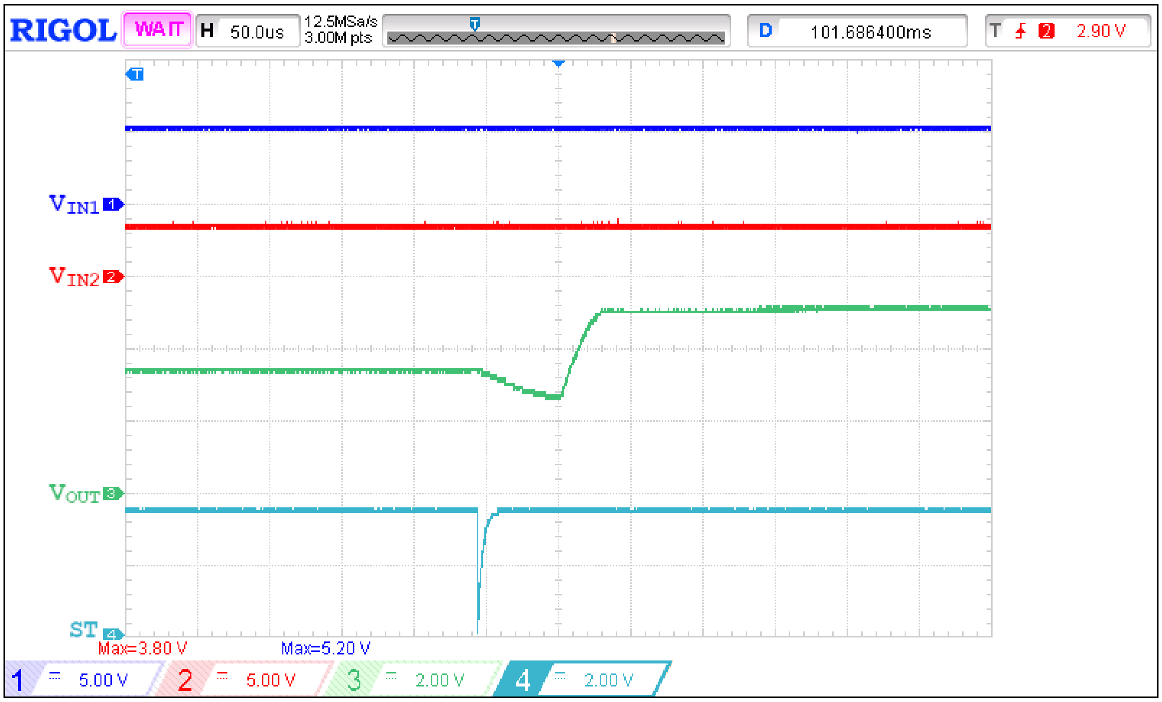


Figure 14. Higher voltage level priority operation waveform when IN1 is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF (extended view)

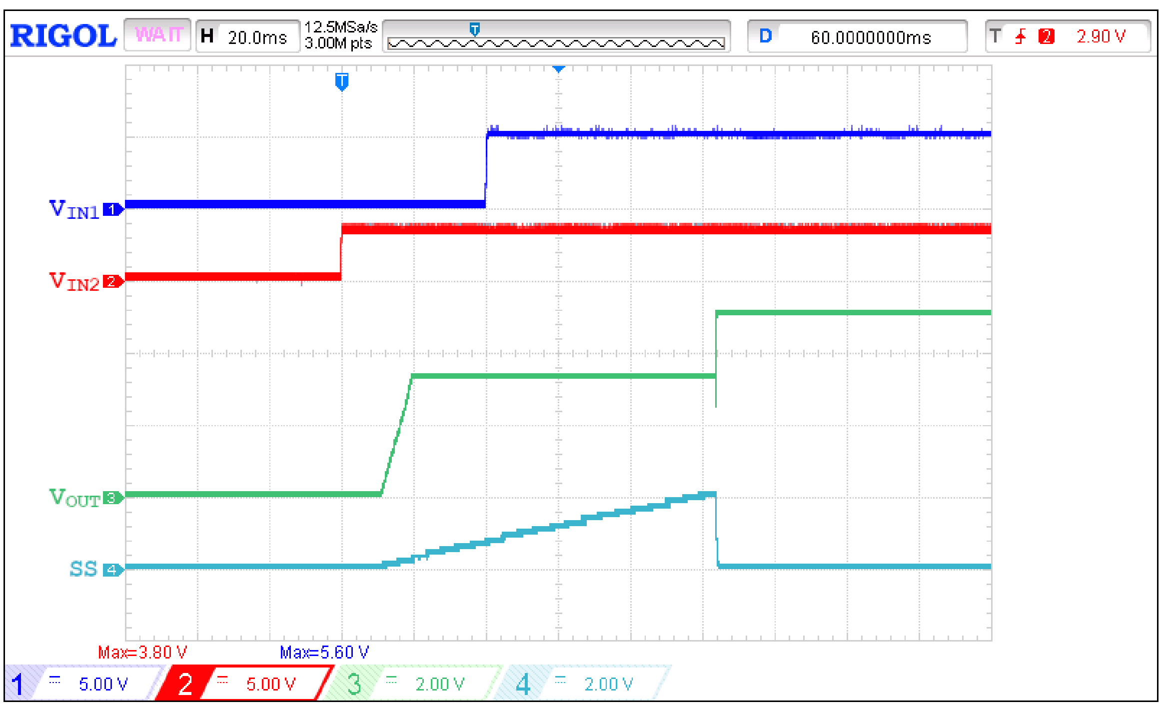


Figure 15. Higher voltage level priority operation waveform when IN1 is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 µF

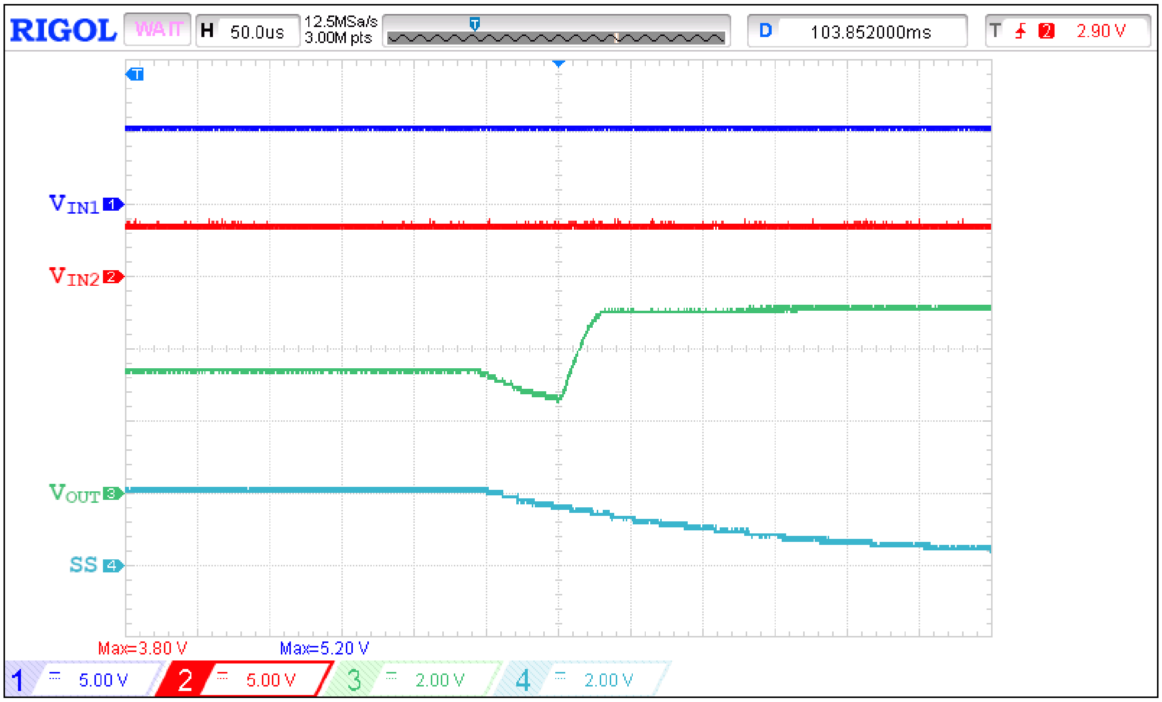


Figure 16. Higher voltage level priority operation waveform when IN1 is applied before first SS rise is done for V_{IN1} = 5 V, V_{IN2} = 3.3 V, SEL = 0 V, PR = 0 V, C_{SS} = 220 nF, R_{LOAD} = 100 Ω, C_{LOAD} = 2 μF (extended view)

Active Current Limit Operation Waveforms

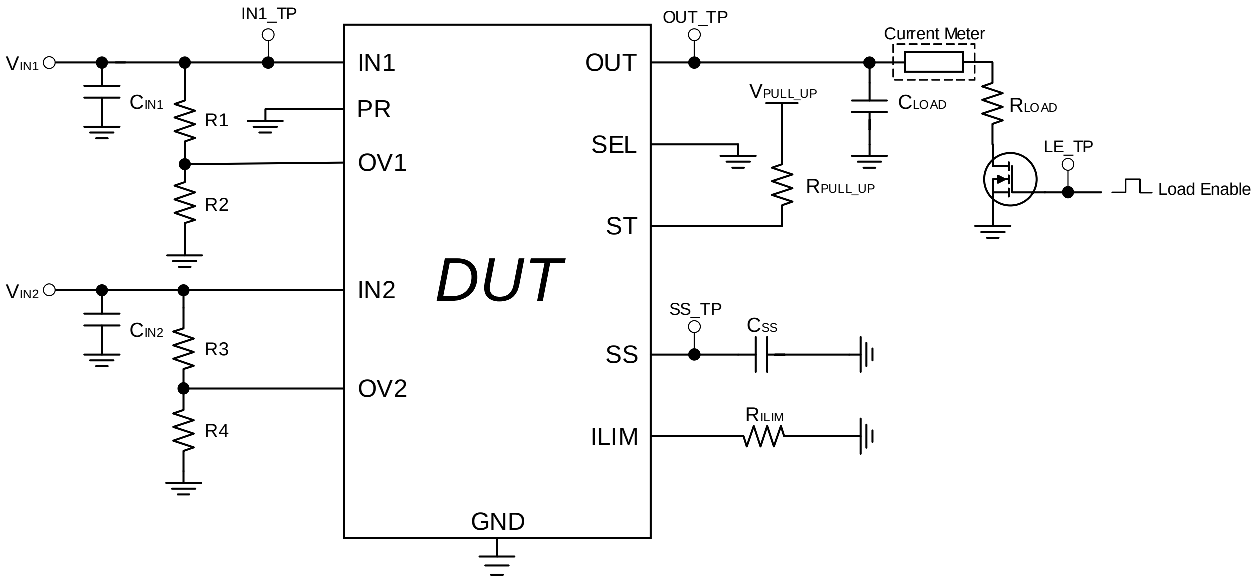


Figure 17. Test setup for Active Current Limit Operation

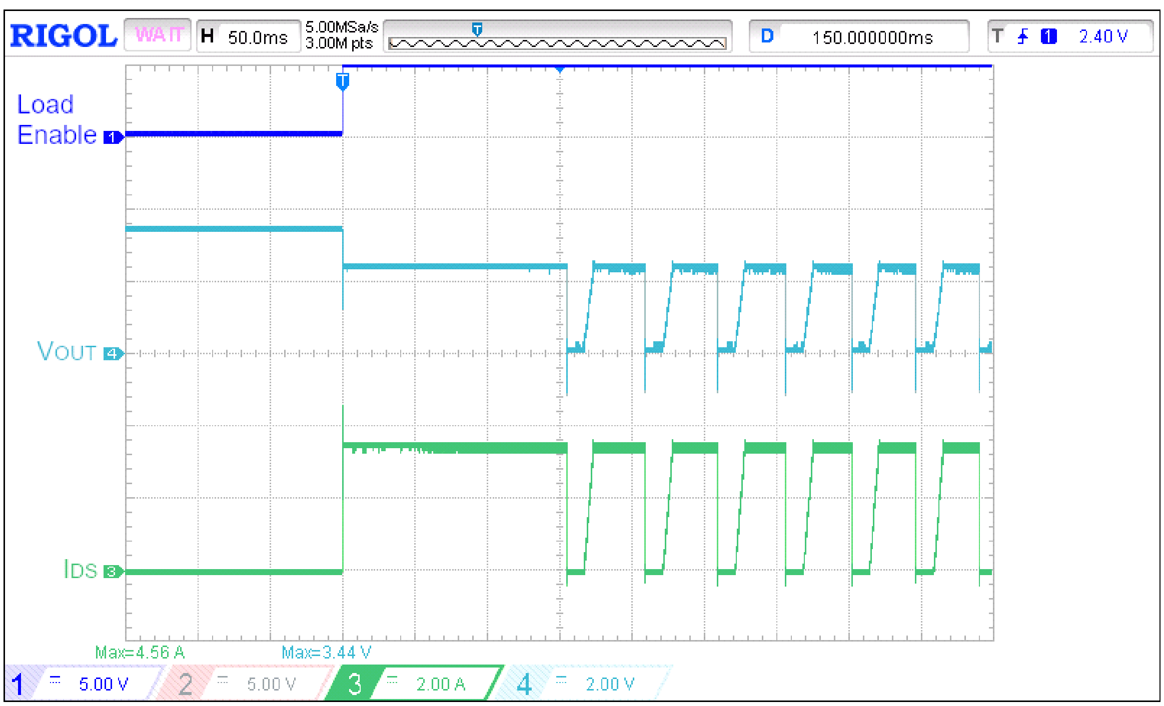


Figure 18. Active Current Limit operation waveform for V_{IN1} = 3.3 V, C_{SS} = 220 nF, R_{ILIM} = 31.6 kΩ, R_{LOAD} = 0.66 Ω, C_{LOAD} = 2 µF

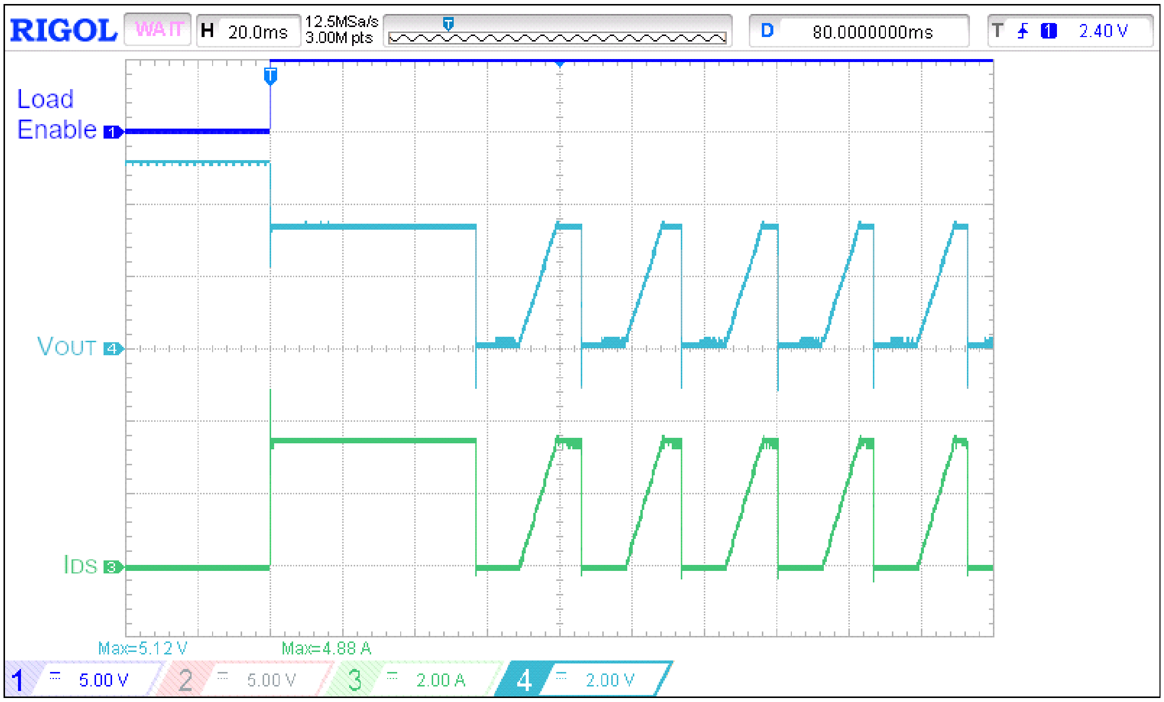


Figure 19. Active Current Limit operation waveform for V_{IN1} = 5 V, C_{SS} = 220 nF, R_{ILIM} = 31.6 kΩ, R_{LOAD} = 1 Ω, C_{LOAD} = 2 µF

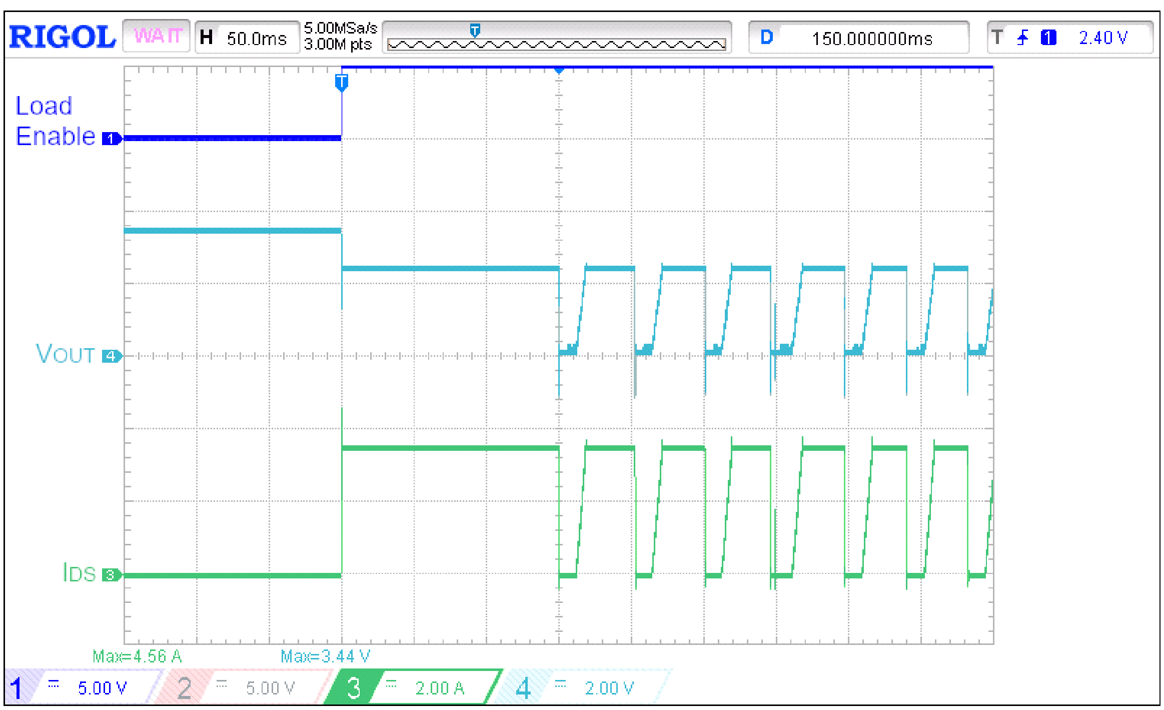


Figure 20. Active Current Limit operation waveform for V_{IN2} = 3.3 V, C_{SS} = 220 nF, R_{ILIM} = 31.6 kΩ, R_{LOAD} = 0.66 Ω, C_{LOAD} = 2 µF

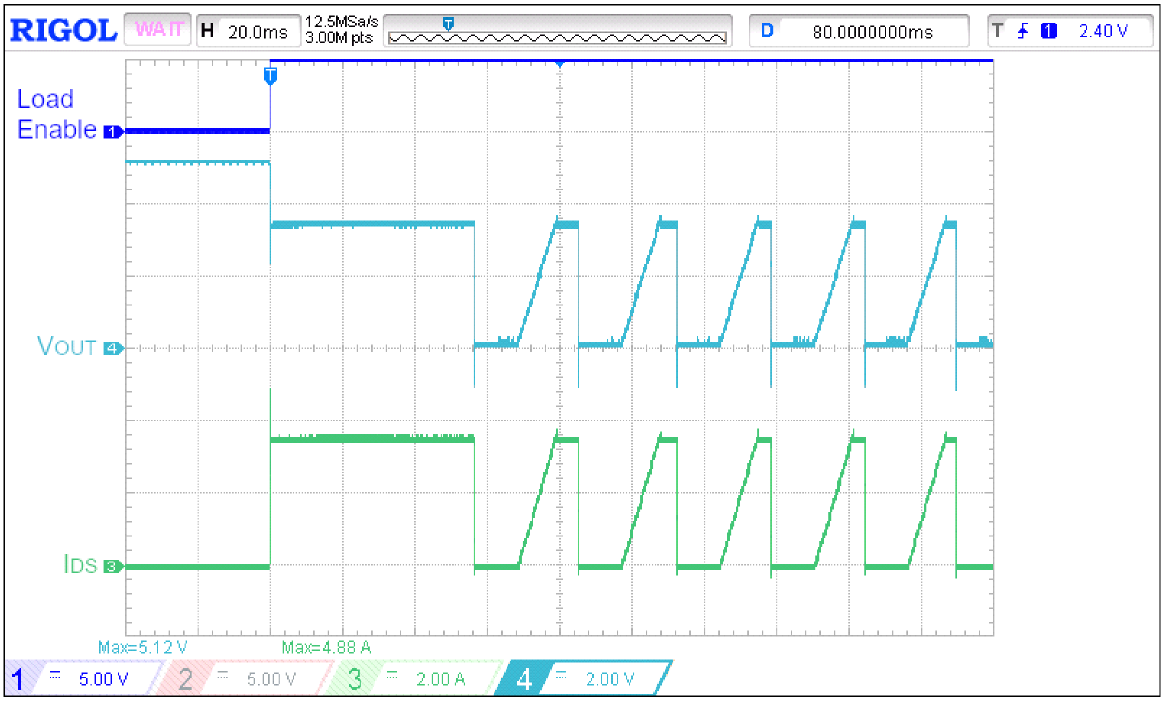


Figure 21. Active Current Limit operation waveform for V_{IN2} = 5 V, C_{SS} = 220 nF, R_{ILIM} = 31.6 kΩ, R_{LOAD} = 1 Ω, C_{LOAD} = 2 µF

APPLICATIONS INFORMATION

SLG59H1401C Power-Up Considerations

Once V_{IN1} voltage is valid ($V_{IN1} > V_{IN1(UVLO)}$ and V_{IN1} < Overvoltage lockout level set by OV1) and has priority under V_{IN2}, a turn on delay (T_{ON_Delay}) will occur and then, for soft start, output voltage start rising with slew rate ($V_{OUT(SR)}$) set by C_{SS} capacitor. After the total turn on time (T_{Total_ON}), soft start will not be used again for V_{IN1} until it becomes not valid ($V_{IN1} < V_{IN1(UVLO)}$ or V_{IN1} > Overvoltage lockout level set by OV1). When V_{IN2} voltage becomes valid ($V_{IN2} > V_{IN2(UVLO)}$ and V_{IN2} < Overvoltage lockout level set by OV2) and $V_{SEL} > V_{REF}$, a turn on delay (T_{ON_Delay}) will occur again and then, for soft start, output voltage start rising with slew rate ($V_{OUT(SR)}$) set by C_{SS} capacitor. After the total turn on time (T_{Total_ON}), soft start will not be used again for V_{IN2} until it becomes not valid ($V_{IN2} < V_{IN2(UVLO)}$ or V_{IN2} > Overvoltage lockout level set by OV2). If V_{IN2} becomes valid and selected before V_{OUT} ends rising with V_{IN1}, the V_{OUT} switching procedure to V_{IN2} will start after V_{OUT} rising has ended with V_{IN1}.

This is an example of power up procedure when V_{IN1} is applied before V_{IN2}. In case V_{IN2} is applied before V_{IN1} the procedure will be similar.

Soft Start introduction

The output voltage slew rate can be configured by changing the C_{SS} capacitance. The Table below shows the typical slew rate and T_{Total_ON} time across C_{SS} capacitance, $V_{IN[1,2]}$, and Temperature from -40 °C to 85 °C for R_{LOAD} = 100 Ω and C_{LOAD} = 2 µF.

Typical Slew rate and T_{Total_ON} time across C_{SS} capacitance, $V_{IN[1,2]}$, and Temperature from -40 °C to 85 °C for R_{LOAD} = 100 Ω and C_{LOAD} = 2 µF.

C_{SS}, µF	$V_{OUT(SR)}$, V/ms	T_{Total_ON}, ms			
	$V_{IN[1,2]}$ = 2.8 V to 5.5 V	$V_{IN[1,2]}$ = 2.8 V	$V_{IN[1,2]}$ = 3.3 V	$V_{IN[1,2]}$ = 5.0 V	$V_{IN[1,2]}$ = 5.5 V
0.1	0.72	14.7	15.4	17.7	18.5
0.22	0.32	19.1	20.7	25.8	27.4
0.47	0.15	28.4	31.7	42.7	46.2
1.0	0.065	48.3	56.1	80.4	88.4

Resistor Divider Calculations for Overvoltage Protection and Operating Mode Selection

To set the overvoltage threshold for OV1 and OV2, and V_{PR} and V_{SEL} levels, a typical voltage divider, illustrated in Figure 22 is used.

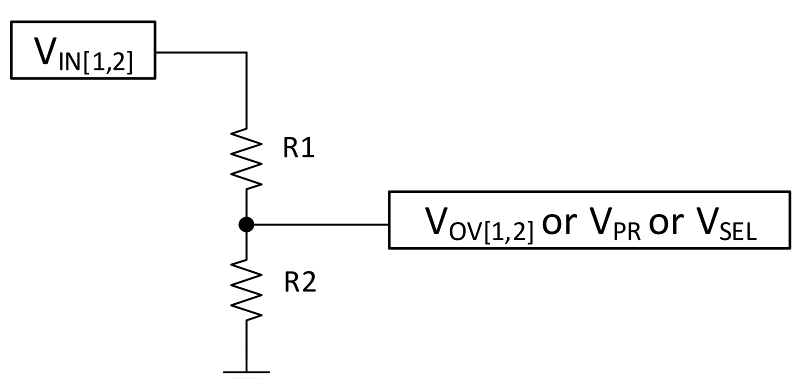


Figure 22. Typical Resistive Voltage Divider

In order to calculate the voltage divider, the equation below is used

$$R1 = \frac{R2 \times (V_{IN[1,2]} - V_{REF})}{V_{REF}}$$

where:

R1 = calculated resistor value in kΩ;

R2 = resistor closest to ground. Recommended R2 value is 5 kΩ;

$V_{IN[1,2]}$ = V_{IN1} or V_{IN2} voltage level at which protection should be triggered;

V_{REF} = Internal voltage reference for OV1, OV2, PR and SEL pins.

Using SLG59H1401C in OR'ing applications

In the case of OR'ing two supplies, if both power rails are valid, then the higher voltage is passed to the output. If one of the power rails suddenly disappears, then output OUT is automatically switched to the other available power rail. If both power rails have equal voltage levels, then based on the V_{COMP} spec, IN2 has higher priority and will be switched to OUT. If V_{IN2} falls below the V_{COMP} Hysteresis, then IN1 will switch to OUT. To set SLG59H1401C in OR'ing mode, connect the PR and SEL pins to GND or V_{PR} and V_{SEL} should be < V_{REF}.

OV1 and OV2 with external resistors connected to IN1 and IN2 respectively can be configured to provide overvoltage protection.

The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the ST pin is high, IN1 is the output or the output is Hi-Z. If the ST pin is low, IN2 is the output.

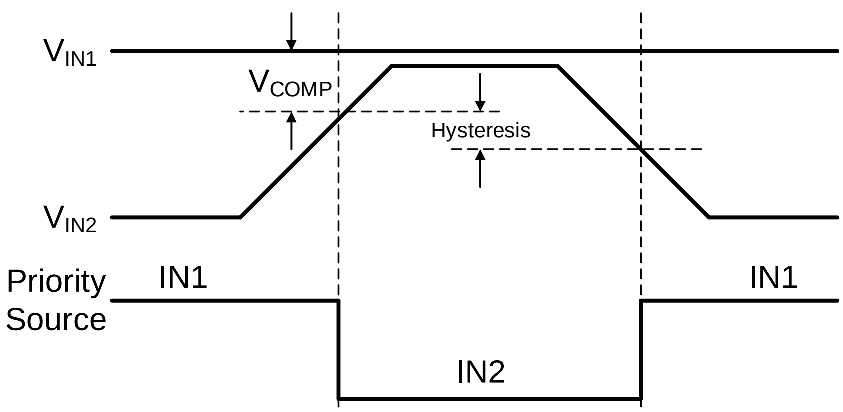


Figure 23. V_{COMP} Priority Source Selection

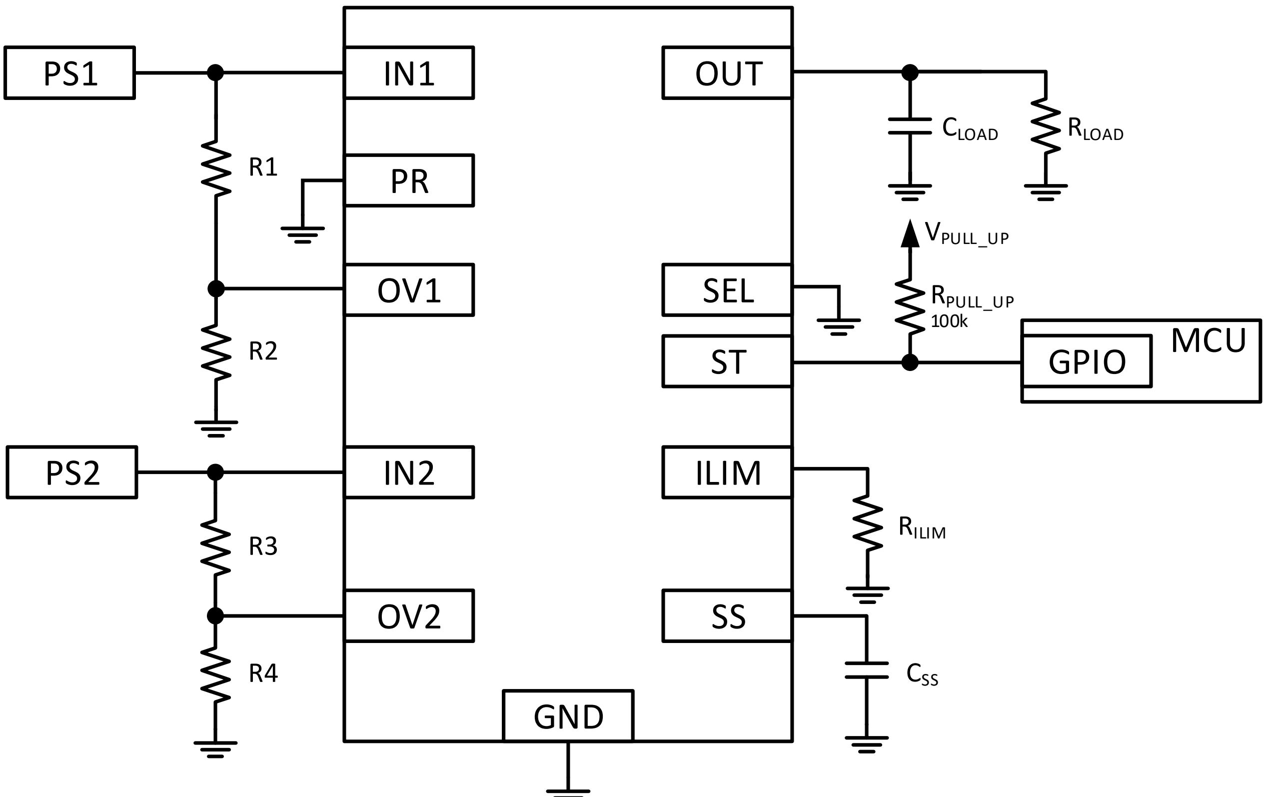


Figure 24. Connection diagram of using SLG59H1401C in OR'ing applications

Using SLG59H1401C in manual power rail selection applications

In the case of using the SLG59H1401C in a manual power rail selection application, an external voltage ≥ V_{REF} should be applied at the PR pin through a pull up resistor. If $V_{PR} \geq V_{REF}$ and $V_{SEL} < V_{REF}$, then IN1 will be selected. By toggling $V_{SEL} \geq V_{REF}$, IN2 will be selected.

OV1 and OV2 with external resistors connected to IN1 and IN2 respectively can be configured to provide overvoltage protection.

The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the ST pin is high, IN1 will be at output or the output is Hi-Z. If the pin is low, IN2 will be at output.

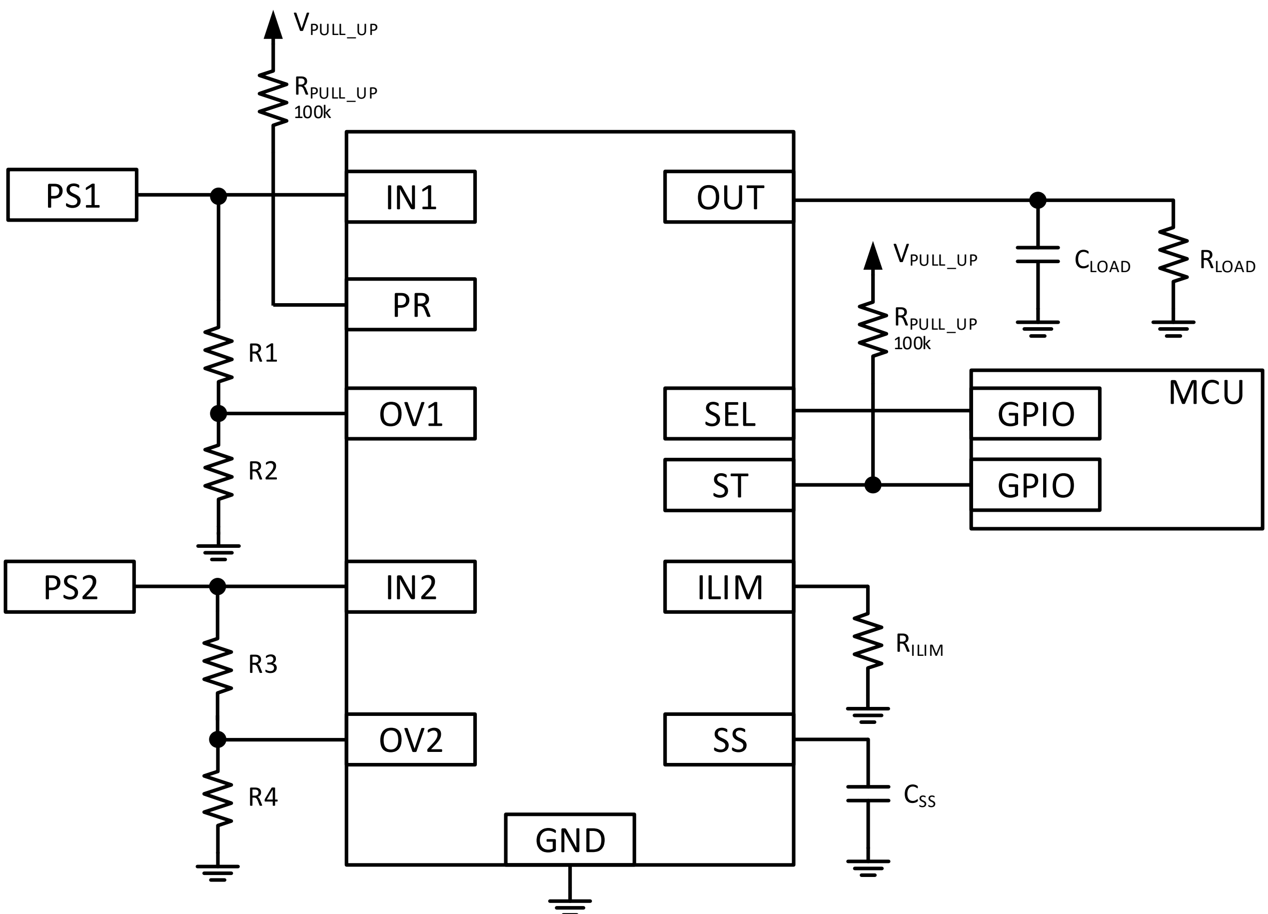


Figure 25. Connection diagram of using SLG59H1401C in manual power rail selection applications

Using SLG59H1401C in manual power rail selection applications with priority

In the case of using SLG59H1401C in applications where automatic and manual switching is required, the PR pin must be connected through the common voltage divider R1, R2, R3 to IN1 as illustrated in Figure 26. When V_{IN1} falls to induce $V_{PR} < V_{REF}$ and $V_{SEL} < V_{REF}$, SLG59H1401C will operate in VCOMP mode and largest voltage will be on the output. If $V_{SEL} \geq V_{REF}$ then IN2 will be selected.

OV1 and OV2 with external resistors are connected to IN1 and IN2 respectively and can be configured to provide overvoltage protection.

The ST pin can be pulled high with a resistor to provide feedback on the status of the system. If the ST pin is high, IN1 will be at the output or the output is Hi-Z. If the pin is low, IN2 will be at the output.

.

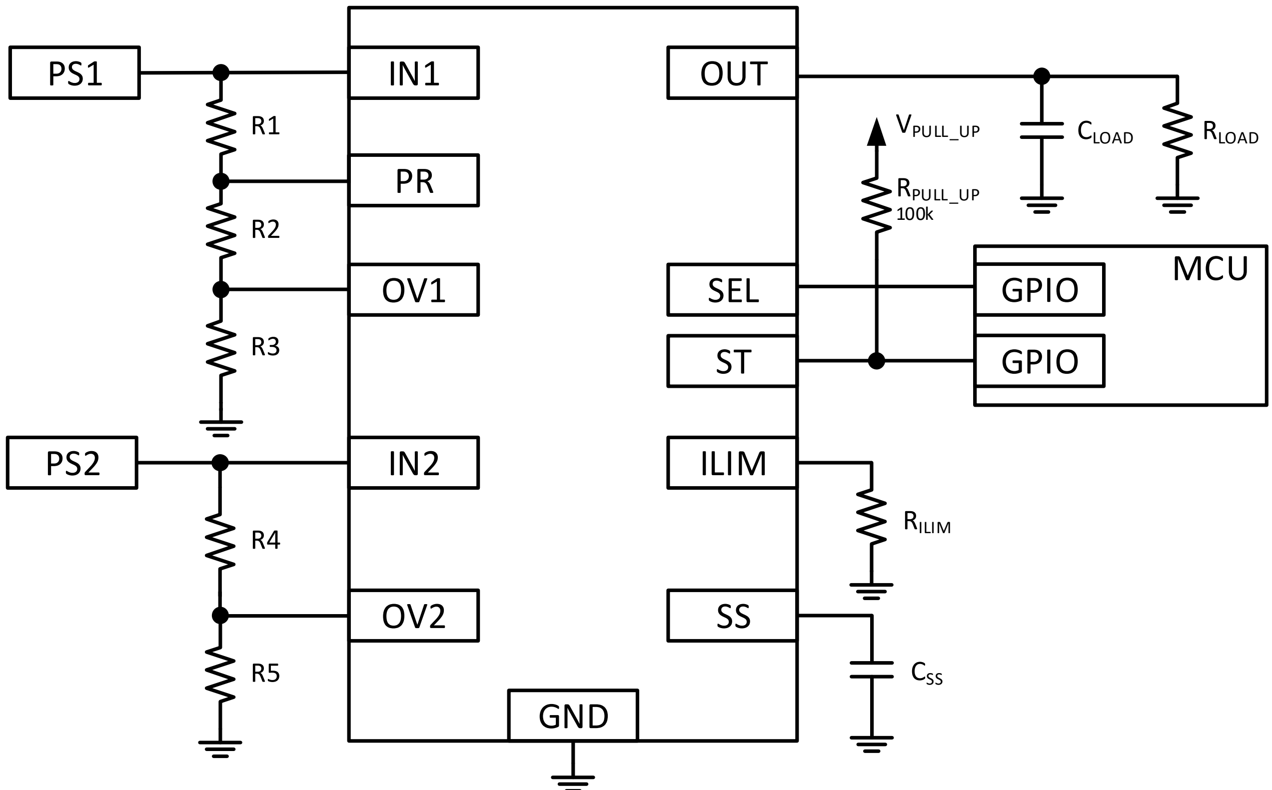


Figure 26. Connection diagram of using SLG59H1401C in manual power rail selection applications with priority

Resistor divider for this type of application solution is calculated in two steps:

1. Calculate voltage divider section for OV1 threshold:

$$R_{COMMON} = \frac{R3 \times (V_{IN1} - V_{REF})}{V_{REF}}$$

where:

R_{COMMON} = calculated common resistance value for R1 + R2 in kΩ;
R3 = resistor closest to ground. Recommended R3 value is 5 kΩ;
V_{IN1} = V_{IN1} voltage at which overvoltage protection should be triggered;
V_{REF} = Internal voltage reference for OV1 pin.

2. Calculate voltage divider section for priority threshold:

$$R1 = \frac{(R_{COMMON} + R3) \times (V_{IN1} - V_{REF})}{V_{IN1}}$$

$$R2 = R_{COMMON} - R1$$

where:

R_{COMMON} = calculated common resistance value for R1 + R2 in kΩ;

R1, R2 = resistors near PR pin;

R3 = resistor closest to ground. Recommended R3 value is 5 kΩ;

V_{IN1} = V_{IN1} voltage at which PR threshold should be triggered;

V_{REF} = Internal voltage reference for OV1 and PR pins.

SLG59H1401C Current Limiting

The SLG59H1401C has two modes of current limiting

1. Standard Current Limiting Mode (with Thermal Protection)

The output current is initially limited to the Active Current Limit specification given in the Electrical Characteristics table. The current limiting circuit is very fast and responds within a few micro-seconds to sudden loads. When overload is sensed, the current limiting circuit increases the FET resistance to keep the current from exceeding the Active Current Limit.

The ACL level can be adjusted by choosing the appropriate ±1%-tolerance R_{ILIM} value and can be calculated by the following equations:

For R_{ILIM} range from 31.6 kΩ to 100 kΩ:

$$I_{ACL} = 69.1 / R_{ILIM}^{0.861}$$

where:

R_{ILIM} = Resistor on ILIM pin, in kOhms (kΩ)

However, if an overload condition persists, the die temperature rise due to the increased FET resistance while at maximum current can activate Thermal Protection. If the die temperature exceeds the $THERM_{ON}$ specification, the FET is shut completely OFF, allowing the die to cool. When the die cools to the $THERM_{OFF}$ temperature, the FET is allowed to turn back on. This process may repeat as long as the overload condition is present.

2. Short Circuit Current Limiting Mode (with Thermal Protection)

In the case of a hard short, such as a solder bridge on the power rail, the current is limited to protect the chip. Thermal Protection is also present and may be activated during Short Circuit Current Limit protection operation.

Fast Reverse Current Blocking (RCB)

Each channel has Always ON Reverse Current Blocking. If the output is forced above the selected input by V_{IRCB}, the channel will switch off to stop the reverse current I_{RCB} within t_{RCB}. As the output falls to within the V_{RCB} of V_{IN}, the selected channel will quickly turn back on to avoid unnecessary voltage drops during fast switchover (t_{SW}).

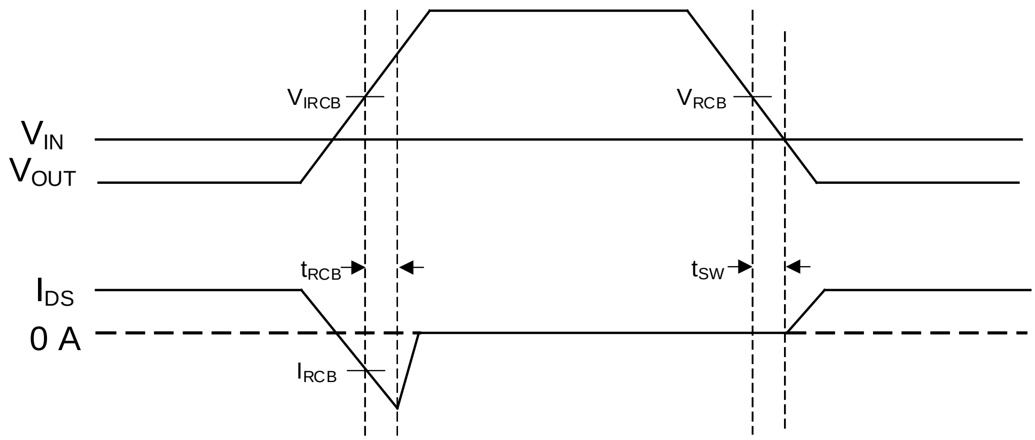


Figure 27. Reverse Current Blocking Behavior

Power Dissipation

The junction temperature of the SLG59H1401C depends on factors such as board layout, ambient temperature, external air flow over the package, load current, and the RDS_{ON}-generated voltage drop across each load switch. While the primary contributor to the increase in the junction temperature of the SLG59H1401C is the power dissipation of its load switches, its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD_{TOTAL} = (RDS_{ON[1,2]} \times I_{DS[1,2]}{}^2)$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$RDS_{ON[1,2]}$ = Channel 1 and Channel 2 load switch ON resistance, in Ohms (Ω), respectively

$I_{DS[1,2]}$ = Channel 1 and Channel 2 Output current, in Amps (A), respectively

and

$$T_J = PD_{TOTAL} \times \theta_{JA} + T_A$$

where:

T_J = Die junction temperature, in Celsius degrees (°C)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt (°C/W) – highly dependent on pcb layout

T_A = Ambient temperature, in Celsius degrees (°C)

In nominal operating mode, the SLG59H1401C's power dissipation can also be calculated by taking into account the voltage drop across each load switch ($V_{IN[1,2]} - V_{OUT}$) and the magnitude of that channel's output current ($I_{DS[1,2]}$):

$$PD_{TOTAL} = (V_{IN[1,2]} - V_{OUT}) \times I_{DS[1,2]}$$

$$PD_{TOTAL} = (V_{IN[1,2]} - (R_{LOAD} \times I_{DS[1,2]})) \times I_{DS[1,2]}$$

where:

PD_{TOTAL} = Total package power dissipation, in Watts (W)

$V_{IN[1,2]}$ = Channel 1 and Channel 2 Input Voltage, in Volts (V), respectively

R_{LOAD} = Output Load Resistance, in Ohms (Ω)

$I_{DS[1,2]}$ = Channel 1 and Channel 2 output current, in Amps (A), respectively

V_{OUT} = Output voltage, or $R_{LOAD} \times I_{DS[1,2]}$

Layout Guidelines:

1. Since the IN[1,2] and OUT pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with an absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in Figure 28, illustrates proper techniques for heat to transfer as efficiently as possible out of the device;

2. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input $C_{IN[1,2]}$ and output C_{LOAD} low-ESR capacitors as close as possible to the SLG59H1401C's IN[1,2] and OUT pins;

3. The GND pin should be connected to system analog or power ground plane.

SLG59H1401C Evaluation Board:

A High Voltage GreenFET Evaluation Board for SLG59H1401C is designed according to the statements above and is illustrated on Figure 28. Please note that evaluation board has IN[1,2]_Sense and OUT_Sense pads. They cannot carry high currents and dedicated only for $RDS_{ON[1,2]}$ evaluation.

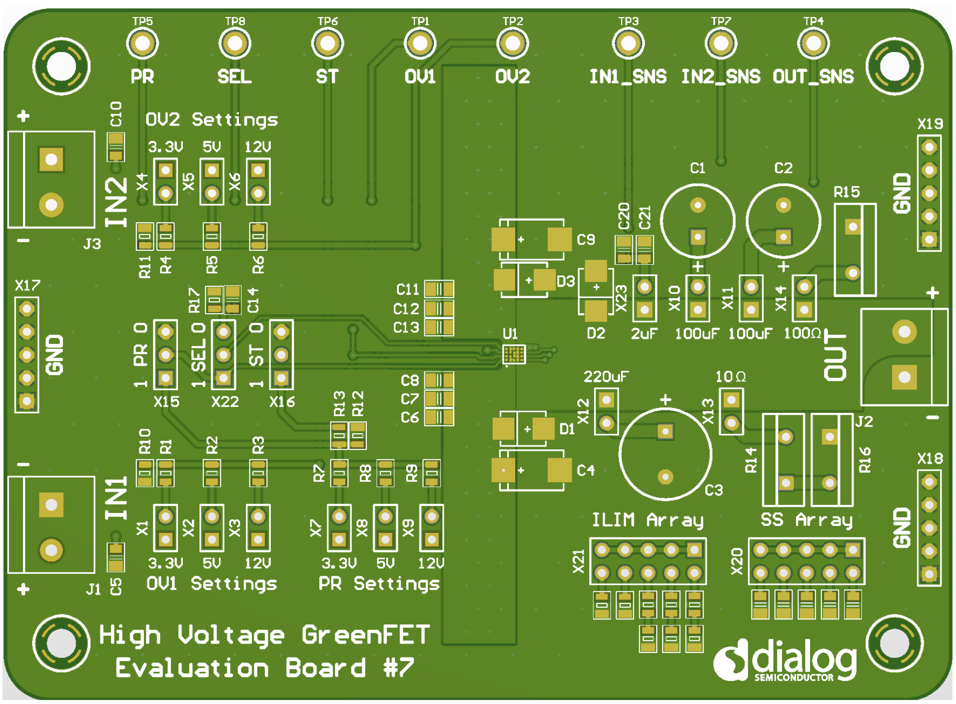


Figure 28. SLG59H1401C Evaluation Board

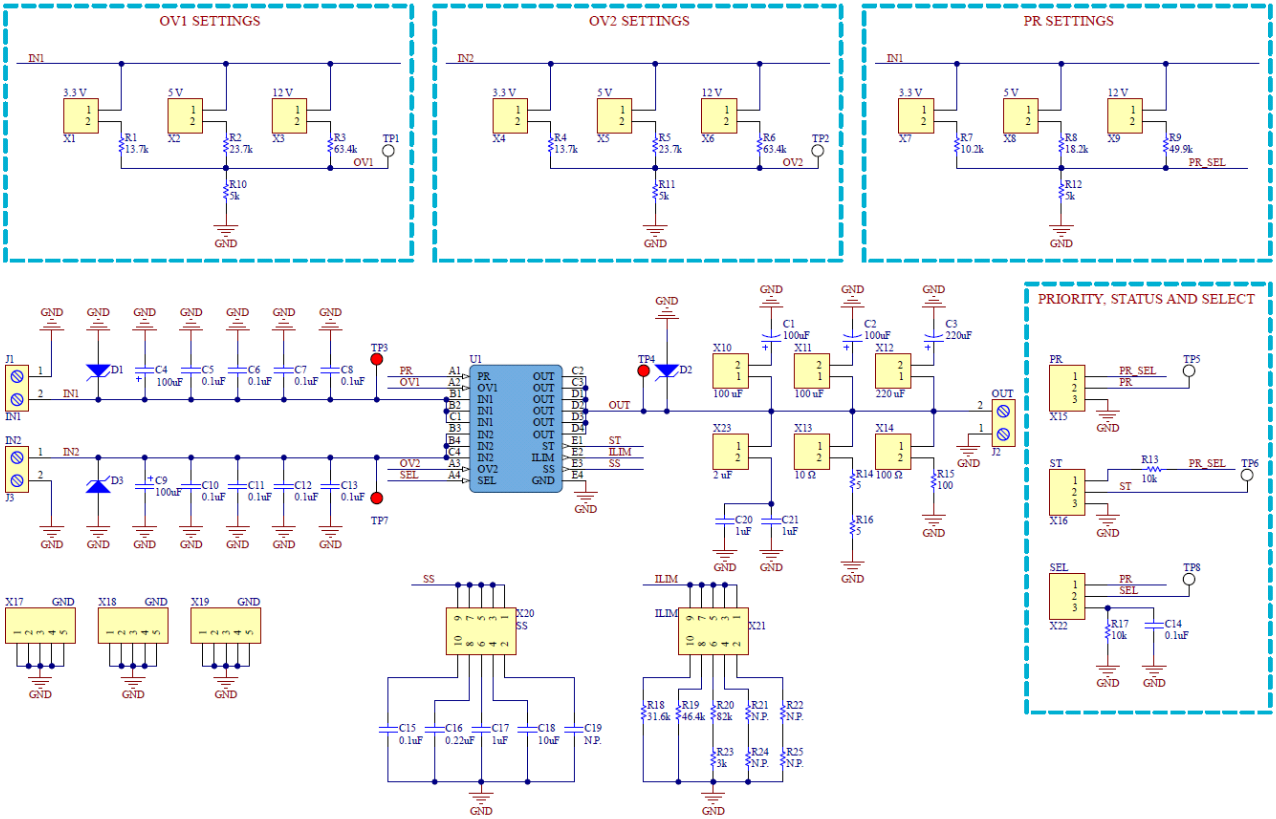


Figure 29. SLG59H1401C Evaluation Board Schematic

Basic EVB Configuration

1. Connect oscilloscope probes to IN[1,2], OUT, ST etc.;

2. Connect jumpers on X1-X3 and X4-X6 to configure overvoltage protection threshold for Channel 1 and Channel 2 respectively. Jumpers for OV[1,2] Settings sets the typical operating input voltage, and the overvoltage protection threshold will be 20% higher than that setting. For example, if jumper for OV1 Settings is located at 3.3 V position – overvoltage threshold is 3.96 V, and etc.

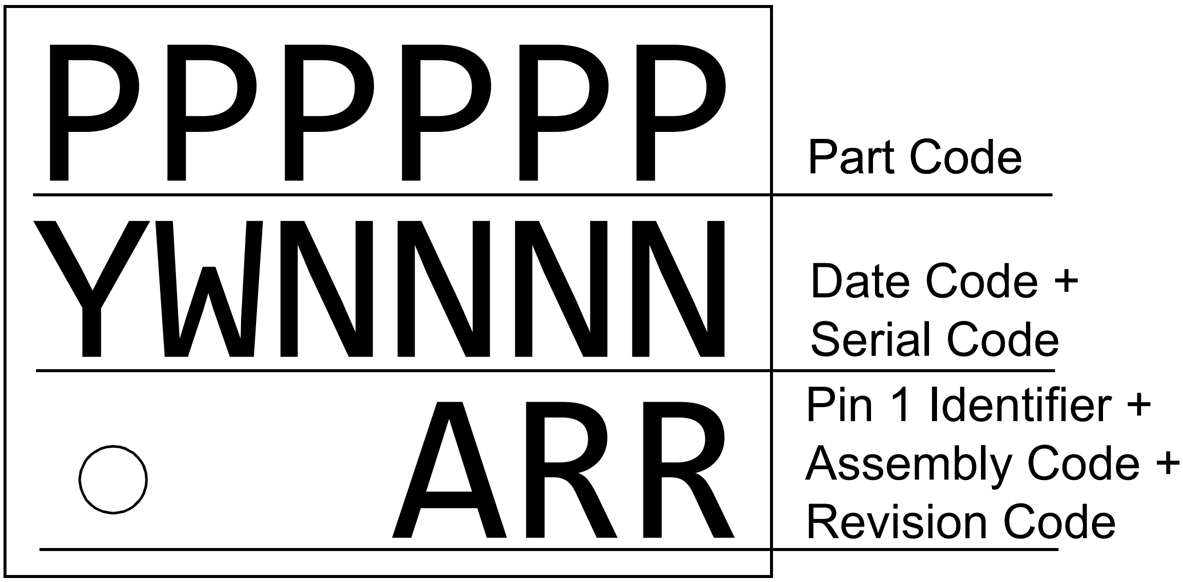
3. Connect jumpers on X7-X9 to configure the PR level. Jumper for PR Settings sets the typical operating input voltage in Priority mode. If the input voltage falls below the typical operating voltage level by around 4%…5%, V_{PR} will be lower than V_{REF} and SLG59H1401C will operate in VCOMP mode.

4.Configure SS and ILIM using X20 and X21 respectively. For more information, please refer to the Soft start introduction section and SLG59H1401C Current Limiting section in this Datasheet.

5. Select the desired operation mode using X15, X22 and connect a Pull-Up resistor to ST pin using X16. For more information regarding different operation modes please refer to the SLG59H1401C Normal Operation State Table in this datasheet.

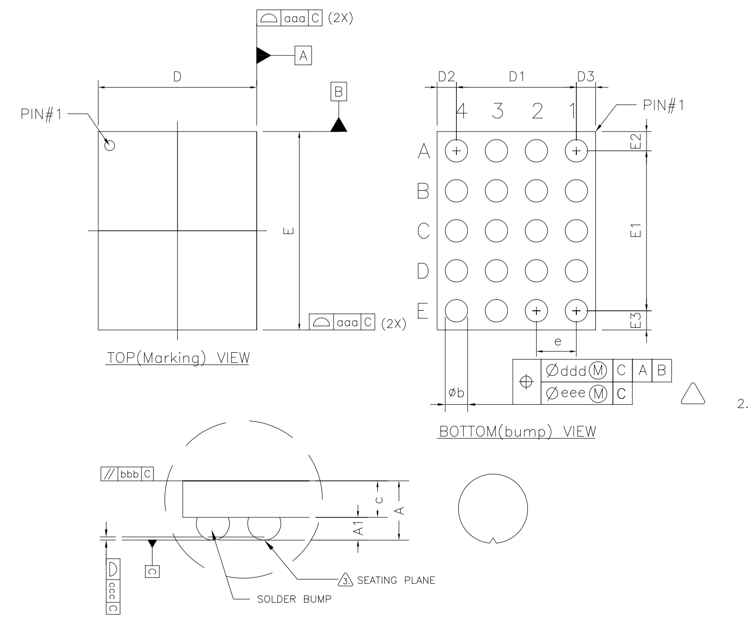
6. Logic High for the SEL pin configuration is connected to the PR pin signal. This means that in order to apply a High state to the SEL pin, it needs to apply logic High to the PR signal first. Such a configuration allows it to work in manual channel selection mode to switchover between Channel 1 and Channel 2 regardless of voltage levels on $V_{IN[1,2]}$.

Package Top Marking System Definition



Package Drawing and Dimensions

20 Lead WLCSP Package 1.985 mm x 1.585 mm



Symbol	Dimensions in mm			Dimensions in inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.4400	0.4700	0.5000	0.0173	0.0185	0.0197
A1	0.1500	0.1650	0.1800	0.0059	0.0065	0.0071
c	0.2800	0.3050	0.3300	0.0110	0.0120	0.0130
D	1.5600	1.5850	1.6100	0.0614	0.0624	0.0634
E	1.9600	1.9850	2.0100	0.0772	0.0781	0.0791
b	0.1950	0.2250	0.2550	0.0077	0.0089	0.0100
D1	---	1.2000	---	---	0.0472	---
D2	---	0.1925	---	---	0.0076	---
D3	---	0.1925	---	---	0.0076	---
E1	---	1.6000	---	---	0.0630	---
E2	---	0.1925	---	---	0.0076	---
E3	---	0.1925	---	---	0.0076	---
e	---	0.4000	---	---	0.0157	---
aaa	---	0.025	---	---	0.001	---
bbb	---	0.060	---	---	0.002	---
ccc	---	0.030	---	---	0.001	---
ddd	---	0.050	---	---	0.002	---
eee	---	0.050	---	---	0.002	---

NOTE:

1. CONTROLLING DIMENSION : MILLIMETER.
2. DIMENSION IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER, PARALLEL TO PRIMARY DATUM C
3. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS
4. THE SOLDER BALL SIZE PRIOR REFLOW IS 210 UM.

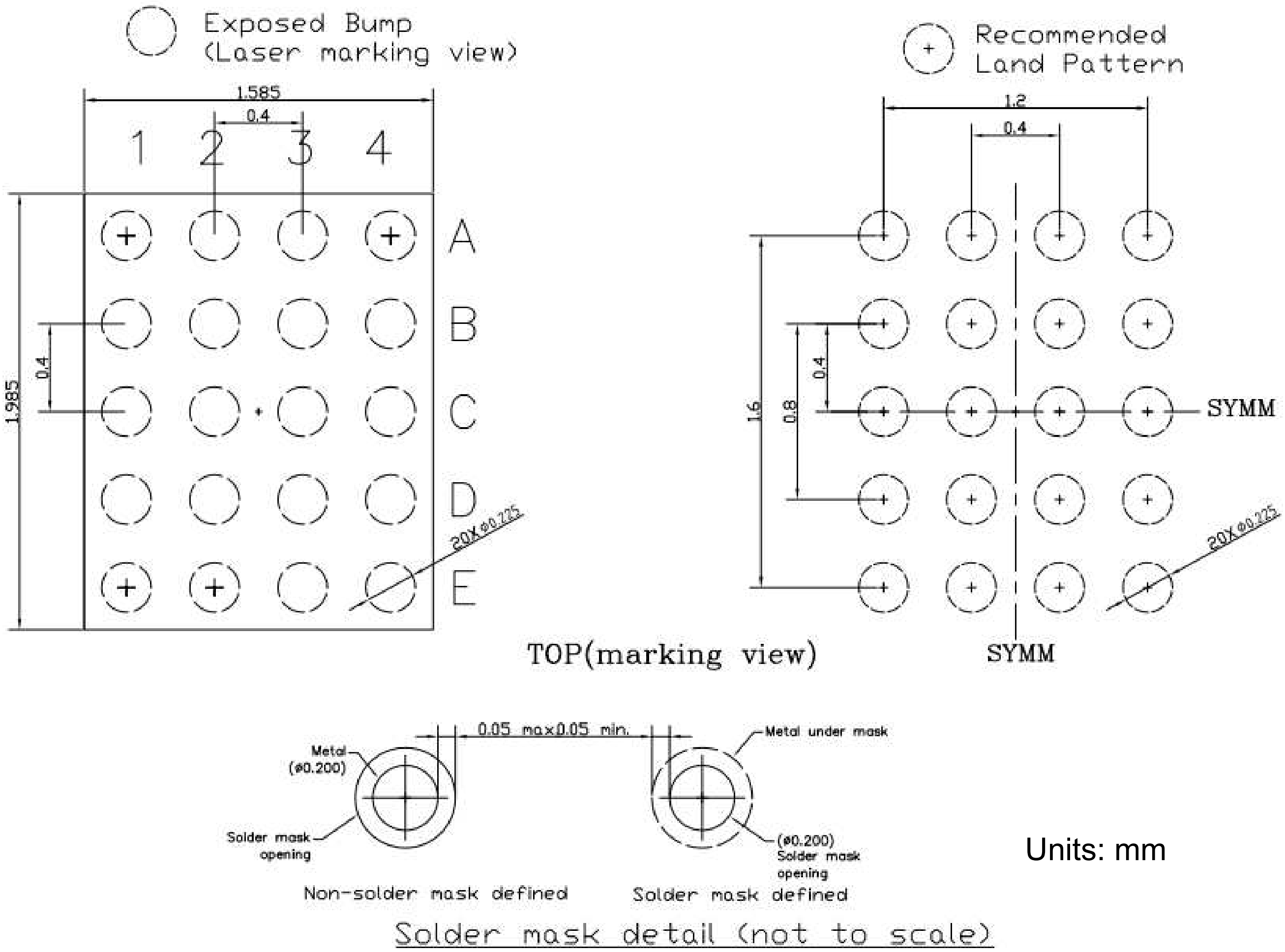
STATUS:
RELEASED

TERMINAL FINISH:
SAC405

TITLE:
CABOT WLCSP 20L
1.585x1.985x0.47mm 0.4P
PACKAGE OUTLINE

REV:	REVISION NOTE:
A	NEW DRAWING

Recommended Landing Pattern



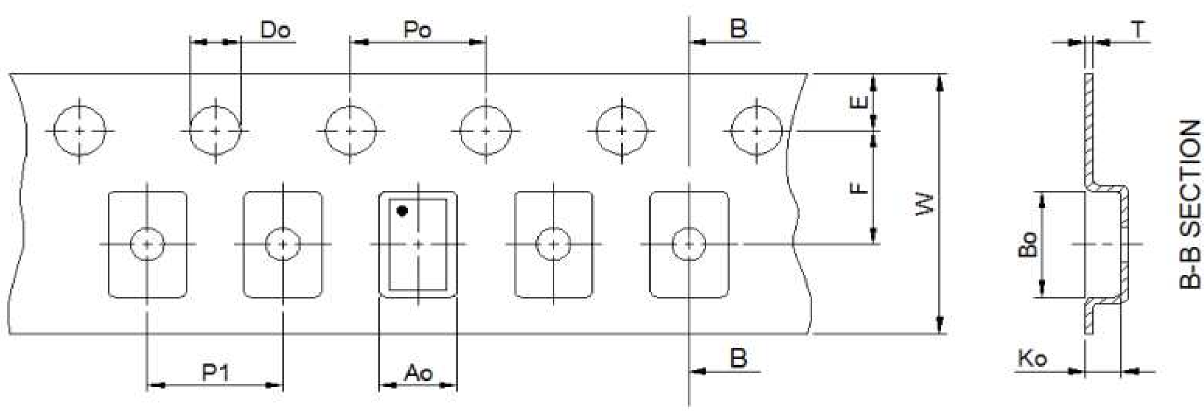
Units: mm

Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size	Units per Reel	Max Units per Box	Reel & Hub Size (mm)	Trailer A		Leader B		Pocket Tape (mm)	
						Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
WLCSP 20L 1.585 x 1.985 mm, 0.4P Green	20	1.585 x 1.985 x 0.47 mm	3,000	3,000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length [mm]	Pocket BTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]	Index Hole to Pocket Center [mm]	Tape Width [mm]	Tape Thickness [mm]
	A0	B0	K0	P0	P1	D0	E	F	W	W
WLCSP 20L 1.585 x 1.985 mm, 0.4P Green	1.77	2.11	0.75	4	4	1.5	1.75	3.5	8	0.25



Note: 1.Orientation in carrier: Pin1 is at upper left corner (Quadrant 1).

Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.9595 mm^3 (nominal). More information can be found at www.jedec.org.

Revision History

Date	Version	Change
25-Aug-2022	1.01	Fixed Pin Description for IN1
15-Jul-2022	1.0	Production Release

Corporate Headquarters

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Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.