SLG59M1600V



7.8 m Ω , 9 A Load Switch with Discharge and Reverse Current Blocking

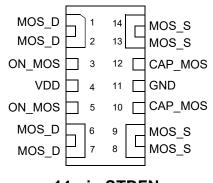
General Description

Pin Configuration

The SLG59M1600V is designed for load switching application. The part comes with one 9 A rated MOSFET switched on by an ON control pin. MOSFET turn on time is independently adjusted by an external capacitor.

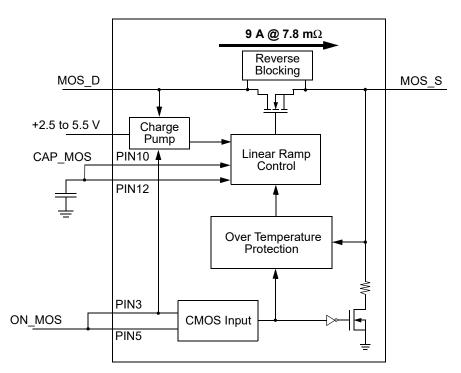
Features

- One 9 A independent MOSFET with reverse current blocking
- Integrated VGS Charge Pump
- Internal discharge for gate and source
- Ramp Control
- Protected by thermal shutdown
- Pb-Free / RoHS Compliant
- Halogen-Free
- STDFN 14L, 1 x 3 x 0.55 mm



14-pin STDFN (Top View)

Block Diagram





Pin Description

Pin #	Pin Name	Туре	Pin Description
1	MOS_D	MOSFET	Drain of MOSFET
2	MOS_D	MOSFET	Drain of MOSFET
3	ON_MOS	Input	Turns on MOS (4 M Ω pull down resistor). Tied to Pin 5 on PCB.
4	VDD	VDD	+5VDD Power
5	ON_MOS	Input	Turns on MOS (4 M Ω pull down resistor). Tied to Pin 3 on PCB.
6	MOS_D	MOSFET	Drain of MOSFET
7	MOS_D	MOSFET	Drain of MOSFET
8	MOS_S	MOSFET	Source of MOSFET
9	MOS_S	MOSFET	Source of MOSFET
10	CAP_MOS	Input	Sets ramp and turn on time for MOSFET. Tied to Pin 12 on PCB.
11	GND	GND	Ground
12	CAP_MOS	Input	Sets ramp and turn on time for MOSFET. Tied to Pin 10 on PCB.
13	MOS_S	MOSFET	Source of MOSFET
14	MOS_S	MOSFET	Source of MOSFET

Ordering Information

Part Number	Туре	Production Flow
SLG59M1600V	STDFN 14L	Industrial, -40 °C to 85 °C
SLG59M1600VTR	STDFN 14L (Tape and Reel)	Industrial, -40 °C to 85 °C



SLG59M1600V

Absolute Maximum Ratings

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
V _D	Power Supply				6	V
Τ _S	Storage Temperature		-65		150	°C
ESD _{HBM}	ESD Protection	Human Body Model	2000			V
ESD _{CDM}	ESD Protection	Charged Device Model	1000			V
MSL	Moisture Sensitivity Level				1	
θ_{JA}	Package Thermal Resistance, Junction-to-Ambient	1mm x 3mm 14L STDFN; Determined us- ing 1 in ² , 1.2 oz. copper pads under VIN and VOUT on FR4 pcb material		71		°C/W
W _{DIS}	Package Power Dissipation				1.2	W
IDS _{MAX}	Max Operating Current				9	А
MOSFET IDS _P	CPeak Current from Drain to Source	For no more than 10 continuous seconds out of every 100 seconds			12	А
•		Aaximum Ratings" may cause permanent damages or any other conditions above those indicate	•			

specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

 T_A = -40 °C to 85 °C (unless otherwise stated)

Parameter	Description	Conditions	Min.	Тур.	Max.	Unit
V _{DD}	Power Supply Voltage		2.5		5.5	V
	Power Supply Current when OFF			0.1	1	μΑ
I _{DD}	Power Supply Current, ON_MOS_1 & ON_MOS_2 (Steady State)			40	70	μA
		T _A 25°C MOSFET @100 mA		7.8	10.5	mΩ
RDS _{ON}	ON Resistance	T _A 70°C MOSFET @100 mA		8.4	12.1	mΩ
		T _A 85°C MOSFET @100 mA		9.0	12.7	mΩ
MOSFET IDS	Current from Drain to Source for each MOSFET	Continuous			9	А
IDS _{LKG}	IDS Leakage (Reverse Blocking enabled)	V_{S} = 1.0 V to 5.0 V, V_{DD} = V_{D} = 0 V, ON_MOS = LOW, Full temp range		0.5	5.0	μA
VD	Drain Voltage		0.85	5.0	V _{DD}	V
T _{ON_Delay}	ON pin Delay Time	50% ON to Ramp Begin, R _L = 20 Ω, no C _L	0	270	500	μs
		50% ON to 90% V _S	Configurable ¹			ms
T _{Total_ON}	Total Turn On Time	Example: CAP (Pin 10 & 12) share a single 4nF capacitor, $V_{DD} = V_D = 5 V$, Source_Cap = 10 μ F, $R_L = 20 \Omega$		1.1		ms
		10% $V_{\rm S}$ to 90% $V_{\rm S}$	C	onfigurable ¹		V/ms
T _{SLEWRATE}	Slew Rate	Example: CAP (Pin 10 & 12) share a single 4nF capacitor, V_{DD} = V_D = 5 V, Source_Cap = 10 μ F, R _L = 20 Ω		6.0		V/ms
CAP _{SOURCE}	Source Cap	Source to GND			1000	μF
R _{DIS}	Discharge Resistance		50	113	150	Ω
ON_V_{IH}	High Input Voltage on ON pin		0.85		V _{DD}	V
ON_V_{IL}	Low Input Voltage on ON pin		-0.3	0	0.3	V
THERMON	Thermal shutoff turn-on temperature			125		°C
THERMOFF	Thermal shutoff turn-off temperature			100		°C



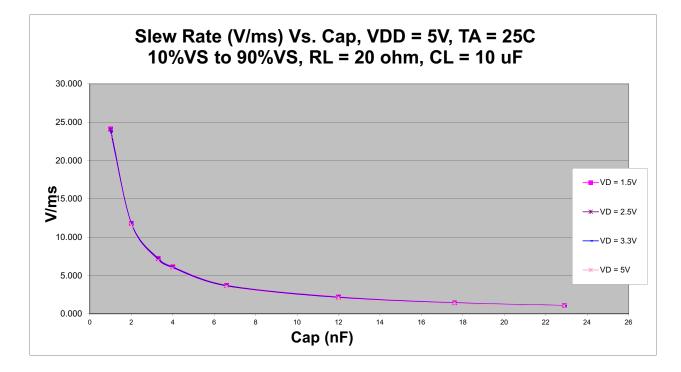
Electrical Characteristics (continued)

 $T_A = -40$ °C to 85 °C (unless otherwise stated)

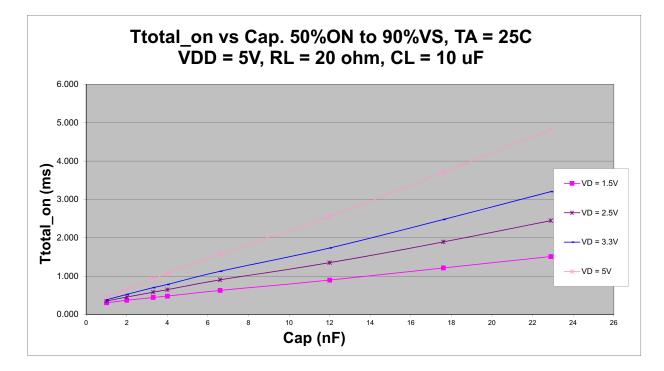
Parameter	Description	Conditions	Min.	Тур.	Max.	Unit	
THERM _{TIME}	Thermal shutoff time				1	ms	
T _{OFF_Delay}	OFF Delay Time	50% ON to V _S Fall, V _{DD} = V _D = 5 V, R _L = 20 Ω , no C _L		1.7	3	μs	
Notes: 1. Refer to table for configuration details.							



T_{SLEW} vs. CAP

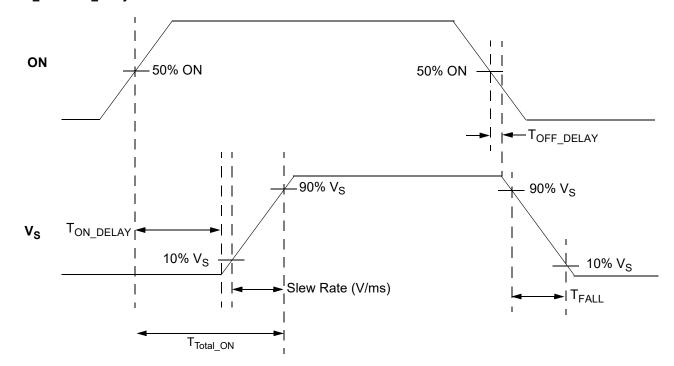


T_{TOTAL_ON} vs. CAP



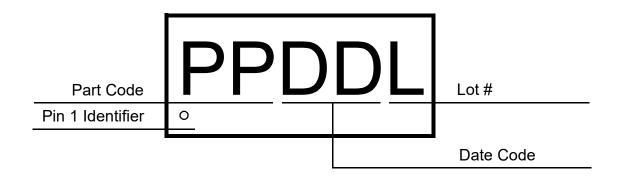


 $T_{Total_ON},\,T_{ON_Delay}$ and Slew Rate Measurement





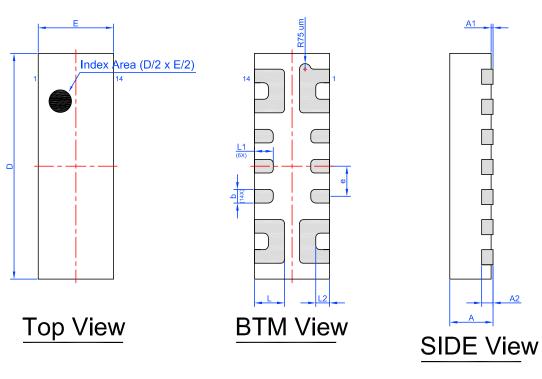
Package Top Marking System Definition





Package Drawing and Dimensions

14 Lead STDFN Package 1 mm x 3 mm (Fused Lead)



Ur	hit:	n	n	า

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
Α	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	0.95	1.00	1.05
A2	0.10	0.15	0.20	L	0.35	0.40	0.45
b	0.13	0.18	0.23	L1	0.20	0.25	0.30
е	().40 BSC	;	L2	0.06	0.11	0.16

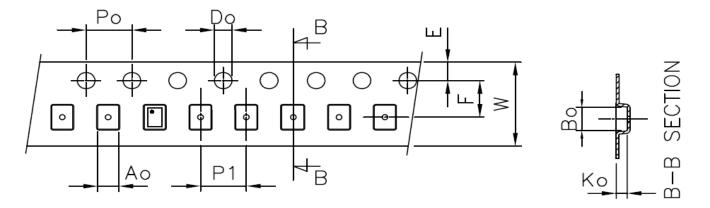


Tape and Reel Specifications

Package	# of	Nominal	Unite nor	Unitenor	Unite por	Unite nor	Unitsper	Max	Reel &	Trail	er A	Lead	ler B	Pocket Ta	ape (mm)
Туре	Pins	Package Size	Reel	Units per Box	Hub Size (mm)	Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch				
STDFN 14L 1x3mm 0.4P FC	14	1x3x0.55mm	3000	3000	178/60	100	400	100	400	8	4				

Carrier Tape Drawing and Dimensions

Package Type	PocketBTM Length [mm]	PocketBTM Width [mm]	Pocket Depth [mm]	Index Hole Pitch [mm]	Pocket Pitch [mm]	Index Hole Diameter [mm]	Index Hole to Tape Edge [mm]		Tape Width [mm]
	A0	В0	K0	P0	P1	D0	Е	F	w
STDFN 14L 1x3mm 0.4P FC		3.15	0.7	4	4	1.5	1.75	3.5	8



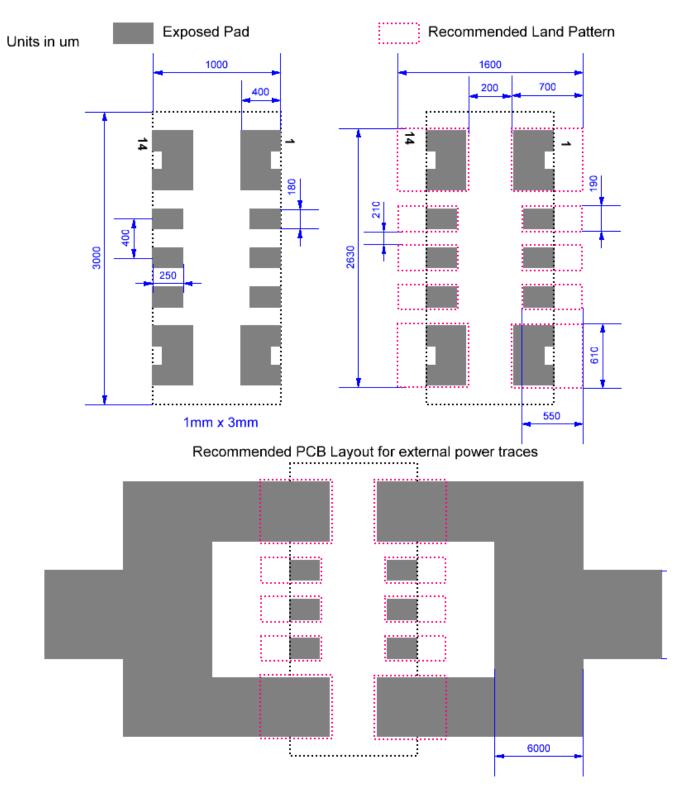
Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 1.65 mm³ (nominal). More information can be found at www.jedec.org.



SLG59M1600V

Recommended Land Pattern and PCB Layout





Revision History

Date	Version	Change
2/10/2022	1.04	Renesas rebranding Fixed typos
3/15/2016	1.03	Fixed RDSon values
11/30/2015	1.02	Updated Abs. Max and Electrical Characteristics Tables
9/29/2015	1.01 Updated Block Diagram	

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu, Koto-ku, Tokyo 135-0061, Japan www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit <u>www.renesas.com/contact-us/</u>.