SLG7RN45291

GreenPAK ™

RZ/G2L SMARC Boot Logic Control

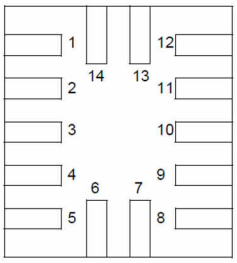
General Description

Renesas SLG7RN45291 is a low power and small form device. The SoC is housed in a 2mm x 2.2mm STQFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Pin Configuration



14-pin STQFN
(Top View)

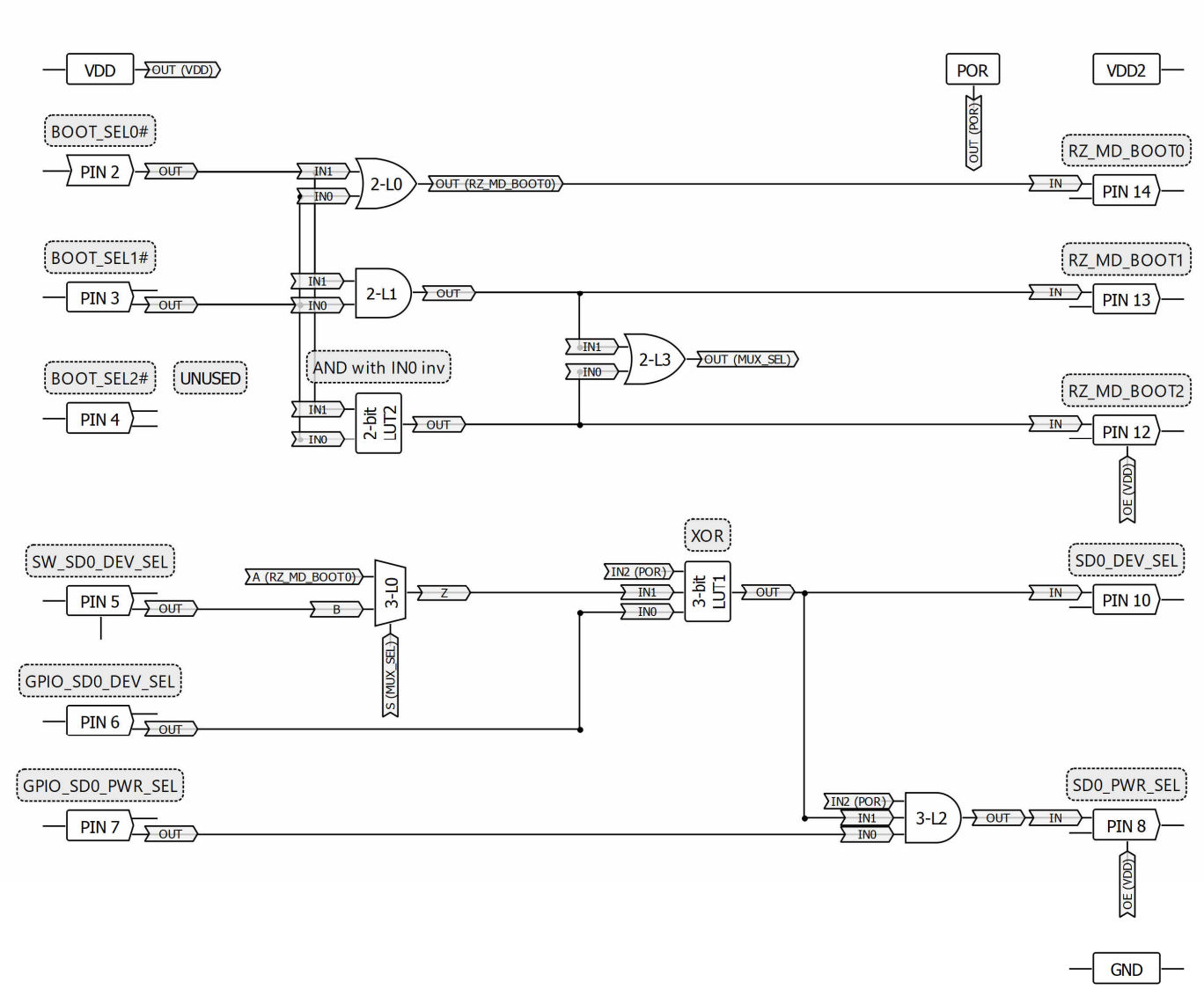
Output Summary

1 Output - Open Drain NMOS 1X
4 Outputs - Push Pull 1X

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	SD0_PWR_SEL
2	BOOT_SEL0#	9	GND
3	BOOT_SEL1#	10	SD0_DEV_SEL
4	BOOT_SEL2#	11	VDD2
5	SW_SD0_DEV_SEL	12	RZ_MD_BOOT2
6	GPIO_SD0_DEV_SEL	13	RZ_MD_BOOT1
7	GPIO_SD0_PWR_SEL	14	RZ_MD_BOOT0

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	BOOT_SEL0#	Digital Input	Low Voltage Digital Input	floating
3	BOOT_SEL1#	Digital Input	Low Voltage Digital Input	floating
4	BOOT_SEL2#	Digital Input	Low Voltage Digital Input	floating
5	SW_SD0_DEV_SEL	Digital Input	Low Voltage Digital Input	floating
6	GPIO_SD0_DEV_SEL	Digital Input	Low Voltage Digital Input	floating
7	GPIO_SD0_PWR_SEL	Digital Input	Low Voltage Digital Input	floating
8	SD0_PWR_SEL	Digital Output	Open Drain NMOS 1X	floating
9	GND	GND	Ground	--
10	SD0_DEV_SEL	Digital Output	Push Pull 1X	floating
11	VDD2	PWR	Supply Voltage	--
12	RZ_MD_BOOT2	Digital Output	Push Pull 1X	floating
13	RZ_MD_BOOT1	Digital Output	Push Pull 1X	floating
14	RZ_MD_BOOT0	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45291V	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	Pins 2, 3, 4, 5, 6, 7, 8	GND - 0.5	VDD + 0.5	V
	Pins 10, 12, 13, 14		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

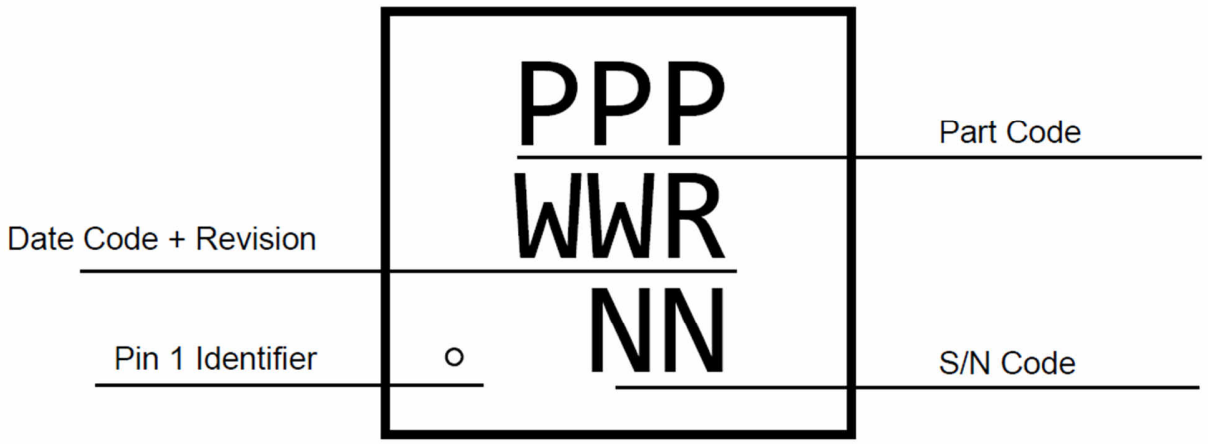
Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	5	5.5	V
V_{DD2}	Supply Voltage		1.71	3.3	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. All inputs are Low	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_{IH}	HIGH-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Low-Level Logic Input at VDD=1.8V	0.94	--	VDD	V
		Low-Level Logic Input at VDD=3.3V	1.06	--	VDD	V
		Low-Level Logic Input at VDD=5.0V	1.15	--	VDD	V
V_{IL}	LOW-Level Input Voltage PIN 2, 3, 4, 5, 6, 7, 8	Low-Level Logic Input at VDD=1.8V	0	--	0.52	V
		Low-Level Logic Input at VDD=3.3V	0	--	0.67	V
		Low-Level Logic Input at VDD=5.0V	0	--	0.77	V
V_{OH2}	HIGH-Level Output Voltage PIN 10, 12, 13, 14	Push-Pull 1X, I_{OH}=100µA at VDD2=1.8V	1.69	1.79	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD2=3.3V	2.74	3.12	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD2=5.0V	4.15	4.76	--	V
V_{OL}	LOW-Level Output Voltage PIN 2, 3, 4, 5, 6, 7, 8	Open Drain NMOS 1X, I_{OL}=100µA at VDD=1.8V	--	0.01	0.02	V
		Open Drain NMOS 1X, I_{OL}=3mA at VDD=3.3V	--	0.08	0.15	V
		Open Drain NMOS 1X, I_{OL}=5mA at VDD=5.0V	--	0.12	0.16	V
V_{OL2}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=100µA at VDD2=1.8V	--	0.01	0.03	V

	PIN 10, 12, 13, 14	Push-Pull 1X, I_{OL}=3mA at VDD2=3.3V	--	0.13	0.23	V
		Push-Pull 1X, I_{OL}=5mA at VDD2=5.0V	--	0.19	0.24	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull 1X, V_{OH}=VDD-0.2V at VDD2=1.8V	1.07	1.70	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD2=3.3V	6.05	12.08	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD2=5.0V	22.08	34.04	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PIN 2, 3, 4, 5, 6, 7, 8	Open Drain NMOS 1X, V_{OL}=0.15V at VDD=1.8V	1.38	2.53	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V at VDD=3.3V	7.31	12.37	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V at VDD=5.0V	10.82	17.38	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PIN 10, 12, 13, 14	Push-Pull 1X, V_{OL}=0.15V at VDD2=1.8V	0.92	1.69	--	mA
		Push-Pull 1X, V_{OL}=0.4V at VDD2=3.3V	4.88	8.24	--	mA
		Push-Pull 1X, V_{OL}=0.4V at VDD2=5.0V	7.22	11.58	--	mA
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 12, 13 and 14 to another.
3. Guaranteed by Design.

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0x4A1A2238			07/11/2023

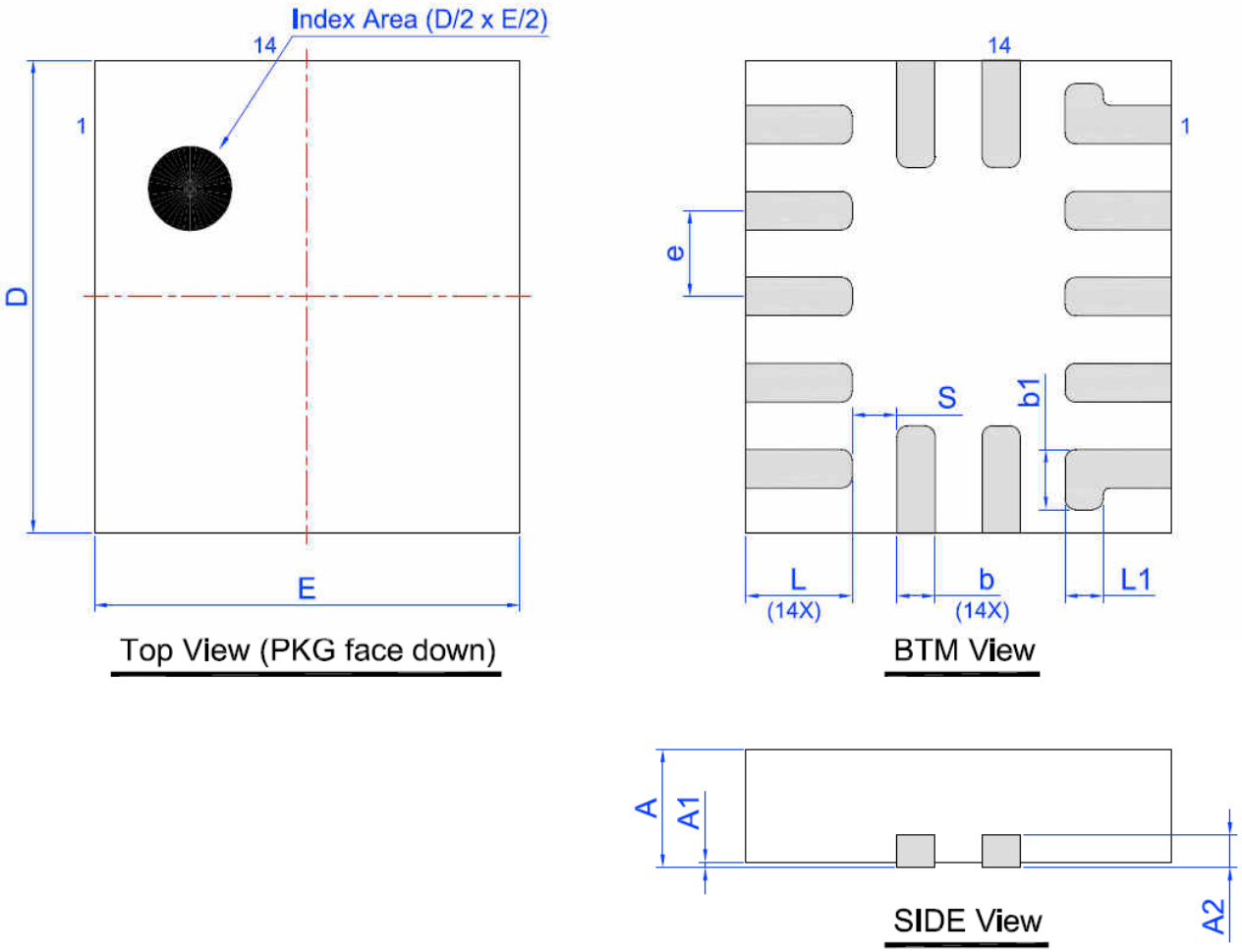
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 14L 2 x 2.2mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

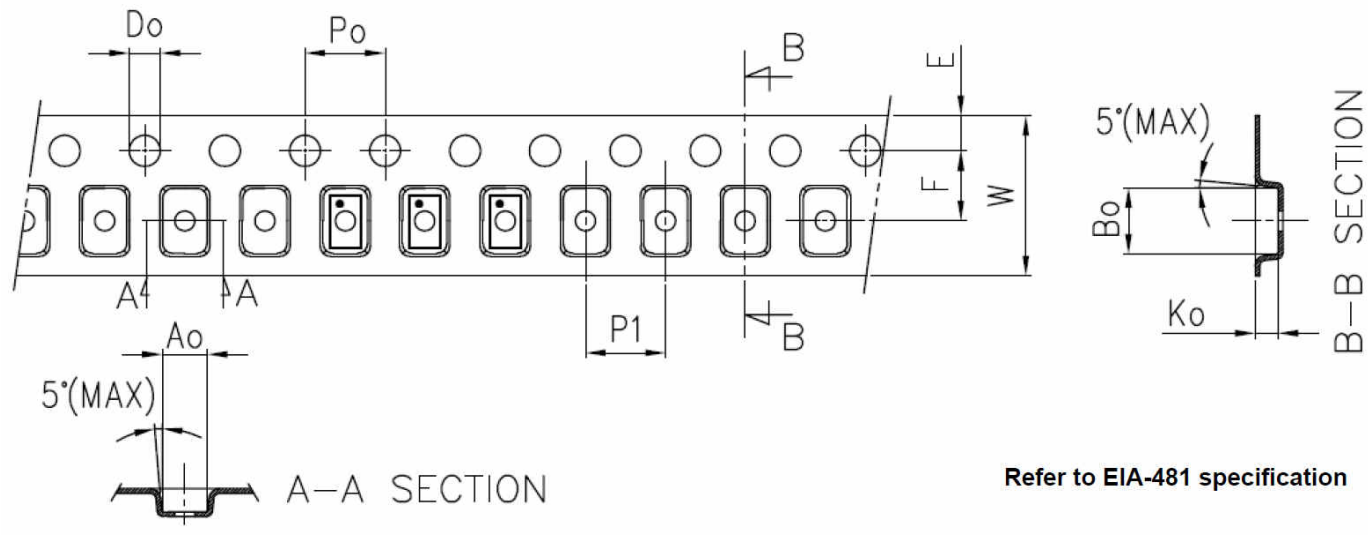
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S		0.21 TYP	
e		0.40 BSC		b1		0.28 TYP	
				L1		0.18 TYP	

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 2x2.2mm 0.4P COL	14	2 x 2.2x 0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2x2.2 mm 0.4P COL	2.2	2.35	0.8	4	4	1.5	1.75	3.5	8

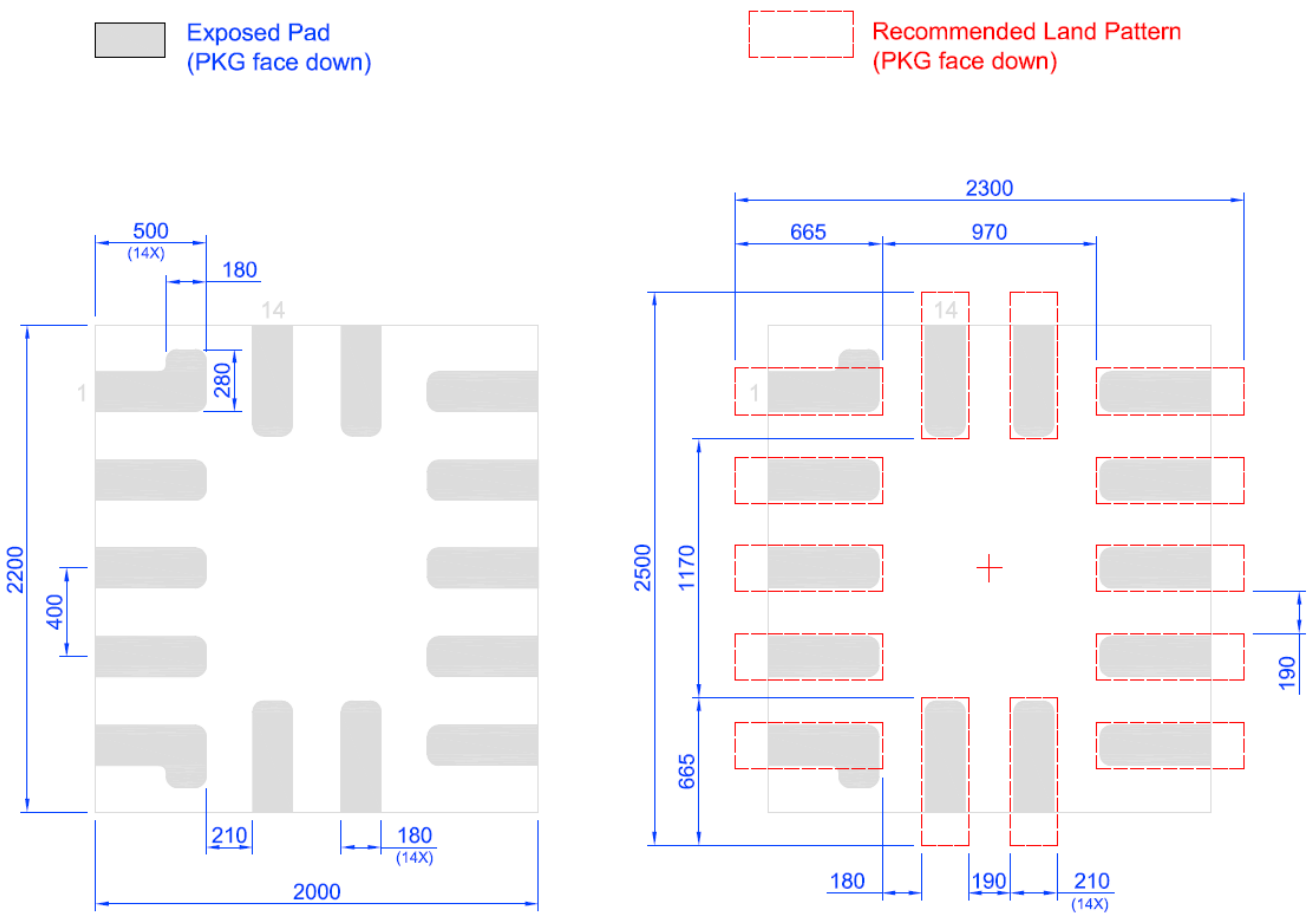


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Unit:um

Datasheet Revision History

Date	Version	Change
10/06/2021	0.10	New design
07/11/2023	0.11	Moved to Renesas template

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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