SLG7RN45294

GreenPAK ™

RZ/G2L SMARC SPI/CAN Level Shifter

General Description

Renesas SLG7RN45294 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

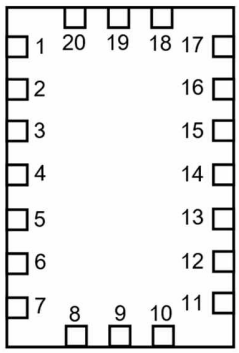
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

Output Summary

3 Outputs - Open Drain NMOS 1X
5 Outputs - Push Pull 1X

Pin Configuration

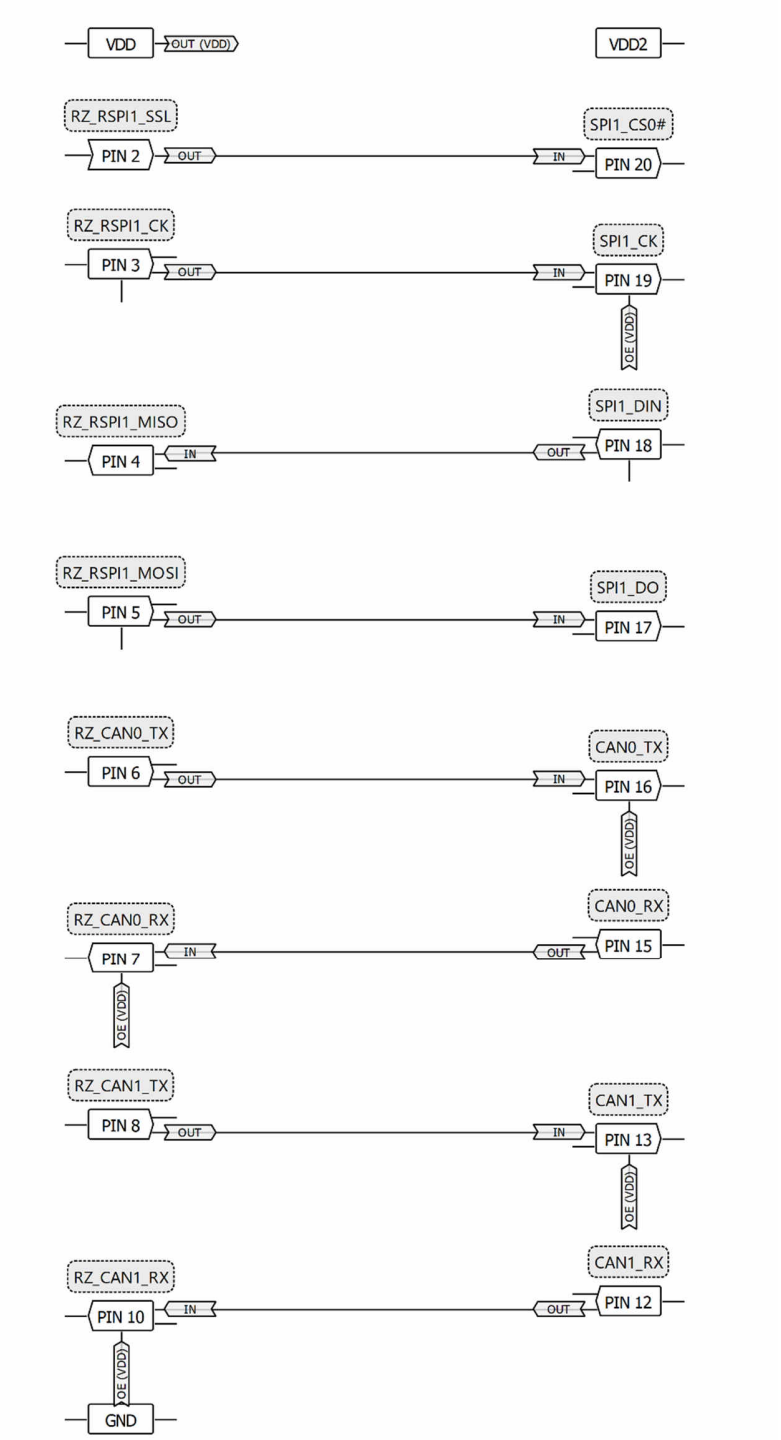


STQFN-20
(Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	GND
2	RZ_RSPI1_SSL	12	CAN1_RX
3	RZ_RSPI1_CK	13	CAN1_TX
4	RZ_RSPI1_MISO	14	VDD2
5	RZ_RSPI1_MOSI	15	CAN0_RX
6	RZ_CAN0_TX	16	CAN0_TX
7	RZ_CAN0_RX	17	SPI1_DO
8	RZ_CAN1_TX	18	SPI1_DIN
9	NC	19	SPI1_CK
10	RZ_CAN1_RX	20	SPI1_CS0#

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	RZ_RSPI1_SSL	Digital Input	Digital Input with Schmitt trigger	floating
3	RZ_RSPI1_CK	Digital Input	Digital Input with Schmitt trigger	floating
4	RZ_RSPI1_MISO	Digital Output	Open Drain NMOS 1X	floating
5	RZ_RSPI1_MOSI	Digital Input	Digital Input with Schmitt trigger	floating
6	RZ_CAN0_TX	Digital Input	Digital Input with Schmitt trigger	floating
7	RZ_CAN0_RX	Digital Output	Open Drain NMOS 1X	floating
8	RZ_CAN1_TX	Digital Input	Digital Input with Schmitt trigger	floating
9	NC	--	Keep Floating or Connect to GND	--
10	RZ_CAN1_RX	Digital Output	Open Drain NMOS 1X	floating
11	GND	GND	Ground	--
12	CAN1_RX	Digital Input	Digital Input with Schmitt trigger	floating
13	CAN1_TX	Digital Output	Push Pull 1X	floating
14	VDD2	PWR	Supply Voltage	--
15	CAN0_RX	Digital Input	Digital Input with Schmitt trigger	floating
16	CAN0_TX	Digital Output	Push Pull 1X	floating
17	SPI1_DO	Digital Output	Push Pull 1X	floating
18	SPI1_DIN	Digital Input	Digital Input with Schmitt trigger	floating
19	SPI1_CK	Digital Output	Push Pull 1X	floating
20	SPI1_CS0#	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN45294V	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on VDD relative to GND		-0.5	7	V
Supply voltage on VDD2 relative to GND		-0.5	VDD + 0.5	V
DC Input voltage	PINs 2, 3, 4, 5, 6, 7, 8, 9, 10	GND - 0.5	VDD + 0.5	V
	PINs 12, 13, 15, 16, 17, 18, 19, 20		VDD2 + 0.5	
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		500	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.7	5	5.5	V
V_{DD2}	Supply Voltage		1.71	1.8	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{VDD}	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	45	mA
		T_J = 110°C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85°C	--	--	86	mA
		T_J = 110°C	--	--	41	mA
V_{IH}	HIGH-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Logic Input with Schmitt Trigger at VDD=5.0V	3.34	--	VDD	V
V_{IH2}	HIGH-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Logic Input with Schmitt Trigger at VDD2=1.8V	1.28	--	VDD	V
		Logic Input with Schmitt Trigger at VDD2=3.3V	2.14	--	VDD	V
		Logic Input with Schmitt Trigger at VDD2=5.0V	3.34	--	VDD	V
V_{IL}	LOW-Level Input Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Logic Input with Schmitt Trigger at VDD=5.0V	0	--	1.41	V
V_{IL2}	LOW-Level Input Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Logic Input with Schmitt Trigger at VDD2=1.8V	0	--	0.49	V
		Logic Input with Schmitt Trigger at VDD2=3.3V	0	--	0.97	V

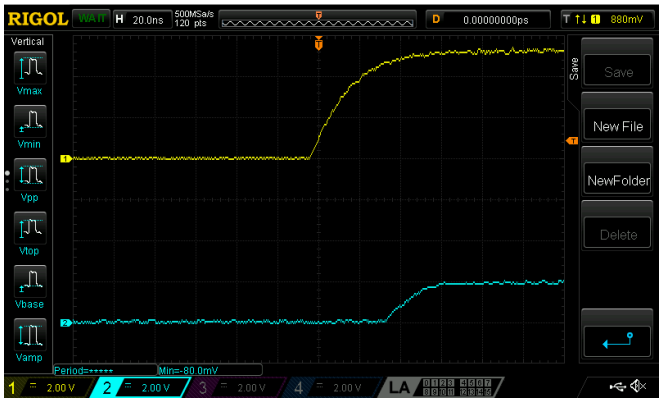
		Logic Input with Schmitt Trigger at VDD2=5.0V	0	--	1.41	V
V_{OH2}	HIGH-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OH}=100µA at VDD2=1.8V	1.69	1.79	--	V
		Push-Pull 1X, I_{OH}=3mA at VDD2=3.3V	2.74	3.12	--	V
		Push-Pull 1X, I_{OH}=5mA at VDD2=5.0V	4.15	4.76	--	V
V_{OL}	LOW-Level Output Voltage PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Open Drain NMOS 1X, I_{OL}=5mA at VDD=5.0V	--	0.12	0.16	V
V_{OL2}	LOW-Level Output Voltage PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, I_{OL}=100µA at VDD2=1.8V	--	0.01	0.03	V
		Push-Pull 1X, I_{OL}=3mA at VDD2=3.3V	--	0.13	0.23	V
		Push-Pull 1X, I_{OL}=5mA at VDD2=5.0V	--	0.19	0.24	V
I_{OH2}	HIGH-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OH}=VDD-0.2V at VDD2=1.8V	1.07	1.70	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD2=3.3V	6.05	12.08	--	mA
		Push-Pull 1X, V_{OH}=2.4V at VDD2=5.0V	22.08	34.04	--	mA
I_{OL}	LOW-Level Output Current (see Note 1) PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10	Open Drain NMOS 1X, V_{OL}=0.4V at VDD=5.0V	10.82	17.38	--	mA
I_{OL2}	LOW-Level Output Current (see Note 1) PINs 12, 13, 15, 16, 17, 18, 19, 20	Push-Pull 1X, V_{OL}=0.15V at VDD2=1.8V	0.92	1.69	--	mA
		Push-Pull 1X, V_{OL}=0.4V at VDD2=3.3V	4.88	8.24	--	mA
		Push-Pull 1X, V_{OL}=0.4V at VDD2=5.0V	7.22	11.58	--	mA
T_{SU}	Startup Time	From VDD rising past PON_{THR}	0.61	1.24	1.65	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.41	1.54	1.66	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.00	1.15	1.31	V

Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, PINs 12, 13, 15, 16, 17, 18, 19, and 20 to another.
3. Guaranteed by Design.

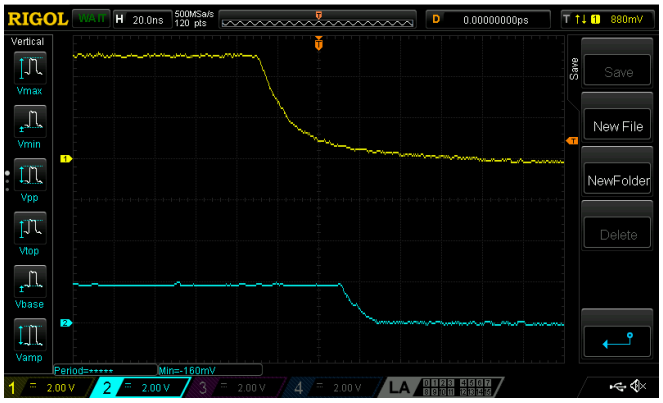
Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 2 (RZ_RSPI1_SSL)
Channel 2 (light blue/2nd line) – PIN# 20 (SPI1_CS0#)

1. Transient from Low to High
(PIN# 2 (RZ_RSPI1_SSL) => PIN# 20 (SPI1_CS0#))

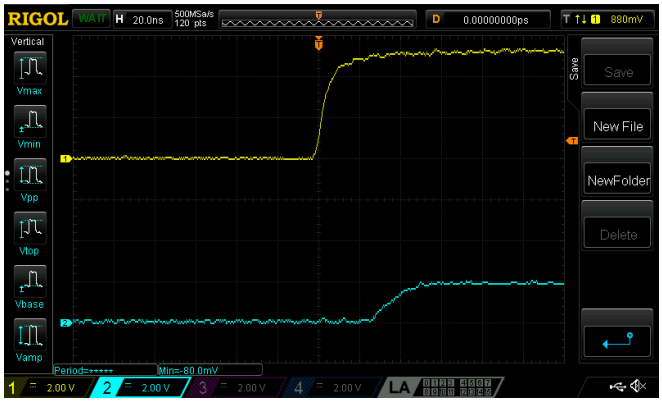


2. Transient from High to Low
(PIN# 2 (RZ_RSPI1_SSL) => PIN# 20 (SPI1_CS0#))

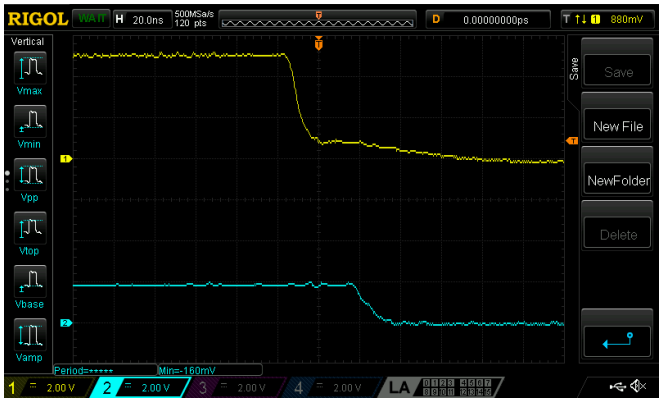


Channel 1 (yellow/top line) – PIN# 3 (RZ_RSPI1_CK)
Channel 2 (light blue/2nd line) – PIN# 19 (SPI1_CK)

3. Transient from Low to High
(PIN# 3 (RZ_RSPI1_CK) => PIN# 19 (SPI1_CK))



4. Transient from High to Low
(PIN# 3 (RZ_RSPI1_CK) => PIN# 19 (SPI1_CK))



Channel 1 (yellow/top line) – PIN# 4 (RZ_RSPI1_MISO) with external 5kΩ pull up resistor
Channel 2 (light blue/2nd line) – PIN# 18 (SPI1_DIN)

5. Transient from Low to High
(PIN# 18 (SPI1_DIN) => PIN# 4 (RZ_RSPI1_MISO))

6. Transient from High to Low
(PIN# 18 (SPI1_DIN) => PIN# 4 (RZ_RSPI1_MISO))

Channel 1 (yellow/top line) – PIN# 5 (RZ_RSPI1_MOSI)
Channel 2 (light blue/2nd line) – PIN# 17 (SPI1_DO)

7. Transient from Low to High
(PIN# 5 (RZ_RSPI1_MOSI) => PIN# 17 (SPI1_DO))

8. Transient from High to Low
(PIN# 5 (RZ_RSPI1_MOSI) => PIN# 17 (SPI1_DO))

Channel 1 (yellow/top line) – PIN# 6 (RZ_CAN0_TX)
Channel 2 (light blue/2nd line) – PIN# 16 (CAN0_TX)

9. Transient from Low to High
(PIN# 6 (RZ_CAN0_TX) => PIN# 16 (CAN0_TX))

10. Transient from High to Low
(PIN# 6 (RZ_CAN0_TX) => PIN# 16 (CAN0_TX))

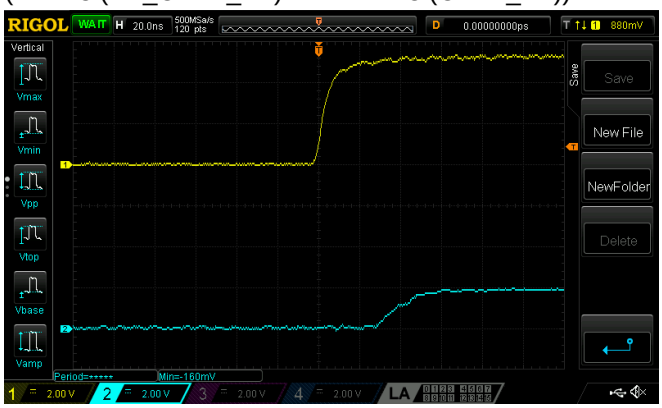
Channel 1 (yellow/top line) – PIN# 7 (RZ_CAN0_RX) with external 5kΩ pull up resistor
Channel 2 (light blue/2nd line) – PIN# 15 (CAN0_RX)

11. Transient from Low to High
(PIN# 15 (CAN0_RX) => PIN# 7 (RZ_CAN0_RX))

12. Transient from High to Low
(PIN# 15 (CAN0_RX) => PIN# 7 (RZ_CAN0_RX))

Channel 1 (yellow/top line) – PIN# 8 (RZ_CAN1_TX)
Channel 2 (light blue/2nd line) – PIN# 13 (CAN1_TX)

13. Transient from Low to High
(PIN# 8 (RZ_CAN1_TX) => PIN# 13 (CAN1_TX))



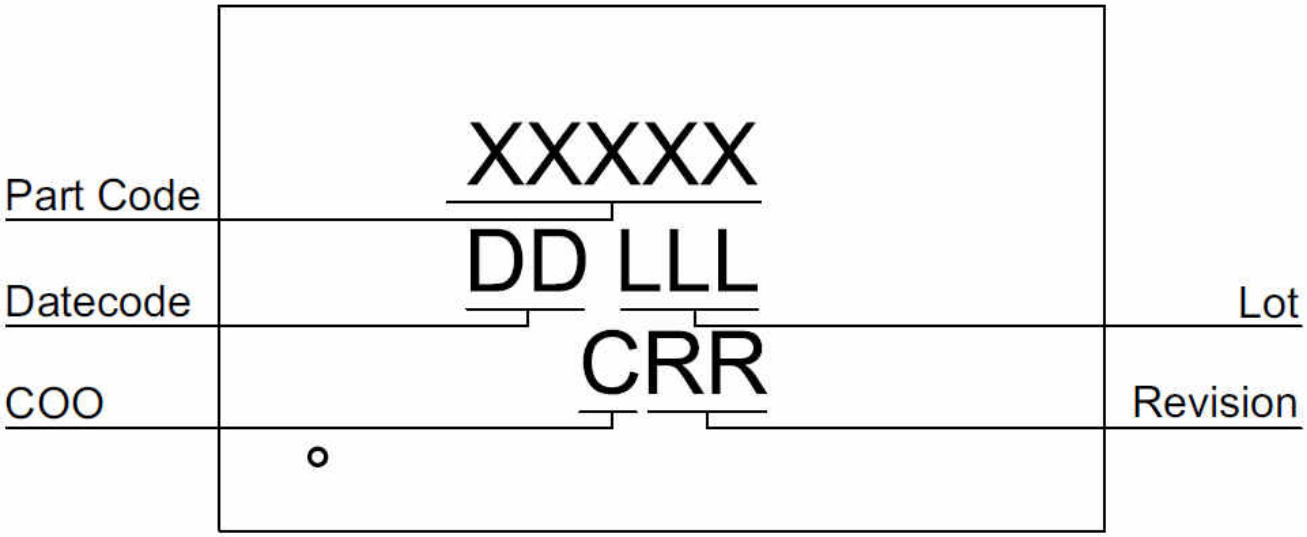
14. Transient from High to Low
(PIN# 8 (RZ_CAN1_TX) => PIN# 13 (CAN1_TX))

Channel 1 (yellow/top line) – PIN# 10 (RZ_CAN1_RX) with external 5kΩ pull up resistor
Channel 2 (light blue/2nd line) – PIN# 12 (CAN1_RX)

15. Transient from Low to High
(PIN# 12 (CAN1_RX) => PIN# 10 (RZ_CAN1_RX))

16. Transient from High to Low
(PIN# 12 (CAN1_RX) => PIN# 10 (RZ_CAN1_RX))

Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0xA06DDF4E			07/11/2023

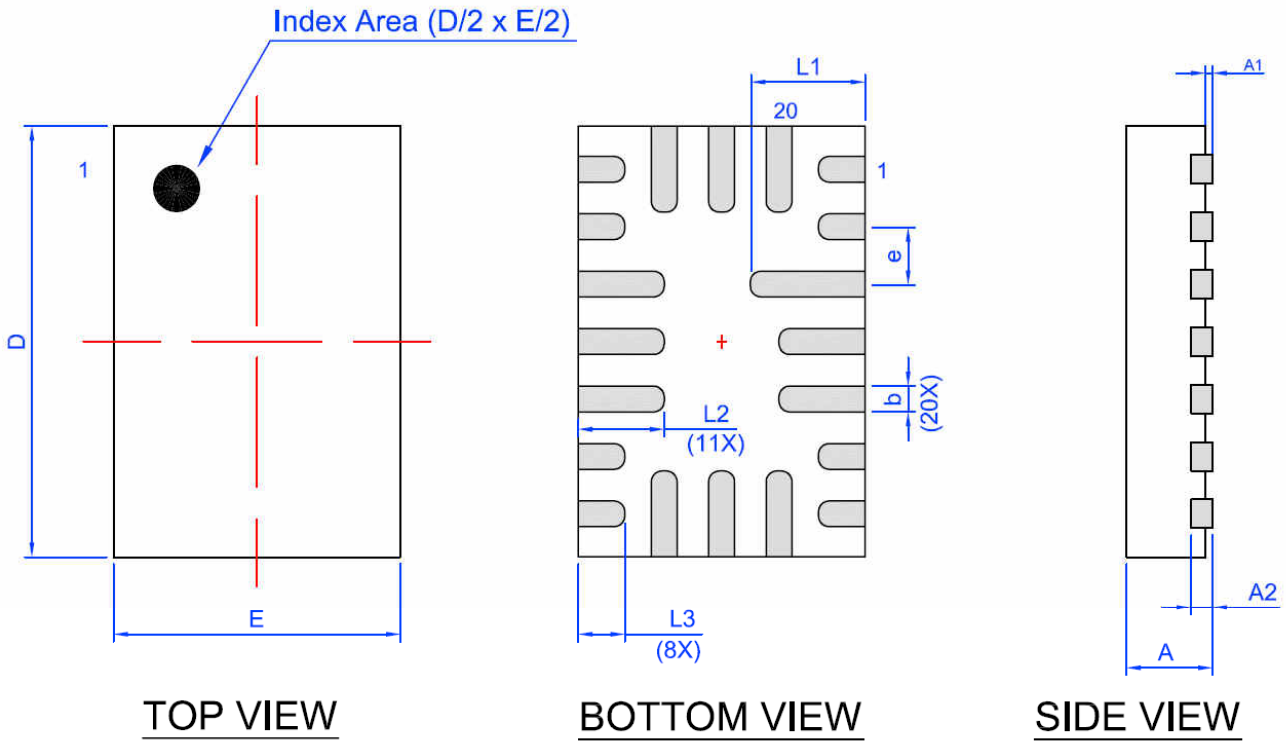
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package
JEDEC MO-220



Unit: mm

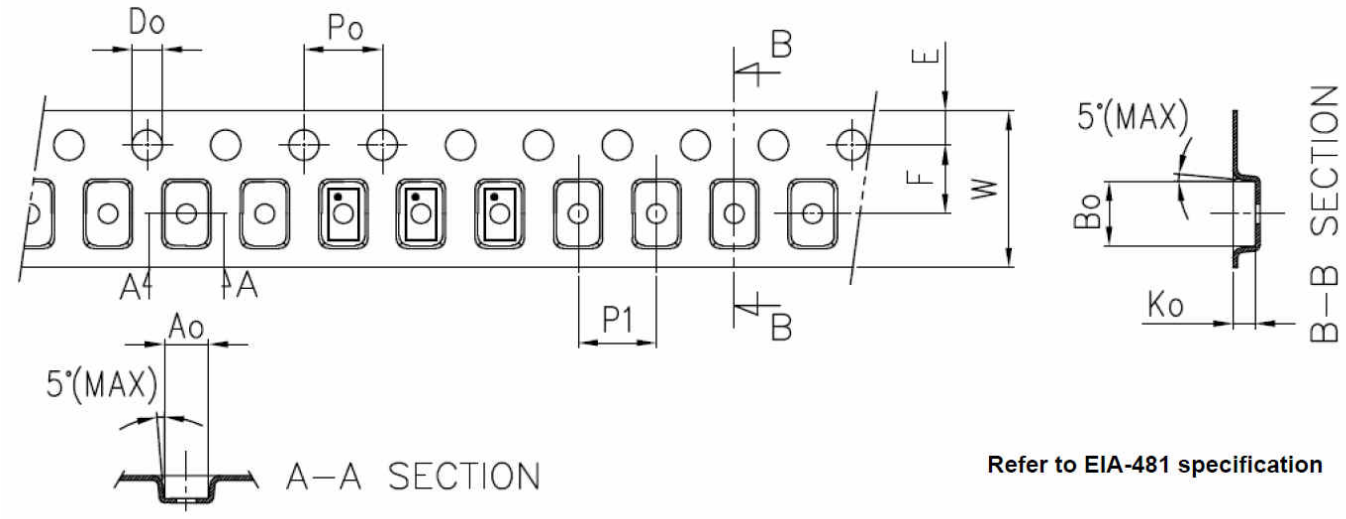
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P COL	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3 mm 0.4P COL	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

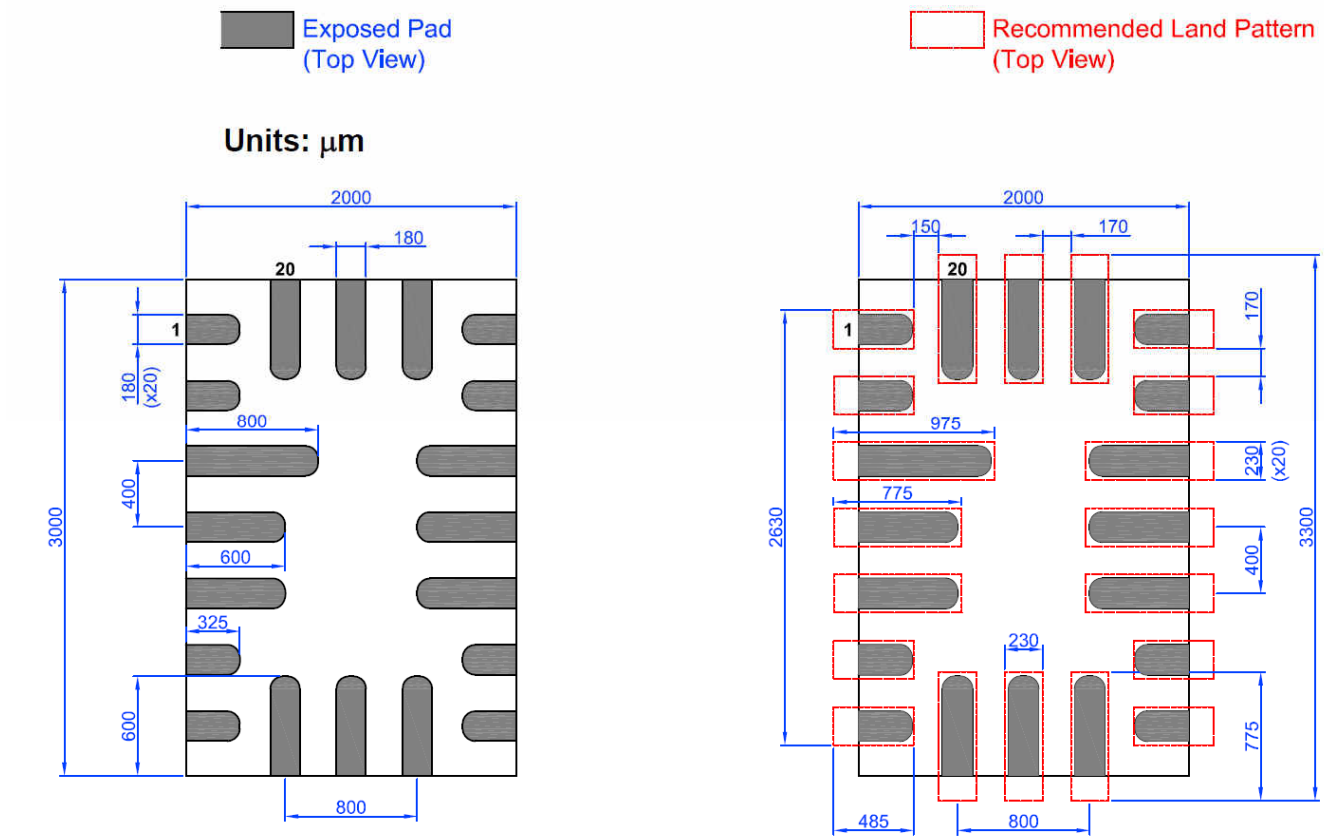


Refer to EIA-481 specification

Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm^3 (nominal). More information can be found at www.jedec.org.

Recommended Land Pattern



Datasheet Revision History

Date	Version	Change
10/07/2021	0.10	New design
07/11/2023	0.11	Moved to Renesas template

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

© 2024 Renesas Electronics Corporation. All rights reserved.