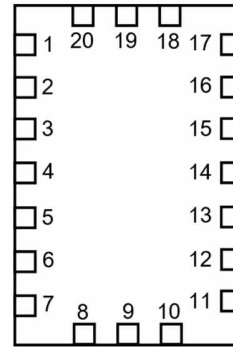


**RZ/G2L SMARC SPI/CAN Level Shifter**
**General Description**

Renesas SLG7RN45294 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

**Features**

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

**Pin Configuration**

**STQFN-20  
(Top View)**
**Output Summary**

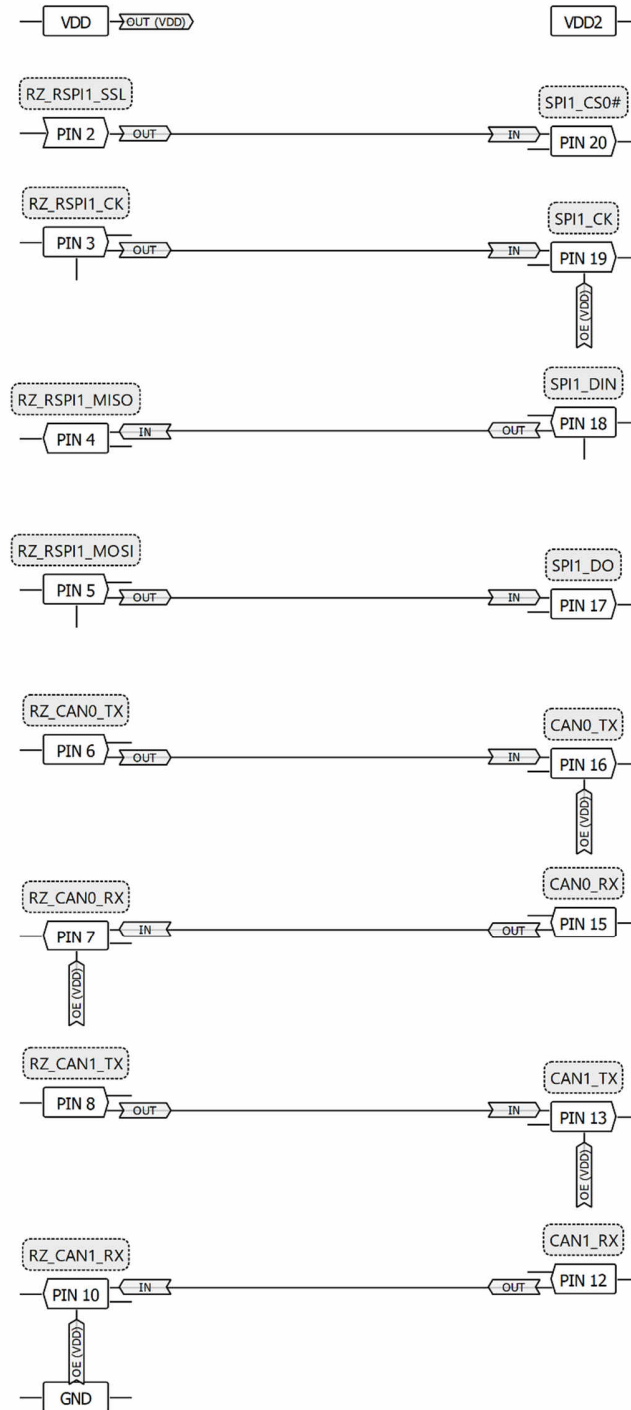
3 Outputs - Open Drain NMOS 1X  
5 Outputs - Push Pull 1X

**Pin name**

| Pin # | Pin name      | Pin # | Pin name  |
|-------|---------------|-------|-----------|
| 1     | VDD           | 11    | GND       |
| 2     | RZ_RSPI1_SSL  | 12    | CAN1_RX   |
| 3     | RZ_RSPI1_CK   | 13    | CAN1_TX   |
| 4     | RZ_RSPI1_MISO | 14    | VDD2      |
| 5     | RZ_RSPI1_MOSI | 15    | CAN0_RX   |
| 6     | RZ_CAN0_TX    | 16    | CAN0_TX   |
| 7     | RZ_CAN0_RX    | 17    | SPI1_DO   |
| 8     | RZ_CAN1_TX    | 18    | SPI1_DIN  |
| 9     | NC            | 19    | SPI1_CK   |
| 10    | RZ_CAN1_RX    | 20    | SPI1_CS0# |

RZ/G2L SMARC SPI/CAN Level Shifter

Block Diagram



**RZ/G2L SMARC SPI/CAN Level Shifter**
**Pin Configuration**

| Pin # | Pin Name      | Type           | Pin Description                    | Internal Resistor |
|-------|---------------|----------------|------------------------------------|-------------------|
| 1     | VDD           | PWR            | Supply Voltage                     | --                |
| 2     | RZ_RSPI1_SSL  | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 3     | RZ_RSPI1_CK   | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 4     | RZ_RSPI1_MISO | Digital Output | Open Drain NMOS 1X                 | floating          |
| 5     | RZ_RSPI1_MOSI | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 6     | RZ_CAN0_TX    | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 7     | RZ_CAN0_RX    | Digital Output | Open Drain NMOS 1X                 | floating          |
| 8     | RZ_CAN1_TX    | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 9     | NC            | --             | Keep Floating or Connect to GND    | --                |
| 10    | RZ_CAN1_RX    | Digital Output | Open Drain NMOS 1X                 | floating          |
| 11    | GND           | GND            | Ground                             | --                |
| 12    | CAN1_RX       | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 13    | CAN1_TX       | Digital Output | Push Pull 1X                       | floating          |
| 14    | VDD2          | PWR            | Supply Voltage                     | --                |
| 15    | CAN0_RX       | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 16    | CAN0_TX       | Digital Output | Push Pull 1X                       | floating          |
| 17    | SPI1_DO       | Digital Output | Push Pull 1X                       | floating          |
| 18    | SPI1_DIN      | Digital Input  | Digital Input with Schmitt trigger | floating          |
| 19    | SPI1_CK       | Digital Output | Push Pull 1X                       | floating          |
| 20    | SPI1_CS0#     | Digital Output | Push Pull 1X                       | floating          |

**Ordering Information**

| Part Number  | Package Type                            |
|--------------|---|
| SLG7RN45294V | 20-pin STQFN - Tape and Reel (3k units) |

**RZ/G2L SMARC SPI/CAN Level Shifter**
**Absolute Maximum Conditions**

| Parameter                                      | Min.                                | Max.      | Unit       |
|--|-------------------------------------|-----------|------------|
| Supply Voltage on VDD relative to GND          | -0.5                                | 7         | V          |
| Supply voltage on VDD2 relative to GND         | -0.5                                | VDD + 0.5 | V          |
| DC Input voltage                               | PINs 2, 3, 4, 5, 6, 7, 8, 9, 10     | GND - 0.5 | VDD + 0.5  |
|  | PINs 12, 13, 15, 16, 17, 18, 19, 20 |           | VDD2 + 0.5 |
| Maximum Average or DC Current<br>(Through pin) | Push-Pull 1x                        | --        | 11         |
|  | OD 1x                               | --        | 11         |
| Current at Input Pin                           | -1.0                                | 1.0       | mA         |
| Input leakage (Absolute Value)                 | --                                  | 1000      | nA         |
| Storage Temperature Range                      | -65                                 | 150       | °C         |
| Junction Temperature                           | --                                  | 150       | °C         |
| ESD Protection (Human Body Model)              | 2000                                | --        | V          |
| ESD Protection (Charged Device Model)          | 500                                 | --        | V          |
| Moisture Sensitivity Level                     |                                     | 1         |            |

**Electrical Characteristics**

| Symbol           | Parameter   | Condition/Note                                | Min. | Typ. | Max. | Unit |
|------------------|---|---|------|------|------|------|
| V <sub>DD</sub>  | Supply Voltage  |   | 4.7  | 5    | 5.5  | V    |
| V <sub>DD2</sub> | Supply Voltage  |   | 1.71 | 1.8  | 5.5  | V    |
| T <sub>A</sub>   | Operating Temperature   |   | -40  | 25   | 85   | °C   |
| C <sub>VDD</sub> | Capacitor Value at VDD  |   | --   | 0.1  | --   | μF   |
| C <sub>IN</sub>  | Input Capacitance   |   | --   | 4    | --   | pF   |
| I <sub>Q</sub>   | Quiescent Current   | Static inputs and floating outputs            | --   | 1    | --   | μA   |
| V <sub>O</sub>   | Maximal Voltage Applied to any PIN in High-Impedance State                |   | --   | --   | VDD  | V    |
| I <sub>VDD</sub> | Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2) | T <sub>J</sub> = 85°C                         | --   | --   | 45   | mA   |
|                  |   | T <sub>J</sub> = 110°C                        | --   | --   | 22   | mA   |
| I <sub>GND</sub> | Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2) | T <sub>J</sub> = 85°C                         | --   | --   | 86   | mA   |
|                  |   | T <sub>J</sub> = 110°C                        | --   | --   | 41   | mA   |
| V <sub>IH</sub>  | HIGH-Level Input Voltage<br>PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10            | Logic Input with Schmitt Trigger at VDD=5.0V  | 3.34 | --   | VDD  | V    |
| V <sub>IH2</sub> | HIGH-Level Input Voltage<br>PINs 12, 13, 15, 16, 17, 18, 19, 20           | Logic Input with Schmitt Trigger at VDD2=1.8V | 1.28 | --   | VDD  | V    |
|                  |   | Logic Input with Schmitt Trigger at VDD2=3.3V | 2.14 | --   | VDD  | V    |
|                  |   | Logic Input with Schmitt Trigger at VDD2=5.0V | 3.34 | --   | VDD  | V    |
| V <sub>IL</sub>  | LOW-Level Input Voltage<br>PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10             | Logic Input with Schmitt Trigger at VDD=5.0V  | 0    | --   | 1.41 | V    |
| V <sub>IL2</sub> | LOW-Level Input Voltage<br>PINs 12, 13, 15, 16, 17, 18, 19, 20            | Logic Input with Schmitt Trigger at VDD2=1.8V | 0    | --   | 0.49 | V    |
|                  |   | Logic Input with Schmitt Trigger at VDD2=3.3V | 0    | --   | 0.97 | V    |

**RZ/G2L SMARC SPI/CAN Level Shifter**

|   |   |  |       |       |      |    |
|---|---|--|-------|-------|------|----|
|   |   | Logic Input with Schmitt Trigger at VDD2=5.0V            | 0     | --    | 1.41 | V  |
| V <sub>OH2</sub>  | HIGH-Level Output Voltage<br>PINs 12, 13, 15, 16, 17, 18,<br>19, 20                 | Push-Pull 1X, I <sub>OH</sub> =100μA at<br>VDD2=1.8V     | 1.69  | 1.79  | --   | V  |
|   |   | Push-Pull 1X, I <sub>OH</sub> =3mA at<br>VDD2=3.3V       | 2.74  | 3.12  | --   | V  |
|   |   | Push-Pull 1X, I <sub>OH</sub> =5mA at<br>VDD2=5.0V       | 4.15  | 4.76  | --   | V  |
| V <sub>OL</sub>   | LOW-Level Output Voltage<br>PINs 2, 3, 4, 5, 6, 7, 8, 9 and<br>10                   | Open Drain NMOS 1X,<br>I <sub>OL</sub> =5mA at VDD=5.0V  | --    | 0.12  | 0.16 | V  |
| V <sub>OL2</sub>  | LOW-Level Output Voltage<br>PINs 12, 13, 15, 16, 17, 18,<br>19, 20                  | Push-Pull 1X, I <sub>OL</sub> =100μA at<br>VDD2=1.8V     | --    | 0.01  | 0.03 | V  |
|   |   | Push-Pull 1X, I <sub>OL</sub> =3mA at<br>VDD2=3.3V       | --    | 0.13  | 0.23 | V  |
|   |   | Push-Pull 1X, I <sub>OL</sub> =5mA at<br>VDD2=5.0V       | --    | 0.19  | 0.24 | V  |
| I <sub>OH2</sub>  | HIGH-Level Output Current<br>(see Note 1)<br>PINs 12, 13, 15, 16, 17, 18,<br>19, 20 | Push-Pull 1X, V <sub>OH</sub> =VDD-0.2V<br>at VDD2=1.8V  | 1.07  | 1.70  | --   | mA |
|   |   | Push-Pull 1X, V <sub>OH</sub> =2.4V at<br>VDD2=3.3V      | 6.05  | 12.08 | --   | mA |
|   |   | Push-Pull 1X, V <sub>OH</sub> =2.4V at<br>VDD2=5.0V      | 22.08 | 34.04 | --   | mA |
| I <sub>OL</sub>   | LOW-Level Output Current<br>(see Note 1)<br>PINs 2, 3, 4, 5, 6, 7, 8, 9 and<br>10   | Open Drain NMOS 1X,<br>V <sub>OL</sub> =0.4V at VDD=5.0V | 10.82 | 17.38 | --   | mA |
| I <sub>OL2</sub>  | LOW-Level Output Current<br>(see Note 1)<br>PINs 12, 13, 15, 16, 17, 18,<br>19, 20  | Push-Pull 1X, V <sub>OL</sub> =0.15V at<br>VDD2=1.8V     | 0.92  | 1.69  | --   | mA |
|   |   | Push-Pull 1X, V <sub>OL</sub> =0.4V at<br>VDD2=3.3V      | 4.88  | 8.24  | --   | mA |
|   |   | Push-Pull 1X, V <sub>OL</sub> =0.4V at<br>VDD2=5.0V      | 7.22  | 11.58 | --   | mA |
| T <sub>SU</sub>   | Startup Time  | From VDD rising past<br>PON <sub>THR</sub>               | 0.61  | 1.24  | 1.65 | ms |
| PON <sub>THR</sub>  | Power On Threshold  | V <sub>DD</sub> Level Required to Start<br>Up the Chip   | 1.41  | 1.54  | 1.66 | V  |
| POFF <sub>THR</sub>   | Power Off Threshold   | V <sub>DD</sub> Level Required to Switch<br>Off the Chip | 1.00  | 1.15  | 1.31 | V  |
| <b>Note:</b><br>1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.<br>2. The GreenPAK's power rails are divided in two sides. PINs 2, 3, 4, 5, 6, 7, 8, 9 and 10 are connected to one side, PINs 12, 13, 15, 16, 17, 18, 19, and 20 to another.<br>3. Guaranteed by Design. |   |  |       |       |      |    |

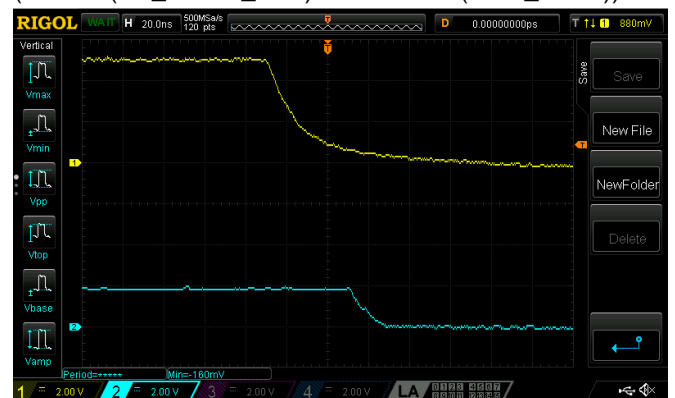
## Functionality Waveforms

Channel 1 (yellow/top line) – PIN# 2 (RZ\_RSPI1\_SSL)  
 Channel 2 (light blue/2nd line) – PIN# 20 (SPI1\_CS0#)

1. Transient from Low to High  
 (PIN# 2 (RZ\_RSPI1\_SSL) => PIN# 20 (SPI1\_CS0#))

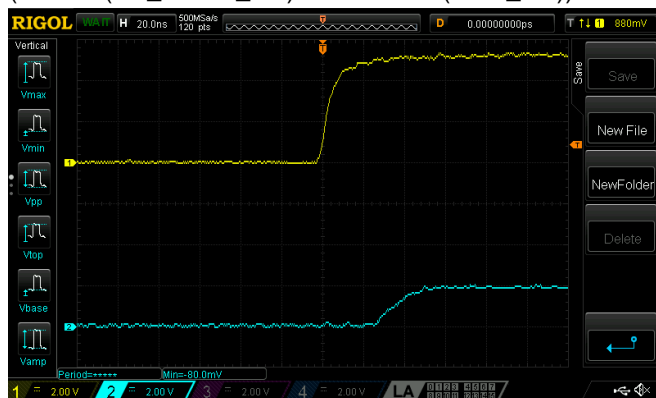


2. Transient from High to Low  
 (PIN# 2 (RZ\_RSPI1\_SSL) => PIN# 20 (SPI1\_CS0#))

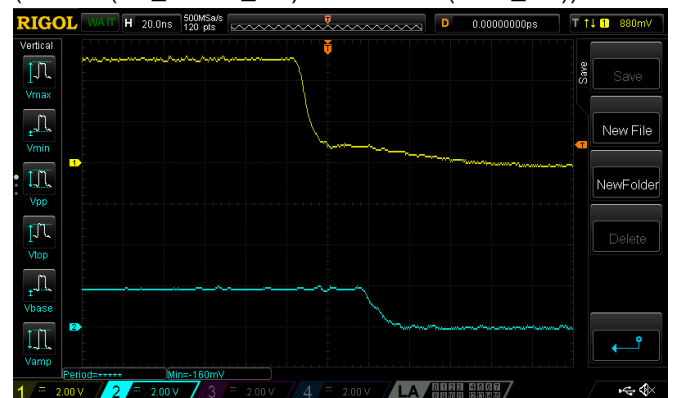


Channel 1 (yellow/top line) – PIN# 3 (RZ\_RSPI1\_CK)  
 Channel 2 (light blue/2nd line) – PIN# 19 (SPI1\_CK)

3. Transient from Low to High  
 (PIN# 3 (RZ\_RSPI1\_CK) => PIN# 19 (SPI1\_CK))



4. Transient from High to Low  
 (PIN# 3 (RZ\_RSPI1\_CK) => PIN# 19 (SPI1\_CK))



**RZ/G2L SMARC SPI/CAN Level Shifter**

Channel 1 (yellow/top line) – PIN# 4 (RZ\_RSPI1\_MISO) with external 5kΩ pull up resistor

Channel 2 (light blue/2nd line) – PIN# 18 (SPI1\_DIN)

5. Transient from Low to High  
(PIN# 18 (SPI1\_DIN) => PIN# 4 (RZ\_RSPI1\_MISO))



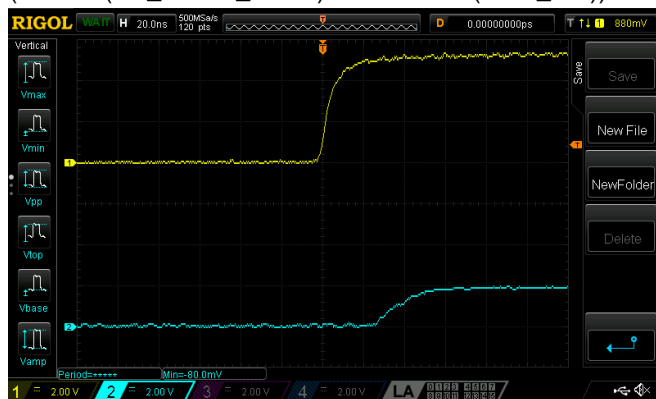
6. Transient from High to Low  
(PIN# 18 (SPI1\_DIN) => PIN# 4 (RZ\_RSPI1\_MISO))



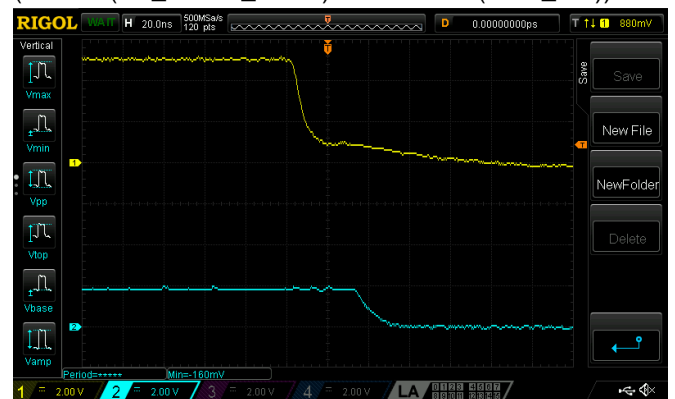
Channel 1 (yellow/top line) – PIN# 5 (RZ\_RSPI1\_MOSI)

Channel 2 (light blue/2nd line) – PIN# 17 (SPI1\_DO)

7. Transient from Low to High  
(PIN# 5 (RZ\_RSPI1\_MOSI) => PIN# 17 (SPI1\_DO))



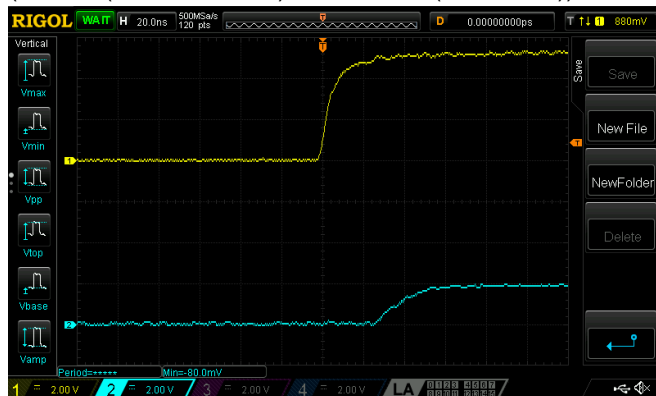
8. Transient from High to Low  
(PIN# 5 (RZ\_RSPI1\_MOSI) => PIN# 17 (SPI1\_DO))



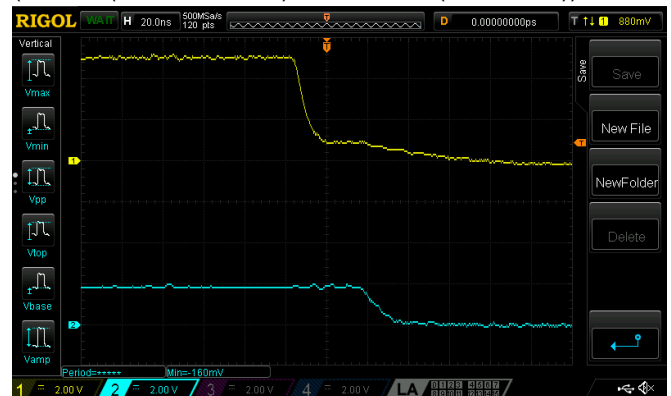
**RZ/G2L SMARC SPI/CAN Level Shifter**

Channel 1 (yellow/top line) – PIN# 6 (RZ\_CAN0\_TX)  
 Channel 2 (light blue/2nd line) – PIN# 16 (CAN0\_TX)

9. Transient from Low to High  
 (PIN# 6 (RZ\_CAN0\_TX) => PIN# 16 (CAN0\_TX))

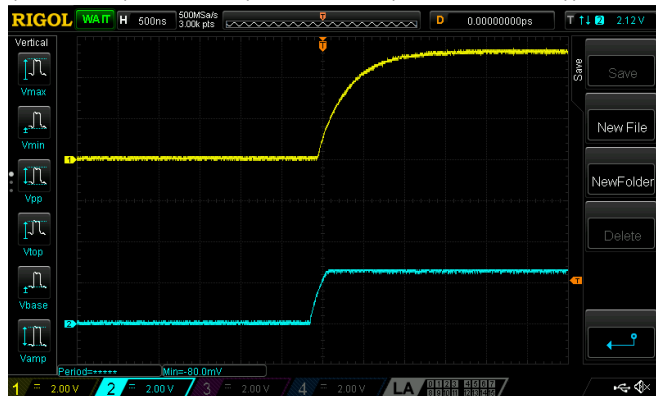


10. Transient from High to Low  
 (PIN# 6 (RZ\_CAN0\_TX) => PIN# 16 (CAN0\_TX))

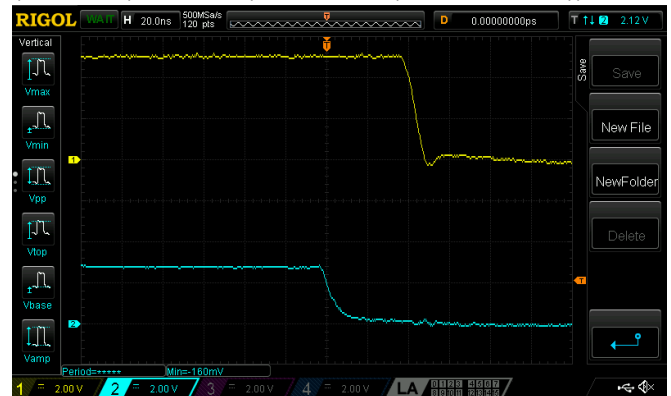


Channel 1 (yellow/top line) – PIN# 7 (RZ\_CAN0\_RX) with external 5kΩ pull up resistor  
 Channel 2 (light blue/2nd line) – PIN# 15 (CAN0\_RX)

11. Transient from Low to High  
 (PIN# 15 (CAN0\_RX) => PIN# 7 (RZ\_CAN0\_RX))



12. Transient from High to Low  
 (PIN# 15 (CAN0\_RX) => PIN# 7 (RZ\_CAN0\_RX))

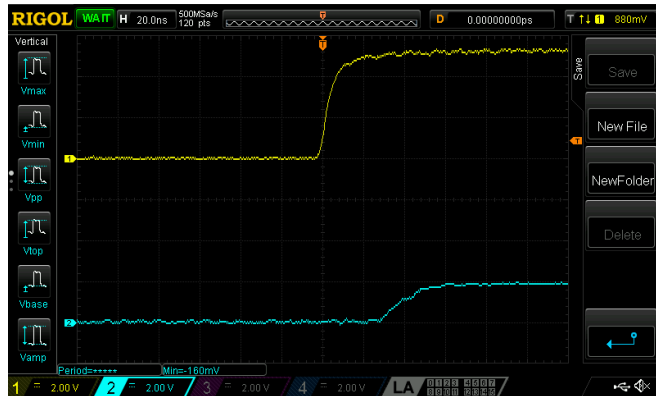




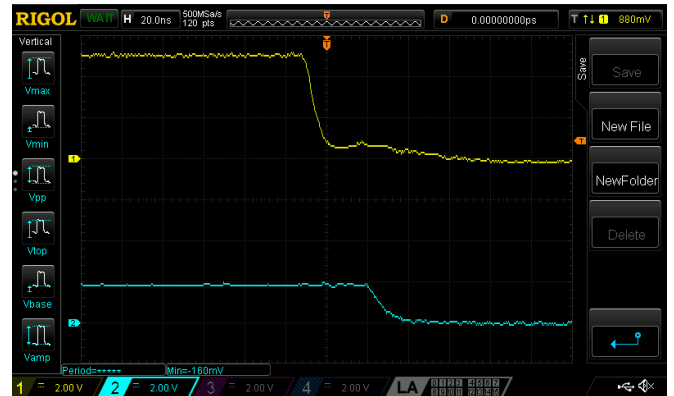
**RZ/G2L SMARC SPI/CAN Level Shifter**

Channel 1 (yellow/top line) – PIN# 8 (RZ\_CAN1\_TX)  
 Channel 2 (light blue/2nd line) – PIN# 13 (CAN1\_TX)

13. Transient from Low to High  
 (PIN# 8 (RZ\_CAN1\_TX) => PIN# 13 (CAN1\_TX))

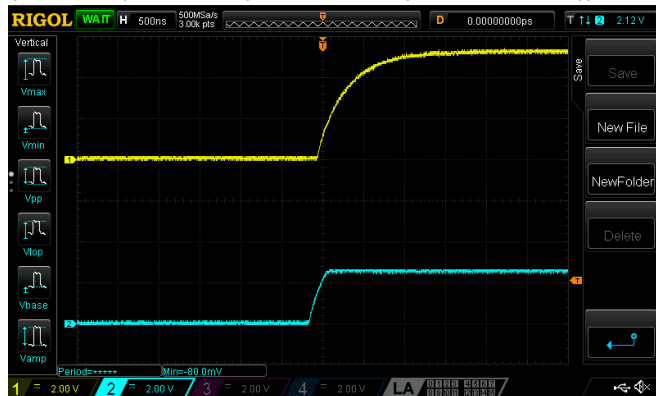


14. Transient from High to Low  
 (PIN# 8 (RZ\_CAN1\_TX) => PIN# 13 (CAN1\_TX))

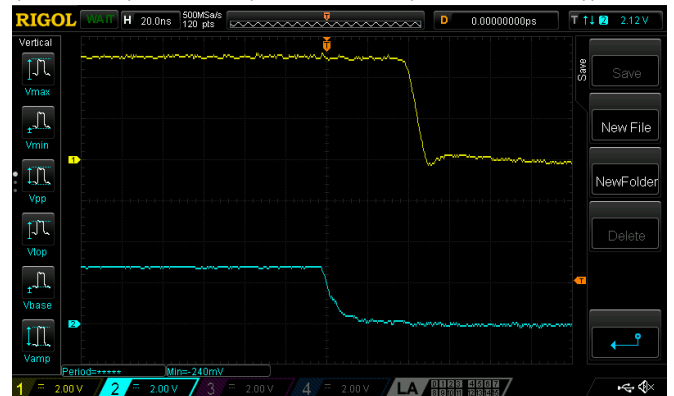


Channel 1 (yellow/top line) – PIN# 10 (RZ\_CAN1\_RX) with external 5kΩ pull up resistor  
 Channel 2 (light blue/2nd line) – PIN# 12 (CAN1\_RX)

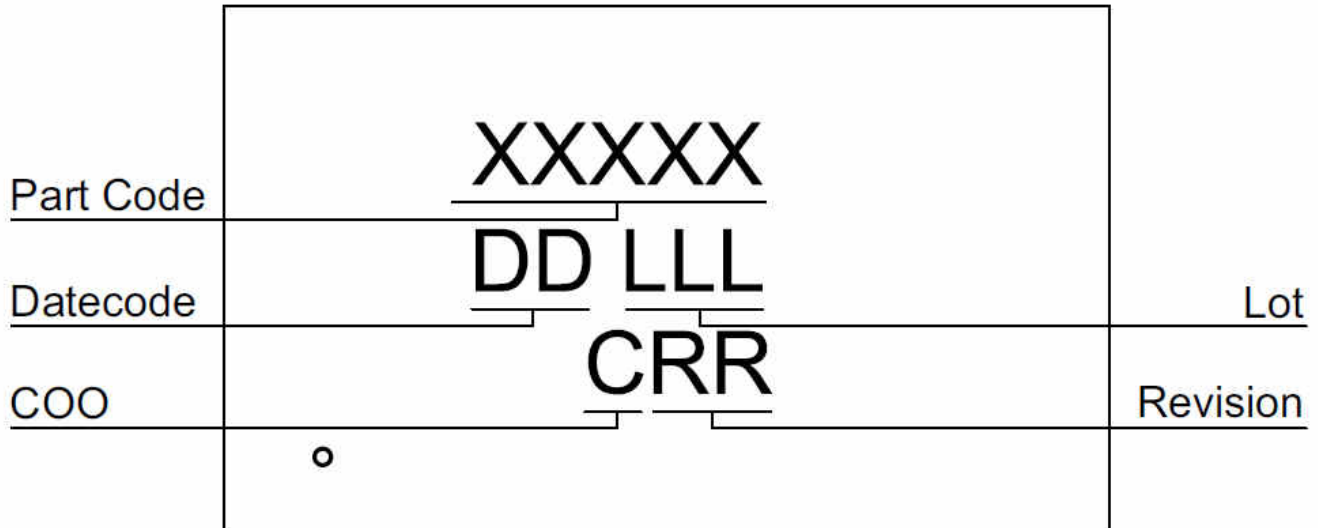
15. Transient from Low to High  
 (PIN# 12 (CAN1\_RX) => PIN# 10 (RZ\_CAN1\_RX))



16. Transient from High to Low  
 (PIN# 12 (CAN1\_RX) => PIN# 10 (RZ\_CAN1\_RX))



#### Package Top Marking



- XXXXX – Part ID Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

| Datasheet Revision | Programming Code Number | Lock Status | Checksum   | Part Code | Revision | Date       |
|--------------------|-------------------------|-------------|------------|-----------|----------|------------|
| 0.11               | 001                     | U           | 0xA06DDF4E |           |          | 07/11/2023 |

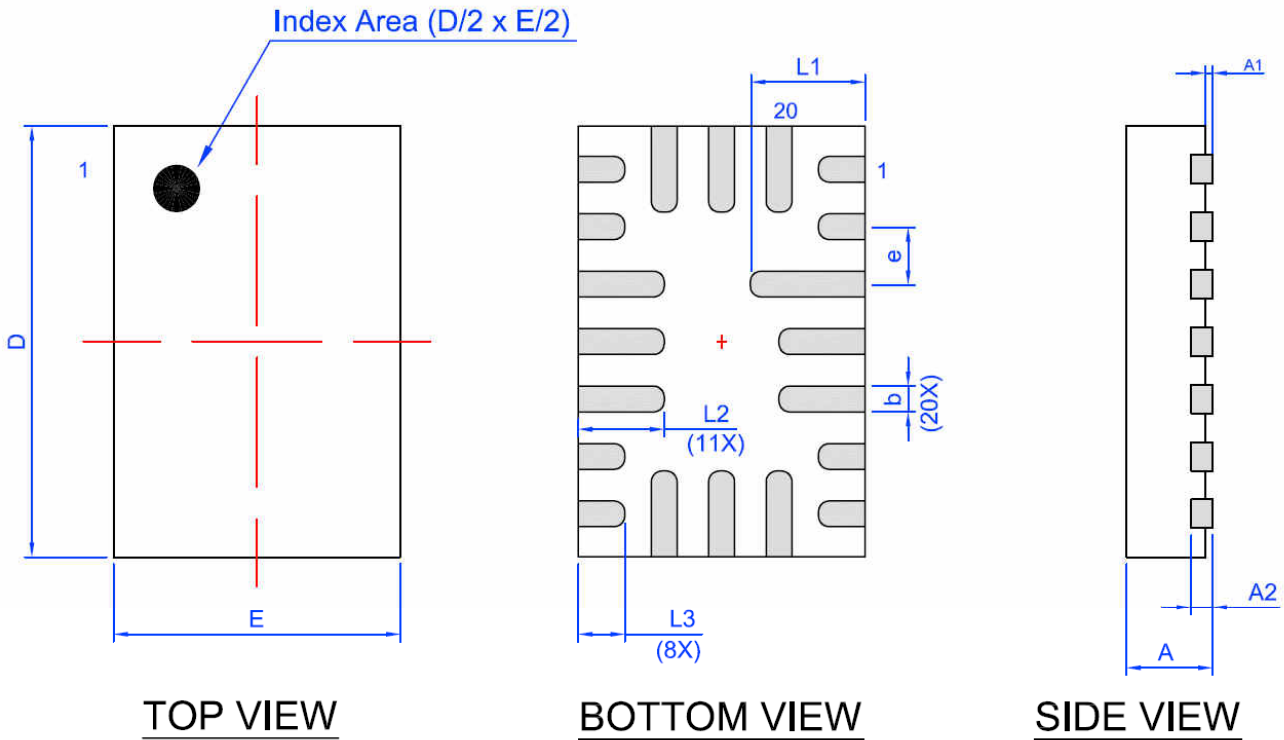
Lock coverage for this part is indicated by  $\surd$ , from one of the following options:

|         |   |
|---------|---|
| $\surd$ | Unlocked  |
|         | Locked for read, bits <1535:0>                      |
|         | Locked for write, bits <1535:0>                     |
|         | Locked for write all bits                           |
|         | Locked for read and write bits <1535:0>             |
|         | Locked for read bits <1535:0> and write of all bits |

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

#### Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P COL Package  
JEDEC MO-220



Unit: mm

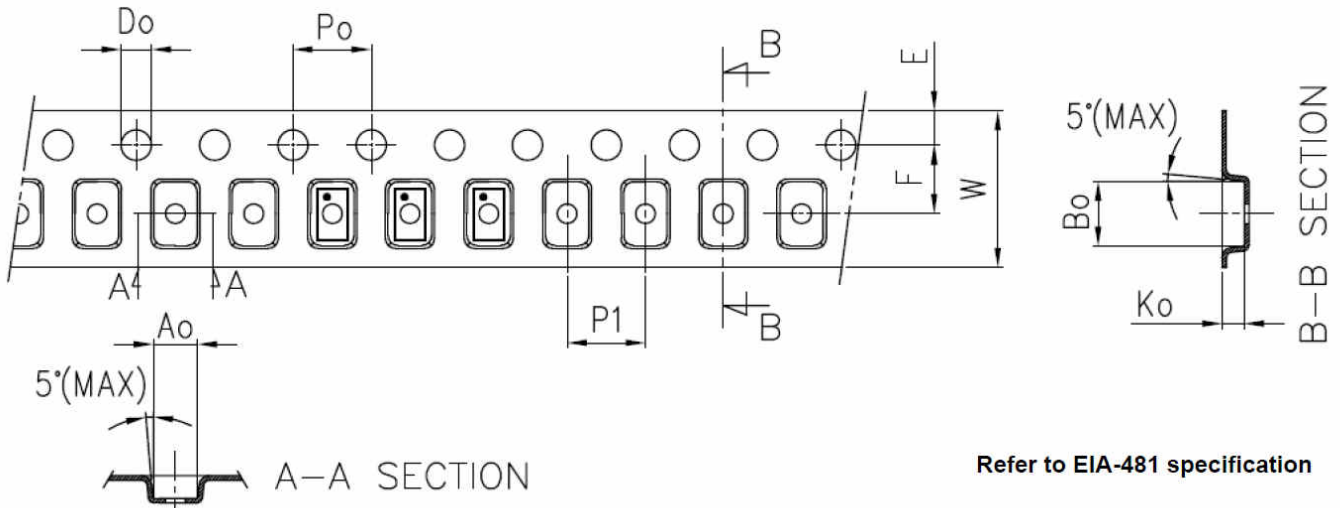
| Symbol | Min      | Nom. | Max   | Symbol | Min   | Nom.  | Max   |
|--------|----------|------|-------|--------|-------|-------|-------|
| A      | 0.50     | 0.55 | 0.60  | D      | 2.95  | 3.00  | 3.05  |
| A1     | 0.005    | -    | 0.050 | E      | 1.95  | 2.00  | 2.05  |
| A2     | 0.10     | 0.15 | 0.20  | L1     | 0.75  | 0.80  | 0.85  |
| b      | 0.13     | 0.18 | 0.23  | L2     | 0.55  | 0.60  | 0.65  |
| e      | 0.40 BSC |      |       | L3     | 0.275 | 0.325 | 0.375 |

#### Tape and Reel Specification

| Package Type                         | # of Pins | Nominal Package Size [mm] | Max Units |         | Reel & Hub Size [mm] | Leader (min) |             | Trailer (min) |             | Tape Width [mm] | Part Pitch [mm] |
|--------------------------------------|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
|                                      |           |                           | per Reel  | per Box |                      | Pockets      | Length [mm] | Pockets       | Length [mm] |                 |                 |
| STQFN<br>20L<br>2x3mm<br>0.4P<br>COL | 20        | 2x3x0.55                  | 3000      | 3000    | 178/60               | 100          | 400         | 100           | 400         | 8               | 4               |

#### Carrier Tape Drawing and Dimensions

| Package Type                       | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|------------------------------------|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
|                                    | A0                | B0               | K0           | P0               | P1           | D0                  | E                       | F                           | W          |
| STQFN<br>20L 2x3<br>mm 0.4P<br>COL | 2.2               | 3.15             | 0.76         | 4                | 4            | 1.5                 | 1.75                    | 3.5                         | 8          |



#### Recommended Reflow Soldering Profile

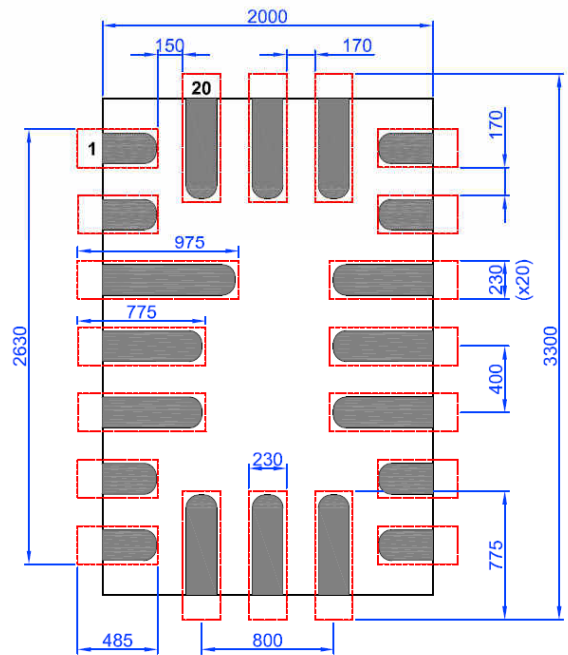
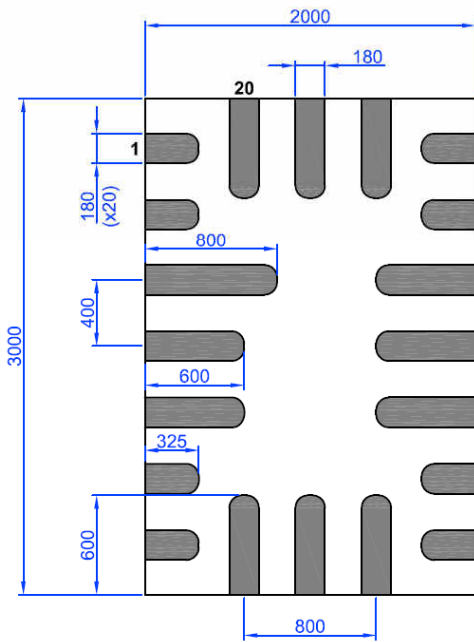
Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

#### Recommended Land Pattern

 Exposed Pad  
(Top View)

 Recommended Land Pattern  
(Top View)

Units:  $\mu\text{m}$



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**Datasheet Revision History**

| <b>Date</b> | <b>Version</b> | <b>Change</b>             |
|-------------|----------------|---------------------------|
| 10/07/2021  | 0.10           | New design                |
| 07/11/2023  | 0.11           | Moved to Renesas template |

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