SLG7RN45652

GreenPAK ™

DC Motor Driver

General Description

The SLG7RN45652 provides a small, low power component for commonly used Mixed-Signal and H-Bridge functions.

The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

Configurable PWM macrocells in combination with Special High Voltage outputs will be useful for a motor drive or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load.

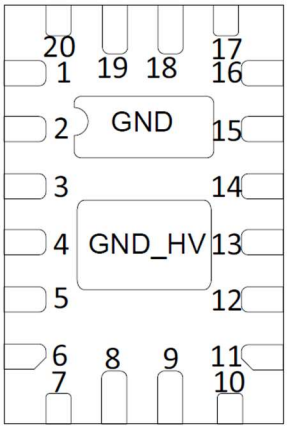
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package
- Four High Voltage High Current Drive GPOs
- Current up to 1.5A RMS per GPO/ H-Bridge
- Differential Amplifier with Integrator
- Two Current Sense Comparators
- Two PWM Macrocells

Output Summary

2 Outputs - High Drive Push Pull

Pin Configuration

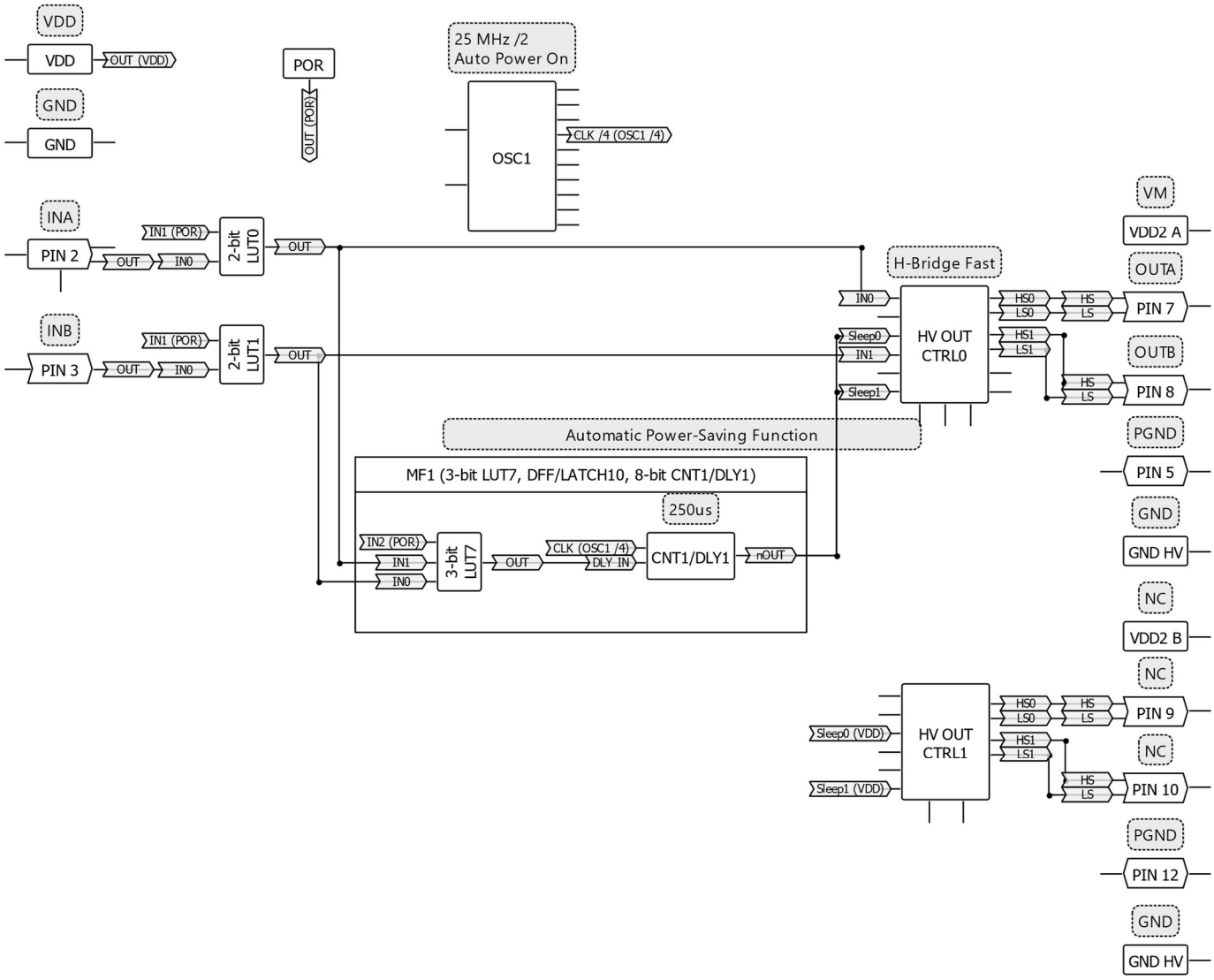


STQFN-20L
(Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	11	VDD2_B
2	INA	12	PGND
3	INB	13	GND
4	GND	14	NC
5	PGND	15	NC
6	VDD2_A	16	NC
7	OUTA	17	NC
8	OUTB	18	GND
9	NC	19	NC
10	NC	20	NC

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	INA	Digital Input	Low Voltage Digital Input	1MΩ pulldown
3	INB	Digital Input	Low Voltage Digital Input	1MΩ pulldown
4	GND	GND	Ground	--
5	PGND	Analog Input/Output	Analog Input/Output	floating
6	VDD2_A	PWR	Supply Voltage	
7	OUTA	High Drive Output	High Drive Push Pull	floating
8	OUTB	High Drive Output	High Drive Push Pull	floating
9	NC	--	Keep Floating or Connect to GND	--
10	NC	--	Keep Floating or Connect to GND	--
11	VDD2_B	PWR	Supply Voltage	
12	PGND	Analog Input/Output	Analog Input/Output	floating
13	GND	GND	Ground	--
14	NC	--	Keep Floating or Connect to GND	--
15	NC	--	Keep Floating or Connect to GND	--
16	NC	--	Keep Floating or Connect to GND	--
17	NC	--	Keep Floating or Connect to GND	--
18	GND	GND	Ground	--
19	NC	--	Keep Floating or Connect to GND	--
20	NC	--	Keep Floating or Connect to GND	--

Ordering Information

Part Number	Package Type
SLG7RN45652V	20-pin STQFN
SLG7RN45652VTR	20-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Description	Condition	Min.	Max.	Unit
Supply voltage on VDD relative to GND				-0.3	7.0	V
Supply voltage on VDD2 relative to GND				-0.3	18	V
DC Input Voltage				GND - 0.5V	VDD + 0.5V	V
Maximum VDD Average or DC Current		(Through VDD or GND pin) for VDD group		--	120	mA
Maximum VDD2 Average or DC Current		(Through each VDD2_A, VDD2_B, SENSE_A or SENSE_B pin)		--	2000	mA
Maximum Average or DC Current (VDD2 power supply)	Push-Pull /Half Bridge	Through VDD2 High Current Group pins		--	1500	mA
Maximum pulsed current sink/sourced per HV HD pin		Pulse width < 0.5ms; duty cycle < 2%		--	Internally limited by OCP	mA
Current at Input Pin		Through VDD Group pin		-0.1	1.0	mA
Input Leakage Current (Absolute Value)				--	1000	nA
Storage Temperature Range				-65	150	°C
Junction Temperature				--	150	°C
ESD Protection (Human Body Model)				4000	--	V
ESD Protection (Charged Device Model)				1300	--	V
Moisture Sensitivity Level				1		

Thermal Information

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
Θ_{JA}	Thermal Resistance	4L JEDEC PCB	--	--	65	°C/W
Θ_{JA}	Thermal Resistance	4L JEDEC PCB with a thermal vias that connect thermal pad through all layers of the PCB	--	--	46	°C/W
$\Theta_{JC(top)}$	Junction-to-case (top) Thermal Resistance		--	23.50	--	°C/W
Θ_{JB}	Junction-to-board Thermal Resistance		--	25.51	--	°C/W
$\Psi_{JC(top)}$	Junction-to-case (top) Characterization Parameter		--	6.80	--	°C/W
Ψ_{JB}	Junction-to-board Characterization Parameter		--	24.44	--	°C/W

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		2.3	4.2	5	V
V_{DD2_A}	Supply Voltage		3	12	13.2	V
V_{DD2_B}	Supply Voltage		3	12	13.2	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		0.1	--	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current VDD side	Static inputs and floating outputs, PINs 2 and 3 are HIGH	--	11.0	--	µA
$I_{Q\ VDD2\_A}$	Quiescent Current VDD2_A side	Static inputs and floating outputs, PINs 2 and 3 are HIGH	--	0.5	--	µA
V_{IH}	HIGH-Level Input Voltage (Note 1)	Low-Level Logic Input at VDD=2.5V (Note 1)	1.25	--	VDD+ 0.3	V
		Low-Level Logic Input at VDD=3.3V (Note 1)	1.25	--	VDD+ 0.3	V
		Low-Level Logic Input at VDD=5.0V (Note 1)	1.25	--	VDD+ 0.3	V
V_{IL}	LOW-Level Input Voltage (Note 1)	Low-Level Logic Input at VDD=2.5V (Note 1)	GND- 0.3	--	0.5	V
		Low-Level Logic Input at VDD=3.3V (Note 1)	GND- 0.3	--	0.5	V
		Low-Level Logic Input at VDD=5.0V (Note 1)	GND- 0.3	--	0.5	V
V_{OH2}	HIGH-Level Output Voltage for V_{DD2} High Current Group	Push-Pull, V_{DD}=5±10%, I_{OH2}=10mA	4.496	--	--	V
		Push-Pull, V_{DD}=9V±10%, I_{OH2}=10mA	8.097	--	--	V
		Push-Pull, V_{DD}=12V±10%, I_{OH2}=10mA	10.797	--	--	V
V_{OL2}	LOW-Level Output Voltage for V_{DD2} High Current Group	Push-Pull, V_{DD}=5±10%, I_{OL2}=10mA	--	--	0.004	V
		Push-Pull, V_{DD}=9V±10%, I_{OL2}=10mA	--	--	0.004	V
		Push-Pull, V_{DD}=12V±10%, I_{OL2}=10mA	--	--	0.004	V
R_{PULL_DOWN}	Pull Down Resistance T_J=-40°C to 85°C	Pull down on PINs 2, 3	790	--	1250	kΩ
	Pull Down Resistance T_J=-40°C to 150°C	Pull down on PINs 2, 3	790	--	1250	kΩ
T_{DLY1}	Delay1 Time	At temperature 25°C	244	250	257	µs
		At temperature -40 +85°C	238	250	263	µs
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.8	1.98	2.16	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	1.33	1.55	1.83	V

Note: 1 No hysteresis.
Note: 2 DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.

HV Output Electrical Characteristic (Pre-driver Mode)

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
t_R	Rise time HV OUT	VDD2=5V, 16Ω to GND, 10% to 90% VDD2, T_J=-40°C to 85°C	10	13	21	ns
		VDD2=5V, 16Ω to GND, 10% to 90% VDD2, T_J=-40°C to 150°C	10	13	22	ns
t_F	Fall time HV OUT	VDD2=5V, 16Ω to GND, 10% to 90% VDD2, T_J=-40°C to 85°C	8	11	23	ns
		VDD2 = 5 V, 16 Ω to GND, 10 % to 90 % VDD2, T_J=-40 °C to 150°C	8	11	25	ns
t_{DEAD}	Dead band time of HV_GPOx_HD in Predriver mode(not for Driver mode) (Break before making For Full Bridge and Half Bridge mode)	VDD2=3V, T_J=-40°C to 150°C	--	55	--	ns
		VDD2=5V, T_J=-40°C to 150°C	--	23	--	ns
		VDD2=13.2V, T_J=-40°C to 150°C	--	22	--	ns
PWM_t_{DEAD}	PWM dead band time	Configured in PWM block		0; 1·Tclk; 2·Tclk; 3·Tclk;		Clk time
$R_{DS(ON)}$	HS FET on resistance (SENSE, GND_HV and GND Pins are connected together)	VDD2=13.2V, Io=500mA, T_J=25°C	--	171	--	mΩ
		VDD2=13.2V, Io=500mA, T_J=150°C	--	--	295	mΩ
		VDD2=9.0V, Io=500mA, T_J=25°C	--	171	--	mΩ
		VDD2=9.0V, Io=500mA, T_J=150°C	--	--	295	mΩ
		VDD2=5.0V, Io=500mA, T_J=25°C	--	177	--	mΩ
		VDD2=5.0V, Io=500mA, T_J=150°C	--	--	305	mΩ
		VDD2=3.0V, Io=500mA, T_J=25°C	--	256	--	mΩ
		VDD2=3.0V, Io=500mA, T_J=150°C	--	--	426	mΩ
$R_{DS(ON)}$	LS FET on resistance (SENSE_A, SENSE_B, GND_HV and GND Pins are connected together, RDS(ON) with Sense Pin=GND, If Sense Pin VDD=0.5V additional 100mΩ at worst case)	VDD2=13.2V, Io=500mA, T_J=25°C	--	182	--	mΩ
		VDD2=13.2V, Io=500mA, T_J=150°C	--	--	332	mΩ
		VDD2=9.0V, Io=500mA, T_J=25°C	--	182	--	mΩ
		VDD2=9.0V, Io=500mA, T_J=150°C	--	--	331	mΩ
		VDD2=5.0V, Io=500mA, T_J=25°C	--	185	--	mΩ

		VDD2=5.0V, Io=500mA, T_J=150°C	--	--	338	mΩ
		VDD2=3.0V, Io=500mA, T_J=25°C	--	232	--	mΩ
		VDD2=3.0V, Io=500mA, T_J=150°C	--	--	414	mΩ
I_{OFF}	Off-state leakage current	GPO0_HD, GPO1_HD (Note1), VDD2=5.0V, T_J=-40°C to 85°C PWM is off, including the charge pump OSC	23.2	--	32.9	µA
		GPO0_HD, GPO1_HD (Note1), VDD2=5.0V, T_J=-40°C to 150°C PWM is off, including the charge pump OSC	23.2	--	35.2	µA
		GPO2_HD, GPO3_HD, VDD2=5.0V, T_J=-40°C to 85°C PWM is off, including the charge pump OSC	--	--	0.2	nA
		GPO2_HD, GPO3_HD, VDD2=5.0V, T_J=-40°C to 150°C PWM is off, including the charge pump OSC	--	--	1.5	µA
I_{cc}	Charge Pump consumption current (from VDD1 Pin or VDD2 Pin)	VDD2=5.0V, T_J=-40°C to 150°C, PWM is off, including the charge pump OSC	--	--	200	µA
I_{cc}	Charge Pump consumption current (from VDD1 Pin or VDD2 Pin)	VDD2=5.0V, T_J=-40°C to 150°C, PWM=250kHz	100	--	800	µA
t_{WAKE}	Wake-up time	HV SLEEP OUT high to output transition, BG is always on, Another pins SLEEP - disable	--	82.3	134	µs
Note: 1 There is a resistive voltage divider in front of Diff Amplifier that is connected to GPO0_HD and GPO1_HD.						

Protection Circuits

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
I_{OCP}	Overcurrent protection threshold	Per any HS or LS FET	--	2.18	--	A
t_{OCP1} (Disabled)	OCP deglitch time (Note 1)	VDD=5V, VDD2=5V, T=25°C, Deglitch=Enable, High Side	--	2.497	--	µs
		VDD=5V, VDD2=5V, T=25°C, Deglitch=Enable, Low Side	--	1.232	--	µs
t_{OCP2}	OCP retry time (Note 2)	Delay=988µs	--	982	--	µs
V_{UVLO} (Disabled) (Note 3)	Recover from undervoltage lockout	At rising edge of VDD2	--	--	2.90	V
	Undervoltage lockout	At falling edge of VDD2	--	--	2.77	V
T_{TSD}	Thermal shutdown temperature	Junction temperature T_J	135	141	159	°C

T_{HYST}	Thermal shutdown hysteresis		--	16	--	°C

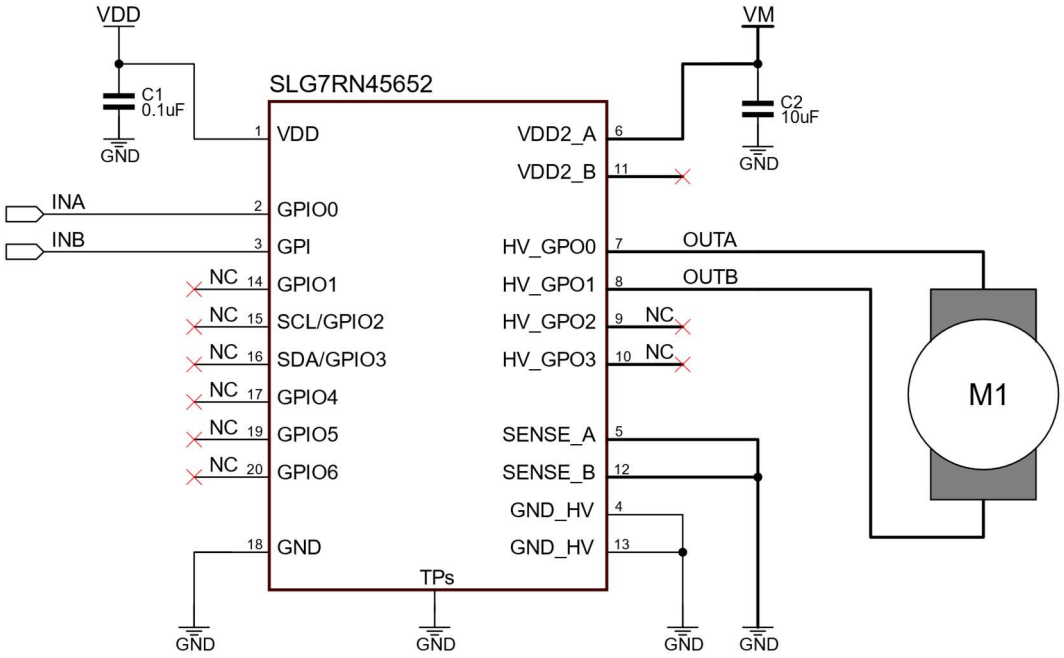
Note: 1 OCP deglitch time option can be enabled by register [873] and register [875] separately for each Full Bridge. The High Side FETs doesn't have OCP deglitch time if the current through the FET is higher than IOCP level during enable time.This is done to avoid huge currents during retry when the short is persist on the output.
Note: 2 OCP retry time can be selected separately for each HV OUT: HV GPO0 - registers[780:778], HV GPO1 - registers[788:786], HV GPO2 - registers[796:794], HV GPO3 - registers[804:802].
Note: 3 UVLO Function can be enabled separately for VDD2_A by register [864] and VDD2_B by register [865].

Truth Tables

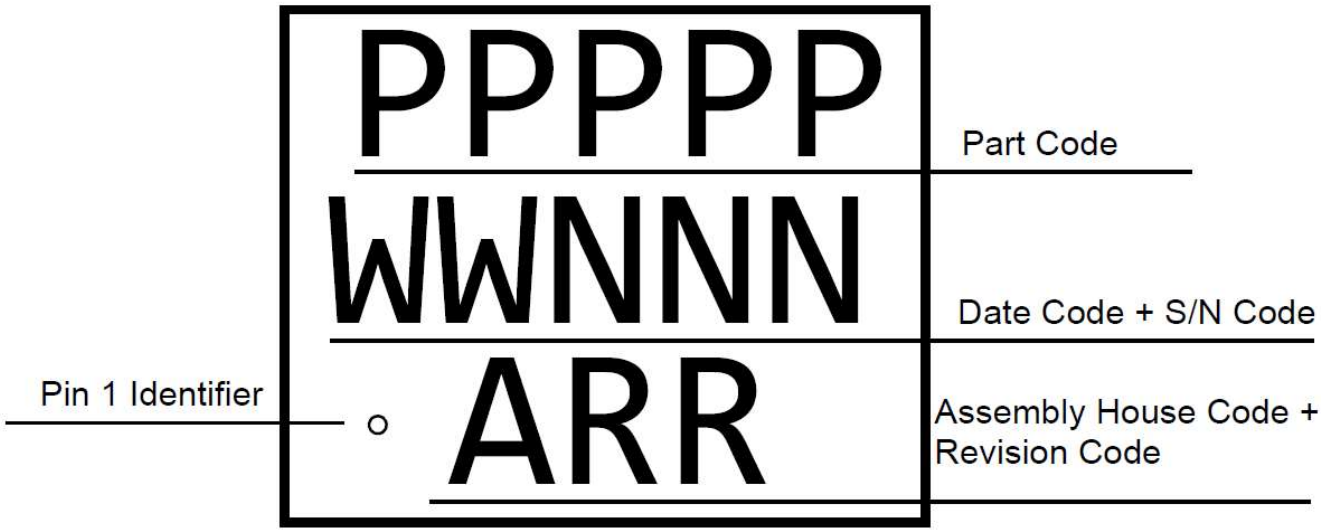
1. I/O Truth Table

INA	INB	OUTA	OUTB	Function
H	H	Hi-Z	Hi-Z	Open
L	H	H	L	Clockwise
H	L	L	H	Counter clockwise
L	L	L	L	Short Brake

Typical Application Circuit



Package Top Marking



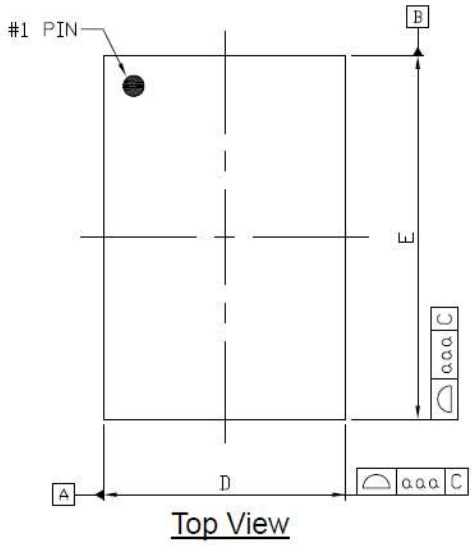
Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
1.01	002	L	0x78289D1D	45652		06/30/2022

Lock coverage for this part is indicated by √, from one of the following options:

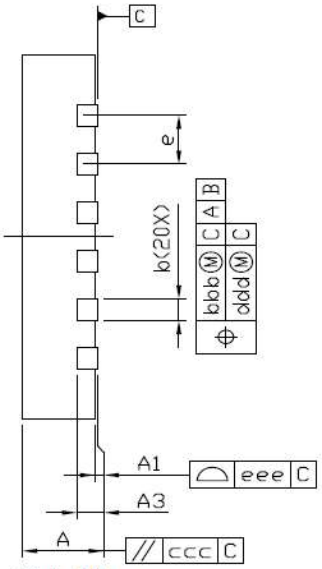
	Unlocked
√	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

The IC security bit is locked/set for code security for production unless otherwise specified.
The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

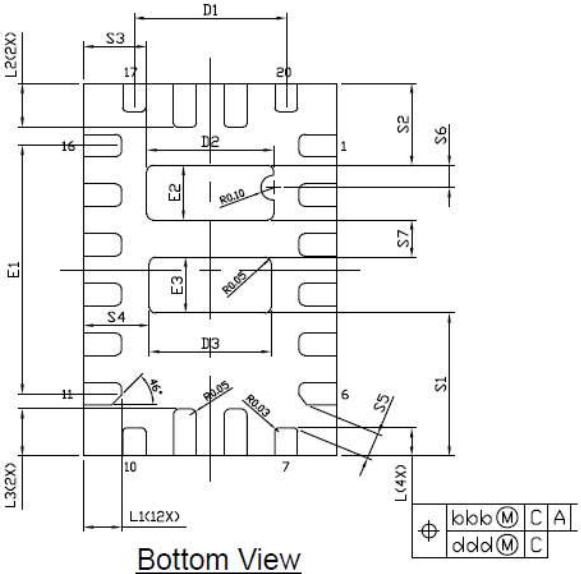
Package Outlines



Top View



Side View



Bottom View

Notes:

1. All dimensions are in millimeters.

2. Dimension "b" applies to metalized terminal and is measured between 0.15 mm and 0.30 mm from the terminal tip. If the terminal has the optional radius on the other end of the terminal, the dimension "b" should not be measured in that radius area.

3. Bilateral coplanarity zone applies to the exposed heat sink slug as well as the terminal.

Controlling dimension: mm

Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.50	0.55	0.60	0.020	0.022	0.024
A1	0.000	0.020	0.050	0.000	0.001	0.002
A3	0.10	0.15	0.20	0.004	0.006	0.008
D	1.95	2.00	2.05	0.077	0.079	0.081
E	2.95	3.00	3.05	0.116	0.118	0.120
D1	1.15	1.20	1.25	0.045	0.047	0.049
E1	1.95	2.00	2.05	0.077	0.079	0.081
D2	0.95	1.00	1.05	0.037	0.039	0.041
E2	0.39	0.44	0.49	0.015	0.017	0.019
D3	0.91	0.96	1.01	0.036	0.038	0.040
E3	0.40	0.45	0.50	0.016	0.018	0.020
S1	1.10	1.15	1.20	0.043	0.045	0.047
S2	0.61	0.66	0.71	0.024	0.026	0.028
S3	0.45	0.50	0.55	0.018	0.020	0.022
S4	0.47	0.52	0.57	0.018	0.020	0.022
S5	0.208 REF			0.008 REF		
S6	0.180 REF			0.007 REF		
S7	0.300 REF			0.012 REF		

"A1" max lead coplanarity 0.05 mm
Standard tolerance: ±0.05

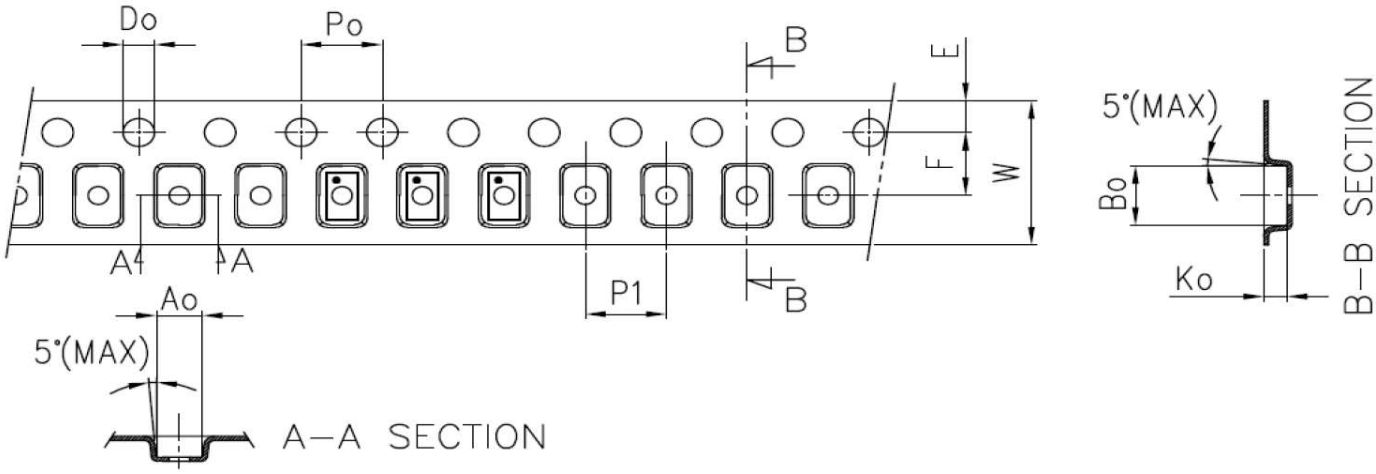
Symbol	MILLIMETER			INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
e	0.40 BSC			0.016 BSC		
L	0.175	0.225	0.275	0.007	0.009	0.011
L1	0.250	0.300	0.350	0.010	0.012	0.014
L2	0.300	0.350	0.400	0.012	0.014	0.016
L3	0.330	0.380	0.430	0.013	0.015	0.017
b	0.130	0.180	0.230	0.005	0.007	0.009
aaa	0.07			0.003		
bbb	0.07			0.003		
ccc	0.1			0.004		
ddd	0.05			0.002		
eee	0.08			0.003		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2mm x 3mm 0.4P FCD Green	20	2.0x3.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2mm x 3mm 0.4P FCD Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

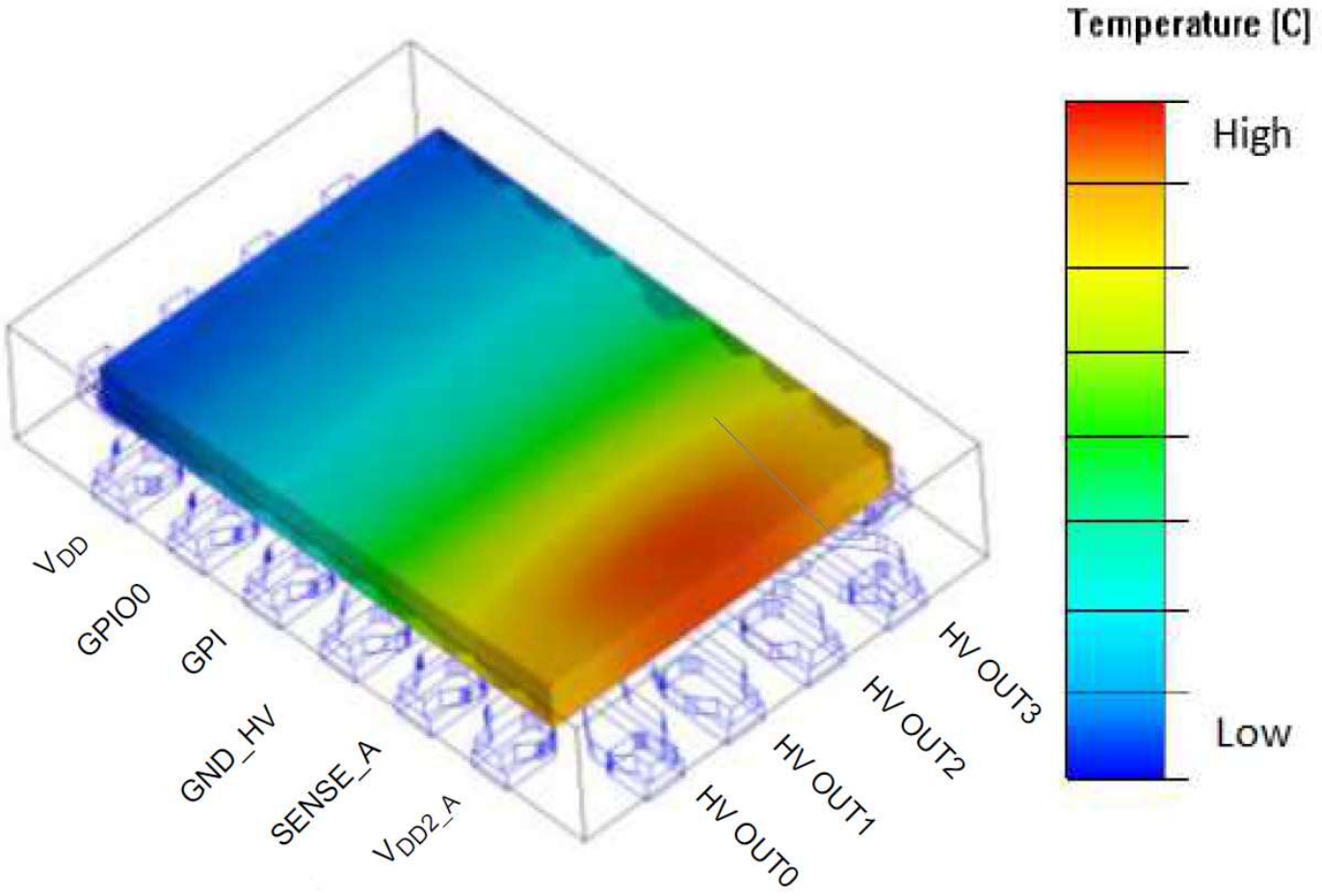


Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020. More information can be found at www.jedec.org.

Thermal Guidelines

Actual thermal characteristics will depend on number and position of vias, PCB type, copper layers, and other factors. Operating temperature range is from -40 °C to 85 °C. To guarantee reliable operation, the junction temperature of the SLG7RN45652 must not exceed 150 °C.



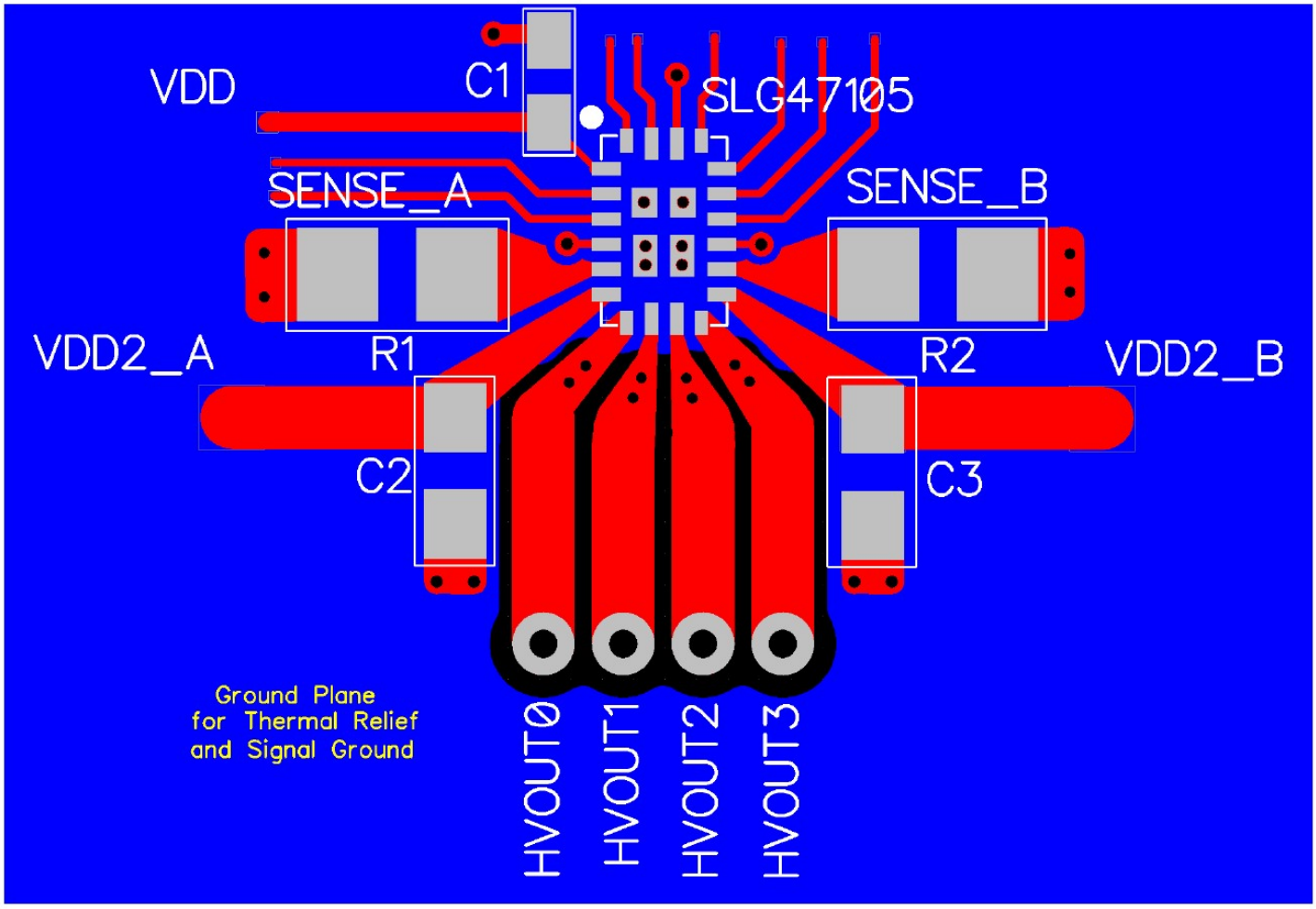
Layout consideration

PCB should have enough ground plane to dissipate heat. SLG7RN45652 has two additional pads which provide enhanced thermal dissipation. Thermal vias are used to transfer heat from chip to other layers of the PCB.
The sense resistors and power capacitors should be placed as close as possible to the chip for reducing parasitic parameters.

It's highly recommended to place low-ESR capacitor between VDD2_A, VDD2_B, and GND pin to keep input voltage stable and reduce ripple. This capacitor should be placed as close to the pins as possible. Also, the capacitor must have the low input impedance at the switching frequency. The recommended value of this capacitor is 1-10 µF for most applications. Motors with larger armature inductors require larger input capacitors.

Also, it's highly recommended to place 0.1 µF ceramic capacitor between VDD and GND.

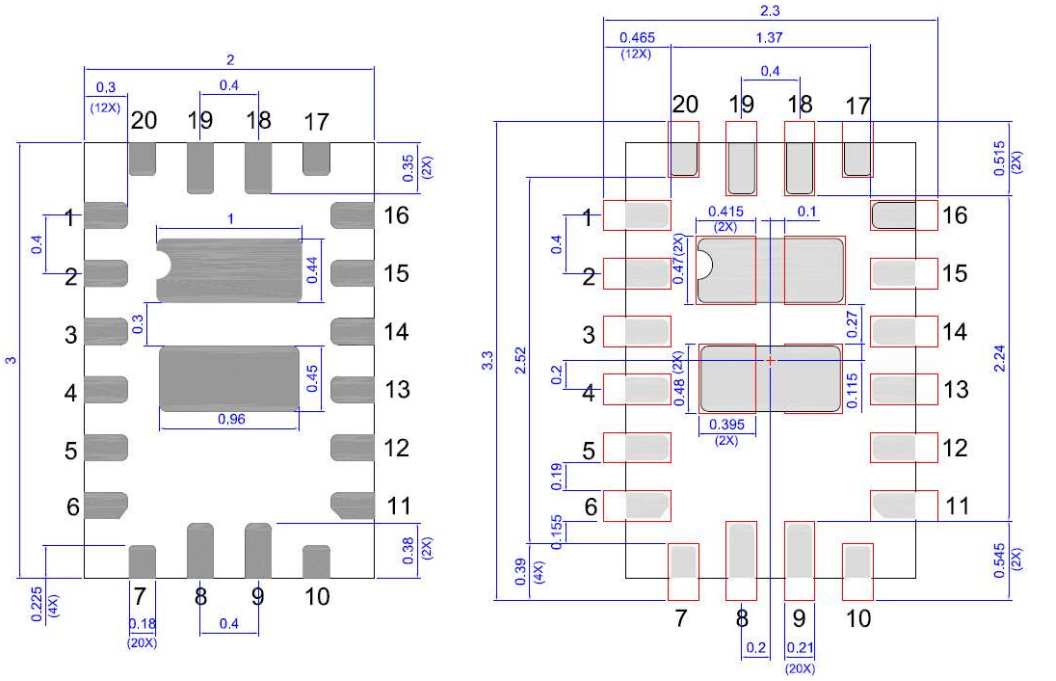
PCB Layout Example



Recommended Land Pattern

Expose Pad
(Package face down)

Recommended Landing Pattern
(Package face down)



Datasheet Revision History

Date	Version	Change
03/22/2022	0.10	New design for SLG47105V chip
03/31/2022	0.11	Updated Device Revision Table
05/06/2022	0.12	Updated Lock Status
05/12/2022	0.13	Updated Device Revision Table
05/12/2022	1.00	Production Release
06/30/2022	1.01	Updated design functionality. Updated VDD range

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.